Quasi-resonant AC/DC Converter Built-in 650 V GaN HEMT

BM3GQ1A2MUV-LBZ

General Description

This product guarantees long time support in industrial market.
BM3GQ1A2MUV-LBZ is a quasi-resonant AC/DC converter that provides an optimum system for all products which has an electrical outlet. Quasi-resonant operation enables soft switching and helps to keep the EMI low.
It can be designed easily because 650 V GaN HEMT and current detection resistor are integrated.
The burst operation reduces power consumption at light load.
BM3GQ1A2MUV-LBZ includes various protection functions, such as soft start function, burst operation function, over current protection per cycle, over voltage protection, overload protection.

Features

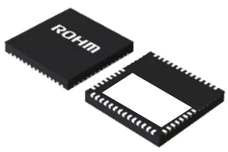
- Long Time Support Product for Industrial Applications
- Built-in 650 V GaN HEMT
- Quasi-resonant Type (Low EMI)
- Frequency Reduction Function
- Burst Operation at Light Load
- VCC UVLO (Under Voltage Lock Out)
- Over Current Protection Circuit per Cycle
- Soft Start Function
- ZT Trigger Mask Function
- ZT OVP (Over Voltage Protection)
- AC UVLO (Under Voltage Lock Out)
- X-capacitor Discharge Function

Key Specifications

- Operating Power Supply Voltage Range:
  - VCC: 7.4 V to 55 V
  - DRAIN: 650 V (Max)
- Normal Operating Current: 800 µA (Typ)
- Burst Mode Operating Current: 500 µA (Typ)
- Maximum Operating Frequency: 120 kHz (Typ)
- GaN HEMT ON Resistance: 150 mΩ (Typ)
- Operating Temperature: -40 °C to +125 °C

Package

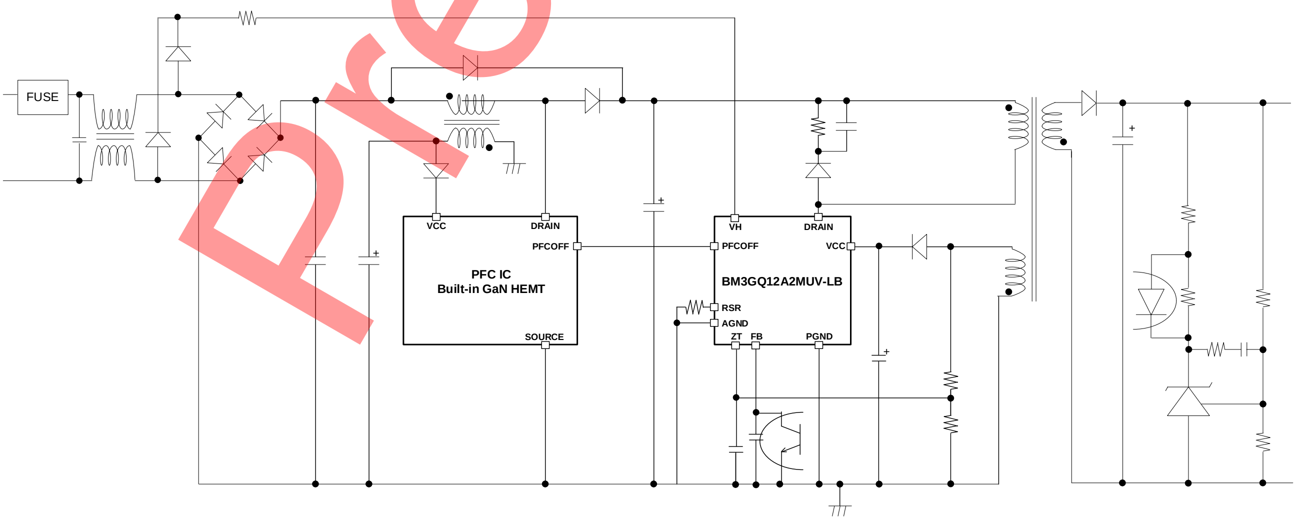
Package	W (Typ) x D (Typ) x H (Max)
VQFN41V8080K	8.0 mm x 8.0 mm x 1.0 mm pitch 0.5 mm



Applications

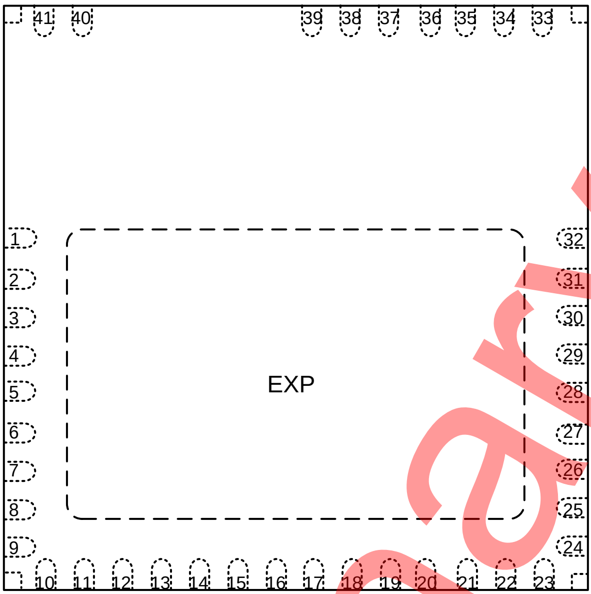
- Industrial Equipment, AC Adaptor, Household Appliances etc.

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

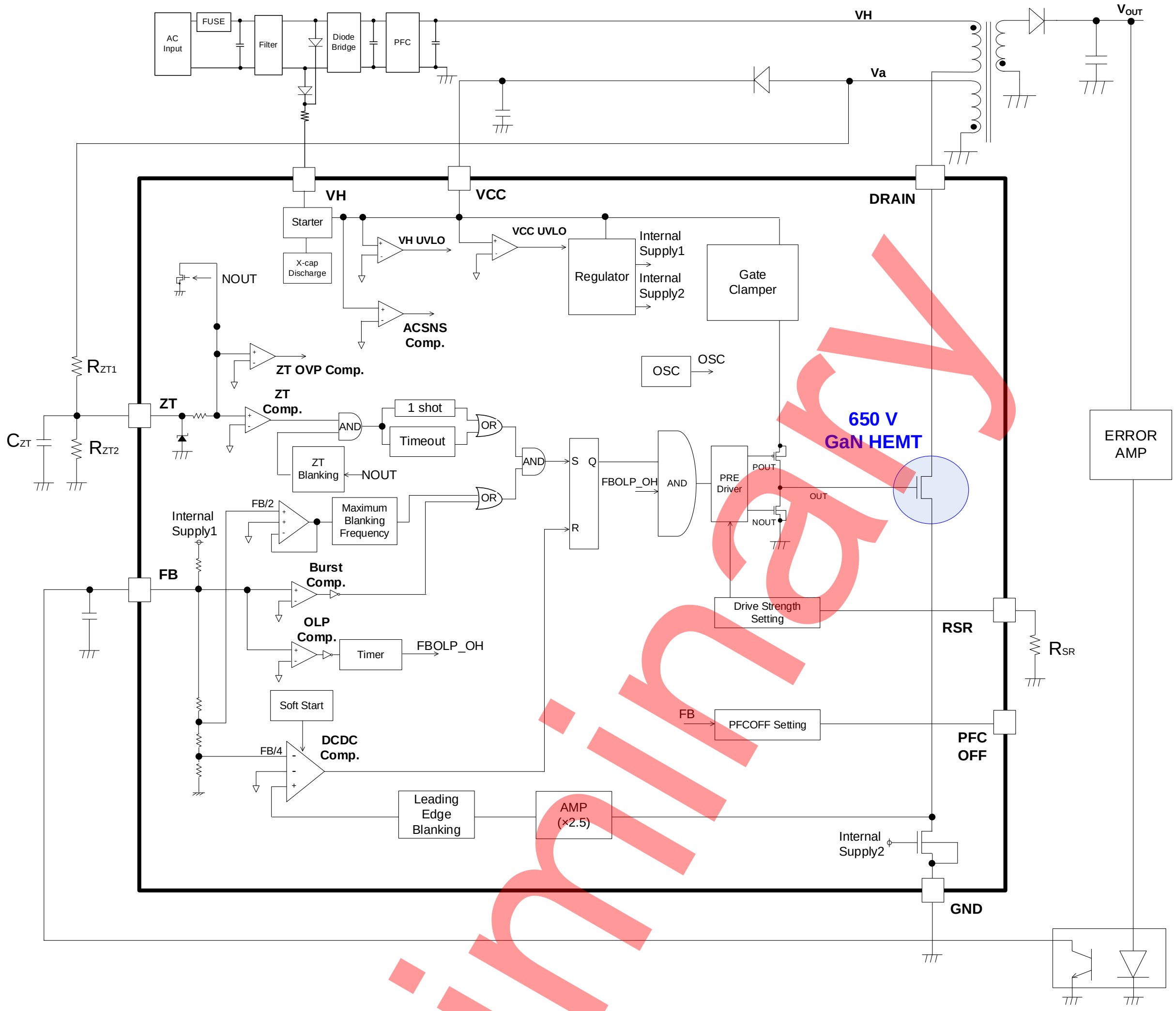


Pin Descriptions

Pin No.	Pin Name	I/O	Function
1-2, 17-22, 25-32	PGND	O	Power GND pin
3, 5, 7, 9, 10, 12, 14, 16, 23, 24	N.C.	-	Non connected pin(Note 1)
4	VCC	I	Power supply input pin
6	AGND	O	Analog GND pin(Note 2)
8	RSR	I	Gate drive strength adjustment pin
11	PFCOFF	O	PFCOFF signal output pin
13	FB	I	Feedback signal input pin
15	ZT	I	Zero current detection pin
33-39	DRAIN	I	GaN HEMT DRAIN pin
40, 41	VH	I	Starter current input / AC voltage monitor
-	EXP	O	Power GND pin(Note 2)
-	C.S	-	Corner pin(Note 3)
-	C.N.C	-	Non connection at corner(Note 1)

(Note 1) Do not connect to other pins.
(Note 2) Connect to the PGND pin on the PCB.
(Note 3) It is connected to the PGND pin internally, but do not connect to other pins on the PCB.

Block Diagram



Description of Blocks

1 Startup Circuit

This IC has a built-in startup circuit. It achieves low standby power and high-speed startup.
When AC input voltage is applied, the startup current is charged to the VCC pin from the VH pin though the startup circuit. The charge is stopped after the VCC pin voltage rises and VCC UVLO is released.

1.1 AC UVLO (Under Voltage Lock Out)

The AC voltage occurs at the VH pin when input power supply is applied.
The switching operation does not start until the peak voltage of the VH pin becomes more than V_{INLVP} after the VCC pin voltage is charged to more than V_{UVLO1} through the startup circuit. When the VH pin peak voltage is more than V_{INLVP}, AC UVLO is released, and IC starts switching. If input power supply is stopped, the VH pin peak voltage becomes lower than V_{INLVP} for t_{INLVP}, the AC UVLO is detected, and IC stops switching.

1.2 X-capacitor Discharge Function

When the AC voltage is not detected any more for t_{INLVP} (such as the plug is pulled out), X-capacitor discharge function starts to operate. X-capacitor is discharged to GND through startup circuit.

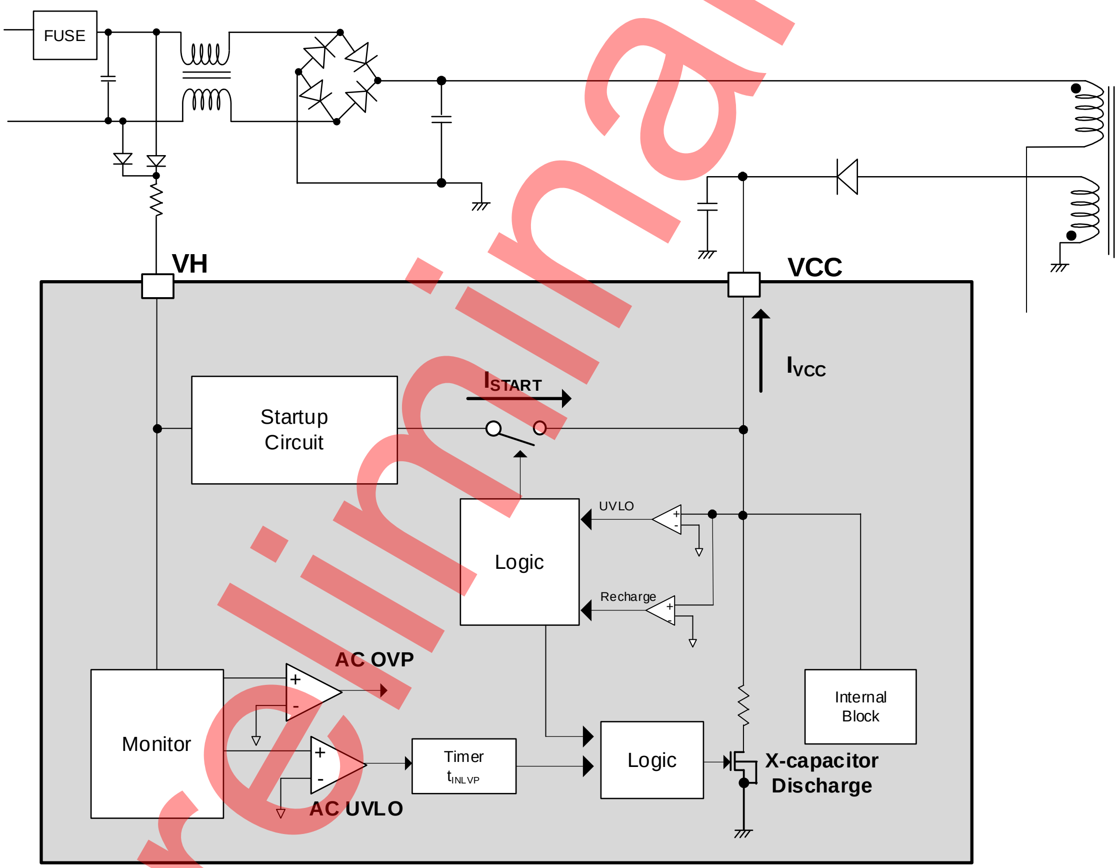


Figure 1. Block Diagram of the VH Pin and the VCC Pin

1 Startup Circuit – continued

The timing chart of the X-capacitor discharge operation is shown below.

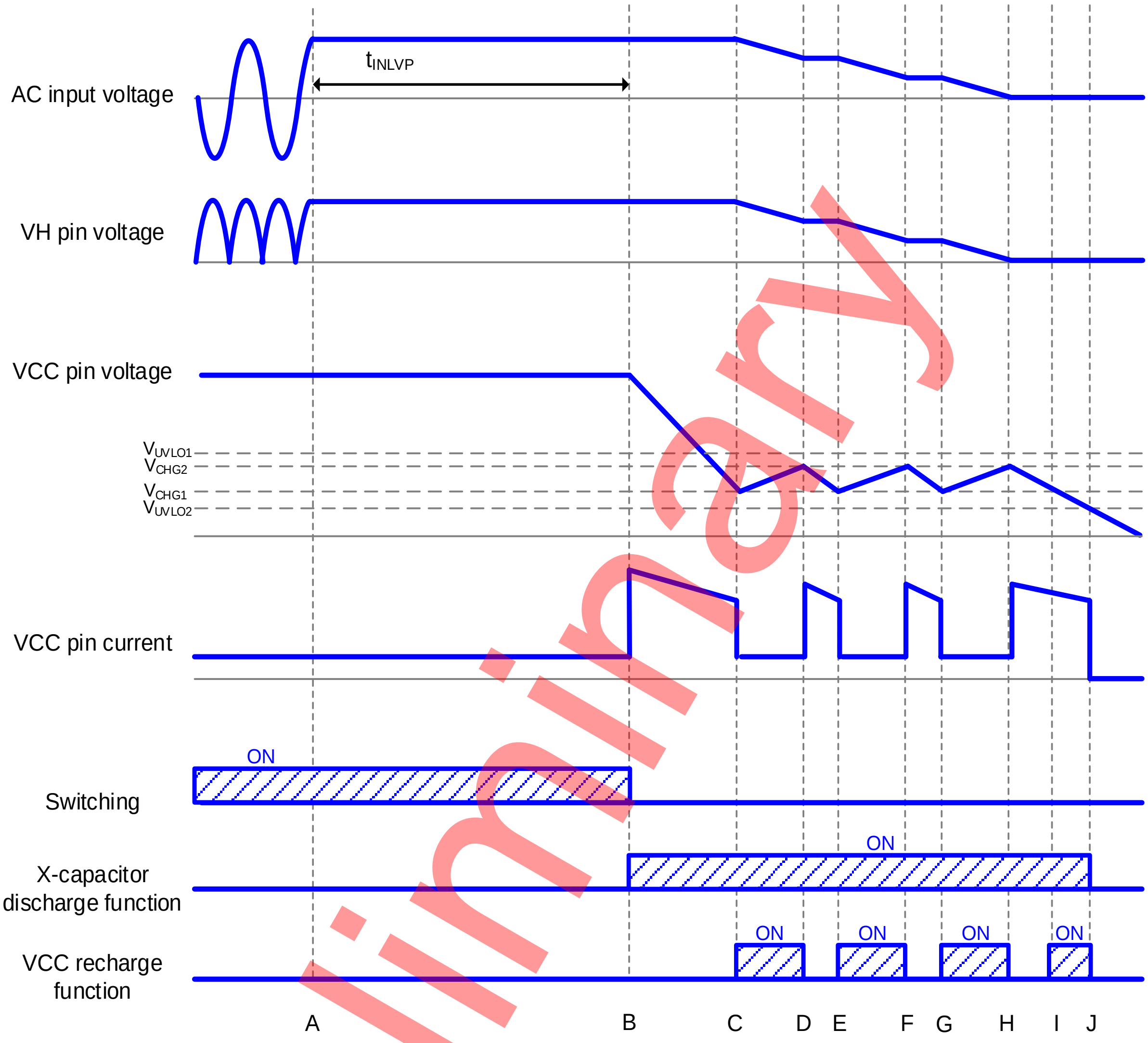


Figure 2. Timing Chart of X-capacitor Discharge Function

A: AC input voltage is turned OFF.
B: After t_{INLVP} from A, the switching stops and the X-capacitor discharge function operates.
C: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge operation starts.
D: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge operation stops.
E: Same as C.
F: Same as D.
G: Same as C.
H: Same as D.
I: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low VH pin voltage.
J: When the VCC pin voltage becomes less than V_{UVLO2}, VCC UVLO operates.

Description of Blocks – continued

2 Startup Sequence

The startup sequence is shown in Figure 3.

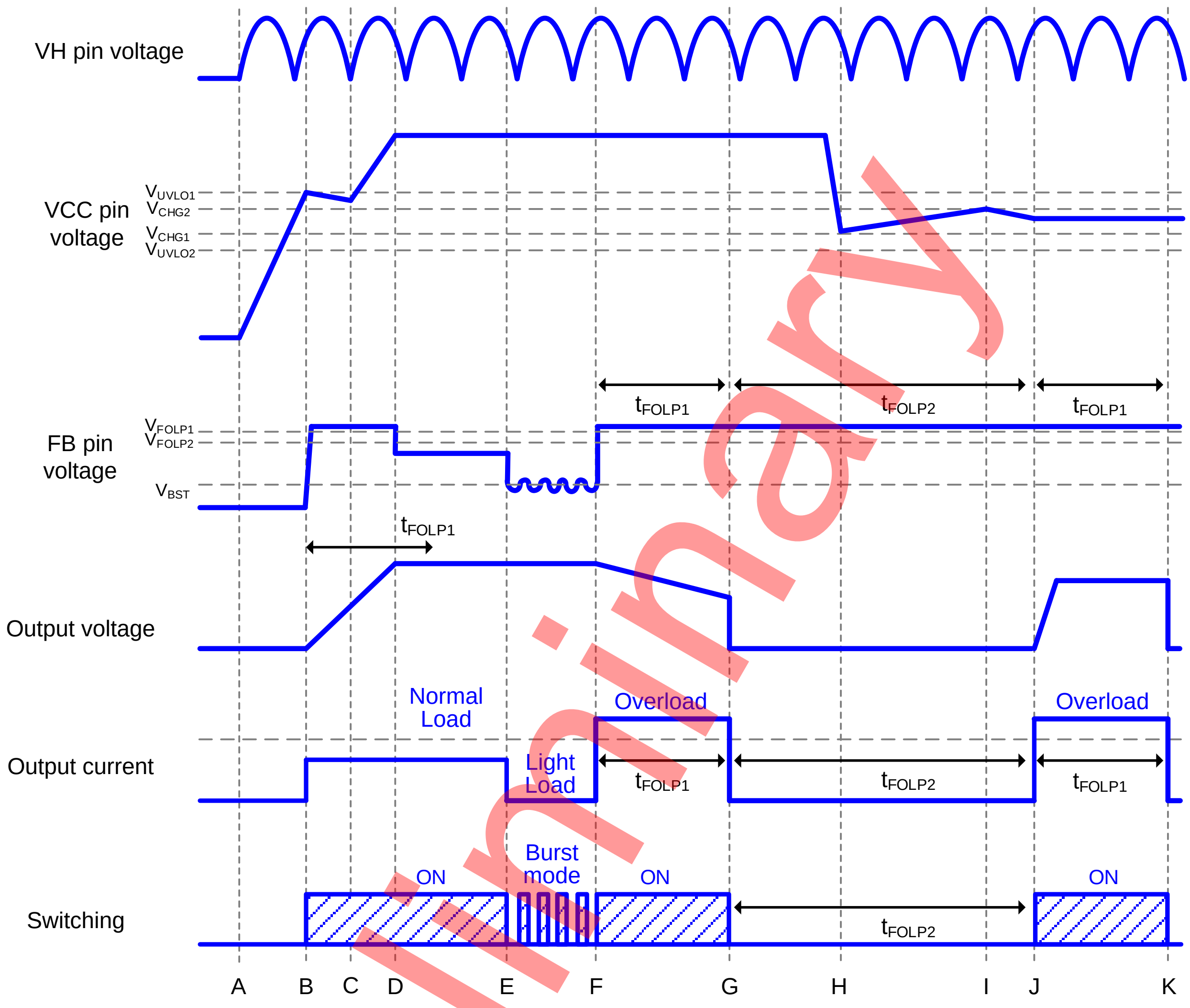


Figure 3. Startup Sequence Timing Chart

- A: The VH pin voltage is applied and the VCC pin voltage rises.
- B: If the VCC pin voltage becomes more than V_{UVLO1}, the IC starts to operate. And if the IC judges the other protection functions as normal condition, it starts the switching operation. The soft start function limits the over current detection current to prevent overshoot on output voltage and current rising. When the switching operation starts, the output voltage rises.
- C: Until the output voltage becomes a constant value or more from startup, the VCC pin voltage drops by the VCC pin current consumption.
- D: It is necessary to set the output capacitor to ensure the output voltage rises to targeted value within t_{FOLP1}.
- E: At light load, the burst operation starts to reduce the power consumption if the FB pin voltage becomes less than V_{BST}.
- F: When the FB pin voltage becomes more than V_{FOLP1}, the IC starts the overload operation.
- G: When the condition that the FB pin voltage becomes more than V_{FOLP1} for t_{FOLP1}, the switching stops for t_{FOLP2} period by FB OLP. If the FB pin voltage becomes less than V_{FOLP2}, FB OLP detect timer (t_{FOLP1}) is reset.
- H: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates.
- I: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge function stops operating.
- J: After t_{FOLP2} period from G, the switching operation restarts by soft start operation.
- K: Same as G.

Description of Blocks – continued

3 VCC Pin Protection Function

This IC has the internal protection functions at the VCC pin as shown below.

3.1 VCC UVLO (Under Voltage Lock Out)

This is auto restart comparator with a voltage hysteresis.

3.2 VCC Recharge Function

If the VCC pin voltage drops to less than V_{CHG1} after once the VCC pin becomes more than V_{UVLO1} and the IC starts to operate, the VCC recharge function operates. At this time, the VCC pin is recharged from the VH pin through the startup circuit. When the VCC pin voltage becomes more than V_{CHG2}, this recharge is stopped.

4 DC/DC Converter Function

BM3GQ1A2MUV-LBZ uses PFM (Pulse Frequency Modulation) mode control. The FB pin, the ZT pin are monitored to provide an optimized DC/DC system. GaN HEMT ON width (turn OFF) is controlled by the FB pin, and the OFF width (turn ON) is controlled by the ZT pin.

4.1 Determination of ON Width (Turn OFF)

ON width is controlled by the FB pin. It is determined by comparing the FB pin voltage with the sense voltage generated by DRAIN current. In addition, the comparator level is changed by FB pin voltage, as shown in Figure 4. I_{LIM1} and I_{LIM2} value changes depending on the VH pin peak voltage. (refer to PFCOFF function)

mode 1: Burst operation
mode 2: Frequency reduction operation
mode 3: Maximum frequency operation
mode 4: Overload operation (switching operation is stopped when overload is detected)

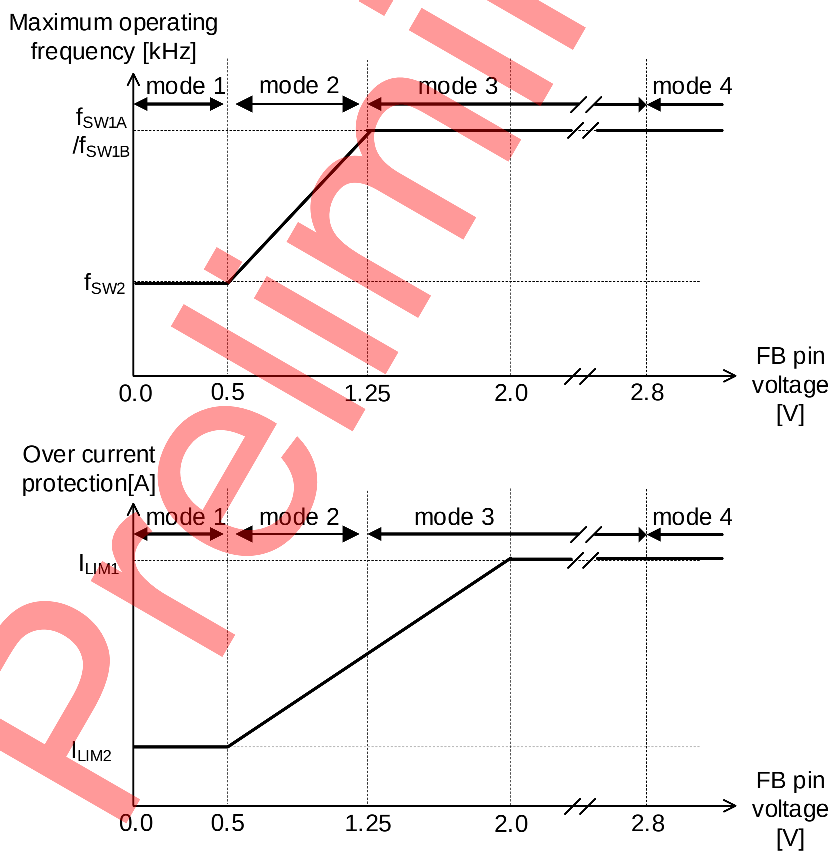


Figure 4. State Transition of Switching Frequency

4 DC/DC Converter Function – continued

4.2 L.E.B. (Leading Edge Blanking) Function

When the GaN HEMT is turned ON, surge current occurs at each capacitor component and drive current. Therefore, when the DRAIN pin Current rises temporarily, detection errors may occur in the over current protection circuit. To prevent detection errors, BM3GQ1A2MUV-LBZ has the L.E.B. function. This function masks the over current detection circuit for t_{LEB} after GaN HEMT turns ON.

4.3 Determination of OFF Width (Turn ON)

The OFF width is controlled at the ZT pin. While switching is OFF, the power stored in the coil is supplied to the secondary side output capacitor. When this process ends, there is no more current flowing to the secondary side, so the DRAIN pin voltage of GaN HEMT drops. Consequently, the voltage on the auxiliary coil side also drops. A voltage that was resistance-divided by R_{ZT1} and R_{ZT2} is applied to the ZT pin. When this voltage level drops to V_{ZT1} or less, switching is turned ON by the ZT comparator. To detect zero current status at the ZT pin, time constants are generated using C_{ZT}, R_{ZT1}, and R_{ZT2} (refer to block diagram). Additionally, there are also the ZT pin trigger mask and the ZT pin trigger timeout function in this IC.

4.4 ZT Trigger Mask Function

When GaN HEMT turns OFF, noise may occur at the ZT pin. At this time, the ZT comparator is masked for the t_{ZTMASK} to prevent the detection error of ZT comparator (Figure 5).

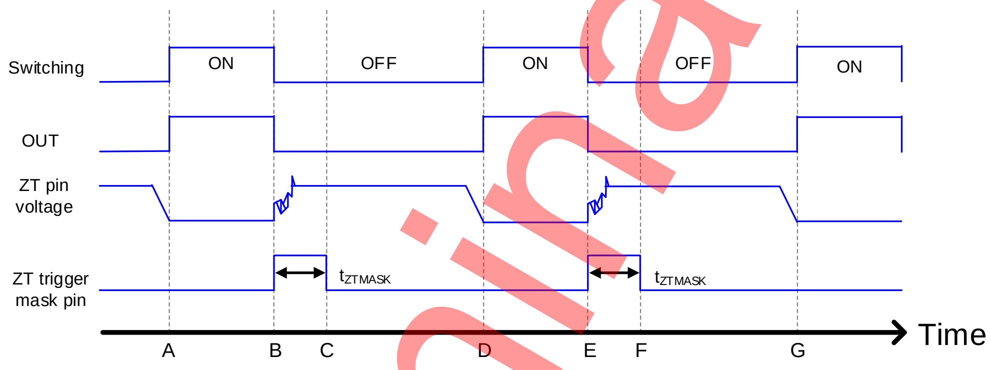


Figure 5. ZT Trigger Mask Function

A: Switch turns ON.
B: Switch turns OFF.
C: Because noise occurs at the ZT pin, the ZT comparator is masked for t_{ZTMASK} after switch turns OFF.
D: Same as A.
E: Same as B.
F: Same as C.
G: Same as A.

4 DC/DC Converter Function – continued

4.5 ZT Pin Trigger Timeout Function

ZT Pin Trigger Timeout Function 1

When the ZT pin voltage is not higher than V_{ZT2} during t_{ZTOUT1} because of the decrease of output voltage or the shorted the ZT pin such as at startup, the switch is forced to turn ON.

ZT Pin Trigger Timeout Function 2

After the ZT comparator detects the bottom, the switch is forced to turn ON when the next bottom is not detected within t_{ZTOUT2}. After the ZT comparator detected signal once, this function operates. For that, it does not operate at startup or at low output voltage. This function is for the case that IC is not able to detect bottom by decreasing auxiliary winding voltage.

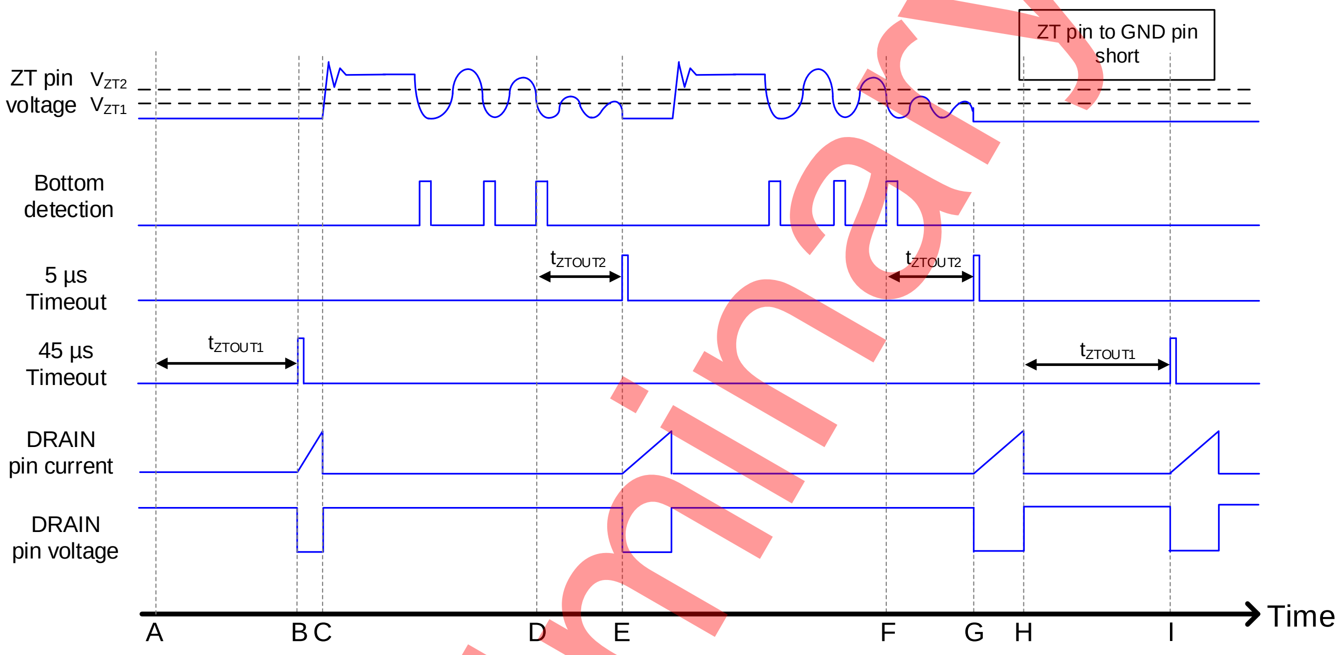


Figure 6. ZT Pin Trigger Timeout Function

A: At startup, the IC starts to operate by the ZT pin trigger timeout function1 because of the ZT pin voltage is 0 V.
B: Switch turns ON after t_{ZTOUT1} by the ZT pin trigger timeout function 1.
C: Switch turns OFF.
D: The bottom is detected and the ZT pin voltage drops to lower than V_{ZT2}.
E: Switch turns ON after t_{ZTOUT2} from D by the ZT pin trigger timeout function 2.
F: Same as D.
G: Same as E.
H: The ZT pin is shorted to GND.
I: Same as B.

Description of Blocks – continued

5 Soft Start Function

Normally, rush current occurs while AC power supply is applied. BM3GQ1A2MUV-LBZ includes a soft start function to prevent the overshoot on output voltage and abnormal current during startup. Soft start function performs the following operation after startup (Figure 7).

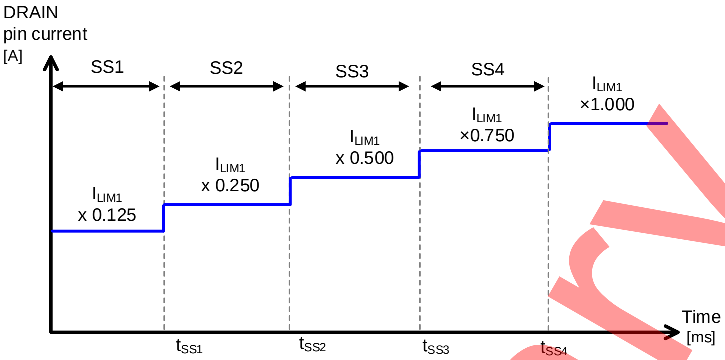


Figure 7. Soft Start Function

6 FB OLP (Over Load Protection)

The overload protection function operates in auto restart mode. This function monitors the overload status of the secondary output current at the FB pin and stops the switching when the overload status is detected. During overload status, current no longer flows to the opto-coupler, so the FB pin voltage rises. When the FB pin voltage keeps being over V_{FOLP1} for t_{FOLP1}, the switching operation is stopped by the overload protection function for t_{FOLP2}. If the FB pin voltage drops to lower than V_{FOLP2} within t_{FOLP1} after once it exceeds V_{FOLP1}, the overload protection timer is reset.
At startup, the FB pin voltage is pulled up to the internal voltage by a pull up resistor, so operation starts from V_{FOLP1} or above. Therefore, it is necessary for the design to set the FB pin voltage at V_{FOLP2} or less within t_{FOLP1}. In other words, the startup time of the secondary output voltage must be set to within t_{FOLP1} after the IC starts.

7 ZT OVP (Over Voltage Protection) Function

ZT OVP (over voltage protection) function operates in auto restart mode. When the ZT pin voltage keeps being over V_{ZTL} for t_{MASK}, the switching operation is stopped by the over voltage protection circuit for t_{ZTOVP}.

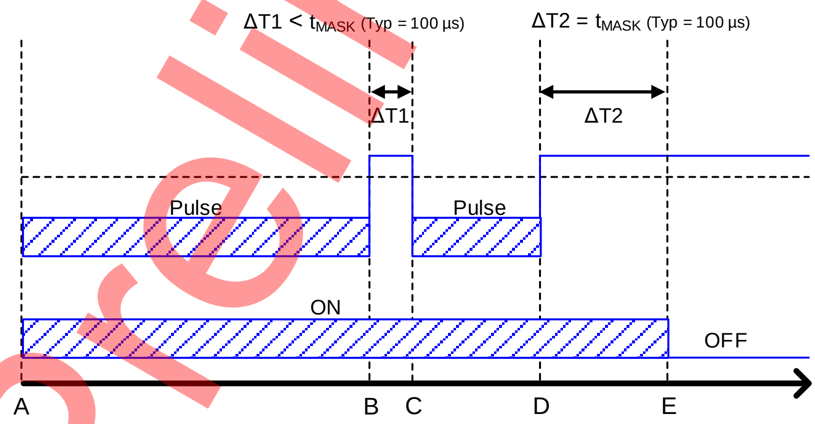


Figure 8. ZT OVP Function

A: Switching starts and the ZT pin starts pulse operation.
B: The ZT pin voltage becomes more than V_{ZTL}.
C: Reset to the normal operations when the ZT pin voltage becomes less than V_{ZTL} within t_{MASK}.
D: The ZT pin voltage becomes more than V_{ZTL}.
E: Switching stops when the ZT pin voltage keeps being over than V_{ZTL} for t_{MASK}.

Description of Blocks – continued

8 Thermal Shutdown Function

Thermal shutdown function is auto restart type. Thermal shutdown function is worked when the junction temperature becomes more than T_{SD1} for t_{TSD}, switching is stopped. Switching restart when the junction temperature becomes less than T_{SD2}.

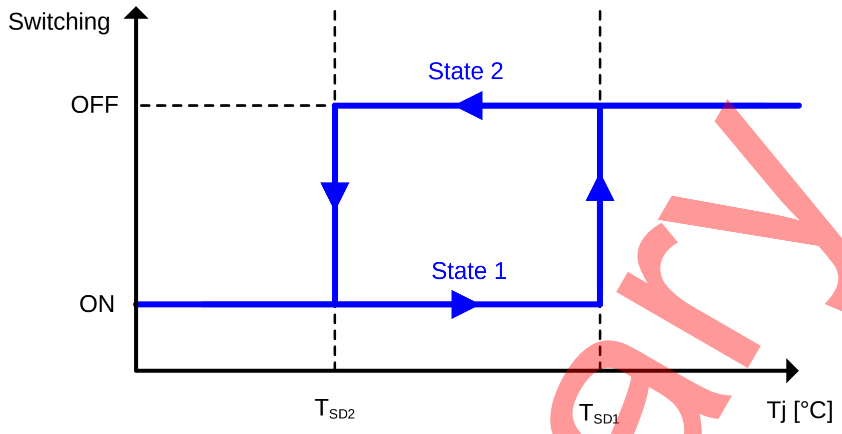


Figure 9. Thermal Shutdown Function

9 Drive Strength Setting Function

Generally, there is a tradeoff between efficiency and EMI. A higher switching slew rate reduces their switching loss, in the other hand, it also increases their switching noise. By adjusting a resistor between the RSR pin and the GND pin (RSR), the Turn OFF DRAIN slew rate (SR_{OFF}) can be selected within the range shown in the following figure 10.
It allows users to optimize the switching speed according to specific application, such as an EMI filter space, PCB layout, etc.

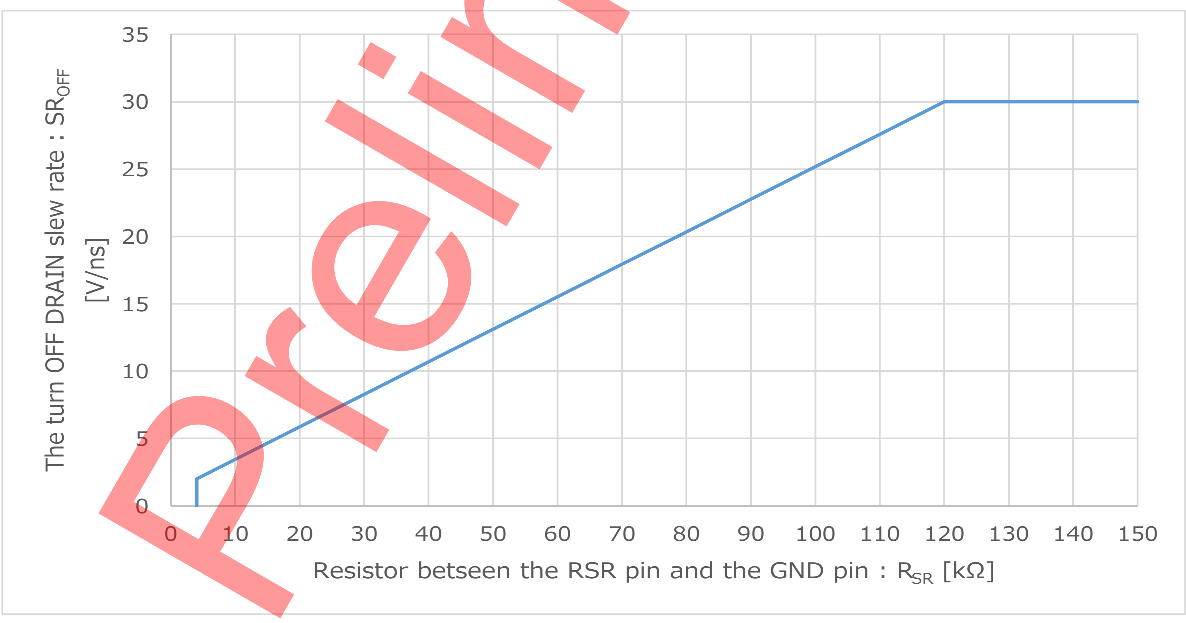


Figure 10. The Turn OFF DRAIN Slew Rate SR_{OFF} vs Resistor between the RSR Pin and the GND Pin R_{SR}

Description of Blocks – continued

10 PFCOFF Function

BM3GQ1A2MUV-LBZ has PFCOFF function to improve efficiency at light load. IO equivalence block diagram of the PFCOFF pin is shown in figure 11 and timing chart of the PFCOFF function is shown in figure 12. When PFCOFF switch state is ON, if the FB pin voltage continues to be more than V_{PFCONX} for t_{PFCOFF}, PFCOFF switch state becomes OFF. V_{PFCONX} changes to V_{PFCON1}, V_{PFCON2}, V_{PFCON3}, V_{PFCON4}, or V_{PFCON5} depending on the VH pin peak voltage. On the other hand, when PFCOFF switch state is OFF, if the FB pin voltage continues to be less than V_{PFCOFF} for t_{PFCOFF}, PFCOFF switch state becomes ON.

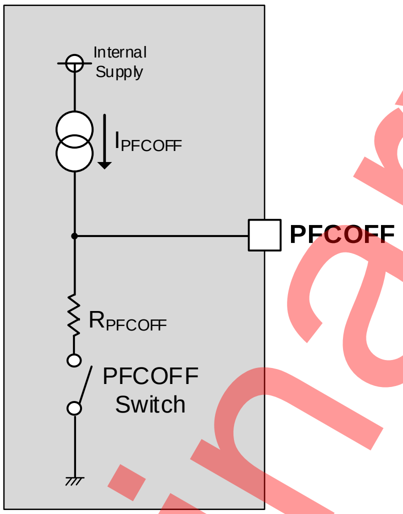


Figure 11. IO Equivalence Block Diagram of the PFCOFF Pin

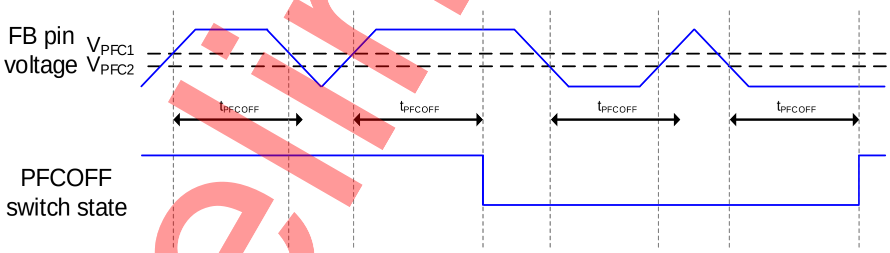


Figure 12. Timing Chart of the PFCOFF Function

When PFCOFF switch state is ON, the values of I_{LIM1} and I_{LIM2} change depending on the VH pin peak voltage.
When PFCOFF switch state is OFF, the values I_{LIM1} and I_{LIM2} are fixed at I_{LIM1G} and I_{LIM2G} respectively. However, when the PFCOFF pin is shorted to the AGND pin, the values I_{LIM1} and I_{LIM2} are constantly fixed at I_{LIM1G} and I_{LIM2G} respectively. Also, when the PFCOFF pin is pulled down with 47 kΩ resistance, the values of I_{LIM1} and I_{LIM2} constantly change depending on the VH pin peak voltage.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +57	V	VCC pin
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +6.5	V	FB pin, ZT pin, PFCOFF pin, RSR pin
Maximum Applied Voltage 3	V_{MAX3A}	-0.3 to +650	V	DRAIN pin voltage, VH pin voltage
	V_{MAX3B}	-0.3 to +800	V	DRAIN pin pulse voltage (t_{PULSE} < 1μs)*(Note 1)*
DRAIN Pin Current (RMS)	$I_{D(RMS)}$	T.B.D.	A	DRAIN pin RMS current
DRAIN Pin Current (PULSE)	$I_{D(PULSE)}$	T.B.D.	A	DRAIN pin pulse current (t_{PULSE} < 1μs)*(Note 1)*
ZT Pin Maximum Current	I_{SZT}	±3.0	mA	
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
VQFN41V8080K				
Junction to Ambient	θ_{JA}	T.B.D.	T.B.D.	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	T.B.D.	T.B.D.	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating Power Supply Voltage Range 1	V_{CC}	7.4	15.0	55.0	V	VCC pin voltage
Operating Power Supply Voltage Range 2	V_{DRAIN}	-0.3	-	+650	V	DRAIN pin voltage
RSR Pulled Down Resistance Range	R_{SR}	6.8	-	-	kΩ	

Electrical Characteristics (Unless otherwise specified V_{CC} = 15 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Power Block]						
Drain Breakdown Voltage	$V_{(BR)DSS1}$	650	-	-	V	DRAIN pin voltage
	$V_{(BR)DSS2}$	800	-	-	V	DRAIN pin voltage (t_{PULSE} < 1μs)
DRAIN Leak Current	I_{DSS}	-	-	10	μA	V_D = 650 V, V_{FB} = 0 V
GaN HEMT ON Resistance	R_{ON1}	-	150	195	mΩ	I_D = 1 A, Ta=25 °C
	R_{ON2}	-	360	-	mΩ	I_D = 1 A, Ta=150 °C
Sense FET ON Resistance	R_{ON3}	35	50	65	mΩ	I_D = 1 A, Ta=25 °C
	R_{ON4}	-	90	-	mΩ	I_D = 1 A, Ta=150 °C
DRAIN to PGND Pin ON Resistance	R_{ON5}	-	200	260	mΩ	R_{ON5} = R_{ON1} + R_{ON3}
	R_{ON6}	-	450	-	mΩ	R_{ON6} = R_{ON2} + R_{ON4}
[Startup Circuit]						
Startup Current 1	I_{START1}	0.1	0.3	1.0	mA	V_{CC} = 0 V
Startup Current 2	I_{START2}	1.0	3.0	6.0	mA	V_{CC} = 6 V
OFF Current	I_{START3}	-	10	25	μA	
Startup Current Switching Voltage	I_{SC}	0.45	0.75	1.05	V	
AC UVLO Voltage	V_{INLVP}	75	85	95	V	VH peak voltage
AC UVLO Stop Timer	t_{INLVP}	90	128	166	ms	
[Operating Current]						
Standby Current	I_{STB}	-	80	120	μA	VCC = 6 V
Normal Operating Current	I_{ON1}	-	800	1600	μA	FB pin voltage = 2.0 V (at pulse operation)
Burst Operating Current	I_{ON2}	-	500	750	μA	FB pin voltage = 0.0 V (at burst operation)
[VCC Pin Protection Function]						
VCC UVLO Voltage 1	V_{UVLO1}	8.90	9.50	10.10	V	VCC pin voltage rising
VCC UVLO Voltage 2	V_{UVLO2}	6.10	6.50	6.90	V	VCC pin voltage falling
VCC UVLO Hysteresis Voltage	V_{UVLO3}	-	3.00	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2}
VCC Recharge Start Voltage	V_{CHG1}	6.60	7.00	7.40	V	VCC pin voltage falling
VCC Recharge Stop Voltage	V_{CHG2}	7.50	8.00	8.50	V	VCC pin voltage rising
VCC Recharge Hysteresis Voltage	V_{CHG3}	-	1.00	-	V	V_{CHG3} = V_{CHG2} - V_{CHG1}
Thermal Shut Down Temperature 1	T_{SD1}	150	175	200	°C	Temperature rising(Note 6)
Thermal Shut Down Temperature 2	T_{SD2}	-	100	-	°C	Temperature falling(Note 6)
Thermal Shut Down Hysteresis	T_{SD3}	-	75	-	°C	
Thermal Shut Down Detect Timer	t_{TSD}	50	100	150	μs	

(Note 6) Over temperature protection operates over maximum junction temperature. This IC cannot guarantee for the thermal destruction in case of the operation over maximum junction temperature, always operate at maximum junction temperature or less.

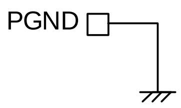
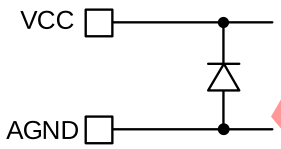
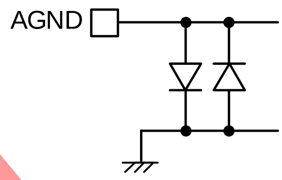
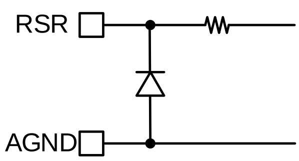
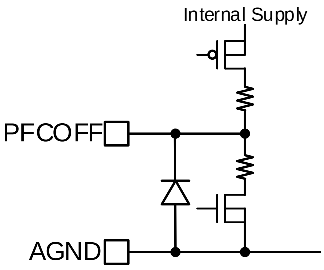
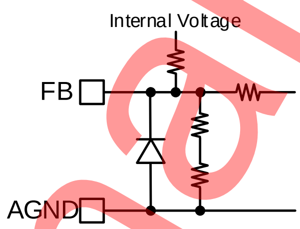
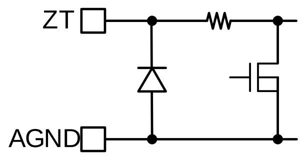
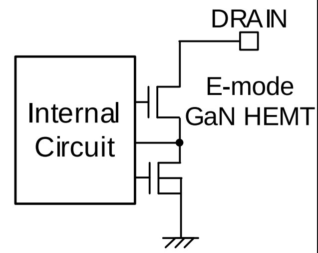
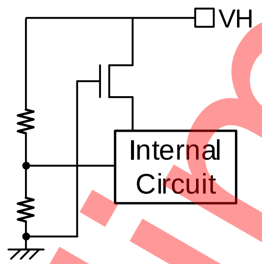
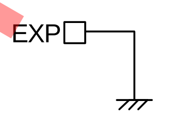
Electrical Characteristics (Unless otherwise specified V_{CC} = 15 V, Ta = 25 °C) – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[DC/DC Converter Block (Turn OFF)]						
FB Pin Pull up Resistance	R_{FB}	21	30	39	kΩ	
Over Current Detection Current 1 A	I_{LIM1A}	5.700	6.000	6.300	A	FB pin voltage = 2.0 V VH peak < 127 V
Over Current Detection Current 2 A	I_{LIM2A}	1.350	1.500	1.650	A	FB pin voltage = 0.5 V VH peak < 127 V
Over Current Detection Current 1 B	I_{LIM1B}	4.692	5.100	5.508	A	FB pin voltage = 2.0 V 127 V < VH peak < 170 V
Over Current Detection Current 2 B	I_{LIM2B}	1.122	1.275	1.428	A	FB pin voltage = 0.5 V 127 V < VH peak < 170 V
Over Current Detection Current 1 C	I_{LIM1C}	4.140	4.500	4.860	A	FB pin voltage = 2.0 V 170 V < VH peak < 212 V
Over Current Detection Current 2 C	I_{LIM2C}	0.990	1.125	1.260	A	FB pin voltage = 0.5 V 170 V < VH peak < 212 V
Over Current Detection Current 1 D	I_{LIM1D}	3.864	4.200	4.536	A	FB pin voltage = 2.0 V 212 V < VH peak < 255 V
Over Current Detection Current 2 D	I_{LIM2D}	0.924	1.050	1.176	A	FB pin voltage = 0.5 V 212 V < VH peak < 255 V
Over Current Detection Current 1 E	I_{LIM1E}	3.698	4.020	4.342	A	FB pin voltage = 2.0 V 255 V < VH peak < 297 V
Over Current Detection Current 2 E	I_{LIM2E}	0.884	1.005	1.126	A	FB pin voltage = 0.5 V 255 V < VH peak < 297 V
Over Current Detection Current 1 F	I_{LIM1F}	3.588	3.900	4.212	A	FB pin voltage = 2.0 V 297 V < VH peak < 339 V
Over Current Detection Current 2 F	I_{LIM2F}	0.858	0.975	1.092	A	FB pin voltage = 0.5 V 297 V < VH peak < 339 V
Over Current Detection Current 1 G	I_{LIM1G}	3.422	3.720	4.018	A	FB pin voltage = 2.0 V VH peak > 339 V
Over Current Detection Current 2 G	I_{LIM2G}	0.818	0.930	1.042	A	FB pin voltage = 0.5 V VH peak > 339 V
DRAIN Pin Leading Edge Blanking Time	t_{LEB}	-	180	-	ns	
Minimum ON Width	t_{MIN}	-	300	-	ns	
[DC/DC Converter Block]						
Maximum Operating Frequency 1	f_{SW1}	108	120	132	kHz	FB pin voltage = 2.0 V
Maximum Operating Frequency 2	f_{SW2}	22	35	48	kHz	FB pin voltage = 0.5 V
FB Pin Burst Voltage 1	V_{BST1}	0.300	0.350	0.400	V	FB pin voltage rising
FB Pin Burst Voltage 2	V_{BST2}	0.250	0.300	0.350	V	FB pin voltage falling
FB Pin Burst Hysteresis Voltage	V_{BST3}	-	0.050	-	V	
FB Pin Frequency Reduction Start Voltage	V_{FBSW1}	0.450	0.500	0.550	V	
FB Pin Frequency Reduction End Voltage	V_{FBSW2}	1.150	1.250	1.350	V	
ZT Pin Comparator Voltage 1	V_{ZT1}	30	60	90	mV	ZT pin voltage falling
ZT Pin Comparator Voltage 2	V_{ZT2}	60	90	120	mV	ZT pin voltage rising
ZT Pin Comparator Hysteresis Voltage	V_{ZT3}	-	30	-	mV	$V_{ZT3} = V_{ZT2} - V_{ZT1}$
ZT Pin Trigger Mask Time	t_{ZTMASK}	0.25	0.60	0.95	µs	
ZT Pin Trigger Timeout Period 1	t_{ZTOUT1}	10.5	15.0	19.5	µs	
ZT Pin Trigger Timeout Period 2	t_{ZTOUT2}	3.5	5.0	6.5	µs	
Maximum ON Time	t_{ONMAX}	31.5	45.0	58.5	µs	

Electrical Characteristics (Unless otherwise specified V_{CC} = 15 V, Ta = 25 °C) – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[DC/DC Protection Functions]						
Soft Start Time 1	t_{SS1}	0.70	1.00	1.30	ms	
Soft Start Time 2	t_{SS2}	1.40	2.00	2.60	ms	
Soft Start Time 3	t_{SS3}	2.80	4.00	5.20	ms	
Soft Start Time 4	t_{SS4}	5.60	8.00	10.40	ms	
FB OLP Voltage 1	V_{FOLP1}	2.500	2.800	3.100	V	FB pin voltage rising
FB OLP Voltage 2	V_{FOLP2}	2.300	2.600	2.900	V	FB pin voltage falling
FB OLP Detect Timer	t_{FOLP1}	52	64	76	ms	
FB OLP Release Timer	t_{FOLP2}	416	512	608	ms	
ZT OVP Voltage	V_{ZTOVP}	5.1	5.5	5.9	V	
ZT OVP Detect Timer	t_{MASK}	50	100	150	µs	
ZT OVP Release Timer	t_{ZTOVP}	416	512	608	ms	
[PFCOFF Functions]						
PFCON FB Voltage 1	V_{PFCON1}	0.77	0.82	0.87	V	VH peak < 127 V
PFCON FB Voltage 2	V_{PFCON2}	0.85	0.90	0.95	V	127 V < VH peak < 170 V
PFCON FB Voltage 3	V_{PFCON3}	0.92	0.97	1.02	V	170 V < VH peak < 212 V
PFCON FB Voltage 4	V_{PFCON4}	0.95	1.01	1.07	V	212 V < VH peak < 297 V
PFCON FB Voltage 5	V_{PFCON5}	0.99	1.05	1.11	V	VH peak > 297 V
PFCOFF FB Voltage	V_{PFCOFF}	0.79	0.85	0.91	V	
PFCOFF Timer	t_{PFCOFF}	832	1024	1216	ms	
PFCOFF Output Current	I_{PFCOFF}	12.7	15.0	17.3	µA	
PFCOFF Pin Pull Down Resistance	R_{PFCOFF}	37.6	47.0	56.4	kΩ	
[RSR Functions]						
RSR Output Current	I_{RSR}	9.5	10.0	10.5	µA	
RSR Short Protection Voltage	V_{RSR}	20	40	60	mV	
Turn OFF Slew Rate 1	SR_1	-	3	-	V/ns	R_{SR} = 6.8 kΩ
Turn OFF Slew Rate 2	SR_2	-	33	-	V/ns	R_{SR} = OPEN

I/O Equivalence Circuits

1, 2, 17-22, 25-32	PGND	3, 5, 7, 9, 10, 12, 14, 16, 23, 24	N.C.	4	VCC	6	AGND
		–					
8	RSR	11	PFCOFF	13	FB	15	ZT
							
33-39	DRAIN	40, 41	VH	-	EXP		
							

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

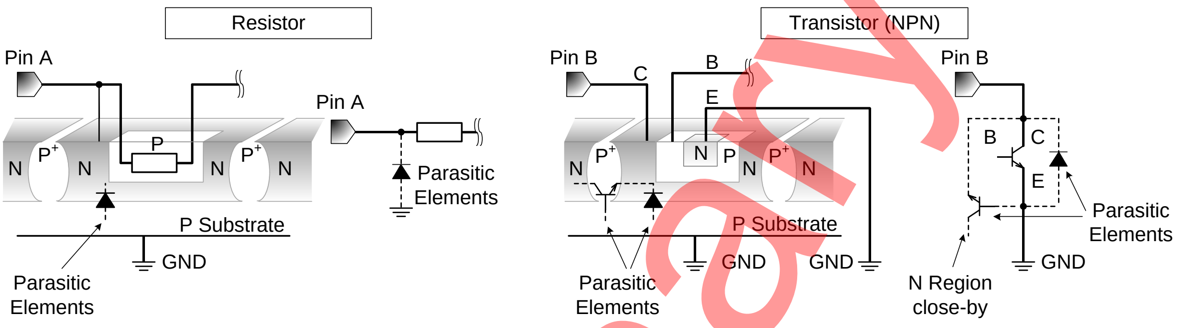


Figure 13. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn off power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

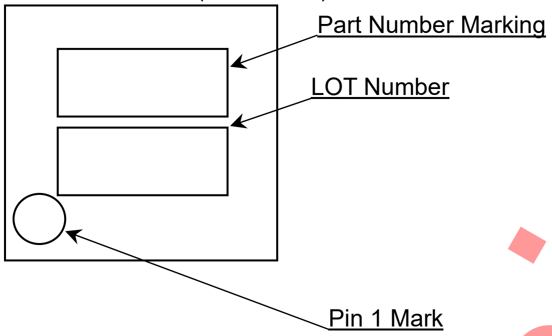
Ordering Information

B	M	3	G	Q	1	A	2	M	U	V	-	L	B	Z	E	2

G: Integrated GaN HEMT Q: Quasi-resonant AC/DC 1: f_{SW1} = 120 kHz A: With X-capacitor discharge 2: I_{LIM1A} = 6 A	Package MUV: VQFN41V8080K	Product Rank LB for Industrial applications Packaging and forming specification E2: Embossed tape and reel

Marking Diagram

VQFN41V8080K (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN41V8080K
T.B.D.	

Revision History

Date	Revision	Changes
31.Jul.2024	001	Target spec

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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