Half Bridge Power Stage IC Integrated 2ch 650 V GaN HEMT

BM4G005MUV-LBZ

Preliminary

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.
BM4G005MUV-LBZ is power stage IC which integrates driver, protections and two 650V enhancement -mode GaN HEMT. This IC provides an optimum solution for all electronics systems that requires high power density and efficiency.
By integrating the 650 V enhancement-mode GaN HEMT and silicon driver to ROHM's original package, parasitic inductance caused by a PCB and wire bonding is reduced significantly compared to traditional discrete solutions.
Owing to this, a high switching slew rate up to 150 V/ns can be achieved. On the other hand, adjustable gate drive strength contributes to low EMI, and various protections and other additional functions provide optimized cost, PCB size.
This IC is designed to adapt major exist controllers, so that it also can be used to replace the traditional discrete power switches, such as super junction MOSFET to achieve higher power or more compact PCB size.

Key Specifications

- Power Supply Voltage Range
  - VCC pin: 9.3 V to 25 V
  - BST pin referred to SW: 8.0 V to 25 V
  - BST pin: 683V(Max)
  - HD pin: 683 V (Max)
  - SW pin: -5.0V to +650 V (Max)
  - IN pin: -0.3 V to +33 V (Max)
- VCC Operating Current @ 500 kHz: TBD mA (Typ)
- VCC Quiescent Current: 210 µA (Typ)
- BST Quiescent Current: 120 µA (Typ)
- Allowable Input Switching Frequency: 1 MHz (Max)
- Turn-on Delay Time: 60 ns (Typ)
- Turn-off Delay Time: 60 ns (Typ)
- Operating Temperature Range: -40 °C to +105 °C
- GaN HEMT D-S ON State Resistance: 50 mΩ (Typ)

Package

Package	W (Typ) x D (Typ) x H (Max)
SQFN37V100K	10.0 mm x 10.0 mm x 1.0 mm pitch 0.65 mm

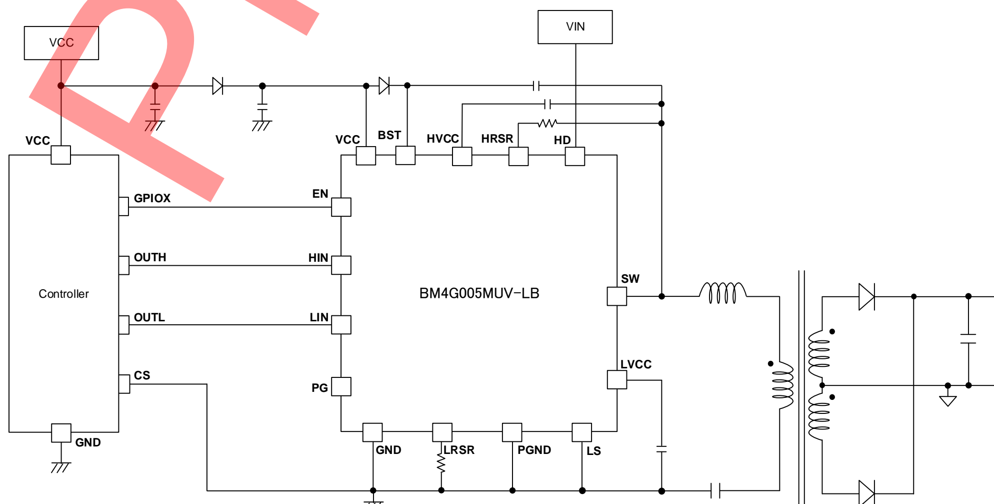
Features

- Wide Operating Range for VCC and IN Pin Voltage
- Low VCC Quiescent and Operating Current
- Low Propagation Delay
- High dv/dt Immunity
- High Precision LDO (LVCC/HVCC) for Gate Drive
- Adjustable Turn-on Gate Drive Strength
- Enable Signal Input
- Power Good Signal Output
- LVCC and HVCC UVLO Protection
- VCC UVLO Protection
- Thermal Shutdown Protection

Applications

- Power Supply by Bridge Topology such as Totem-pole PFC, LLC, Active Clamp Flyback, etc.

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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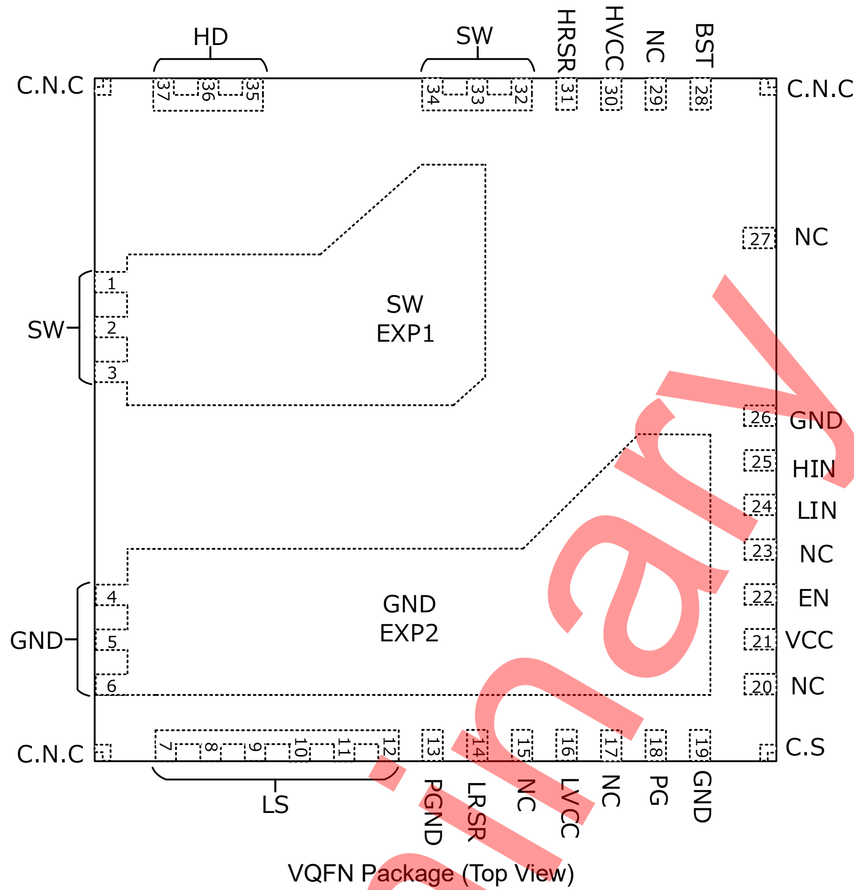
Pin Configuration



VQFN Package (Top View)

Preliminary

Pin Descriptions

Pin No.	Pin Name	I/O	Function
1,2,3 32,33,34,EXP1	SW	I/O	Half bridge output pin
4,5,6,19,26 EXP2	GND	O	Logic side GND pin
7,8,9,10,11,12	LS	O	Low side GaN HEMT SOURCE pin
13	PGND	O	Low side power GND pin
14	LRSR	I	Low side gate drive strength adjustment pin
15,17,20,23,27,29	N.C.	-	Non connection
16	LVCC	I/O	Low side driver power supply pin
18	PG	O	Power good signal output pin
21	VCC	I	Logic side power supply pin
22	EN	I	Enable signal input pin
24	LIN	I	Low side driver logic input pin
25	HIN	I	High side driver logic input pin
28	BST	O	Bootstrap diode anode connection pin
30	HVCC	I	High side driver power supply pin
31	HRSR	I	High side gate drive strength adjustment pin
-	C.S	-	Corner pin
-	C.N.C	-	Non connection at corner

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Block Diagram

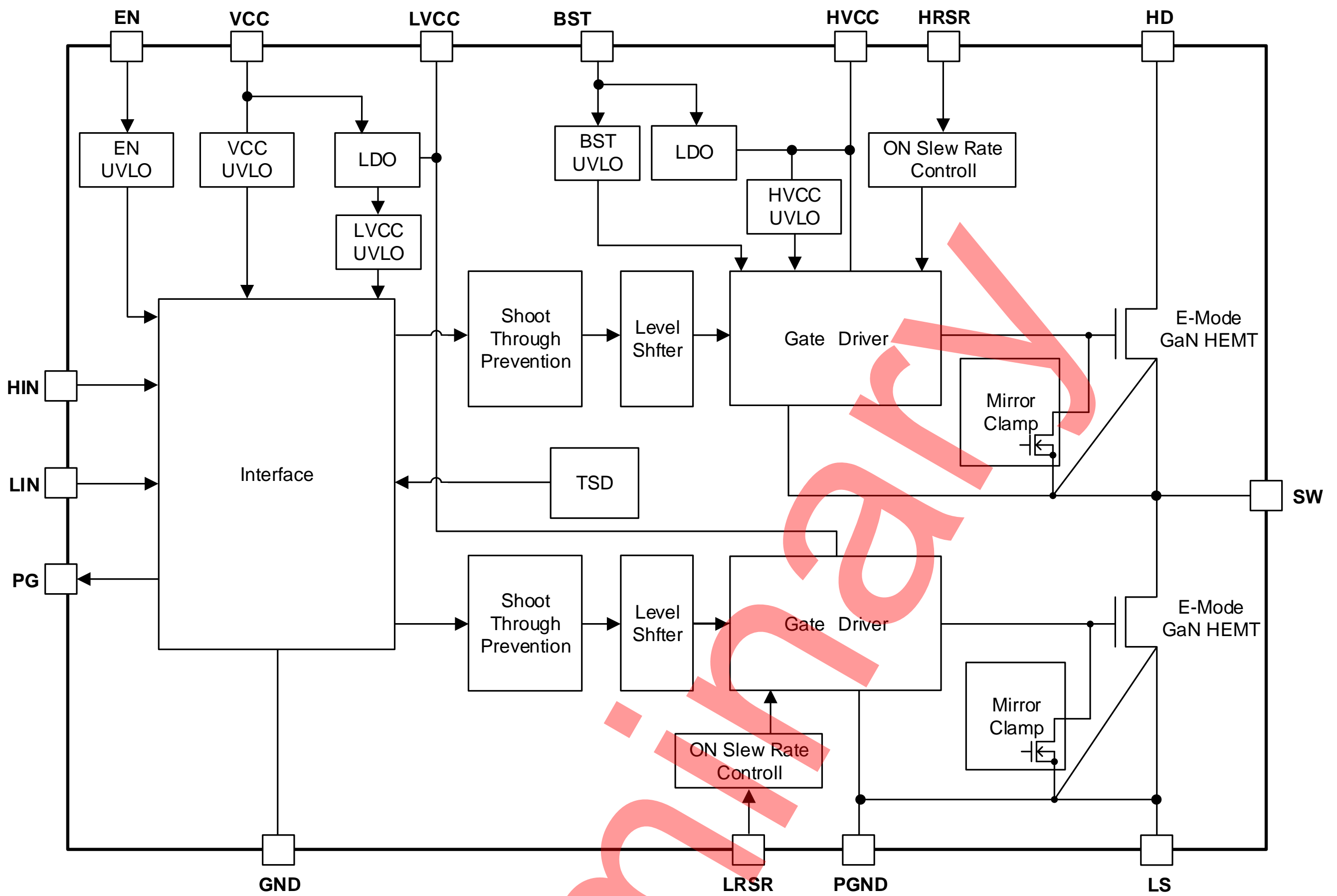

Figure 1. Block Diagram

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Description of Blocks

1 Overview

The IC, which integrates two GaN devices, gate drivers and other additional functions such as protections, offers an optimum solution for making high power density design much easier and more efficient.
Due to a zero reverse recovery and extremely low output capacitance of GaN device, the IC achieves excellent efficiency especially in bridge-based topologies. It is also possible to replace existing Si MOSFETs and heatsinks to improve the efficiency and PCB size.
The integrated gate drivers with wide operating the VDD pin and IN pin input voltage range bring a remarkable switching performance such as a high drain slew rate and low propagation delay, and they also make the GaN devices even much easier to use than traditional Si MOFET discrete.
Furthermore, various protections such as VCC UVLO, EN UVLO, LVCC UVLO, HVCC UVLO, BST UVLO and thermal shutdown (TSD) are also integrated to protect this IC from damages. A power good signal is outputted from the PG pin, and it switches to a low level if any abnormal state is detected.

2 Feature Descriptions

The IC is designed to be efficient, robust, and easy using.

2.1 Enhancement-Mode GaN HEMT

This IC integrates an enhancement-mode (normally-off) GaN device.
The enhancement-mode GaN device has smaller parasitic inductance and less switching loss than the cascode topology which connects a depletion-mode (normally-on) GaN device and a Si MOSFET in series because the cascode topology has additional parasitic inductance between a depletion-mode GaN device and Si MOSFET.
These characteristics offer advanced switching performance physically, and that is significant especially in large current applications.

2.2 Gate Driver

This IC integrates an original gate driver for the enhancement-mode GaN devices.

2.3 Level Shifter

This IC integrates level shifter circuit which has low propagation delay and high dv/dt immunity.

2.4 VCC UVLO, EN UVLO, LVCC UVLO, HVCC UVLO, BST UVLO, TSD

This IC has some protection circuits.

2.5 LDO

This IC integrates a LDO regulator with 5.75 V output voltage which is outputted from LVCC pin and HVCC pin.
The low side LDO output (LVCC pin voltage) is disabled when VCC UVLO is detected.
It is recommended to use an output capacitor C_{LVCC} of at least 0.22 µF between the LVCC pin and the PGND pin.
Also, the high side LDO output (HVCC pin voltage) is disabled when BST UVLO is detected.
It is recommended to use an output capacitor C_{HVCC} of at least 0.22 µF between the HVCC pin and the SW pin.
The ceramic capacitor which has low ESR should be used for an output capacitor C_{LVCC} and C_{HVCC}.

2.6 ON Slew Rate Control

Generally, there is a tradeoff between efficiency and EMI. A higher switching slew rate reduces the switching loss, on the other hand, it also increases the switching noise.
By adjusting resistors between the HRSR pin and the SW pin (R_{HRSR}) between the LRSR pin and the LGND pin (R_{LRSR}), the turn-on drain slew rate can be selected freely from 3 V/ns to 50 V/ns.
It allows users to optimize the switching speed according to specific circumstance, such as an EMI filter space, PCB layout, etc.

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Feature Descriptions – continued

2.7 Interface

It is possible to use the output of most of general MCUs or ACDC controllers as the HIN pin's input signal or LIN pin's input signal directly, due to the original interface circuit.
The relationship between HIN or LIN pin's logic signal level and high or low side GaN HEMT's state are shown in Table 1.
However, both side GaN HEMT are forced to be OFF state if either VCC UVLO, EN UVLO, LVCC UVLO, or TSD is detected.
High side GaN HEMT is forced to be OFF state if BST UVLO or HVCC UVLO is detected.

Table 1. Relationship between HIN or LIN pin's logic signal level and high or low side GaN HEMT's state

Input		Output	
HIN	LIN	High side GaN HEMT	Low side GaN HEMT
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF

The PG pin is an open drain output for a power good signal of this IC.
If VCC UVLO, EN UVLO, LVCC UVLO, or TSD are all released, the PG pin voltage goes a high impedance state after the delay time t_{D_PG}.
If either VCC UVLO, EN UVLO, LVCC UVLO, or TSD is detected, the PG pin is pulled down to low level by internal resistor R_{PG_PD}.
It can be outputted to the controller IC to report the abnormal state of this IC.
The protections and abnormal states, and corresponding PG pin state are shown in Table 2.
However, if VCC pin voltage is V_{OFF} or less, PG pin is forcibly high impedance state.

Table 2. PG pins state

Protections and Abnormal States ("1" = Detected, "0" = Released, "X"=Don't care)				PG Pin State
VCC UVLO	EN UVLO	LVCC UVLO	TSD	
0	0	0	0	Hi-Z
1	X	X	X	Pull Down
X	1	X	X	Pull Down
X	X	1	X	Pull Down
X	X	X	1	Pull Down

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Feature Descriptions – continued

2.8 Shoot Through Prevention

This IC integrates shoot through prevention function.
This function prevents logic input signal on one side from propagating to the GaN HEMT gate voltage and turning it on for turn-on mask time t_{MASK} after the logic input signal on the other side is turned off.
This function does not affect the delay time from input to gate driver outputs when the dead time between LIN and HIN.

For the example, the timing chart when the Shoot Through Prevention function operates in Figure 2.

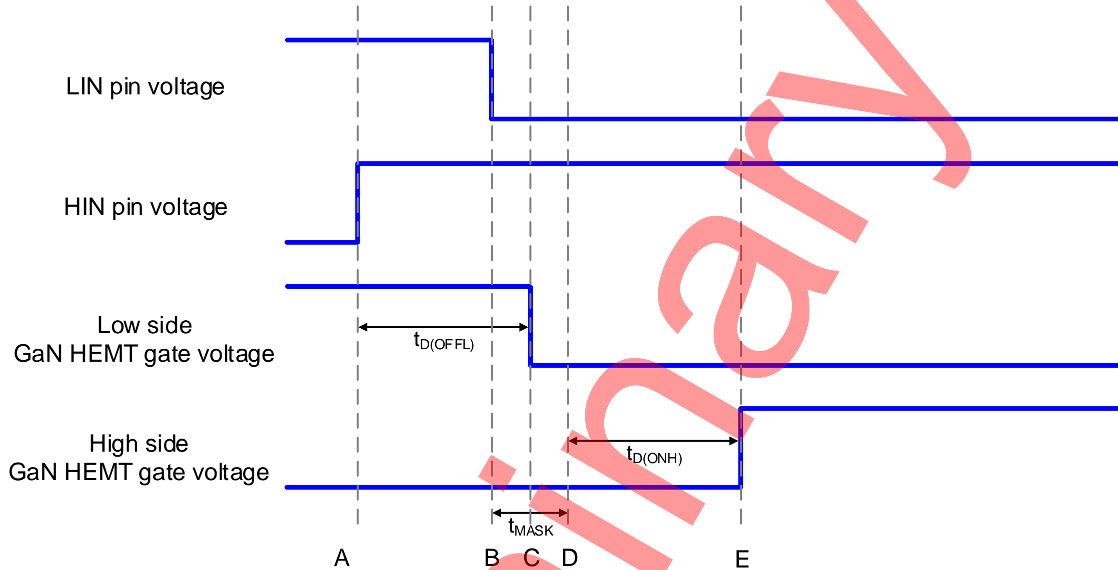

Figure 2. Shoot Through Prevention function

A: HIN logic input signal is turned on while LIN Logic input singal is ON.
B: LIN logic input signal is turned off and t_{MASK} starts to be counted.
C: Low side GaN HEMT gate voltage output is turned off after the low side turn-off delay time $t_{D(OFFL)}$ from A due to interface logic.
D: The period of t_{MASK} ends and HIN logic input signal starts to be propagated to high side GaN HEMT gate voltage.
E: High side gate GaN HEMT gate voltage is turned on after the high side turn-on delay time $t_{D(ONH)}$ from D.

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Feature Descriptions – continued

2.9 Mirror Clamp

This IC integrates high side and low side Mirror Clamp function.

Table 3. Low side Mirror Clamp state

LIN	Low side Gan HEMT Gate Voltage	Internal MOSFET
0	Over than V_{MC}	OFF
0	Less than V_{MC}	ON
1	Over than V_{MC}	OFF
1	Less than V_{MC}	OFF

Table 4. High side Mirror Clamp state

HIN	High side GaN HEMT Gate Voltage	Internal MOSFET
0	Over than V_{MC}	OFF
0	Less than V_{MC}	ON
1	Over than V_{MC}	OFF
1	Less than V_{MC}	OFF

For the example, the timing chart when the low side Mirror Clamp function operates in Figure 3.

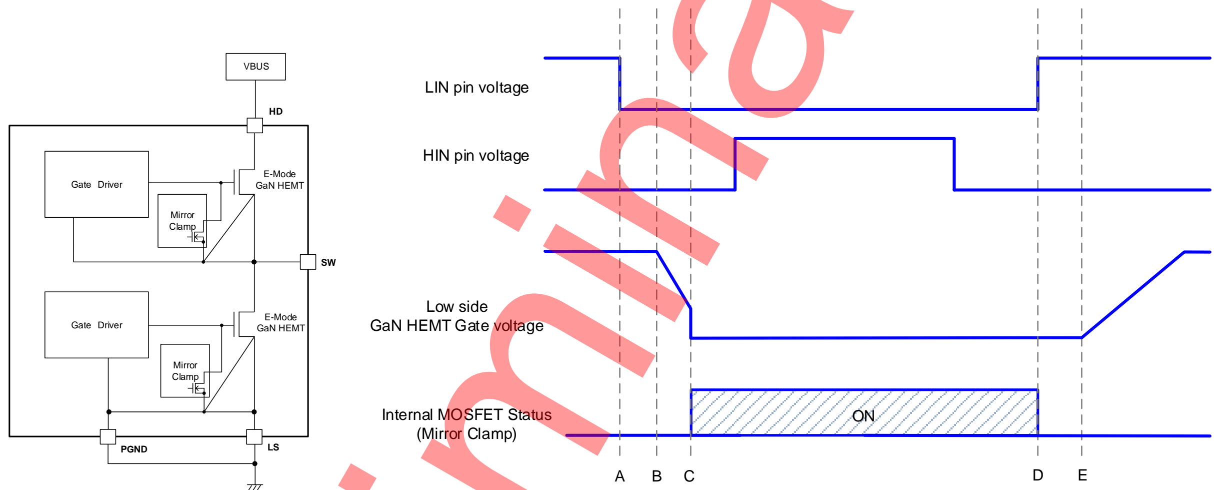

Figure 3. Mirror Clamp Function (Low Side)

A: LIN logic input signal is turned off.
B: Low side GaN HEMT gate voltage is falling.
C: Low side GaN HEMT gate voltage is turned off, Mirror Clamp function is detected.
The internal MOSFET is turned on.
D: LIN logic input signal is turned on and the internal MOSFET is turned off.
E: Low side GaN HEMT gate voltage is turned on and rising.

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Description of Blocks – continued

3 Start Sequence

Start sequence is shown in Figure 4.

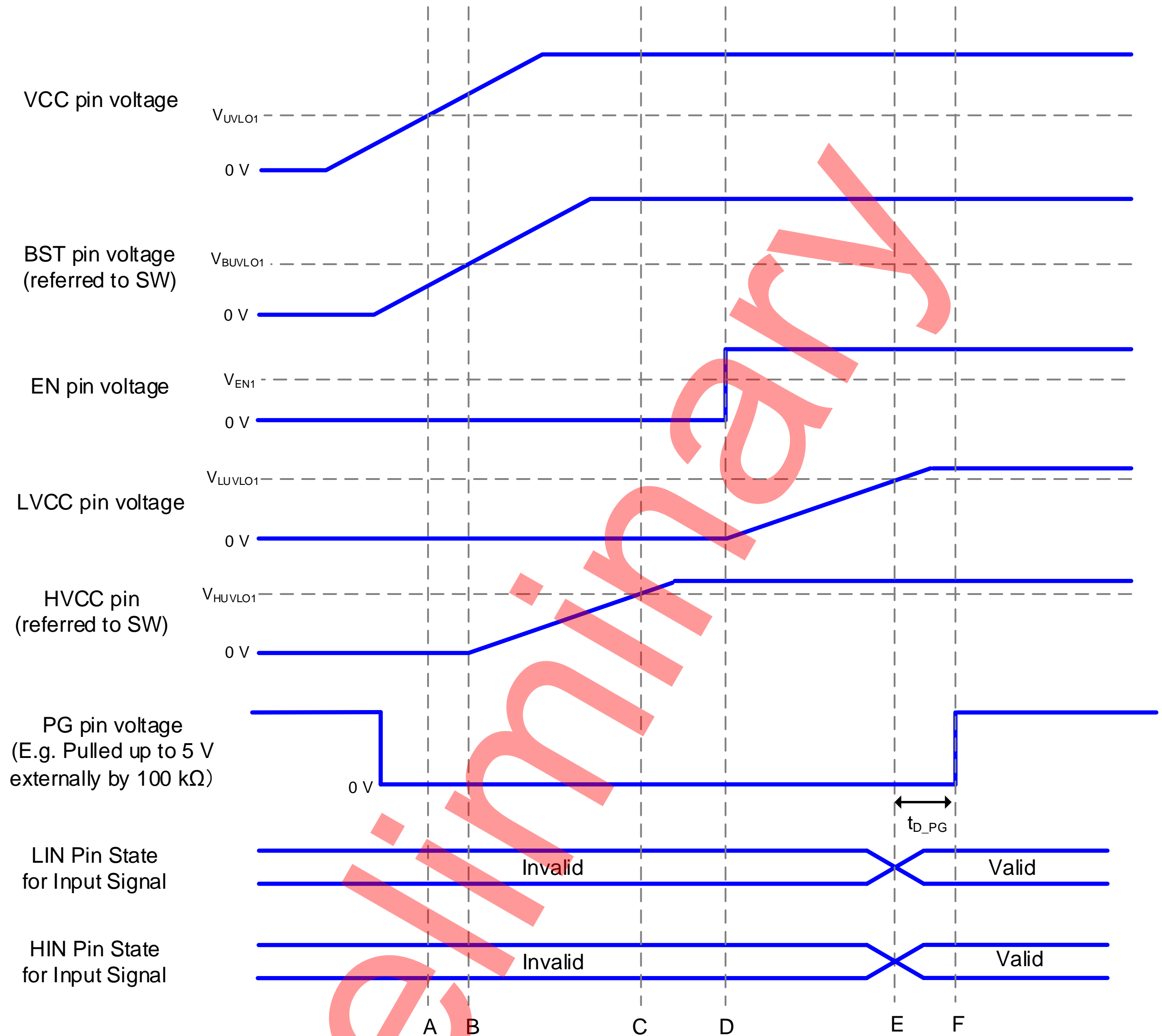

Figure 4. Start Sequences

A: When the VCC pin voltage exceeds V_{UVLO1}, VCC UVLO is released.

B: When the BST pin voltage exceeds V_{BUVLO1}, BST UVLO is released, the LDO regulator for high side drive starts, and HVCC pin voltage starts to rise.

C: When the HVCC pin voltage exceeds V_{HUVLO1}, HVCC UVLO is released.

D: When the EN pin voltage exceeds V_{EN1}, EN UVLO is released.
VCC ULVO and EN UVLO released, the LDO regulator for low side drive starts, and LVCC pin voltage starts to rise.

E: When the LVCC pin voltage exceeds V_{LUVLO1}, LVCC UVLO is released and the input signal to LIN pin becomes enabled.
Here, HVCC UVLO released, the condition that the input signal to HIN pin becomes enabled.

F: The PG pin state changes from internally pulled down to a high impedance after t_{D_PG} from E.

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1A}	-0.3 to +683	V	HD - SW, SW, HVCC, HRSR pin voltage, DC
	V_{MAX1B}	-0.3 to +730	V	HD - SW, SW, HVCC, HRSR pin voltage, tpulse < 1 μs(Note 1)
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +33	V	VCC, EN, HIN, LIN pin voltage
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +33	V	BST pin voltage referred to SW
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +7.0	V	LVCC, PG, LRSR pin voltage
Maximum Applied Voltage 5	V_{MAX5}	-0.3 to +7.0	V	HVCC, HRSR pin voltage referred to SW
Maximum Applied Voltage 6	V_{MAX6}	-2.5 to +2.5	V	PGND pin voltage referred to GND
Maximum Inflow Current	I_{MAX}	5.0	mA	PG pin Inflow current
DRAIN pin Current	$I_{D(RMS)}$	20.9	A	RMS
	$I_{D(PULSE)}$	66.1	A	Pulse (GATE = ON, tpulse < 1 μs)
DRAIN dv/dt	dv/dt	150	V/ns	V_D = 0V to 400V
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %.

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
VQ53TV100AW				
Junction to Ambient	θ_{JA}	T.B.D.	T.B.D.	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	T.B.D.	T.B.D.	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range 1	V_{HD}	-	-	650	V	HD pin voltage
Power Supply Voltage Range 2	V_{CC}	9.3	15	25	V	VCC pin voltage
Power Supply Voltage Range 3	V_{BST}	8.0	15	25	V	VCC pin voltage
Input Voltage Voltage Range 1	V_{IN_H}	3.0	5	V_{CC}	V	IN pin high voltage
Input Voltage Voltage Range 2	V_{IN_L}	-0.3	0	+0.3	V	IN pin low voltage
SW Voltage Range	V_{SW}	-3.5	0	600	V	SW pin voltage
PGND Voltage Range	V_{PGND}	-1.5	0	+1.5	V	PGND pin voltage referred to GND
LVCC Load Current Range	I_{LVCC}	-	-	10	mA	
LVCC pin Output Capacitor Range	C_{LVCC}	0.22	-	1	µF	
HVCC Load Current Range	I_{HVCC}	-	-	10	mA	
HVCC pin Output Capacitor Range	C_{HVCC}	0.22	-	1	µF	
BST pin Output Capacitor Range	C_{BST}	TBD	-	-	µF	
Operating Temperature	Topr	-40	-	+105	°C	Surrounding temperature

Electrical Characteristics

(Unless noted otherwise, V_{CC}=15V, V_{BST} = 15 V, Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
GaN HEMT (Each side)						
D-S Withstand Voltage	$V_{(BR)DDS1}$	650	-	-	V	GaN HEMT is off
D Pin Leak Current	I_{DSS1}	-	-	100	µA	GaN HEMT is off, V_{DS} = 600 V, Tj = 25 °C
	I_{DSS2}	-	10	-	µA	GaN HEMT is off, V_{DS} = 600 V, Tj = 150 °C
D-S ON State Resistance	$R_{DS1(ON)}$	-	50	70	mΩ	GaN HEMT is on, I_D = 0.5 A, Tj = 25 °C
	$R_{DS2(ON)}$	-	TBD	-	mΩ	GaN HEMT is on, I_D = 0.5 A, Tj = 150 °C
S-D Reverse Voltage	V_{SD}	-	2.36	-	V	I_D = -8.0 A, V_{IN} = 0 V
Output Capacitance	C_{OSS}	-	65.6	-	pF	V_{IN} = 0V, V_D = 400V, f = 1MHz
Energy Related Effective Output Capacitance	$C_{O(ER)}$	-	97.4	-	pF	V_{IN} = 0V, V_D = 0V to 400V
Time Related Effective Output Capacitance	$C_{O(TR)}$	-	150.5	-	pF	I_D = Constant, V_{IN} = 0V, V_D = 0V to 400V
Reverse Recovery Charge	Q_{RR}	-	0	-	nC	
VCC Blocks						
VCC Operating Current	I_{ON1}		TBD	TBD	mA	Operating at 500 kHz, duty = 50 % R_{LRSR} = OPEN
VCC Quiescent Current	I_{ON2}	-	210	330	µA	V_{LIN} = V_{HIN} = 0 V
VCC Standby Current	I_{STB}	-	120	180	µA	V_{CC} = 9.3 V
VCC UVLO Release Voltage	V_{UVLO1}	8.0	8.6	9.2	V	At VCC pin voltage rising
VCC UVLO Detection Voltage	V_{UVLO2}	7.5	8.1	8.7	V	At VCC pin voltage dropping
VCC UVLO Hysteresis	V_{UVLO3}	-	0.5	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2}
EN Blocks						
EN UVLO Release Voltage	V_{EN1}	1.8	2.0	2.2	V	At EN pin voltage rising
EN UVLO Detection Voltage	V_{UVLO2}	1.3	1.5	1.7	V	At EN pin voltage dropping
EN UVLO Hysteresis	V_{UVLO3}	-	0.5	-	V	V_{EN3} = V_{EN1} - V_{EN2}
EN Leakage Current	I_{EN_LEAK}	-	2.0	4.0	µA	V_{EN} = 5 V

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Electrical Characteristics - continued

(Unless noted otherwise, V_{CC} = 15 V, V_{BST} = 15 V, Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Blocks						
LIN, HIN N Threshold Voltage	V_{IN_ON}	-	(2.2)	2.6	V	
LIN, HIN FF Threshold Voltage	V_{IN_ON}	0.9	(1.2)	-	V	
LIN, HIN hreshold Hysteresis	V_{IN_HYS}	-	1.0	-	V	
LIN, HIN eakage Current	I_{IN_LEAK}	-	3.5	-	µA	V_{LIN}, V_{HIN} = 5 V
TSD Blocks						
TSD Temperature 1	T_{SD1}	(150)	(175)	(200)	°C	At temperature rising (Note 1)
TSD Temperature 2	T_{SD2}	-	(100)	-	°C	At temperature dropping (Note 1)
TSD Hysteresis	T_{SD3}	-	(75)	-	°C	T_{SD3} = T_{SD1} - T_{SD2}
TSD Timer	t_{TSD}	50	100	150	µs	
LVCC Blocks						
LVCC Output Voltage	V_{LVCC}	5.50	5.75	6.00	V	
LVCC Maximum Output Current	I_{LVCC}	10	-	-	mA	
LVCC UVLO Release Voltage	V_{LUVLO1}	4.20	4.60	5.00	V	At LVCC pin voltage rising
LVCC UVLO Detection Voltage	V_{LUVLO2}	3.90	4.30	4.70	V	At LVCC pin voltage dropping
LVCC UVLO Hysteresis	V_{LUVLO3}	-	0.30	-	V	V_{LUVLO3} = V_{LUVLO1} - V_{LUVLO2}
LVCC Internal Pull-down Resistor	R_{LVCC}	2.6	5.2	7.8	kΩ	EN = 0 V
HVCC Blocks						
HVCC Output Voltage	V_{HVCC}	5.50	5.75	6.00	V	
HVCC Maximum Output Current	I_{HVCC}	10	-	-	mA	
HVCC UVLO Release Voltage	V_{HUVLO1}	4.20	4.60	5.00	V	At HVCC pin voltage rising
HVCC UVLO Detection Voltage	V_{HUVLO2}	3.90	4.30	4.70	V	At HVCC pin voltage falling
HVCC UVLO Hysteresis	V_{HUVLO3}	-	0.30	-	V	V_{HUVLO3} = V_{HUVLO1} - V_{HUVLO2}
HVCC Internal Pull-down Resistance	R_{HVCC}	0.6	1.3	2.0	kΩ	EN = 0 V
BST Blocks						
BST Operating Current	I_{BSTON1}	-	TBD	TBD	mA	Operating at 500 kHz, duty = 50 % R_{HRSR} = OPEN
BST Quiescent Current	I_{BSTON2}	-	120	180	µA	V_{HIN} = 0 V
BST UVLO Release Voltage	V_{BUVLO1}	6.70	7.30	7.90	V	At BST pin voltage rising
BST UVLO Detection Voltage	V_{BUVLO2}	6.40	7.00	7.60	V	At BST pin voltage falling
BST UVLO Hysteresis	V_{BUVLO2}	-	0.30	-	V	V_{BUVLO3} = V_{BUVLO1} – V_{BUVLO2}
PG Blocks						
PG Pin Internal Pull-down Resistor	R_{PG_PD}	-	100	200	Ω	

(Note 1) No shipping inspection.

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Electrical Characteristics - continued

(Unless noted otherwise, V_{CC} = 15 V, V_{BST} = 15 V, Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Switching Items						
Low Side Turn-on Delay Time	$t_{D(ONL)}$	-	60	90	ns	V_{CC}, V_{BST} = 12V to 25 V (Note 1) (Note 2)
		-	60	120 (TBD)	ns	V_{CC}, V_{BST} = 9.3V to 11 V (Note 1) (Note 2)
Low Side Turn-off Delay Time	$t_{D(OFFL)}$	-	60	90	ns	V_{CC}, V_{BST} = 12V to 25 V (Note 1) (Note 2)
		-	60	120 (TBD)	ns	V_{CC}, V_{BST} = 9.3V to 11 V (Note 1) (Note 2)
High Side Turn-on Delay Time	$t_{D(ONH)}$	-	60	90	ns	V_{CC}, V_{BST} = 12V to 25 V (Note 1) (Note 2)
		-	60	120 (TBD)	ns	V_{CC}, V_{BST} = 9.3V to 11 V (Note 1) (Note 2)
High Side Turn-off Delay Time	$t_{D(OFFH)}$	-	60	90	ns	V_{CC}, V_{BST} = 12V to 25 V (Note 1) (Note 2)
		-	60	120 (TBD)	ns	V_{CC}, V_{BST} = 9.3V to 11 V (Note 1) (Note 2)
Turn-on Mask Time	t_{MASK}	35	65	100	ns	
Low Side Fall Time	t_{FL}	-	4.8		ns	R_{LRSR} = 0 Ω (Note 1) (Note 2)
Low Side Rise Time	t_{RL}	-	8	-	ns	(Note 1) (Note 2) (Note 3)
High Side Fall Time	t_{FH}	-	4.8	-	ns	R_{HRSR} = 0 Ω (Note 1) (Note 2)
High Side Rise Time	t_{RH}	-	8	-	ns	(Note 1) (Note 2) (Note 3)
Low Side Turn-on Slew Rate 1	SR_{ONL1}	-	TBD	-	V/ns	R_{LRSR} = OPEN (Note 1) (Note 2)
Low Side Turn-on Slew Rate 2	SR_{ONL2}	-	50	-	V/ns	R_{LRSR} = 0 Ω (Note 1) (Note 2)
High Side Turn-on Slew Rate 1	SR_{ONH1}	-	TBD	-	V/ns	R_{HRSR} = OPEN (Note 1) (Note 2)
High Side Turn-on Slew Rate 2	SR_{ONH2}	-	50	-	V/ns	R_{HRSR} = 0 Ω (Note 1) (Note 2)
Minimum Input Pulse width	t_{PW_MIN}	-	-	30	ns	V_{CC}, V_{BST} = 15 V (Note 1)
		-	-	40	ns	V_{CC}, V_{BST} = 9.3V to 25 V (Note 1)
Allowable Input Switching Frequency	f_{SW}	-	-	1.0	MHz	HIN or LIN pin

(Note 1) No shipping inspection.
(Note 2) Refer to 'Switching Parameter Measurement Information'.
(Note 3) Varies greatly depending on the conditions of the application.

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Switching Parameter Measurement Information

Figure 5 shows the circuit for measurements of switching parameters (Low Side).
Figure 6 shows instruction of them.

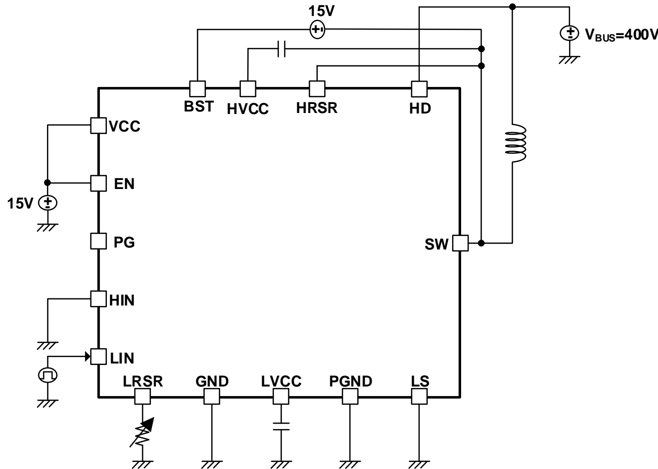

Figure 5. Switching Parameters Measurement Circuit (Low Side)

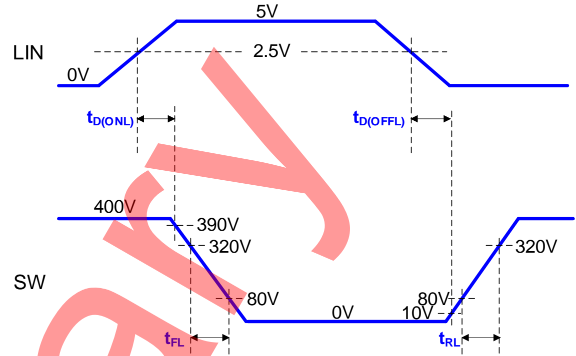

Figure 6. Instruction of Switching Parameters (Low Side)

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1 **Low Side Turn-on Delay Time: $t_{D(ONL)}$**
The low side turn-on delay time is the time from rising edge of the LIN pin voltage (LIN pin voltage is rising to 2.5 V) to when the GaN HEMT starts turning on (SW pin voltage is falling to 390 V).

2 **Low Side Fall Time: t_{FL}**
The low side fall time is the time it takes for SW pin voltage falls from 320 V to 80 V.

3 **Low Side Turn-off Propagation Delay: $t_{D(OFFL)}$**
The low side turn-off delay time is the time from falling edge of the LIN pin voltage (LIN pin voltage is falling to 2.5 V) to when the GaN HEMT starts turning off (SW pin voltage is rising to 10 V).

4 **Low Side Rise Time: t_{RL}**
The low side rise time is the time it takes for SW pin voltage rises from 80 V to 320 V.

5 **Low Side Turn-on Slew Rate: SR_{ONL}**
The low side turn-on slew rate is the slew rate which is when SW pin voltage falls from 320 V to 80 V.
It is calculated by the formula below.

$$SR_{ONL} = \frac{240V}{t_{FL}}$$

where:
SR_{ONL} is the low side turn-on slew rate.
t_{FL} is the low side fall time.

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Switching Parameter Measurement Information - continued

Figure 7 shows the circuit for measurements of switching parameters (High Side).
Figure 8 shows instruction of them.

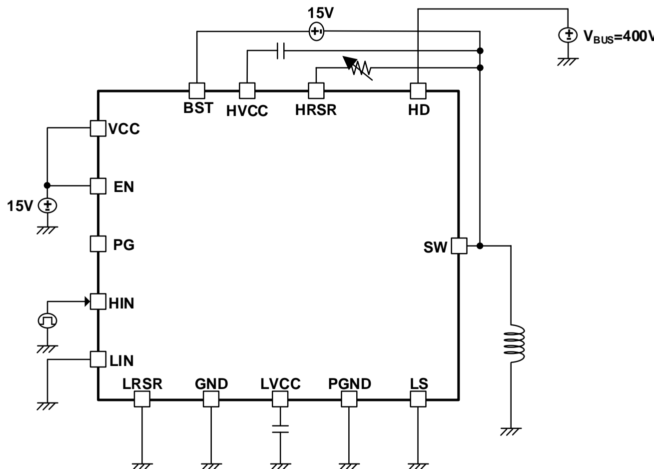

Figure 7. Switching Parameters Measurement Circuit (High Side)

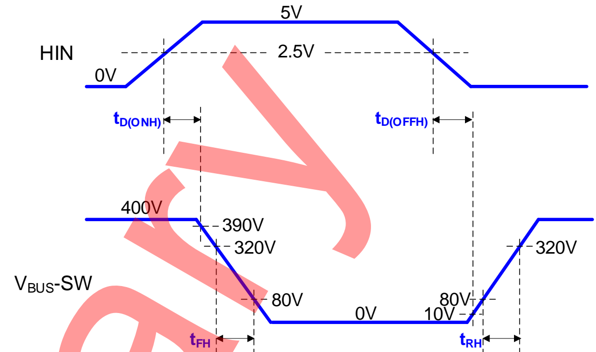

Figure 8. Instruction of Switching Parameters (High Side)

1 High Side Turn-on Delay Time: $t_{D(ONH)}$
The high side turn-on delay time is the time from rising edge of the HIN pin voltage (HIN pin voltage is rising to 2.5 V) to when the GaN HEMT starts turning on (SW-V_{BUS} pin voltage is falling to 390 V).

2 High Side Fall Time: t_{FH}
The high side fall time is the time it takes for SW-V_{BUS} pin voltage falls from 320 V to 80 V.

3 High Side Turn-off Propagation Delay: $t_{D(OFFH)}$
The high side turn-off delay time is the time from falling edge of the HIN pin voltage (HIN pin voltage is falling to 2.5 V) to when the GaN HEMT starts turning off (SW-V_{BUS} pin voltage is rising to 10 V).

4 High Side Rise Time: t_{RH}
The high side rise time is the time it takes for SW-V_{BUS} pin voltage rises from 80 V to 320 V.

5 High Side Turn-on Slew Rate: SR_{ONH}
The low side turn-on slew rate is the slew rate which is when SW-V_{BUS} pin voltage falls from 320 V to 80 V.
It is calculated by the formula below.

$$SR_{ONH} = \frac{240V}{t_{RH}}$$

where:
SR_{ONH} is the high side turn-on slew rate.
t_{RH} is the high side rise time

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Typical Performance Curves

(Reference Data)

T.B.D.

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I/O Equivalence Circuit

T.B.D.

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

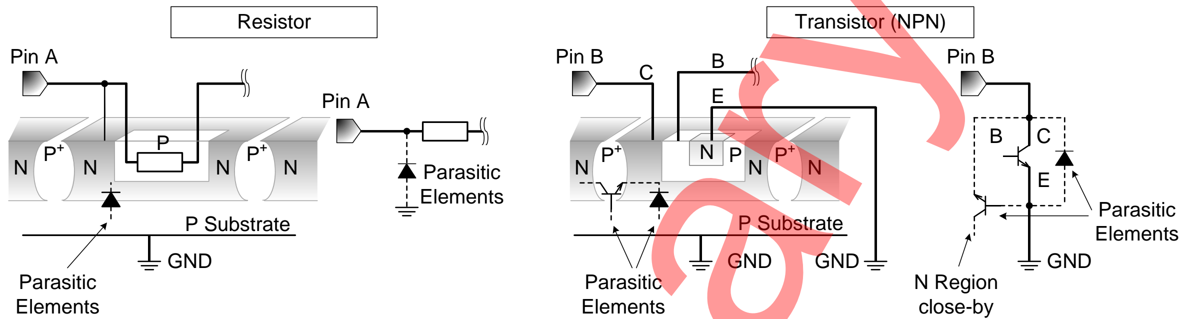

Figure 9. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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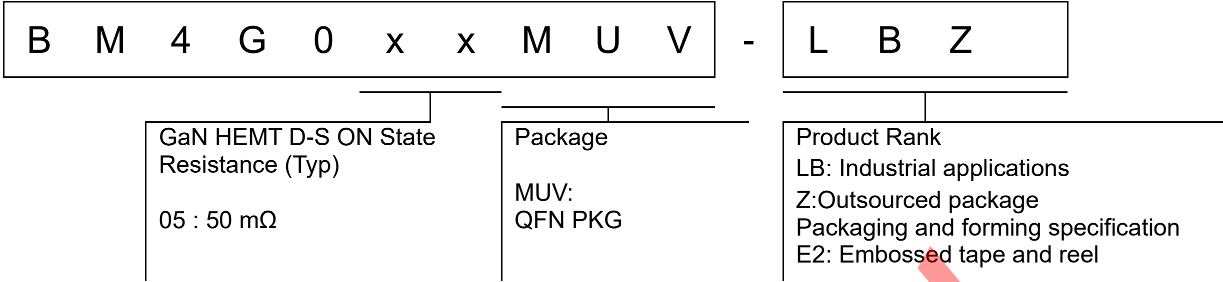
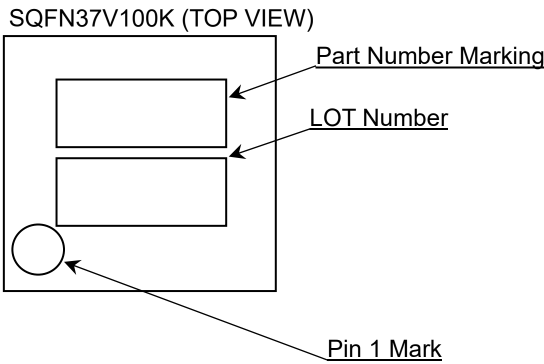
Ordering Information



Marking Diagram



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Physical Dimension and Packing Information

Package Name	SQFN37V100K
T.B.D.	

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Revision History

Date	Revision	Changes
6.Jun.2024	000	New Release (Temporary version)

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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