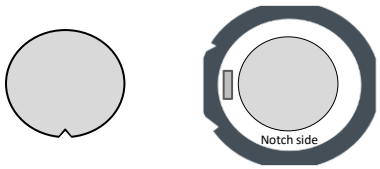
SG6306WN

650V 20A Insulated Gate Bipolar Transistor Datasheet

V_{CES}	650V
$I_{C\ (Nominal)}$	20A
$V_{CE(sat)\ (Typ.)}$	1.5V
Max. Possible Chips per Wafer	2829pcs

●Outline

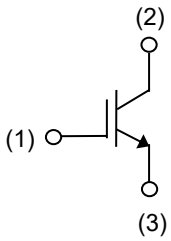
Wafer (W05) Unsawn on foil (U03)



●Features

1) Trench Light Punch Through Type
2) Low Collector - Emitter Saturation Voltage
3) High Speed Switching
4) Low Switching Loss & Soft Switching

●Inner Circuit



(1) Gate
(2) Collector
(3) Emitter

●Application

PFC

UPS

Welding

Solar Inverter

IH

●Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Collector - Emitter Voltage, T_j = 25°C	V_{CES}	650	V
Gate - Emitter Voltage	V_{GES}	±30	V
Collector Current	I_C *1	*1)	A
Pulsed Collector Current	I_{CP} *2	80	A
Operating Junction Temperature	T_j	-40 to +175	°C

*1 Depending on thermal properties of assembly

*2 Pulse width limited by $T_{jmax.}$

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●Design Assurance

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Reverse Bias Safe Operating Area	RBSOA*3	I_C = 80A, V_{CC} = 520V, V_P = 650V, V_{GE} = 15V, R_G = 100Ω, T_j = 175℃	FULL SQUARE			-

*3 Design assurance without measurement

●Electrical Characteristics (at T_j = 25°C unless otherwise specified, in case of TO-247N package)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Collector - Emitter Breakdown Voltage	BV_{CES}	I_C = 10μA, V_{GE} = 0V	650	-	-	V
Collector Cut - off Current	I_{CES}	V_{CE} = 650V, V_{GE} = 0V	-	-	10	μA
Gate - Emitter Leakage Current	I_{GES}	V_{GE} = ±30V, V_{CE} = 0V	-	-	±200	nA
Gate - Emitter Threshold Voltage	$V_{GE(th)}$	V_{CE} = 5V, I_C = 13.3mA	5.0	6.0	7.0	V
Collector - Emitter Saturation Voltage	$V_{CE(sat)}$*3	I_C = 20A, V_{GE} = 15V, T_j = 25°C	-	1.5	1.9	V
		T_j = 175°C	-	1.85	-	
Input Capacitance	C_{ies}	V_{CE} = 30V, V_{GE} = 0V, f = 1MHz	-	1680	-	pF
Output Capacitance	C_{oes}		-	47	-	
Reverse transfer Capacitance	C_{res}		-	31	-	
Total Gate Charge	Q_g	V_{CE} = 400V, I_C = 20A, V_{GE} = 15V	-	59	-	nC
Gate - Emitter Charge	Q_{ge}		-	13	-	
Gate - Collector Charge	Q_{gc}		-	23	-	

*3 Design assurance without measurement

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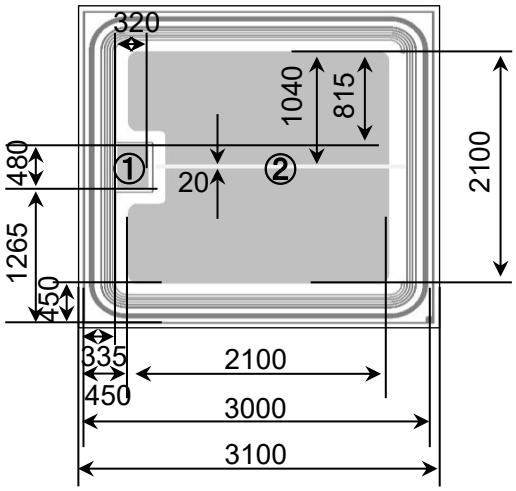
●Chip Information



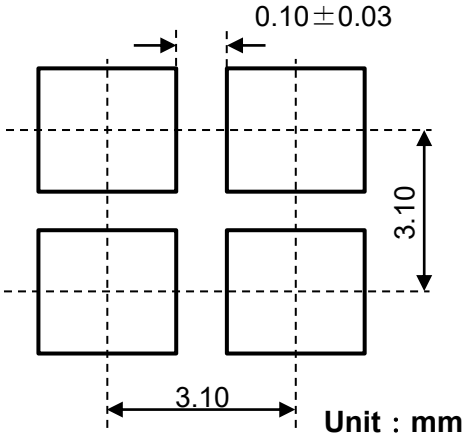
Unit : μm

: Pad Area

① : Gate Bonding Pad

② : Emitter Bonding Pad

Backside : Collector



Wafer Size	200mm
Wafer Thickness	0.07±0.01mm
Chip Size	3.10mm×3.10mm
Cut Line Width	0.10±0.03mm
Top Side Metallization	AlCu:4.4μm
Back Side Metallization	Ti/Ni:0.4μm/Au:0.05μm
Passivation	Polyimide

●Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

This chip data sheet refers to the device data sheet	RGW40TS65

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