

Operational Amplifier

Automotive Ground Sense Operational Amplifier

LM2902EZFV-C
General Description

LM2902EZFV-C is high-gain and ground sense input operational amplifier. This IC is monolithic IC integrated quad independent operational amplifier on a single chip. An operating voltage range is wide with 3 V to 36 V. This operational amplifier is the most suitable for automotive requirements such as engine control unit, electric power steering, anti-lock braking system and so on because it has features of low supply current.

Features

- AEC-Q100 Qualified (Note 1)
- Operable from Almost GND Level for Both Input and Output
- Single or Dual Power Supply Operation
- Standard Op-Amp Pin-assignments
- Low Supply Current
- Wide Operating Supply Voltage Range
- High Open Loop Voltage Gain
- Wide Operating Temperature Range

(Note 1) Grade 1

Applications

- Engine Control Unit
- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Automotive Electronics

Key Specifications

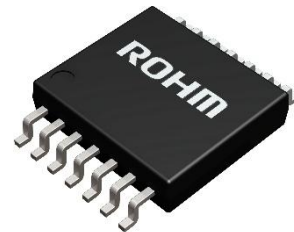
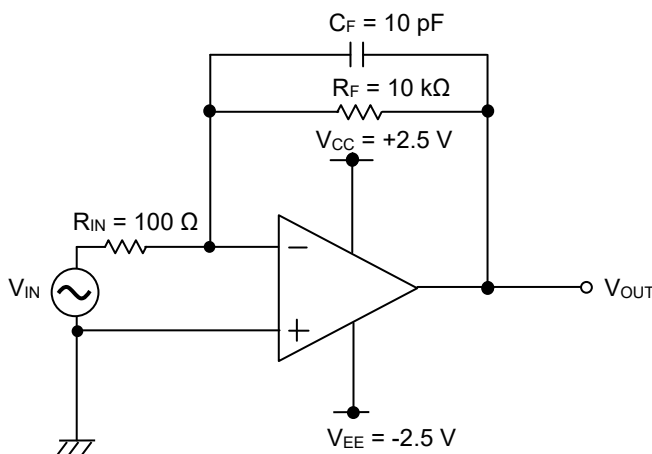
- Operating Supply Voltage Range
 - Single Supply: 3.0 V to 36.0 V
 - Dual Supply: ± 1.5 V to ± 18.0 V
- Operating Temperature Range: -40 °C to +125 °C
- Low Supply Current: 1 mA (Typ)
- Input Offset Current: 2 nA (Typ)
- Input Bias Current: 20 nA (Typ)

Package

SSOP-B14

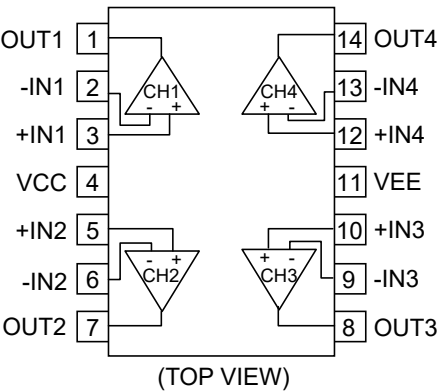
W (Typ) x D (Typ) x H (Max)

5.0 mm x 6.4 mm x 1.35 mm


Typical Application Circuit


$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

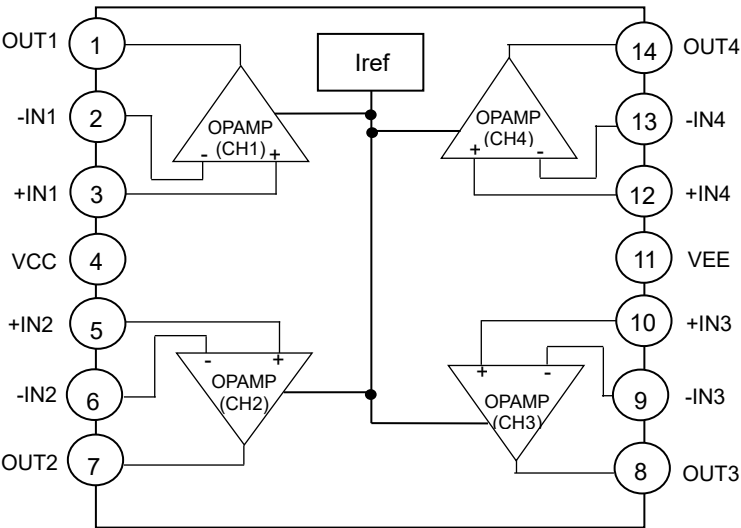
Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	OUT1	Output (1 ch)
2	-IN1	Inverting input (1 ch)
3	+IN1	Non-inverting input (1 ch)
4	VCC	Positive power supply
5	+IN2	Non-inverting input (2 ch)
6	-IN2	Inverting input (2 ch)
7	OUT2	Output (2 ch)
8	OUT3	Output (3 ch)
9	-IN3	Inverting input (3 ch)
10	+IN3	Non-inverting input (3 ch)
11	VEE	Negative power supply / Ground
12	+IN4	Non-inverting input (4 ch)
13	-IN4	Inverting input (4 ch)
14	OUT4	Output (4 ch)

Block Diagram



Description of Blocks

- 1. OPAMP:
This block is a ground sense operational amplifier with differential input stage.
- 2. Iref:
This block supplies reference current which is needed to operate OPAMP block.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{CC}-V_{EE}$	36	V
Differential Input Voltage ^(Note 1)	V_{ID}	36	V
Common-mode Input Voltage Range	V_{ICMR}	$(V_{EE} - 0.3)$ to $(V_{EE} + 36)$	V
Output Current ^(Note 2)	I_{OUT}	±40	mA
Input Current	I_I	±10	mA
Maximum Junction Temperature	T_{jmax}	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input.

The input pin voltage is set to V_{EE} or more.

(Note 2) The excessive heat generation may occur due to the short-circuit from the output pin to the power supply pin. Do not use the output pin short to power supply. Use the output current less than 40 mA regardless of the power supply voltage.

Thermal Resistance^(Note 3)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 5)	2s2p ^(Note 6)	
SSOP-B14				
Junction to Ambient	θ _{JA}	159.6	92.8	°C/W
Junction to Top Characterization Parameter ^(Note 4)	Ψ _{JT}	13	9	°C/W

(Note 3) Based on JESD51-2A(Still-Air).

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3.

(Note 6) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	Single Supply	V_{CC}	3.0	-	36.0	V
	Dual Supply		±1.5	-	±18.0	
Operating Temperature		T_{opr}	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified $V_{CC} = 5\text{ V}$, $V_{EE} = 0\text{ V}$)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage	V_{IO}	25 °C	-	2.0	3.8	mV	$V_{OUT} = 1.4\text{ V}$ Absolute value
		-40 °C to +125 °C	-	-	6.0		$V_{CC} = 5\text{ V to }30\text{ V}$ $V_{OUT} = 1.4\text{ V}$ Absolute value
Input Offset Current	I_{IO}	25 °C	-	2.0	40	nA	$V_{OUT} = 1.4\text{ V}$ Absolute value
		-40 °C to +125 °C	-	-	50		
Input Bias Current	I_B	25 °C	-	20	60	nA	$V_{OUT} = 1.4\text{ V}$ Absolute value
		-40 °C to +125 °C	-	-	100		
Supply Current	I_{CC}	25 °C	-	1.0	2.0	mA	$R_L = \infty$, All Op-Amps
		-40 °C to +125 °C	-	-	2.5		
Output Voltage High	V_{OH}	25 °C	3.5	-	-	V	$R_L = 2\text{ k}\Omega$
		-40 °C to +125 °C	3.2	-	-		
		-40 °C to +125 °C	27	28	-		$V_{CC} = 30\text{ V}$, $R_L = 10\text{ k}\Omega$
Output Voltage Low	V_{OL}	-40 °C to +125 °C	-	5.0	20	mV	$R_L = \infty$
Large Signal Voltage Gain	A_v	25 °C	88	100	-	dB	$R_L \geq 2\text{ k}\Omega$, $V_{CC} = 15\text{ V}$ $V_{OUT} = 1.4\text{ V to }11.4\text{ V}$
		-40 °C to +125 °C	88	-	-		
Common-mode Input Voltage Range	V_{ICMR}	25 °C	0	-	3.5	V	$(V_{CC}-V_{EE}) = 5\text{ V}$ $V_{OUT} = V_{EE} + 1.4\text{ V}$
		-40 °C to +125 °C	0	-	3.0		
Common-mode Rejection Ratio	CMRR	-40 °C to +125 °C	65	80	-	dB	$V_{OUT} = 1.4\text{ V}$
Power Supply Rejection Ratio	PSRR	-40 °C to +125 °C	70	100	-	dB	$V_{CC} = 5\text{ V to }30\text{ V}$
Output Source Current ^(Note 1)	I_{OH}	25 °C	20	30	40	mA	$V_{+IN} = 1\text{ V}$, $V_{-IN} = 0\text{ V}$ $V_{OUT} = 0\text{ V}$ 1 ch is short circuit Absolute value
		-40 °C to +125 °C	10	-	-		
Output Sink Current ^(Note 1)	I_{OL}	25 °C	20	27	40	mA	$V_{+IN} = 0\text{ V}$, $V_{-IN} = 1\text{ V}$ $V_{OUT} = 5\text{ V}$ 1 ch is short circuit Absolute value
		-40 °C to +125 °C	2.0	-	-		
		25 °C	20	50	-	μA	$V_{+IN} = 0\text{ V}$, $V_{-IN} = 1\text{ V}$ $V_{OUT} = 200\text{ mV}$
Slew Rate	SR	25 °C	-	0.2	-	V/ μs	$V_{CC} = 15\text{ V}$, $A_v = 0\text{ dB}$ $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$
Gain Bandwidth Product	GBW	25 °C	-	0.5	-	MHz	$V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$ $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$
Channel Separation	CS	25 °C	-	120	-	dB	$f = 1\text{ kHz}$, Input Referred

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Typical Performance Curves

$V_{EE} = 0\text{ V}$

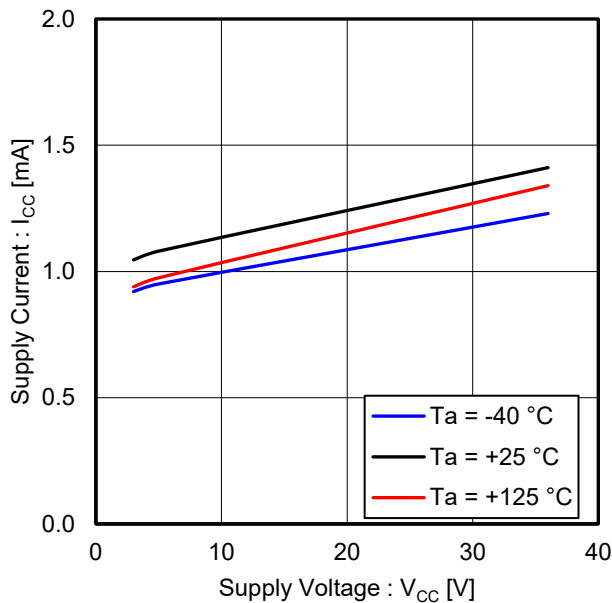


Figure 1. Supply Current vs Supply Voltage

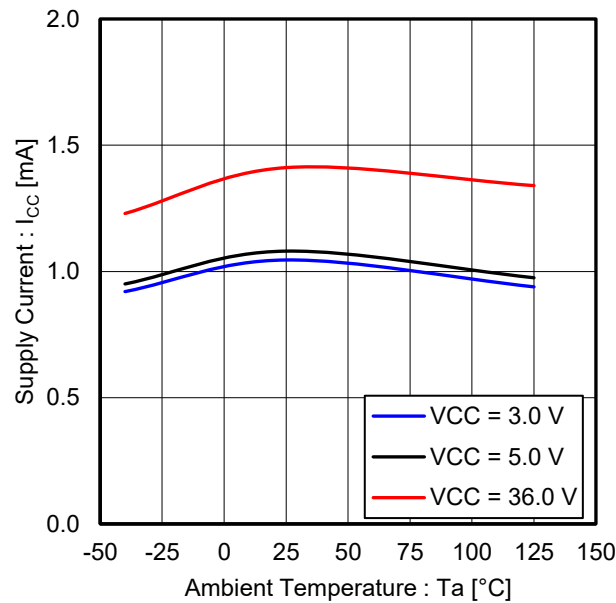


Figure 2. Supply Current vs Ambient Temperature

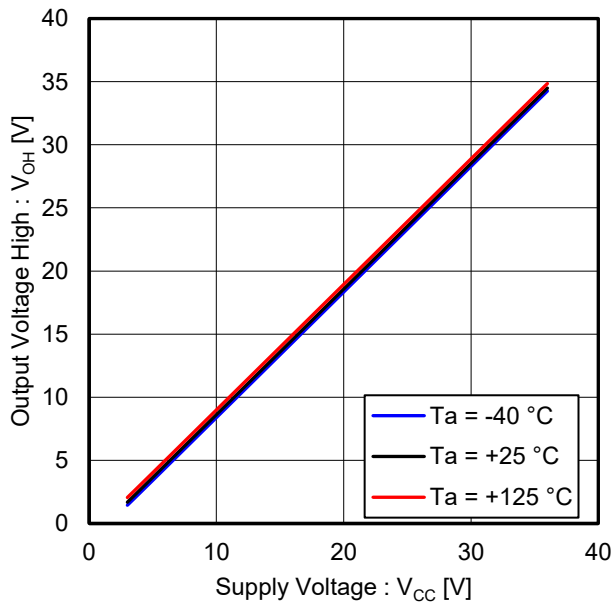


Figure 3. Output Voltage High vs Supply Voltage
($R_L = 10\text{ k}\Omega$)

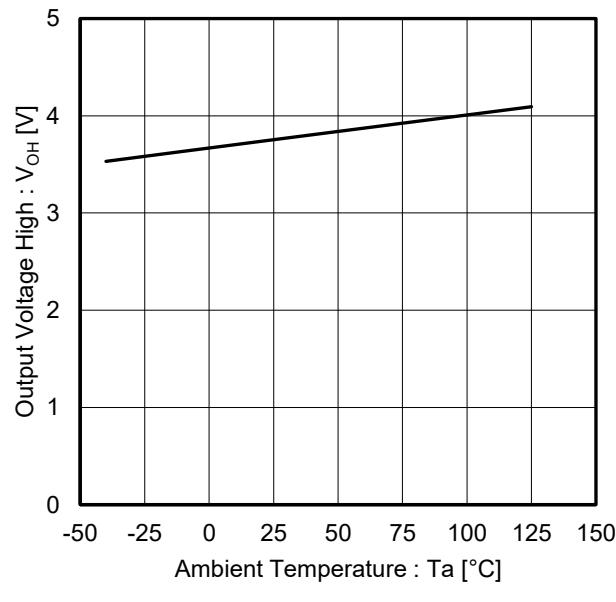


Figure 4. Output Voltage High vs Ambient Temperature
($V_{CC} = 5\text{ V}, R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
 $V_{EE} = 0\text{ V}$

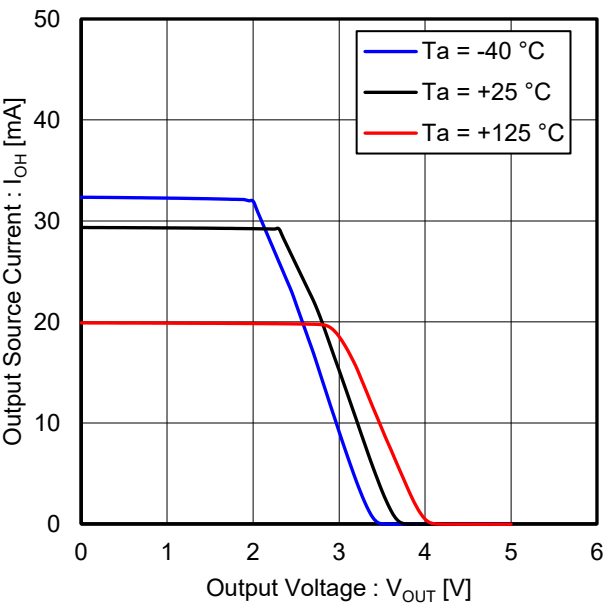


Figure 5. Output Source Current vs Output Voltage
($V_{CC} = 5\text{ V}$)

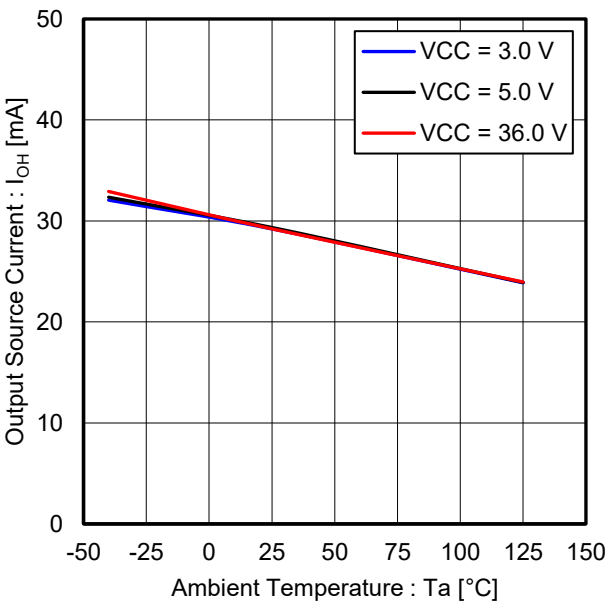


Figure 6. Output Source Current vs Ambient Temperature
($V_{OUT} = 0\text{ V}$)

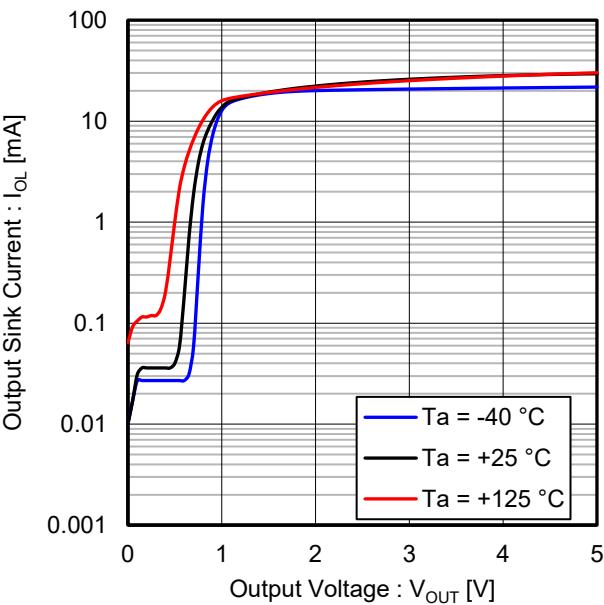


Figure 7. Output Sink Current vs Output Voltage
($V_{CC} = 5\text{ V}$)

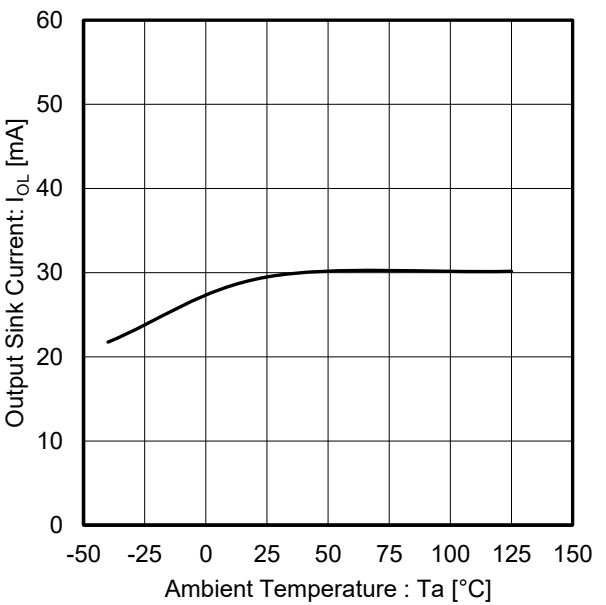


Figure 8. Output Sink Current vs Ambient Temperature
($V_{CC} = 5\text{ V}$, $V_{OUT} = 5\text{ V}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
 $V_{EE} = 0\text{ V}$

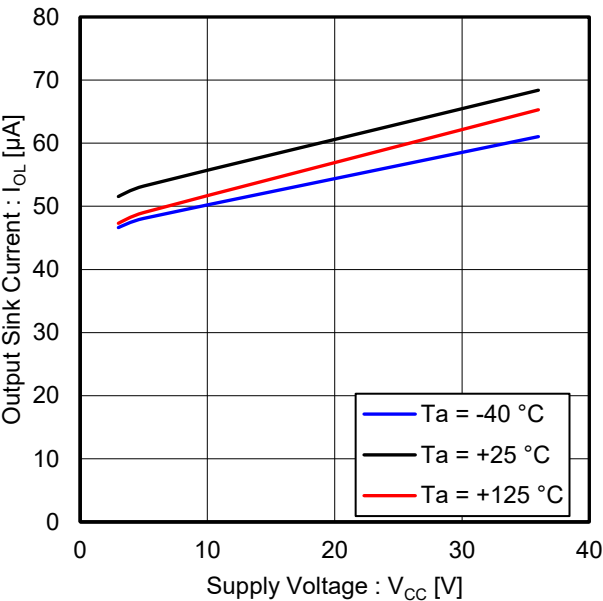


Figure 9. Output Sink Current vs Supply Voltage
($V_{OUT} = 0.2\text{ V}$)

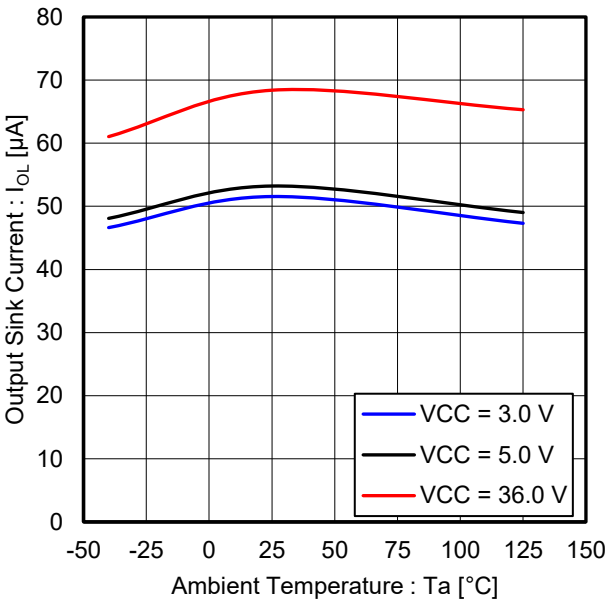


Figure 10. Output Sink Current vs Ambient Temperature
($V_{OUT} = 0.2\text{ V}$)

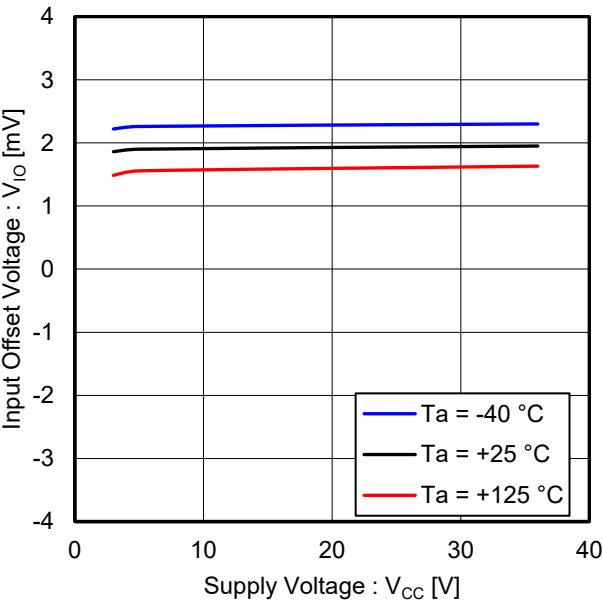


Figure 11. Input Offset Voltage vs Supply Voltage
($V_{ICM} = V_{CC}/2$)

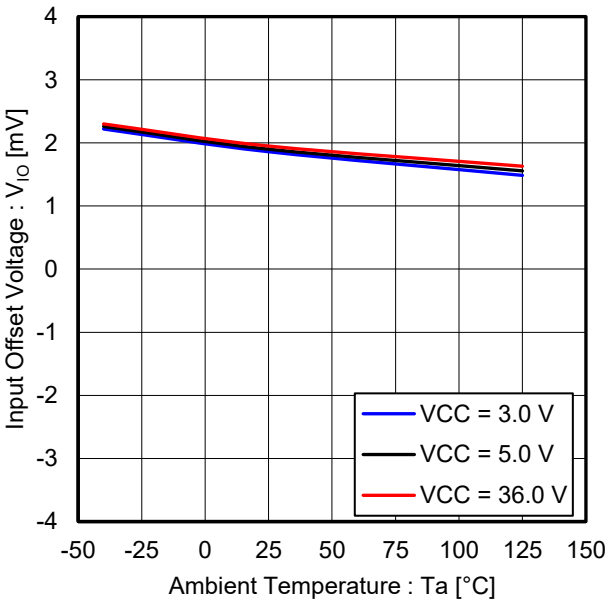


Figure 12. Input Offset Voltage vs Ambient Temperature
($V_{ICM} = V_{CC}/2$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

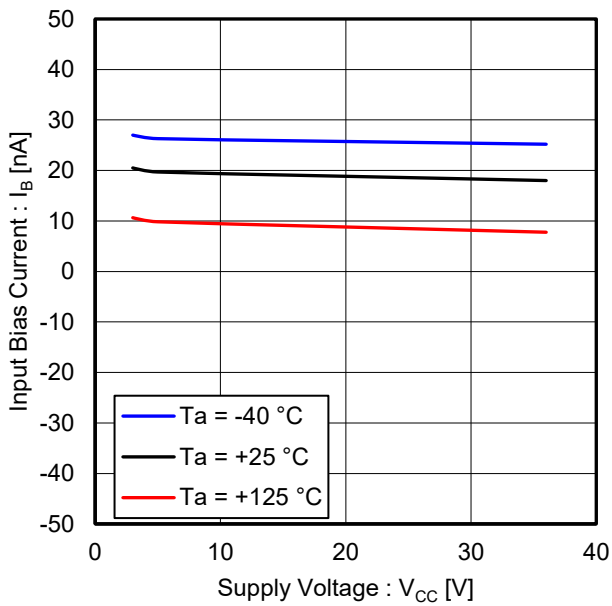
 $V_{EE} = 0\text{ V}$ 

Figure 13. Input Bias Current vs Supply Voltage
($V_{ICM} = V_{CC}/2$)

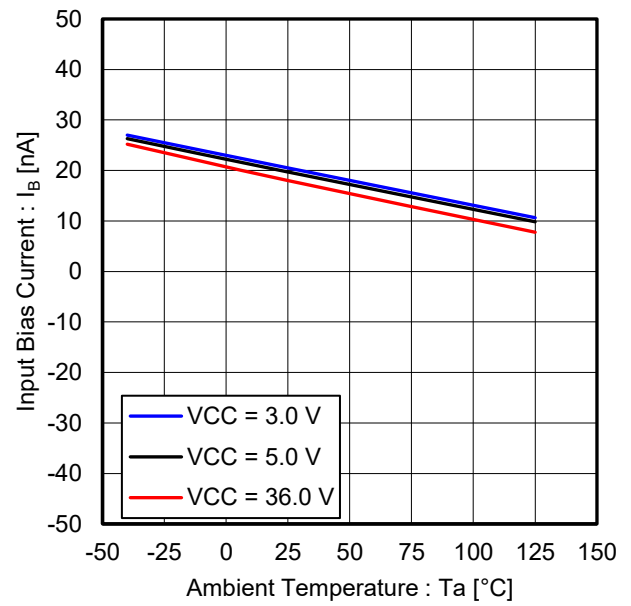


Figure 14. Input Bias Current vs Ambient Temperature
($V_{ICM} = V_{CC}/2$)

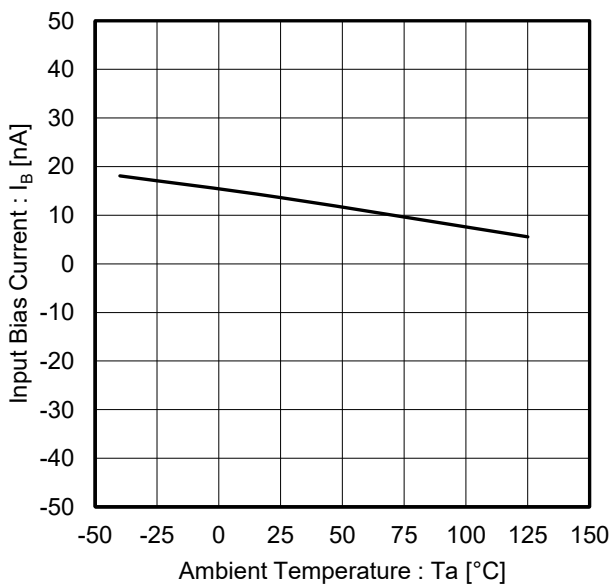


Figure 15. Input Bias Current vs Ambient Temperature
($V_{CC} = 30\text{ V}$, $V_{ICM} = 28\text{ V}$, $V_{OUT} = 1.4\text{ V}$)

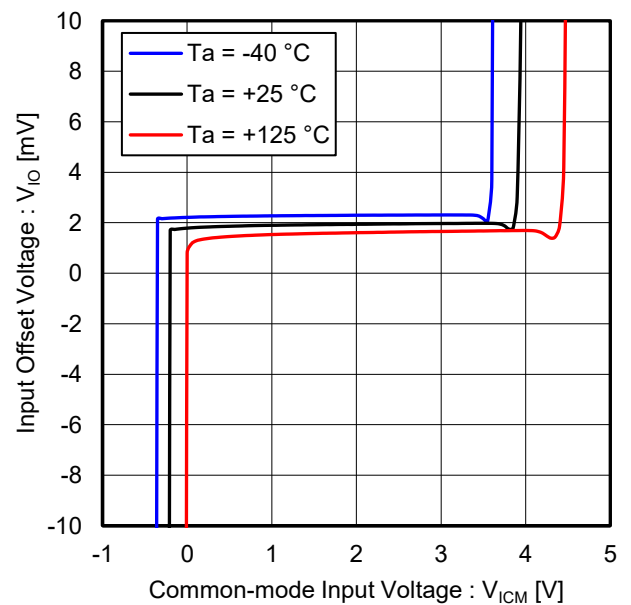


Figure 16. Input Offset Voltage vs Common-mode Input Voltage
($V_{CC} = 5\text{ V}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
 $V_{EE} = 0\text{ V}$

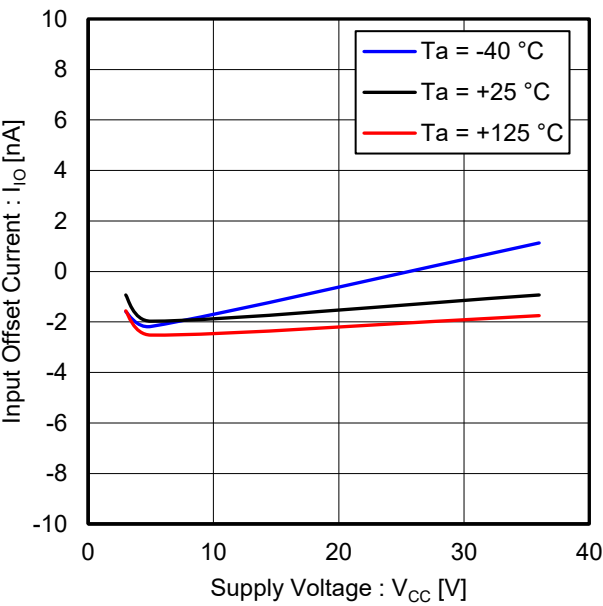


Figure 17. Input Offset Current vs Supply Voltage
($V_{ICM} = V_{CC}/2$)

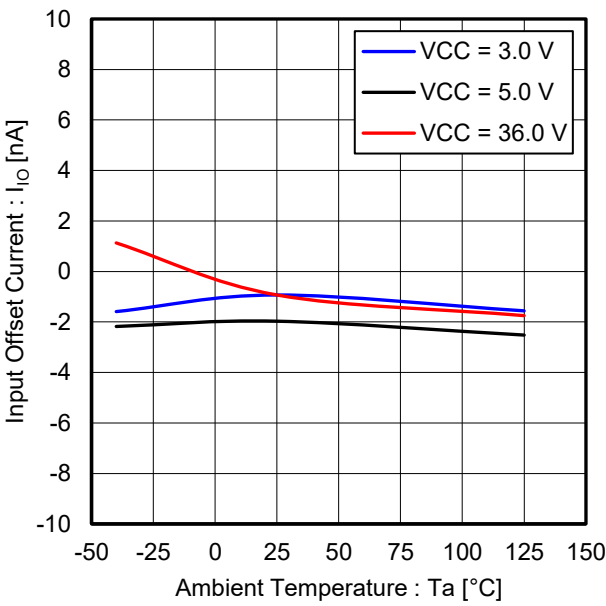


Figure 18. Input Offset Current vs Ambient Temperature
($V_{ICM} = V_{CC}/2$)

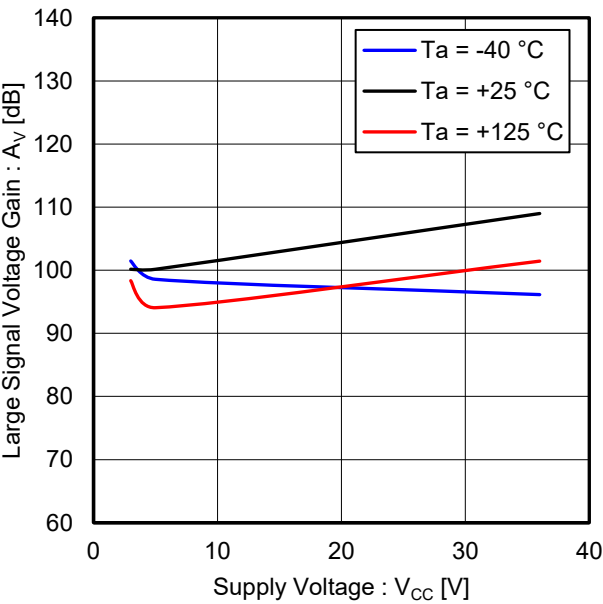


Figure 19. Large Signal Voltage Gain vs Supply Voltage
($R_L = 2\text{ k}\Omega$)

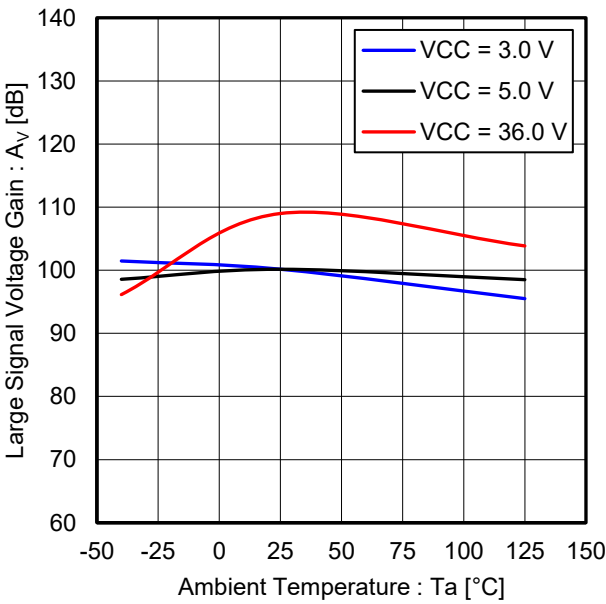


Figure 20. Large Signal Voltage Gain vs Ambient Temperature
($R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = 0\text{ V}$

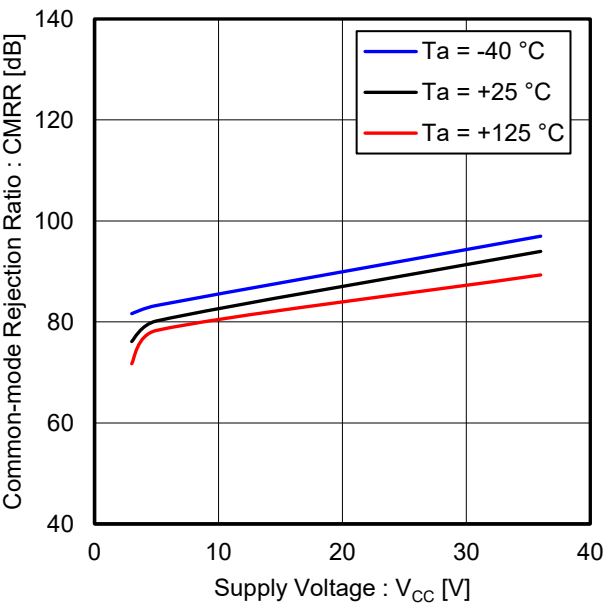


Figure 21. Common-mode Rejection Ratio vs Supply Voltage
($V_{OUT} = 1.4\text{ V}$)

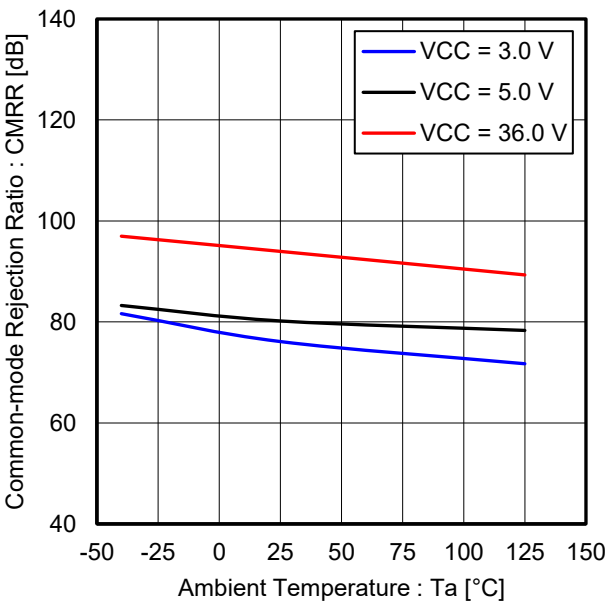


Figure 22. Common-mode Rejection Ratio vs Ambient Temperature
($V_{OUT} = 1.4\text{ V}$)

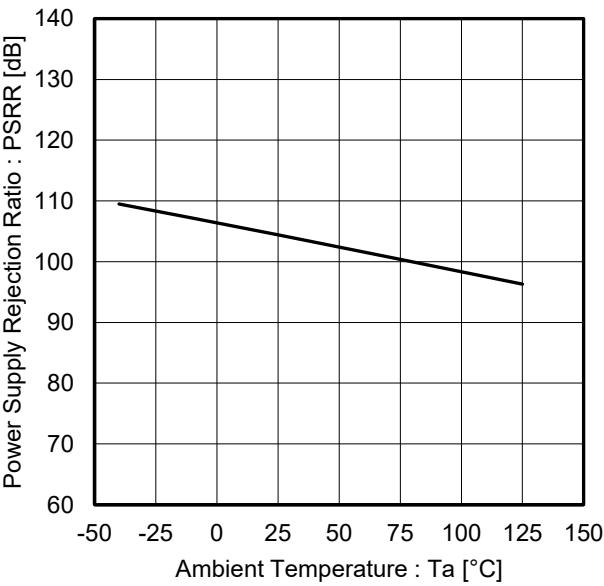


Figure 23. Power Supply Rejection Ratio vs Ambient Temperature
($V_{CC} = 5\text{ V}$)

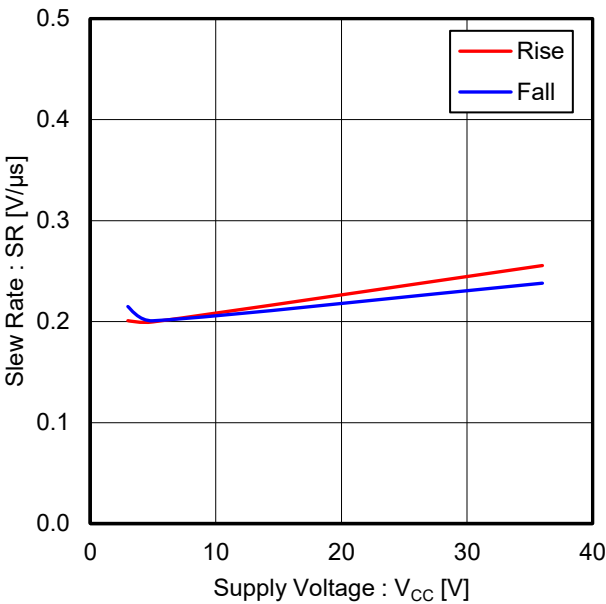


Figure 24. Slew Rate vs Supply Voltage
($T_a = 25^\circ\text{C}$, $R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
 $V_{EE} = 0\text{ V}$

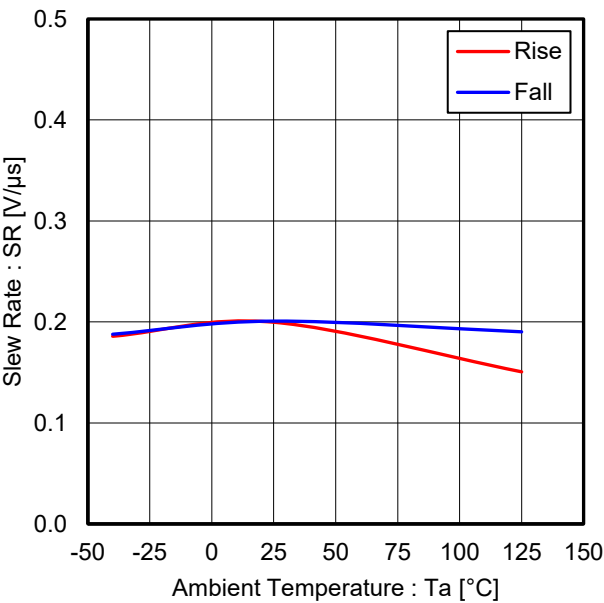


Figure 25. Slew Rate vs Ambient Temperature
($V_{CC} = 5\text{ V}$, $R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Application Information

1. Unused Circuits

When there are unused circuits, it is recommended that they are connected as in right figure, and set the non-inverting input pin to electric potential within the common-mode input voltage range (V_{ICMR}).

2. Input Voltage

Applying $V_{EE} + 36\text{ V}$ to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure circuit operation. Note that the circuit operates normally only when the input voltage is within the common-mode input voltage range of the electric characteristics.

3. Power Supply (single/dual)

The Op-Amp operates when the voltage is supplied between the VCC and VEE pin. Therefore, the single supply Op-Amp can be used as dual supply Op-Amp as well.

4. Output Capacitor

When the VCC pin is shorted to V_{EE} (GND) electric potential in a state where electric charge is accumulated in the external capacitor that is connected to the output pin, the accumulated electric charge flow through parasitic elements or pin protection elements inside the circuit and discharges to the VCC pin. It may cause damage to the elements inside the circuit (thermal destruction). When using this IC as an application circuit which does not constitute a negative feedback circuit and does not occur the oscillation by an output capacitive load such as a voltage comparator, connect a capacitor of $0.1\text{ }\mu\text{F}$ or less to the output pin to prevent IC damage caused by the accumulation of electric charge as mentioned above.

5. Oscillation by Output Capacitor

Pay attention to the oscillation by capacitive load in designing an application which constitutes a negative feedback loop circuit with this IC.

6. Handling the IC

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations of the electrical characteristics due to the piezo resistance effects. Pay attention to defecting or bending the board.

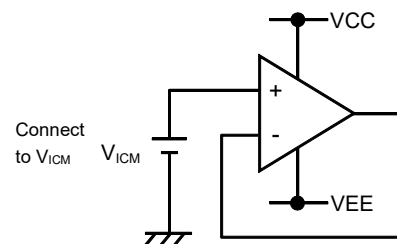


Figure 26. Example of application unused circuit processing

Application Examples

○Voltage Follower

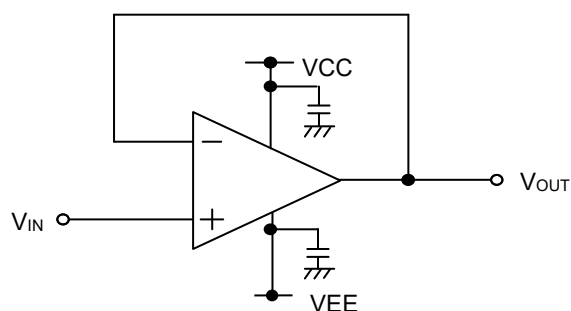


Figure 27. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$$V_{OUT} = V_{IN}$$

○Inverting Amplifier

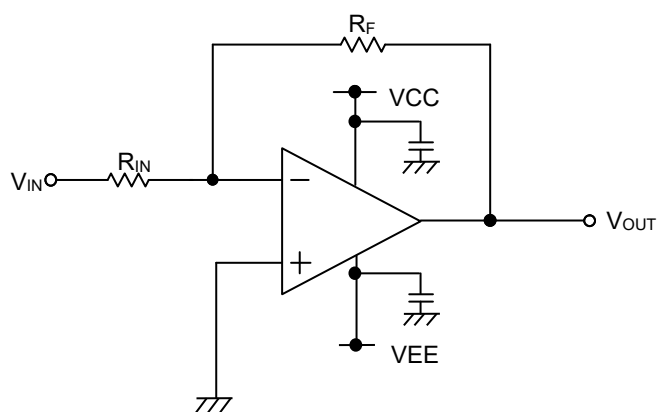


Figure 28. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F , and then it outputs phase-inverted voltage. The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN} .

○Non-inverting Amplifier

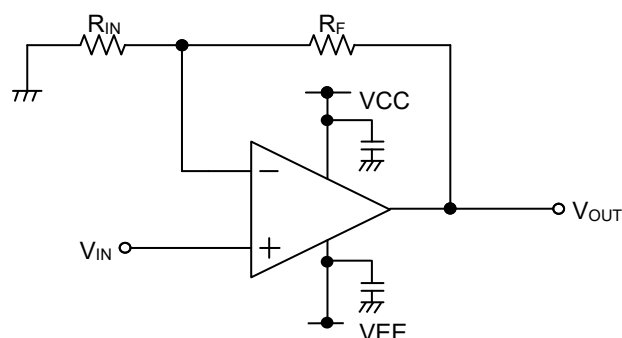


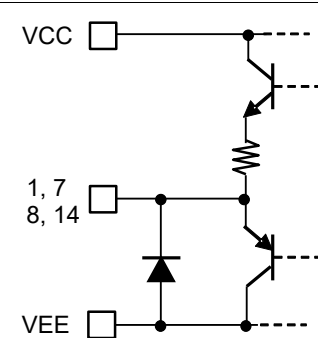
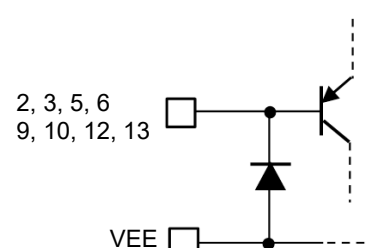
Figure 29. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F . The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1 7 8 14	OUT1 OUT2 OUT3 OUT4	Output	
2 3 5 6 9 10 12 13	-IN1 +IN1 +IN2 -IN2 -IN3 +IN3 +IN4 -IN4	Input	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

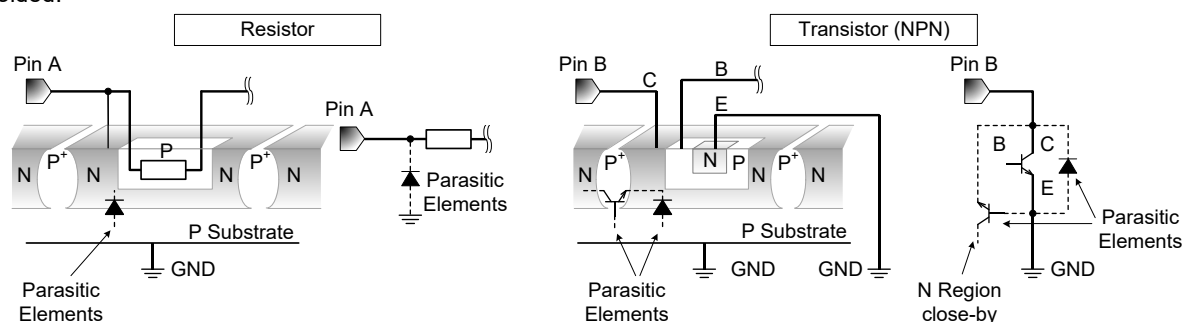
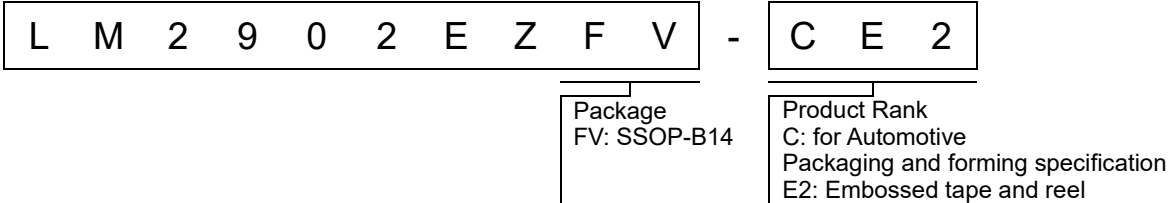


Figure 30. Example of Monolithic IC Structure

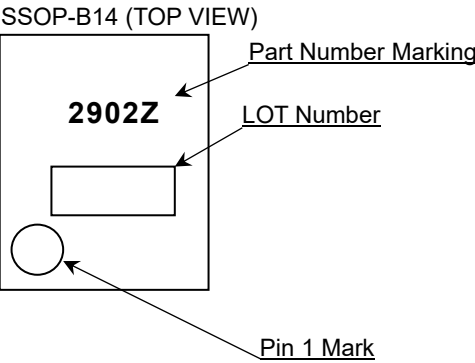
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

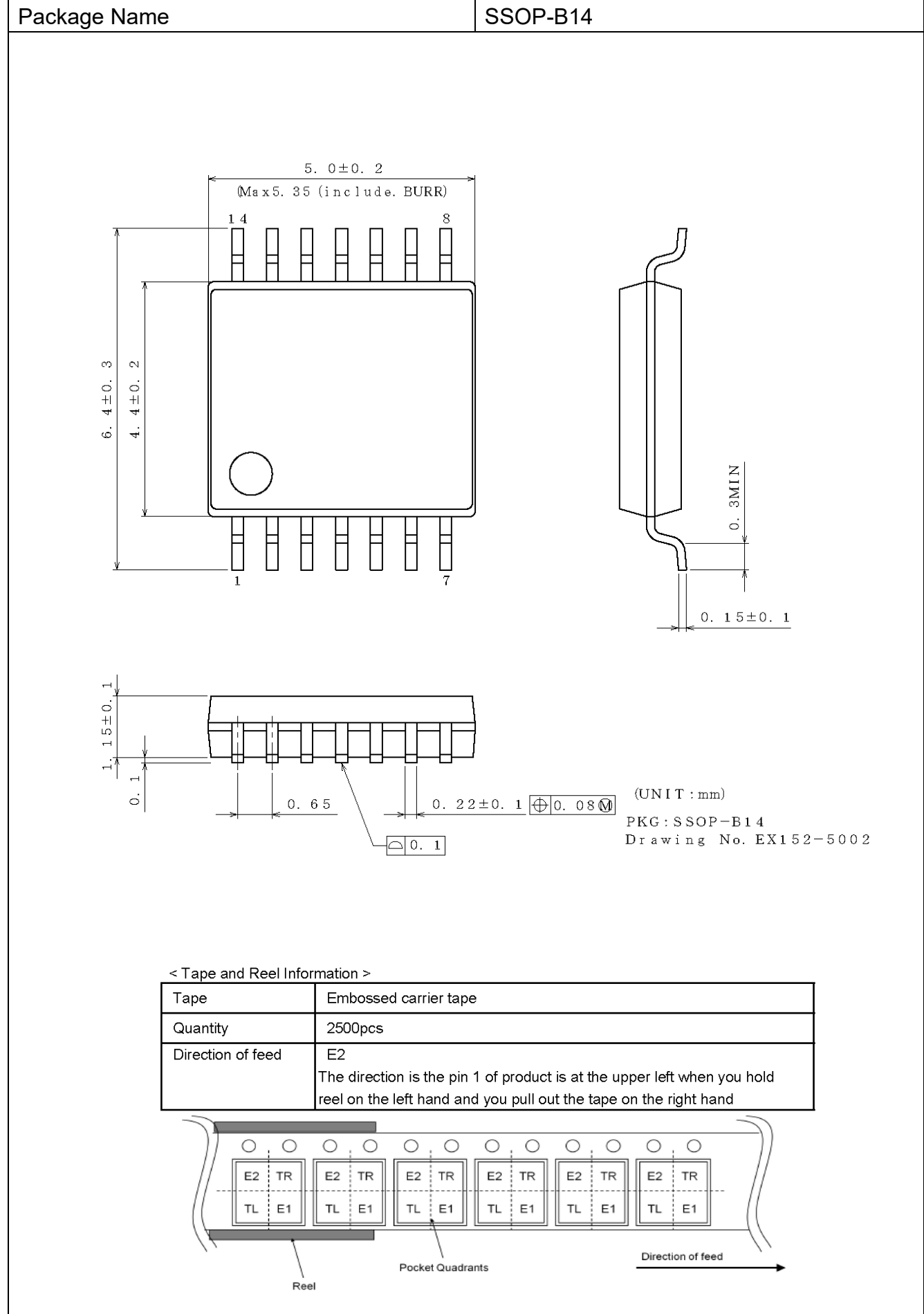
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
25.Nov.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
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 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

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