

Operational Amplifiers

High Speed Operational Amplifiers

LM3472xxx LM3474xx

General Description

LM3472xxx and LM3474xx integrate dual or quad independent high voltage gain Op-amps on a single chip. These have features of high gain bandwidth, high slew rate and operating voltage range is wide with 3 V to 36 V.

Features

- Single or Dual Power Supply Operation
- Wide Operating Supply Voltage Range
- Standard Op-amp Pin-assignments
- High Open-loop Voltage Gain
- Internal ESD Protection Circuit
- Common-mode Input Voltage Range Includes Ground Level, Allowing Direct Ground Sensing
- Wide Output Voltage Range

Applications

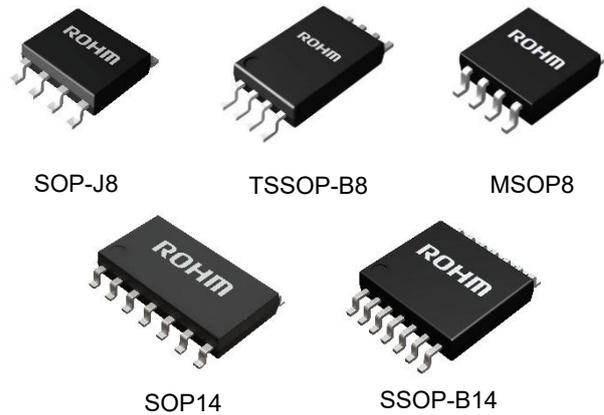
- Current Detection Amplifier
- Buffer Amplifier
- Active Filter
- Consumer Electronics

Key Specifications

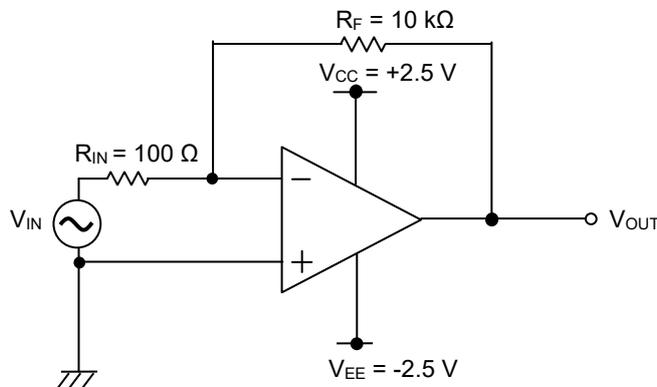
- Operating Supply Voltage Range
Single Supply: 3.0 V to 36.0 V
Dual Supply: ±1.5 V to ±18.0 V
- Temperature Range: -40 °C to +125 °C
- Input Offset Voltage: 10 mV (Max)
- Input Offset Current: 6 nA (Typ)
- Input Bias Current: 100 nA (Typ)
- Output Voltage Range:
($V_S = 30\text{ V}$) $V_{EE} + 0.3\text{ V}$ to $V_{CC} - 1.0\text{ V}$ (Typ)
- Slew Rate: 10 V/ μs (Typ)
- Gain Bandwidth Product: 4 MHz (Typ)

Package

Package	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.9 mm x 6.0 mm x 1.65 mm
TSSOP-B8	3.0 mm x 6.4 mm x 1.2 mm
MSOP8	2.9 mm x 4.0 mm x 0.9 mm
SOP14	8.7 mm x 6.2 mm x 1.71 mm
SSOP-B14	5.0 mm x 6.4 mm x 1.35 mm



Typical Application Circuit

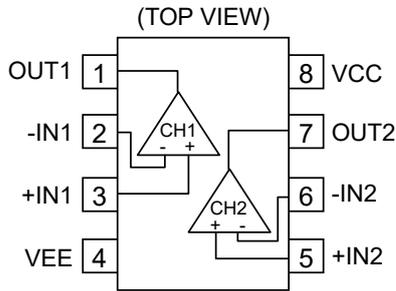


$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

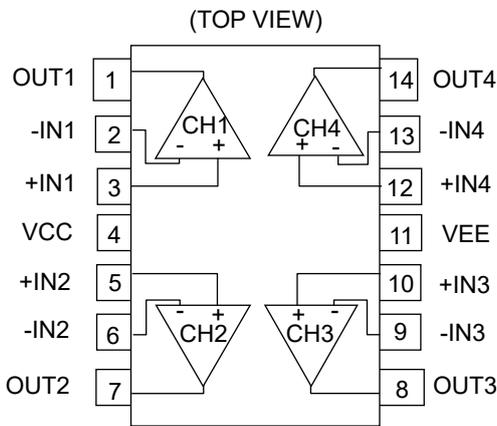
Pin Configurations

LM3472FJ : SOP-J8
 LM3472FVT : TSSOP-B8
 LM3472FVM : MSOP8



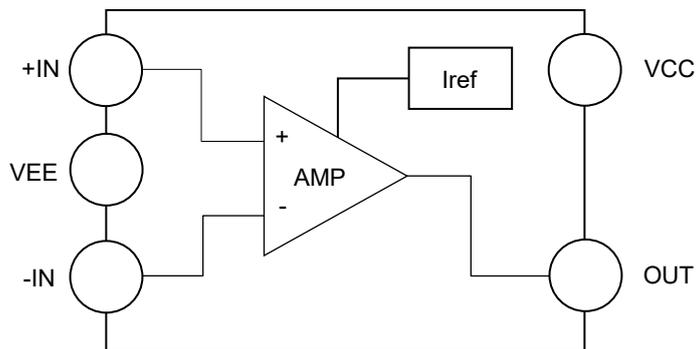
Pin No.	Pin Name	Function
1	OUT1	Output1
2	-IN1	Inverting input1
3	+IN1	Non-inverting input1
4	VEE	Negative power supply / Ground
5	+IN2	Non-inverting input2
6	-IN2	Inverting input2
7	OUT2	Output2
8	VCC	Positive power supply

LM3474F : SOP14
 LM3474FV : SSOP-B14



Pin No.	Pin Name	Function
1	OUT1	Output1
2	-IN1	Inverting input1
3	+IN1	Non-inverting input1
4	VCC	Positive power supply
5	+IN2	Non-inverting input2
6	-IN2	Inverting input2
7	OUT2	Output2
8	OUT3	Output3
9	-IN3	Inverting input3
10	+IN3	Non-inverting input3
11	VEE	Negative power supply / Ground
12	+IN4	Non-inverting input4
13	-IN4	Inverting input4
14	OUT4	Output4

Block Diagram



(Per 1ch. Iref is common to all channel.)

Description of Blocks

- AMP: This block is an operational amplifier with a wide operating supply voltage range, a high slew rate (10 V/μs) and high-gain bandwidth product (4 MHz).
- Iref: This block supplies reference current which is needed to operate AMP block.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage (V _{CC} - V _{EE})	V _S	36	V
Differential Input Voltage ^(Note 1)	V _{ID}	36	V
Common-mode Input Voltage Range	V _{ICMR}	(V _{EE} - 0.3) to (V _{EE} + 36.0)	V
Input Current	I _I	±10	mA
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	T _{jmax}	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to V_{EE} or more.

Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
SOP-J8				
Junction to Ambient	θ _{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	18	11	°C/W
TSSOP-B8				
Junction to Ambient	θ _{JA}	251.9	152.1	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	31	20	°C/W
MSOP8				
Junction to Ambient	θ _{JA}	284.1	135.4	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	21	11	°C/W
SOP14				
Junction to Ambient	θ _{JA}	166.5	108.1	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	26	22	°C/W
SSOP-B14				
Junction to Ambient	θ _{JA}	159.6	92.8	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	13	9	°C/W

(Note 2) Based on JESD51-2A (Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating Supply Voltage ($V_{CC} - V_{EE}$)	Single Supply	Vs	3.0	5.0	36.0	V
	Dual Supply		± 1.5	± 2.5	± 18.0	
Operating Temperature		Topr	-40	+25	+125	$^{\circ}\text{C}$

Electrical Characteristics (Unless otherwise specified $V_S = 30\text{ V}$, $V_{EE} = -15\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	1	10	mV	$V_{OUT} = 0\text{ V}$ Absolute value
Input Offset Current	I_{IO}	-	6	75	nA	$V_{OUT} = 0\text{ V}$ Absolute value
Input Bias Current ^(Note 1)	I_B	-	100	150	nA	$V_{OUT} = 0\text{ V}$
Supply Current	I_{CC}	-	2.0	2.5	mA/Ch	$R_L = \infty$
Output Voltage High	V_{OH}	3.7	4.0	-	V	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 2\text{ k}\Omega$
		13.7	14.0	-		$R_L = 10\text{ k}\Omega$
		13.5	-	-		$R_L = 2\text{ k}\Omega$
Output Voltage Low	V_{OL}	-	0.1	0.3	V	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $R_L = 2\text{ k}\Omega$
		-	-14.7	-14.3		$R_L = 10\text{ k}\Omega$
		-	-	-13.5		$R_L = 2\text{ k}\Omega$
Large Signal Voltage Gain	A_v	80	100	-	dB	$R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$
Common-mode Input Voltage Range	V_{ICMR}	0	-	3.0	V	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{OUT} = V_S / 2$
Common-mode Rejection Ratio	CMRR	60	80	-	dB	$V_{OUT} = 0\text{ V}$
Power Supply Rejection Ratio	PSRR	60	90	-	dB	$V_{OUT} = 0\text{ V}$
Output Source Current ^(Note 2)	I_{SOURCE}	10	30	-	mA	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{+IN} = 1\text{ V}$, $V_{-IN} = 0\text{ V}$ $V_{OUT} = 0\text{ V}$, 1 CH is short circuit
Output Sink Current ^(Note 2)	I_{SINK}	20	70	-	mA	$V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$, $V_{+IN} = 0\text{ V}$, $V_{-IN} = 1\text{ V}$ $V_{OUT} = 5\text{ V}$, 1 CH is short circuit
Gain Bandwidth Product	GBW	-	4	-	MHz	-
Slew Rate	SR	-	10	-	V/ μs	$V_{IN} = -10\text{ V}$ to $+10\text{ V}$, $G = 0\text{ dB}$, $R_L = 2\text{ k}\Omega$
Channel Separation	CS	-	120	-	dB	-

(Note 1) Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

(Note 2) Under high temperatures, please consider the power dissipation when selecting the output current. When the output pin is continuously shorted the output current reduces the internal temperature by flushing.

Typical Performance Curves

$V_{EE} = -15\text{ V}$

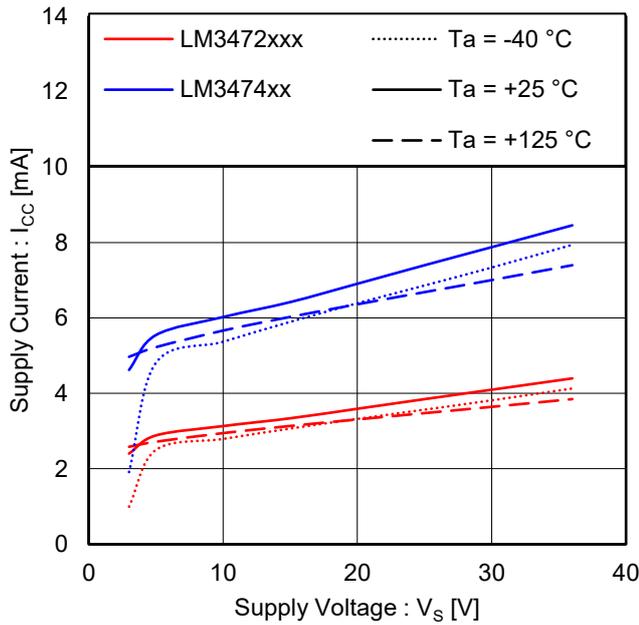


Figure 1. Supply Current vs Supply Voltage
($V_{ICM} = V_S / 2$, $G = 0\text{ dB}$)

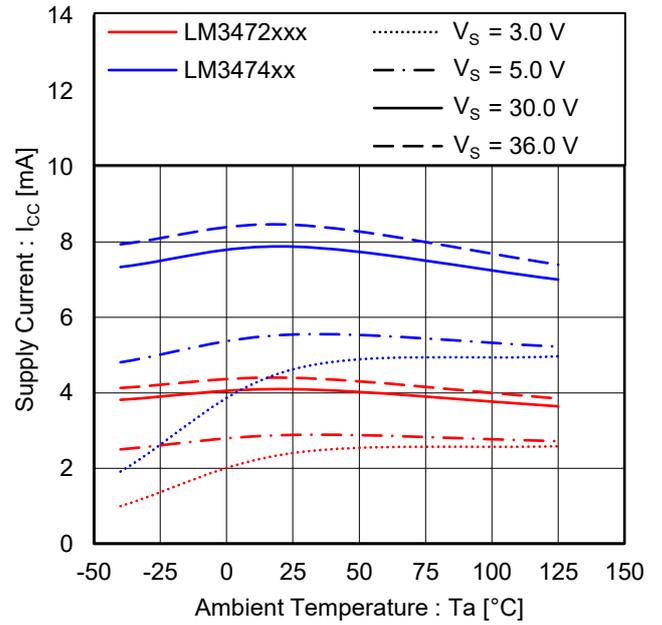


Figure 2. Supply Current vs Ambient Temperature
($V_{ICM} = V_S / 2$, $G = 0\text{ dB}$)

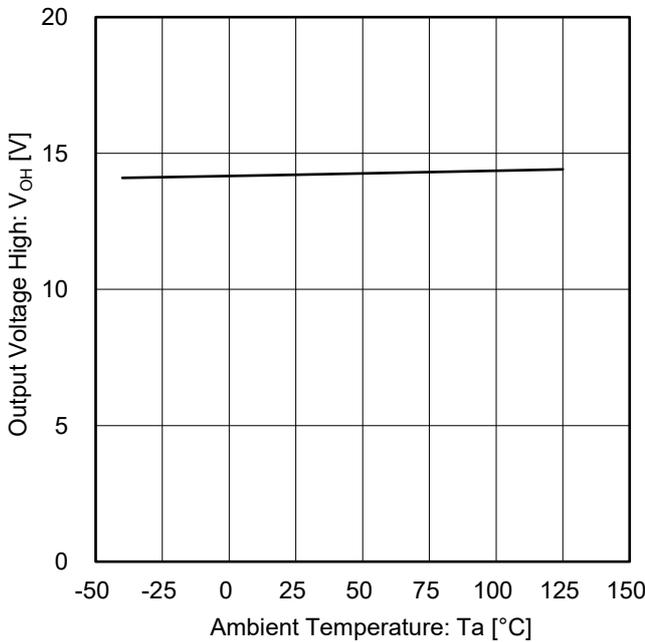


Figure 3. Output Voltage High vs Ambient Temperature
($V_S = 30\text{ V}$, $R_L = 10\text{ k}\Omega$)

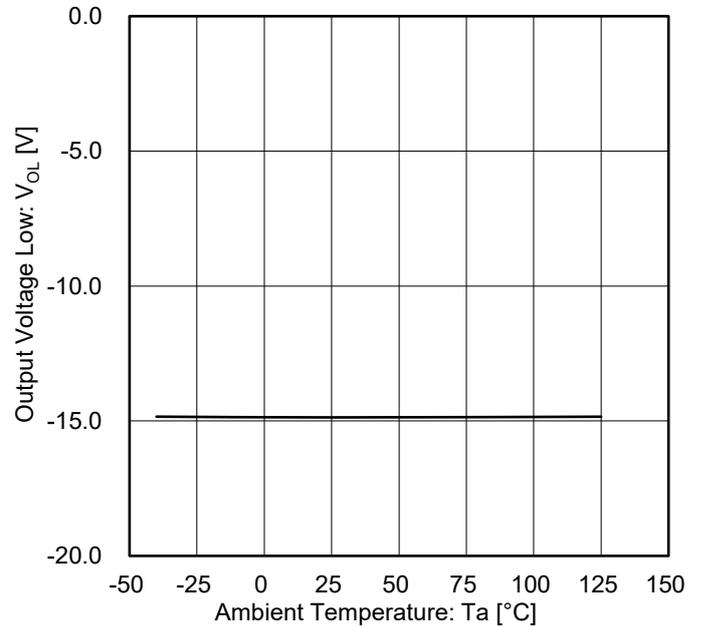


Figure 4. Output Voltage Low vs Ambient Temperature
($V_S = 30\text{ V}$, $R_L = 10\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = -15\text{ V}$

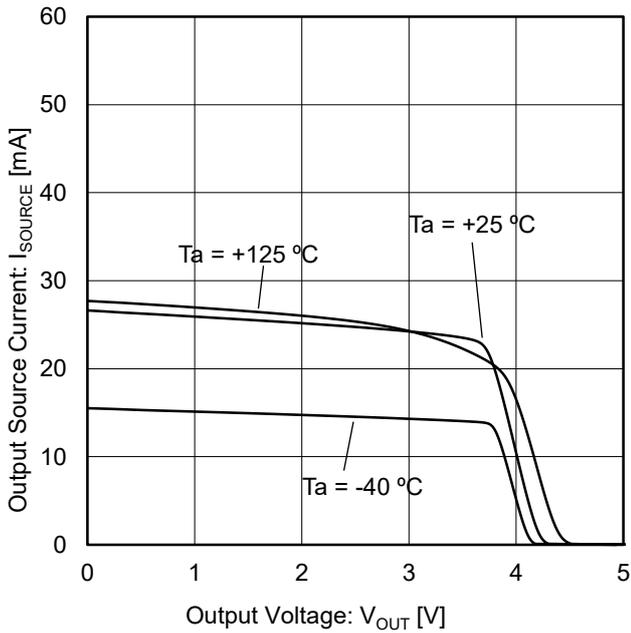


Figure 5. Output Source Current vs Output Voltage ($V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$)

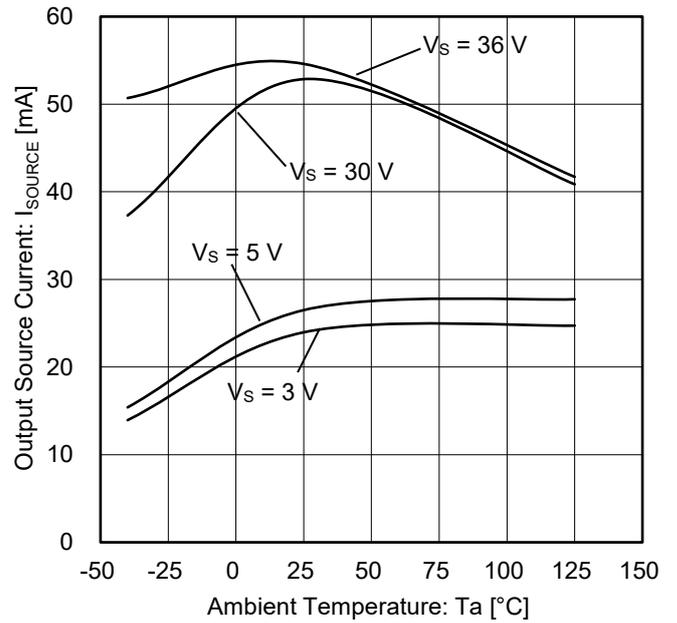


Figure 6. Output Source Current vs Ambient Temperature ($V_{OUT} = 0\text{ V}$, $V_{EE} = 0\text{ V}$)

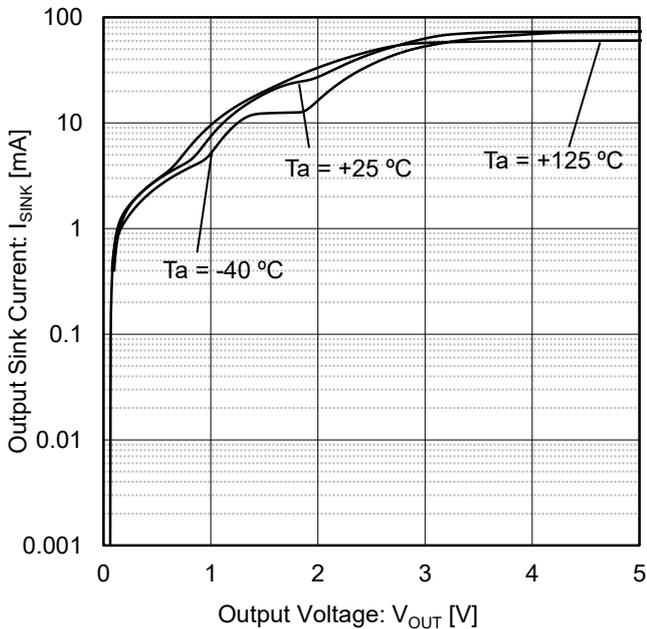


Figure 7. Output Sink Current vs Output Voltage ($V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$)

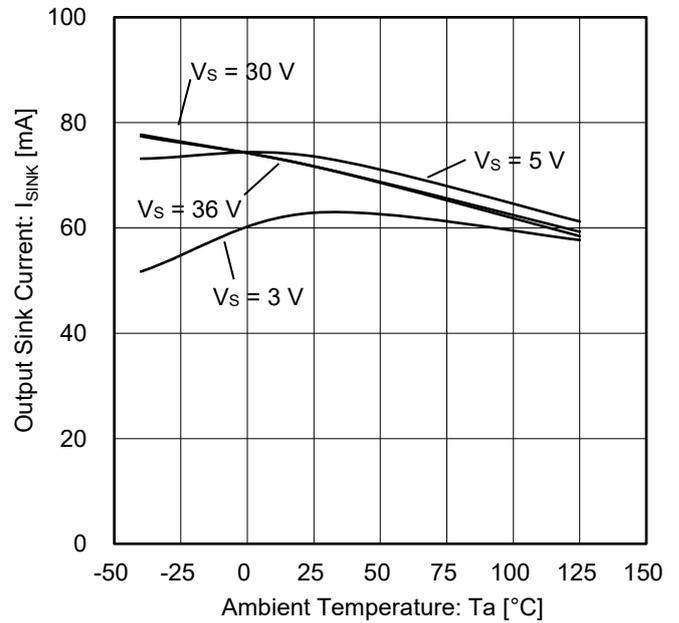


Figure 8. Output Sink Current vs Ambient Temperature ($V_{OUT} = V_S$, $V_{EE} = 0\text{ V}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = -15\text{ V}$

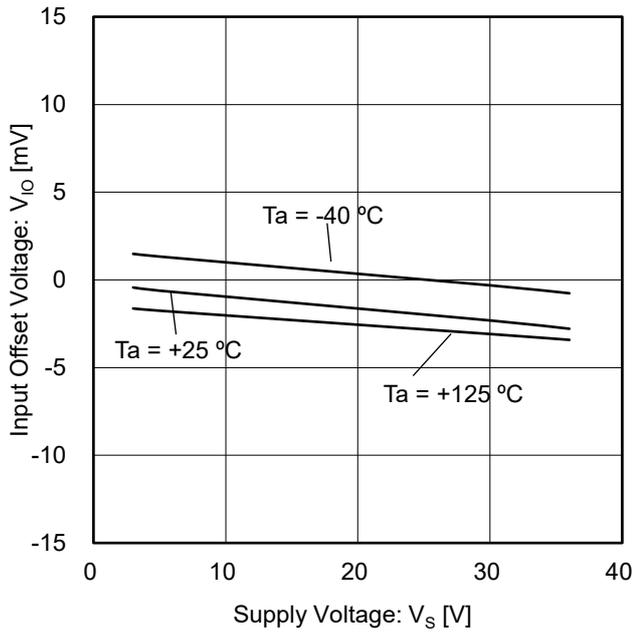


Figure 9. Input Offset Voltage vs Supply Voltage ($V_{ICM} = V_s / 2, V_{OUT} = V_s / 2$)

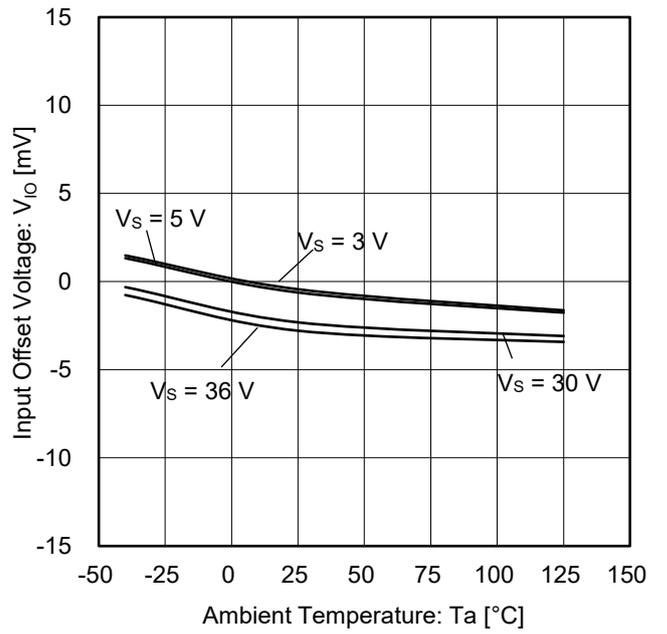


Figure 10. Input Offset Voltage vs Ambient Temperature ($V_{ICM} = V_s / 2, V_{OUT} = V_s / 2$)

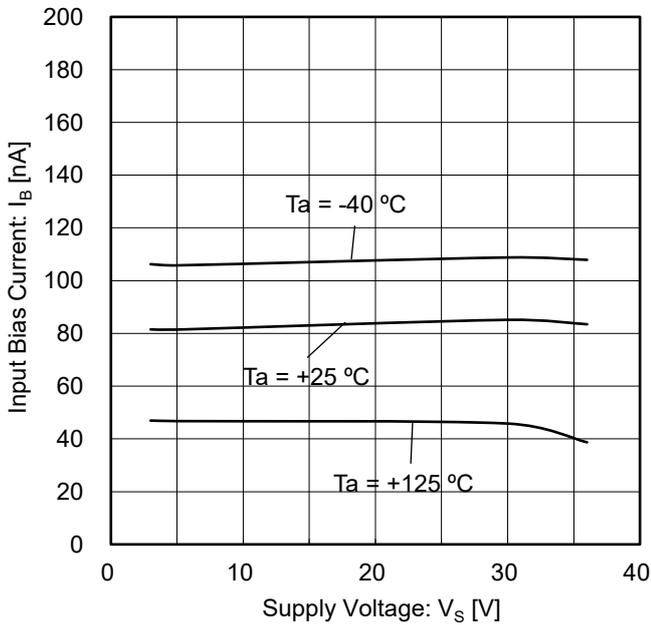


Figure 11. Input Bias Current vs Supply Voltage ($V_{ICM} = V_s / 2, V_{OUT} = V_s / 2$)

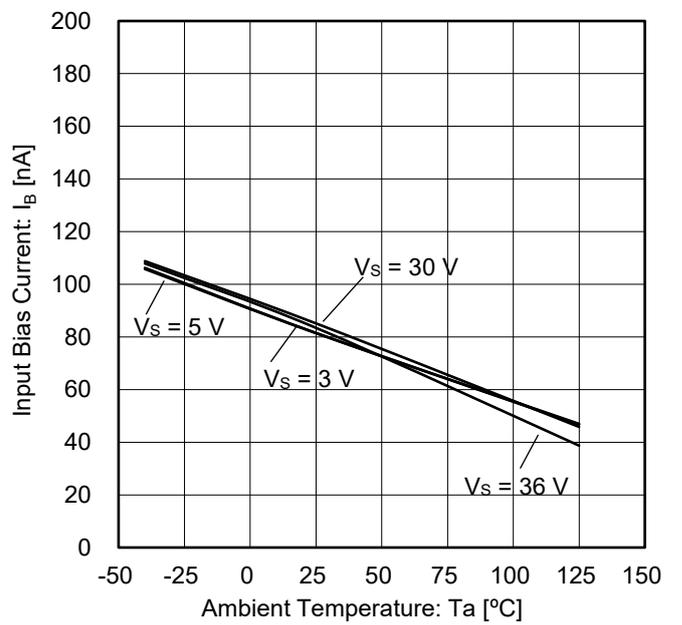


Figure 12. Input Bias Current vs Ambient Temperature ($V_{ICM} = V_s / 2, V_{OUT} = V_s / 2$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = -15\text{ V}$

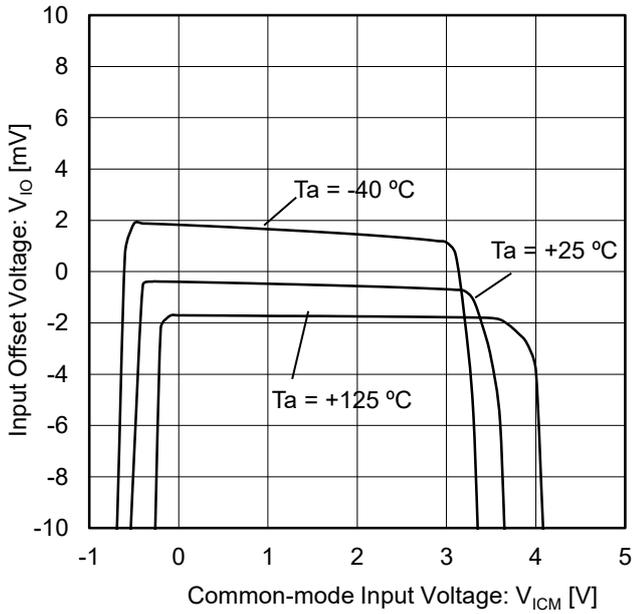


Figure 13. Input Offset Voltage vs Common-mode Input Voltage ($V_S = 5\text{ V}$, $V_{EE} = 0\text{ V}$)

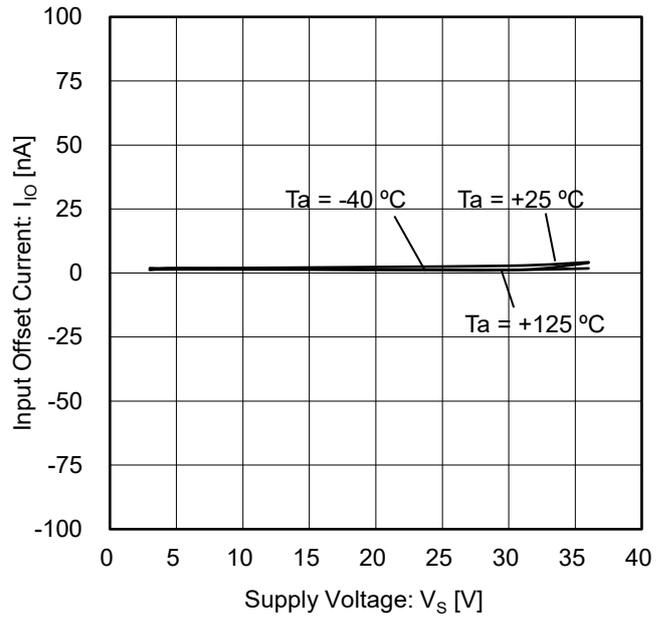


Figure 14. Input Offset Current vs Supply Voltage ($V_{ICM} = V_S / 2$, $V_{OUT} = V_S / 2$)

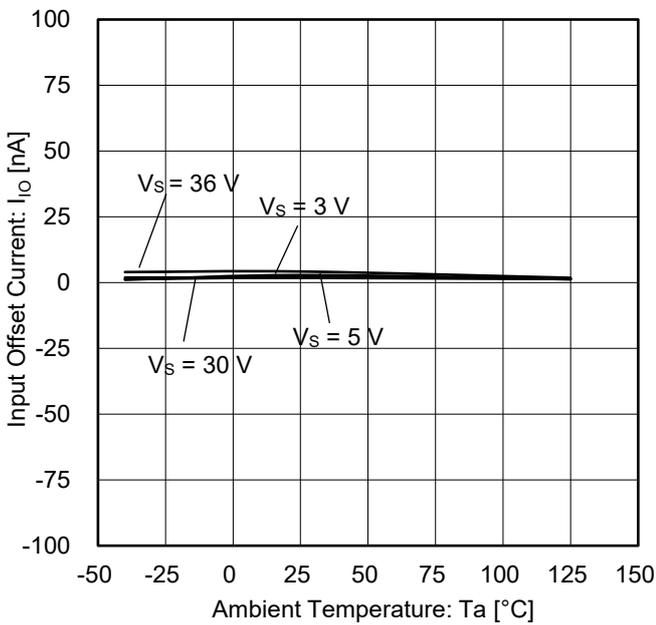


Figure 15. Input Offset Current vs Ambient Temperature ($V_{ICM} = V_S / 2$, $V_{OUT} = V_S / 2$)

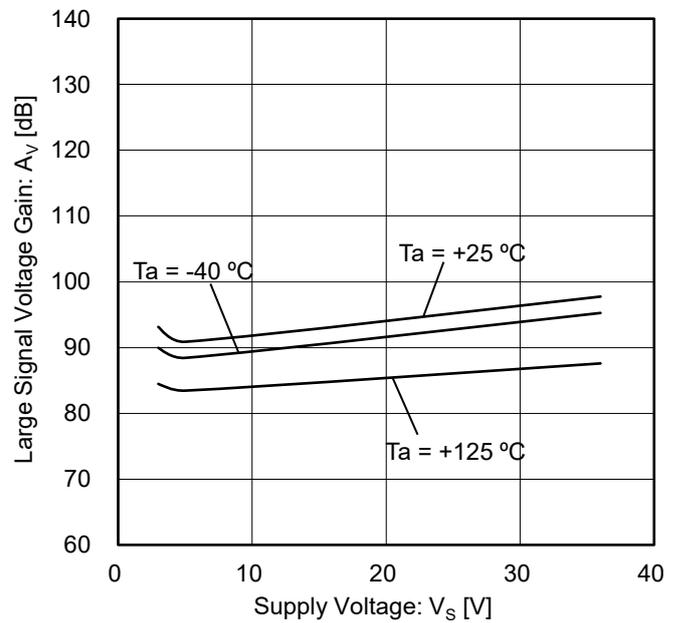


Figure 16. Large Signal Voltage Gain vs Supply Voltage ($R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = -15\text{ V}$

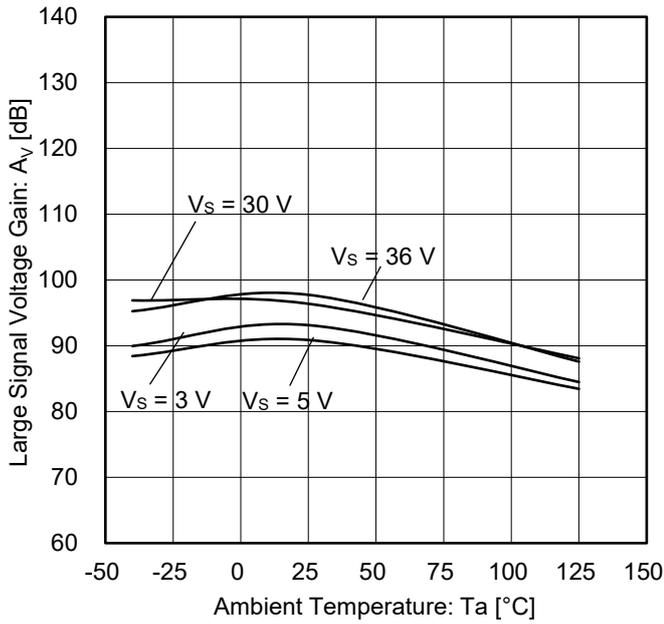


Figure 17. Large Signal Voltage Gain vs Ambient Temperature ($R_L = 2\text{ k}\Omega$)

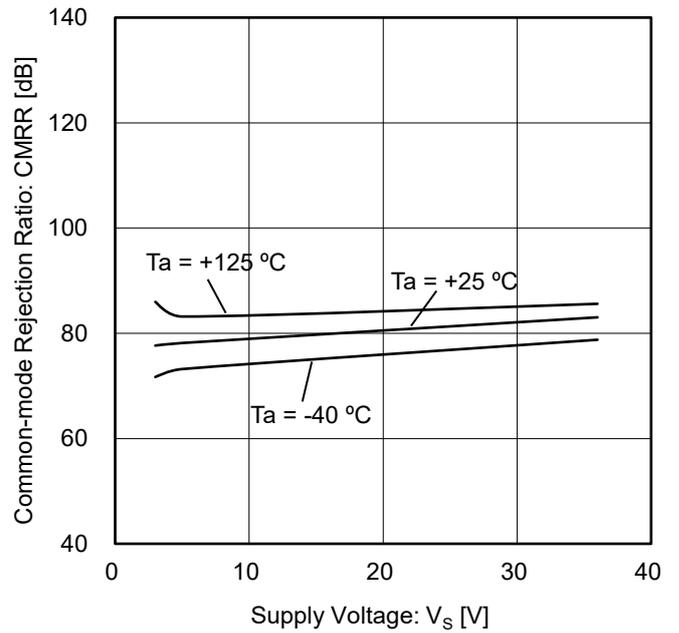


Figure 18. Common-mode Rejection Ratio vs Supply Voltage

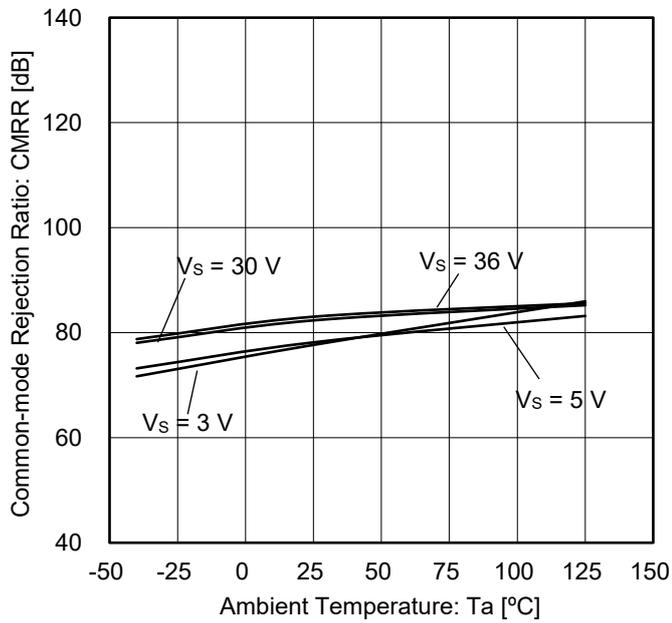


Figure 19. Common-mode Rejection Ratio vs Ambient Temperature

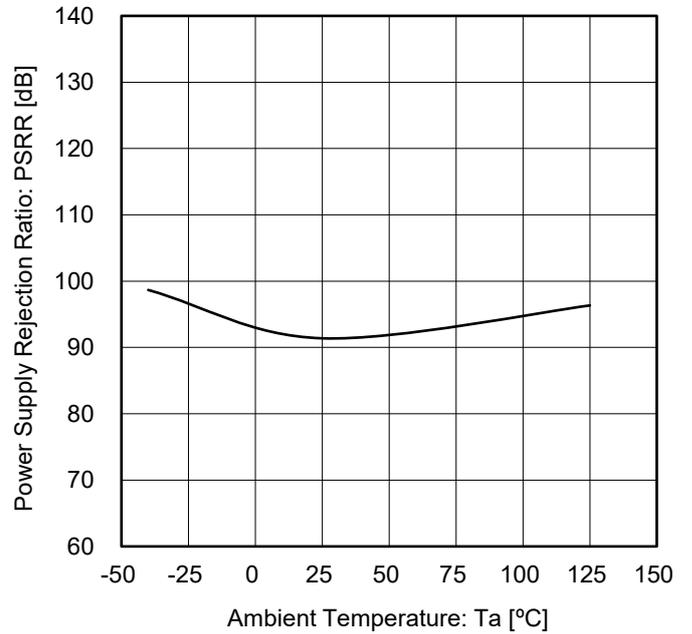


Figure 20. Power Supply Rejection Ratio vs Ambient Temperature

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

$V_{EE} = -15\text{ V}$

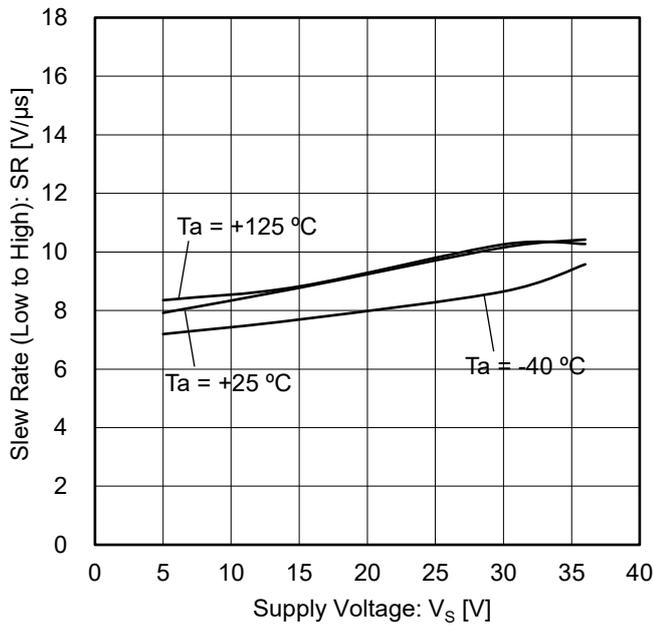


Figure 21. Slew Rate (Low to High) vs Supply Voltage ($R_L = 2\text{ k}\Omega$)

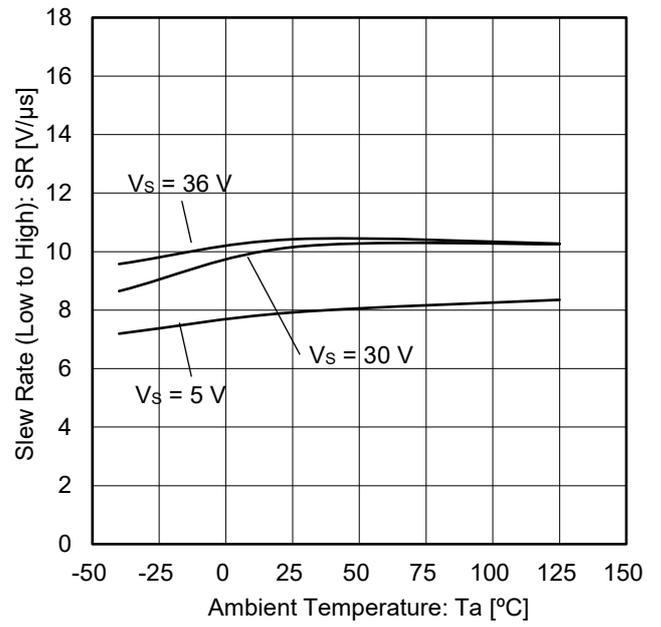


Figure 22. Slew Rate (Low to High) vs Ambient Temperature ($R_L = 2\text{ k}\Omega$)

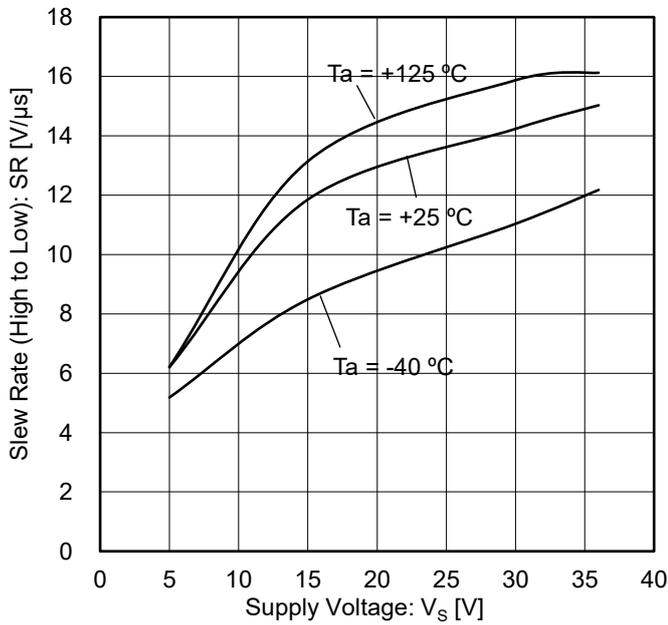


Figure 23. Slew Rate (High to Low) vs Supply Voltage ($R_L = 2\text{ k}\Omega$)

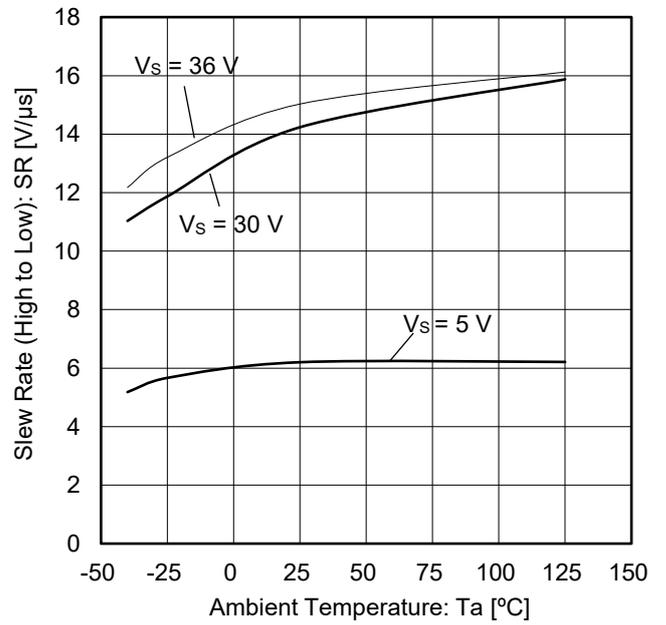


Figure 24. Slew Rate (High to Low) vs Ambient Temperature ($R_L = 2\text{ k}\Omega$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued

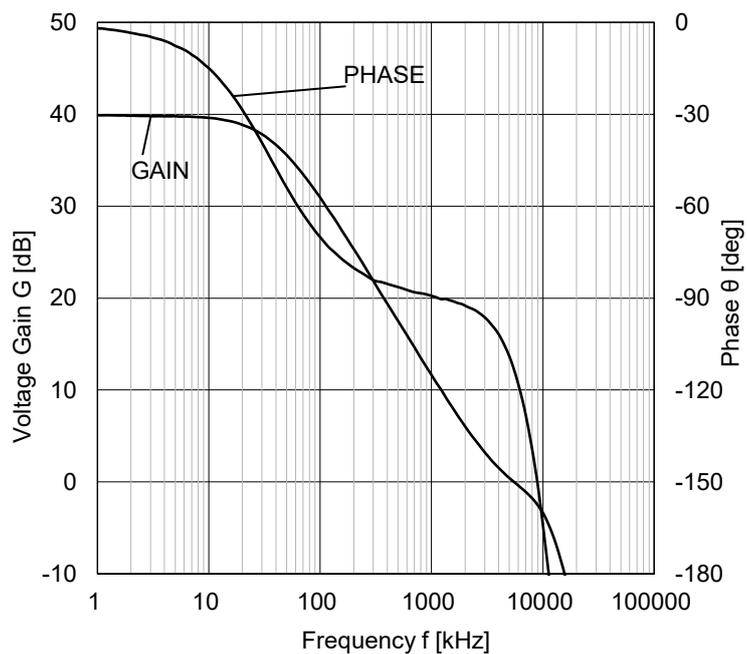
 $V_{EE} = -15\text{ V}$ 

Figure 25.
Voltage Gain, Phase vs Frequency
($V_S = 30\text{ V}$, $A_V = 40\text{ dB}$
 $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $T_a = 25\text{ }^\circ\text{C}$)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Application Information

1) Unused Circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 26, setting the non-inverting input pin within the Common-mode Input Voltage Range (V_{ICMR}).

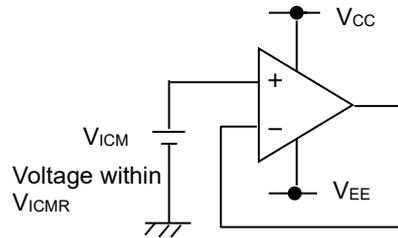


Figure 26. Example of application circuit for unused op-amp

2) Input Voltage

Applying $V_{EE} + 36$ V to the input pin is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the Common-mode Input Voltage range of the electric characteristics.

3) Power Supply (Single / Dual)

The op-amp operates when the voltage supplied is between V_{CC} and V_{EE} . Therefore, the single supply op-amp can be used as dual supply op-amp as well.

4) IC Handling

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuations of the electrical characteristics due to piezo resistance effects. Please pay attention to deflecting or bending the board.

5) Output Capacitor

When the V_{CC} pin is shorted to V_{EE} (GND) electric potential in a state where electric charge is accumulated in the external capacitor that is connected to the output pin, the accumulated electric charge will flow through parasitic elements or pin protection elements inside the circuit and discharges to the V_{CC} pin and thus may cause damage to the internal circuit (by thermal destruction). When using this IC as a comparator, when not used in a negative feedback circuit, and when used in an application circuit where an output capacitive load does not cause oscillations, please set the value of the capacitor connected to the output pin to $0.1 \mu\text{F}$ or less to prevent IC damage caused by the accumulation of electric charge as mentioned above.

6) Oscillation by Output Capacitor

Please pay attention to the oscillation by capacitive load and in designing an application of constitutes a negative feedback loop circuit with these ICs.

Application Examples

oVoltage Follower

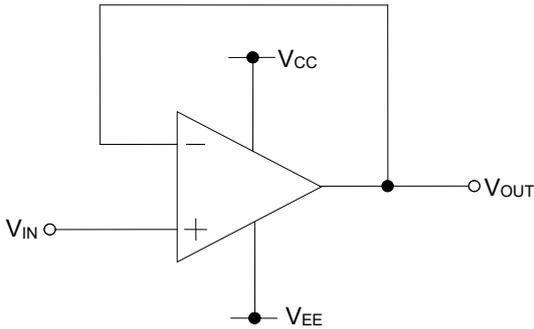


Figure 27. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage due to high input impedance and low output impedance. Computation for output voltage is shown below.

$$V_{OUT} = V_{IN}$$

oInverting Amplifier

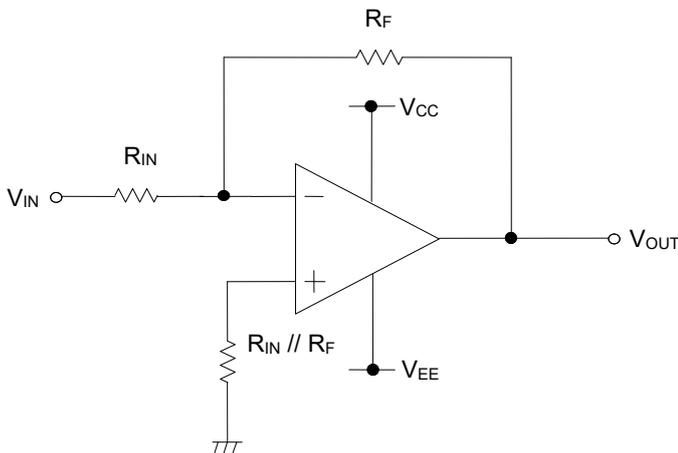


Figure 28. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F , and then it outputs phase-inverted voltage (V_{OUT}). The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN} .

oNon-inverting Amplifier

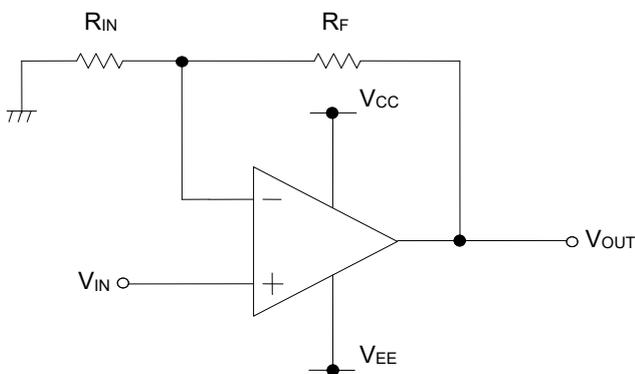


Figure 29. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F . The output voltage (V_{OUT}) is in-phase with the input voltage and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

OLM3472FJ, LM3472FVT, LM3472FVM

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1 7	OUT1 OUT2	Output	
2 3 5 6	-IN1 +IN1 +IN2 -IN2	Input	

OLM3474F, LM3474FV

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1 7 8 14	OUT1 OUT2 OUT3 OUT4	Output	
2 3 5 6 9 10 12 13	-IN1 +IN1 +IN2 -IN2 -IN3 +IN3 +IN4 -IN4	Input	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

- When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
- When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

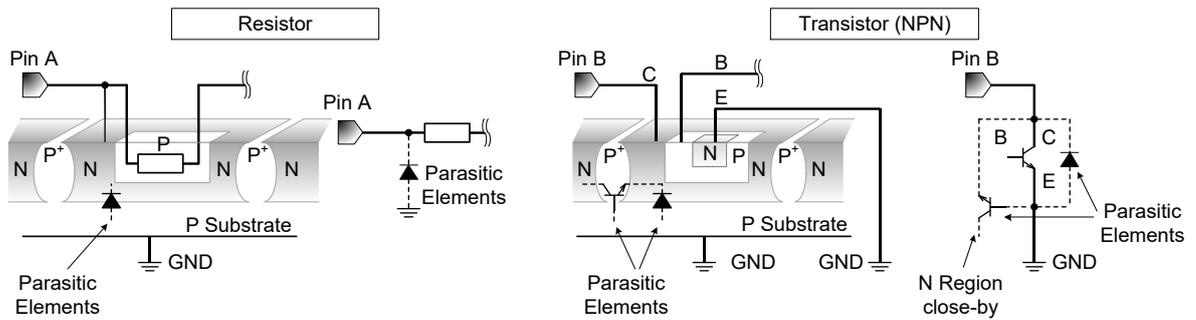
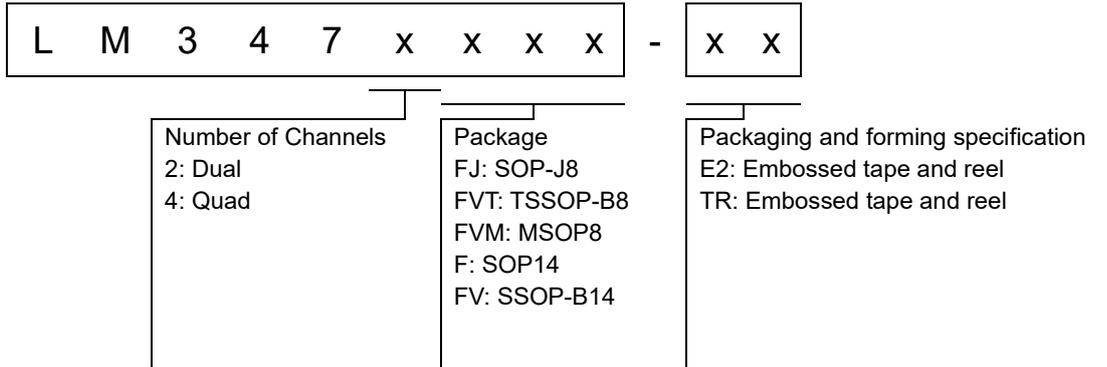


Figure 30. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

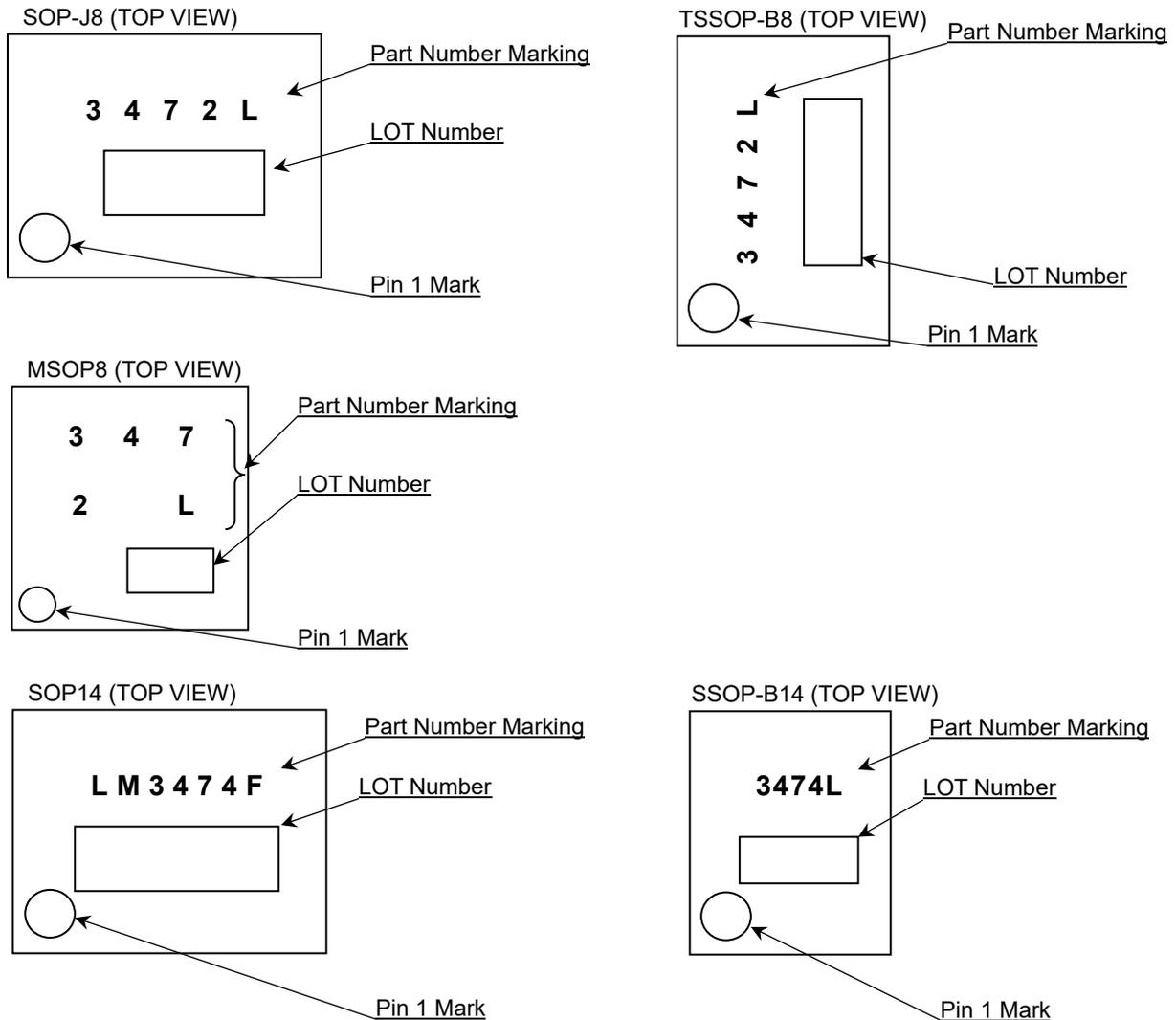
Ordering Information



Lineup

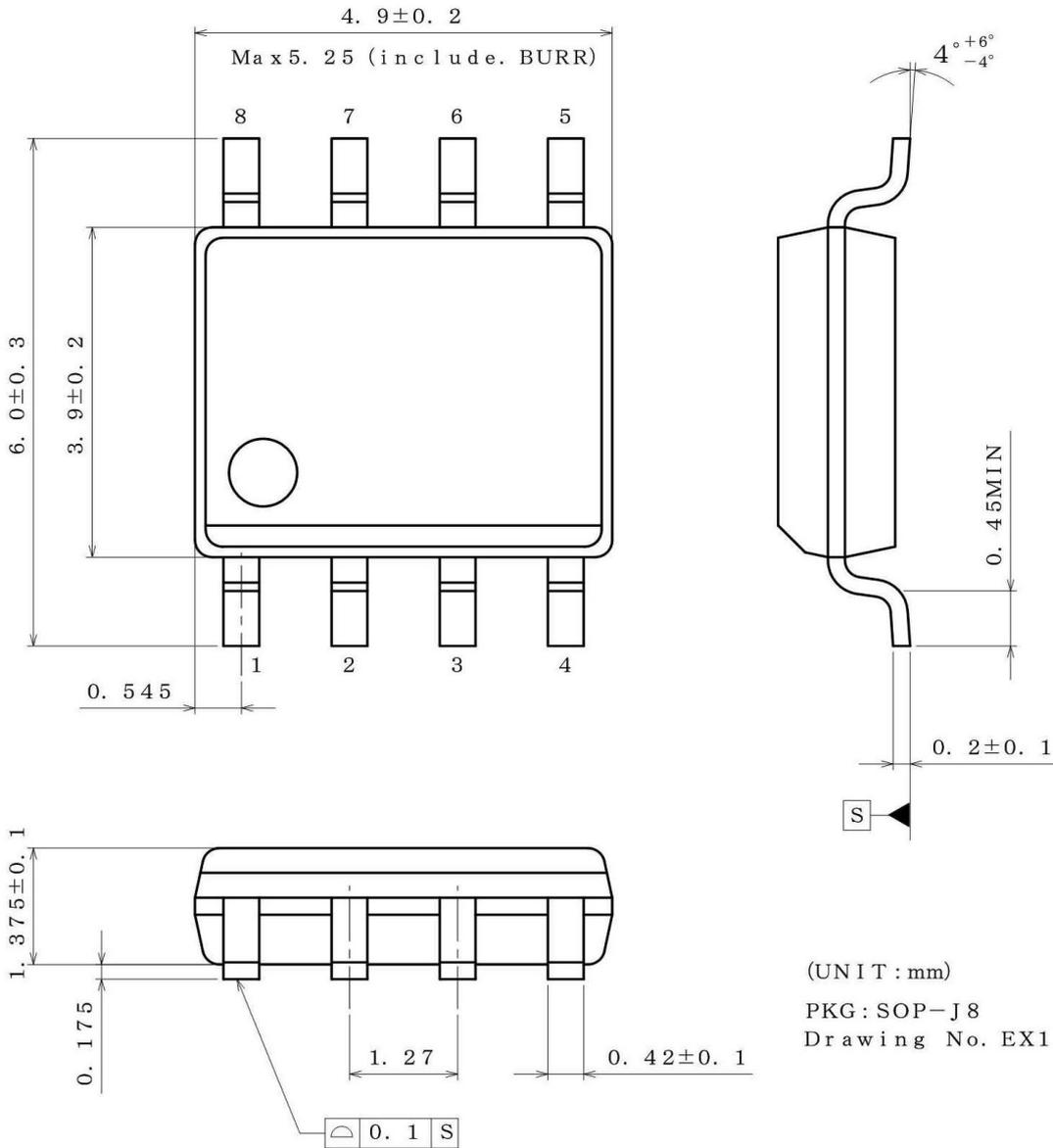
Temperature Range	Operating Supply Voltage Range	Number of Channels	Package		Orderable Part Number
			Package	Reel of	
-40 °C to +125 °C	3.0 V to 36.0 V	Dual	SOP-J8	2500	LM3472FJ-E2
			TSSOP-B8	3000	LM3472FVT-E2
			MSOP8	3000	LM3472FVM-TR
		Quad	SOP14	2500	LM3474F-E2
			SSOP-B14	2500	LM3474FV-E2

Marking Diagram



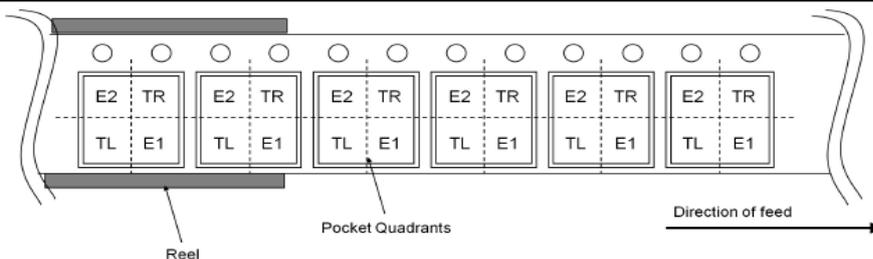
Physical Dimension and Packing Information

Package Name	SOP-J8
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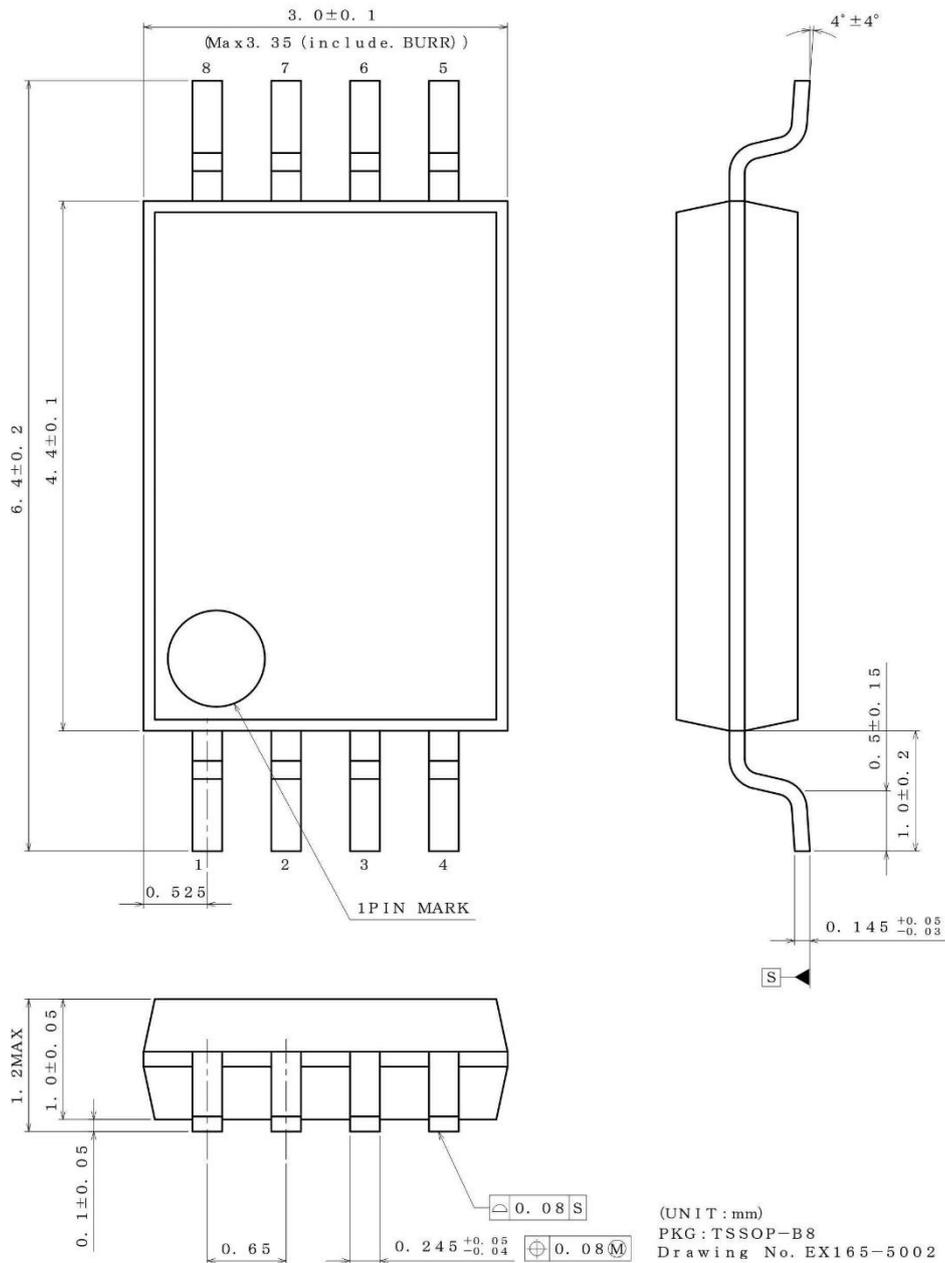
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



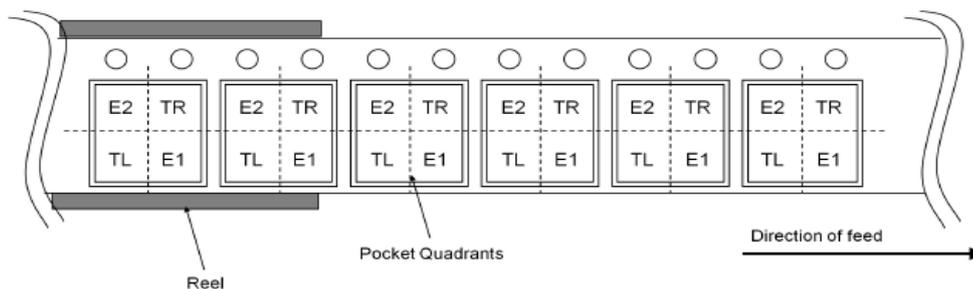
Physical Dimension and Packing Information – continued

Package Name	TSSOP-B8
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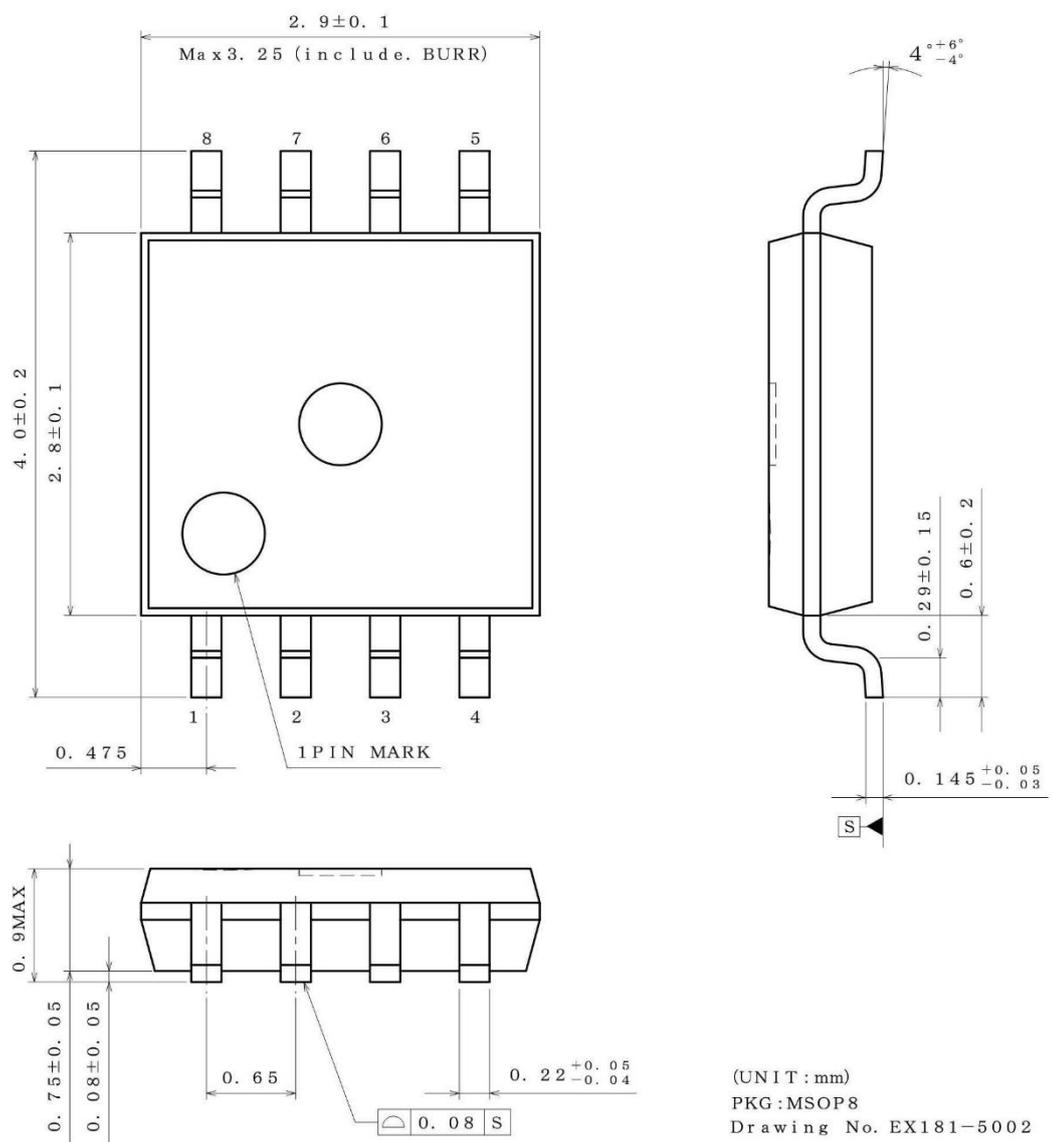
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



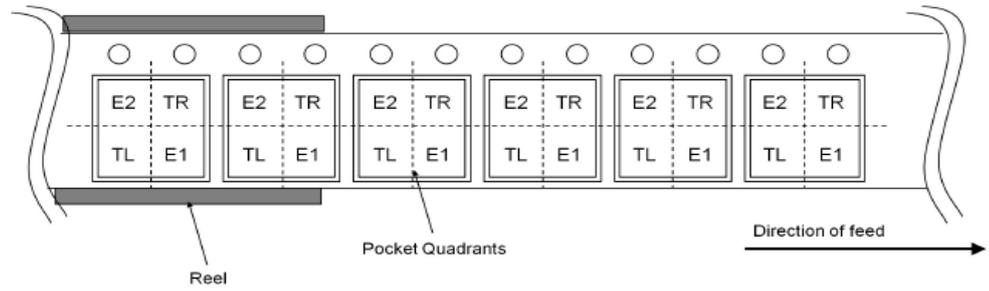
Physical Dimension and Packing Information – continued

Package Name	MSOP8
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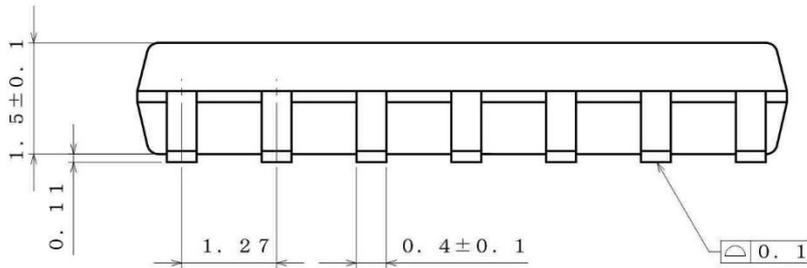
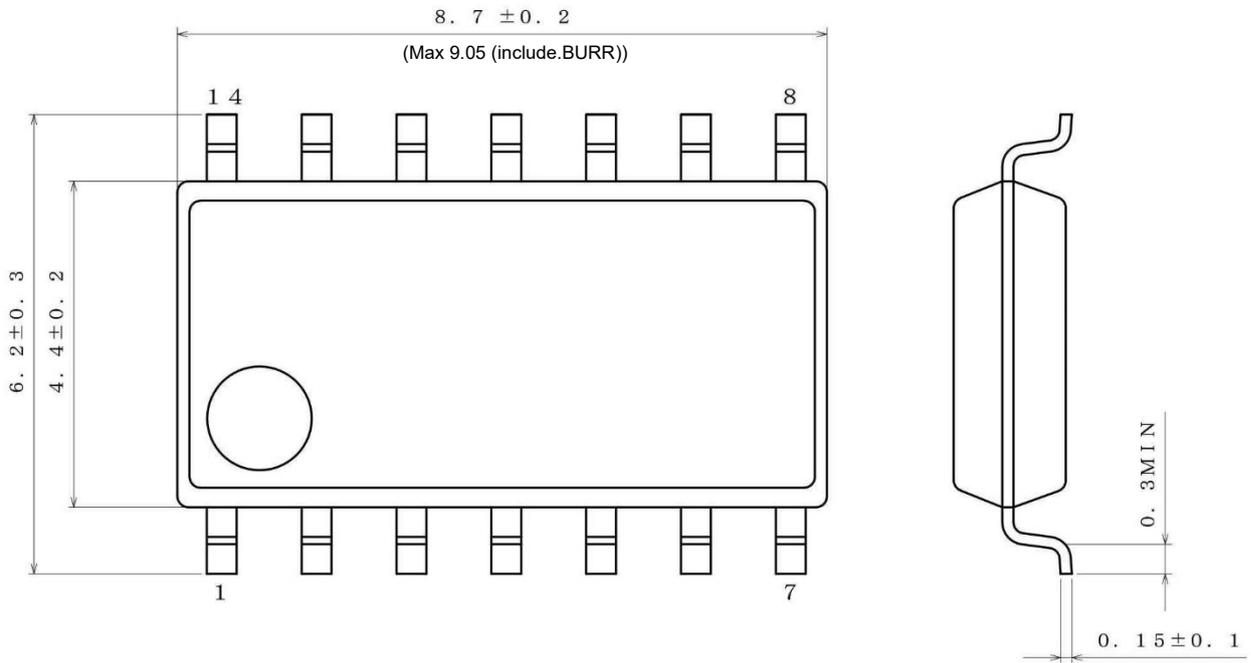
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1 pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Physical Dimension and Packing Information – continued

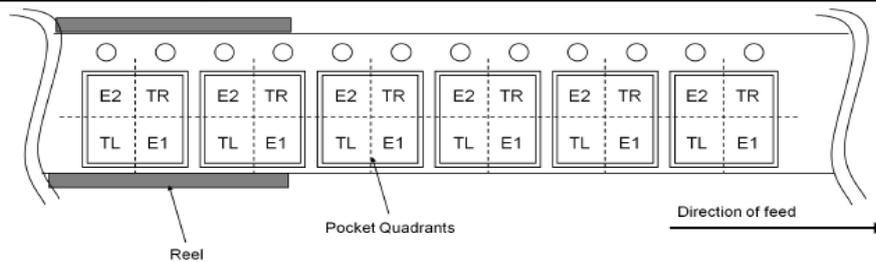
Package Name	SOP14
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(UNIT: mm)
 PKG: SOP14
 Drawing No.: EX113-5001

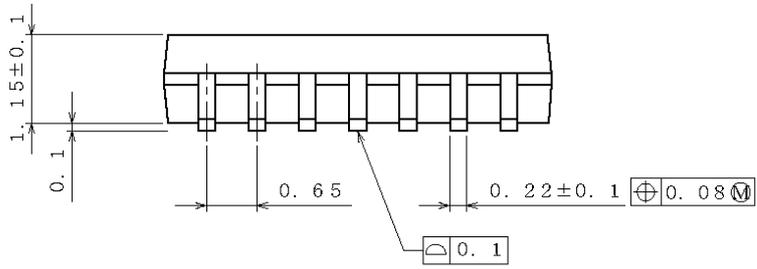
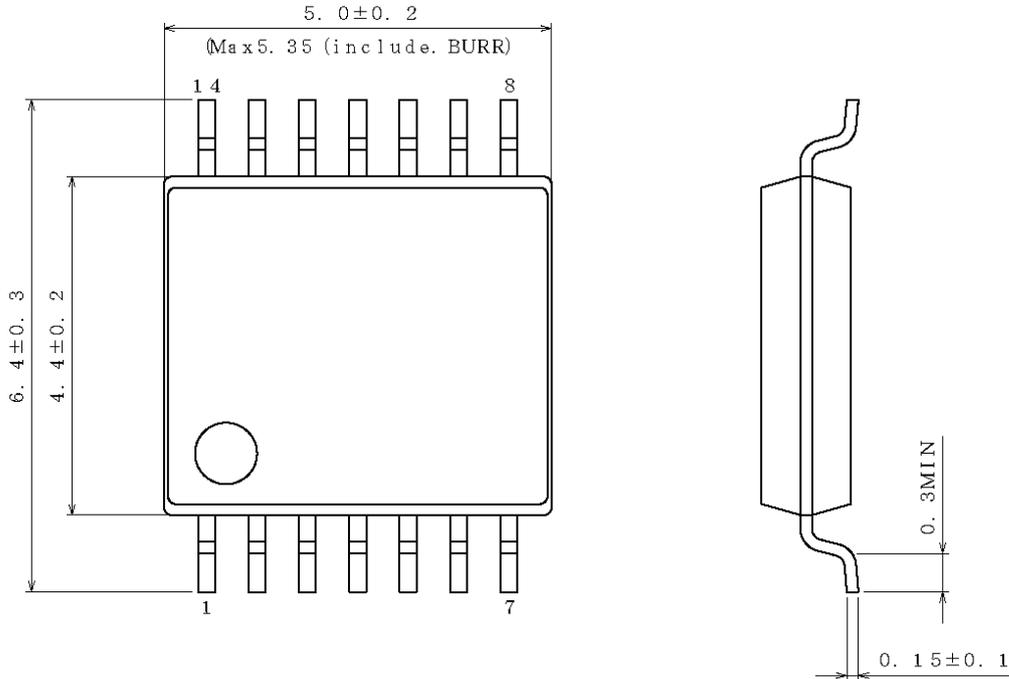
< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Physical Dimension and Packing Information – continued

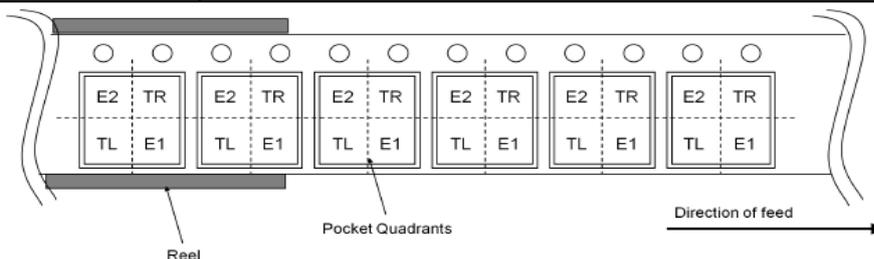
Package Name	SSOP-B14
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(UNIT : mm)
 PKG : SSOP-B14
 Drawing No. EX152-5002

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Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
29.Oct.2025	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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