A/D Converter Series for Automotive

Successive Approximation A/D Converter 12 bit, 0.5 MSPS to 1 MSPS, 8-channel, SPI Interface

BD79104MUF-M

General Description

The BD79104MUF-M is a general purpose, 12 bit 8-channel successive approximation A/D converter. The sampling rate of BD79104MUF-M ranges from 0.5 MSPS to 1 MSPS.

Features

- AEC-Q100 Qualified*(Note 1)*
- Maximum 1 MSPS Sampling Rate
- Low Power Consumption
- Small VQFN16FV3030 Package
- Serial Interface Compatible with SPI/QSPI/MICROWIRE
- Single-ended Input
- Output Code in Straight Binary Format

(Note 1) Grade 1

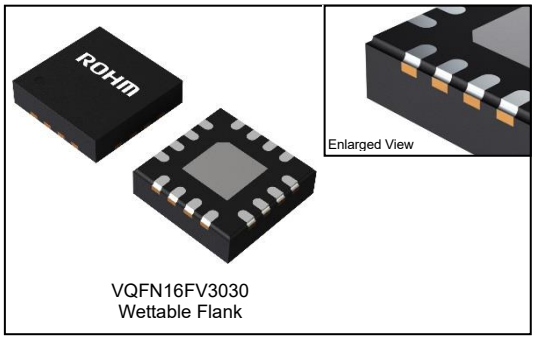
Applications

- Car Navigation Systems
- Automotive Cluster Display
- Battery Management Systems (BMS)
- Data Acquisition Systems

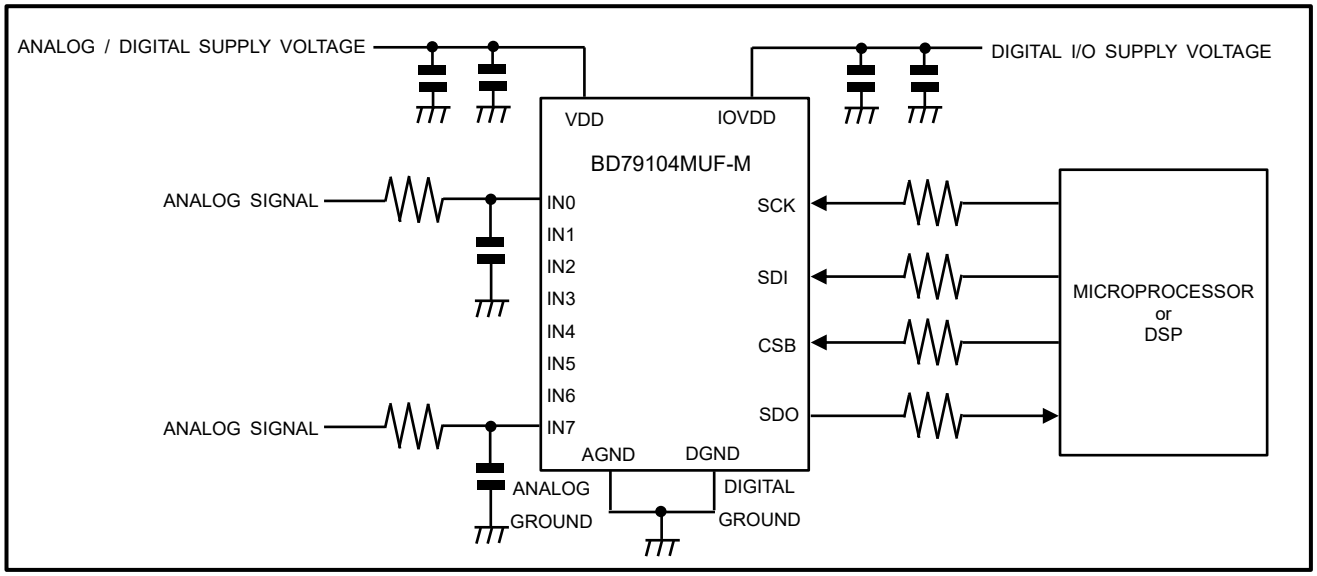
Key Specifications

- Supply Voltage Range (VDD): 2.70 V to 5.25 V
- Supply Voltage Range (IOVDD): 1.65 V to 5.25 V
- Sampling Rate: 0.5 MSPS to 1.0 MSPS
- Power Consumption:
  (In 1 MSPS Operation) 4 mW @ V_{DD} = 3.6 V (Typ)
  9.5 mW @ V_{DD} = 5.25 V (Typ)
- INL: ±1.0 LSB @ V_{DD} = 3 V (Typ)
- DNL: +1.2 / -0.99 LSB @ V_{DD} = 3 V (Typ)
- SNR: 72 dB @ V_{DD} = 3 V (Typ)
- SINAD: 72 dB @ V_{DD} = 3 V (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN16FV3030	3.0 mm x 3.0 mm x 1.0 mm



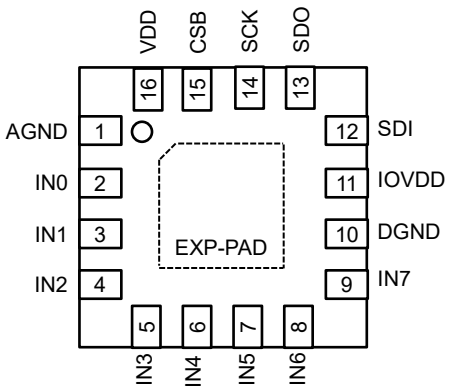
Typical Application Circuit



Contents

Pin Configuration

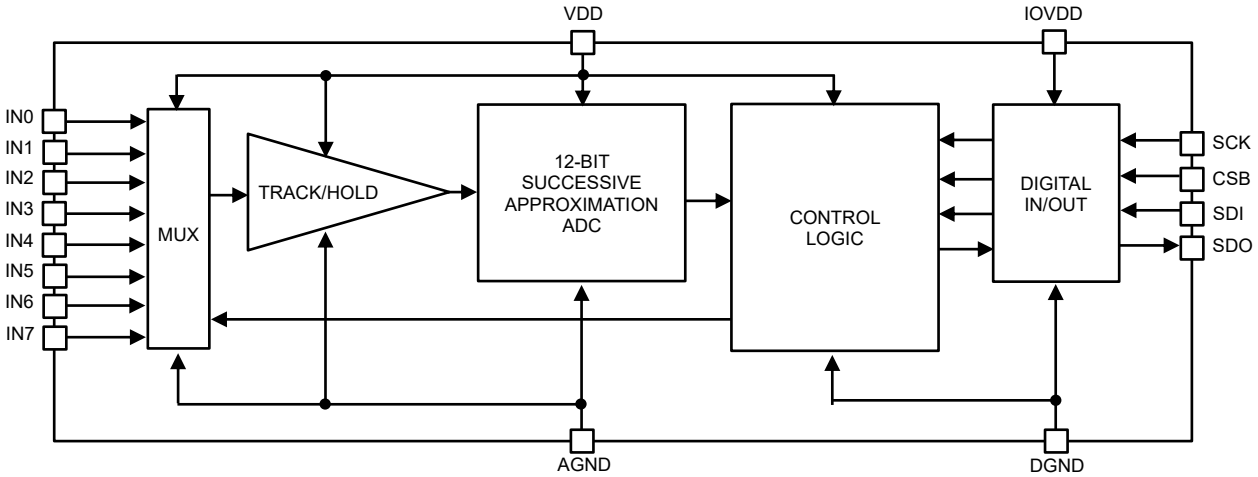
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	AGND	Analog ground pin. This voltage level is the zero scale of the analog input.
2	IN0	Analog input pin 0. The voltage range must be between 0 V and V_{DD}.
3	IN1	Analog input pin 1. The voltage range must be between 0 V and V_{DD}.
4	IN2	Analog input pin 2. The voltage range must be between 0 V and V_{DD}.
5	IN3	Analog input pin 3. The voltage range must be between 0 V and V_{DD}.
6	IN4	Analog input pin 4. The voltage range must be between 0 V and V_{DD}.
7	IN5	Analog input pin 5. The voltage range must be between 0 V and V_{DD}.
8	IN6	Analog input pin 6. The voltage range must be between 0 V and V_{DD}.
9	IN7	Analog input pin 7. The voltage range must be between 0 V and V_{DD}.
10	DGND	Digital ground pin.
11	IOVDD	Digital I/O power supply pin.
12	SDI	Digital data input pin.
13	SDO	Digital data output pin.
14	SCK	Digital clock input pin.
15	CSB	Chip select pin. A/D conversion starts at the falling edge of this signal.
16	VDD	Analog/Digital power supply pin. This voltage is the full scale of the analog input.
-	EXP-PAD	Connect the EXP-PAD to AGND.

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Analog/Digital Supply Voltage	V_{DD}	5.7	V
Digital I/O Supply Voltage	V_{IOVDD}	V_{DD}+0.3, max 5.7	V
Analog Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	-0.3 to V_{IOVDD}+0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
VQFN16FV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	23	10	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog/Digital Supply Voltage	V_{DD}	2.70	-	5.25	V
Digital I/O Supply Voltage	V_{IOVDD}	1.65	-	V_{DD}	V
Analog Input Voltage	V_{IN}	0	-	V_{DD}	V
Digital Input Voltage	V_{DIN}	0	-	V_{IOVDD}	V
Operating Temperature	Topr	-40	+25	+125	°C
Clock Frequency	f_{SCK}	10	-	20	MHz
Sampling Rate	f_S	0.5	-	1.0	MSPS

Electrical Characteristics

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V, f_{SCK} = 20 MHz, f_S = 1 MSPS

Parameter	Symbol	Min	Typ	Max	Unit	Parameter
Statistic Converter Characteristics						
Resolution with No Missing Codes	R_{ES}	-	12	-	bit	
Integral Non-linearity1	I_{NL1}	-1.2	-	+1.2	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Integral Non-linearity2	I_{NL2}	-1.0	-	+1.0	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Differential Non-linearity1	D_{NL1}	-0.99	-	+1.2	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Differential Non-linearity2	D_{NL2}	-0.99	-	+1.2	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Offset Error	O_E	-2.3	±1.1	+2.3	LSB	Ta = 25 °C
Gain Error	G_E	-2.0	±0.8	+2.0	LSB	Ta = 25 °C
Dynamic Converter Characteristics (f_{IN} = 100 kHz, V_{IN} = -0.02 dBFS)						
Signal to Noise and Distortion Ratio1	S_{INAD1}	70	72	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Signal to Noise and Distortion Ratio2	S_{INAD2}	70	72	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Signal to Noise Ratio1	S_{NR1}	70.8	72.0	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Signal to Noise Ratio2	S_{NR2}	70.8	72.0	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Total Harmonic Distortion	T_{HD}	-	-80	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Spurious-free Dynamic Range	S_{FDR}	-	82	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V, f_{IN} = 100 kHz
Effective Number of Bits1	E_{NOB1}	11.3	11.6	-	bit	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Effective Number of Bits2	E_{NOB2}	11.3	11.6	-	bit	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Inter-channel Isolation1	I_{SO1}	-	-85	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Inter-channel Isolation2	I_{SO2}	-	-84	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Inter-modulation Distortion1 (Second Order Term)	I_{MD1}	-	-78	-	dB	V_{DD} = 5.25 V, V_{IOVDD} = 3.0 V 103.5 kHz, 113.5 kHz
Inter-modulation Distortion2 (Third Order Term)	I_{MD2}	-	-76	-	dB	V_{DD} = 5.25 V, V_{IOVDD} = 3.0 V 103.5 kHz, 113.5 kHz
Full Power Band Width	f_{PBW}	-	10	-	MHz	V_{DD} = V_{IOVDD} = 5 V
Aperture Delay	t_{AD}	-	4.3	-	ns	V_{DD} = V_{IOVDD} = 5 V
Aperture Jitter	t_{AJ}	-	30	-	ps	V_{DD} = V_{IOVDD} = 5 V
Clock Frequency	f_{SCK}	10	-	20	MHz	
Sampling Rate	f_S	500 k	-	1 M	SPS	
Track/Hold Acquisition Time	t_{ACQ}	-	-	3	SCK cycles	

Electrical Characteristics - continued

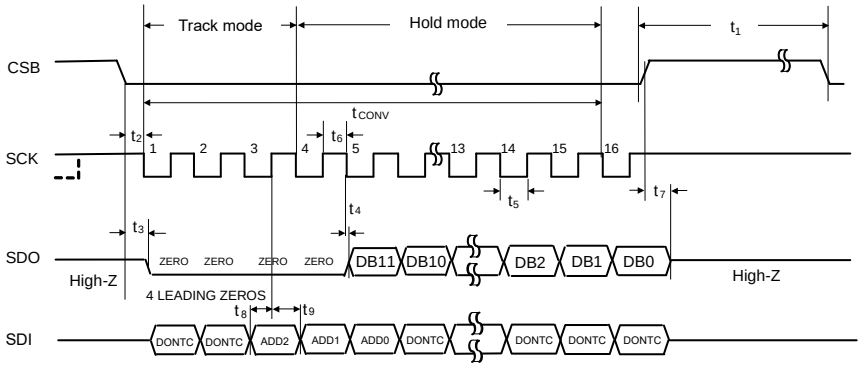
Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V, f_{SCK} = 20 MHz, f_S = 1 MSPS

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Analog Input Characteristics						
Input Range	V_{IN}	0	-	V_{DD}	V	
Input DC Leakage Current	I_{LEAK}	-1.0	±0.1	+1.0	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance1	C_{INA1}	-	28	-	pF	track mode, V_{DD} = 5 V
Input Capacitance2	C_{INA2}	-	4	-	pF	hold mode, V_{DD} = 5 V
Digital Input Characteristics						
High Input Voltage	V_{IH}	0.7 x V_{IOVDD}	-	-	V	
Low Input Voltage	V_{IL}	-	-	0.3 x V_{IOVDD}	V	
Input Current	I_{IND}	-1.0	±0.1	+1.0	µA	V_{IND} = 0 V or V_{IOVDD}
Input Capacitance	C_{IND}	-	2.5	-	pF	
Digital Output Characteristics						
Output High Voltage1	V_{OH1}	V_{IOVDD} - 0.20	V_{IOVDD} - 0.03	-	V	I_{SOURCE} = 200 µA
Output High Voltage2	V_{OH2}	-	V_{IOVDD} - 0.1	-	V	I_{SOURCE} = 1 mA
Output Low Voltage1	V_{OL1}	-	0.02	0.40	V	I_{SINK} = 200 µA
Output Low Voltage2	V_{OL2}	-	0.1	-	V	I_{SINK} = 1 mA
High-Z Leakage Current	I_{OZ}	-10.0	±0.1	+10.0	µA	V_{OZ} = 0 V or V_{DD}
High-Z Output Capacitance	C_{OUT}	-	2	-	pF	
Current Consumption						
Operational Current Consumption1	I_{A1}	-	1.8	2.7	mA	V_{DD} = V_{IOVDD} = 5.25 V, f_S = 1 MSPS
Operational Current Consumption2	I_{A2}	-	1.1	1.5	mA	V_{DD} = V_{IOVDD} = 3.6 V, f_S = 1 MSPS
Stand-by Current Consumption1	I_{S1}	-	0.5	-	µA	V_{DD} = V_{IOVDD} = 5.25 V, SCK off
Stand-by Current Consumption2	I_{S2}	-	0.3	-	µA	V_{DD} = V_{IOVDD} = 3.6 V, SCK off

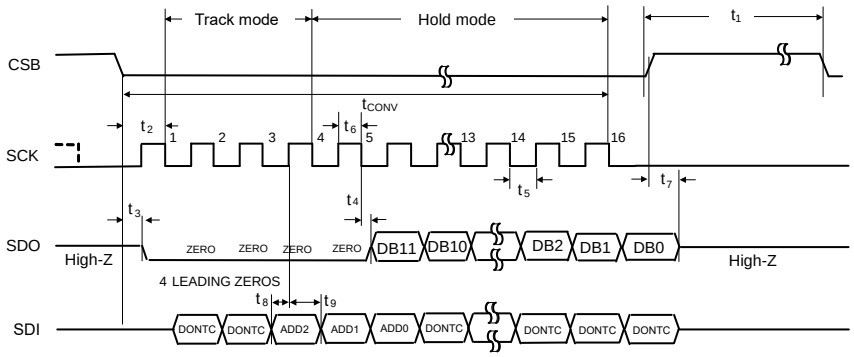
Timing Specifications

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V, f_{SCK} = 20 MHz, C_L = 25 pF

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Conversion Time	t_{CONV}	-	16	-	SCK	
CSB Pulse Width	t_1	10	-	-	ns	
CSB Setup Time	t_2	10	-	-	ns	
SDO Enable Time	t_3	-	-	20	ns	
SDO Access Time1	t_4	-	-	40	ns	V_{IOVDD} = 1.65 V to 3.6 V
SDO Access Time2	t_4	-	-	20	ns	V_{IOVDD} = 4.75 V to 5.25 V
SCK Low Pulse Width	t_5	0.4 x t_{SCK}	-	-	ns	$t_{SCK} = 1/f_{SCK}$
SCK High Pulse Width	t_6	0.4 x t_{SCK}	-	-	ns	$t_{SCK} = 1/f_{SCK}$
SDO Disable Time1	t_7	-	-	25	ns	V_{IOVDD} = 1.65 V to 3.6 V
SDO Disable Time2	t_7	-	-	25	ns	V_{IOVDD} = 4.75 V to 5.25 V
SDI Setup Time	t_8	10	-	-	ns	
SDI Hold Time	t_9	10	-	-	ns	
Power-up Time	t_{POWUP}	-	15	-	µs	



(a) If SCK is high at the falling edge of CSB



(b) If SCK is low at the falling edge of CSB

Figure 1. Serial Interface Timing Chart

Term Definitions

ACQUISITION TIME:
It is the time when the voltage of the sampling capacitor equals input voltage from the charge start.

APERTURE DELAY:
It is defined as the time when the input voltage is held since a sampling capacitor was separated with outside by a 4th falling edge of SCK.

APERTURE JITTER:
The variation in the aperture delays in sampling operations. Aperture jitter gets to affect output noise.

INTEGRAL NON-LINEARLITY (INL):
It is a measure of the deviation of each individual code from a line drawn from zero scale (0.5 LSB below the first code transition) through full scale (0.5 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

DIFFERENTIAL NON-LINEARLITY (DNL):
It is the measure of the maximum deviation from the ideal step size of 1 LSB.

OFFSET ERROR (OE):
It is the deviation of the first code transition “(000…000) to (000…001)” from the ideal of 0.5 LSB.

FULL SCALE ERROR (FSE):
It is the deviation of the last code transition “(111…110) to (111…111)” from the ideal of “V_{DD}-1.5 LSB”.

GAIN ERROR (GE):
It is defined as full scale error minus offset error.

TOTAL HARMONIC DISTORTION (THD):
It is the ratio, expressed in dB or dBc, of the RMS total of the first 5 harmonic components at the output to the RMS level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^{\,2} + \cdots + A_{f6}^{\,2}}{A_{f1}^{\,2}}}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

SIGNAL TO NOISE AND DISTORTION RATIO (SINAD):
It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, including harmonics but excluding DC component.

EFFECTIVE NUMBER OF BITS (ENOB):
It is another method of specifying Signal to Noise and Distortion Ratio. ENOB is defined as “(SINAD-1.76) / 6.02” and says that the converter is equivalent to a perfect A/D converter of this number of bits.

SIGNAL TO NOISE RATIO (SNR):
It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, not including harmonics and DC component.

SPURIOUS FREE DYNAMIC RANGE (SFDR):
It is the difference, expressed in dB, between the RMS value of the input signal to the RMS value of the peak spurious spectral component, where a peak spurious spectral component is any spurious signal present in the output spectrum that is not present at the input.

CONVERSION TIME:
It is the required time for the A/D converter to convert the input signal to the digital code.

Typical Performance Curves

(Reference Data)

Unless otherwise noted, Ta = 25 °C.

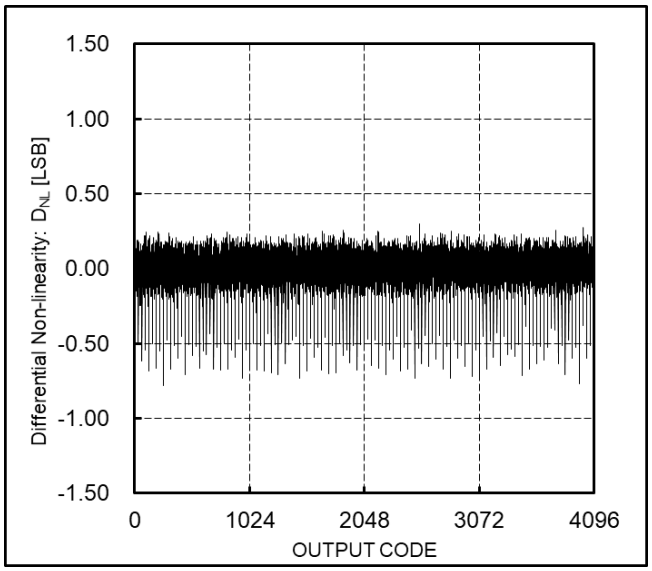


Figure 2. Differential Non-linearity vs OUTPUT CODE
(V_{IOVDD} = V_{DD} = 3 V, f_{SCK} = 10 MHz, f_S = 500 kSPS)

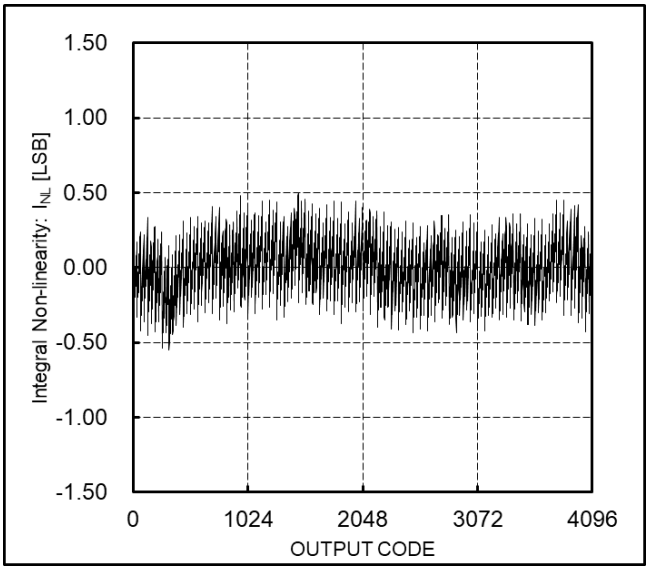


Figure 3. Integral Non-linearity vs OUTPUT CODE
(V_{IOVDD} = V_{DD} = 3 V, f_{SCK} = 10 MHz, f_S = 500 kSPS)

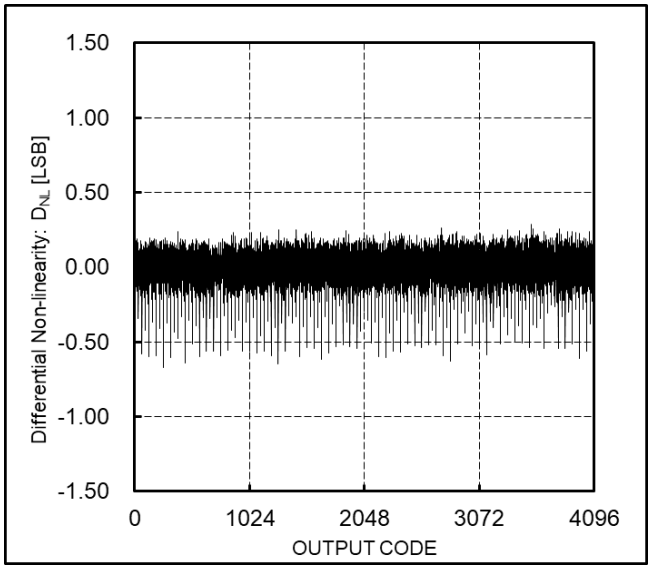


Figure 4. Differential Non-linearity vs OUTPUT CODE
(V_{IOVDD} = V_{DD} = 3 V, f_{SCK} = 20 MHz, f_S = 1 MSPS)

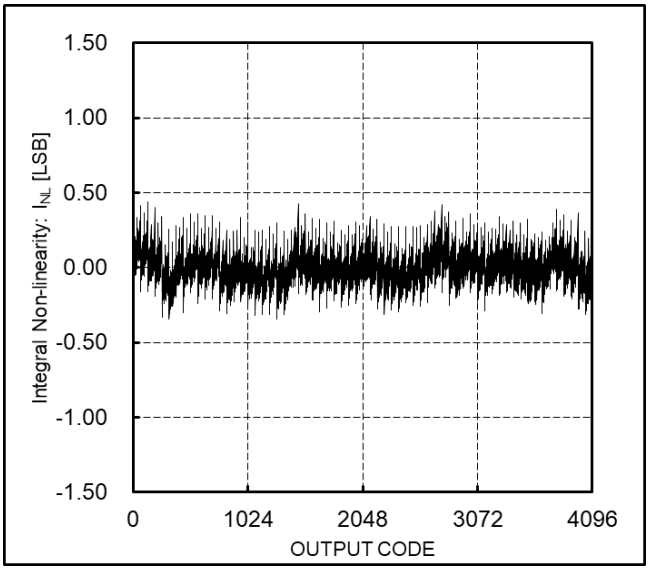


Figure 5. Integral Non-linearity vs OUTPUT CODE
(V_{IOVDD} = V_{DD} = 3 V, f_{SCK} = 20 MHz, f_S = 1 MSPS)

Typical Performance Curves – continued

(Reference Data)

Unless otherwise noted, Ta = 25 °C, f_{IN} = 100 kHz.

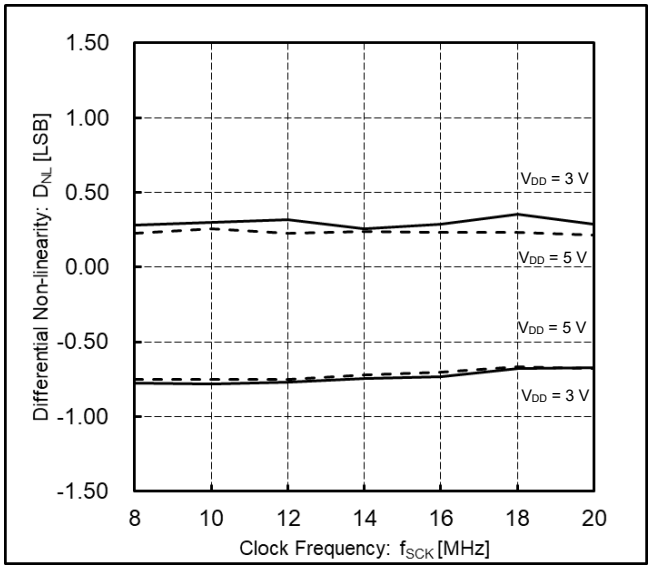


Figure 6. Differential Non-linearity vs Clock Frequency

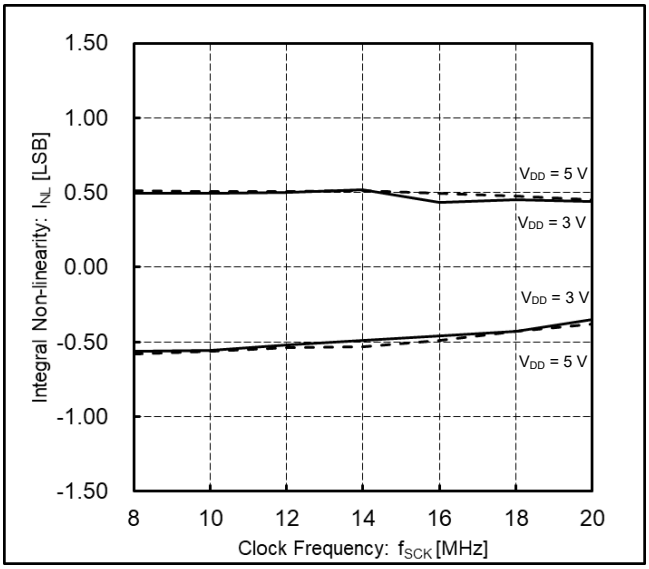


Figure 7. Integral Non-linearity vs Clock Frequency

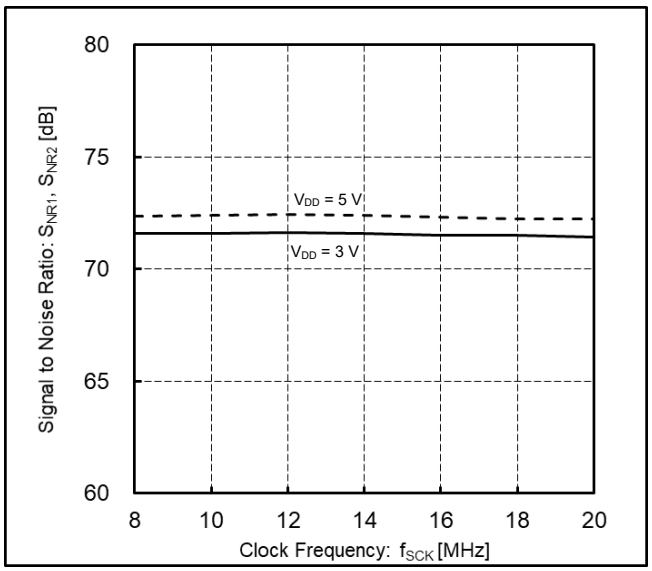


Figure 8. Signal to Noise Ratio vs Clock Frequency

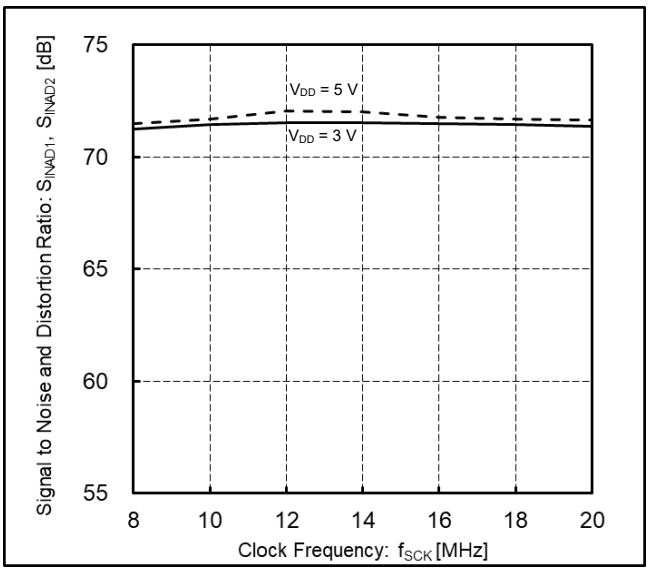


Figure 9. Signal to Noise and Distortion Ratio vs Clock Frequency

Typical Performance Curves – continued

(Reference Data)

Unless otherwise noted, Ta = 25 °C, f_{IN} = 100 kHz.

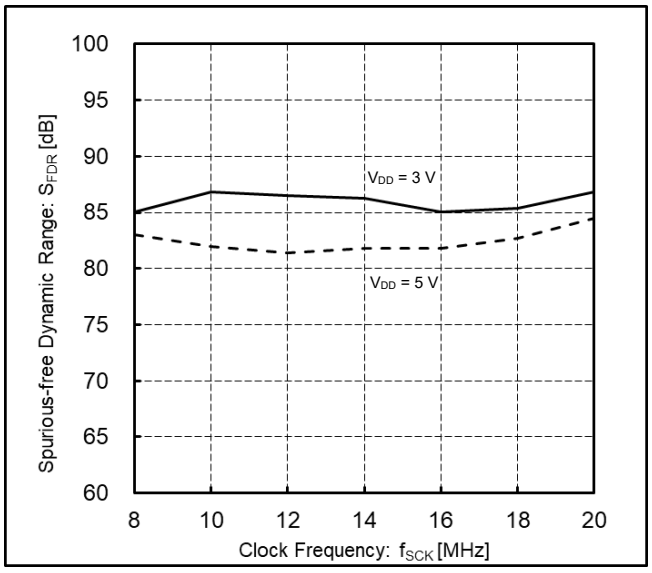


Figure 10. Spurious-free Dynamic Range vs Clock Frequency

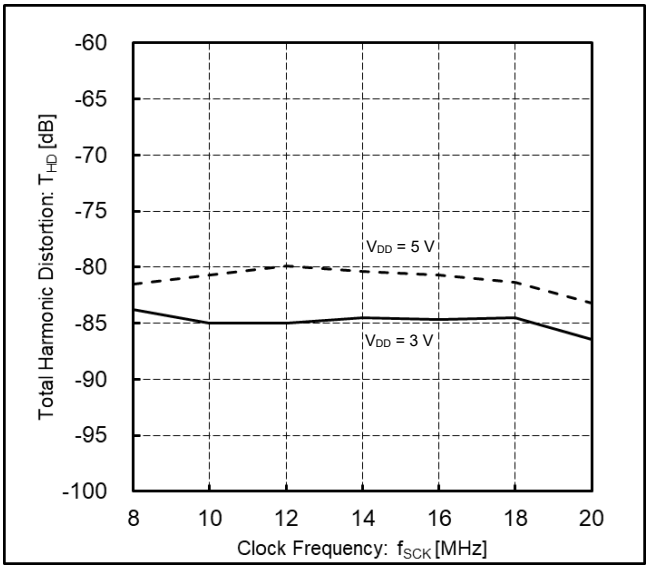


Figure 11. Total Harmonic Distortion vs Clock Frequency

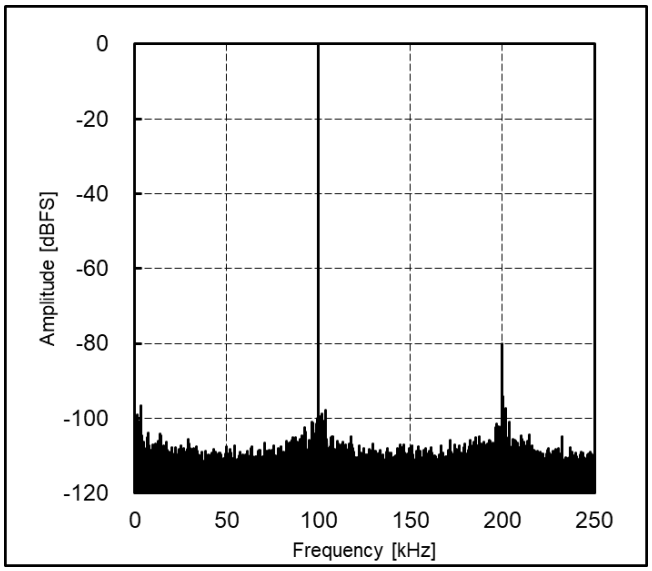


Figure 12. Amplitude vs Frequency
(V_{IOVDD} = 3 V, V_{DD} = 5 V, f_{SCK} = 10 MHz, f_S = 500 kSPS)

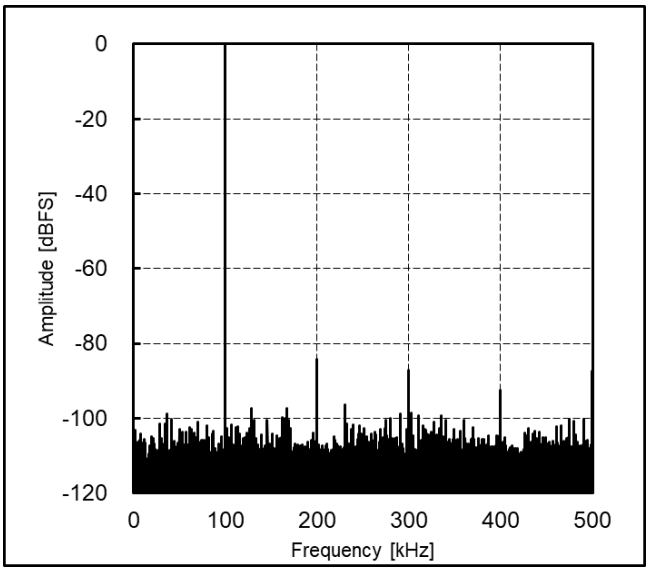


Figure 13. Amplitude vs Frequency
(V_{IOVDD} = 3 V, V_{DD} = 5 V, f_{SCK} = 20 MHz, f_S = 1 MSPS)

Description of Functions

1. Overview of A/D Conversion Process

This product is a successive-approximation A/D converter designed with a charge-redistribution D/A converter. Simplified schematics of the A/D converter are shown in Figure 14 and Figure 15.

Figure 14 shows the A/D converter in Track mode: the switch SW1 is in the position A, SW2 is closed and balances the comparator. Then, the sampling capacitor is charged with the analog input voltage V_{IN}.

Figure 15 shows the A/D converter in Hold mode. When a conversion starts, the A/D converter goes into Hold mode: SW2 becomes open, SW1 connects the sampling capacitor to ground through the position B and the comparator loses its balance. The control logic controls the input voltage of the comparator via the sampling capacitors of the charge-redistribution D/A converter to get the comparator back into a balanced state. A/D conversion finishes when the comparator balances again. The control logic also generates the output code of the A/D converter.

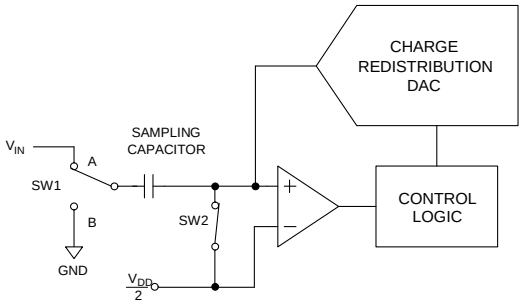


Figure 14. Track Mode

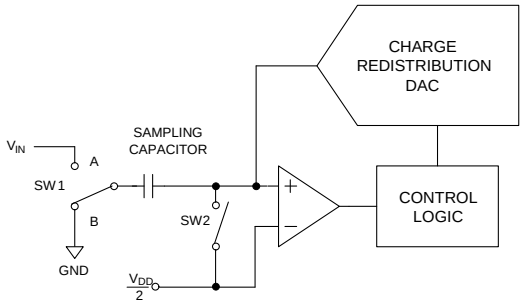


Figure 15. Hold Mode

2. Ideal Transfer Characteristics

Figure 16 shows the ideal transfer characteristics of this product. Code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for this product is V_{DD} / 4096. The output code format of the A/D converter is straight binary.

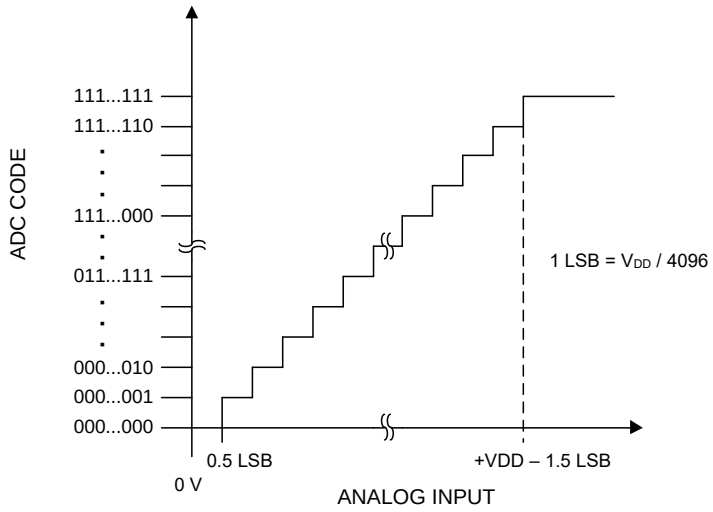
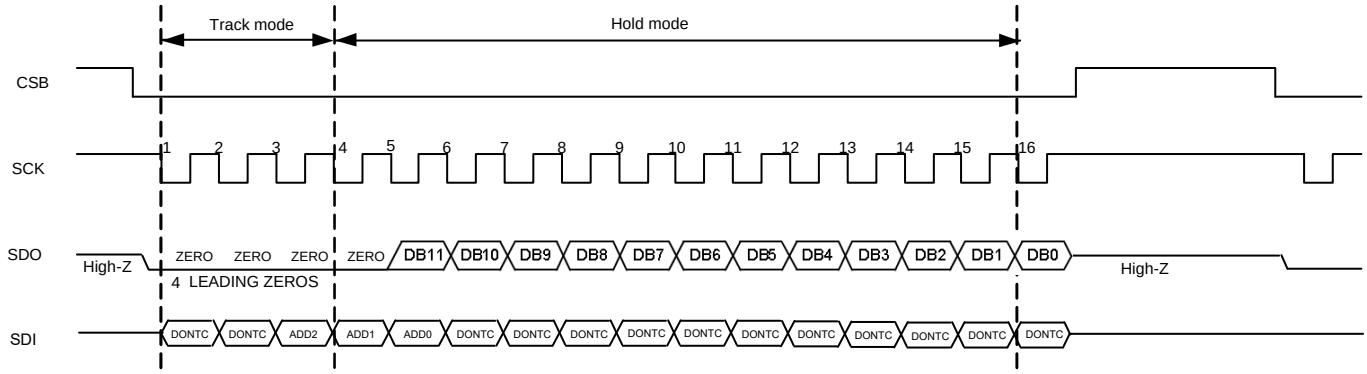


Figure 16. Ideal Transfer Characteristics

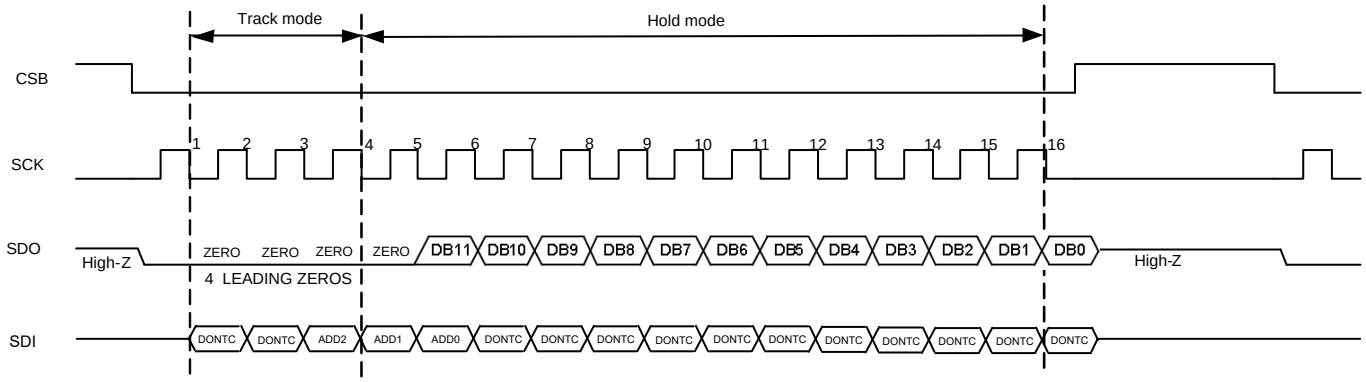
Description of Functions – continued

3. Serial Interface

The serial interface timing is shown in Figure 17. When CSB goes low, both a conversion process and data transfer are started. At the falling edge of CSB, SDO changes its state from High-Z to Low. Then, the converter moves to Track mode at the first falling edge of SCK. At the 4th falling edge of SCK, the converter moves from Track mode to Hold mode. A tracked input signal is sampled and held for conversion at this point. SDO goes back to High-Z at the rising edge of CSB.
16 SCK cycles are needed to read a complete data of the A/D conversion from this product. First, four leading zeros come out from SDO. Then, the 12 bit data comes out bit by bit, starting from the MSB. The first zero is clocked out to SDO at the falling edge of CSB. The remaining leading 3 zeros and data bits are clocked out to SDO at the falling edge of SCK; the host IC, the receiver of the A/D conversion data, is needed to receive the data at the rising or falling edge of SCK after the SDO access time has elapsed.
To perform A/D conversion properly, this product needs at least 16 SCK cycles while CSB is low. If the A/D conversion is interrupted in the middle of the conversion with CSB going to high before 16 SCK cycles, the following A/D conversion may not be performed normally. Therefore, it is necessary that equal to or more than 16 falling edges of SCK exist while CSB is low.
In addition, SCK should be held either high or low at the falling edge of CSB. If SCK is low at the falling edge of CSB, as shown in Figure 17(b), a time move to Track mode length is about a half clock period longer than one if SCK is high as shown in Figure 17(a).



(a) If SCK is high at the falling edge of CSB



(b) If SCK is low at the falling edge of CSB

Figure 17. Serial Interface Timing

Description of Functions – continued

4. Control of CSB
   As shown in Figure 18, the A/D conversion can be performed even if CSB remains low after second communication.
   CSB should be high after all communication is completed while the A/D conversion is stopped.

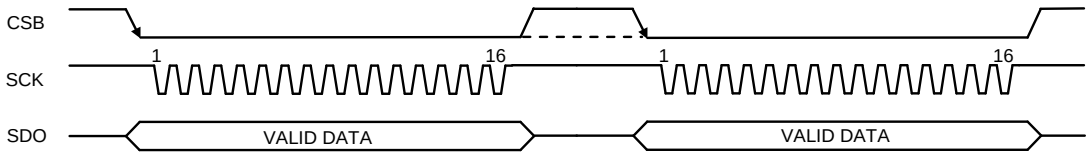


Figure 18. A/D Conversion after Power-up

5. Input Channel Selection
   As shown in Figure 17, the Input channel to be converted in the next communication is selected by setting the SDI input data ADD0, ADD1, and ADD2 as shown Table 1 when the 3rd SCK clock is inputted after the CSB becomes low.
   The IN0 pin is selected after power-up.

Table 1. Input Channel Selection

ADD2	ADD1	ADD0	Input Channel
0	0	0	IN0 (Default)
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

Application Example

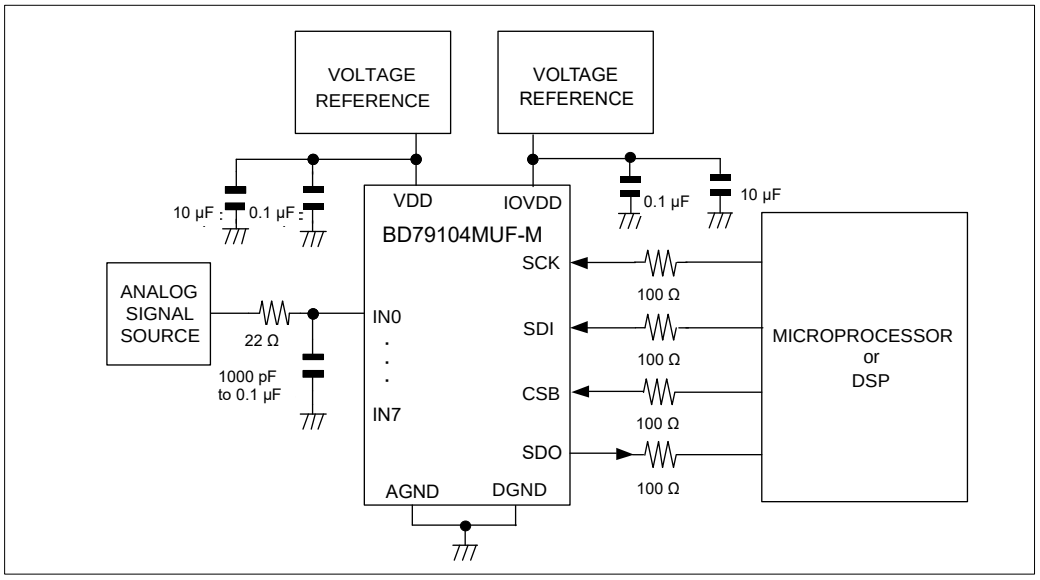


Figure 19. Application Circuit

As shown in Figure 19, a power supply pin connects voltage source and put two bypass capacitors for the high frequency and low frequency noise between VDD and AGND and between IOVDD and DGND to make the maximum use of the A/D converter's capability. Ceramic capacitors of 0.1 µF and 1 µF to 10 µF are to be used as bypass capacitor for this product. Especially, the capacitor of 0.1 µF should be placed as close to the IOVDD and VDD pins of this product as possible.
Because the voltages of VDD and AGND are used as the reference voltages for the A/D converter, the deviation of the supply voltage directly affects the full scale and has much influence on its characteristics. Therefore, the fully stable supply voltage should be connected to VDD.

The output impedance of the analog input signal source should be small enough. Charge in the sampling capacitor is swept out to the IN pin at the transition from Hold mode to Track mode because of the difference of the voltage between the input signal voltage and the sampling capacitor voltage. This charge could cause undesirable voltage deviation. If influence of the deviation remains at the transition from Track mode to Hold mode, it could cause the conversion error.
If a buffer amplifier is used to get low output impedance, high-speed response is required of the buffer amplifier. A decoupling capacitor and a resister on the IN analog input could support the amplifier to reduce the influence of the charge.

I/O Equivalence Circuit

(1) Analog Input Pin

The equivalent analog input circuit is shown in Figure 20. The diodes, D_1 and D_2, are placed for ESD protection. If the analog input voltage is more than "V_{DD}+0.3 V", or less than "V_{AGND}-0.3 V", these diodes are turned on and forward current is generated. This current might cause malfunction or irreversible damage to this product. The capacitance value of the C_1 in Figure 20 is typically 4 pF, derived from the package parasitic capacitance. The R_1 is the resistance of the track/hold switch, typically 500 Ω. The C_2 is the sampling capacitance of this product, and the capacitance value is typically 24 pF.

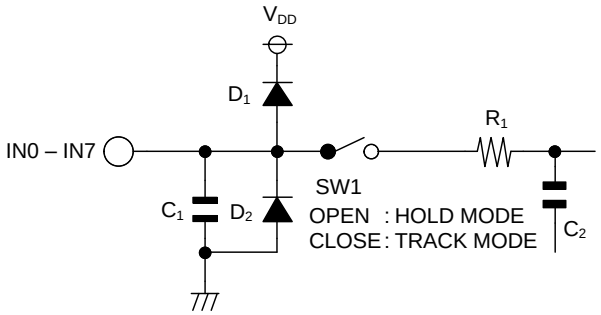


Figure 20. Analog Input Equivalent Circuit

(2) Digital Input and Output Pins

The equivalent digital input, SCK, SDI and CSB, circuit is shown in Figure 21. The diodes, D_1 and D_2, are placed for ESD protection. Digital input voltage range is the range from ground pin, DGND, to digital power pin, IOVDD.

The equivalent digital output, SDO, circuit is shown in Figure 22. Output voltage range is the range from ground pin, DGND, to digital power pin, IOVDD.

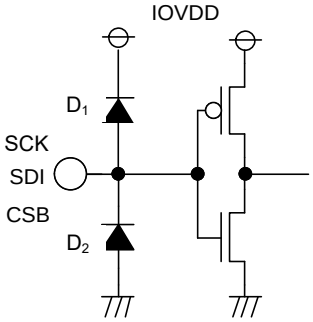


Figure 21. Equivalent Digital Input Circuit

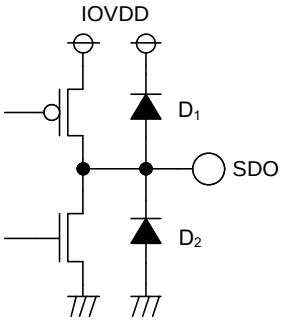


Figure 22. Equivalent Digital Output Circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

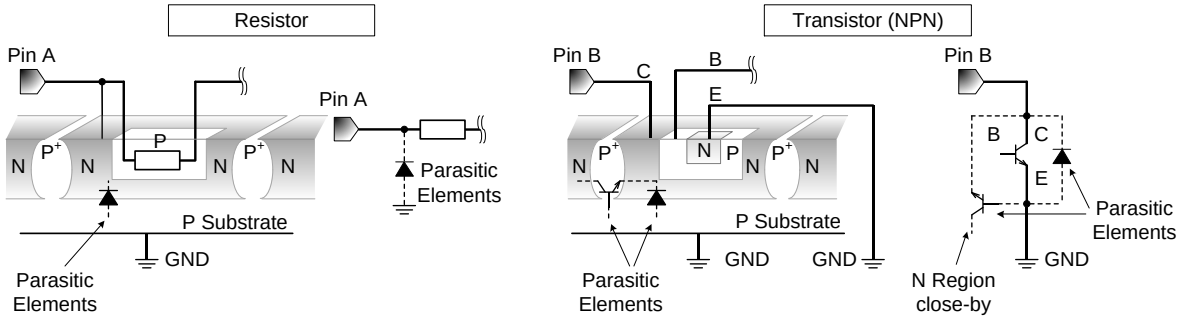


Figure 23. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

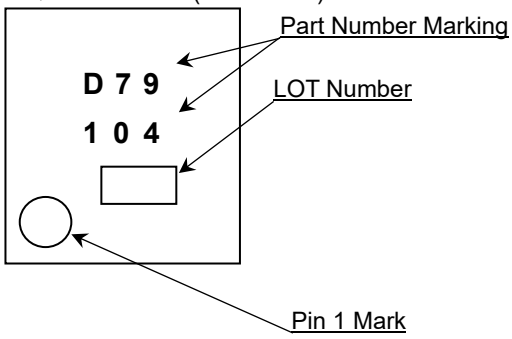
B	D	7	9	1	0	4	M	U	F	-	M E 2

Package
MUF: VQFN16FV3030

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

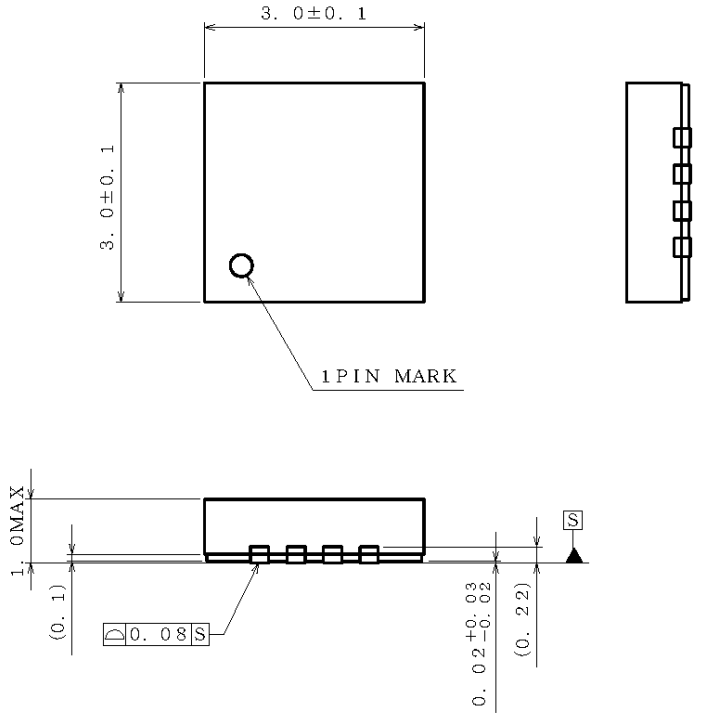
Marking Diagram

VQFN16FV3030 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN16FV3030

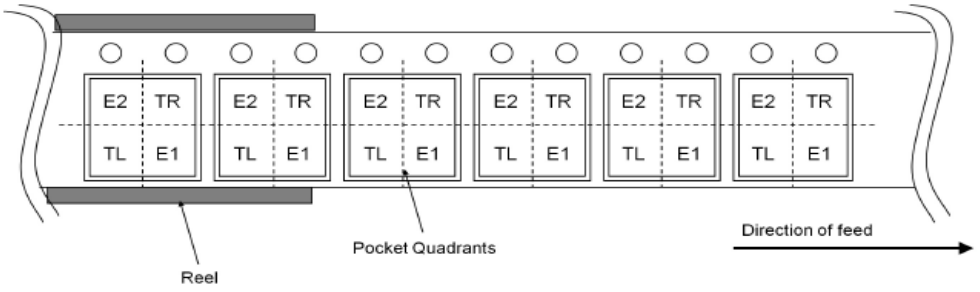


(UNIT : mm)
PKG : VQFN16FV3030
Drawing No. EX396−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
12.Jan.2023	001	New Release