

# Signal Monitor IC Series for Automotive

## Signal Monitor Hub IC

### 16-channel, SPI Interface

**BD79111MUF-C**

#### General Description

The BD79111MUF-C is a signal monitor hub IC featuring a built-in 12-bit successive-approximation register ADC with a maximum sampling rate of 0.5 MSPS. The 16-Channel can each be configured as analog input, digital input, or digital output.

#### Features

- AEC-Q100 Qualified<sup>(Note 1)</sup>
  - Maximum 0.5 MSPS Sampling Rate
  - Low Power Consumption
  - Compact VQFN24FV4040 Package
  - SPI/QSPI/MICROWIRE Compatible Serial Interface
  - 16-Channel Single-Ended Input
  - Straight Binary Output Format
  - Daisy-Chain Connection Support
  - CRC Function Include
  - GPIO Function Include
- (Note 1) Grade 1*

#### Applications

- Automotive Zone ECU
- Automotive Body Domain Controller
- Automotive Cluster Display
- Data Acquisition System

#### Key Specifications

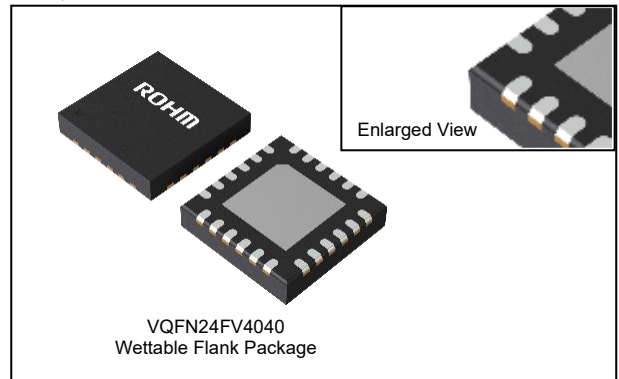
- Supply Voltage Range (VDD): 2.7 V to 5.5 V
- Supply Voltage Range (IOVDD): 1.65 V to 5.5 V
- Sampling Rate: MAX 0.5 MSPS
- Power Consumption  
(0.5 MSPS Operation): 5.0 mW @ V<sub>DD</sub> = 3.6 V (Typ)  
9.9 mW @ V<sub>DD</sub> = 5.5 V (Typ)
- INL: ±2.0 LSB @ V<sub>DD</sub> = 3 V (Typ)
- DNL: ±1.0 LSB @ V<sub>DD</sub> = 3 V (Typ)
- SNR: 72 dB @ V<sub>DD</sub> = 3 V (Typ)
- Operating Temperature Range: -40 °C to +125 °C

#### Package

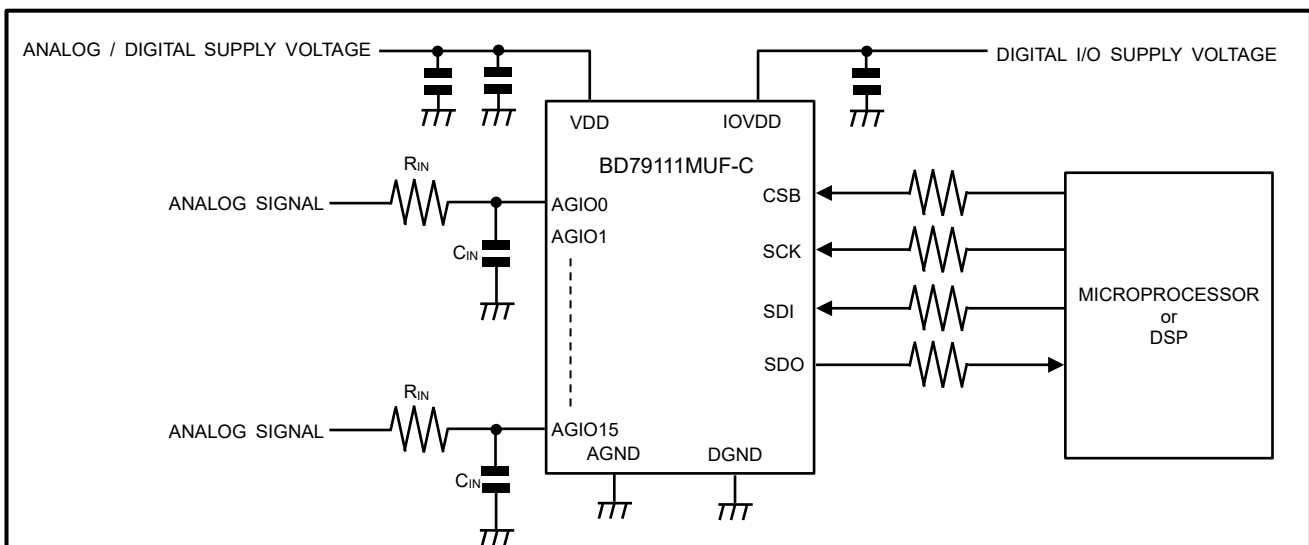
VQFN24FV4040

W (Typ) x D (Typ) x H (Max)

4.0 mm x 4.0 mm x 1.0 mm



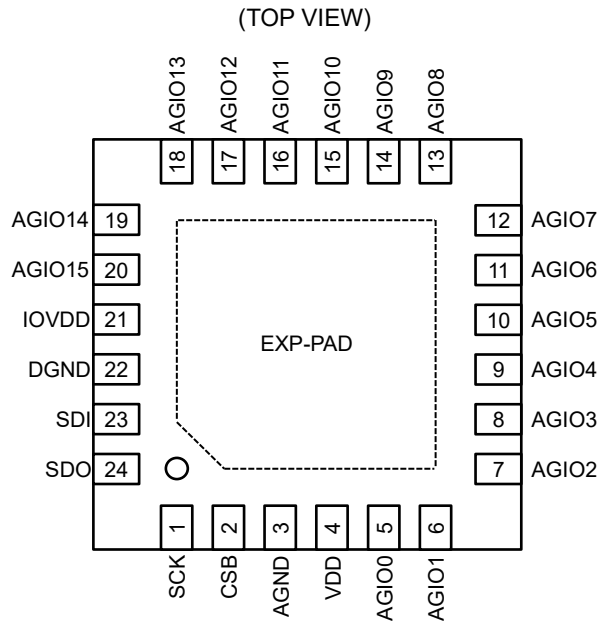
#### Typical Application Circuit



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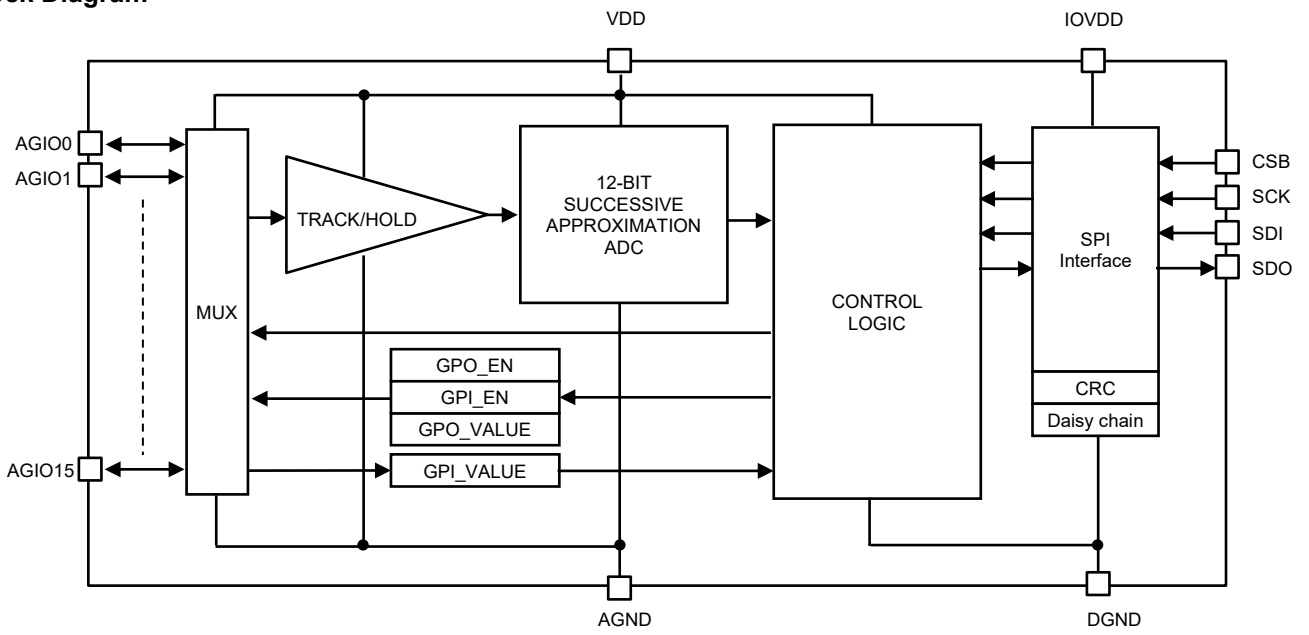
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	SCK	Digital clock input pin This clock synchronizes A/D conversion and the output of results, as well as the writing and reading of registers. When connected in a daisy chain, this clock is used to capture data input from SDI.
2	CSB	Chip select pin When this pin is low, data can be transmitted and received synchronized with SCK.
3	AGND	Analog/Digital ground pin AGND serves as the reference for the analog zero-scale voltage.
4	VDD	Analog/Digital power supply pin This voltage serves as the reference for the analog full-scale voltage. Connect a 0.1 μF ceramic capacitor and a 1 to 10 μF one to AGND near this pin.
5	AGIO0	Channel 0: Analog Input or GPIO pin
6	AGIO1	Channel 1: Analog Input or GPIO pin
7	AGIO2	Channel 2: Analog Input or GPIO pin
8	AGIO3	Channel 3: Analog Input or GPIO pin
9	AGIO4	Channel 4: Analog Input or GPIO pin
10	AGIO5	Channel 5: Analog Input or GPIO pin
11	AGIO6	Channel 6: Analog Input or GPIO pin
12	AGIO7	Channel 7: Analog Input or GPIO pin
13	AGIO8	Channel 8: Analog Input or GPIO pin
14	AGIO9	Channel 9: Analog Input or GPIO pin
15	AGIO10	Channel 10: Analog Input or GPIO pin
16	AGIO11	Channel 11: Analog Input or GPIO pin
17	AGIO12	Channel 12: Analog Input or GPIO pin
18	AGIO13	Channel 13: Analog Input or GPIO pin
19	AGIO14	Channel 14: Analog Input or GPIO pin
20	AGIO15	Channel 15: Analog Input or GPIO pin
21	IOVDD	Digital I/O power supply pin Connect a 0.1 μF ceramic capacitor to DGND near this pin.
22	DGND	Digital I/O ground pin
23	SDI	Digital data input pin Data input to this pin can be captured on the rising edge of SCK and used for A/D conversion channels or for setting the GPIO of each channel.
24	SDO	Digital data output pin The results of A/D conversion and register readout are output from this pin. When CSB is high, this pin is in a Hi-Z state.
-	EXP-PAD	Connect EXP-PAD to DGND

Block Diagram



**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Analog/Digital Supply Voltage	V <sub>DD</sub>	6.0	V
Digital I/O Supply Voltage	V <sub>IOVDD</sub>	6.0	V
AGIO Input Voltage	V <sub>AGIN</sub>	-0.3 to V <sub>DD</sub> +1.0	V
AGIO Input Current (Each Pin)	I <sub>AGIN1</sub>	±5	mA
AGIO Input Current (Total of All Pins)	I <sub>AGIN2</sub>	±35	mA
Digital Input Voltage (CSB,SCK,SDI)	V <sub>DIN</sub>	-0.3 to V <sub>IOVDD</sub> +0.3	V
Maximum Junction Temperature	T <sub>jmax</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Thermal Resistance**<sup>(Note 2)</sup>

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 4)</sup>	2s2p <sup>(Note 5)</sup>	
VQFN24FV4040				
Junction to Ambient	θ <sub>JA</sub>	150.6	27.9	°C/W
Junction to Top Characterization Parameter <sup>(Note 3)</sup>	Ψ <sub>JT</sub>	20	9	°C/W

(Note 2) Based on JESD51-2A (Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note 6)</sup>	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Analog/Digital Supply Voltage	V <sub>DD</sub>	2.7	-	5.5	V
Digital I/O Supply Voltage	V <sub>IOVDD</sub>	1.65	-	5.50	V
AGIO Input Voltage	V <sub>AGIN</sub>	0	-	V <sub>DD</sub>	V
Digital Input Voltage (CSB,SCK,SDI)	V <sub>DIN</sub>	0	-	V <sub>IOVDD</sub>	V
Operating Temperature	T <sub>opr</sub>	-40	+25	+125	°C
Clock Frequency	f <sub>SCK</sub>	0.50	-	10	MHz
Sampling Rate	f <sub>s</sub>	-	-	0.5	MSPS

**Electrical Characteristics**

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>IOVDD</sub> = 1.65 V to 5.5 V, f<sub>SCK</sub> = 5 MHz, f<sub>S</sub> = 0.25 MSPS, R<sub>IN</sub> = 24 Ω, C<sub>IN</sub> = 33 nF

Parameter	Symbol	Min	Typ	Max	Unit	Parameter
Statistic Converter Characteristics <sup>(Note 7)</sup>						
Resolution	R <sub>ES</sub>	-	12	-	bit	
Integral Non-linearity1	I <sub>NL1</sub>	-2.0	-	+2.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Integral Non-linearity2	I <sub>NL2</sub>	-2.0	-	+2.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Differential Non-linearity1	D <sub>NL1</sub>	-1.0	-	+1.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Differential Non-linearity2	D <sub>NL2</sub>	-1.0	-	+1.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Offset Error 1	O <sub>E1</sub>	-4.0	-	+4.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Offset Error 2	O <sub>E2</sub>	-4.0	-	+4.0	LSB	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Gain Error 1	G <sub>E1</sub>	-0.15	-	+0.15	%	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Gain Error 2	G <sub>E2</sub>	-0.15	-	+0.15	%	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Dynamic Converter Characteristics (f <sub>IN</sub> = 2 kHz, V <sub>IN</sub> = -0.02 dBFS) <sup>(Note 7)</sup>						
Signal to Noise Ratio1	S <sub>NR1</sub>	68.0	72.0	-	dB	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Signal to Noise Ratio2	S <sub>NR2</sub>	68.0	72.0	-	dB	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Effective Number of Bits1	E <sub>NOB1</sub>	10.0	11.6	-	bit	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Effective Number of Bits2	E <sub>NOB2</sub>	10.0	11.6	-	bit	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V
Inter-channel Isolation1	I <sub>SO1</sub>	-	-85	-	dB	Ta = 25 °C, V <sub>DD</sub> = 5.0 V V <sub>IOVDD</sub> = 3.0 V
Inter-channel Isolation2	I <sub>SO2</sub>	-	-84	-	dB	Ta = 25 °C, V <sub>DD</sub> = 3.0 V V <sub>IOVDD</sub> = 3.0 V

(Note 7) Characteristic values are measured when all AGIO pins are set to GPI\_EN = 0 and GPO\_EN = 0.

**Electrical Characteristics - continued**

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V<sub>DD</sub> = 2.7 V to 5.5 V, V<sub>IOVDD</sub> = 1.65 V to 5.5 V, f<sub>SCK</sub> = 5 MHz, f<sub>s</sub> = 0.25 MSPS

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Analog Input Characteristics</b>						
Input Voltage Range	V <sub>AGIN</sub>	0	-	V <sub>DD</sub>	V	
Input DC Leakage Current	I <sub>LEAK</sub>	-10	±0.1	+10	μA	V <sub>AGIN</sub> = 0 V or V <sub>DD</sub>
Input Capacitance1	C <sub>INA1</sub>	-	14	-	pF	track mode, V <sub>DD</sub> = 5 V
Input Capacitance2	C <sub>INA2</sub>	-	4	-	pF	hold mode, V <sub>DD</sub> = 5 V
<b>Digital Input Characteristics (CSB,SCK,SDI)</b>						
High Input Voltage	V <sub>IH</sub>	0.7 x V <sub>IOVDD</sub>	-	-	V	
Low Input Voltage	V <sub>IL</sub>	-	-	0.3 x V <sub>IOVDD</sub>	V	
Input Current	I <sub>DIN</sub>	-1	±0.1	+1	μA	V <sub>DIN</sub> = 0 V or V <sub>IOVDD</sub>
Input Capacitance	C <sub>DIN</sub>	-	4	-	pF	
<b>Digital Output Characteristics (SDO)</b>						
Output High Voltage1	V <sub>OH1</sub>	V <sub>IOVDD</sub> - 0.20	V <sub>IOVDD</sub> - 0.03	-	V	I <sub>SOURCE</sub> = 200 μA
Output High Voltage2	V <sub>OH2</sub>	-	V <sub>IOVDD</sub> - 0.1	-	V	I <sub>SOURCE</sub> = 1 mA
Output Low Voltage1	V <sub>OL1</sub>	-	0.02	0.40	V	I <sub>SINK</sub> = 200 μA
Output Low Voltage2	V <sub>OL2</sub>	-	0.1	-	V	I <sub>SINK</sub> = 1 mA
High-Z Leakage Current	I <sub>OZ</sub>	-10	±0.1	+10	μA	V <sub>OZ</sub> = 0 V or V <sub>DD</sub>
High-Z Output Capacitance	C <sub>OUT</sub>	-	4	-	pF	
<b>Digital Input Characteristics (GPI)</b>						
High Input Voltage	V <sub>AGIH</sub>	0.7 x V <sub>DD</sub>	-	V <sub>DD</sub>	V	
Low Input Voltage	V <sub>AGIL</sub>	0	-	0.3 x V <sub>DD</sub>	V	
Input Current	I <sub>AGIN</sub>	-10	±0.1	+10	μA	V <sub>AGIN</sub> = 0 V or V <sub>DD</sub>
<b>Digital Output Characteristics (GPO)</b>						
Output High Voltage	V <sub>OH</sub>	0.8 x V <sub>DD</sub>	-	V <sub>DD</sub>	V	I <sub>SOURCE</sub> = 2 mA
Output Low Voltage	V <sub>OL</sub>	0	-	0.2 x V <sub>DD</sub>	V	I <sub>SINK</sub> = 2 mA
<b>Current Consumption</b>						
VDD Operational Current Consumption1	I <sub>A1</sub>	-	1.8	2.7	mA	V <sub>DD</sub> = V <sub>IOVDD</sub> = 5.5 V, f <sub>s</sub> = 0.5 MSPS
VDD Operational Current Consumption2	I <sub>A2</sub>	-	1.4	2.1	mA	V <sub>DD</sub> = V <sub>IOVDD</sub> = 3.6 V, f <sub>s</sub> = 0.5 MSPS
VDD Operational Current Consumption3	I <sub>A3</sub>	-	1.5	2.3	mA	V <sub>DD</sub> = V <sub>IOVDD</sub> = 5.5 V, f <sub>s</sub> = 0.25 MSPS
VDD Operational Current Consumption4	I <sub>A4</sub>	-	1.2	1.8	mA	V <sub>DD</sub> = V <sub>IOVDD</sub> = 3.6 V, f <sub>s</sub> = 0.25 MSPS
VDD Stand-by Current Consumption1	I <sub>S1</sub>	-	0.6	6.0	μA	Ta = 25 °C, V <sub>DD</sub> = V <sub>IOVDD</sub> = CSB = 5.5 V, SCK = 0 V
VDD Stand-by Current Consumption2	I <sub>S2</sub>	-	0.3	6.0	μA	Ta = 25 °C, V <sub>DD</sub> = V <sub>IOVDD</sub> = CSB = 3.6 V, SCK = 0 V
VDD Stand-by Current Consumption3	I <sub>S3</sub>	-	0.6	50	μA	V <sub>DD</sub> = V <sub>IOVDD</sub> = CSB = 5.5 V, SCK = 0 V
VDD Stand-by Current Consumption4	I <sub>S4</sub>	-	0.3	35	μA	V <sub>DD</sub> = V <sub>IOVDD</sub> = CSB = 3.6 V, SCK = 0 V

**Timing Specifications**

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), VDD = 2.7 V to 5.5 V, VIOVDD = 1.65 V to 5.5 V, fsck = 10 MHz, Capacitive load of the SDO pin = 25 pF

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Conversion Time	t <sub>CONV</sub>	-	16	-	SCK	
CSB Pulse Width	t <sub>1</sub>	40	-	-	ns	
CSB Setup Time	t <sub>2</sub>	20	-	-	ns	
CSB Hold Time	t <sub>3</sub>	20	-	-	ns	
SDO Enable Time	t <sub>4</sub>	-	-	30	ns	
SDO Access Time	t <sub>5</sub>	-	-	50	ns	
SCK Low Pulse Width	t <sub>6</sub>	0.4 x t <sub>SCK</sub>	-	-	ns	t <sub>SCK</sub> = 1/fsck
SCK High Pulse Width	t <sub>7</sub>	0.4 x t <sub>SCK</sub>	-	-	ns	t <sub>SCK</sub> = 1/fsck
SDO Disable Time	t <sub>8</sub>	-	-	30	ns	
SDI Setup Time	t <sub>9</sub>	10	-	-	ns	
SDI Hold Time	t <sub>10</sub>	10	-	-	ns	

(Note 8) When using a daisy-chain connection, the SDO pin is connected to the SDI pin of the subsequent device. Make sure that the sum of the SDO access time and the SDI setup time does not exceed the SCK low pulse width.

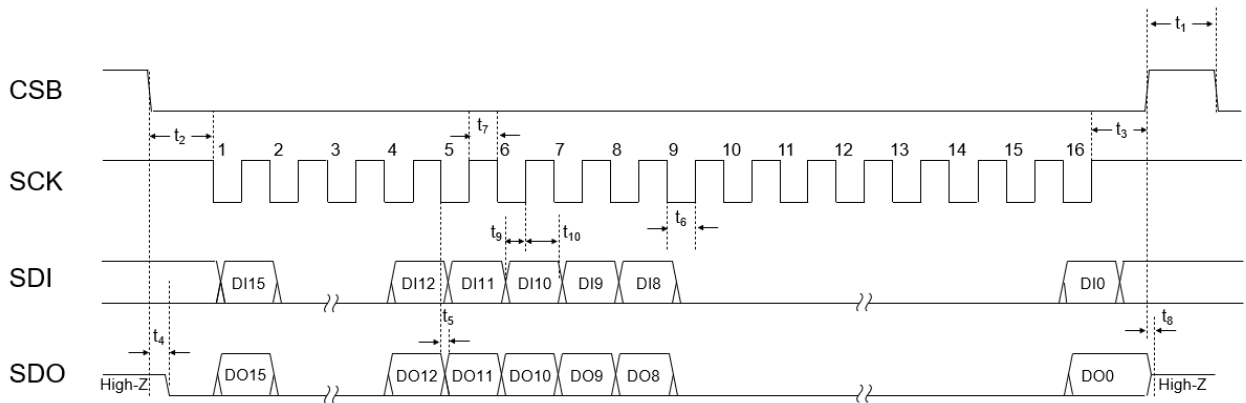


Figure 1. Serial Interface Timing Chart

**Term Definition****ACQUISITION TIME:**

It is the time when the voltage of the sampling capacitor equals input voltage from the charge start.

**INTEGRAL NON-LINEARLITY (INL):**

It is a measure of the deviation of each individual code from the fitted line obtained by applying the least-squares method to all codes, including those from zero scale (0.5 LSB below the first code transition) to full scale (0.5 LSB above the last code transition). The deviation from this line for any given code is measured at the center of that code value.

**DIFFERENTIAL NON-LINEARLITY (DNL):**

It is the measure of the maximum deviation from the ideal step size of 1 LSB.

**OFFSET ERROR (OE):**

It is the deviation of the first code transition "(000...000) to (000...001)" from the ideal of 0.5 LSB.

**FULL SCALE ERROR (FSE):**

It is the deviation of the last code transition "(111...110) to (111...111)" from the ideal of " $V_{DD} - 1.5 \text{ LSB}$ ".

**GAIN ERROR (GE):**

It is defined as full scale error minus offset error.

**EFFECTIVE NUMBER OF BITS (ENOB):**

It is another method of specifying Signal to Noise and Distortion Ratio. ENOB is defined as " $(\text{SINAD}-1.76)/6.02$ " and says that the converter is equivalent to a perfect A/D converter of this number of bits.

**SIGNAL TO NOISE RATIO (SNR):**

It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, not including harmonics and DC component.

**CONVERSION TIME:**

It is the required time for the A/D converter to convert the input signal to the digital code.

Typical Performance Curves

(Reference Data)

Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $V_{IOVDD} = 3\text{ V}$ ,  $f_{SCK} = 10\text{ MHz}$ ,  $f_s = 0.5\text{ MSPS}$

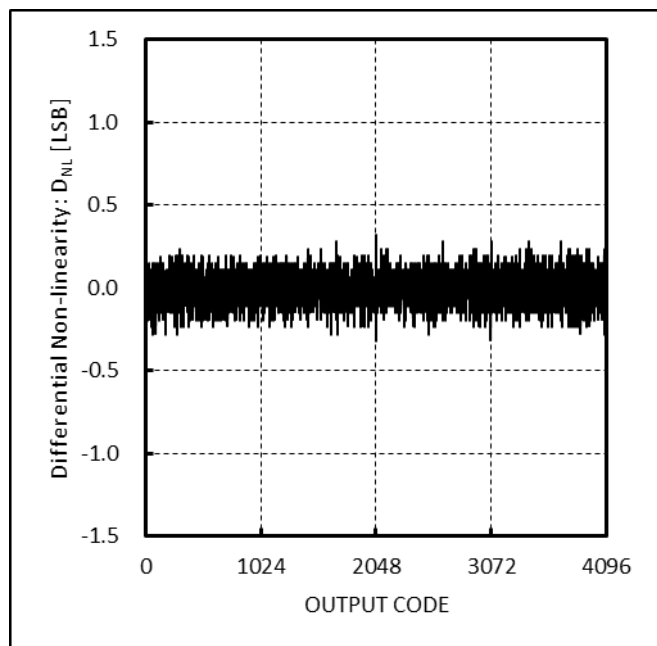


Figure 2. Differential Non-linearity vs OUTPUT CODE  
( $V_{IOVDD} = 3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ )

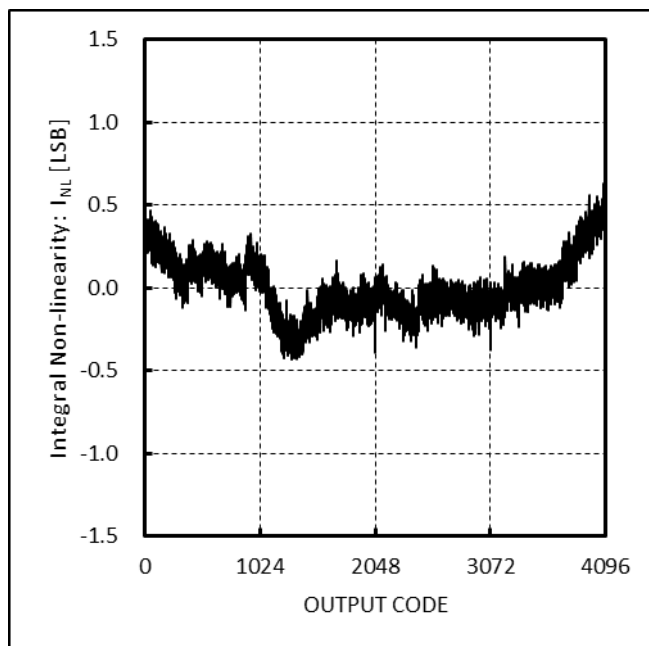


Figure 3. Integral Non-linearity vs OUTPUT CODE  
( $V_{IOVDD} = 3\text{ V}$ ,  $V_{DD} = 5\text{ V}$ )

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $V_{IOVDD} = 3\text{ V}$ ,  $f_{SCK} = 10\text{ MHz}$ ,  $f_s = 0.5\text{ MSPS}$

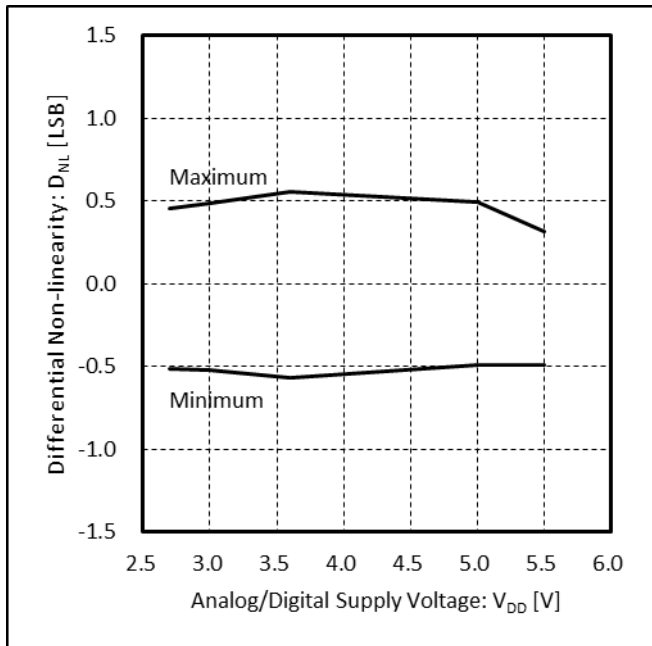


Figure 4.

Differential Non-linearity vs Analog / Digital Supply Voltage

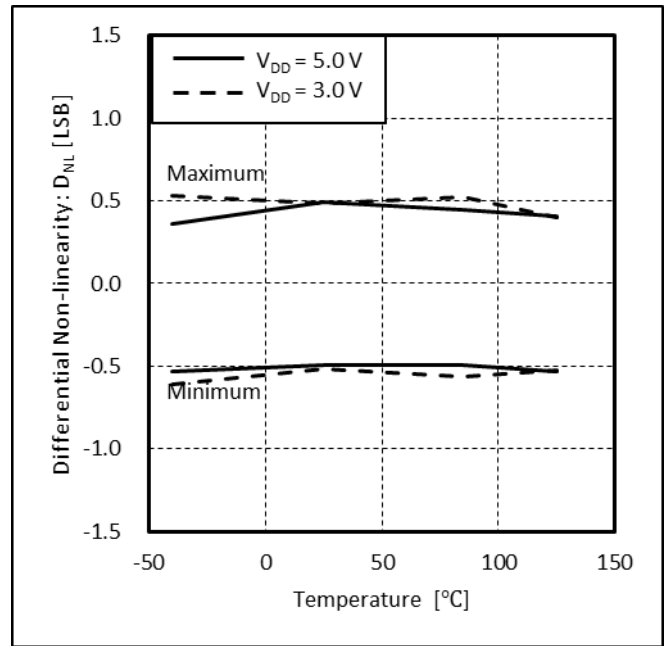


Figure 5. Differential Non-linearity vs Temperature

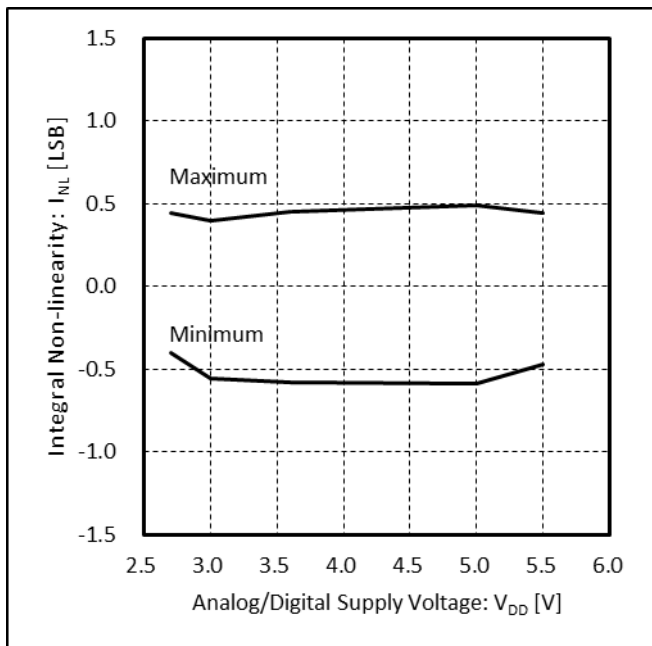


Figure 6.

Integral Non-linearity vs Analog / Digital Supply Voltage

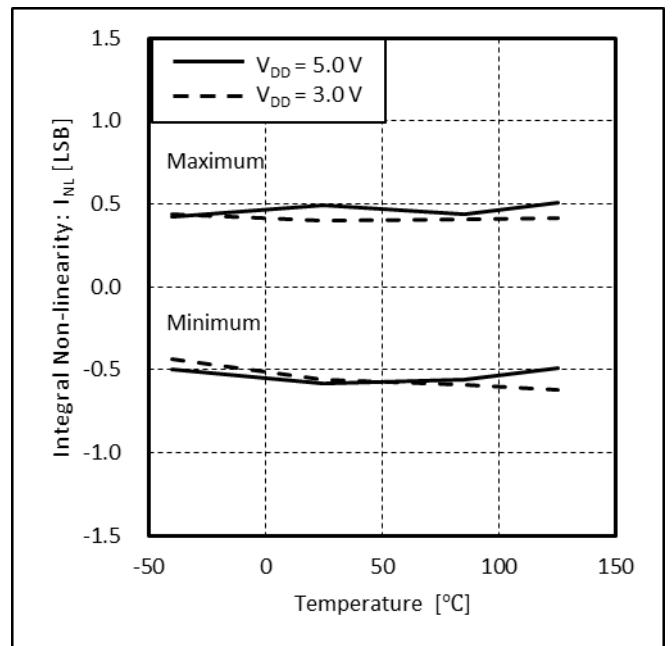


Figure 7. Integral Non-linearity vs Temperature

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $V_{IOVDD} = 3\text{ V}$ ,  $f_{SCK} = 10\text{ MHz}$ ,  $f_s = 0.5\text{ MSPS}$

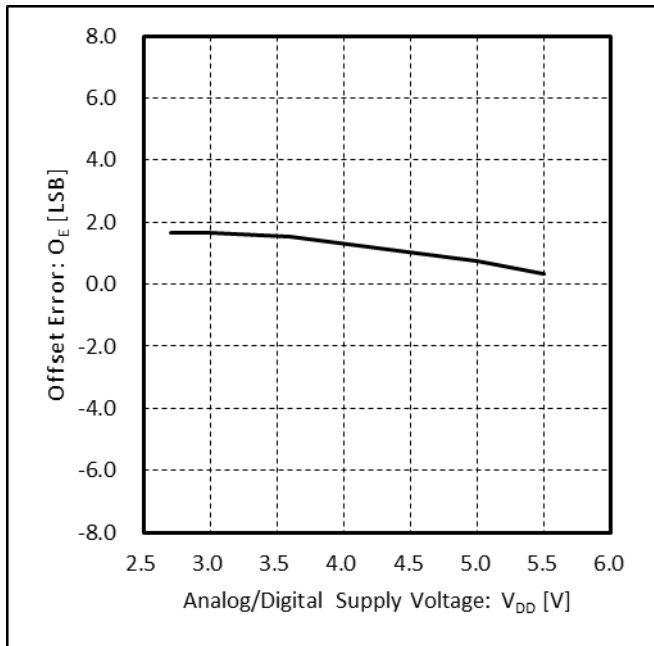


Figure 8.

Offset Error vs Analog / Digital Supply Voltage

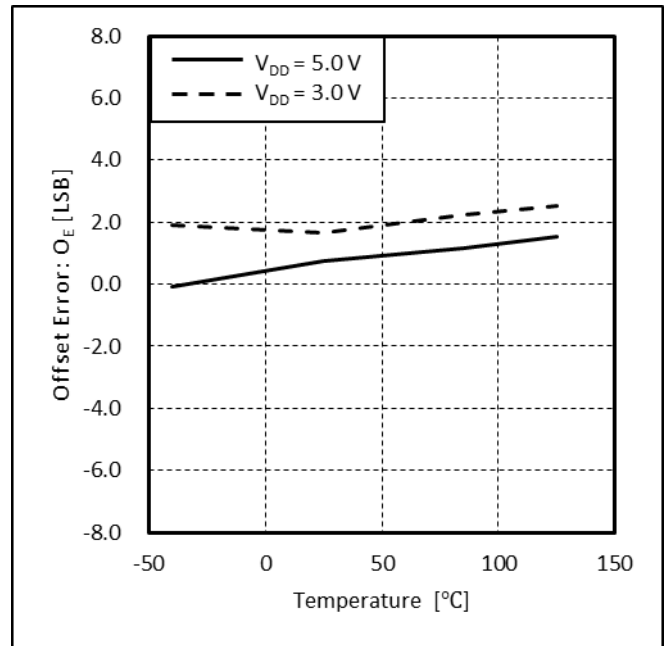


Figure 9. Offset Error vs Temperature

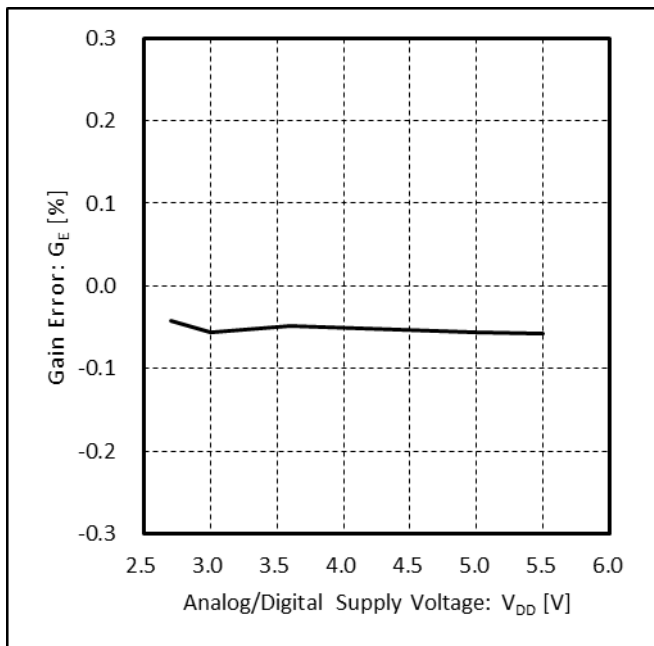


Figure 10.

Gain Error vs Analog / Digital Supply Voltage

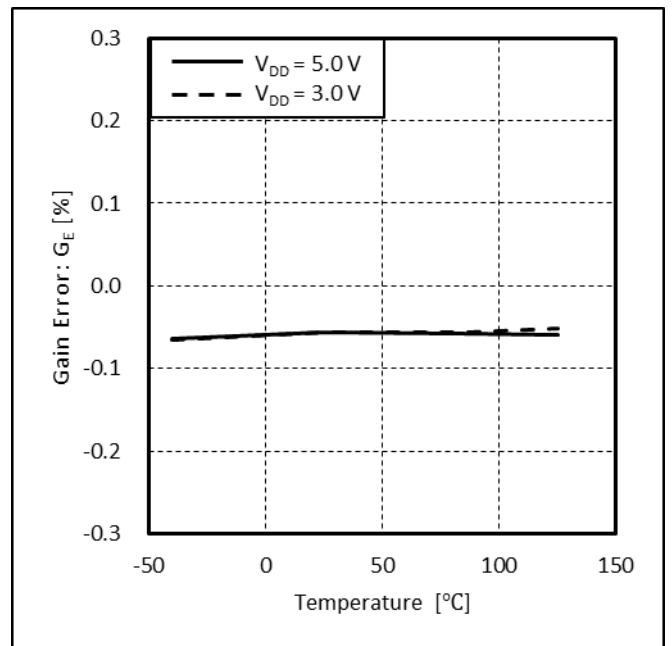


Figure 11. Gain Error vs Temperature

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $V_{IOVDD} = 3\text{ V}$ ,  $f_{SCK} = 10\text{ MHz}$ ,  $f_s = 0.5\text{ MSPS}$

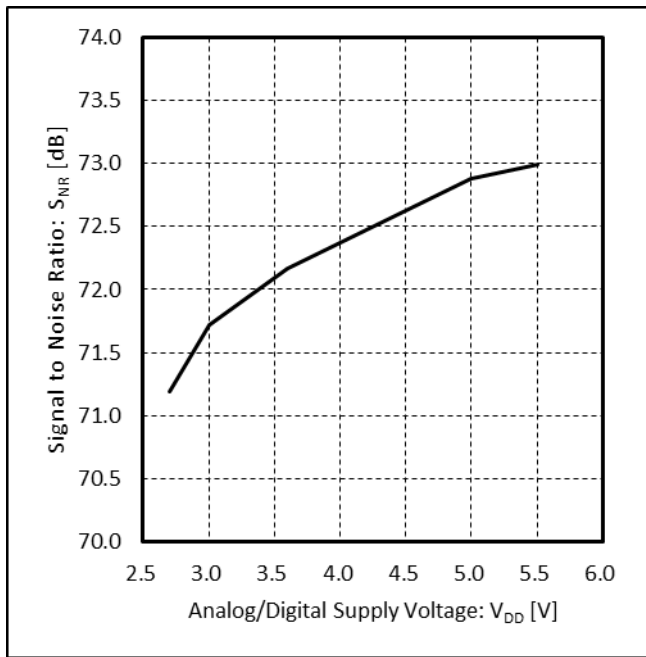


Figure 12.

Signal to Noise Ratio vs Analog / Digital Supply Voltage

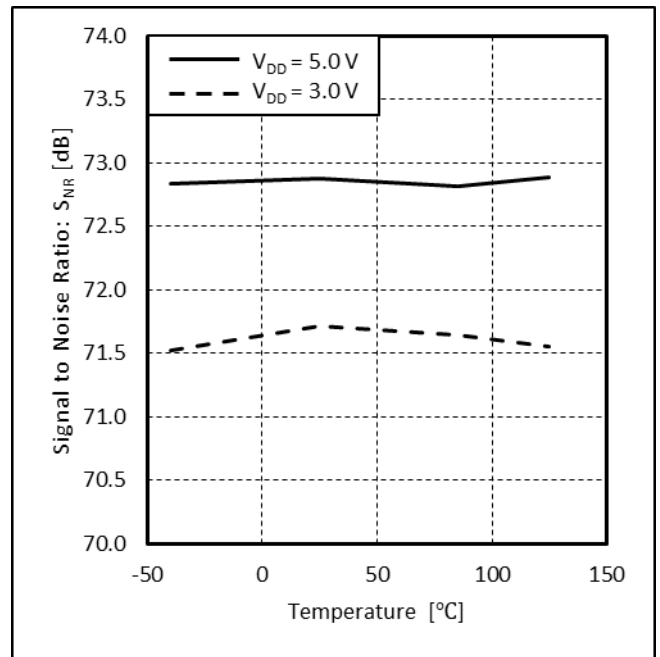


Figure 13. Signal to Noise Ratio vs Temperature

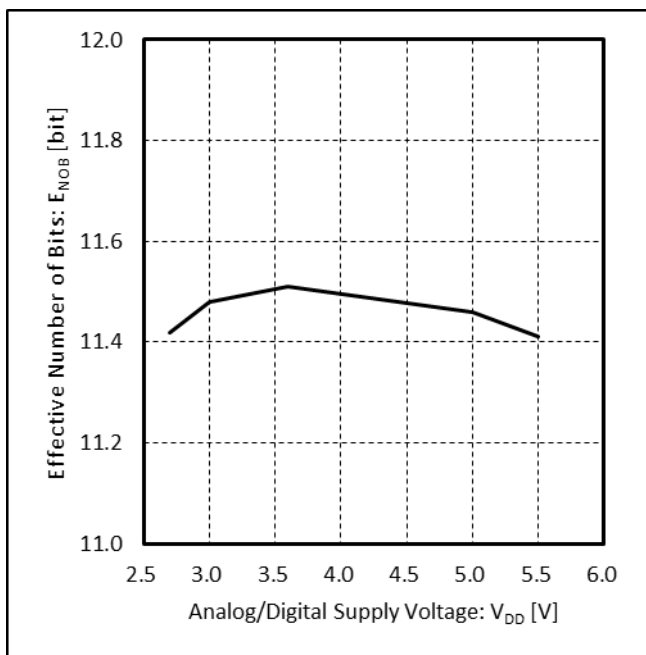


Figure 14.

Effective Number of Bits vs Analog / Digital Supply Voltage

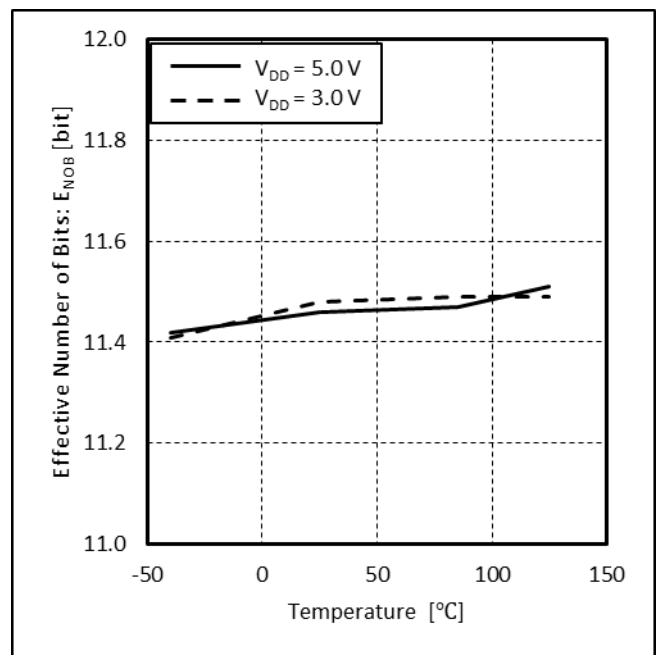


Figure 15. Effective Number of Bits vs Temperature

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3\text{ V}$ ,  $V_{IOVDD} = 3\text{ V}$ ,  $f_{SCK} = 10\text{ MHz}$ ,  $f_s = 0.5\text{ MSPS}$

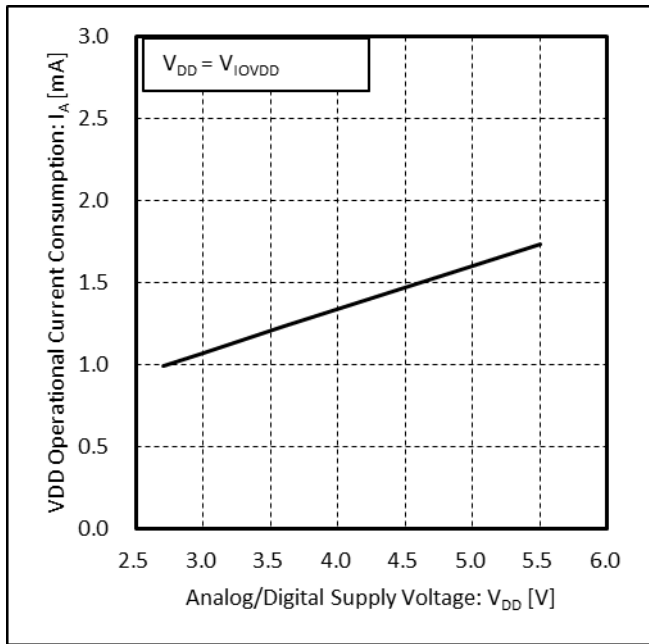


Figure 16. V<sub>DD</sub> Operational Current Consumption vs Analog / Digital Supply Voltage

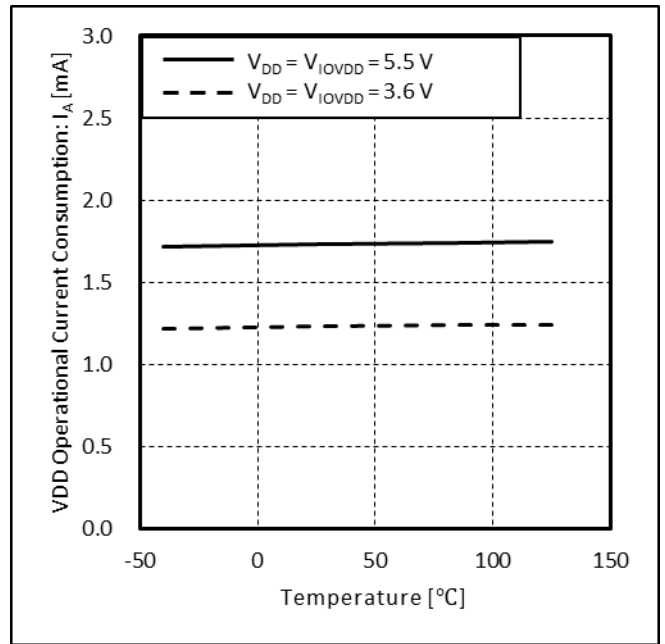


Figure 17. V<sub>DD</sub> Operational Current Consumption vs Temperature

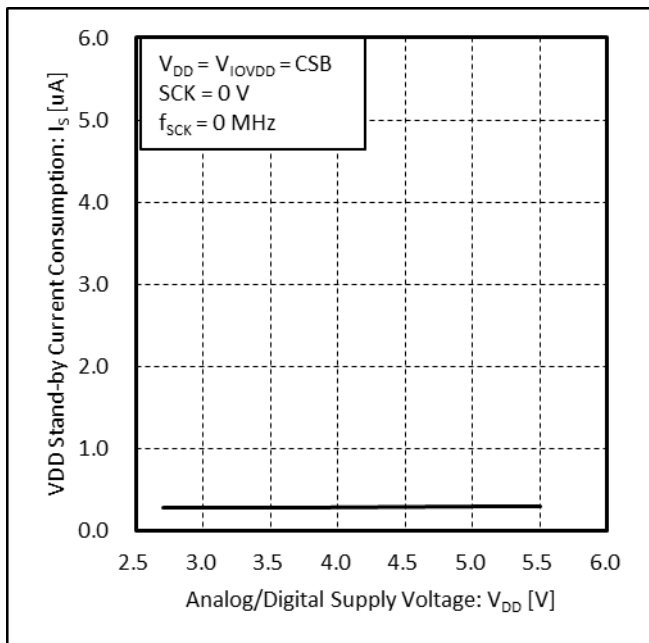


Figure 18. V<sub>DD</sub> Stand-by Current Consumption vs Analog / Digital Supply Voltage

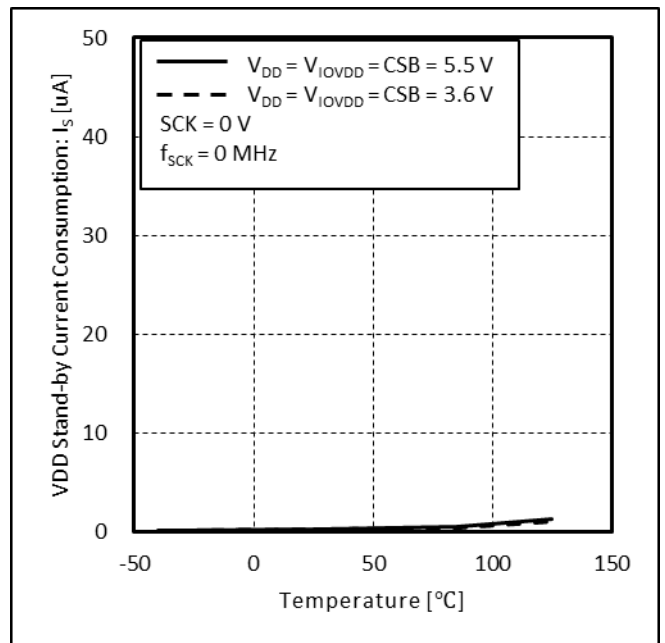


Figure 19. V<sub>DD</sub> Stand-by Current Consumption vs Temperature

Power-up Sequence

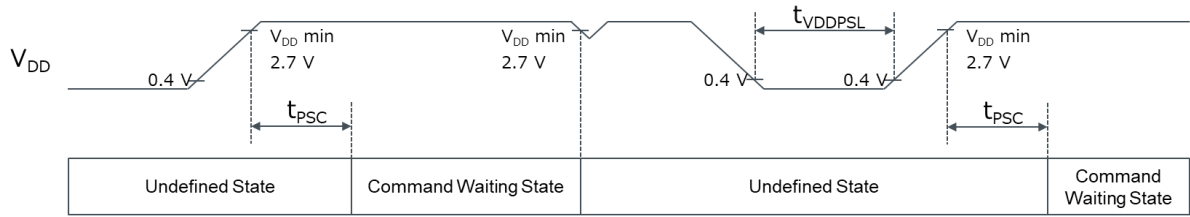


Figure 20. Power-up Timing Chart

T<sub>a</sub> = -40 °C to +125 °C

Parameter	Symbol	Min	Typ	Max	Unit
V <sub>DD</sub> power down time	t <sub>VDDPSL</sub>	1	-	-	ms
SPI command available time from Power-up	t <sub>PSC</sub>	0.1	-	-	ms

After power-on, commands must be issued only after the duration of t<sub>PSC</sub> has elapsed.  
 If the V<sub>DD</sub> supply voltage drops below the recommended operating range, the IC may enter an undefined state.  
 In such cases, power must be turned off completely and then reapplied.  
 Before applying V<sub>DD</sub>, ensure that the V<sub>DD</sub> voltage remains below 0.4 V for at least the duration of t<sub>VDDPSL</sub>.

Description of Functions

1. Overview of A/D Conversion Process

This product features a built-in successive-approximation A/D converter designed with a charge-redistribution D/A converter. Simplified schematics of the A/D converter are shown in Figure 21 and Figure 22.

Figure 21 shows the A/D converter in Track mode: the switch SW1 is in the position A, SW2 is closed and balances the comparator. Then, the sampling capacitor is charged with the analog input voltage  $V_{IN}$ .

Figure 22 shows the A/D converter in Hold mode. When a conversion starts, the A/D converter goes into Hold mode: SW2 becomes open, SW1 connects the sampling capacitor to ground through the position B and the comparator loses its balance. The control logic controls the input voltage of the comparator via the sampling capacitors of the charge-redistribution D/A converter to get the comparator back into a balanced state. A/D conversion finishes when the comparator balances again. The control logic also generates the output code of the A/D converter.

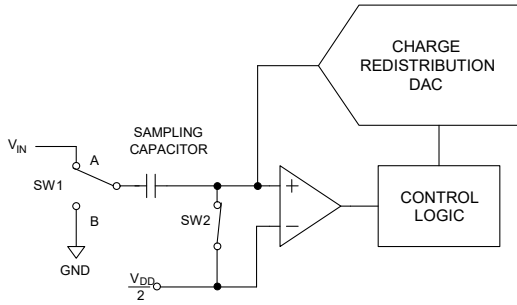


Figure 21. Track Mode

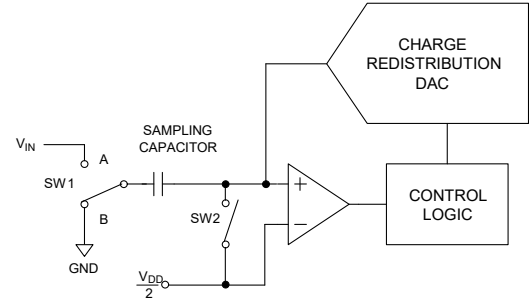


Figure 22. Hold Mode

2. Ideal Transfer Characteristics

Figure 23 shows the ideal transfer characteristics of this product. Code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for this product is  $V_{DD}/4096$ . The output code format of the A/D converter is straight binary.

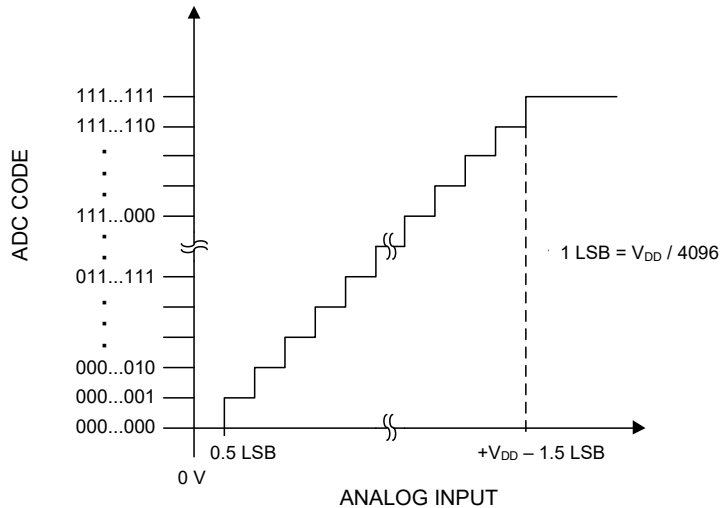


Figure 23. Ideal Transfer Characteristics

Description of Functions – continued

3. GPIO Function

This IC features integrated GPIO functionality, enabling each AGIO pin (AGIO0 to AGIO15) to operate as either a digital input or digital output.

The connection diagram for the AGIO pins is shown in Figure 24. Each AGIO pin can alternatively be configured as an analog input for A/D conversion by setting the ADSEL[3:0] bits during the ADC\_DATA read sequence (refer to Section 4.1). To enable GPIO functionality, the corresponding GPIO control registers—GPI\_EN, GPO\_EN, and GPO\_WRITE\_VALUE—must be configured during the Register Write sequence (see Section 4.3).

Upon power-up, all GPIO control registers are initialized to logic low, and GPIO functionality is disabled by default. The activation or deactivation of GPIO functions, as well as the output logic state of GPO, is applied on the rising edge of CSB following the register write operation.

To enable digital input (GPI) functionality, set the appropriate bit in the GPI\_EN register to high for the desired channel. Input data is latched on the falling edge of CSB and synchronized with SCK; therefore, the input signal must be stable prior to the falling edge of CSB.

To enable digital output (GPO) functionality, set the appropriate bit in the GPO\_EN register to high. The output logic level is determined by the corresponding bit in the GPO\_WRITE\_VALUE register: set to high for logic high output, or low for logic low output.

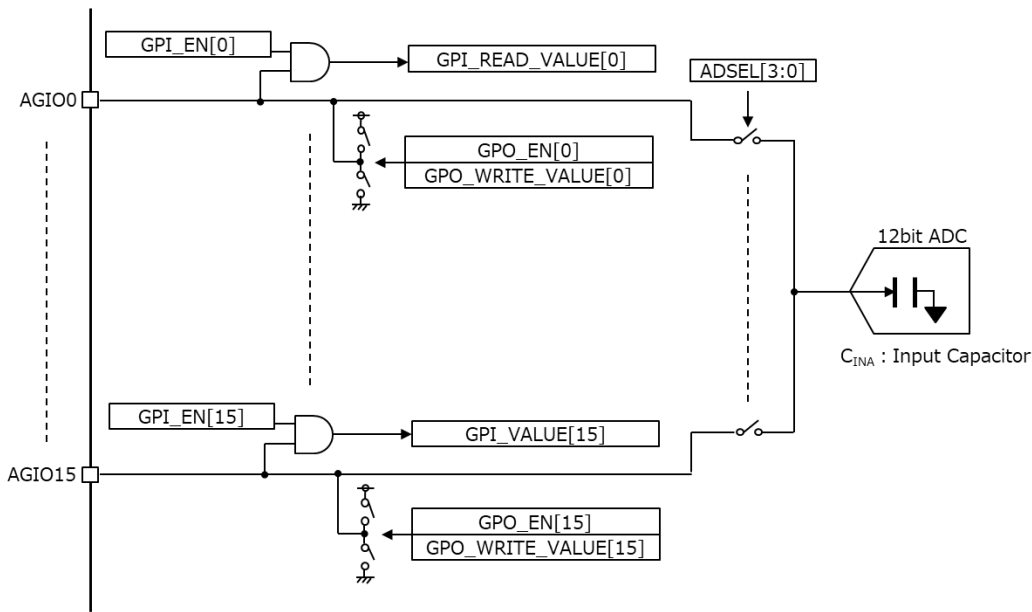


Figure 24. AGIO Pins Connection Diagram

Table 1. AGIO Pins Condition

GPO_EN	GPI_EN	GPO_WRITE_VALUE	Pin Condition
0	0	0	Analog Input
0	0	1	Analog Input
0	1	0	Digital Input
0	1	1	Digital Input
1	0	0	Digital L Output
1	0	1	Digital H Output
1	1	0	Digital L Output Digital Input
1	1	1	Digital H Output Digital Input

Description of Functions – continued

4. Serial Interface

Communication with this IC requires at least 16 SCK cycles while CSB is held low. SDI data is latched on the rising edge of SCK, and SDO data is output on the falling edge of SCK. The receiving side should capture the SDO data either on the rising or falling edge of SCK, after the SDO access time has elapsed.

4.1. ADC\_DATA Read Sequence

Figure 25 shows the communication format of the ADC\_DATA Read Sequence. In the first sequence after power-up, the A/D conversion result of AGIO0A is output from the SDO. By setting ADSEL[3:0] as shown in Table 2, the channel to be A/D converted in the next sequence is selected. The channel specified by ADSEL[3:0] enters track mode from the falling edge of the 1st clock to the falling edge of the 4th clock, and then operates in hold mode from the falling edge of the 4th clock to the falling edge of the 16th clock, during which A/D conversion is performed. If the channel specified by ADSEL[3:0] is connected to a GPI or GPO circuit when A/D conversion is executed, the STATUS\_FLAG is High. If the STATUS\_FLAG outputs High, either set GPI\_EN[x] and GPO\_EN[x] of the specified channel x to 0b, or power down the device once and then re-execute the ADC\_DATA Read Sequence. Refer to Section 4.3 for instructions on how to configure GPI\_EN[x] and GPO\_EN[x].

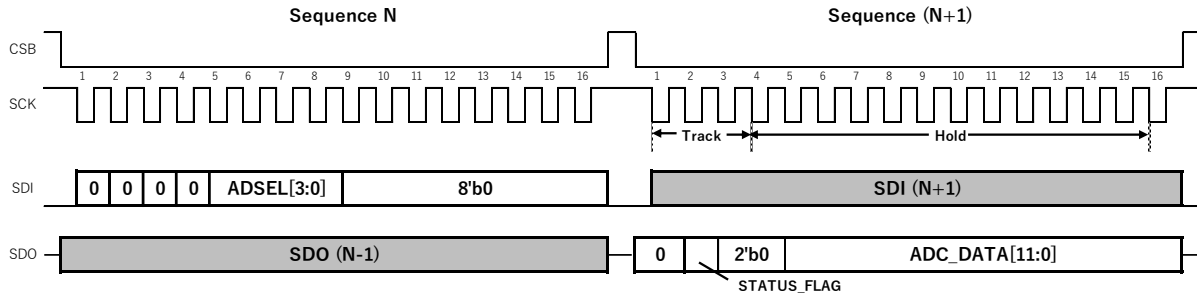


Figure 25. Communication Format of the ADC\_DATA Read Sequence

Table 2. ADC Input Channel Selection

ADSEL[3:0]	
0000b: AGIO0 (Default)	1000b: AGIO8
0001b: AGIO1	1001b: AGIO9
0010b: AGIO2	1010b: AGIO10
0011b: AGIO3	1011b: AGIO11
0100b: AGIO4	1100b: AGIO12
0101b: AGIO5	1101b: AGIO13
0110b: AGIO6	1110b: AGIO14
0111b: AGIO7	1111b: AGIO15

Description of Functions – continued

4.2. Register Read Sequence

The communication format of the Register Read sequence is shown in Figure 26. In the first sequence immediately after power-up, the A/D conversion result of AGIO0 is output from the SDO.

By setting IOSET = 1 and R/W = 1, and specifying the Address, the value of the register at the specified address can be read in the next sequence.

For the configuration of Address[3:0], refer to Table 3. Register Map.

When the GPI\_READ\_VALUE registers (Addresses: 0x2, 0x3) are specified in the Register Read Sequence, the input state of the selected channel is captured and can be read from the register.

The input state is captured between the falling edge of the 1st clock and the falling edge of the 8th clock in the sequence following the address specification.

If the input state changes during this interval, incorrect data may be captured.

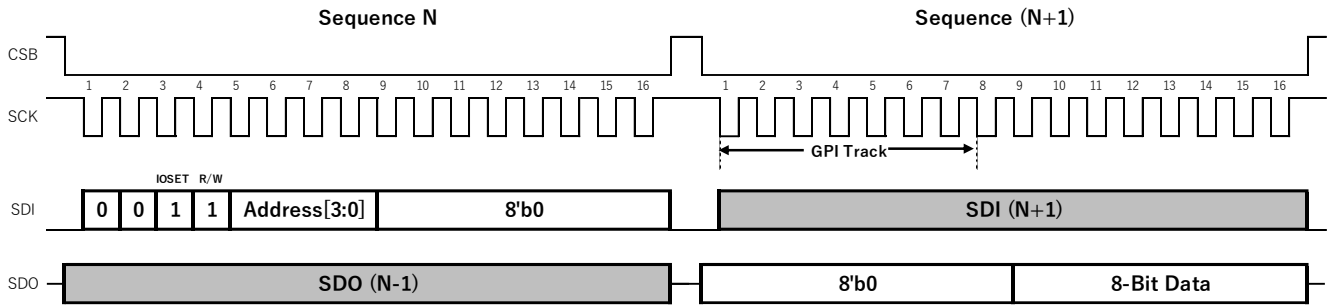


Figure 26. Communication Format of the Register Read Sequence

4.3. Register Write Sequence

Figure 27 shows the communication format of the Register Write sequence. In the first sequence immediately after power-up, the A/D conversion result of AGIO0 is output. By setting IOSET = 1 and R/W = 0, and specifying the Address, data can be written to the corresponding register. Refer to Table 3. Register Map for the configuration of Address[3:0]. The AGIO pin connections and GPO output states are updated on the rising edge of CSB.

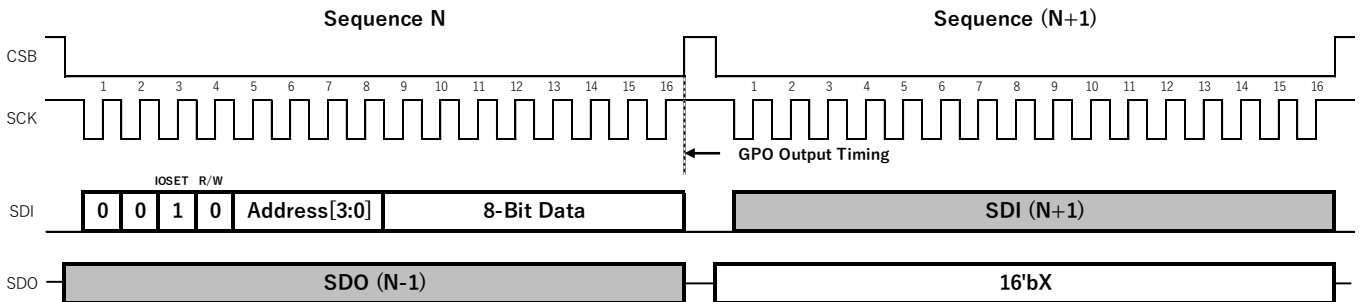


Figure 27. Communication Format of the Register Write Sequence

Description of Functions – continued

Table 3. Register Map

Address	Register Name	R/W	Initial	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	DESCRIPTION
0x2	GPI_READ_VALUE_15_8	R	0x00	GPI_READ_VALUE [15:8]								Input Logic Levels for AGIO15 to AGIO8 0: L-level input 1: H-level input When GPI_EN[x] is set to 0b, the value is 0
0x3	GPI_READ_VALUE_7_0	R	0x00	GPI_READ_VALUE [7:0]								Input Logic Levels for AGIO7 to AGIO0 0: L-level input 1: H-level input When GPI_EN[x] is set to 0b, the value is 0
0x4	WRITE_ZERO	R/W	0x00	0x00								
0x5	WRITE_ZERO	R/W	0x00	0x00								
0x6	GPI_EN_15_8	R/W	0x00	GPI_EN [15:8]								GPI Enable Settings for AGIO15 to AGIO8 0: GPI disabled 1: GPI enabled Pins used for AD conversion must be set to 0
0x7	GPI_EN_7_0	R/W	0x00	GPI_EN [7:0]								GPI Enable Settings for AGIO7 to AGIO0 0: GPI disabled 1: GPI enabled Pins used for AD conversion must be set to 0
0xA	GPO_EN_15_8	R/W	0x00	GPO_EN [15:8]								GPO Enable Settings for AGIO15 to AGIO8 0: GPO disabled (High-Z) 1: GPO enabled Pins used for AD conversion must be set to 0
0xB	GPO_EN_7_0	R/W	0x00	GPO_EN [7:0]								GPO Enable Settings for AGIO7 to AGIO0 0: GPO disabled (High-Z) 1: GPO enabled Pins used for AD conversion must be set to 0
0xE	GPO_WRITE_VALUE_15_8	R/W	0x00	GPO_WRITE_VALUE [15:8]								Output Logic Levels for AGIO15 to AGIO8 0: L-level output 1: H-level output
0xF	GPO_WRITE_VALUE_7_0	R/W	0x00	GPO_WRITE_VALUE [7:0]								Output Logic Levels for AGIO7 to AGIO0 0: L-level output 1: H-level output

Description of Functions – continued

■ Example of GPI Usage

As an example, Figure 28 shows the IC connection diagram when pins AGIO15 to AGIO8 are configured as GPI input and their input states are read.

The corresponding configuration method is shown in Table 4.

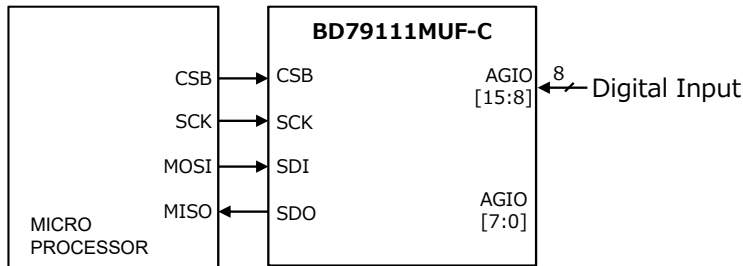


Figure 28. IC Connection Diagram for GPI Usage

Table 4. Example Procedure for GPI Configuration

Configuration Procedure		IOSET	R/W	Address [3:0]	8-Bit_Data
STEP1	Configure AGIO15 to AGIO8 as GPI	1b	0b	0x6	0xFF
STEP2	Read input logic levels of AGIO15 to AGIO8	1b	1b	0x2	-
STEP3	Repeat STEP 2 continuously	-	-	-	-

■ Example of GPO Usage

As an example, Figure 29 shows the IC connection diagram when pins AGIO15 to AGIO8 are used for A/D conversion and pins AGIO7 to AGIO0 are configured as GPO outputs.

The corresponding configuration procedure is shown in Table 5.

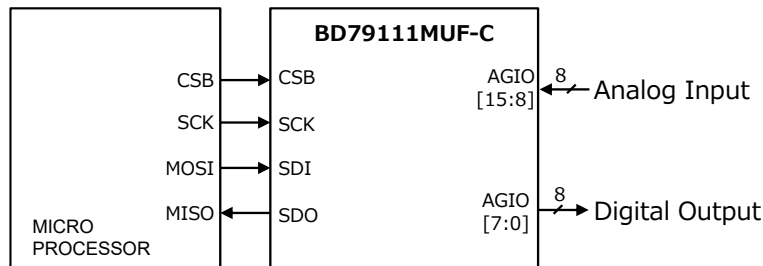


Figure 29. IC Connection Diagram for GPO Usage

Table 5. Example Procedure for GPO Configuration

Configuration Procedure		IOSET	R/W	Address [3:0]	8-Bit_Data
STEP1	Configure AGIO7 to AGIO0 as GPO	1b	0b	0xB	0xFF
STEP2	Read ADC value from AGIO8	0b	{0b+ADSEL[3:0]} = 01000b		-
STEP3	Read ADC value from AGIO9	0b	{0b+ADSEL[3:0]} = 01001b		-
⋮					
STEP9	Read ADC value from AGIO15	0b	{0b+ADSEL[3:0]} = 01111b		-
STEP10	Set the output logic levels for AGIO7 to AGIO0	1b	0b	0xF	Configuration
STEP11	Repeat STEP 2 to STEP 10 continuously	-	-	-	-

Description of Functions – continued

4.4. CRC Function

This IC supports a CRC (Cyclic Redundancy Check) function that appends CRC data to either A/D conversion data or register read values.

Figure 30 shows the communication format when the CRC function is enabled. When using the CRC function, set CRC\_EN to 1 and continue operation with CRC\_EN remaining enabled and 32 clock cycles (32 CLK) per sequence. The output data from the first sequence after switching CRC\_EN to 1 is invalid. CRC becomes effective from the next sequence, and valid data can be obtained. The output data during A/D conversion includes ADSEL[3:0] (see Table 2) and CRC[7:0]. The output data during register read includes Address[3:0] (see Table 3) and CRC[7:0].

Transmission errors can be detected by comparing the ADSEL[3:0] (or Address[3:0]) values between SDI and SDO. Reception errors can be detected by comparing the CRC[7:0] value from SDO with the CRC value calculated on the host side.

The CRC[7:0] is calculated using the generator polynomial CRC-8-CCITT ( $x^8 + x^2 + x + 1$ ) (1 0000 0111). The CRC[7:0] output is the remainder obtained by dividing either ADC\_DATA[11:0] or {4'b0 + 8-Bit\_Data} by the polynomial (1 0000 0111).

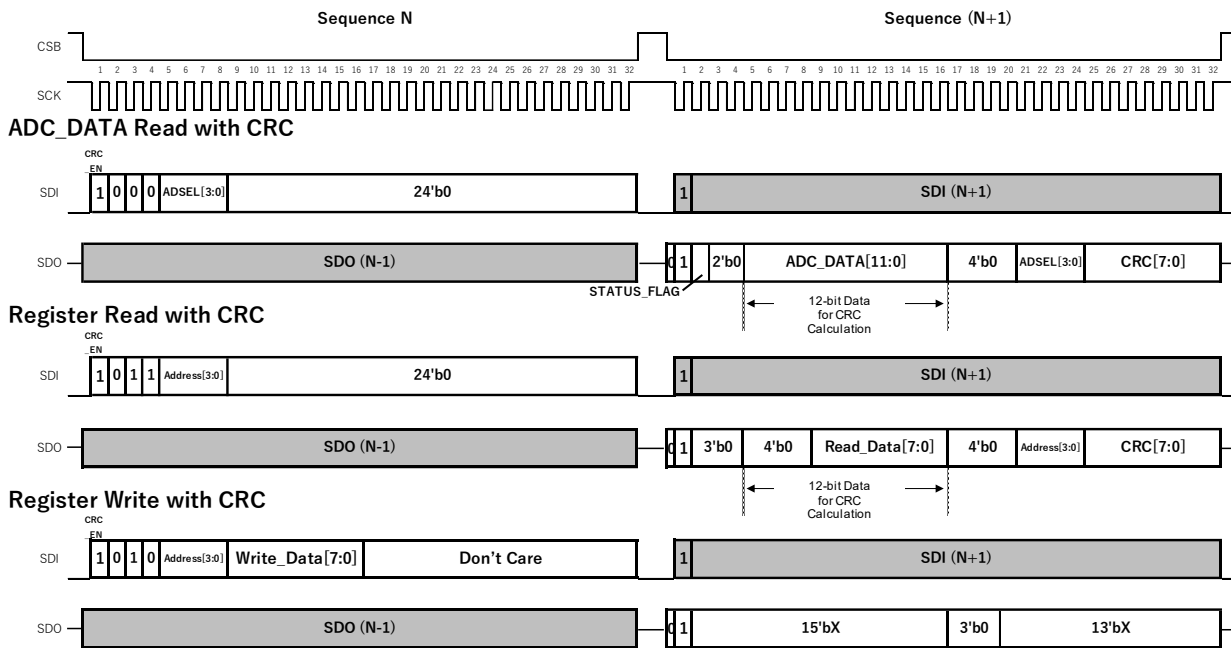


Figure 30. Communication Format When CRC Function is Enabled

Description of Functions – continued

4.5. Daisy-Chain Connection

By connecting multiple ICs of this type in a daisy-chain configuration, it is possible to output the data from all ICs through the SDO of the last IC in the chain.

As an example, Figure 31 shows the connection configuration when three ICs are connected in a daisy chain, and Figure 32 illustrates the corresponding communication format. To retrieve data from all connected ICs, (number of connected devices x 16) clocks are required while CSB is held Low. As long as CSB remains Low, the SDI data is passed along with a delay of 16 CLK to the next IC in the chain or to the communication host. The data format for each IC is the same as when communicating without daisy-chaining. Track/Hold and GPIO data updates are executed simultaneously across all ICs, as shown in Figure 33.

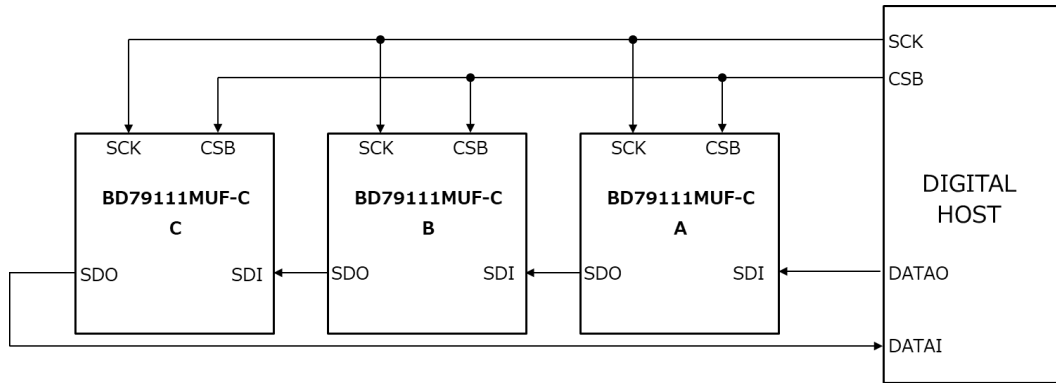


Figure 31. Configuration for Daisy Chain Connection of 3 ICs

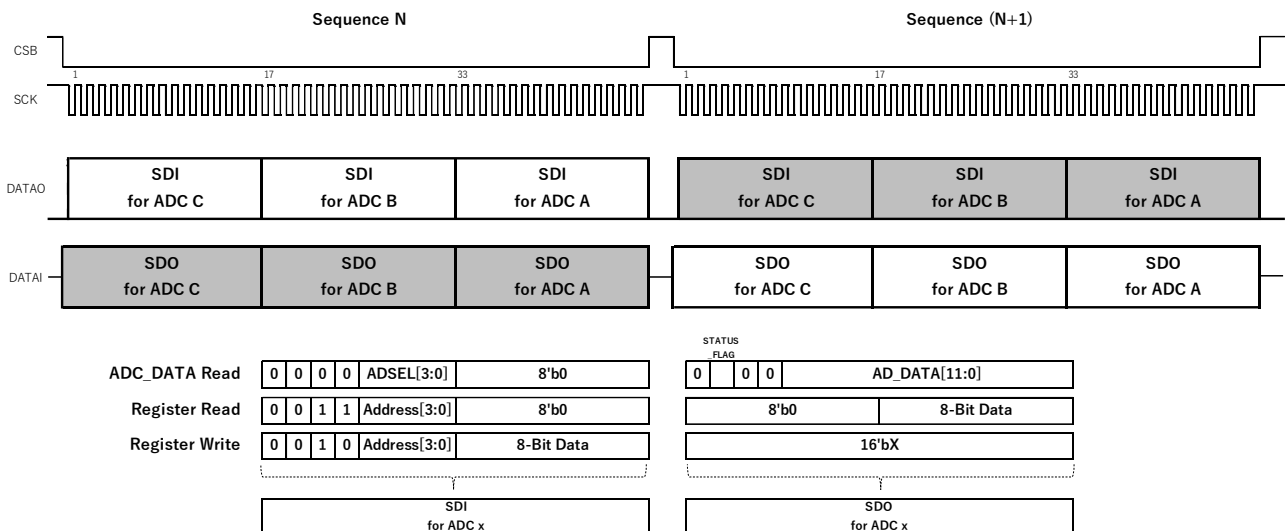


Figure 32. Timing Format for Daisy-Chain Connection of 3 ICs

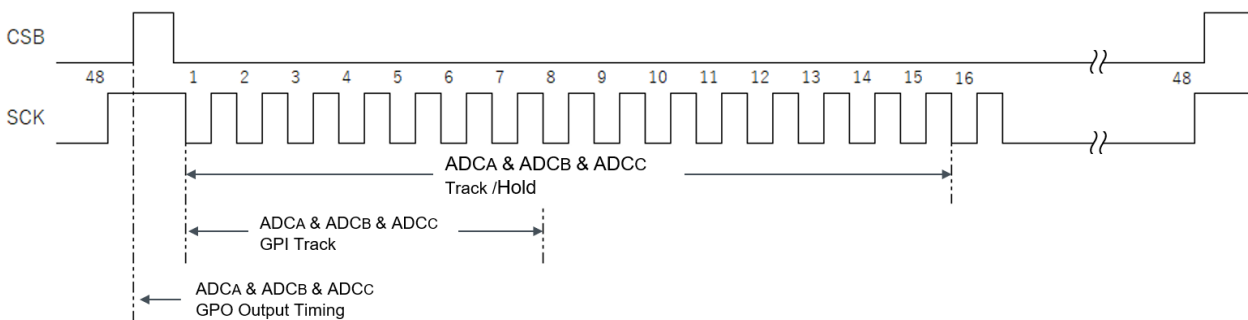


Figure 33. AGIO Pin Update Timing for Daisy-Chain Connection of 3 ICs

Description of Functions – continued

4.6. CRC Function in Daisy-Chain Configuration

CRC Function can also be used when ICs are connected in a daisy-chain configuration. The connection setup is the same as shown in Figure 31.

Figure 34 illustrates the CRC Function enable format when three ICs are connected in a daisy chain. When switching CRC\_EN in a daisy-chain configuration, set the CRC\_EN bit to High for each IC, and write Low to all other bits.

The number of SCK clock cycles required is (number of connected devices x 32) clocks.

A/D conversion data readout and register Read/Write operations can be performed starting from the second sequence after CRC Function has been enabled.

Figure 35 shows the communication format when CRC Function is enabled with three ICs connected in a daisy chain. For the data structure corresponding to each IC, refer to Section 4.4.

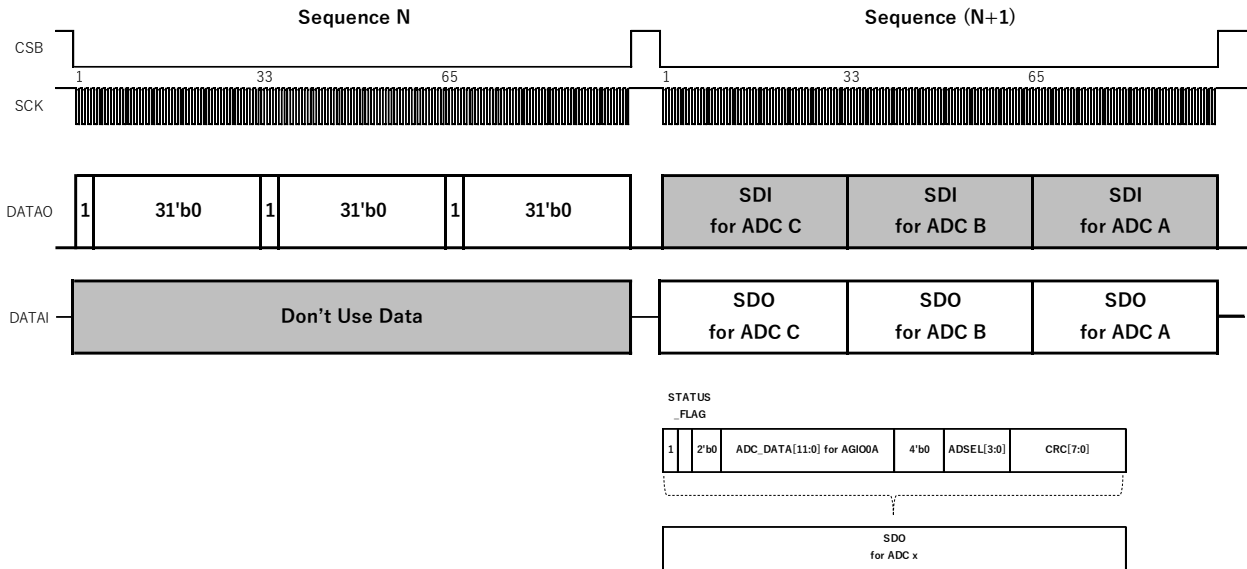


Figure 34. CRC\_EN = 1 Switching Format for Daisy-Chain Connection of 3 ICs

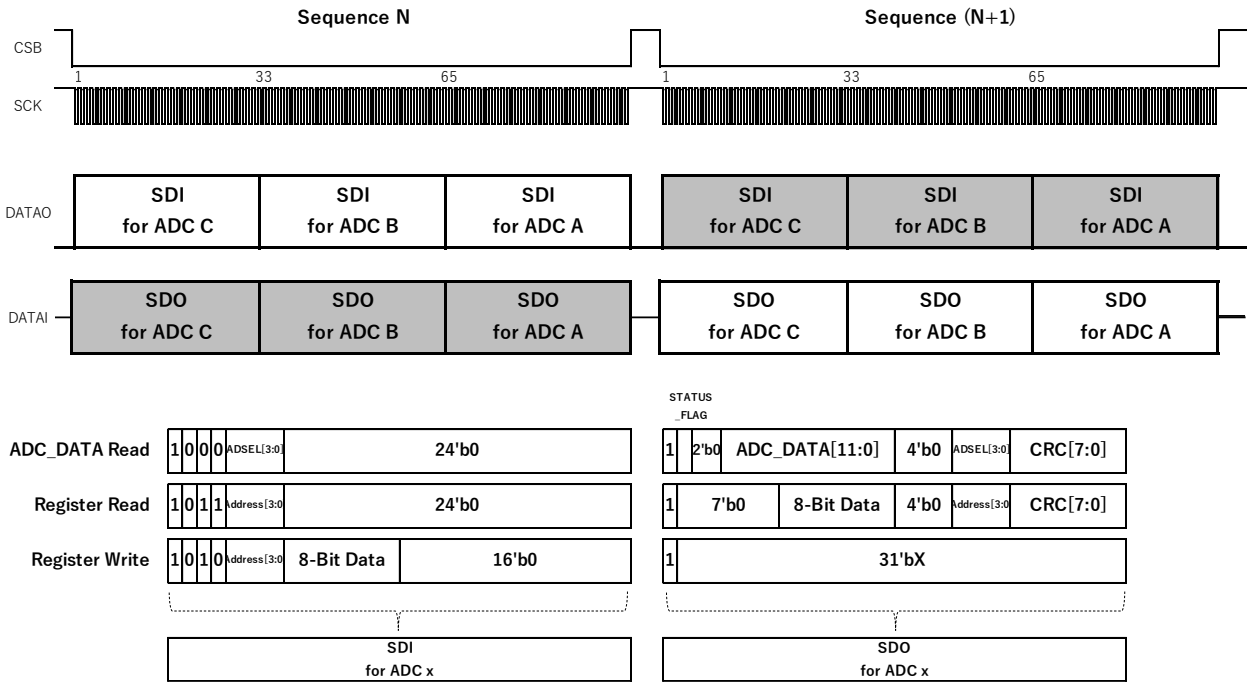


Figure 35. Communication Format in Daisy-Chain Configuration with CRC Function Enabled

Application Example

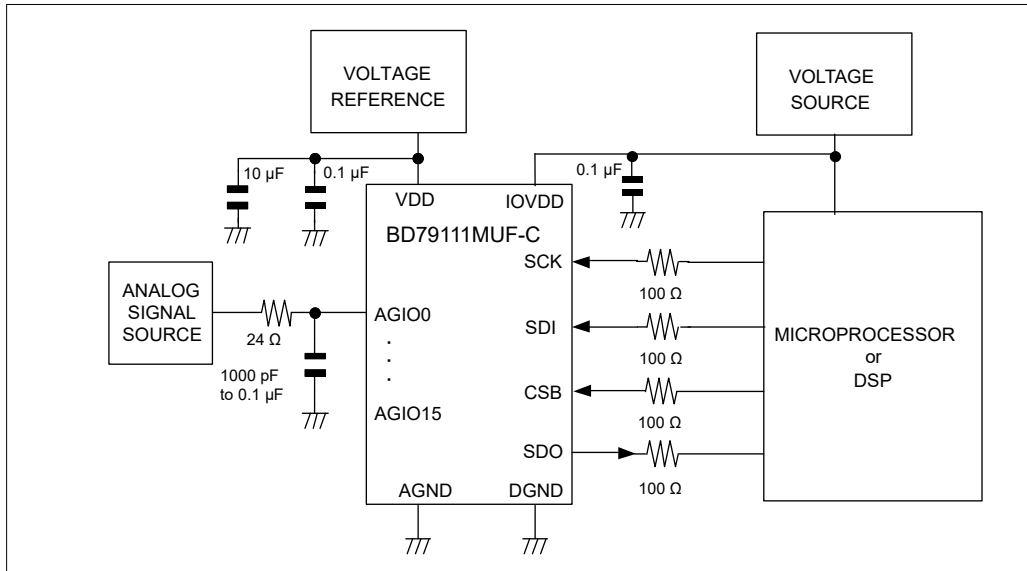


Figure 36. Application Circuit

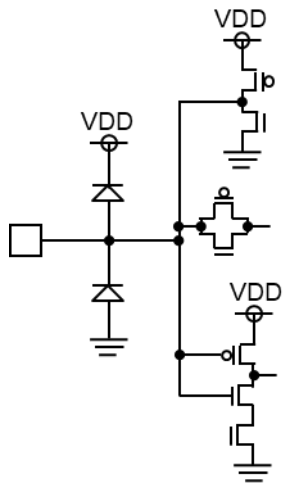
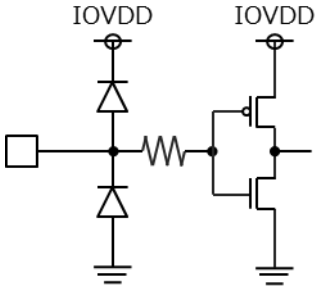
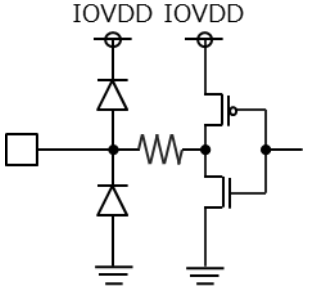
In the application circuit shown in Figure 36, to maximize its original performance, a constant voltage source is connected to the power supply pin, and one bypass capacitor is placed between the IOVDD-DGND pin, while two bypass capacitors for high and low frequencies are placed between the VDD-AGND pin. Use a 0.1 µF ceramic capacitor and a 1 µF to 10 µF capacitor as bypass capacitors for this product, and mount the 0.1 µF capacitor as close as possible to the VDD pin of this product.

Since the power supply VDD and AGND voltage serve as the reference voltage for the A/D converter, any power supply fluctuation will affect the full-scale voltage and impact the characteristics. It is recommended to connect to a power supply with minimal voltage fluctuation.

The output impedance of the analog input signal source should be sufficiently low. Due to the potential difference between the analog signal and the voltage held by the sampling capacitor, the charge of the sampling capacitor may be discharged from the AGIOx pin at the moment of entering track mode from hold mode, causing voltage fluctuations at the AGIOx pin. If this effect remains until the moment of transition from track mode to hold mode, it may cause errors in the A/D conversion result.

When using a buffer amplifier to lower the output impedance, the buffer amplifier itself needs to have a high-speed response. However, by connecting a capacitor and resistor to the AGIOx pin instantaneous voltage fluctuations that the buffer amplifier cannot respond to in time can be reduced.

I/O Equivalence Circuit

Pin Name	Equivalence Circuit Diagram	Pin Name	Equivalence Circuit Diagram
AGIO0 AGIO1 AGIO2 AGIO3 AGIO4 AGIO5 AGIO6 AGIO7 AGIO8 AGIO9 AGIO10 AGIO11 AGIO12 AGIO13 AGIO14 AGIO15		SDI SCK CSB	
		SDO	

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.  
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

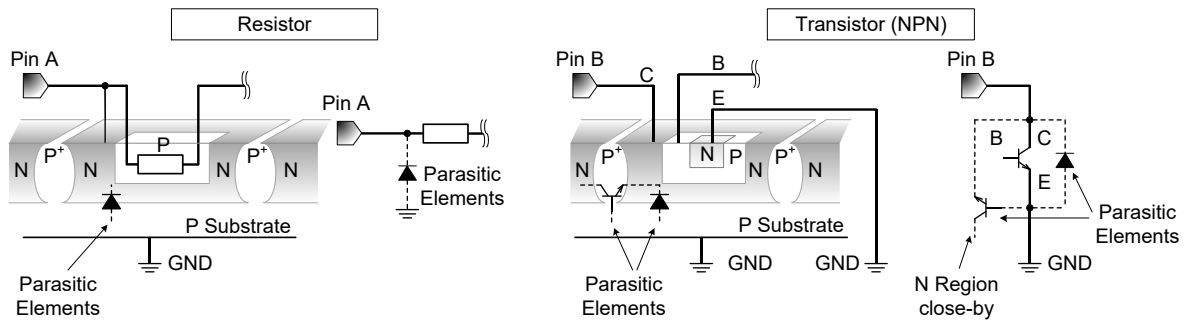
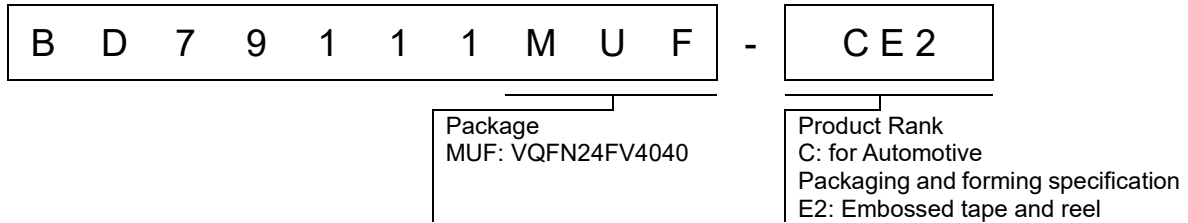


Figure 37. Example of Monolithic IC Structure

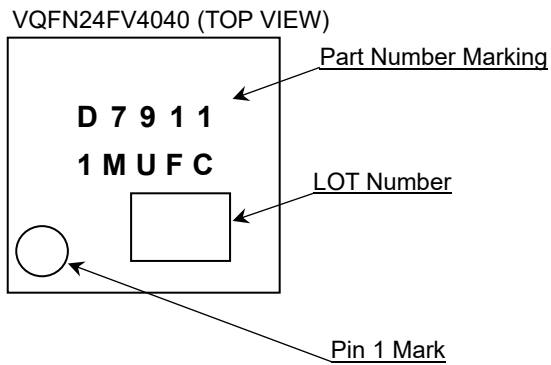
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

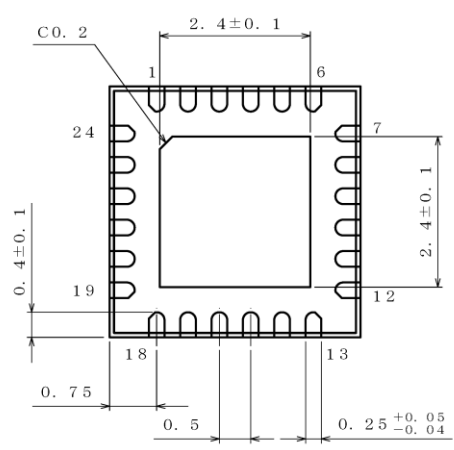
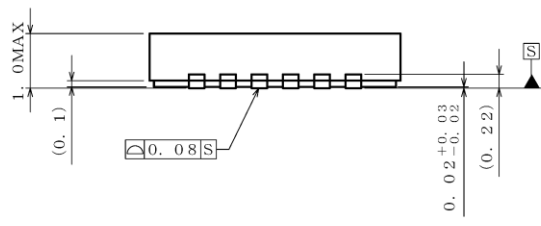
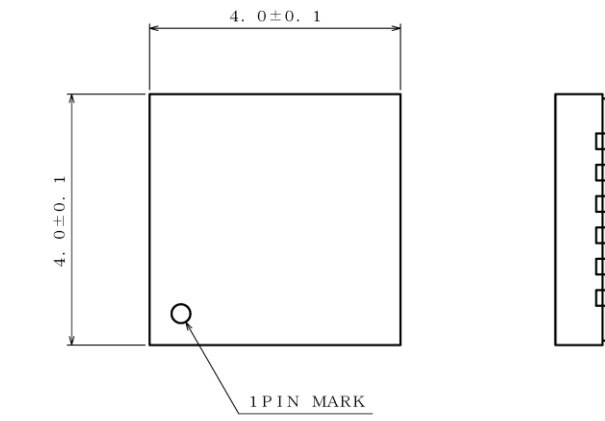


Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN24FV4040
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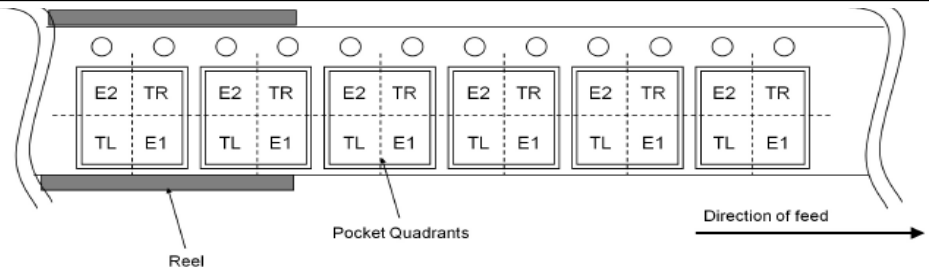
(UNIT : mm)

PKG : VQFN24FV4040  
Drawing No. EX394-5001-1

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



**Revision History**

Date	Revision	Changes
18.Mar.2026	001	New Release

# Notice

## Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment <sup>(Note 1)</sup>, aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
  - [a] Installation of protection circuits or other protective devices to improve system safety
  - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
  - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
  - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

**Precautions Regarding Application Examples and External Circuits**

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

**Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

**Precaution for Storage / Transportation**

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

**Precaution for Product Label**

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

**Precaution for Disposition**

When disposing Products please dispose them properly using an authorized industry waste company.

**Precaution for Foreign Exchange and Foreign Trade act**

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

**Precaution Regarding Intellectual Property Rights**

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.
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**Other Precaution**

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4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

**General Precaution**

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.
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