D/A Converters Series

D/A Converters
10 bit 4 channels • 6 channels Type

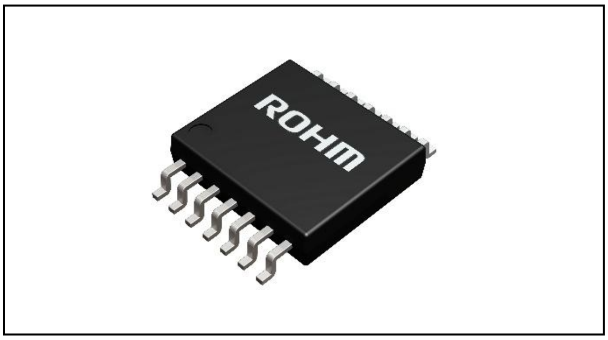
BD7971xFV-LB Series

General Description
This product is a rank product for the industrial equipment market. This is the best product for use in these applications.
BD79712FV-LB and BD79713FV-LB are 10 bit R-2R-type D/A converters with 4 and 6 channels, respectively. Optimized circuitry allows two output voltages to be supplied (3 V / 5 V). A broad power supply voltage range (2.7 V to 5.5 V) is available, providing design flexibility.

Key Specifications
- Power Source Voltage Range: 2.7 V to 5.5 V
- Current Consumption: 1.2 mA (Typ)
- Differential Non Linearity: ±0.8 LSB (Max)
- Integral Non Linearity: ±2.0 LSB (Max)
- Settling Time: 4.5 μs (Max)
- Max Data Transfer Frequency: 30 MHz (Max)
- Operating Temperature Range: -40 °C to +125 °C

Package

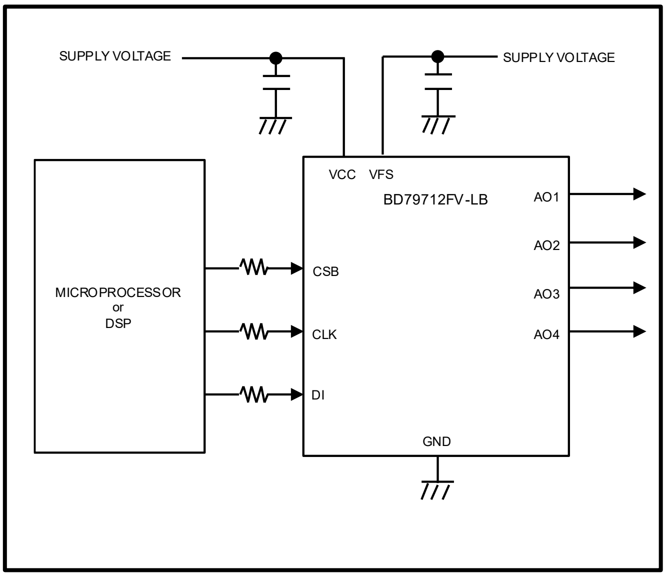
Package	W (Typ) x D (Typ) x H (Max)
SSOP-B14	5.0 mm x 6.4 mm x 1.35 mm

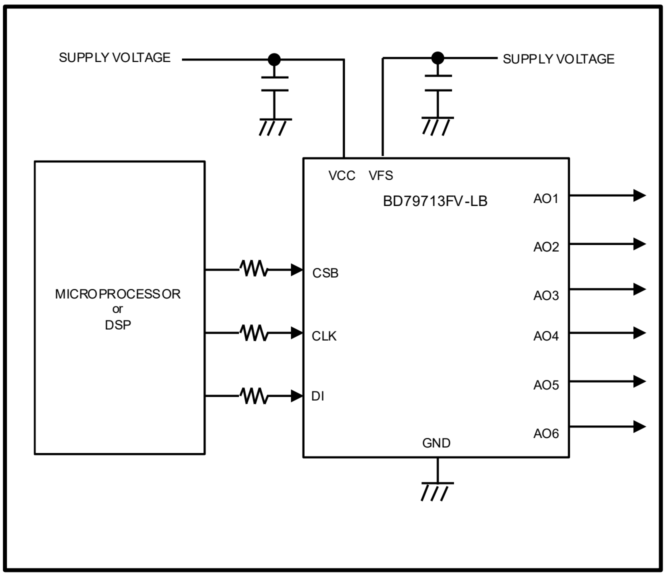


Features
- Compact Package Enabling Adjacent Placement
- Built-in Initial Zero Hold Function
- High Speed Output Response Characteristics
- 3-line Serial Interface

Applications
- Industrial Equipment
- Battery Operating Equipment
- Digital Gain Adjustment or Offset Adjustment
- Programable Voltage Source or Current Source
- Programable Attenuator

Typical Application Circuits



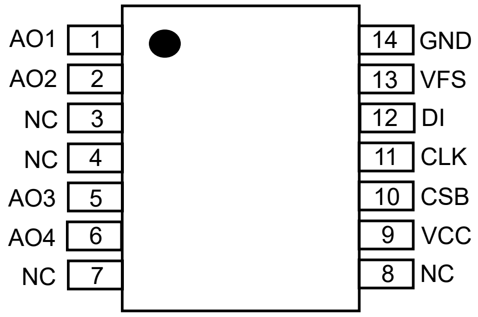


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

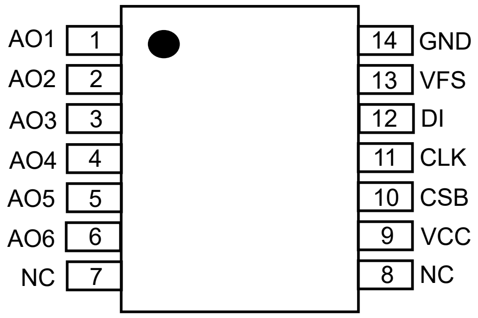
Contents

Pin Configurations

BD79712FV-LB
(TOP VIEW)



BD79713FV-LB
(TOP VIEW)



Pin Descriptions

(BD79712FV-LB)

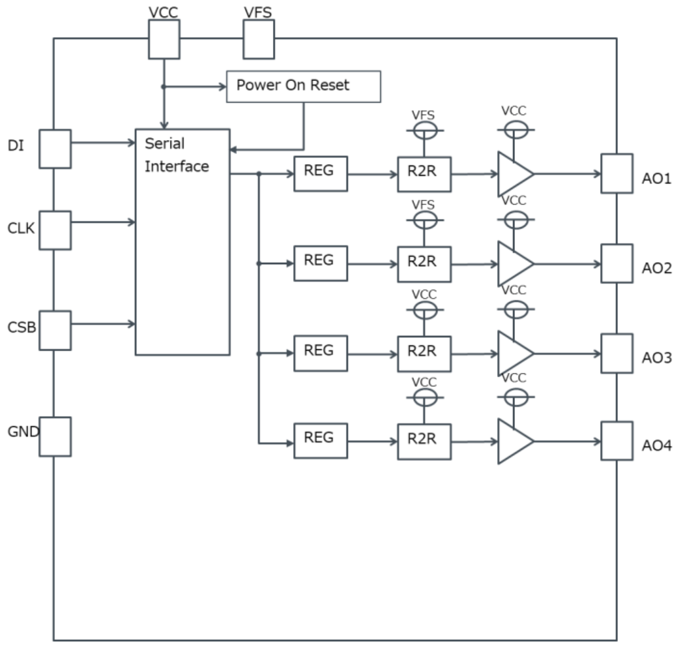
Pin No.	Pin Name	Function
1	AO1	Analog output pin 1.
2	AO2	Analog output pin 2.
3	NC	NC.
4	NC	NC.
5	AO3	Analog output pin 3.
6	AO4	Analog output pin 4.
7	NC	NC.
8	NC	NC.
9	VCC	Power supply pin.
10	CSB	Chip select input pin.
11	CLK	Digital clock input pin.
12	DI	Digital data input pin.
13	VFS	AO1, AO2 Full scale setting pin.
14	GND	Ground pin.

(BD79713FV-LB)

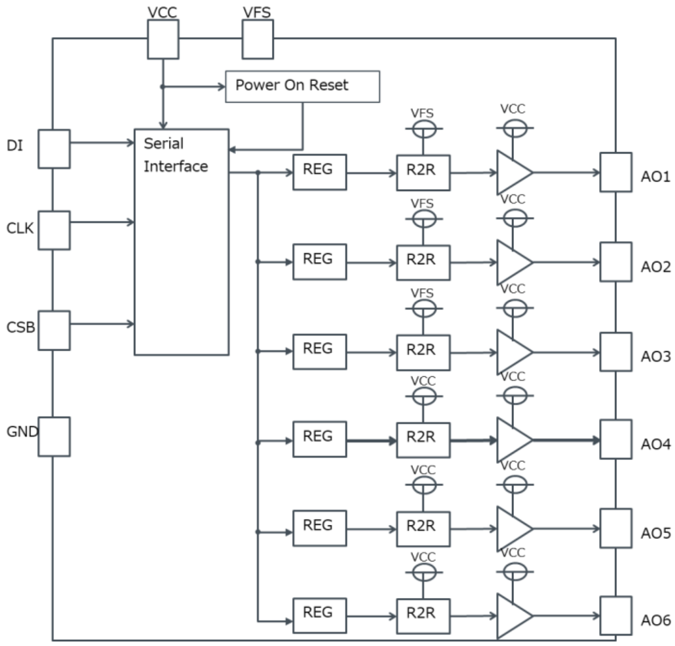
Pin No.	Pin Name	Function
1	AO1	Analog output pin 1.
2	AO2	Analog output pin 2.
3	AO3	Analog output pin 3.
4	AO4	Analog output pin 4.
5	AO5	Analog output pin 5.
6	AO6	Analog output pin 6.
7	NC	NC.
8	NC	NC.
9	VCC	Power supply pin.
10	CSB	Chip select input pin.
11	CLK	Digital clock input pin.
12	DI	Digital data input pin.
13	VFS	AO1, AO2, AO3 Full scale setting pin.
14	GND	Ground pin.

Block Diagrams

BD79712FV-LB



BD79713FV-LB



Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	4s *(Note 4)*	
SSOP-B14				
Junction to Ambient	θ_{JA}	159.6	92.8	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	13	9	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	-	5.5	V
Full Scale Voltage	V_{FS}	2.7	-	V_{CC}	V
Input Voltage	V_{IN}	0	-	V_{CC}	V
Operating Temperature	Topr	-40	+25	+125	°C
Serial Clock Frequency	f_{SCLK}	-	10	30	MHz
Load Capacitance Limit	C_L	-	-	1500	pF

Electrical Characteristics

(Unless otherwise specified V_{CC} = V_{FS} = 2.7 V to 5.5 V, Ta = 25 °C, f_{SCLK} = 30 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<Current Consumption>						
Power Down Current	I_{PD}	-	0.3	-	µA	Power Down Hi-Z, CLK = 0 V, CSB = V_{CC}, DI = V_{CC}
V_{CC} Current Consumption	I_{CC}	-	1.2	2.0	mA	7800h setting
V_{FS} Current Consumption	I_{FS}	-	0.2	0.4	mA	7800h setting
<Logic Interface>						
L Input Voltage	V_{IL}	GND	-	0.2V_{CC}	V	
H Input Voltage	V_{IH}	0.8V_{CC}	-	V_{CC}	V	
Input Current	I_{IN}	-10	-	+10	µA	
<Buffer Amplifier>						
Zero Scale Output Voltage	V_{ZSO}	-	10	-	mV	V_{CC} = 5 V, I_{OH} = 1 mA
Full Scale Output Voltage	V_{FSO}	-	V_{CC} - 0.05	-	V	V_{CC} = 5 V, I_{OL} = 1 mA
<D/A Converter Precision>						
Differential Non Linearity	DNL	-0.8	-	+0.8	LSB	Input range is 00Fh to 3F0h
Integral Non Linearity	INL	-2.0	-	+2.0	LSB	Input range is 00Fh to 3F0h
Power On Reset Release Voltage	V_{POR}	-	1.2	-	V	

Timing Specifications

(Unless otherwise specified V_{CC} = V_{FS} = 2.7 V to 5.5 V, Ta = 25 °C, f_{SCLK} = 30 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
CLK L Level Time	t_{CLKL}	10	-	-	ns	
CLK H Level Time	t_{CLKH}	10	-	-	ns	
DI Setup Time	t_{sDI}	3.5	-	-	ns	
DI Hold Time	t_{hDI}	3.5	-	-	ns	
CSB Setup Time	t_{sCSB}	10	-	-	ns	
CSB Hold Time	t_{hCSB}	10	-	-	ns	
CSB H Level Time	t_{CSBH}	10	-	-	ns	
D/A Output Settling Time	t_{OUT}	-	-	4.5	µs	C_L = 200 pF, R_L = 2 kΩ Set-up Time from 100h to 300h

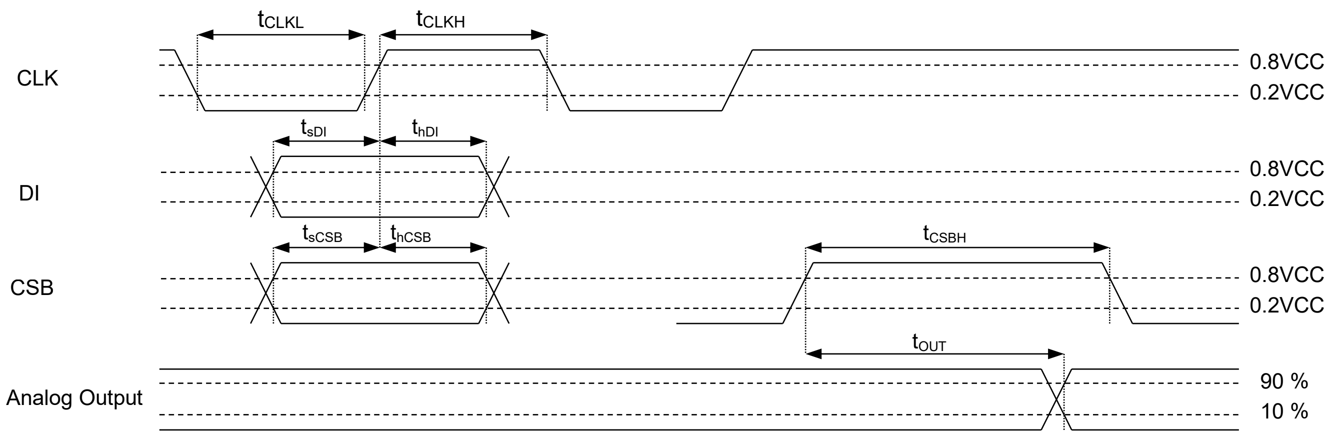


Figure 1. 3-line Serial Bus and Analog Output Timing Chart

Typical Performance Curves

(Reference Data)

Unless otherwise specified V_{CC} = V_{FS} = 3 V, Ta = 25 °C, f_{SCLK} = 30 MHz

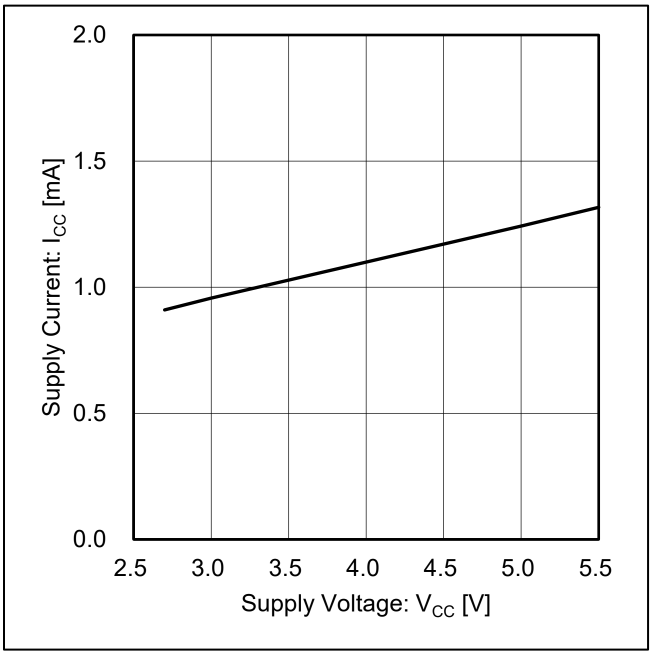


Figure 2. Supply Current vs Supply Voltage
(VCC Current Consumption)

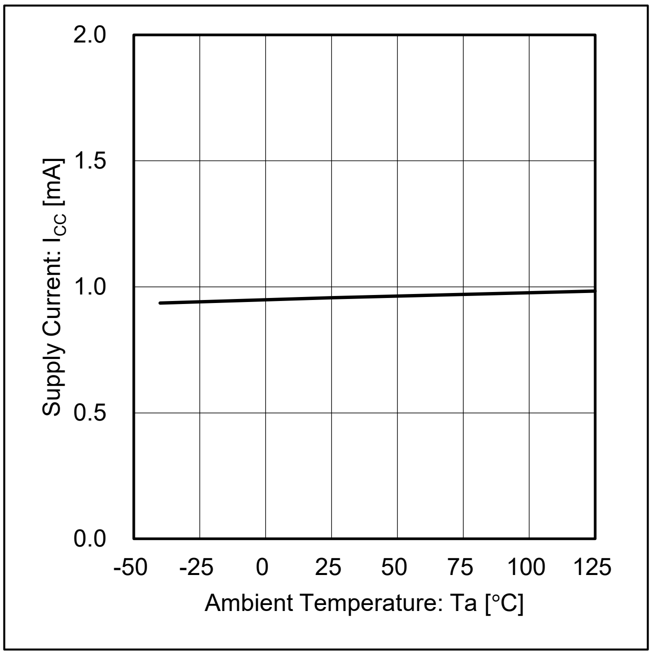


Figure 3. Supply Current vs Ambient Temperature
(VCC Current Consumption)

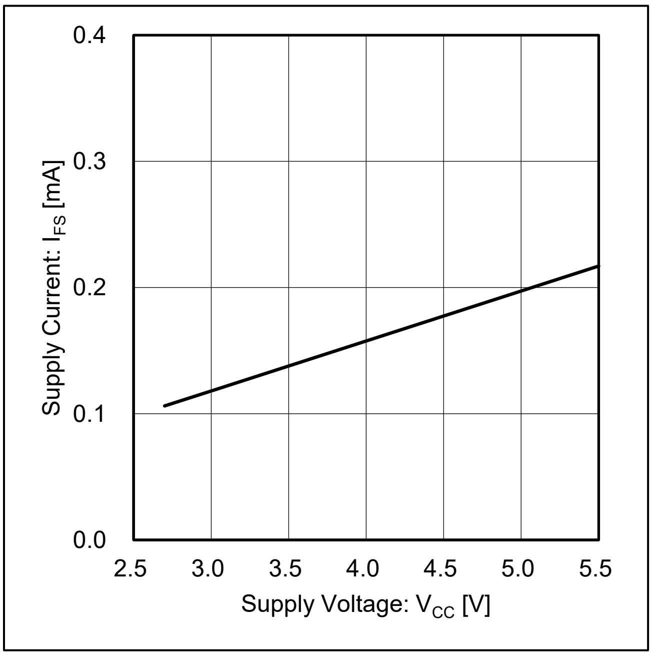


Figure 4. Supply Current vs Supply Voltage
(VFS Current Consumption)

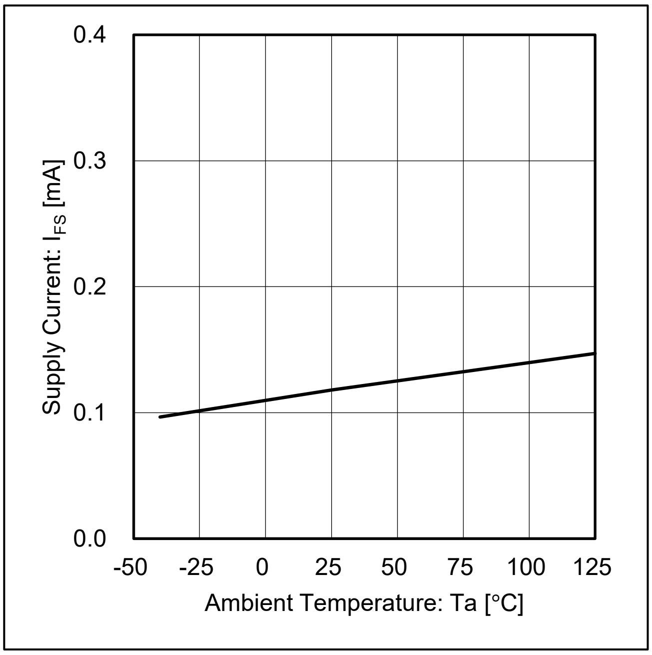


Figure 5. Supply Current vs Ambient Temperature
(VFS Current Consumption)

Typical Performance Curves – continued

(Reference Data)

Unless otherwise specified V_{CC} = V_{FS} = 3 V, Ta = 25 °C, f_{SCLK} = 30 MHz

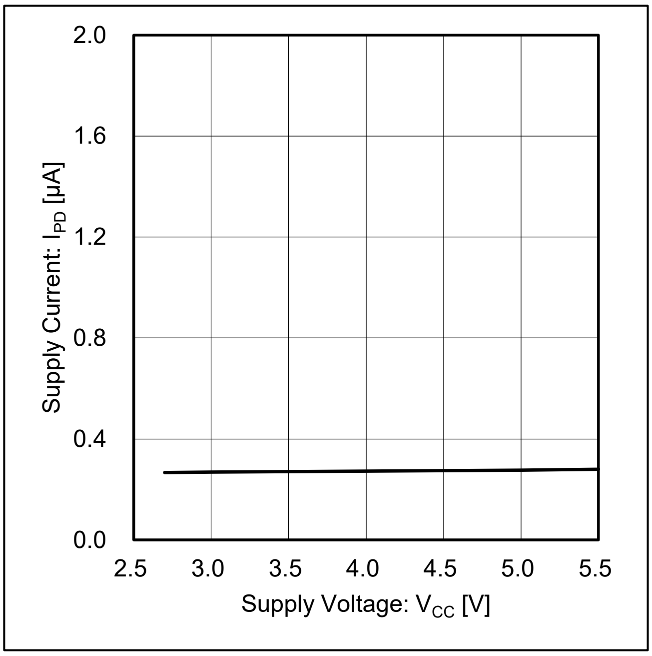


Figure 6. Supply Current vs Supply Voltage (Power Down Current)

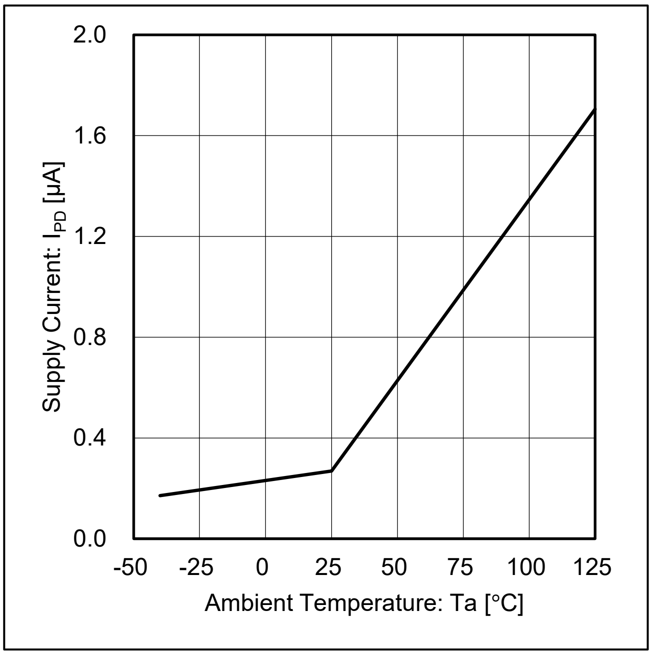


Figure 7. Supply Current vs Ambient Temperature (Power Down Current)

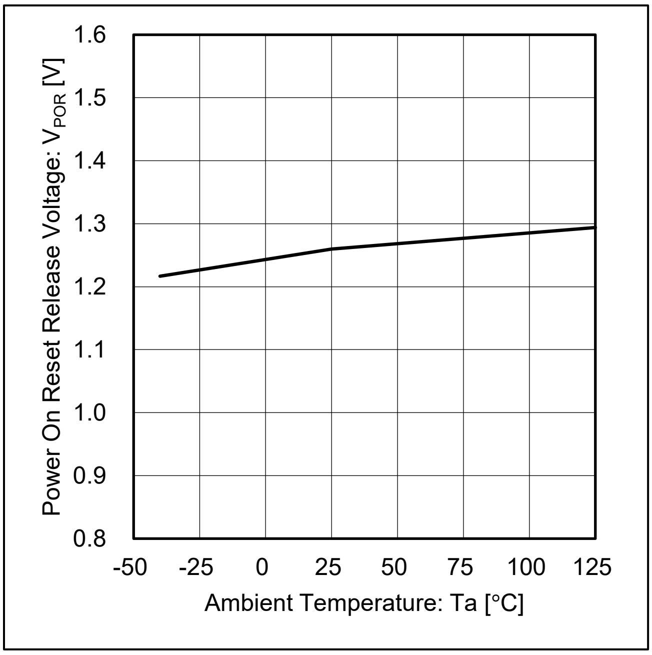


Figure 8. Power On Reset Release Voltage vs Ambient Temperature

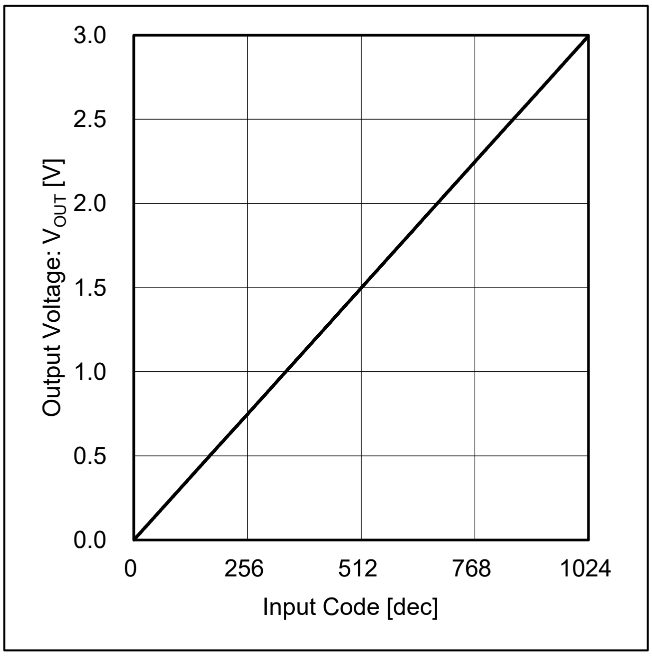


Figure 9. Output Voltage vs Input Code

Typical Performance Curves – continued

(Reference Data)

Unless otherwise specified $V_{CC} = V_{FS} = 3$ V, Ta = 25 °C, $f_{SCLK} = 30$ MHz

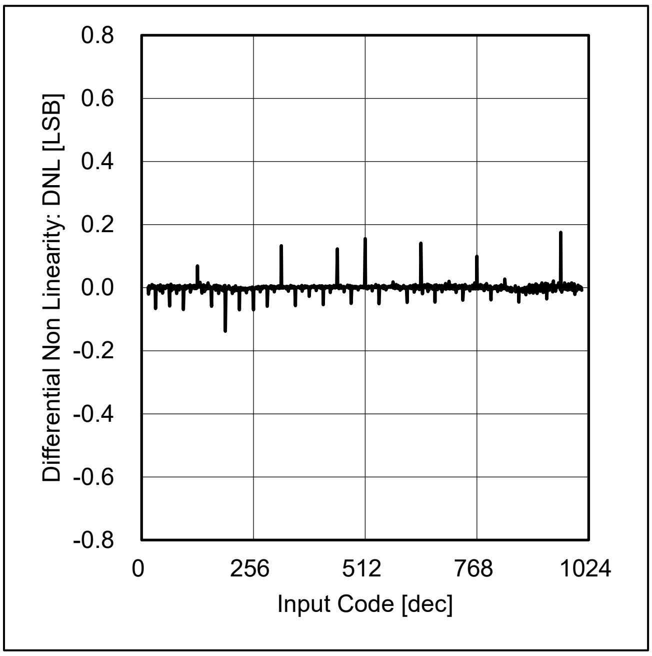


Figure 10. Differential Non Linearity vs Input Code

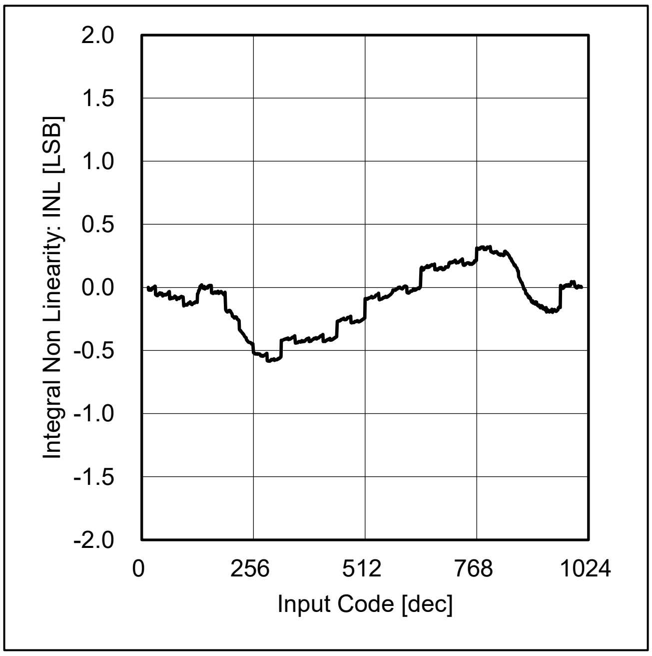


Figure 11. Integral Non Linearity vs Input Code

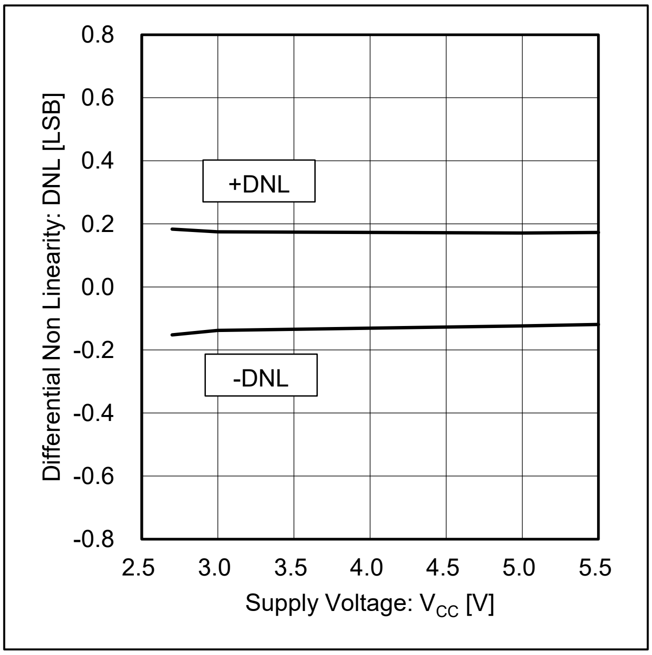


Figure 12. Differential Non Linearity vs Supply Voltage

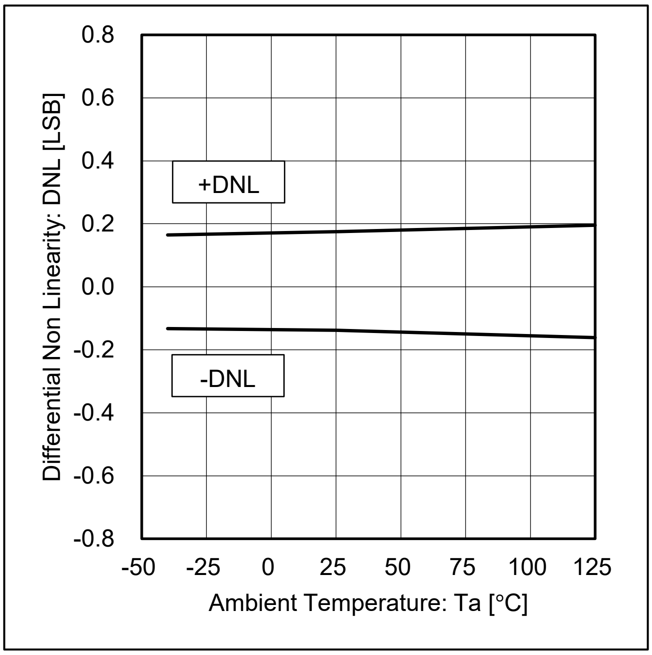


Figure 13. Differential Non Linearity vs Ambient Temperature

Typical Performance Curves – continued

(Reference Data)
Unless otherwise specified $V_{CC} = V_{FS} = 3$ V, Ta = 25 °C, $f_{SCLK} = 30$ MHz

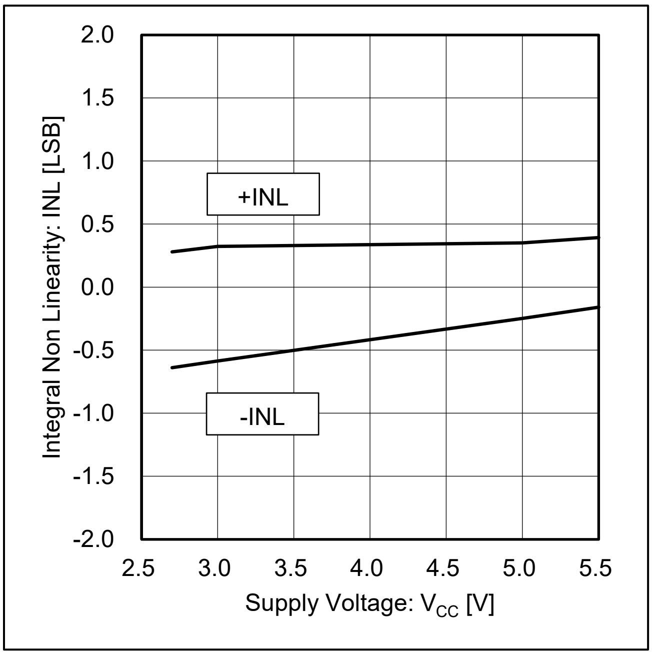


Figure 14. Integral Non Linearity
vs Supply Voltage

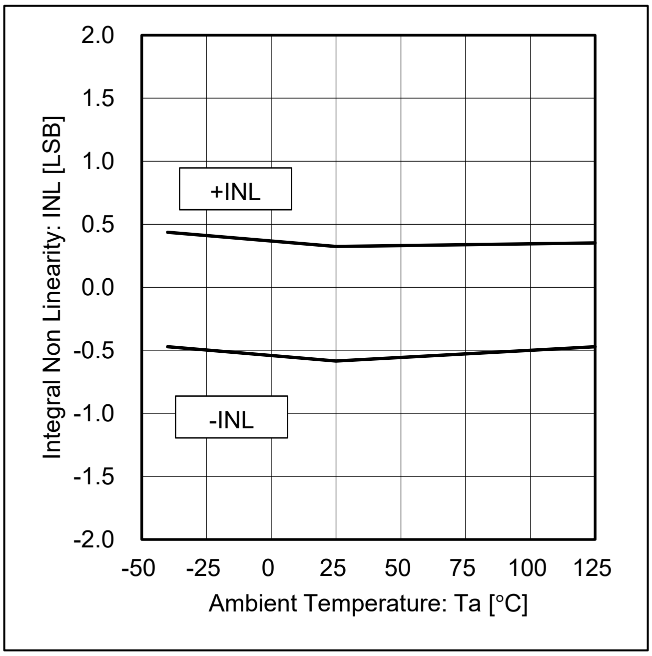


Figure 15. Integral Non Linearity
vs Ambient Temperature

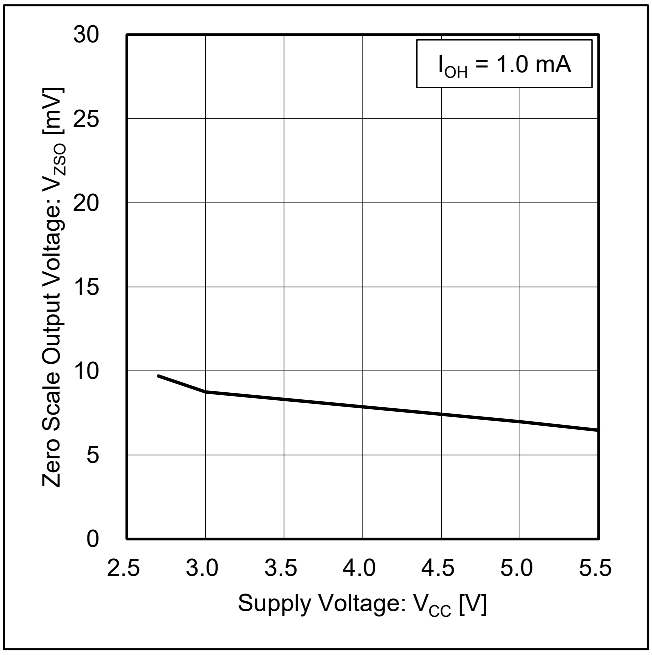


Figure 16. Zero Scale Output Voltage
vs Supply Voltage

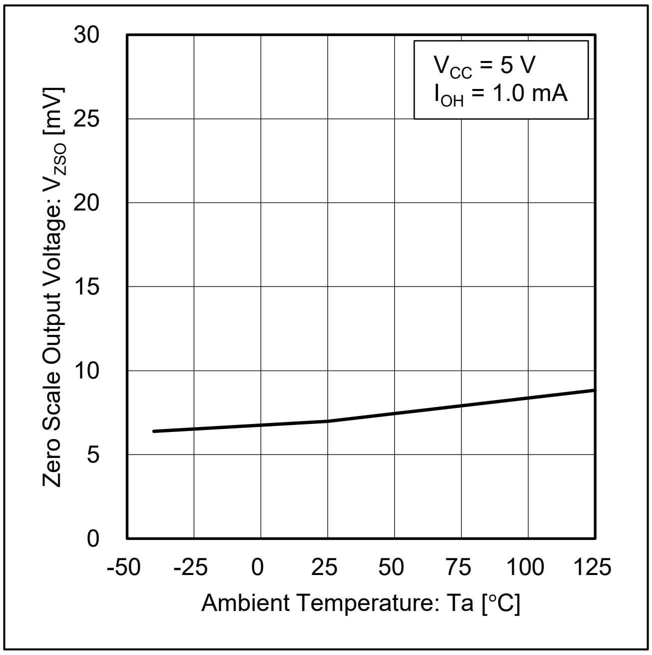


Figure 17. Zero Scale Output Voltage
vs Ambient Temperature

Typical Performance Curves – continued

(Reference Data)

Unless otherwise specified $V_{CC} = V_{FS} = 3$ V, Ta = 25 °C, $f_{SCLK} = 30$ MHz

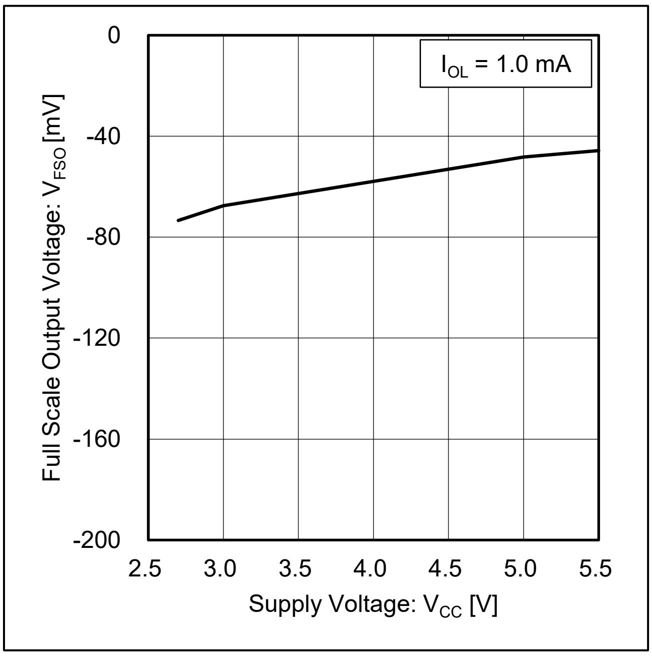


Figure 18. Full Scale Output Voltage vs Supply Voltage

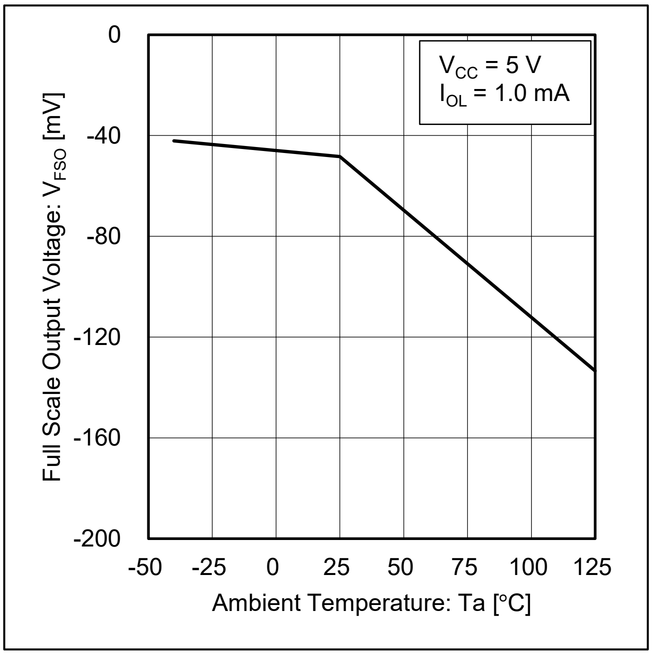


Figure 19. Full Scale Output Voltage vs Ambient Temperature

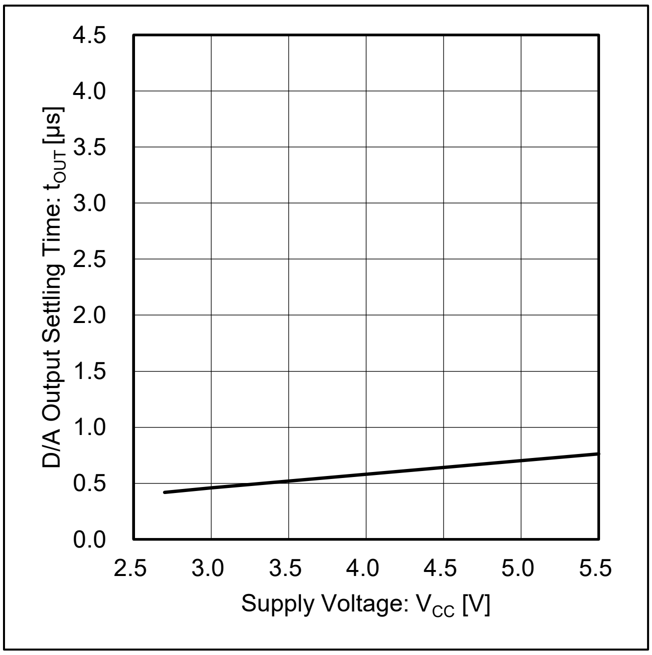


Figure 20. D/A Output Settling Time vs Supply Voltage

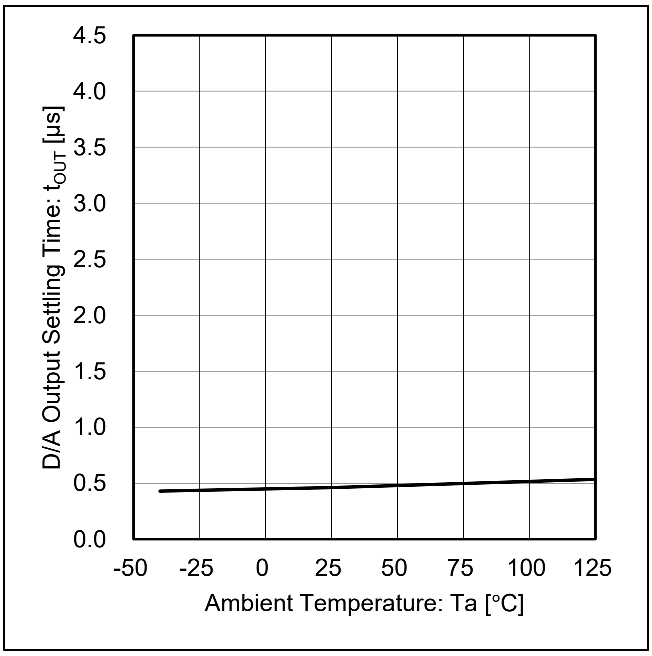


Figure 21. D/A Output Settling Time vs Ambient Temperature

Power-up Sequence

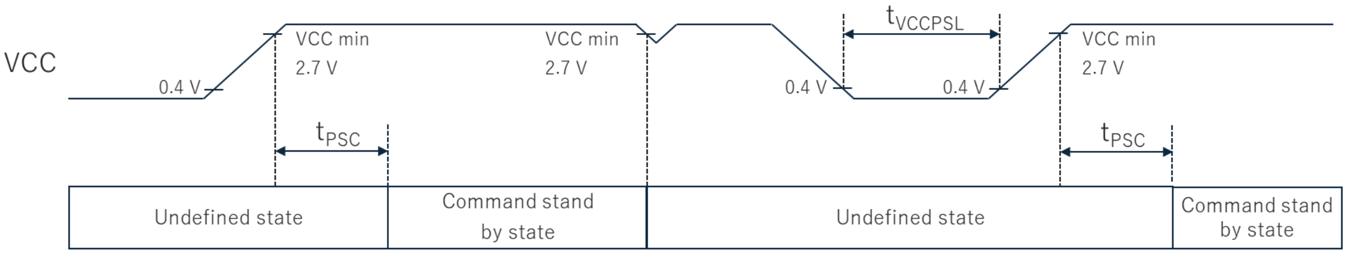


Figure 22. Power-up Timing Chart

(Unless otherwise specified Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
VCC off time	t_{VCCPSL}	1	-	-	ms
SPI command available time from Power-up	t_{PSC}	0.1	-	-	ms

After power-on, commands must be issued only after the duration of t_{PSC} has elapsed.
If the VCC supply voltage drops below the recommended operating range, the IC may enter an undefined state.
In such cases, power must be turned off completely and then reapplied.
Before applying VCC, ensure that the VCC voltage remains below 0.4 V for at least the duration of t_{VCCPSL}.

Communication Format

The Serial Control Interface is 3-line 16 bit serial interface (MSB first).
DI data is read every rising edge of the CLK.
Last 16 bits of data are latched when CSB goes HIGH.

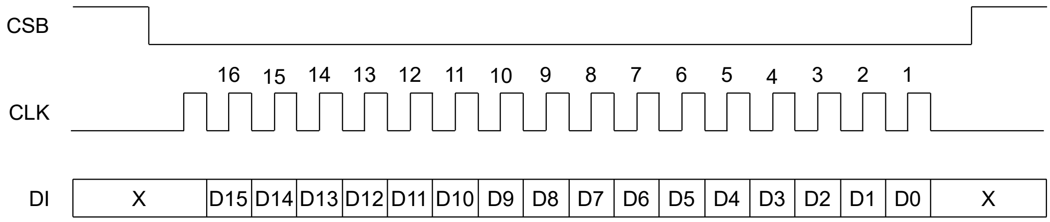


Figure 23. Communication Format

Register Map(Note 5)

Channel Setting

D15	D14	D13	D12	D11 to D2	D1	D0	BD79712FV-LB	BD79713FV-LB
0	0	0	0	00_0000_0000	0	0	Power Down 100 kΩ	Power Down 100 kΩ
0	0	0	1	D/A DATA [9:0]	0	0	AO1 Data Setting and Output	AO1 Data Setting and Output
0	0	1	0	D/A DATA [9:0]	0	0	AO2 Data Setting and Output	AO2 Data Setting and Output
0	0	1	1	D/A DATA [9:0]	0	0	Not used	AO3 Data Setting and Output
0	1	0	0	D/A DATA [9:0]	0	0	Not used	AO4 Data Setting and Output
0	1	0	1	D/A DATA [9:0]	0	0	AO3 Data Setting and Output	AO5 Data Setting and Output
0	1	1	0	D/A DATA [9:0]	0	0	AO4 Data Setting and Output	AO6 Data Setting and Output
0	1	1	1	D/A DATA [9:0]	0	0	All Channel Setting and Output	All Channel Setting and Output
1	0	0	0	00_0000_0000	0	0	Power Down 2.5 kΩ	Power Down 2.5 kΩ
1	0	0	1	D/A DATA [9:0]	0	0	AO1 Data Setting Only	AO1 Data Setting Only
1	0	1	0	D/A DATA [9:0]	0	0	AO2 Data Setting Only	AO2 Data Setting Only
1	0	1	1	D/A DATA [9:0]	0	0	Not used	AO3 Data Setting Only
1	1	0	0	D/A DATA [9:0]	0	0	Not used	AO4 Data Setting Only
1	1	0	1	D/A DATA [9:0]	0	0	AO3 Data Setting Only	AO5 Data Setting Only
1	1	1	0	D/A DATA [9:0]	0	0	AO4 Data Setting Only	AO6 Data Setting Only
1	1	1	1	00_0000_0000	0	0	Power Down Hi-Z	Power Down Hi-Z

Data Setting

D/A DATA [9:0]										Setting
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	
0	0	0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	0	0	1	(Vcc or V_{FS} - GND) /1024x1
0	0	0	0	0	0	0	0	1	0	(Vcc or V_{FS} - GND) /1024x2
0	0	0	0	0	0	0	0	1	1	(Vcc or V_{FS} - GND) /1024x3
0	0	0	0	0	0	0	1	0	0	(Vcc or V_{FS} - GND) /1024x4
1	1	1	1	1	1	1	1	1	0	(Vcc or V_{FS} - GND) /1024x1022
1	1	1	1	1	1	1	1	1	1	(Vcc or V_{FS} - GND) /1024x1023

(Note 5) Do not write '1' to the fields in which value is '0' in above table.

Resister Map – continued

BD79712FV-LB, BD79713FV-LB common

(0000h, 8000h, F000h) Power Down Enable

0000h, Power Down 100 kΩ	All channel are power down mode. Output is 100 kΩ pulldown.
8000h, Power Down 2.5 kΩ	All channel are power down mode. Output is 2.5 kΩ pulldown.
F000h, Power Down Hi-Z	All channel are power down mode. Output is Hi-Z state.

Default value 0x8000

BD79712FV-LB

(1xxxh to 7xxxh) DAC Output

1xxxh, AO1 Output	Output AO1 with setting data from D11 to D2.
2xxxh, AO2 Output	Output AO2 with setting data from D11 to D2.
3xxxh, Not used	Not used
4xxxh, Not used	Not used
5xxxh, AO3 Output	Output AO3 with setting data from D11 to D2.
6xxxh, AO4 Output	Output AO4 with setting data from D11 to D2.
7xxxh, All Channel Output	Output All channel with setting data from D11 to D2.

Default value 0x0000

(9xxxh to Exxxh) DAC Data Setting Only

9xxxh, AO1 Data Setting Only	Set AO1 DAC code with setting data from D11 to D2. Output is no changed.
Axxxh, AO2 Data Setting Only	Set AO2 DAC code with setting data from D11 to D2. Output is no changed.
Bxxxh, Not used	Not used
Cxxxh, Not used	Not used
Dxxxh, AO3 Data Setting Only	Set AO3 DAC code with setting data from D11 to D2. Output is no changed.
Exxxh, AO4 Data Setting Only	Set AO4 DAC code with setting data from D11 to D2. Output is no changed.

Default value 0x0000

BD79713FV-LB

(1xxxh to 7xxxh) DAC Output

1xxxh, AO1 Output	Output AO1 with setting data from D11 to D2.
2xxxh, AO2 Output	Output AO2 with setting data from D11 to D2.
3xxxh, AO3 Output	Output AO3 with setting data from D11 to D2.
4xxxh, AO4 Output	Output AO4 with setting data from D11 to D2.
5xxxh, AO5 Output	Output AO5 with setting data from D11 to D2.
6xxxh, AO6 Output	Output AO6 with setting data from D11 to D2.
7xxxh, All Channel Output	Output All channel with setting data from D11 to D2.

Default value 0x0000

(9xxxh to Exxxh) DAC Data Setting Only

9xxxh, AO1 Data Setting Only	Set AO1 DAC code with setting data from D11 to D2. Output is no changed.
Axxxh, AO2 Data Setting Only	Set AO2 DAC code with setting data from D11 to D2. Output is no changed.
Bxxxh, AO3 Data Setting Only	Set AO3 DAC code with setting data from D11 to D2. Output is no changed.
Cxxxh, AO4 Data Setting Only	Set AO4 DAC code with setting data from D11 to D2. Output is no changed.
Dxxxh, AO5 Data Setting Only	Set AO5 DAC code with setting data from D11 to D2. Output is no changed.
Exxxh, AO6 Data Setting Only	Set AO6 DAC code with setting data from D11 to D2. Output is no changed.

Default value 0x0000

Resister Map – continued

Example Send Command DAC Output

	Send Command	Command details	AO1	AO2
Power On	-	-	Power Down 2.5 kΩ	Power Down 2.5 kΩ
Step1	7800h	Output All channel	Output (V_{FS} - GND) /2	Output (V_{FS} - GND) /2
Step2	1FFCh	Output AO1	Output V_{FS}	Output (V_{FS} - GND) /2

Example Send Command DAC Data Setting Only

	Send Command	Command details	AO1	AO2
Power On	-	-	Power Down 2.5 kΩ	Power Down 2.5 kΩ
Step1	7800h	Output All channel	Output (V_{FS} - GND) /2	Output (V_{FS} - GND) /2
Step2	A000h	Set AO2 DAC data Output is no changed	Output (V_{FS} - GND) /2	Output (V_{FS} - GND) /2
Step3	1FFCh	Output AO1 All channel update DAC output	Output V_{FS}	Output GND

Application Example

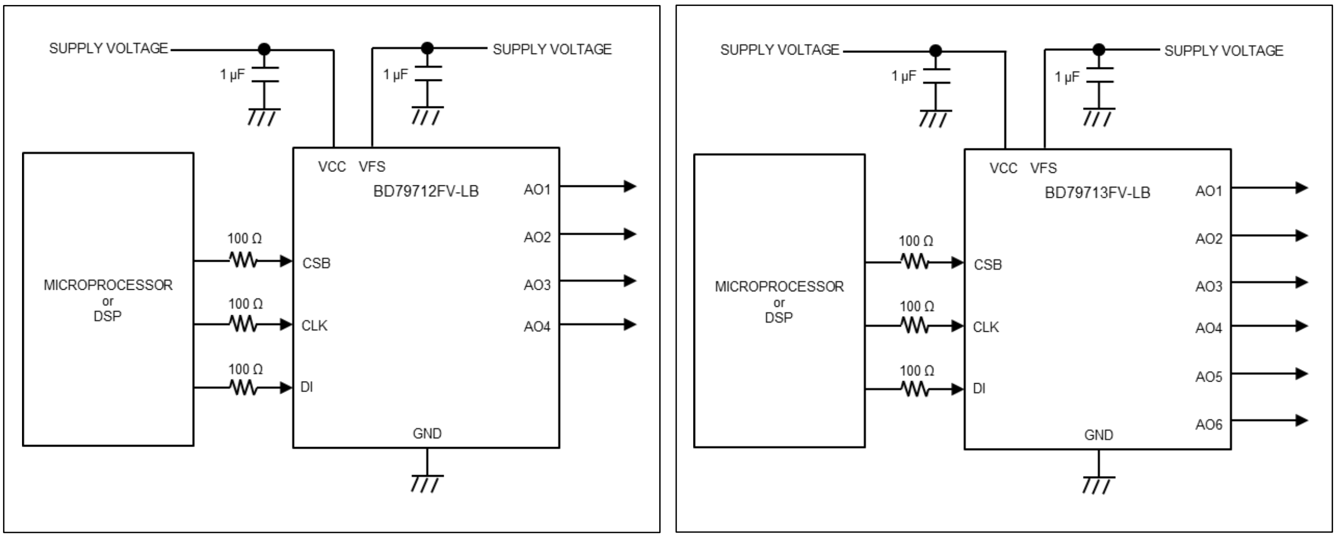
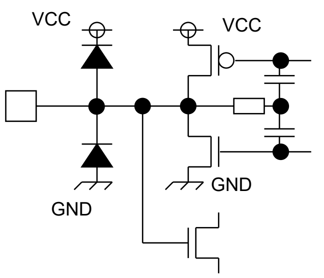
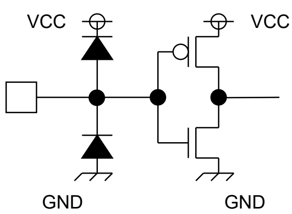
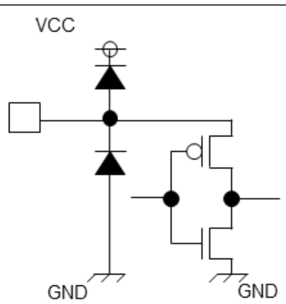


Figure 24. Application Circuit

I/O Equivalence Circuit

Pin Name	Equivalence Circuit Diagram	Pin Name	Equivalence Circuit Diagram
AO1 AO2 AO3 AO4 AO5 AO6		DI CLK CSB	
VFS			

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

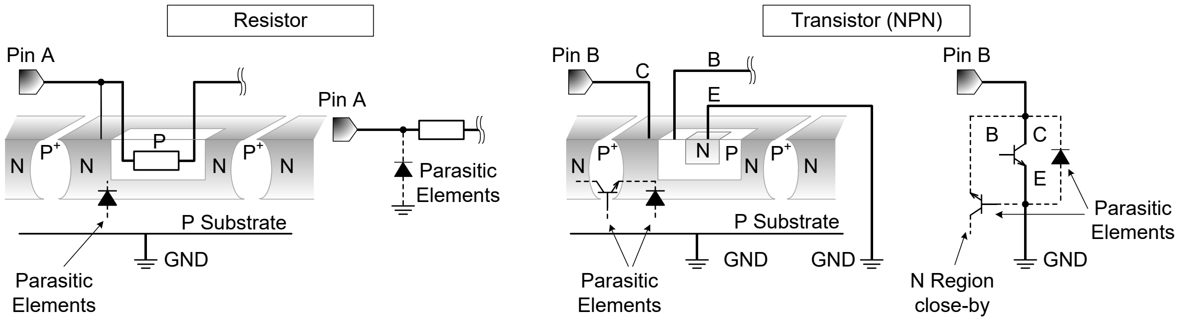


Figure 25. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B D 7 9 7 1 x F V - L B E 2

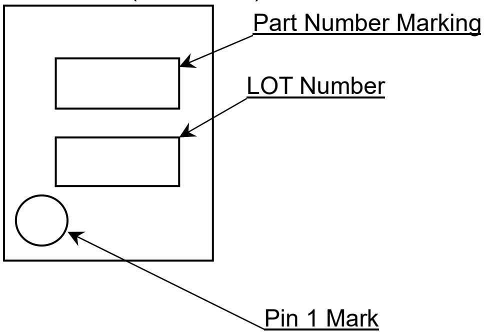
Channels
2: 4 channels
3: 6 channels

Package
FV: SSOP-B14

Product Rank
LB: for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

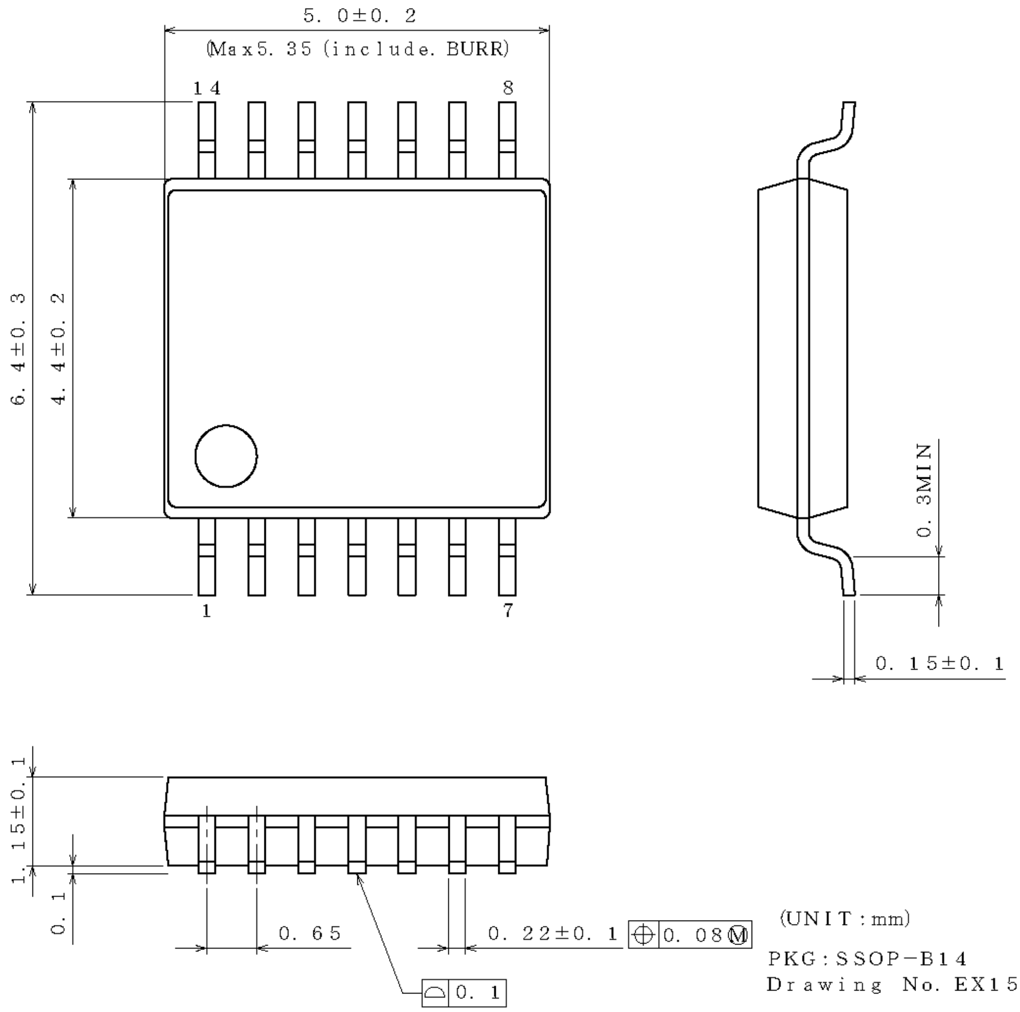
SSOP-B14 (TOP VIEW)



Part Number Marking	Package	Orderable Part Number
79712	SSOP-B14	BD79712FV-LBE2
79713		BD79713FV-LBE2

Physical Dimension and Packing Information

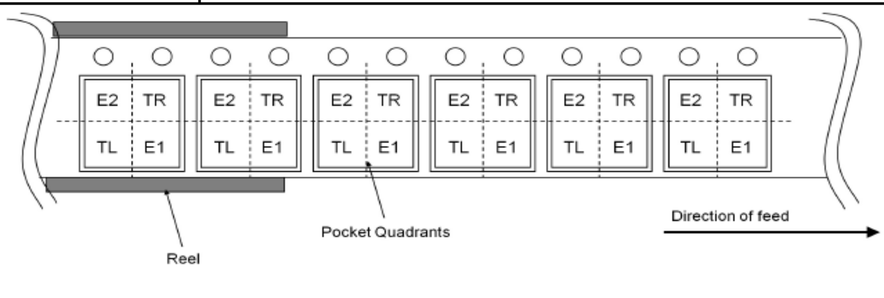
Package Name	SSOP-B14



(UNIT : mm)
PKG : SSOP-B14
Drawing No. EX152-5002

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
20.Jan.2026	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment [(Note 1)], aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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