LVDS Interface LSI

LVDS Splitter for Automotive

BU92RTF82-M

General Description

BU92RTF82-M LVDS splitter has 8 bits LVDS receiver and 8 bits LVDS transmitter, can split 56 bits (2 channels of R/G/B 24 bits and DE, HSYNC, VSYNC, Control Data) of LVDS serial data. Maximum data bit rate is 0.945 Gbps each lane. BU92RTF82-M has reduced swing mode to be able to except further low power and low EMI.
Flexible Input / Output mode is suitable for a variety of application interface.

Features

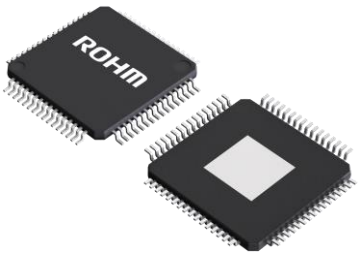
- AEC-Q100 Qualified *(Note 1)*
- LVDS Receiver Support Wide Frequency Range from 20 MHz up to 150 MHz
- LVDS Transmitter Support Wide Frequency Range from 20 MHz up to 135 MHz
- Support Reduced Swing LVDS Output for Low EMI
- Support SSCG (Spread Spectrum Clock Generator)
- Support AGING Function
- Support SPI Slave Function
- Support SPI Master Function
- Support 64Mbit External Flash Memory
- Support Internal OSC (Oscillator)
- Integrated Termination Resistor in LVDS Receiver
- Flexible Input / Output Mode
- Support Fail Detect Function
- Support CRC (Cyclic Redundancy Check) Function
- Support OSD (On-Screen Display) Gen2 Function
- Support IMC (Image Comparison) Function

(Note 1) Grade2

Key Specifications

- Supply Voltage Range: VDDIO 3.0 V to 3.6 V
  LVDSVDD 3.0 V to 3.6 V
  VDD15 1.35 V to 1.65 V
- LVDS Input Frequency 20 MHz to 150 MHz
- LVDS Output Frequency 20 MHz to 135 MHz
- Operating Temperature Range -40 °C to +105 °C

Package	W (Typ) x D (Typ) x H (Max)
HTQFP64AV	12.00 mm x 12.00 mm x 1.00 mm



Applications

- Car Navigation System
- CID (Center Information Display)
- HUD (Head Up Display)

Block Diagram

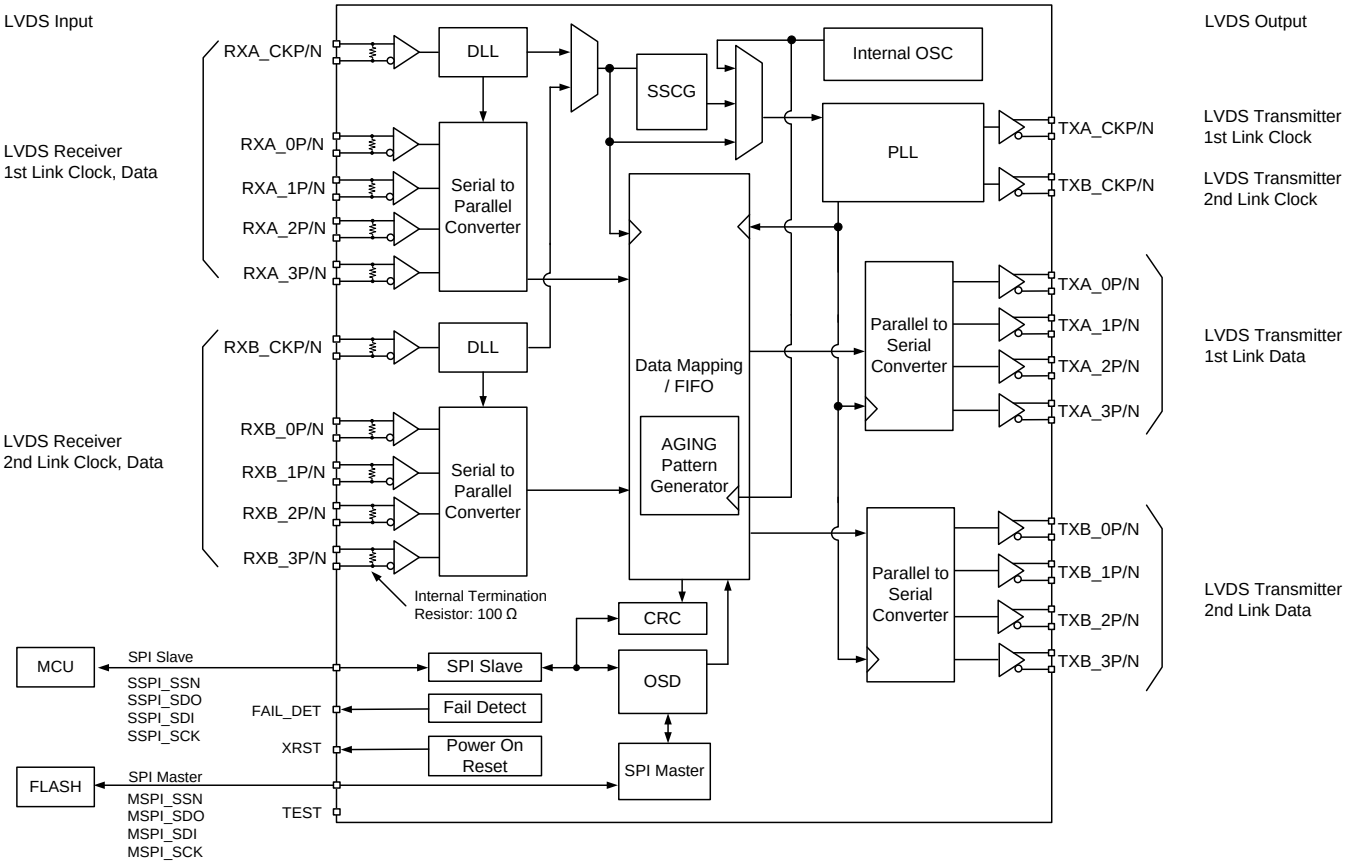


Figure 1. Block Diagram

LVDS Splitter Application Example

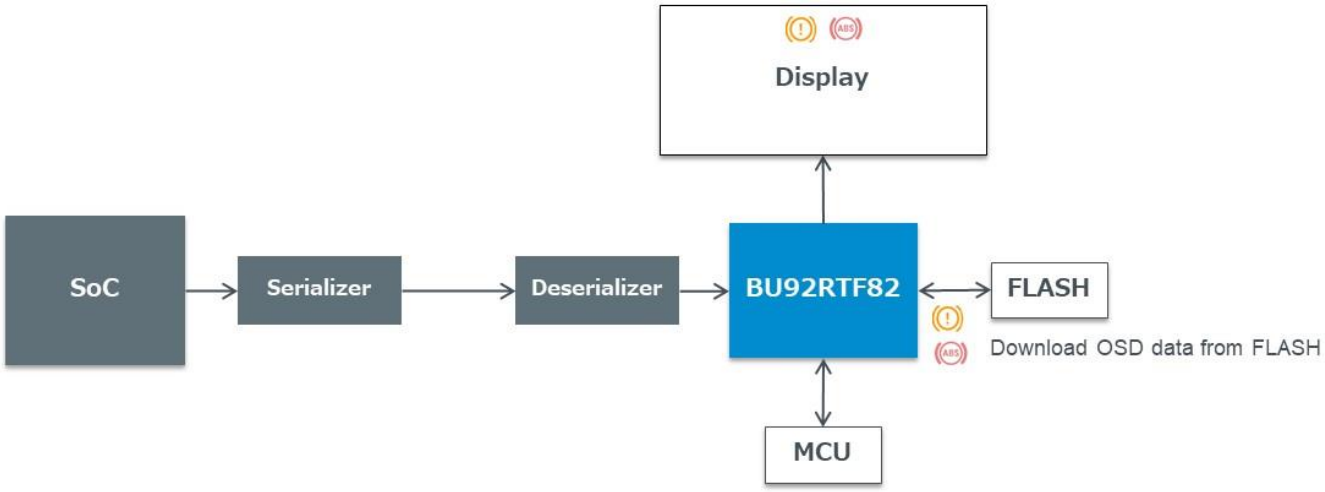


Figure 2. Application Example

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

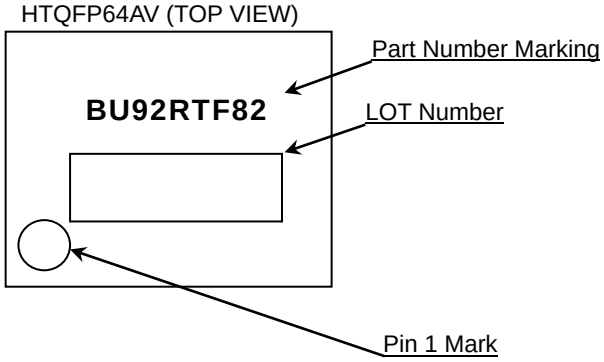
Ordering Information

B U 9 2 R T F 8 2	-	ME2

Product Rank
M: For Automotive
Packaging and Forming Specification
E2: Embossed Tape and Reel

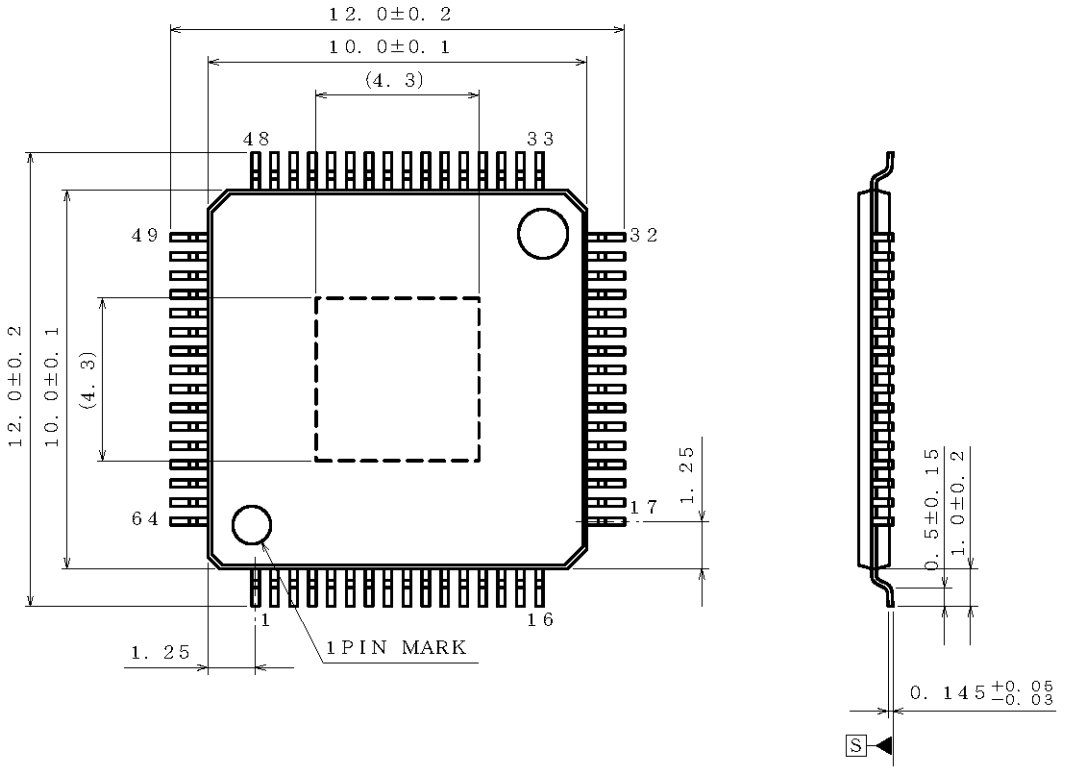
Marking Diagram

HTQFP64AV (TOP VIEW)



Physical Dimension and Packing Information

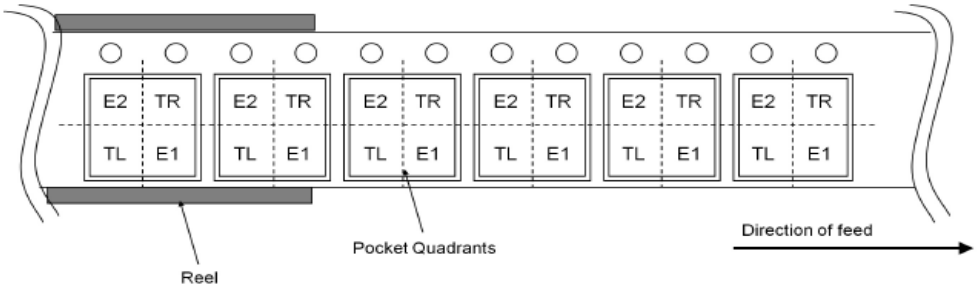
Package Name	HTQFP64AV



(UNIT : mm)
PKG : HTQFP64AV
Drawing No. EX285-5001

<Tape and Reel information>

Tape	**Embossed carrier tape (with dry pack)**
Quantity	**1000pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



Revision History

Date	Revision	Changes
20.Dec.2023	001	New Release