

General Purpose CMOS Logic IC

Automotive Quad 2-input OR gate

BD74C32FV-C

General Description

The BD74C32FV-C is a Quad 2-input OR gate and qualified for automotive applications. This is designed for 1.65 V to 5.5 V power supply voltage operation.

When it is power down, the Output Tolerant circuit protects the output circuit from the back flow current through the connected system.

Features

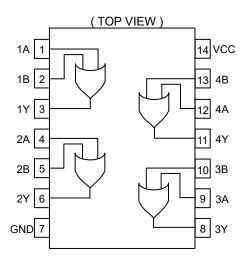
- AEC-Q100 Qualified(Note 1)
 - 4000 V Human-body Model
 - > 1000 V Charged-device Model
- Functional Safety Supportive Automotive Products
- Low Power Consumption
- 5.5 V Tolerant Inputs
- Output Tolerant Supports Partial Power Down Mode Operation

(Note 1) Grade 1

Applications

■ Automotive

Pin Configuration and Logic Diagram



Key Specifications

■ Supply Voltage Range: 1.65 V to 5.5 V

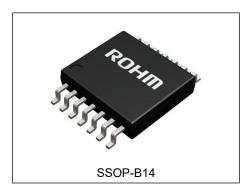
■ Low Current Consumption (Icc): 10 µA (Max)

■ Operating Temperature Range: -40 °C to +125 °C

■ Max Propagation Delay Time: 12.0 ns (@3.0 V)

■ Output Drive Capability: ±4 mA (@3.0 V)

Package SSOP-B14 **W (Typ) x D (Typ) x H (Max)** 5.0 mm x 6.4 mm x 1.35 mm



Pin Descriptions

i iii besoriptions							
Pin No.	Pin Name	Function	I/O				
1	1A	Input 1	I				
2	1B	Input 1	I				
3	1Y	Output 1	0				
4	2A	Input 2	1				
5	2B	Input 2	I				
6	2Y	Output 2	0				
7	GND	Ground	-				
8	3Y	Output 3	0				
9	3A	Input 3	I				
10	3B	Input 3	I				
11	4Y	Output 4	0				
12	4A	Input 4	I				
13	4B	Input 4	I				
14	VCC	Power Supply	-				

Truth Table

Inp	Output			
A	A B			
L	L	L		
L	Н	Н		
Н	L	Н		
Н	Н	Н		

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage Range	Vcc	-0.5 to +6.5	V
Input Voltage Range	Vin	-0.5 to +6.5	V
Input Diode Current (V _{IN} < 0)	I _{IK}	-50	mA
Output Diode Current (Vo < 0)	Іок	-50	mA
Output Current	lo	±50	mA
VCC-GND Current	lcc	±50	mA
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

Deventer	Cross book	Thermal Re	1.1		
Parameter	Symbol	1s ^(Note 3)	2s2p ^(Note 4)	Unit	
SSOP-B14					
Junction to Ambient	θ_{JA}	159.6	92.8	°C/W	
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	13	9	°C/W	

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size	Board Size		
Single	FR-4	114.3 mm x 76.2 mm x	1.57 mmt		
Тор					
Copper Pattern	Thickness				
Footprints and Traces	70 µm				
Layer Number of Measurement Board	Material	Board Size	Board Size		
4 Layers	FR-4	114.3 mm x 76.2 mm x	114.3 mm x 76.2 mm x 1.6 mmt		
Тор		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Cumply Valtage	\/	1.65	-	5.5	V	Operating
Supply Voltage	Vcc	1.5	-	5.5	V	Data Retention Only
Input Voltage	Vin	0	-	5.5	V	-
Output Voltage	Vo	0	-	Vcc	V	-
				00		V _{CC} = 1.65 V to 1.95 V
Input Transition Rise or Fall	A # / A	-	-	20	/\ /	V _{CC} = 2.3 V to 2.7 V
Rate	Δt/Δv	-	-	10	ns/V	V _{CC} = 3.0 V to 3.6 V
		-	-	5		V _{CC} = 4.5 V to 5.5 V
Operating Temperature	Topr	-40	-	+125	°C	-

(Note) The recommended operating conditions are the range where operation is guaranteed. If this ranges are exceeded, operation is not guaranteed even within the absolute maximum ratings. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

(Unless otherwise specified V_{CC} = 1.65 V to 5.5 V and Ta = -40 °C to +125 °C)

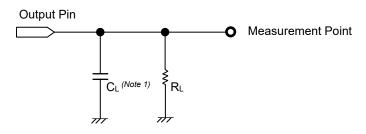
Parameter	Symbol	Min	Тур	Max	Unit	Conditions		
Farameter	Symbol	IVIIII	тур	IVIAX	Offic	Vcc		
Input "H" Voltage	V _{IH}	V _{CC} x 0.75	-	-	V	1.65 V to 1.95 V	-	
iliput H voltage	VIH	Vcc x 0.7	-	-	V	2.0 V to 5.5 V	-	
Input "I " \/oltogo	\/	-	-	Vcc x 0.25	V	1.65 V to 1.95 V	-	
Input "L" Voltage	VIL	-	-	Vcc x 0.3	V	2.0 V to 5.5 V	-	
		V _{CC} - 0.1	-	-		1.65 V to 5.5 V	Ι _{ΟΗ} = -50 μΑ	
Output "H" Voltage	Vон	2.48	-	-	V	3.0 V	I _{OH} = -4 mA	
		3.8	-	-		4.5 V	I _{OH} = -8 mA	
		-	-	0.1		1.65 V to 5.5 V	I _{OL} = 50 μA	
Output "L" Voltage	Vol	-	-	0.5	V	3.0 V	I _{OL} = 4 mA	
		-	-	0.5		4.5 V	I _{OL} = 8 mA	
Input Current	lın	-	-	±2	μΑ	0 V to 5.5 V	V _{IN} = 5.5 V or GND	
Power Off Output Pin Current	loff	-	-	10	μA	0 V	V _{IN} or V _O = 5.5 V	
Quiescent Supply Current	Icc	-	-	10	μA	1.65 V to 5.5 V	-	
Supply Current Increase	ΔΙςς	-	-	600	μA	3.0 V to 5.5 V	One Input: V _{CC} - 0.6 V Other Inputs: V _{CC} or GND	
Input Capacitance	Cı	-	4	-	pF	3.3 V	V _{IN} = V _{CC} or GND Ta = 25 °C	

Switching Characteristics

(Unless otherwise specified V_{CC} = 1.65 V to 5.5 V and Ta = -40 °C to +125 °C)

Parameter	Symbol	FROM	TO	Min	Тур	Max	Unit	Condi	tions	
Farameter	Symbol	(Input)	(Output)	itput) Mill Typ Max Offit	Vcc					
				1.4	-	15.0		1.65 V to 1.95 V	-	
Propagation	t _{PLH}	A or B	V	0.6	-	13.0	no	2.3 V to 2.7 V	-	
Delay Time	t _{PHL}	PHL	Y	0.5	-	12.0	_	3.0 V to 3.6 V	-	
				0.5	-	10.0		4.5 V to 5.5 V	-	
Power	C	-	-	-	12	-	pF	3.3 V	f = 10 MHz, Ta = 25 °C	
Dissipation Capacitance	CPD	C _{PD} -	-	-	-	15	-	pF	5.0 V	f = 10 MHz, Ta = 25 °C

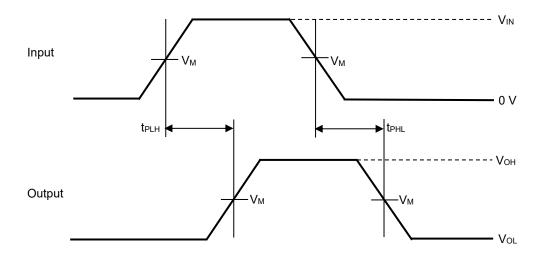
Parameter Measurement Conditions



Measurement Circuit for t_{PLH} and t_{PHL}

Vcc	VIN	V _M	C _L (Note 1)	R_L	tr/tf (Input)
1.65 V to 1.95 V	Vcc	0.5 x Vcc	30 pF	1 kΩ	≤ 2 ns
2.3 V to 2.7 V	V_{CC}	0.5 x V _{CC}	30 pF	500 Ω	≤ 2 ns
3.0 V to 3.6 V	3.0 V	1.5 V	50 pF	500 Ω	≤ 2.5 ns
4.5 V to 5.5 V	Vcc	0.5 x Vcc	50 pF	500 Ω	≤ 2.5 ns

(Note 1) C_L includes probe and test board capacitance.



Measurement Circuit and Timing Chart

Typical Performance Curves

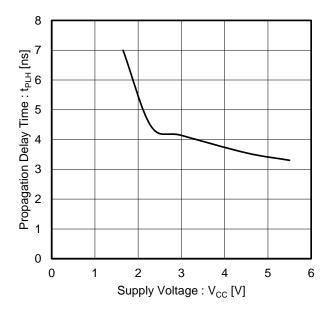


Figure 1. Propagation Delay Time: t_{PLH} vs Supply Voltage: v_{CC} (Ta = 25 °C)

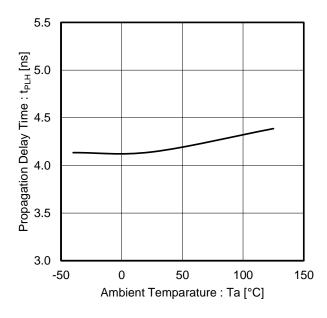


Figure 2. Propagation Delay Time: t_{PLH} vs Ambient Temperature: Ta $(V_{CC} = 3.0 \text{ V})$

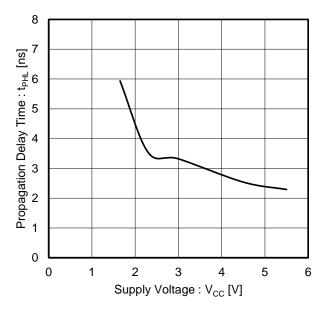


Figure 3. Propagation Delay Time: t_{PHL} vs Supply Voltage: v_{CC} (Ta = 25 °C)

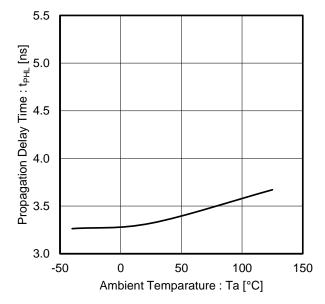


Figure 4. Propagation Delay Time: t_{PHL} vs Ambient Temperature: Ta $(V_{CC} = 3.0 \text{ V})$

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

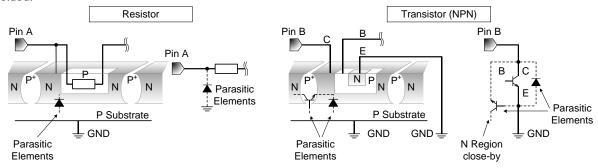


Figure 5. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

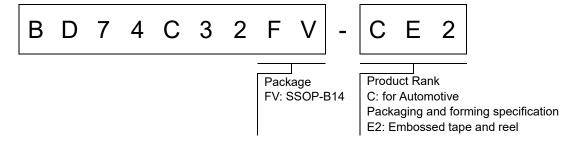
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

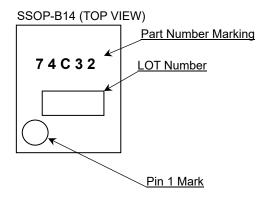
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

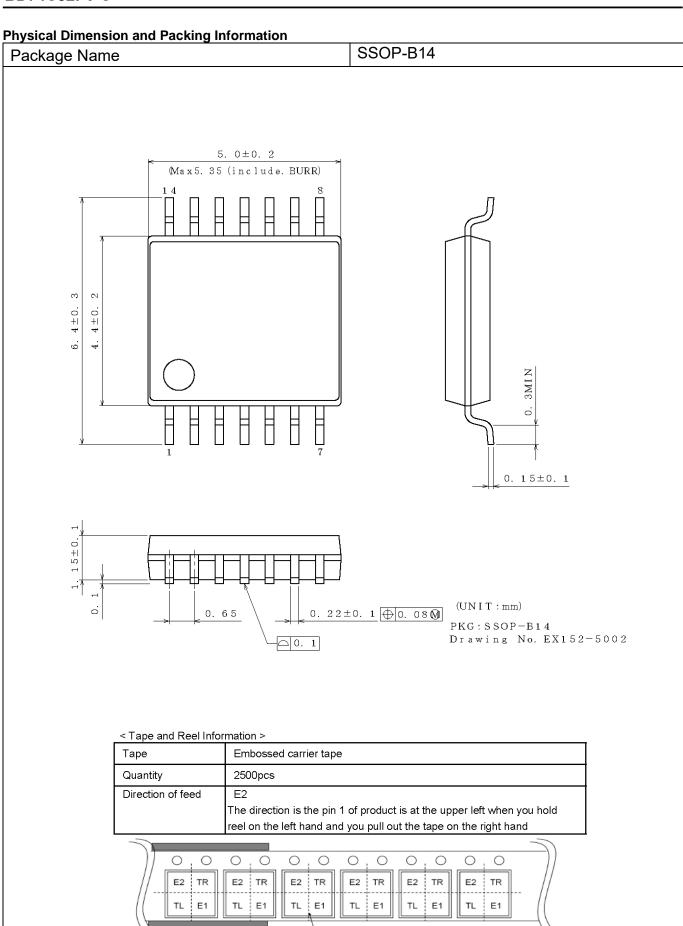
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information



Marking Diagram





Pocket Quadrants

Revision History

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Date	Revision	Changes
21.Feb.2024	001	New Release

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ſ	JÁPAN	USA	USA EU		
Ī	CLASSⅢ	CL ACCIII	CLASS II b	СГУССШ	
ſ	CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ	

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 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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