

General Purpose CMOS Logic IC

Automotive Single Buffer with Open-drain

BD7LS07G-C

General Description

The BD7LS07G-C is a Single Buffer with Open-drain and qualified for automotive applications. This is designed for 1.65 V to 5.5 V power supply voltage operation.

When it is power down, the Output Tolerant circuit protects the output circuit from the back flow current through the connected system.

Features

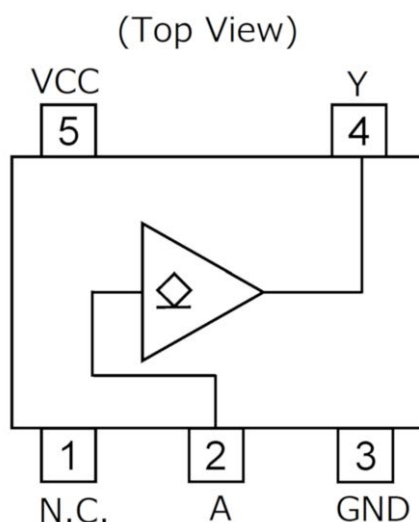
- AEC-Q100 Qualified^(Note 1)
 - 4000 V Human-body Model
 - 1000 V Charged-device Model
- Low Power Consumption
- 5.5 V Tolerant Inputs
- Output Tolerant Supports Partial Power Down Mode Operation
- Package SSOP5 is Similar to SOT-23-5(JEDEC)

(Note 1) Grade 1

Applications

- Automotive

Pin Configuration and Logic Diagram



Key Specifications

- Supply Voltage Range: 1.65 V to 5.5 V
- Low Current Consumption (I_{CC}): 10 μ A (Max)
- Operating Temperature Range: -40 °C to +125 °C
- Max Propagation Delay Time: 10.0 ns (@3.0 V)
- Output Drive Capability: \pm 24 mA (@3.0 V)

Package

SSOP5

W(Typ) x D (Typ) x H (Max)

2.9 mm x 2.8 mm x 1.25 mm



Pin Descriptions

Pin No.	Pin Name	Function	I/O
1	N.C.	No connection	-
2	A	Input	I
3	GND	Ground	-
4	Y	Output	O
5	VCC	Power supply	-

Truth Table

Input A	Output Y
L	L
H	Z

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V _{CC}	-0.5 to +6.5	V
Input Voltage Range	V _{IN}	-0.5 to +6.5	V
Input Diode Current (V _{IN} < 0)	I _{IK}	-50	mA
Output Diode Current (V _O < 0)	I _{OK}	-50	mA
Output Current	I _O	±50	mA
VCC-GND Current	I _{CC}	±50	mA
Maximum Junction Temperature	T _{jmax}	+150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
SSOP5				
Junction to Ambient	θ _{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter ^(Note 2)	ψ _{JT}	40	30	°C/W

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply Voltage	V _{CC}	1.65	-	5.5	V	Operating
		1.5	-	5.5	V	Data Retention Only
Input Voltage	V _{IN}	0	-	5.5	V	-
Output Voltage	V _O	0	-	V _{CC}	V	-
Input Transition Rise or Fall Rate	Δt/Δv	-	-	20	ns/V	V _{CC} = 1.65 V to 1.95 V
		-	-	10		V _{CC} = 2.3 V to 2.7 V
		-	-	5		V _{CC} = 3.0 V to 3.6 V
		-	-	5		V _{CC} = 4.5 V to 5.5 V
Operating Temperature	Topr	-40	-	+125	°C	-

(Note) The recommended operating conditions are the range where operation is guaranteed. If this ranges are exceeded, operation is not guaranteed even within the absolute maximum ratings. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

(Unless otherwise specified $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$ and $T_a = -40 \text{ }^\circ\text{C to } +125 \text{ }^\circ\text{C}$)

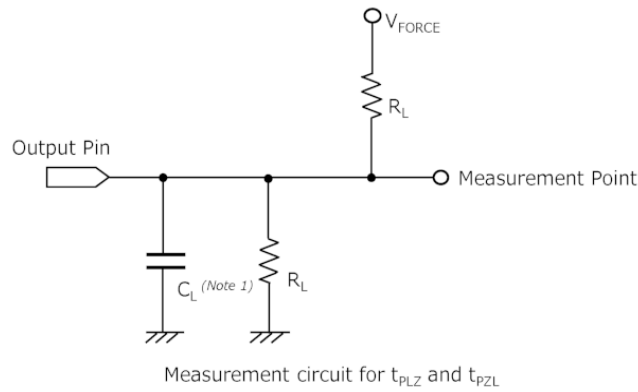
Parameter	Symbol	Min	Typ	Max	Unit	Conditions	
						V_{CC}	
Input "H" Voltage	V_{IH}	$V_{CC} \times 0.7$	-	-	V	1.65 V to 5.5 V	-
Input "L" Voltage	V_{IL}	-	-	$V_{CC} \times 0.3$	V	1.65 V to 5.5 V	-
Output "L" Voltage	V_{OL}	-	-	0.10	V	1.65 V to 5.5 V	$I_{OL} = 100 \mu\text{A}$
		-	-	0.45		1.65 V	$I_{OL} = 4 \text{ mA}$
		-	-	0.40		2.3 V	$I_{OL} = 8 \text{ mA}$
		-	-	0.60		3.0 V	$I_{OL} = 16 \text{ mA}$
		-	-	0.90		3.0 V	$I_{OL} = 24 \text{ mA}$
		-	-	1.00		4.5 V	$I_{OL} = 32 \text{ mA}$
Input Current	I_{IN}	-	-	± 2	μA	0 V to 5.5 V	$V_{IN} = 5.5 \text{ V or GND}$
Power Off Output Pin Current	I_{OFF}	-	-	10	μA	0 V	$V_{IN} \text{ or } V_O = 5.5 \text{ V}$
Off-state Output Pin Current	I_{OZ}			± 10	μA	1.65 V to 5.5 V	$V_{IN} = V_{CC}$ $V_O = V_{CC} \text{ or GND}$
Quiescent Supply Current	I_{CC}	-	-	10	μA	1.65 V to 5.5 V	-
Supply Current Increase	ΔI_{CC}	-	-	600	μA	3.0 V to 5.5 V	Input: $V_{CC} - 0.6 \text{ V}$
Input Capacitance	C_I	-	4	-	pF	3.3 V	$V_{IN} = V_{CC} \text{ or GND}$ $T_a = 25 \text{ }^\circ\text{C}$

Switching Characteristics

(Unless otherwise specified $V_{CC} = 1.65\text{ V to }5.5\text{ V}$ and $T_a = -40\text{ }^\circ\text{C to }+125\text{ }^\circ\text{C}$)

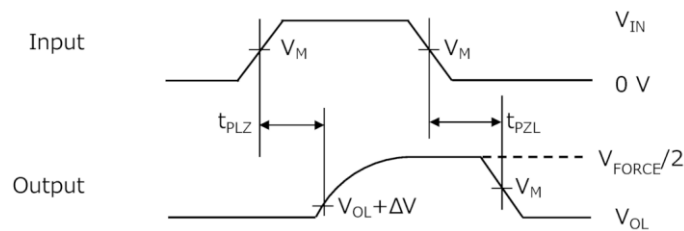
Parameter	Symbol	FROM (Input)	TO (Output)	Min	Typ	Max	Unit	Conditions	
								V_{CC}	
Propagation Delay Time	t_{PLZ} t_{PZL}	A	Y	1.0	-	12.0	ns	1.65 V to 1.95 V	-
				0.4	-	10.0		2.3 V to 2.7 V	-
				0.4	-	10.0		3.0 V to 3.6 V	-
				0.4	-	9.0		4.5 V to 5.5 V	-
Power Dissipation Capacitance	C_{PD}	-	-	-	2	-	pF	3.3 V	$f = 10\text{ MHz, } T_a = 25\text{ }^\circ\text{C}$
		-	-	-	4	-	pF	5.0 V	$f = 10\text{ MHz, } T_a = 25\text{ }^\circ\text{C}$

Parameter Measurement Conditions



V_{CC}	V_{IN}	V_M	V_{FORCE}	C_L (Note 1)	R_L	tr/tf (Inputs)	ΔV
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$2.0 \times V_{CC}$	30 pF	1k Ω	$\leq 2\text{ ns}$	0.15 V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$2.0 \times V_{CC}$	30 pF	500 Ω	$\leq 2\text{ ns}$	0.15 V
3.0 V to 3.6 V	3.0 V	1.5 V	6.0 V	50 pF	500 Ω	$\leq 2.5\text{ ns}$	0.30 V
4.5 V to 5.5 V	V_{CC}	$0.5 \times V_{CC}$	$2.0 \times V_{CC}$	50 pF	500 Ω	$\leq 2.5\text{ ns}$	0.30 V

(Note 1) C_L includes probe and test board capacitance.



Typical Performance Curves

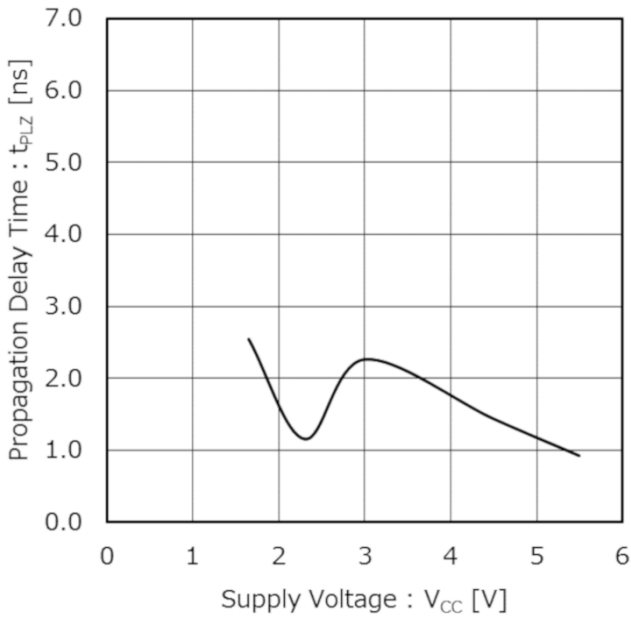


Figure 1. Propagation Delay Time: t_{PLZ} vs Supply Voltage: V_{CC}
($T_a = 25\text{ }^\circ\text{C}$)

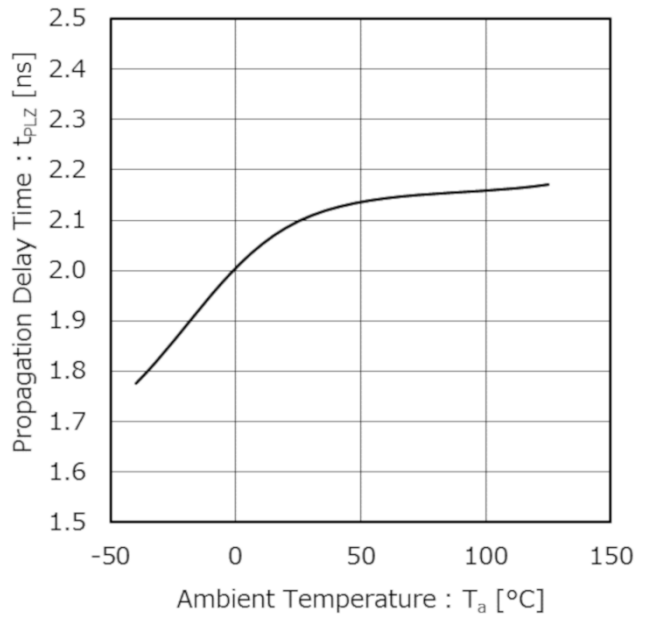


Figure 2. Propagation Delay Time: t_{PLZ} vs Ambient Temperature: T_a
($V_{CC} = 3.3\text{ V}$)

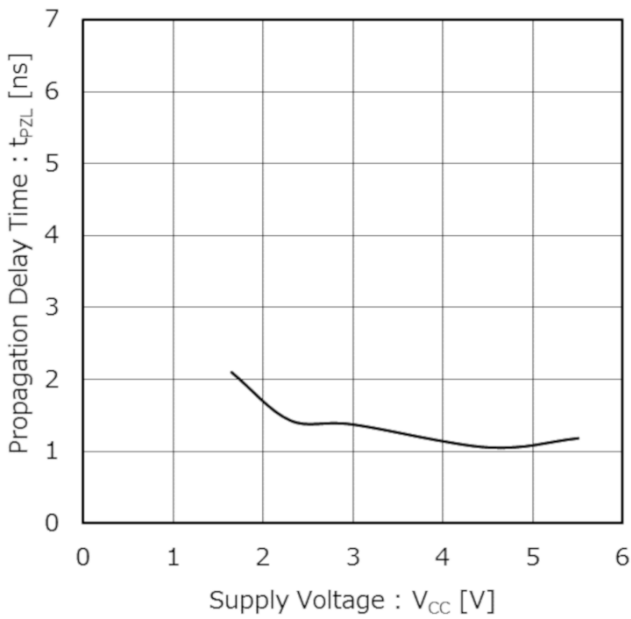


Figure 3. Propagation Delay Time: t_{PZL} vs Supply Voltage: V_{CC}
($T_a = 25\text{ }^\circ\text{C}$)

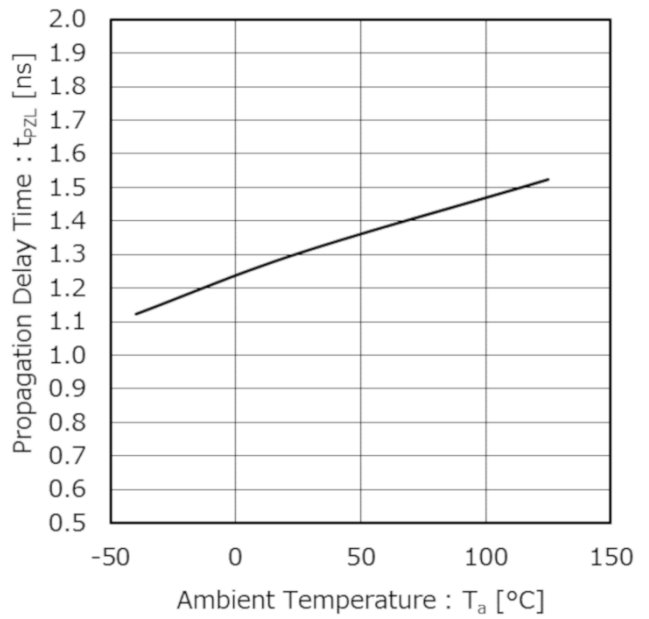


Figure 4. Propagation Delay Time: t_{PZL} vs Ambient Temperature: T_a
($V_{CC} = 3.3\text{ V}$)

Operational Notes

- 1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
- 2. Power Supply Lines**

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- 3. Ground Voltage**

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
- 4. Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
- 5. Recommended Operating Conditions**

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.
- 6. Inrush Current**

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
- 7. Operation Under Strong Electromagnetic Field**

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 8. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- 9. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
- 10. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

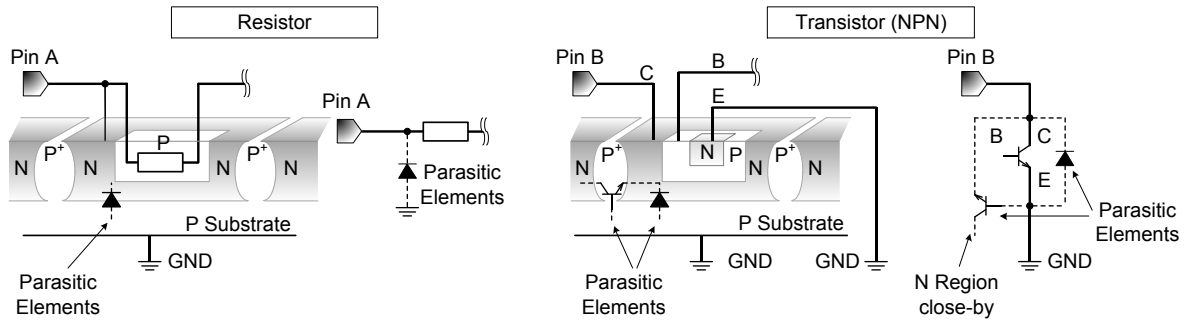
11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these



diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

Example of Monolithic IC Structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B D 7 L S 0 7 G

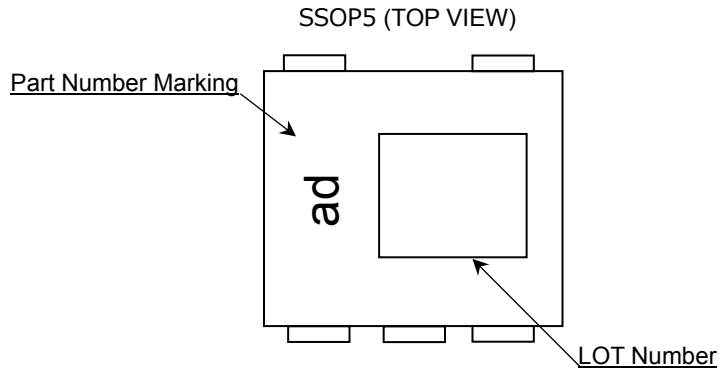
Package
G: SSOP5

-

C T L

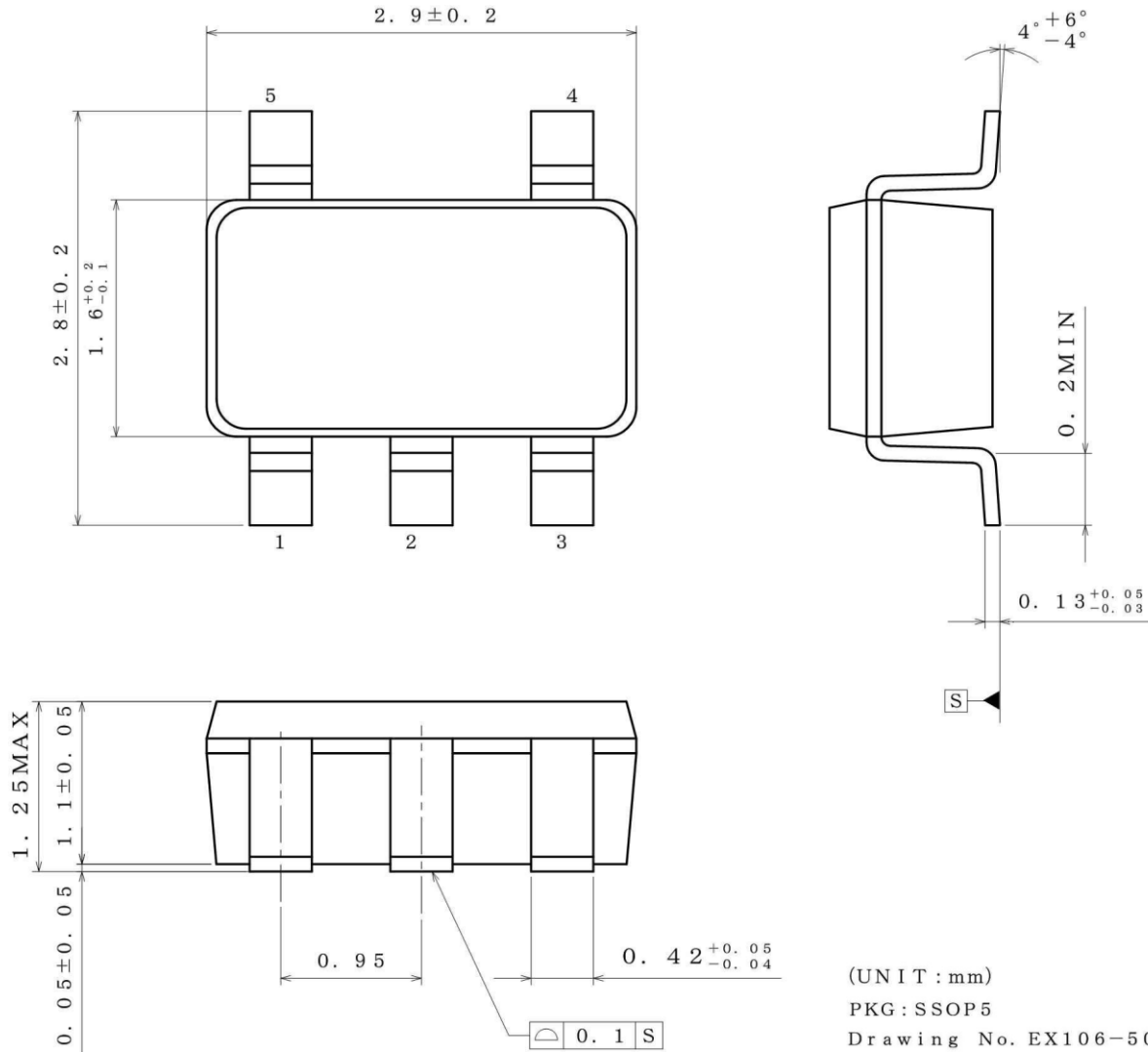
Product Rank
C: for Automotive
Packaging and forming specification
TL: Embossed tape and reel

Marking Diagram

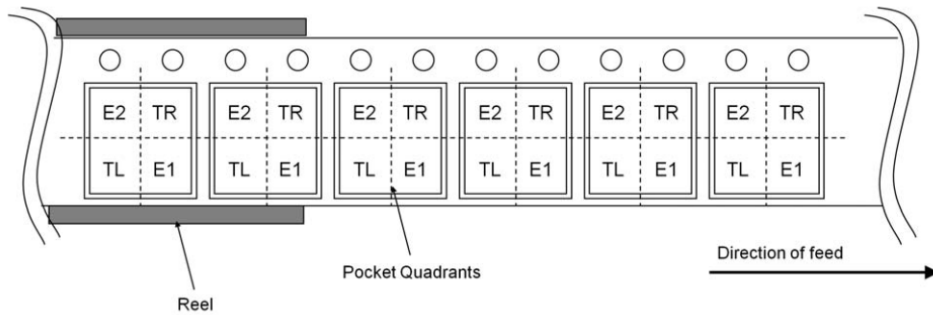


Physical Dimension and Packing Information

Package Name	SSOP5
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Packing Information	
Packing Form	Embossed carrier tape
Quantity	3000 pcs
Direction of feed	TL



Quadrant Assignments for PIN 1 Orientation in Tape
 E2 : PIN1 is placed to the top left corner. TR : PIN1 is placed to the top right corner.
 TL : PIN1 is placed to the lower left. E1 : PIN1 is placed to the lower right.

Revision History

Date	Revision	Changes
21.Apr.2020	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [h] Use of the Products in places subject to dew condensation
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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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