Serial EEPROM Series Standard EEPROM

SPI BUS EEPROM

BR25G256-3

General Description

BR25G256-3 is a 256Kbit serial EEPROM of SPI BUS interface.

Features

- High Speed Clock Action up to 20MHz (Max)
- Wait Function by HOLDB Terminal
- Part or Whole of Memory Arrays Settable as Read only Memory Area by Program
- 1.6V to 5.5V Single Power Source Operation Most Suitable for Battery Use.
- UP to 64 Byte in Page Write Mode.
- For SPI bus interface (CPOL, CPHA) = (0, 0), (1, 1)
- Self-timed Programming Cycle
- Low Current Consumption
  - At Write Action (5V) : 0.6mA (Typ)
  - At Read Action (5V) : 2.0mA (Typ)
  - At Standby Action (5V) : 0.1µA (Typ)
- Address Auto Increment Function at Read Action
- Prevention of Write Mistake
  - Write Prohibition at Power On
  - Write Prohibition by Command Code (WRDI)
  - Write Prohibition by WPB Pin
  - Write Prohibition Block Setting by Status Registers (BP1, BP0)
  - Prevention of Write Mistake at Low Voltage
- More than 100 years Data Retention.
- More than 1 Million Write Cycles.
- Bit Format 32K×8
- Initial Delivery Data
  Memory Array: FFh
  Status Register: WPEN, BP1, BP0 : 0

Packages W(Typ) x D(Typ) x H(Max)

Not Recommended for New Designs

DIP-T8
9.30mm x 6.50mm x 7.10mm

SOP- J8
4.90mm x 6.00mm x 1.65mm

SOP8
5.00mm x 6.20mm x 1.71mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

Figure 1.

○Product structure: Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	0.80 (DIP-T8(Note1))	W	When using at Ta=25°C or higher 8.0mW to be reduced per 1°C.
		0.45 (SOP8)		When using at Ta=25°C or higher 4.5mW to be reduced per 1°C.
		0.45 (SOP-J8)		When using at Ta=25°C or higher 4.5mW to be reduced per 1°C.
		0.33 (TSSOP-B8)		When using at Ta=25°C or higher 3.3mW to be reduced per 1°C.
Storage Temperature	Tstg	- 65 to +150	°C	
Operating Temperature	Topr	- 40 to +85	°C	
Input Voltage / Output Voltage	-	- 0.3 to Vcc+1.0	V	The Max value of Input Voltage/Output Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Input Voltage/Output Voltage is not under -1.0V.
Junction temperature	Tjmax	150	°C	Junction temperature at the storage condition
Electrostatic discharge voltage (human body model)	V_{ESD}	-4000 to +4000	V	

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(Note1) Not Recommended for New Designs.

Memory Cell Characteristics (Ta=25°C, Vcc=1.6V to 5.5V)

Parameter	Limits			Unit
	Min	Typ	Max	
Write Cycles (Note2)	1,000,000	-	-	Times
Data Retention (Note2)	100	-	-	Years

(Note2) Not 100% TESTED

Recommended Operating Ratings

Parameter	Symbol	Ratings		Unit
		Min	Max	
Power Source Voltage	Vcc	1.6	5.5	V
Input Voltage	V_{IN}	0	Vcc	V
Bypass Capacitor	C	0.1	-	µF

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DC Characteristics (Unless otherwise specified, Ta=-40°C to +85°C, Vcc=1.6V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input High Voltage1	V_{IH1}	0.7 x Vcc	-	Vcc+1.0	V	1.7≤Vcc≤5.5V
Input Low Voltage1	V_{IL1}	-0.3 (Note1)	-	0.3 x Vcc	V	1.7≤Vcc≤5.5V
Input High Voltage2	V_{IH2}	0.8 x Vcc	-	Vcc+1.0	V	1.6≤Vcc<1.7V
Input Low Voltage2	V_{IL2}	-0.3 (Note1)	-	0.2 x Vcc	V	1.6≤Vcc<1.7V
Output Low Voltage1	V_{OL1}	0	-	0.4	V	I_{OL}=3.0mA, 2.5≤Vcc≤5.5V
Output Low Voltage2	V_{OL2}	0	-	0.2	V	I_{OL}=1.0mA, 1.6≤Vcc<2.5V
Output High Voltage1	V_{OH1}	Vcc-0.2	-	Vcc	V	I_{OH}=-2.0mA, 2.5V≤Vcc≤5.5V
Output High Voltage2	V_{OH2}	Vcc-0.2	-	Vcc	V	I_{OH}=-400µA, 1.6≤Vcc< 2.5V
Input Leakage Current	I_{LI}	-1	-	1	µA	V_{IN}=0 to Vcc
Output Leakage Current	I_{LO}	-1	-	1	µA	V_{OUT}=0 to Vcc, CSB=Vcc
Supply Current (Write)	I_{CC1}	-	-	1	mA	Vcc=1.8V, f_{SCK}=5MHz, $t_{E/W}$=5ms Byte Write, Page Write, Write Status register
	I_{CC2}	-	-	1.5	mA	Vcc=2.5V, f_{SCK}=10MHz, $t_{E/W}$=5ms Byte Write, Page Write, Write Status register
	I_{CC3}	-	-	2	mA	Vcc=5.5V, f_{SCK}=20MHz, $t_{E/W}$=5ms Byte Write, Page Write, Write Status register
Supply Current (Read)	I_{CC4}	-	-	0.7	mA	Vcc=1.8V, f_{SCK}=5MHz, SO=OPEN Read, Read Status Register
	I_{CC5}	-	-	1	mA	Vcc=2.5V, f_{SCK}=5MHz, SO=OPEN Read, Read Status Register
	I_{CC6}	-	-	1.6	mA	Vcc=2.5V, f_{SCK}=10MHz, SO=OPEN Read, Read Status Register
	I_{CC7}	-	-	3	mA	Vcc=5.5V, f_{SCK}=5MHz, SO=OPEN Read, Read Status Register
	I_{CC8}	-	-	4	mA	Vcc=5.5V, f_{SCK}=10MHz, SO=OPEN Read, Read Status Register
	I_{CC9}	-	-	8	mA	Vcc=5.5V, f_{SCK}=20MHz, SO=OPEN Read, Read Status Register
Standby Current	I_{SB}	-	-	2	µA	Vcc=5.5V, SO=OPEN CSB=HOLDB=WPB=Vcc, SCK=SI=Vcc or GND

(Note1) When the pulse width is 50ns or less, it is -1.0V.

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AC Characteristics (Ta=-40°C to +85°C, unless otherwise specified, load capacity C_L=30pF)

Parameter	Symbol	1.6≤Vcc<1.7V			1.7≤Vcc<2.5V			2.5≤Vcc<4.5V			4.5≤Vcc≤5.5V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	.
SCK Frequency	f_{SCK}	0.01	-	3	0.01	-	5	0.01	-	10	0.01	-	20	MHz
SCK High Time	t_{SCKWH}	125	-	-	80	-	-	40	-	-	20	-	-	ns
SCK Low Time	t_{SCKWL}	125	-	-	80	-	-	40	-	-	20	-	-	ns
CSB High Time	t_{CS}	200	-	-	90	-	-	40	-	-	20	-	-	ns
CSB Setup Time	t_{CSS}	100	-	-	60	-	-	30	-	-	15	-	-	ns
CSB Hold Time	t_{CSH}	100	-	-	60	-	-	30	-	-	15	-	-	ns
SCK Setup Time	t_{SCKS}	100	-	-	50	-	-	20	-	-	15	-	-	ns
SCK Hold Time	t_{SCKH}	100	-	-	50	-	-	20	-	-	15	-	-	ns
SI Setup Time	t_{DIS}	30	-	-	20	-	-	10	-	-	5	-	-	ns
SI Hold Time	t_{DIH}	50	-	-	20	-	-	10	-	-	5	-	-	ns
Data Output Delay Time	t_{PD}	-	-	125	-	-	70	-	-	40	-	-	20	ns
Output Hold Time	t_{OH}	0	-	-	0	-	-	0	-	-	0	-	-	ns
Output Disable Time	t_{OZ}	-	-	200	-	-	80	-	-	40	-	-	20	ns
HOLDB Setting Setup Time	t_{HFS}	0	-	-	0	-	-	0	-	-	0	-	-	ns
HOLDB Setting Hold Time	t_{HFH}	100	-	-	20	-	-	10	-	-	5	-	-	ns
HOLDB Release Setup Time	t_{HRS}	0	-	-	0	-	-	0	-	-	0	-	-	ns
HOLDB Release Hold Time	t_{HRH}	100	-	-	20	-	-	10	-	-	5	-	-	ns
Time from HOLDB to Output High-Z	t_{HOZ}	-	-	100	-	-	80	-	-	40	-	-	20	ns
Time from HOLDB to Output change	t_{HPD}	-	-	100	-	-	80	-	-	40	-	-	20	ns
SCK Rise Time (Note1)	t_{RC}	-	-	2	-	-	2	-	-	2	-	-	2	µs
SCK Fall Time (Note1)	t_{FC}	-	-	2	-	-	2	-	-	2	-	-	2	µs
OUTPUT Rise Time (Note1)	t_{RO}	-	-	100	-	-	50	-	-	40	-	-	20	ns
OUTPUT Fall Time (Note1)	t_{FO}	-	-	100	-	-	50	-	-	40	-	-	20	ns
Write Cycle Time	$t_{E/W}$	-	-	5	-	-	5	-	-	5	-	-	5	ms

(Note1) NOT 100% TESTED

AC Timing Characteristics Conditions

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Load Capacity	C_L	-	-	30	pF
Input Voltage	-	0.2Vcc/0.8Vcc			V
Input / Output Judgment Voltage	-	0.3Vcc/0.7Vcc			V

Input / Output Capacity (Ta=25°C, frequency=5MHz)

Parameter	Symbol	Min	Max	Unit	Conditions
Input Capacity (Note1)	C_{IN}	-	8	pF	V_{IN}=GND
Output Capacity (Note1)	C_{OUT}	-	8		V_{OUT}=GND

(Note1) Not 100% TESTED.

Serial Data Input / Output Timing

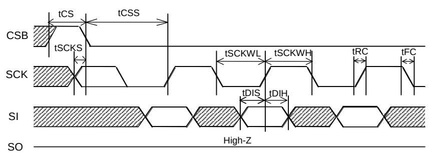

Figure 2-(a). Input timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB

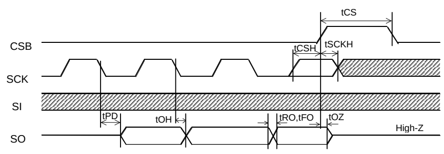

Figure 2-(b). Input / Output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

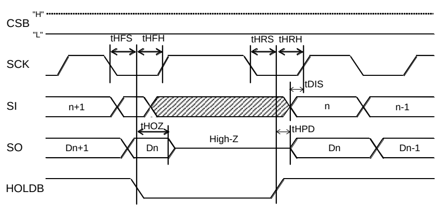

Figure 2-(c). HOLD timing

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Block Diagram

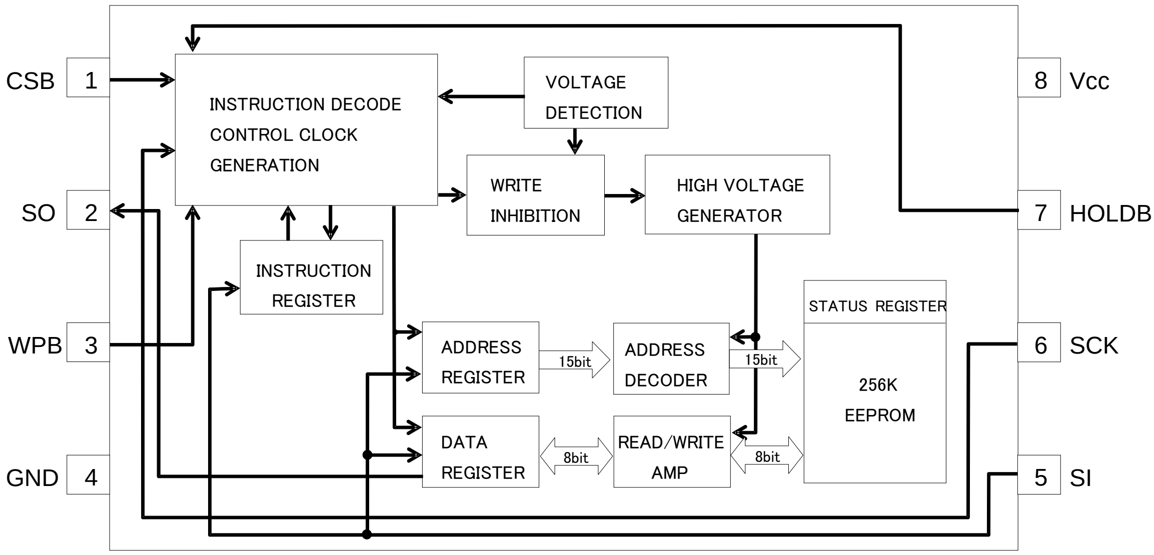

Figure 3. Block Diagram

Pin Configuration

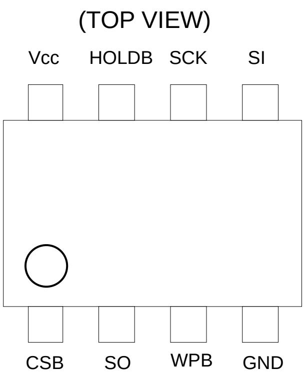

Figure 4. Pin Configuration

Pin Descriptions

Terminal name	Input /Output	Function
Vcc	-	Power source to be connected
GND	-	All input / output reference voltage, 0V
CSB	Input	Chip select input
SCK	Input	Serial clock input
SI	Input	Ope code, address, and serial data input
SO	Output	Serial data output
HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
WPB	Input	Write protect input Write status register command is prohibited

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Typical Performance Curves

(The following characteristic data are Typ Values.)

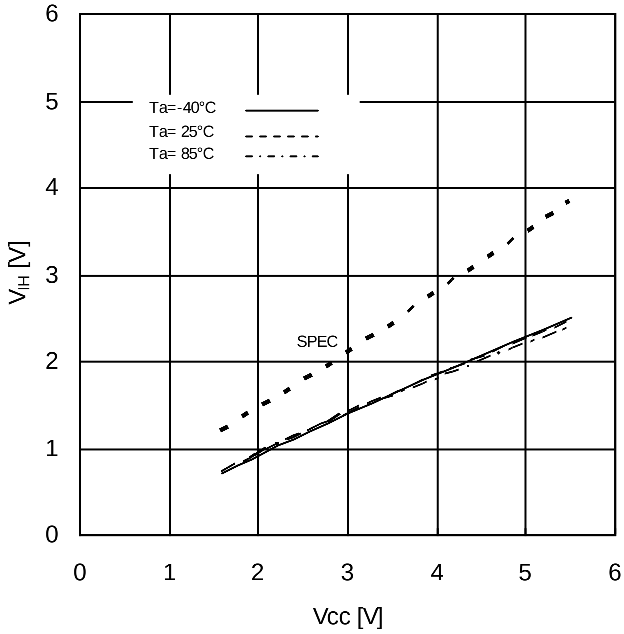

Figure 5. Input High Voltage1,2 vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

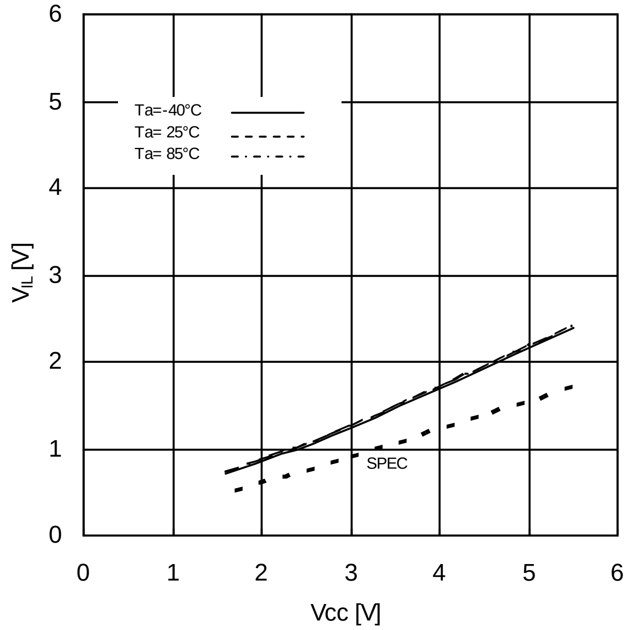

Figure 6. Input Low Voltage1,2 vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

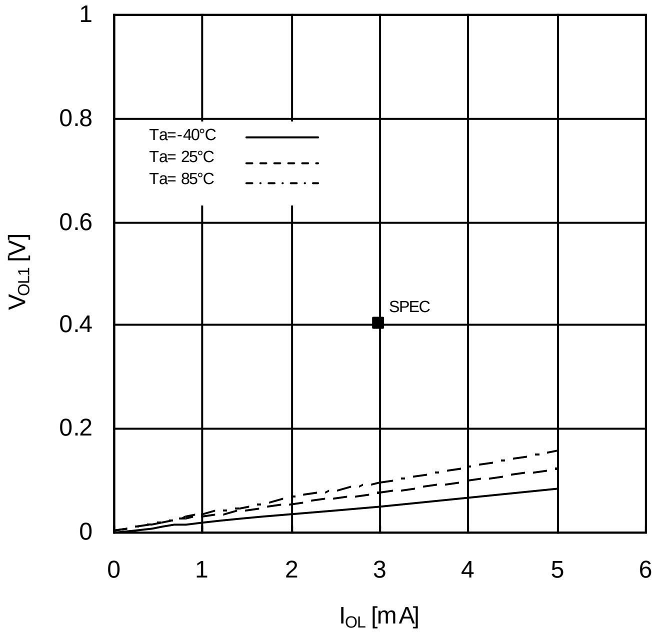

Figure 7. Output Low Voltage1 vs Output Current (Vcc=2.5V)

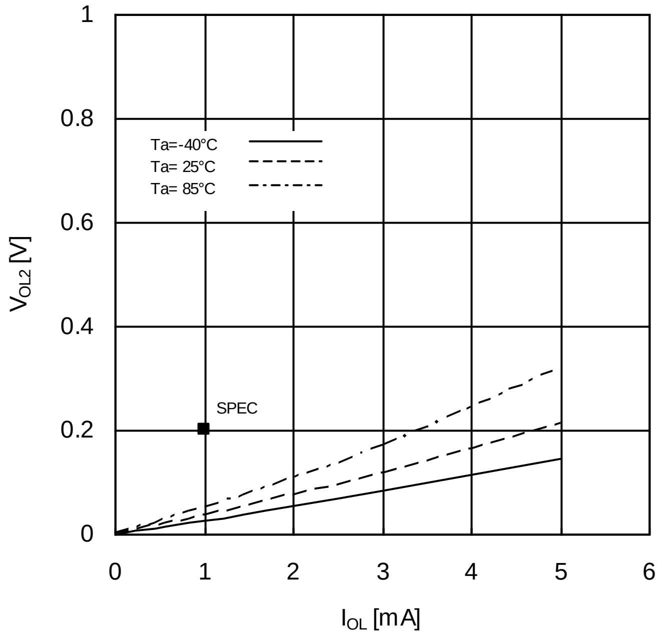

Figure 8. Output Low Voltage2 vs Output Current (Vcc=1.6V)

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Typical Performance Curves - Continued

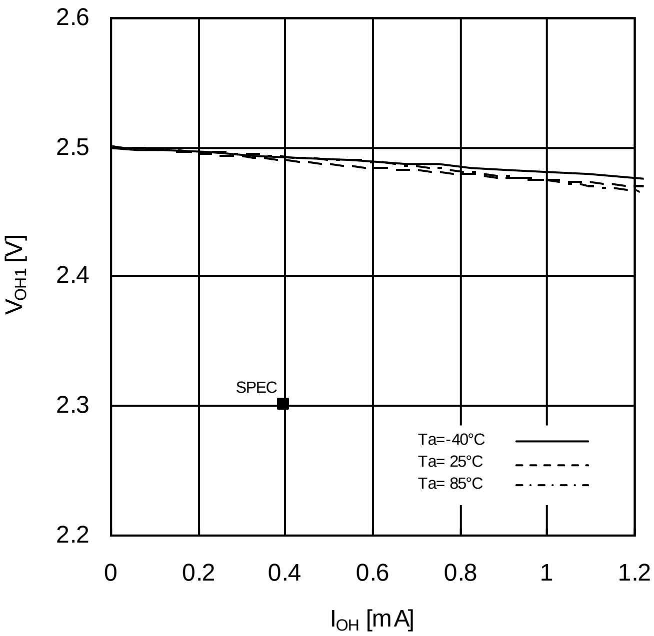

Figure 9. Output High Voltage1 vs Output Current (Vcc=2.5V)

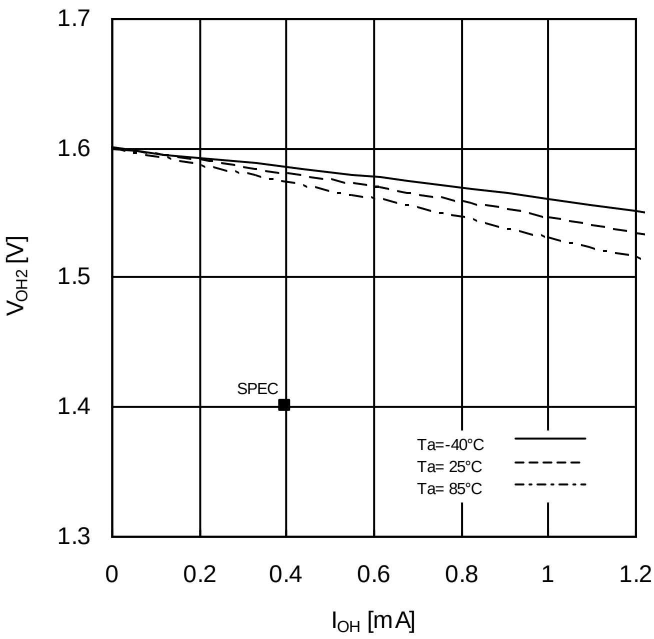

Figure 10. Output High Voltage2 vs Output Current (Vcc=1.6V)

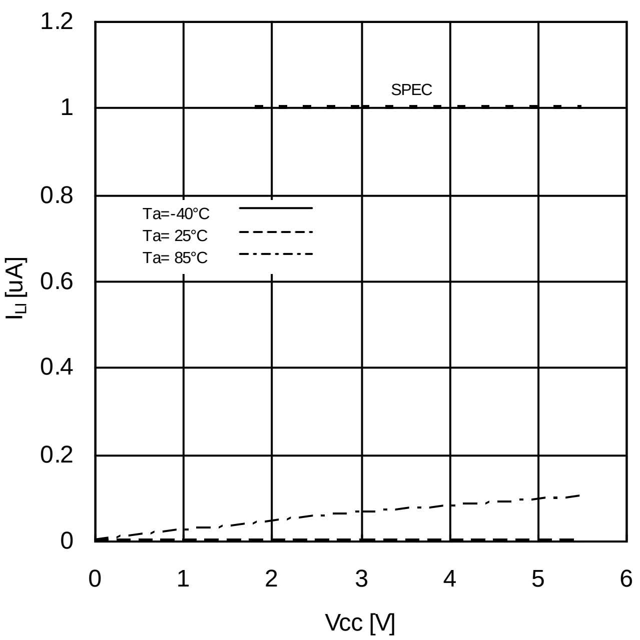

Figure 11. Input Leakage Current vs Supply Voltage (CSB,SCK,SI,HOLDB,WPB)

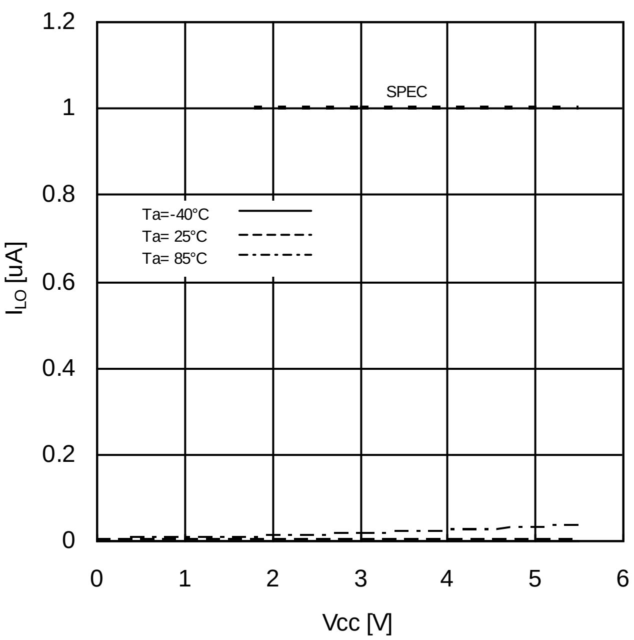

Figure 12. Output Leakage Current vs Supply Voltage (SO)

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Typical Performance Curves - Continued

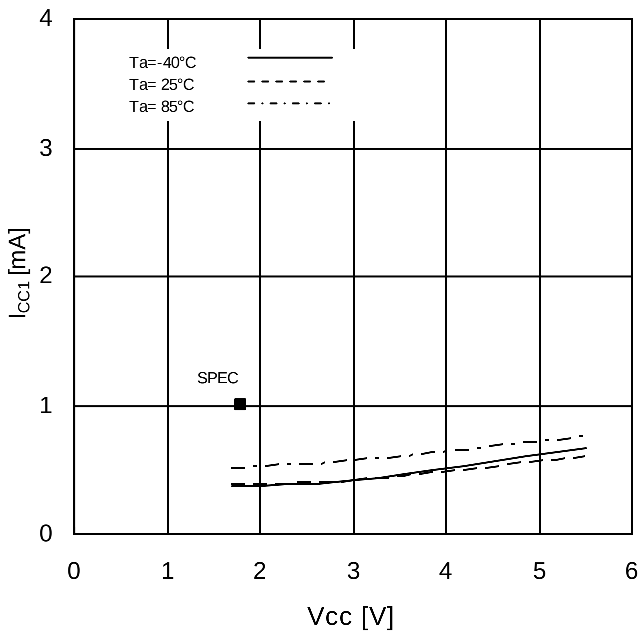

Figure 13. Supply Current (Write) vs Supply Voltage (fSCK=5MHz)

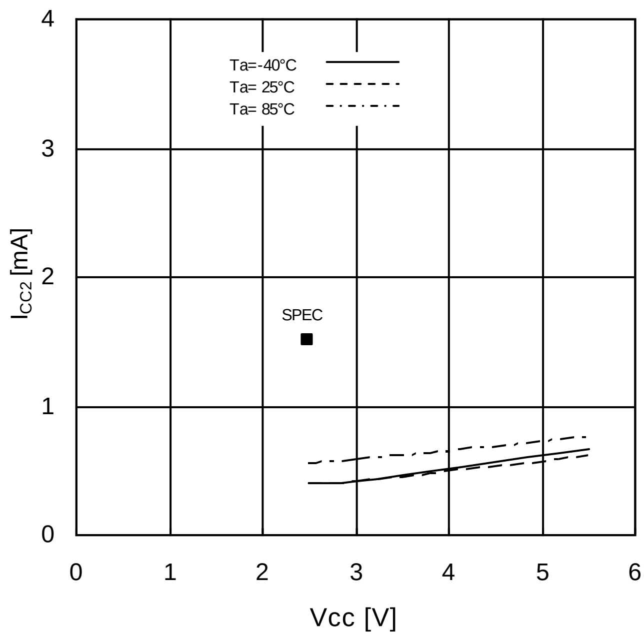

Figure 14. Supply Current (Write) vs Supply Voltage (fSCK=10MHz)

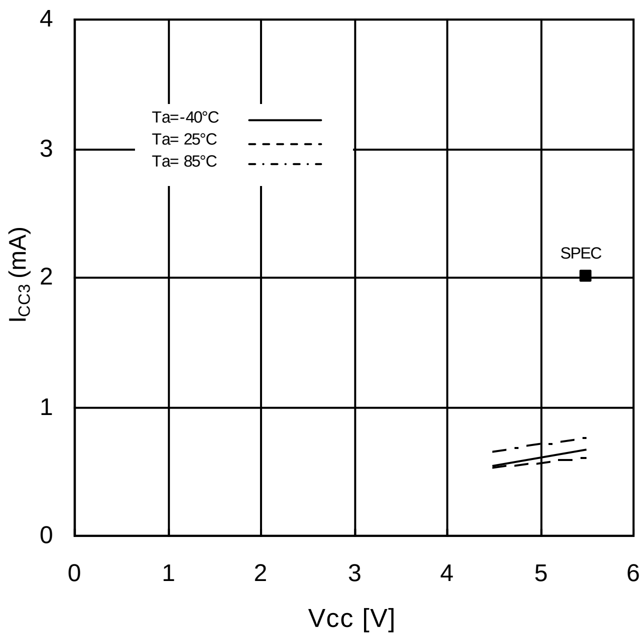

Figure 15. Supply Current (Write) vs Supply Voltage (fSCK=20MHz)

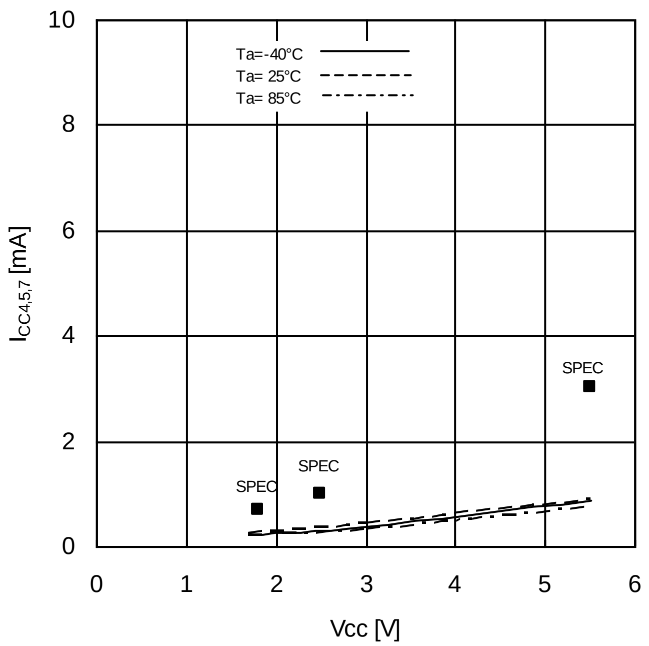

Figure 16. Supply Current (Read) vs Supply Voltage (fSCK=5MHz)

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Typical Performance Curves - Continued

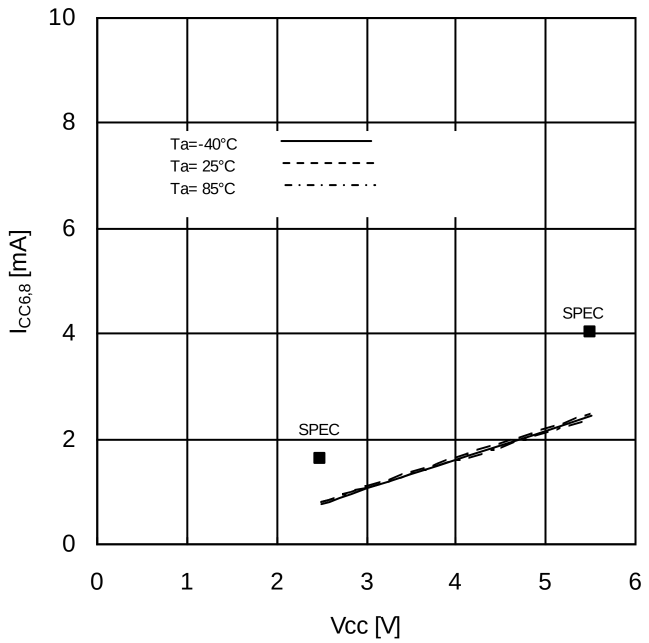

Figure 17. Supply Current (Read) vs Supply Voltage (fSCK=10MHz)

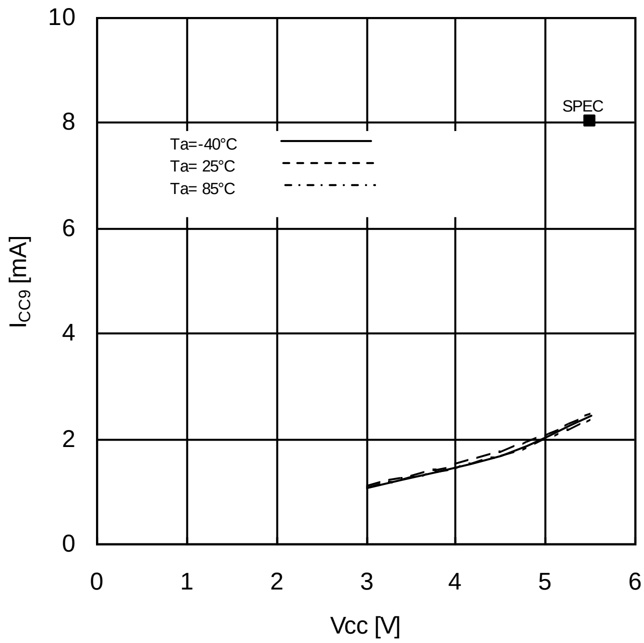

Figure 18. Supply Current (Read) vs Supply Voltage (fSCK=20MHz)

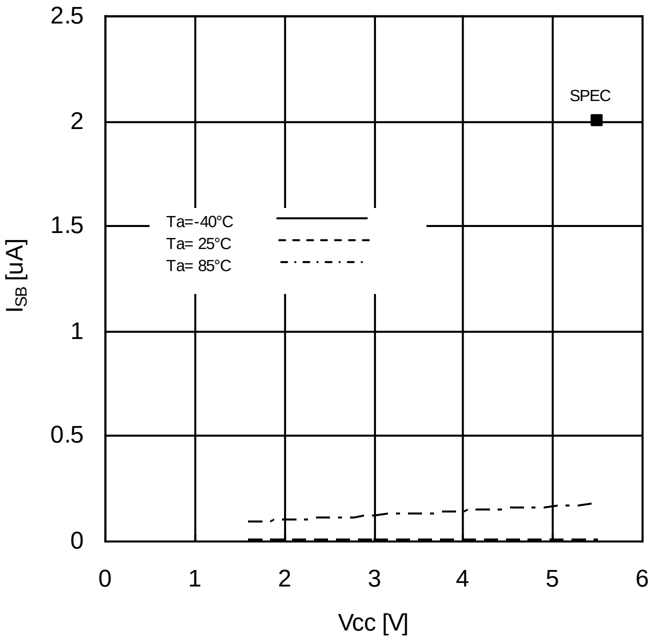

Figure 19. Standby Current vs Supply Voltage

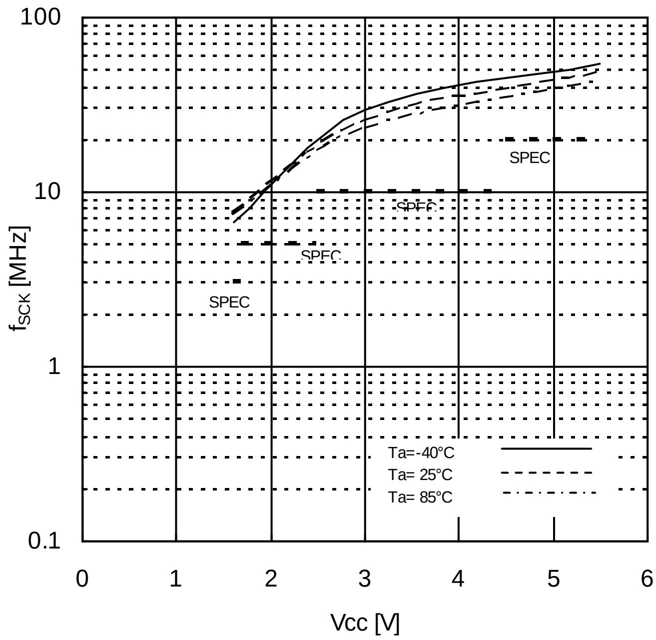

Figure 20. SCK Frequency vs Supply Voltage

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Typical Performance Curves - Continued

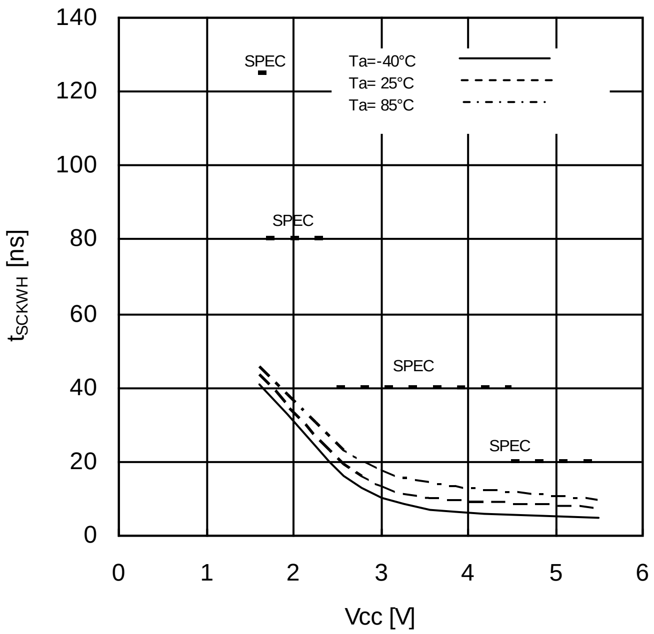

Figure 21. SCK High Time vs Supply Voltage

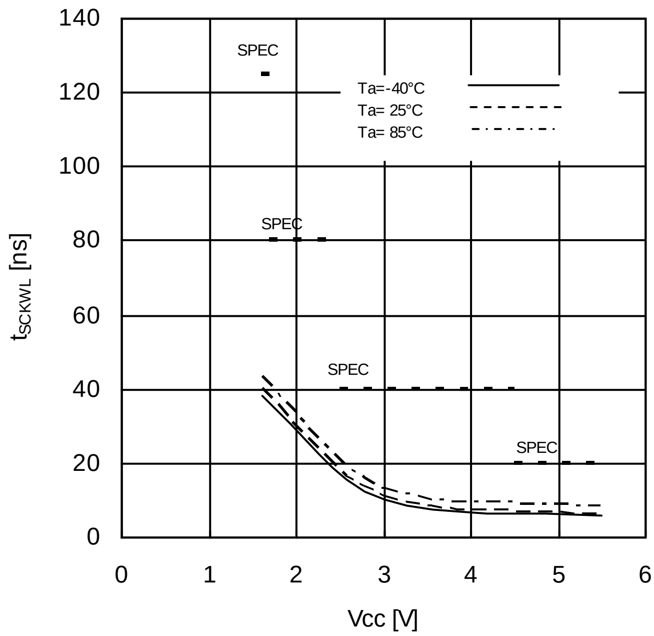

Figure 22. SCK Low Time vs Supply Voltage

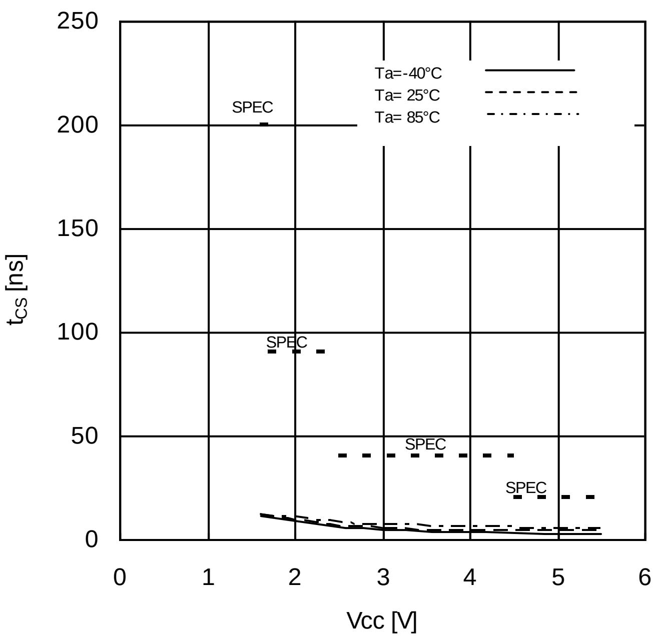

Figure 23. CSB High Time vs Supply Voltage

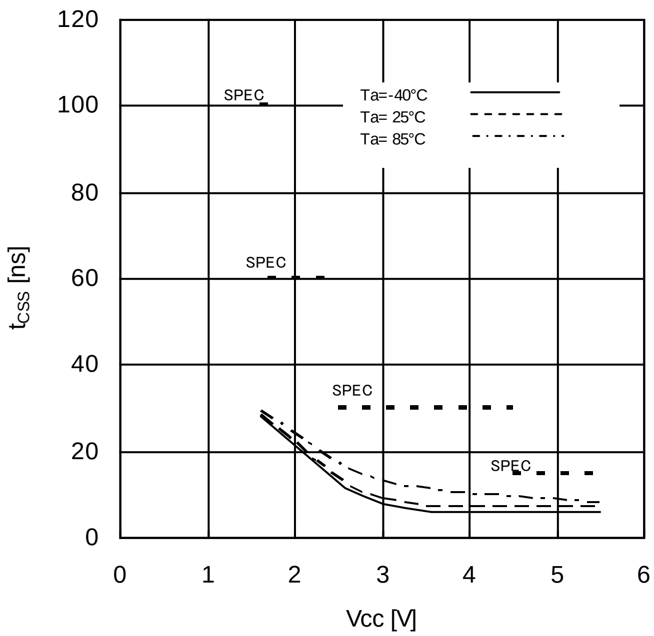

Figure 24. CSB Setup Time vs Supply Voltage

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Typical Performance Curves - Continued

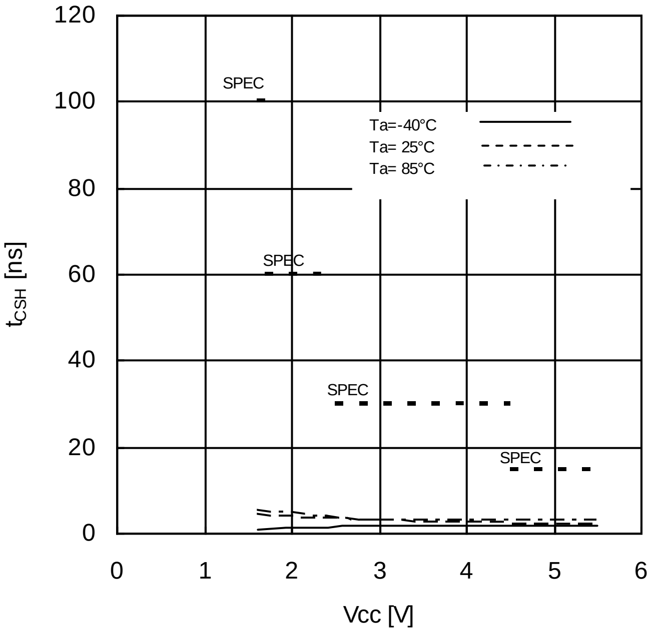

Figure 25. CSB Hold Time vs Supply Voltage

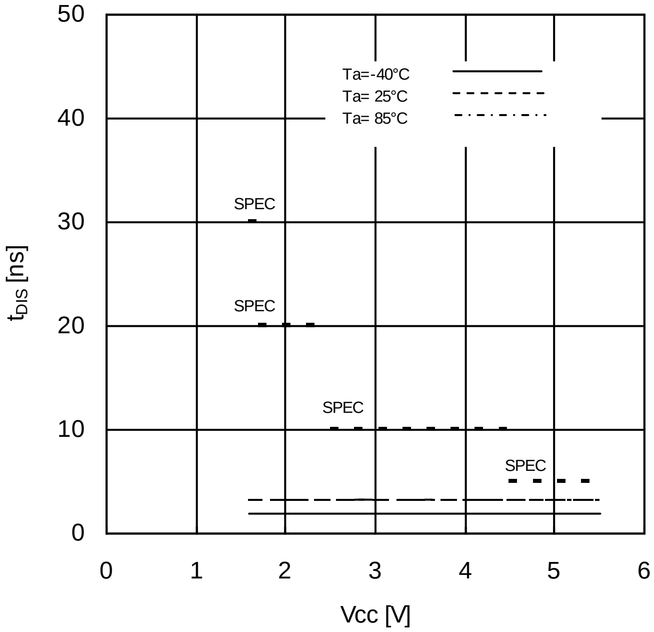

Figure 26. SI Setup Time vs Supply Voltage

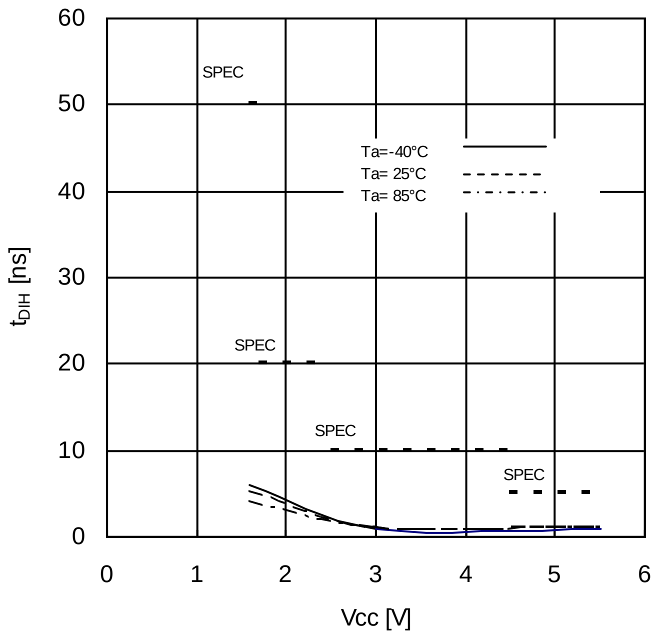

Figure 27. SI Hold Time vs Supply Voltage

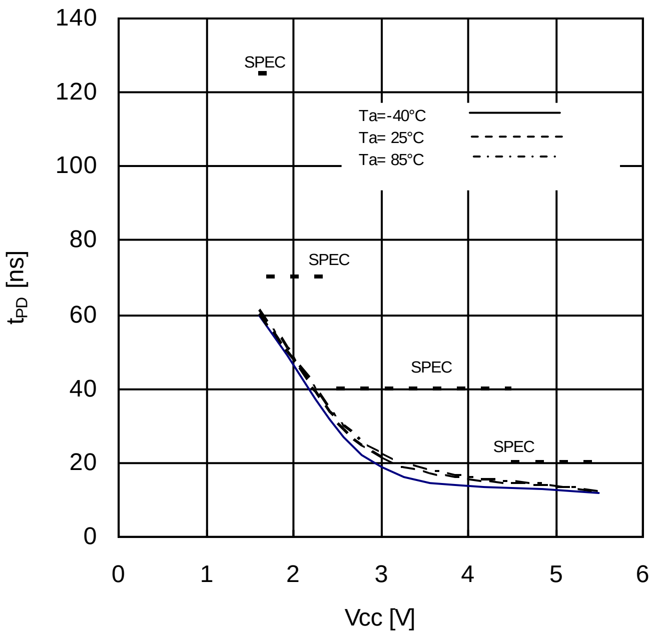

Figure 28. Data Output Delay Time vs Supply Voltage

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Typical Performance Curves - Continued

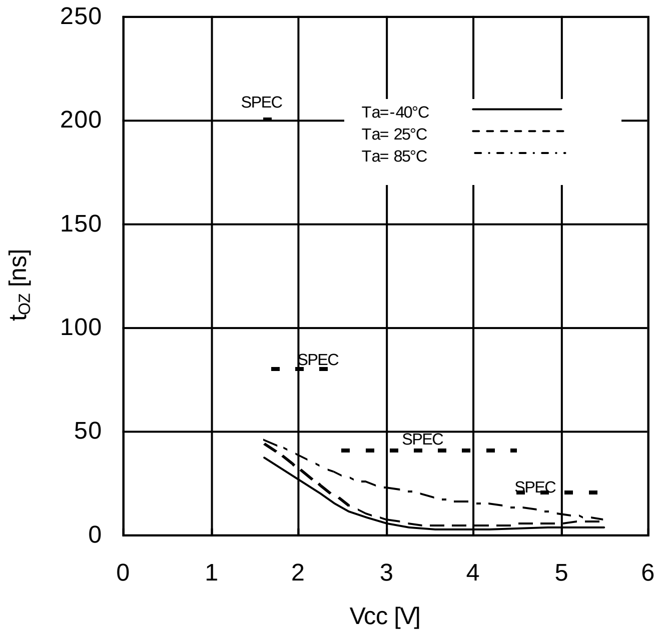

Figure 29. Output Disable Time vs Supply Voltage

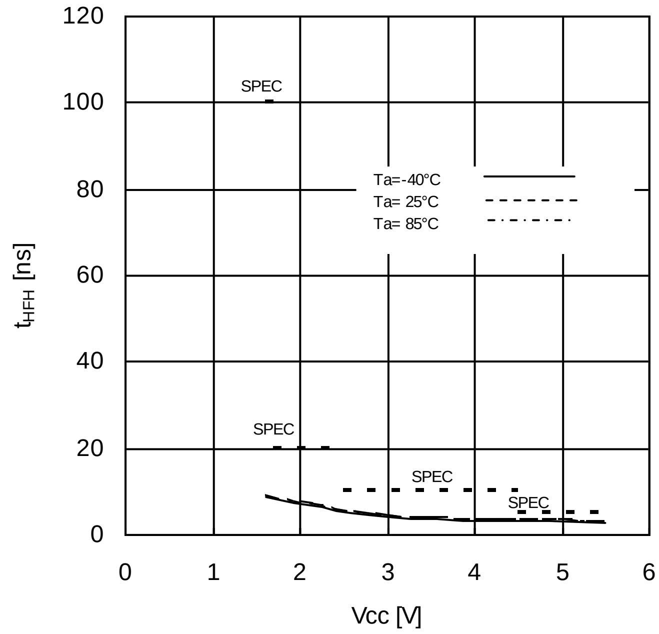

Figure 30. HOLDB Setting Hold Time vs Supply Voltage

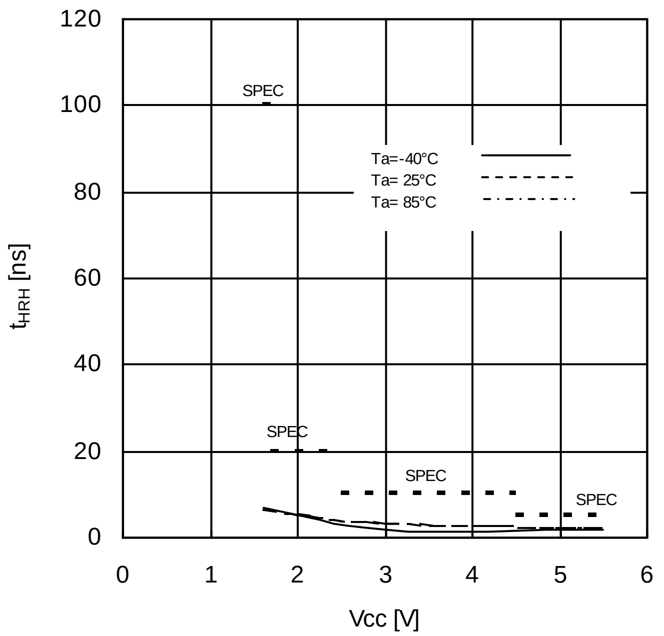

Figure 31. HOLDB Release Hold Time vs Supply Voltage

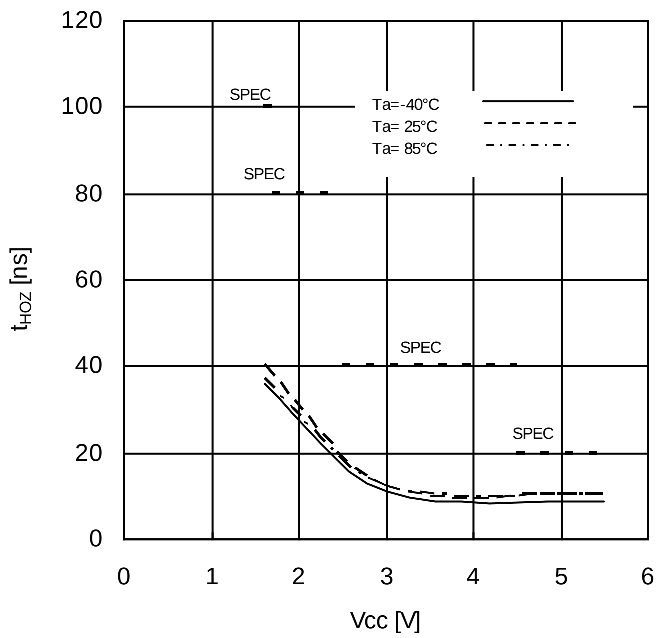

Figure 32. Time from HOLDB to Output High-Z
vs Supply Voltage

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Typical Performance Curves - Continued

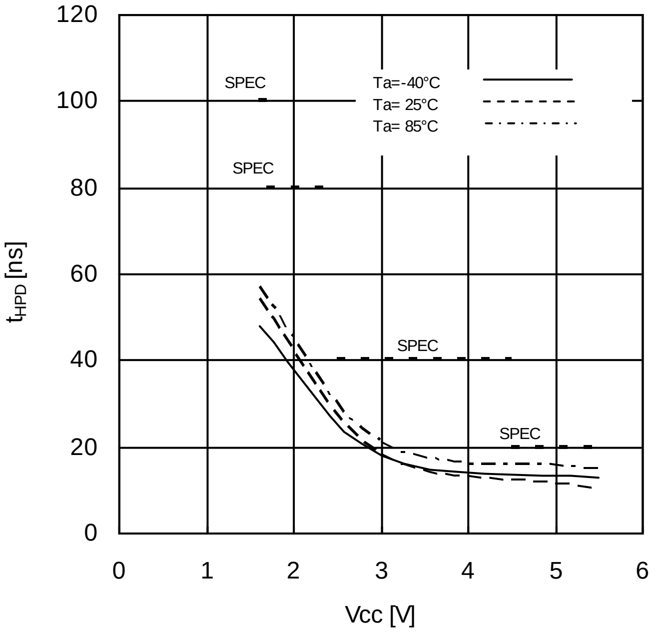

Figure 33. Time from HOLDB to Output change vs Supply Voltage

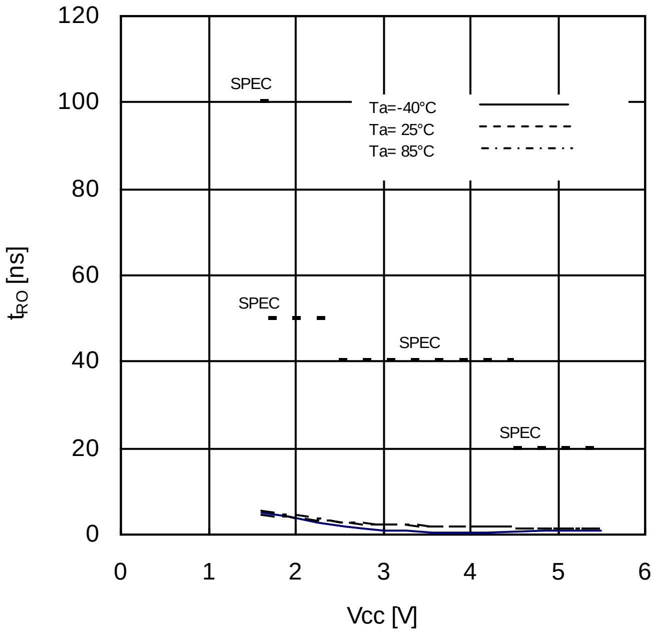

Figure 34. OUTPUT Rise Time vs Supply Voltage

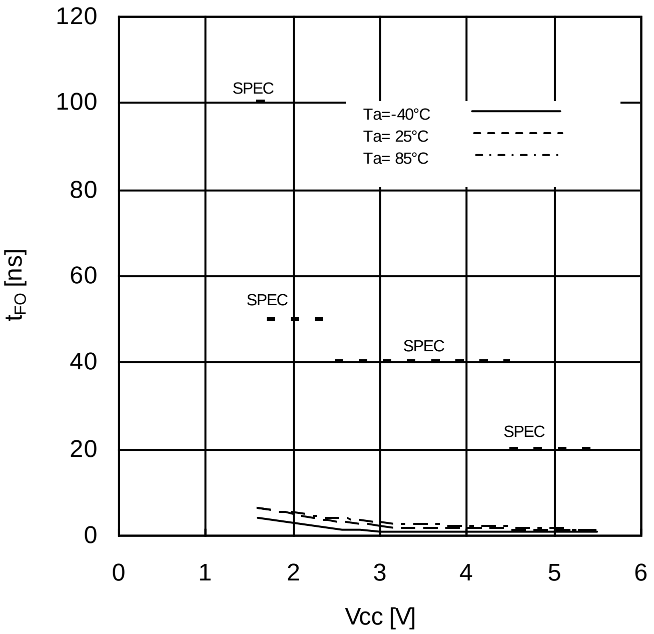

Figure 35. OUTPUT Fall Time vs Supply Voltage

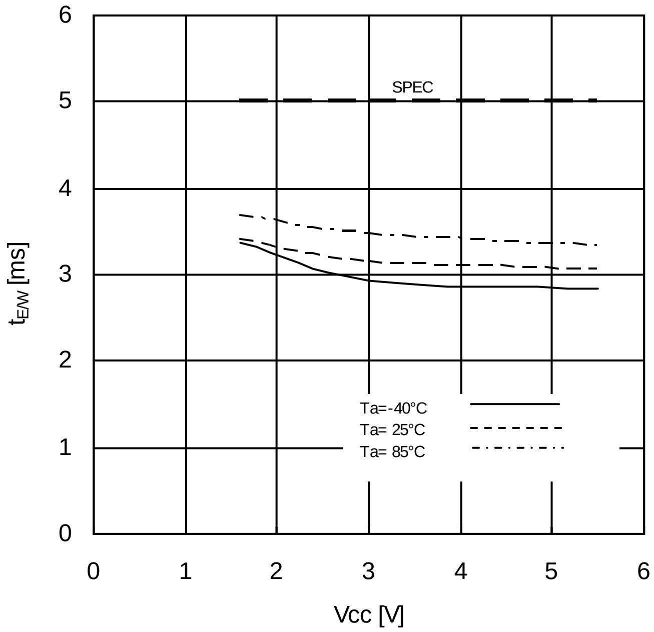

Figure 36. Write Cycle Time vs Supply Voltage

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Features

1. Status Registers

This IC has status register. The status register expresses the following parameters of 8 bits.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Rewrite characteristics and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status register command.

(1) Contexture of Status Register

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

bit	Memory location	Function
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid WPEN=1=valid
BP1 BP0	EEPROM	EEPROM write disable block designation bit
WEN	registers	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted
$\overline{R}$/B	registers	Write cycle status (READY / BUSY) status confirmation bit $\overline{R}$/B=0=READY $\overline{R}$/B=1=BUSY

(2) Write Disable Block Setting

BP1	BP0	Write disable block
0	0	None
0	1	6000h-7FFFh
1	0	4000h-7FFFh
1	1	0000h-7FFFh

2. WPB Pin

By setting WPB=LOW, write command is prohibited. And the write command to be disabled at this moment is WRSR.
However, when write cycle is in execution, no interruption can be made.

WRSR	WRITE
Prohibition possible but WPEN bit “1”	Prohibition impossible

3. HOLDB Pin

By HOLDB pin, data transfer can be interrupted. When SCK=”0”, by making HOLDB from “1” into”0”, data transfer to EEPROM is interrupted. When SCK = “0”, by making HOLDB from “0” into “1”, data transfer is restarted.

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Command Mode

Command	Contents	Ope code	
WREN	Write Enable Command	0000	0110
WRDI	Write Disable Command	0000	0100
READ	Read Command	0000	0011
WRITE	Write Command	0000	0010
RDSR	Read Status Register Command	0000	0101
WRSR	Write Status Register Command	0000	0001

Timing Chart

1. Write Enable (WREN) / Disable (WRDI) Command

WREN (WRITE ENABLE): Write enable

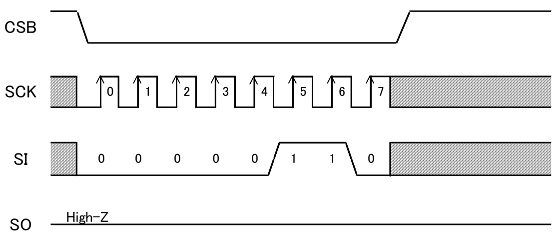

Figure 37. Write enable command

WRDI (WRITE DISABLE): Write disable

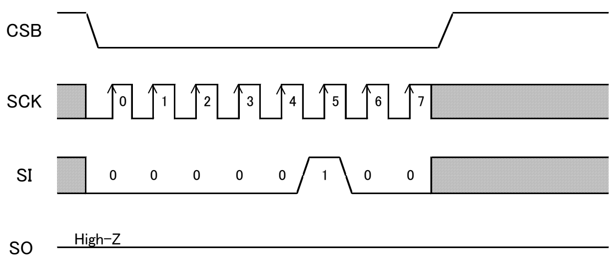

Figure 38. Write disable command

This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective ope codes. The respective commands are accepted at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.
When to carry out write command, it is necessary to set write enable status by the write enable command. If write command is input in the write disable status, the command is cancelled. And even in the write enable status, once write command is executed, it gets in the write disable status. After power on, this IC is in write disable status.

2. Read Command (READ)

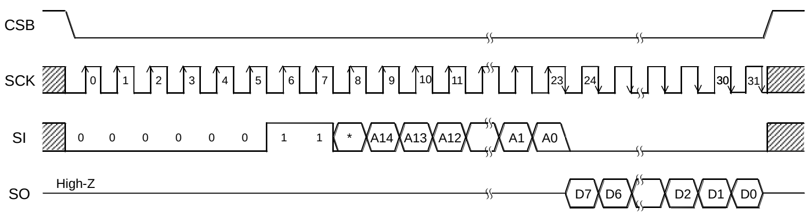

Figure 39. Read command

By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 23-th clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

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3. Write Command (WRITE)

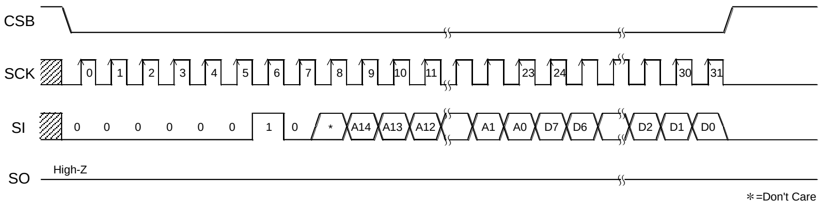

Figure 40. Write command

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of $t_{E/W}$ (Max 5ms). During $t_{E/W}$, other than read status register command is not accepted. Set CSB HIGH between taking the last data (D0) and rising the next SCK clock. At the other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without setting CSB HIGH, 2byte or more data can be written for one $t_{E/W}$. Up to 64 arbitrary bytes can be written. In page write, the insignificant 6 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

4. Write Status Register, Read Status Register Command (WRSR/RDSR)

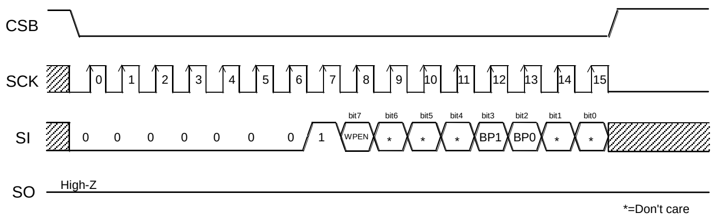

Figure 41. Write status register

Write status register command can write data of status register. The data can be written by this command are 3 bits, that is, WPEN (bit7), BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of $t_{E/W}$ as same as write. As for CSB rise, set CSB HIGH between taking the last data bit (bit0) and the next SCK clock rising. At the other timing, command is cancelled. Write disable block is determined by BP1 BP0, and the block can be selected from 1/4, 1/2, and entire of memory array (Refer to the write disable block setting table.). To the write disabled block, write cannot be made, and only read can be made.

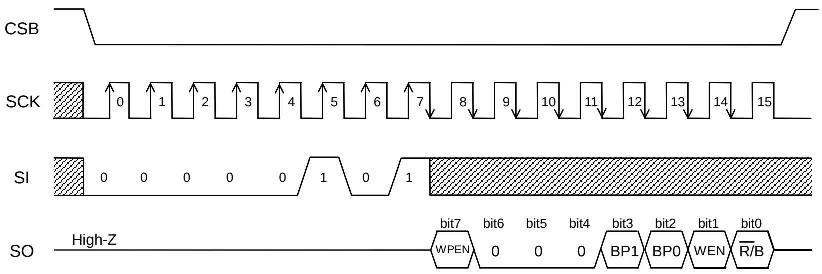

Figure 42. Read status register command

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WPB Cancel Valid Area

WPB is normally fixed to “H” or “L” for use, but when WPB is controlled so as to cancel write status register command, pay attention to the following WPB valid timing.
While write status register command is executed, by setting WPB = “L” in cancel valid area, command can be cancelled. The area from command ope code to CSB rise at internal automatic write start becomes the cancel valid area. However, once write is started, by any input write cycle cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

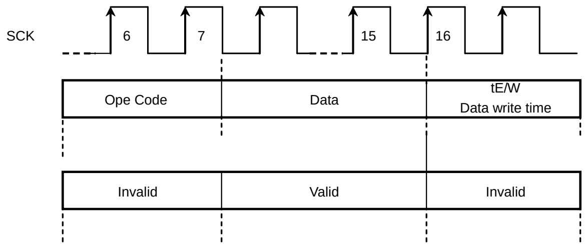

Figure 43. WPB valid timing (At inputting WRSR command)

HOLDB Pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The command communications are carried out when the HOLDB pin is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, keep CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

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Method to Cancel Each Command

1. READ, RDSR
   - Method to cancel : cancel by CSB = “H”.

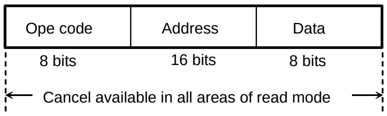

Figure 44. READ cancel valid timing

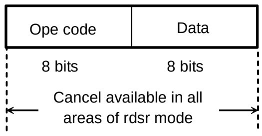

Figure 45. RDSR cancel valid timing

2. WRITE, PAGE WRITE
   - a: Ope code or address input area
     Cancellation is available by CSB=”H”.
   - b: Data input area (D7 to D1 input area)
     Cancellation is available by CSB=”H”.
   - c: Data input area (D0 area)
     In this area, cancellation is not available.
     When CSB is set HIGH, write starts.
   - d: $t_{E/W}$ area
     In the area c, by rising CSB, write starts.
     While writing, by any input, cancellation cannot be made.

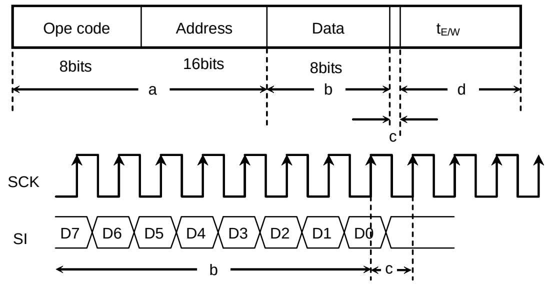

Figure 46. WRITE cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note2) If CSB is rised at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = “L” area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or more.

3. WRSR
   - a: From ope code to 15-th clock rise
     Cancellation is available by CSB=”H”.
   - b: From 15-th clock rise to 16-th clock rise (write enable area)
     In this area, cancellation is not available by CSB=”H”.
     When CSB is set HIGH, write starts.
   - c: After 16-th clock rise.
     Cancellation is available by CSB=”H”.
     However, if write starts (CSB is rised)
     In the area b, cancellation cannot be made by any means.
     And, by inputting on SCK clock, cancellation cannot be made.

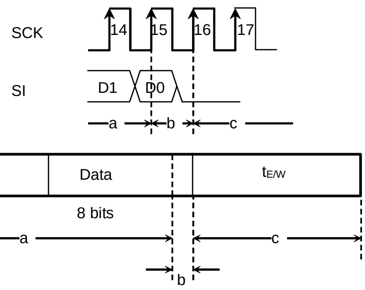

Figure 47. WRSR cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
Note2) If CSB is rised at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = “L” area. As for SCK rise, assure timing of t_{CSS} / t_{CSH} or more.

4. WREN/WRDI
   - a: From ope code to 7-th clock rise, cancellation is available by CSB = “H”.
   - b: Cancellation is not available 7-th clock.

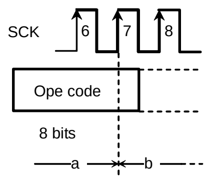

Figure 48. WREN/WRDI cancel valid timing

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I/O Peripheral Circuits

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

Input pin pull up, pull down resistance
When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller V_{OL}, I_{OL} with considering V_{IL} characteristics of this IC.

1. Pull Up Resistance

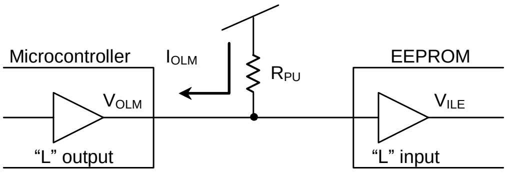

Figure 49. Pull up resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad \ldots ①$$

$$V_{OLM} \leq V_{ILE} \quad \ldots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA,
from the equation ①,

$$R_{PU} \geq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \geq 2.3[k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

- V_{ILE} :EEPROM V_{IL} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

And, in order to prevent malfunction or erroneous write at power ON/OFF, be sure to make CSB pull up.

2. Pull Down Resistance

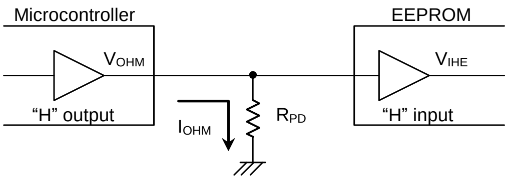

Figure 50. Pull down resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad \ldots ③$$

$$V_{OHM} \geq V_{IHE} \quad \ldots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA,
V_{IHE}=V_{CC}×0.7V, from the equation③,

$$R_{PD} \geq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PD} \geq 11.3[k\Omega]$$

Further, by amplitude V_{IHE}, V_{ILE} of signal input to EEPROM, operation speed changes. By inputting Vcc/GND level amplitude of signal, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8Vcc / 0.2Vcc is input, operation speed becomes slow.(Note1)

In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of Vcc / GND level.
(Note1) In this case, guaranteed value of operating timing is guaranteed.

3. SO Load Capacity Condition

Load capacity of SO output pin affects upon delay characteristic of SO output (Data output delay time, time from HOLDB to High-Z, Output rise time, Output fall time.). In order to make output delay characteristic into better, make SO load capacity small.

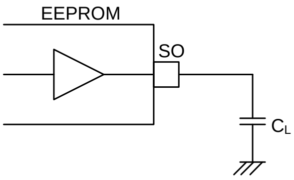

Figure 51. SO load capacity

4. Other cautions

Make the each wire length from the microcontroller to EEPROM input pin same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

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Equivalent Circuit

1. Output Circuit

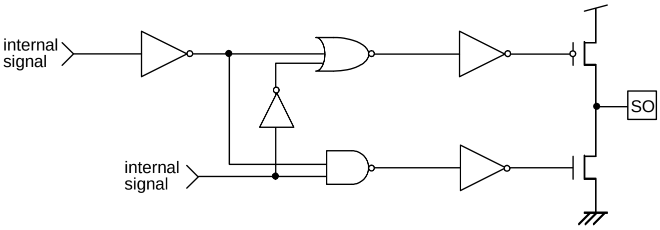

Figure 52. SO output equivalent circuit

2. Input Circuit

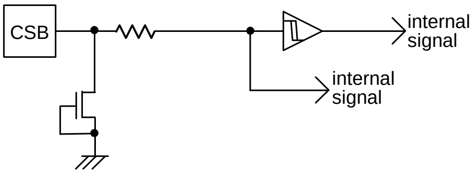

Figure 53. CSB input equivalent circuit

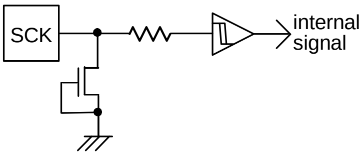

Figure 54. SCK input equivalent circuit

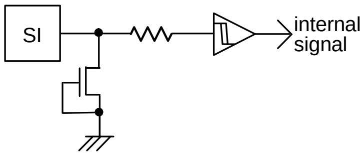

Figure 55. SI input equivalent circuit

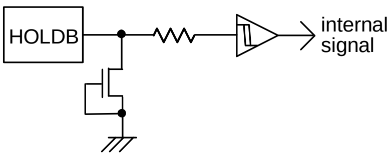

Figure 56. HOLDB input equivalent circuit

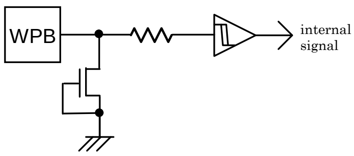

Figure 57. WPB input equivalent circuit

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Power-Up/Down Conditions

1. At Standby
   Set CSB “H”, and be sure to set SCK, SI input “L” or “H”. Do not input intermediate electric potantial.

2. At Power ON/OFF
   When Vcc rise or fall, set CSB=”H” (=Vcc).
   When CSB is “L”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, erroneous write or so. To prevent these, at power ON, set CSB “H”. (When CSB is in “H” status, all inputs are canceled.)

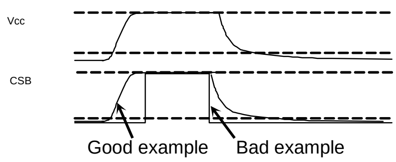

Figure 58. CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to Vcc.
At power OFF, take 10ms or more before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset.

(Bad example) CSB terminal is “L” at power ON/OFF.
In this case, CSB always becomes “L” (active status), and EEPROM may have malfunction or erroneous write owing to noises and the likes.
Even when CSB input is High-Z, the status becomes like this case.

3. Operating Timing after Power ON
   As shown in Figure 53, at standby, when SCK is “H”, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB “H” status.

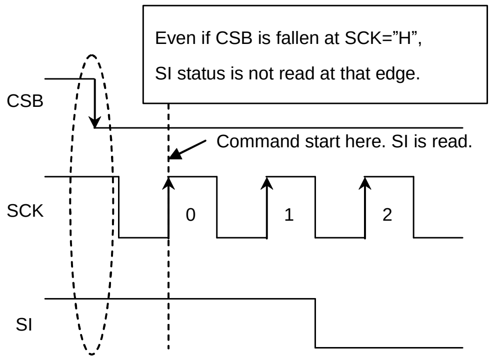

Figure 59. Operating timing

4. At Power on Malfunction Preventing Function
   This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following t_R, t_{OFF}, and V_{bot} are not satisfied, it may become write enable status owing to noises and the likes.

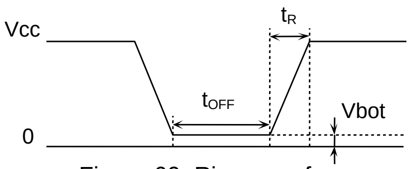

Figure 60. Rise waveform

Recommended conditions of t_R, t_{OFF}, V_{bot}

t_R	t_{OFF}	V_{bot}
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

5. Low Voltage Malfunction Preventing Function
   LVCC (Vcc-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.
   At LVCC voltage (Typ =1.2V) or below, it prevent data rewrite.

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Noise Countermeasures

1. Vcc Noise (bypass capacitor)
When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1µF) between IC Vcc and GND. At that time, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

2. SCK Noise
When the rise time of SCK (t_{RC}) is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SCK (t_{RC}) 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

3. WPB Noise
During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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Ordering Information

B	R	2	5	G	2	5	6	x	x	x	-	3		x	x	x

BUS Type
25: SPI

Operating Temperature/Voltage
-40°C to +85°C / 1.6V to 5.5V

Capacity
256=256K

Package

Blank	: DIP-T8*1	FJ	: SOP-J8
F	: SOP8	FVT	: TSSOP-B8

Process Code

G : Halogen free
Blank : Not Halogen free

Packaging and Forming Specification

E2	: Embossed tape and reel (SOP8, SOP-J8, TSSOP-B8,)
None	: Tube (DIP-T8*1)

*1 Not Recommended for New Designs.

Lineup

Capacity	Package		Orderable Part Number		Remark
	Type	Quantity			
256K	DIP-T8*1	Tube of 2000	BR25G256	-3	Not Halogen free
	SOP8	Reel of 2500	BR25G256F	-3GE2	Halogen free
	SOP-J8		BR25G256FJ	-3GE2	Halogen free
	TSSOP-B8	Reel of 3000	BR25G256FVT	-3GE2	Halogen free

*1 Not Recommended for New Designs.

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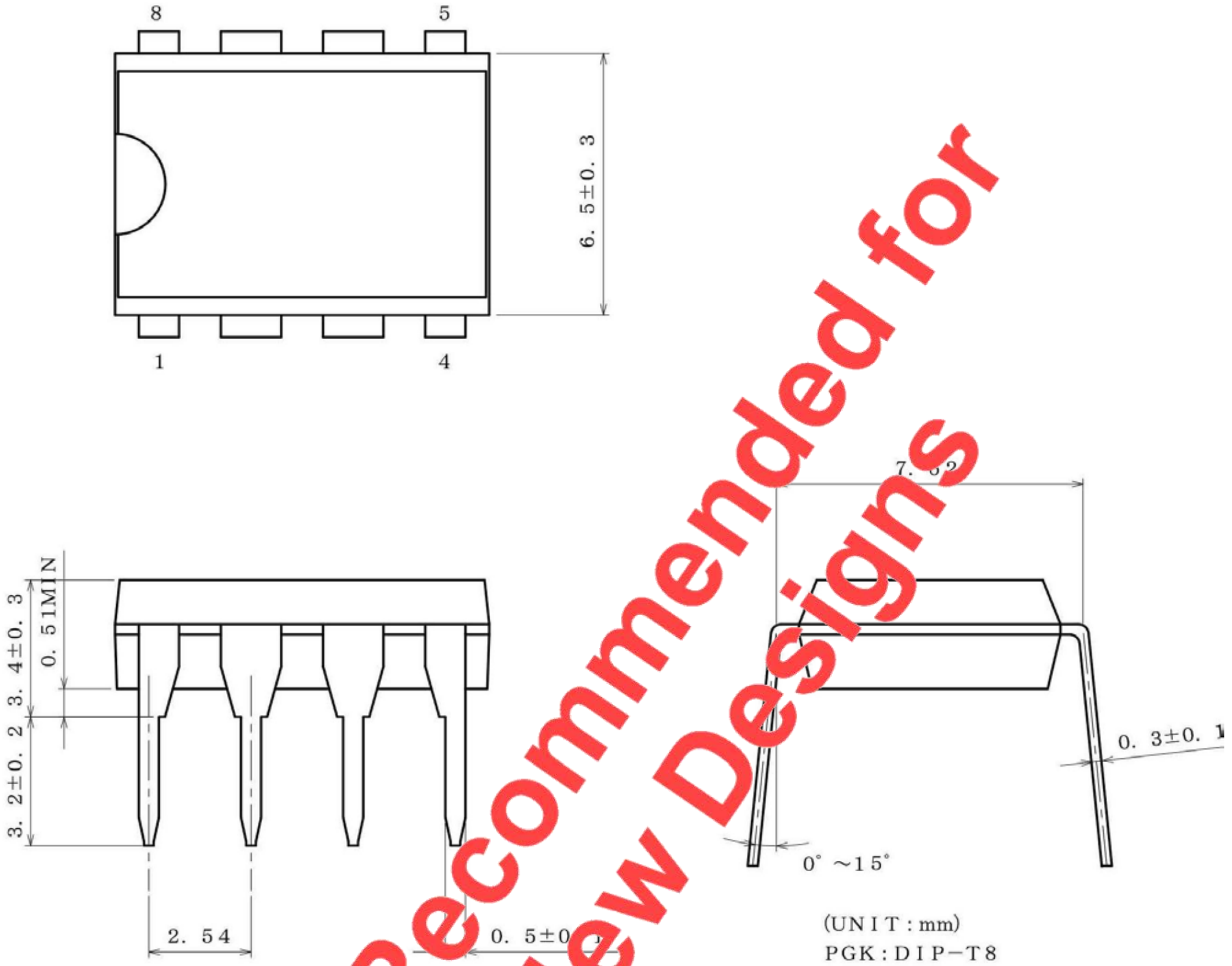
Physical Dimension Tape and Reel Information

Package Name	DIP-T8

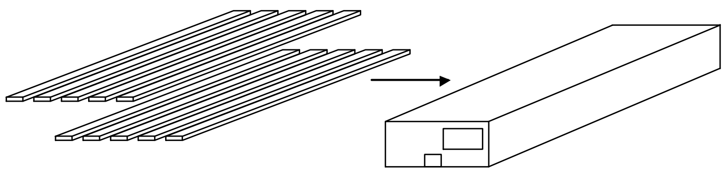


(UNIT : mm)
PGK : DIP−T8
Drawing No. A0782

Not Recommended for New Designs

<Tape and Reel information>

Container	Tube
Quantity	2000pcs
Direction of feed	Direction of products is fixed in a container tube



∗Order quantity needs to be multiple of the minimum quantity.

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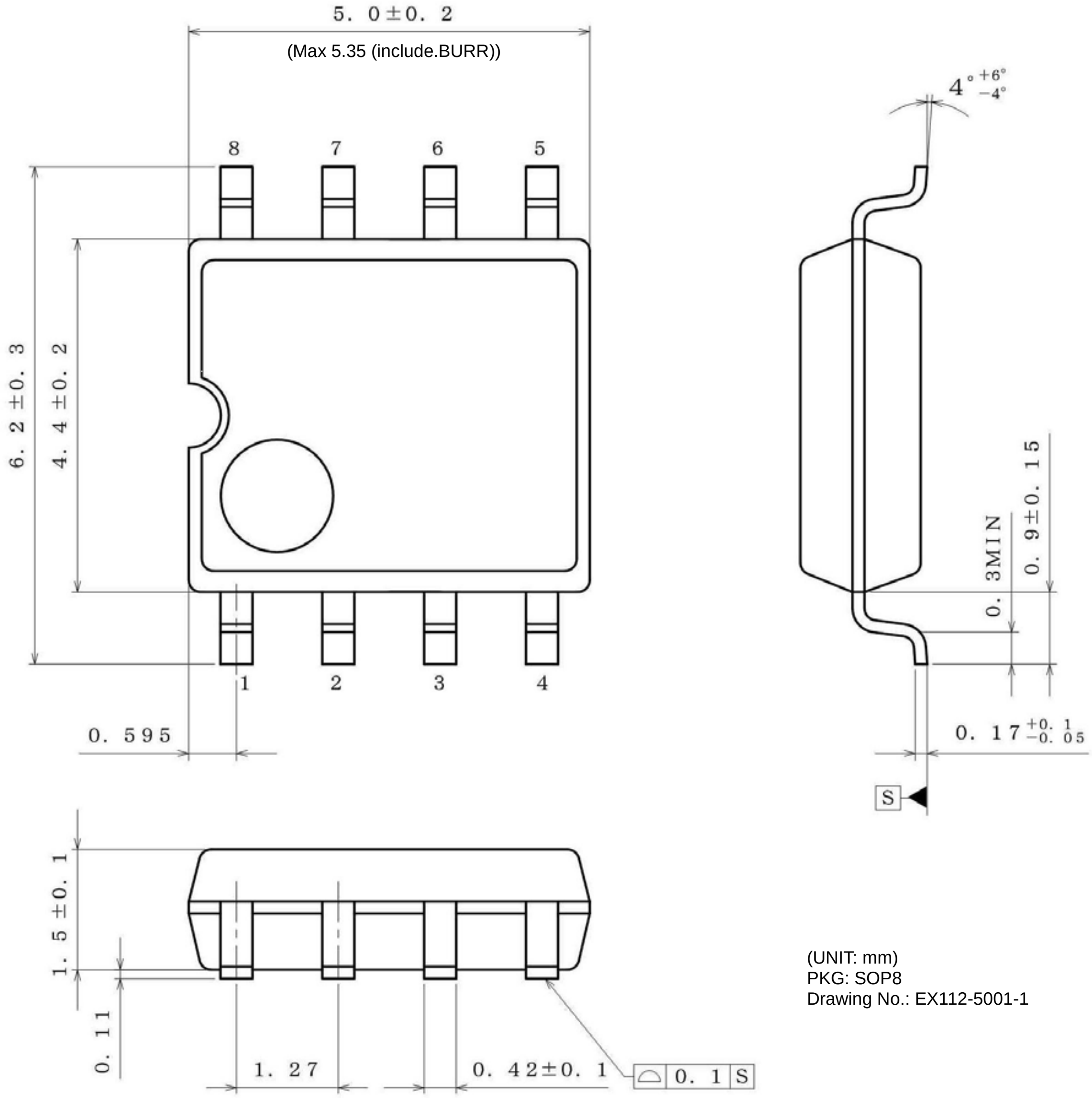
Physical Dimension Tape and Reel Information

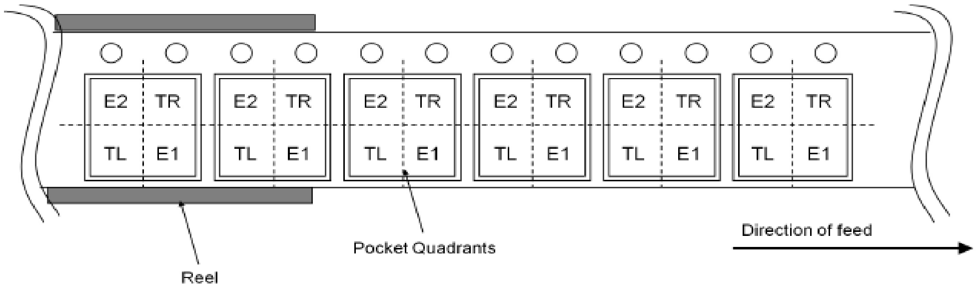
Package Name	SOP8



(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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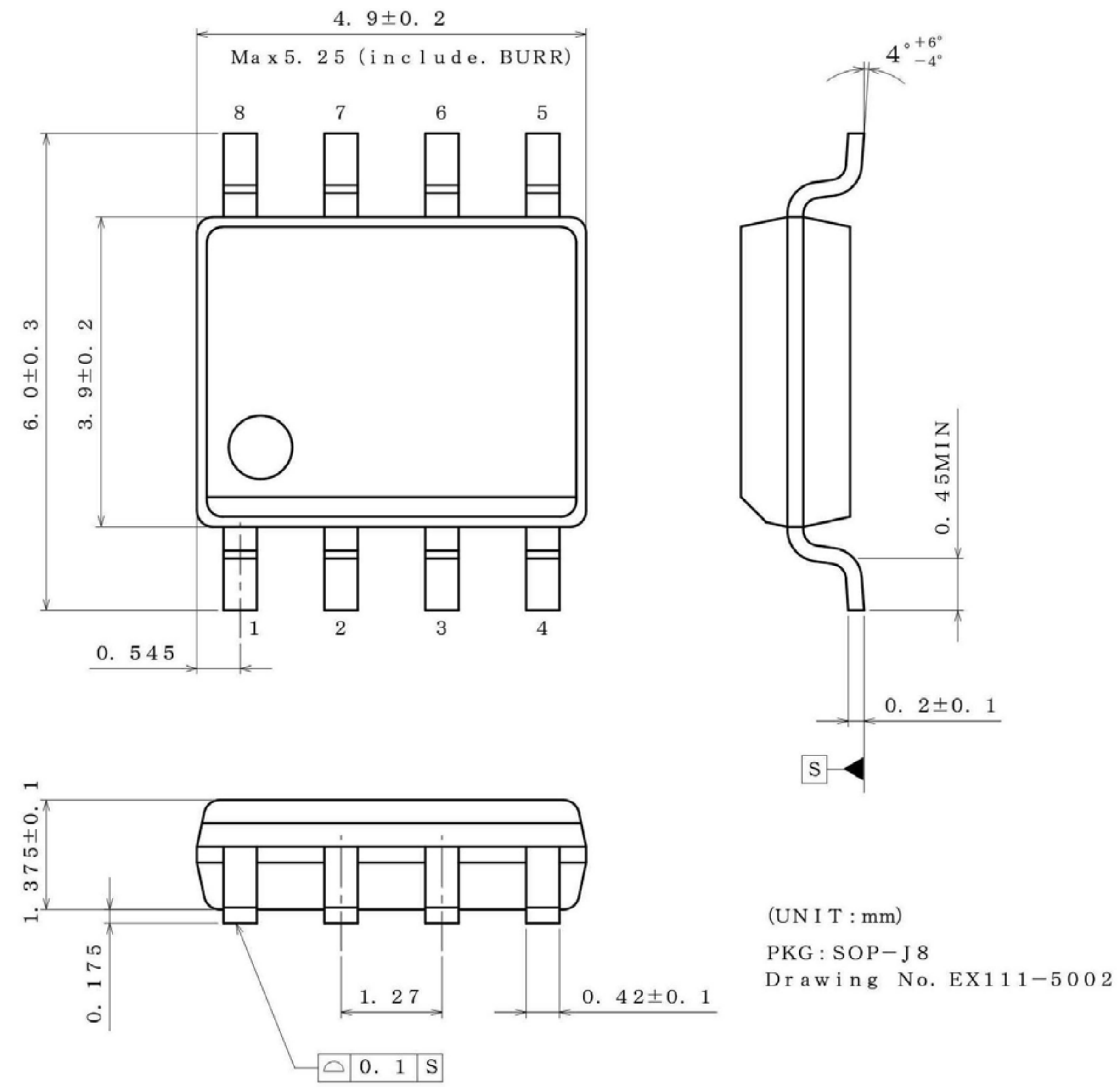
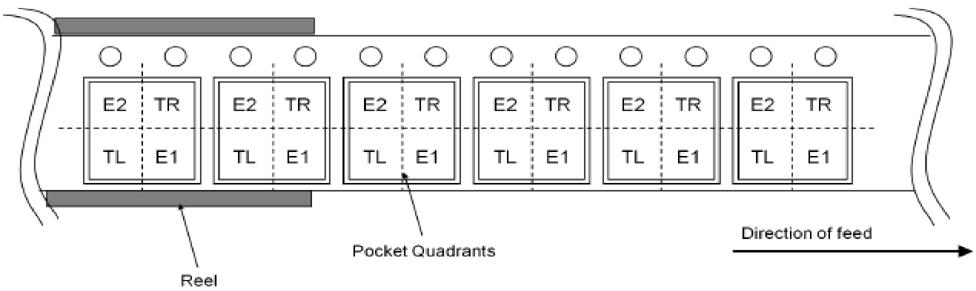
Physical Dimension Tape and Reel Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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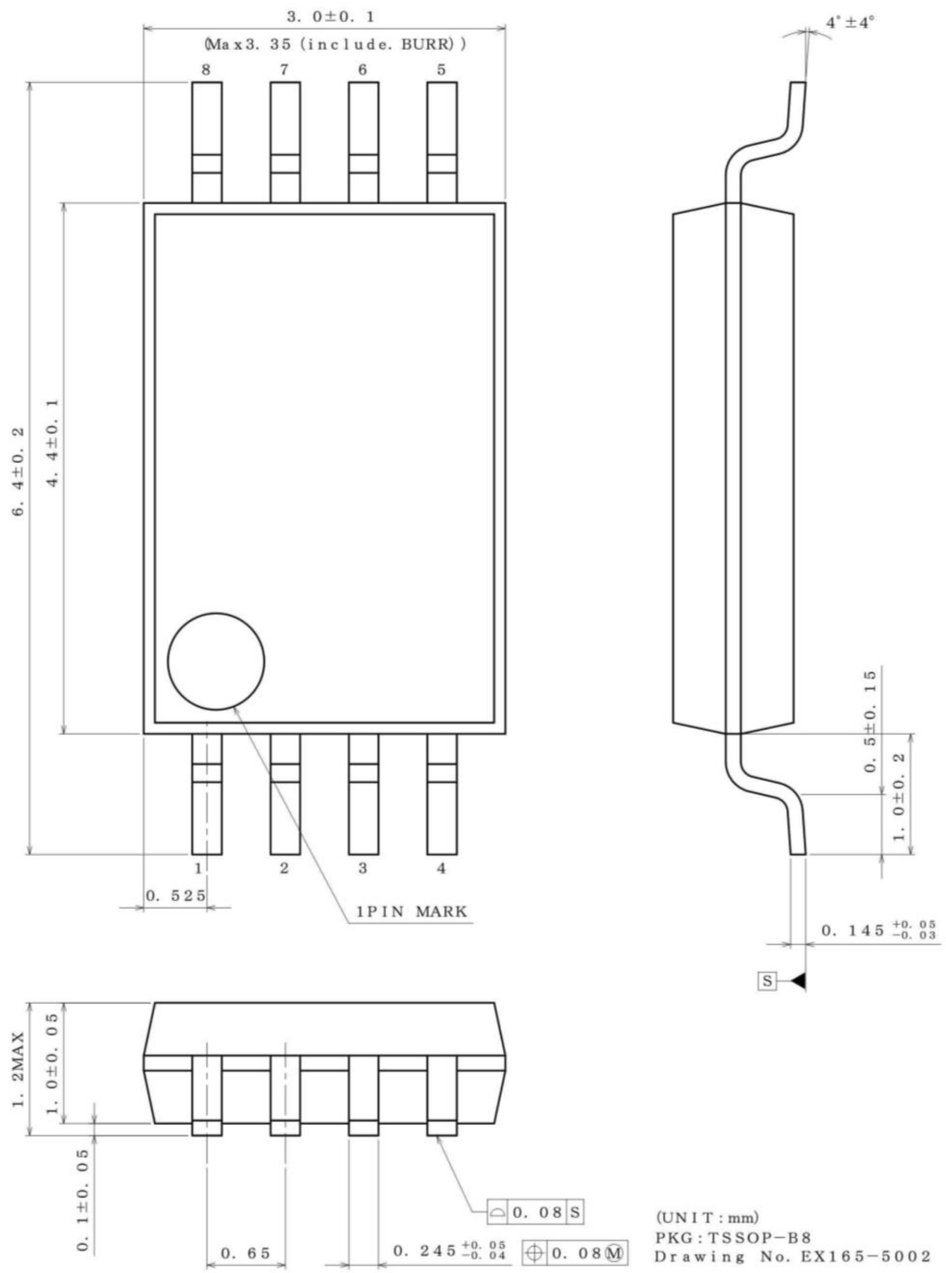
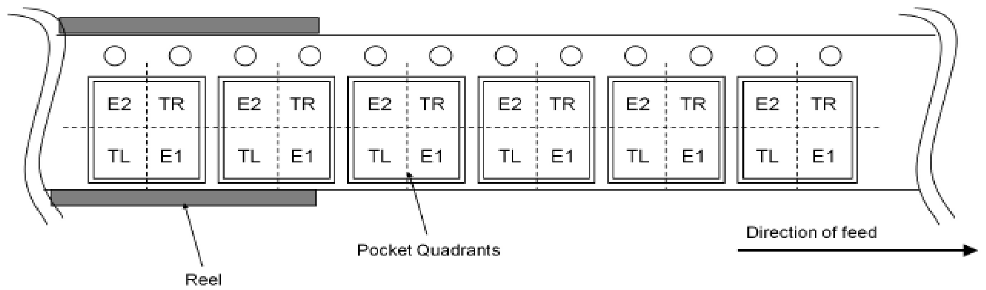
Physical Dimension Tape and Reel Information

Package Name	TSSOP-B8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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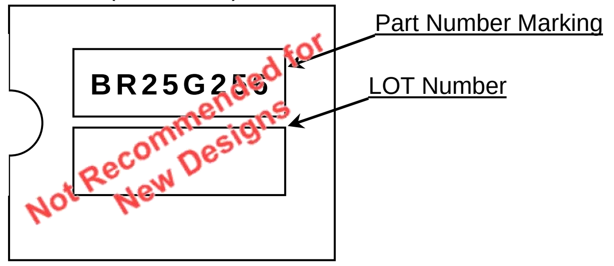
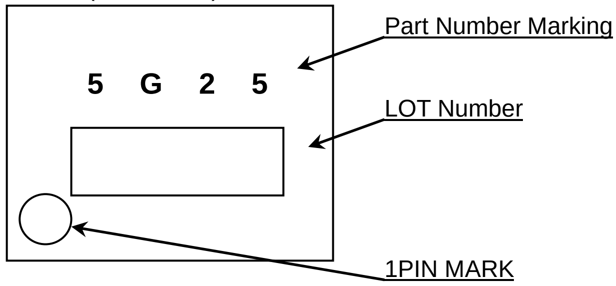
Marking Diagrams

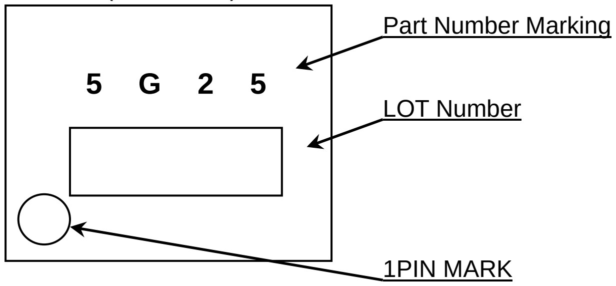
DIP-T8 (TOP VIEW)



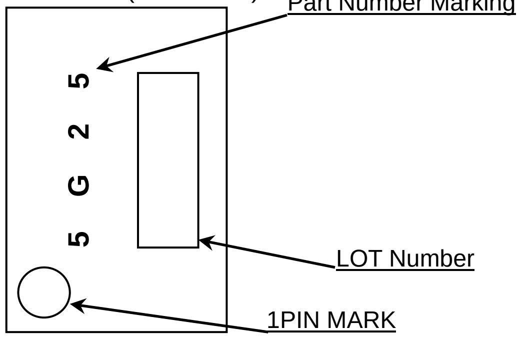
SOP8(TOP VIEW)



SOP-J8(TOP VIEW)



TSSOP-B8(TOP VIEW)



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Revision History

Date	Revision	Changes
06.Dec.2013	001	New Release
04.Dec.2014	002	Update some English words, sentences' descriptions, grammar and formatting. P.1 Update Current Consumption. P.2 Add Electrostatic discharge voltage and bypass capacitor. P.3 Delete supply current I_{cc5}. P.4 Update AC timing characteristics conditions. P.4 Update Serial Data Input / Output Timing. P.5 Update Pin Descriptions. P.6-13 Add typical performance curve. P.30 Update the marking diagrams.
11.Jun.2019	003	Added watermarks and words for Not Recommended New Designs category product. Changed a format of "Physical Dimension and Packing Information".
05.Jan.2021	004	Updated packages and part numbers

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Part Numbering

B	R	2	5	G	2	5	6	F	J	-	3		G	Z	E	2

BUS type
25: SPI

Operating temperature/
Operating Voltage
-40°C to +85°C / 1.6V to 5.5V

Capacity
256=256K

Package
FJ : SOP-J8A

Process Code

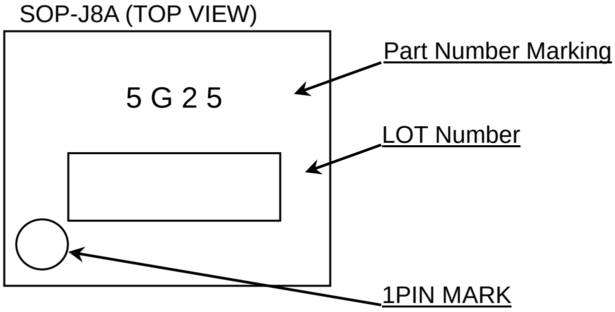
G : Halogen free

Production site
Z :Added

Packaging and Forming Specification
E2 : Embossed tape and reel

Marking Diagrams (TOP VIEW)

SOP-J8A (TOP VIEW)



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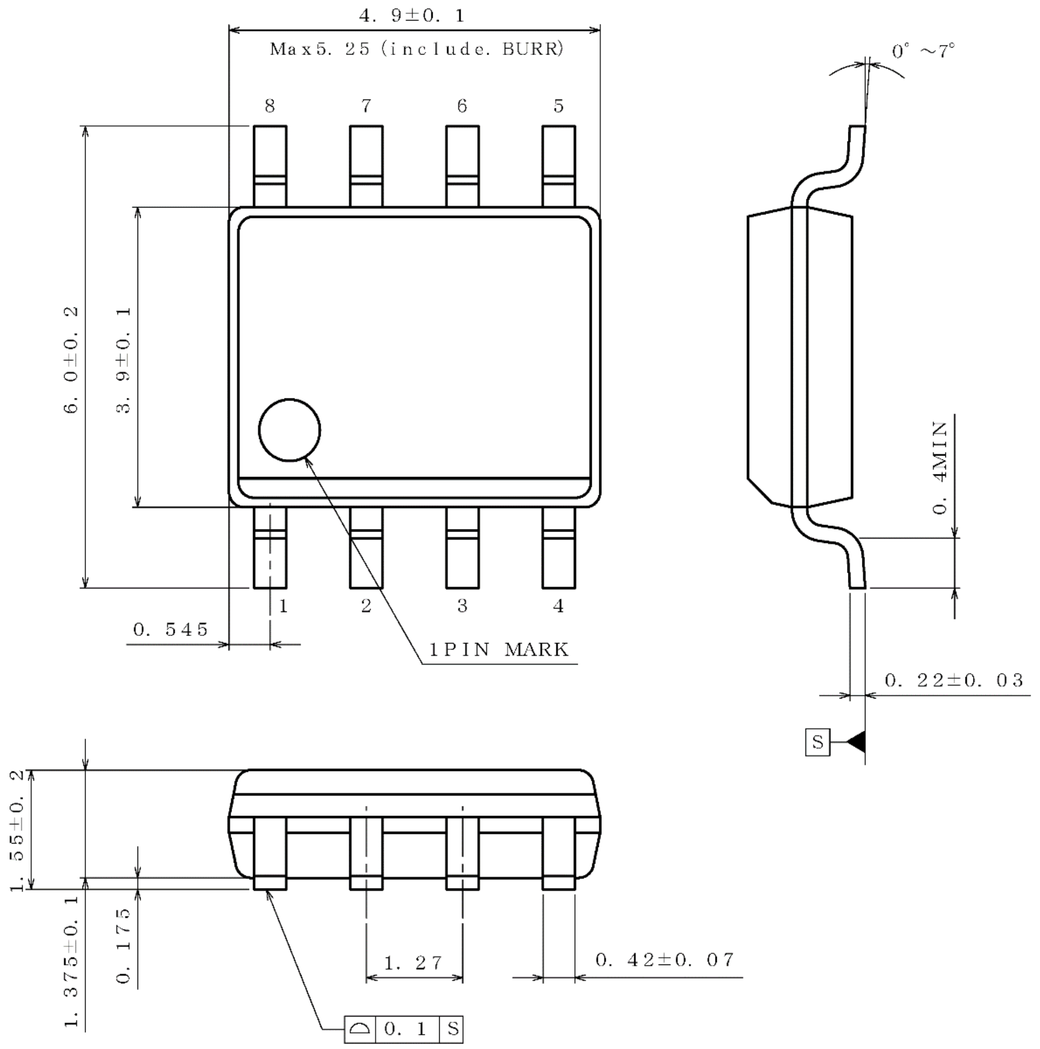
Physical Dimension and Packing Information

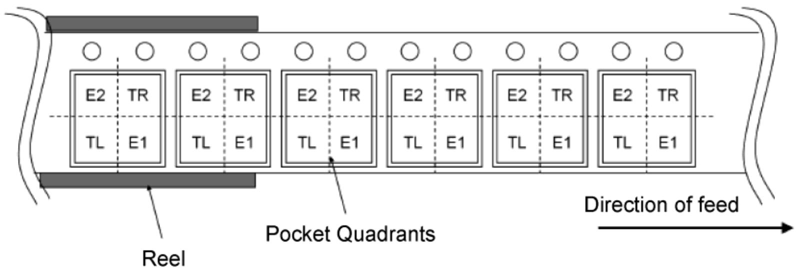
Package Name	SOP-J8A



(UNIT : mm)
PKG : SOP－J8A
Drawing No. EX001－0055－2

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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