Serial EEPROM Series for Automotive EEPROM

125 °C Operation MicroWire BUS EEPROM (3-Wire) for Automotive

BR93H66xxx-5C Series

General Description

BR93H66xxx-5C Series is a 4 Kbit serial EEPROM of serial 3-line interface method.

Features

- AEC-Q100 Qualified(Note 1)
- Functional Safety Supportive Automotive Products
- Conforming to MicroWire BUS
- Bit Format:256 x 16 bit
- Address Auto Increment Function at Read Operation
- Prevention of Write Mistake
  Write Prohibition at Power On
  Write Prohibition by Command Code
  Write Mistake Prevention Circuit at Low Voltage
- Auto Erase and Auto End Function at Programming Cycle
- Data Set to FFFFh on All Addresses at Shipment

(Note 1) Grade 1

Key Specifications

- Supply Voltage: 2.5 V to 5.5 V
- Ambient Operating Temperature: -40 °C to +125 °C
- Clock Frequency: 2 MHz (Max)
- Write Time: 4 ms (Max)
- Write Cycles:
  1 Million Times (Ta ≤ 85 °C)
  0.5 Million Times (Ta ≤ 105 °C)
  0.3 Million Times (Ta ≤ 125 °C)
- Data Retention:
  100 Years (Ta ≤ 25 °C)
  60 Years (Ta ≤ 105 °C)
  50 Years (Ta ≤ 125 °C)

Packages

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.9 mm x 6.0 mm x 1.65 mm
TSSOP-B8	3.0 mm x 6.4 mm x 1.2 mm
MSOP8	2.9 mm x 4.0 mm x 0.9 mm

Applications

- Airbag
- ABS
- ECU

Typical Application Circuit

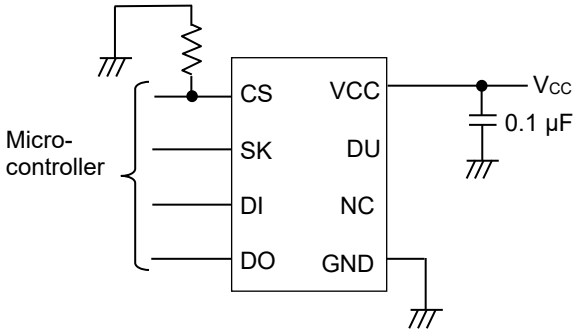

Figure 1. Typical Application Circuit

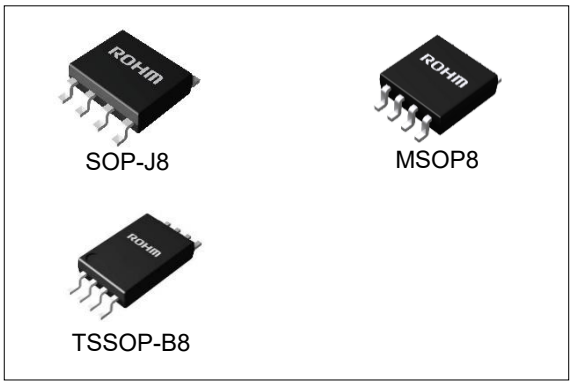

Figure 2

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Configurations

(TOP VIEW)

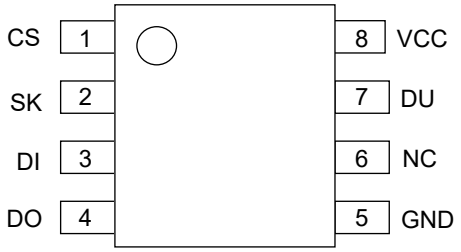

Figure 3. Pin Configuration
(SOP-J8,TSSOP-B8,MSOP8)

Pin Description

Pin No.	Pin Name	Input/Output	Descriptions
1	CS	Input	Chip select input
2	SK	Input	Serial clock input
3	DI	Input	Start bit, opcode, address, and serial data input
4	DO	Output	Serial data output, READY/$\overline{\text{BUSY}}$ status output
5	GND	-	All input/output reference voltage, 0 V
6	NC	-	Non connected*(Note 2)*
7	DU	-	Don't use*(Note 2)*
8	VCC	-	Power supply

(Note 2) Pin may be set to any of VCC or GND or leave as open.

Block Diagram

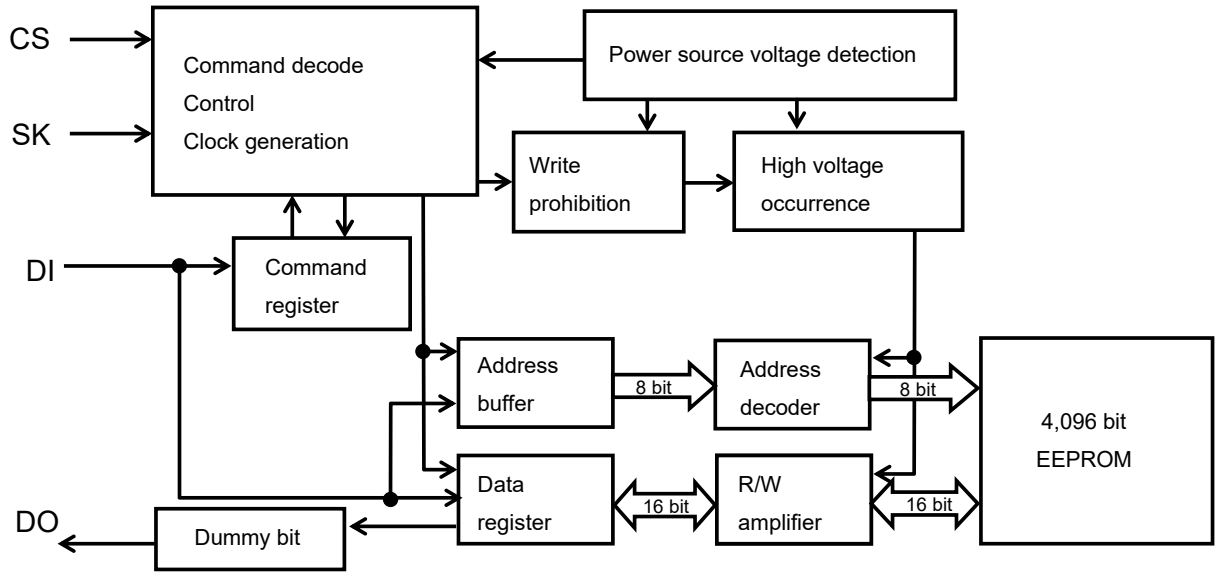

Figure 4. Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	Ta = 25 °C
Input Voltage/Output Voltage	-	-0.3 to V_{CC}+0.3	V	Ta = 25 °C. The maximum value of input voltage/output voltage is not over than 6.5 V.
Electro Static Discharge (Human Body Model)	V_{ESD}	-3000 to +3000	V	Ta = 25 °C
Maximum Output Low Current (DO)	I_{OLMAX}	10	mA	Ta = 25 °C
Maximum Output High Current (DO)	I_{OHMAX}	-10	mA	Ta = 25 °C
Maximum Junction Temperature	Tjmax	150	°C	-
Storage Temperature Range	Tstg	-65 to +150	°C	-

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	18	11	°C/W
TSSOP-B8				
Junction to Ambient	θ_{JA}	251.9	152.1	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	31	20	°C/W
MSOP8				
Junction to Ambient	θ_{JA}	284.1	135.4	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	21	11	°C/W

(Note 3) Based on JESD51-2A (Still-Air)
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

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Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.5	-	5.5	V
Ambient Operating Temperature	Ta	-40	-	+125	°C
Bypass Capacitor*(Note 7)*	C	0.1	-	-	µF

(Note 7) Connect a bypass capacitor between the IC's VCC and GND pin.

Memory Cell Characteristics (V_{CC} = 2.5 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Write Cycles*(Note 8)*	-	1,000,000	-	-	Times	Ta ≤ 85 °C
	-	500,000	-	-	Times	Ta ≤ 105 °C
	-	300,000	-	-	Times	Ta ≤ 125 °C
Data Retention*(Note 8)*	-	100	-	-	Years	Ta ≤ 25 °C
	-	60	-	-	Years	Ta ≤ 105 °C
	-	50	-	-	Years	Ta ≤ 125 °C

(Note 8) Not 100 % TESTED.

Electrical Characteristics (Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 2.5 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input High Voltage	V_{IH}	0.7V_{CC}	-	V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	+0.3V_{CC}	V	
Output Low Voltage 1	V_{OL1}	0	-	0.4	V	I_{OL} = 2.1 mA, 4.0 V ≤ V_{CC} ≤ 5.5 V
Output Low Voltage 2	V_{OL2}	0	-	0.2	V	I_{OL} = 100 µA
Output High Voltage 1	V_{OH1}	2.4	-	V_{CC}	V	I_{OH} = -0.4 mA, 4.0 V ≤ V_{CC} ≤ 5.5 V
Output High Voltage 2	V_{OH2}	V_{CC}-0.2	-	V_{CC}	V	I_{OH} = -100 µA
Input Leakage Current	I_{LI}	-10	-	+10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-10	-	+10	µA	V_{OUT} = 0 V to V_{CC}, CS = 0 V
Supply Current*(Note 9)*	I_{CC1}	-	-	3.0	mA	f_{SK} = 2 MHz, $t_{E/W}$ = 4.0 ms (WRITE)
	I_{CC2}	-	-	1.5	mA	f_{SK} = 2 MHz (READ)
	I_{CC3}	-	-	3.0	mA	f_{SK} = 2 MHz, $t_{E/W}$ = 4.0 ms (WRAL)
Standby Current	I_{SB}	-	-	10	µA	CS = 0 V, DO = OPEN

(Note 9) The average value during operation.

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AC Characteristics (Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC} = 2.5 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
SK Frequency	f_{SK}	-	-	2	MHz
SK HIGH Time	t_{SKH}	200	-	-	ns
SK LOW Time	t_{SKL}	200	-	-	ns
CS LOW Time	t_{CS}	200	-	-	ns
CS Setup Time	t_{CSS}	50	-	-	ns
DI Setup Time	t_{DIS}	50	-	-	ns
CS Hold Time	t_{CSH}	0	-	-	ns
DI Hold Time	t_{DIH}	50	-	-	ns
Data “1” Output Delay Time	t_{PD1}	-	-	200	ns
Data “0” Output Delay Time	t_{PD0}	-	-	200	ns
Time from CS to Output Establishment	t_{SV}	-	-	150	ns
Time from CS to High-Z	t_{DF}	-	-	150	ns
Write Cycle Time	$t_{E/W}$	-	-	4	ms

Input/Output Timing

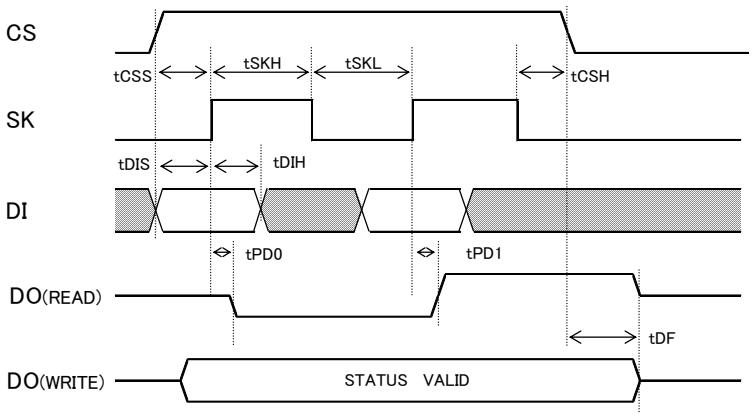

Figure 5. Input/Output Timing

・Data is taken from DI, in sync with the rise of SK.
・At READ command, data is outputted from DO in sync with the rise of SK.
・After WRITE command input, the status signal of WRITE (READY/$\overline{BUSY}$) can be monitored from DO by setting CS to HIGH after t_{CS}, from the fall of CS, and will display a valid status until the next command start bit is inputted. But, if CS is set to LOW, DO sets to High-Z state.
・To execute a series of commands, CS should be set to LOW once after completion of each command for internal circuit reset.

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Typical Performance Curves

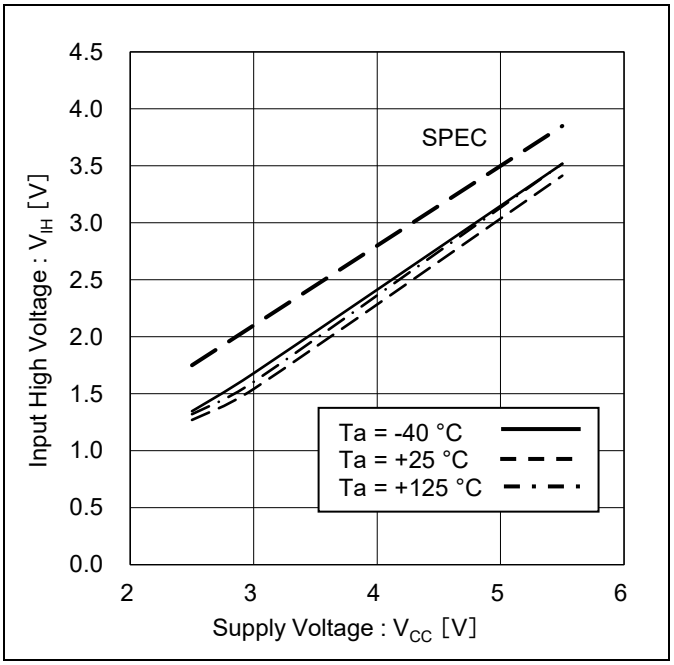

Figure 6. Input High Voltage vs Supply Voltage
(CS, SK, DI)

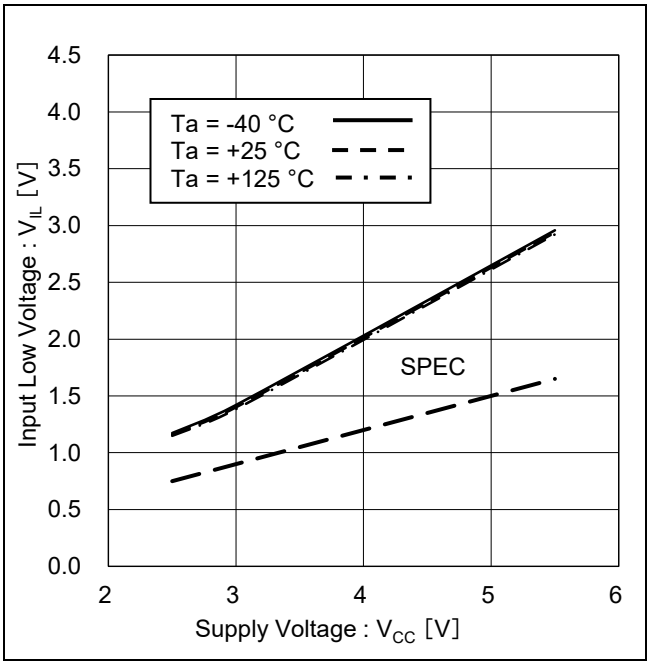

Figure 7. Input Low Voltage vs Supply Voltage
(CS, SK, DI)

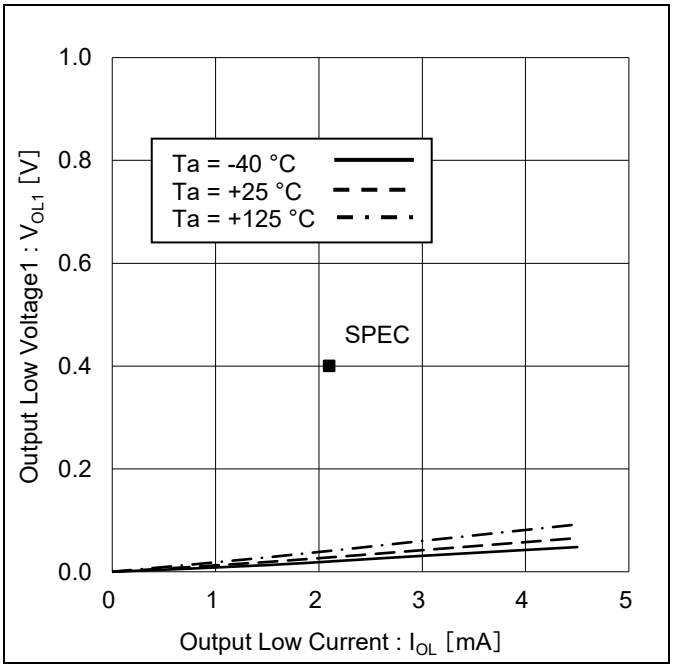

Figure 8. Output Low Voltage1 vs Output Low Current
(V_{CC} = 4.0 V)

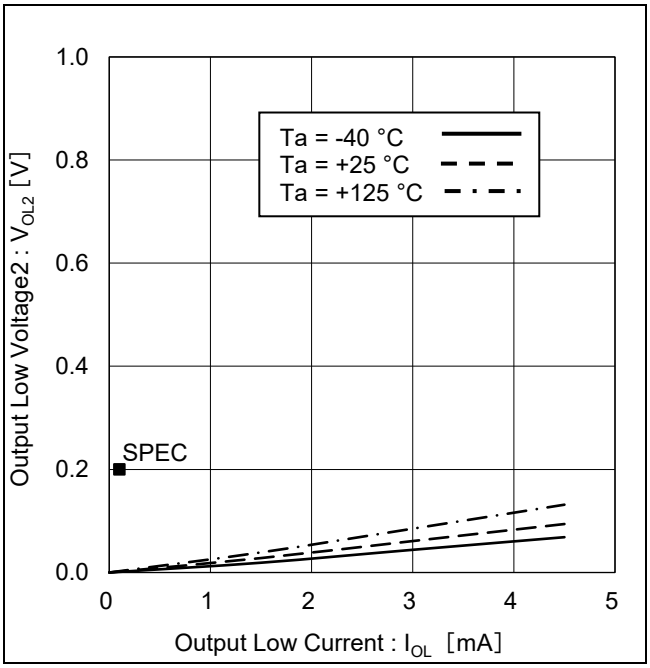

Figure 9. Output Low Voltage2 vs Output Low Current
(V_{CC} = 2.5 V)

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Typical Performance Curves - continued

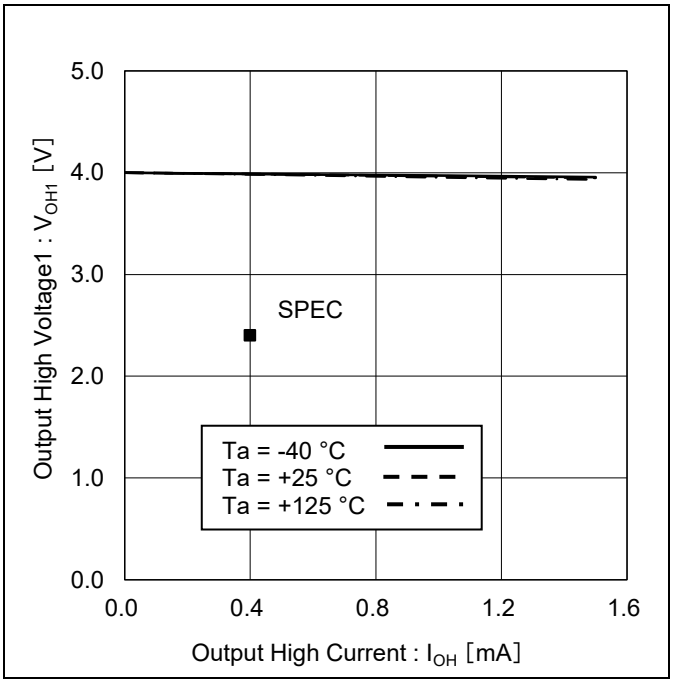

Figure 10. Output High Voltage1 vs Output High Current (V_{CC} = 4.0 V)

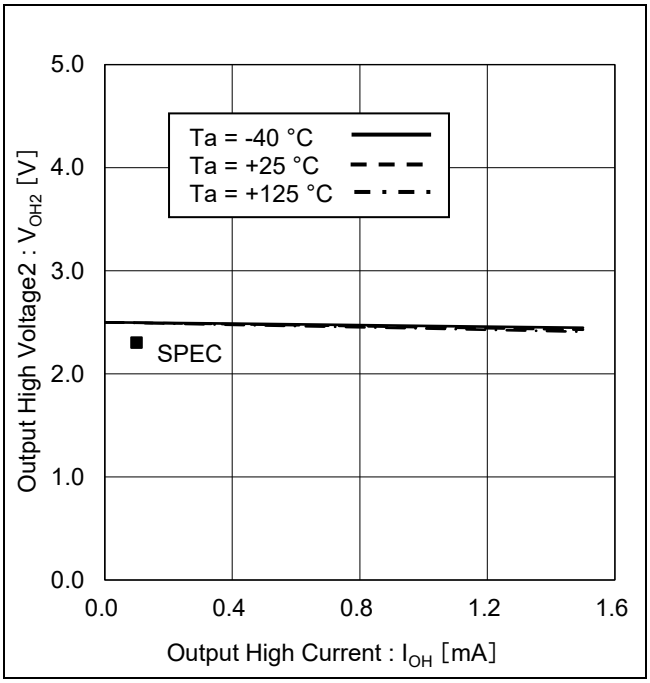

Figure 11. Output High Voltage2 vs Output High Current (V_{CC} = 2.5 V)

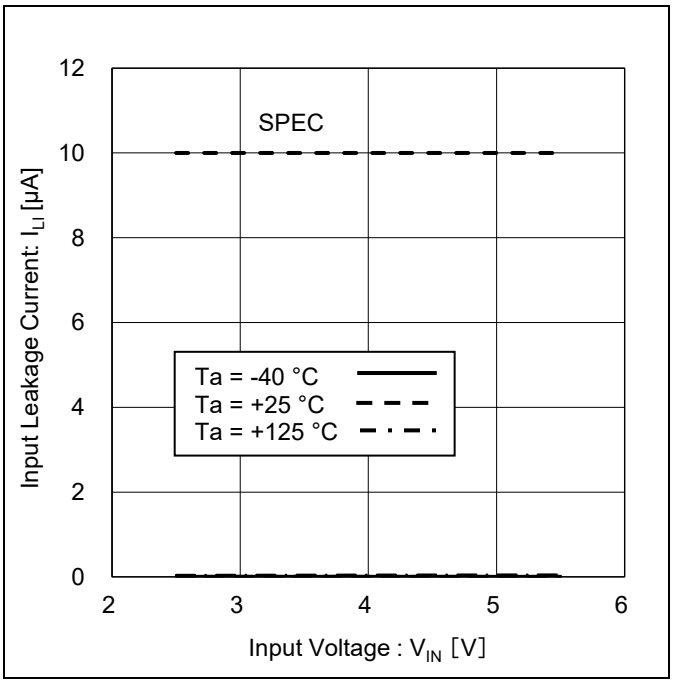

Figure 12. Input Leakage Current vs Input Voltage (CS, SK, DI)

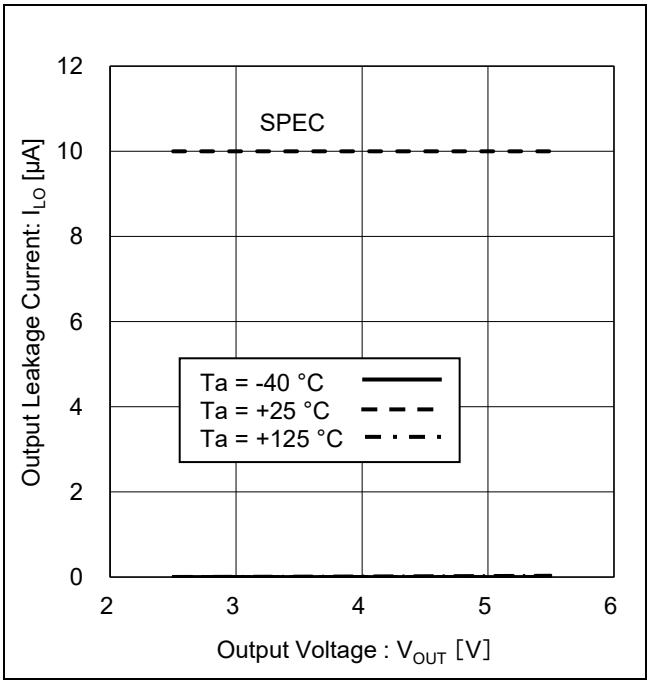

Figure 13. Output Leakage Current vs Output Voltage (DO)

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Typical Performance Curves - continued

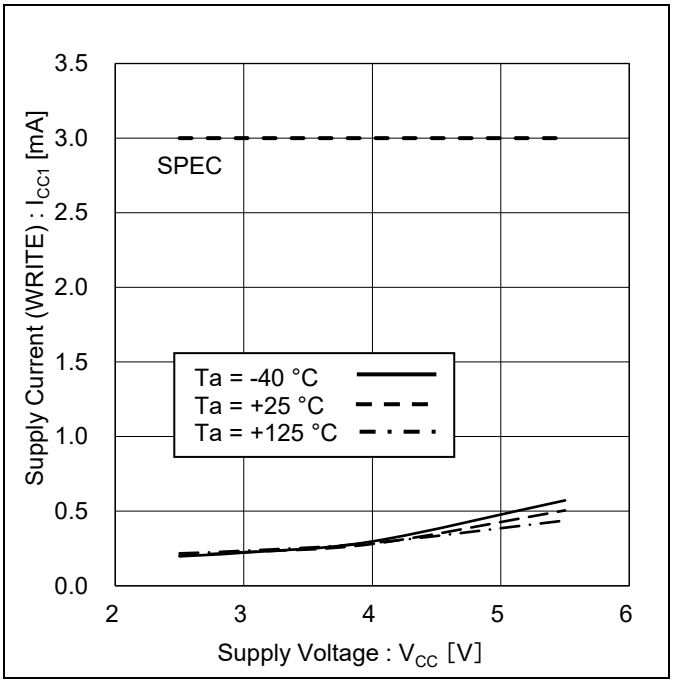

Figure 14. Supply Current (WRITE) vs Supply Voltage
(f_{SK} = 2 MHz)

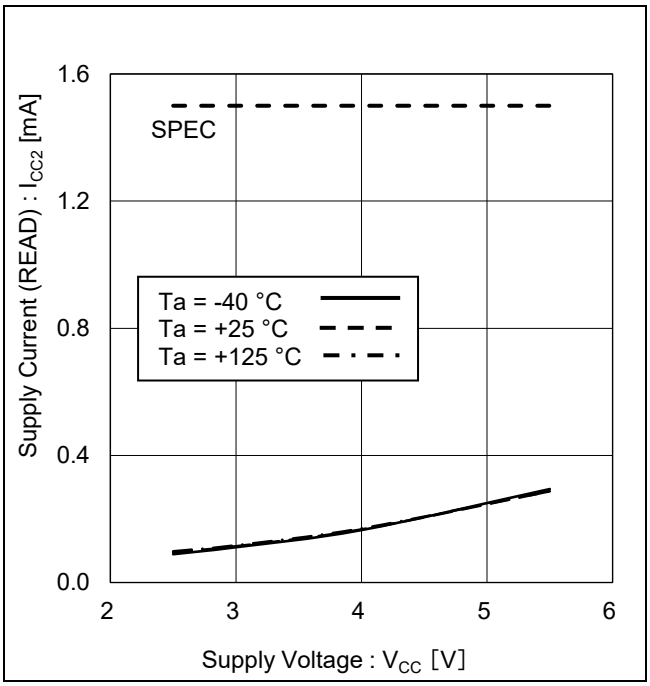

Figure 15. Supply Current (READ) vs Supply Voltage
(f_{SK} = 2 MHz)

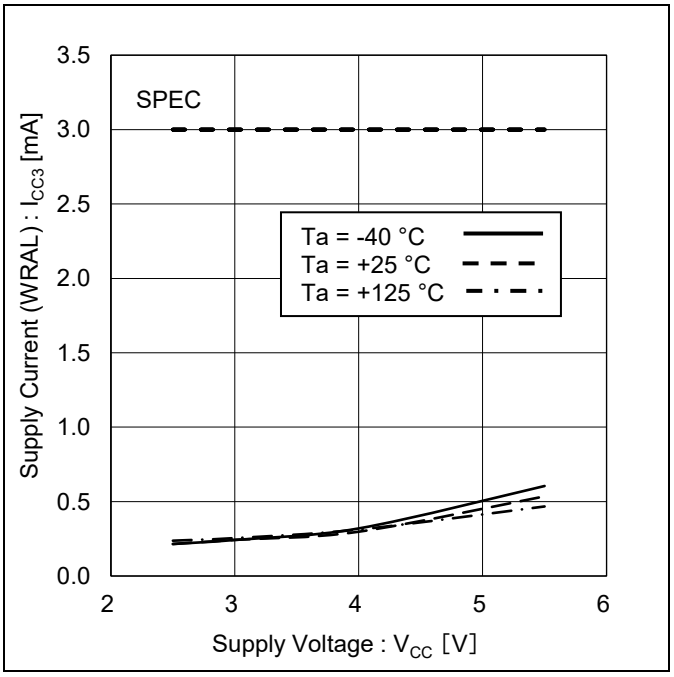

Figure 16. Supply Current (WRAL) vs Supply Voltage
(f_{SK} = 2 MHz)

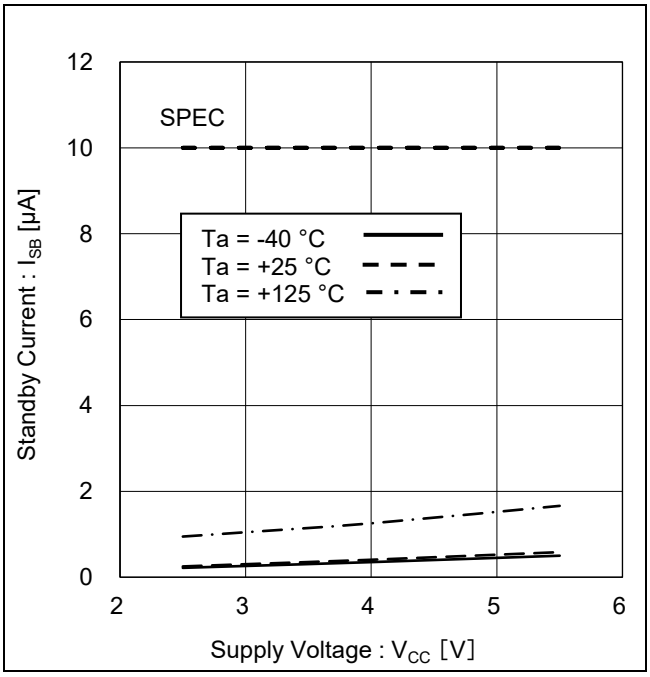

Figure 17. Standby Current vs Supply Voltage

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Typical Performance Curves - continued

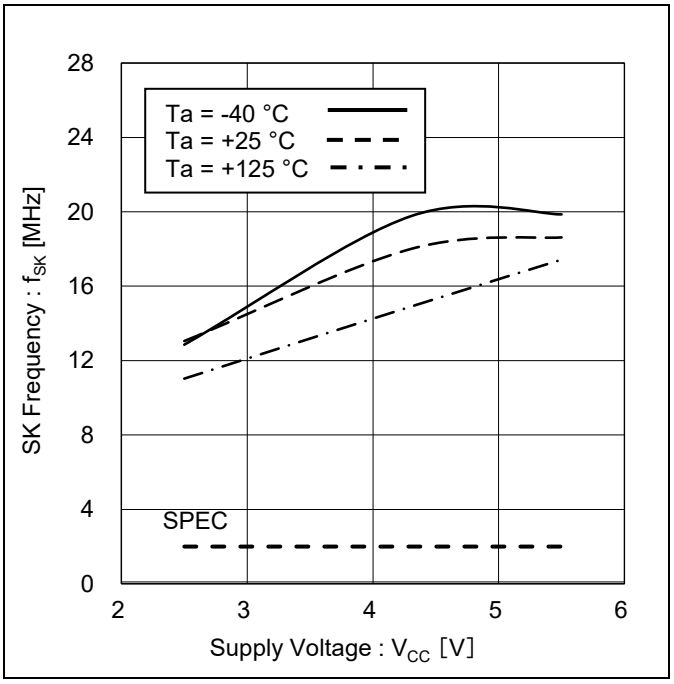

Figure 18. SK Frequency vs Supply Voltage

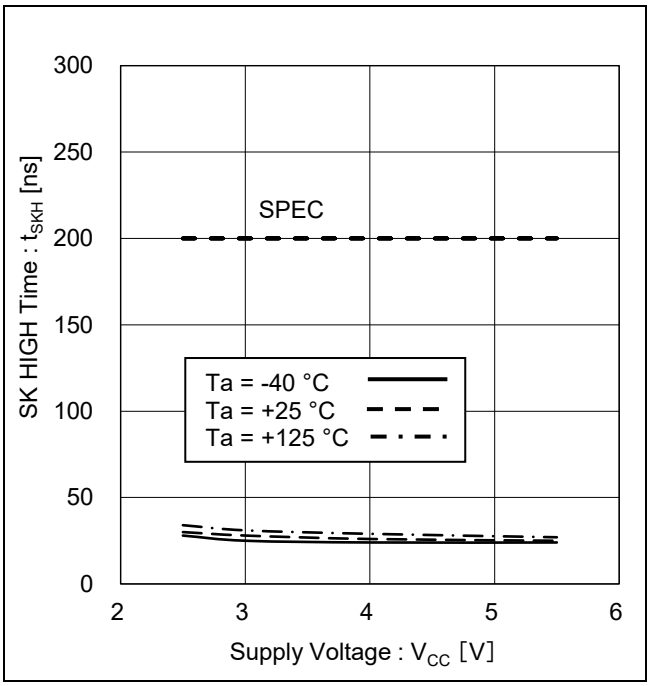

Figure 19. SK HIGH Time vs Supply Voltage

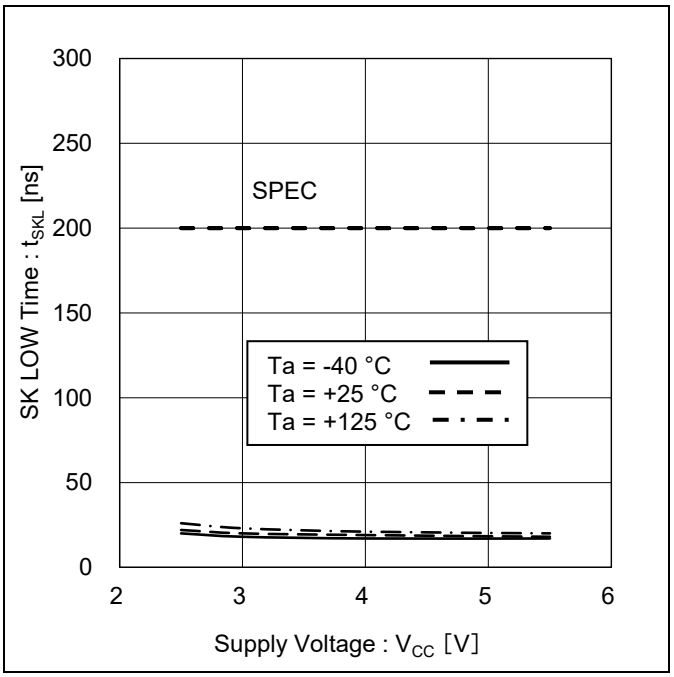

Figure 20. SK LOW Time vs Supply Voltage

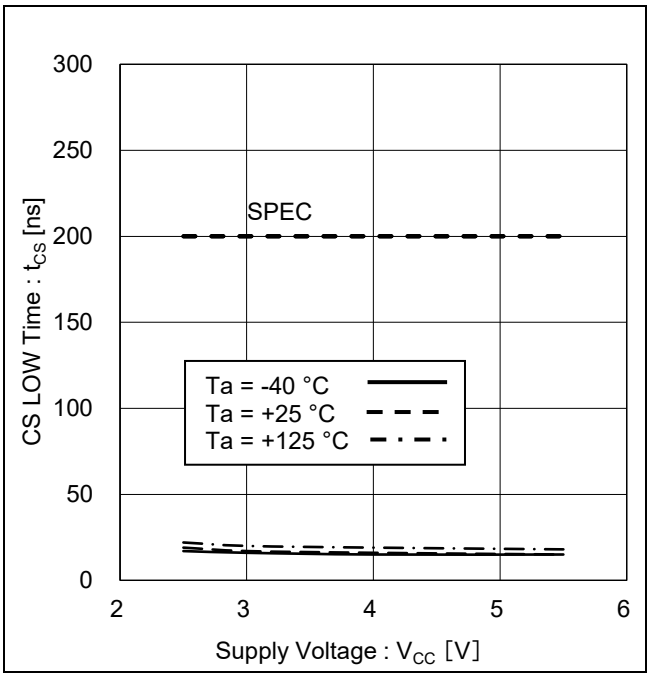

Figure 21. CS LOW Time vs Supply Voltage

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Typical Performance Curves - continued

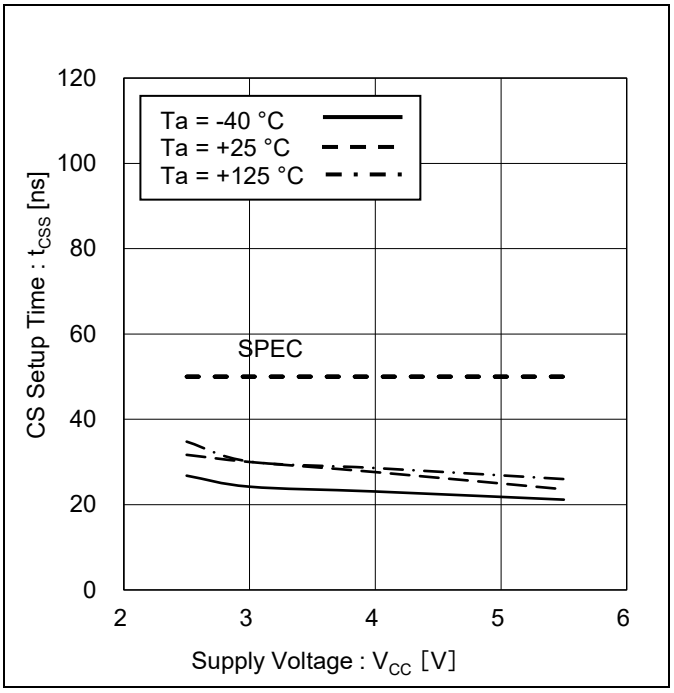

Figure 22. CS Setup Time vs Supply Voltage

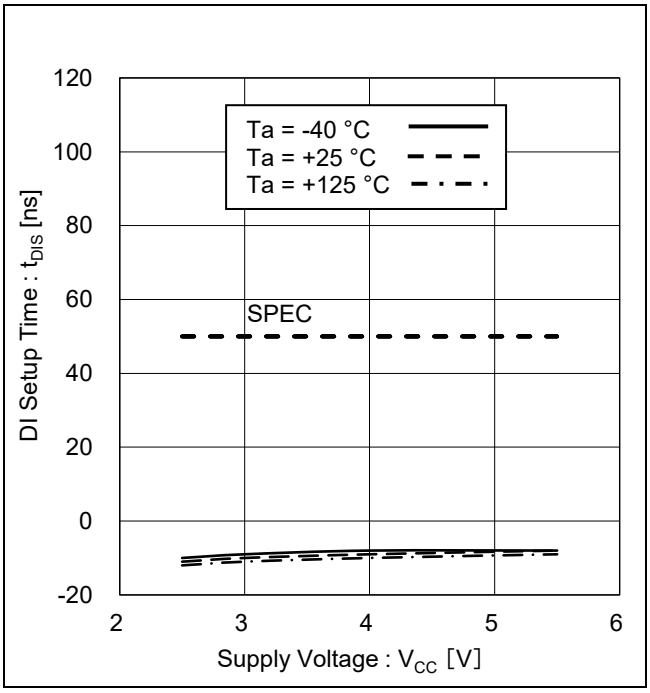

Figure 23. DI Setup Time vs Supply Voltage

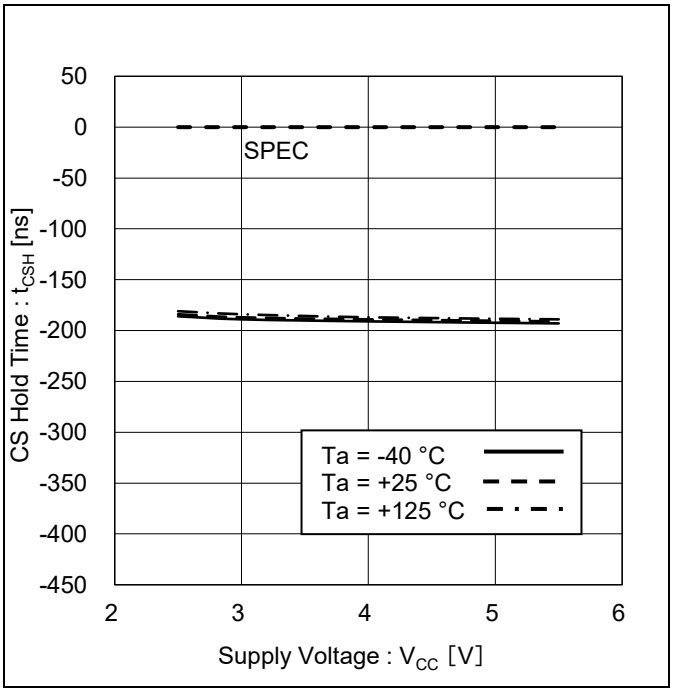

Figure 24. CS Hold Time vs Supply Voltage

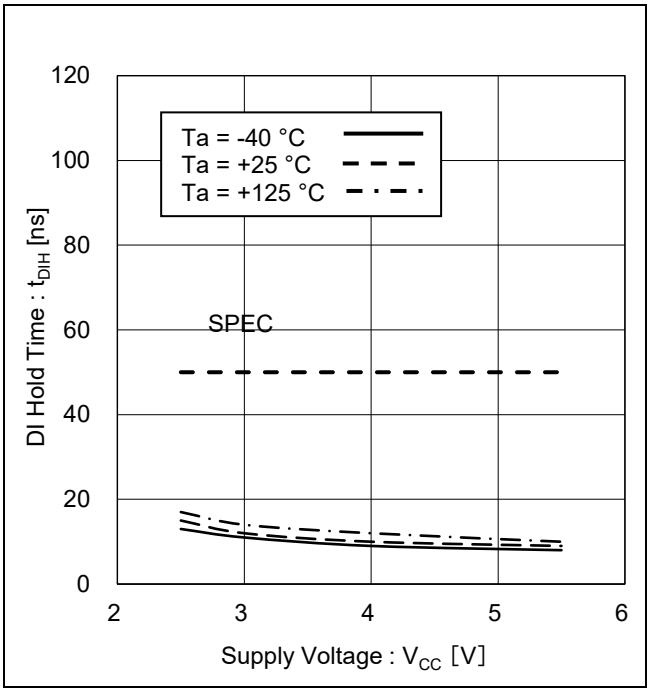

Figure 25. DI Hold Time vs Supply Voltage

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Typical Performance Curves - continued

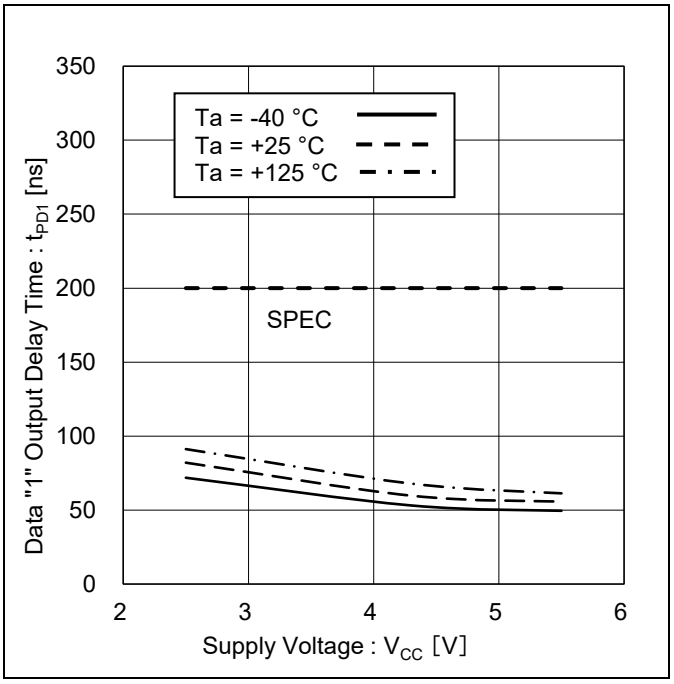

Figure 26. Data "1" Output Delay Time vs Supply Voltage

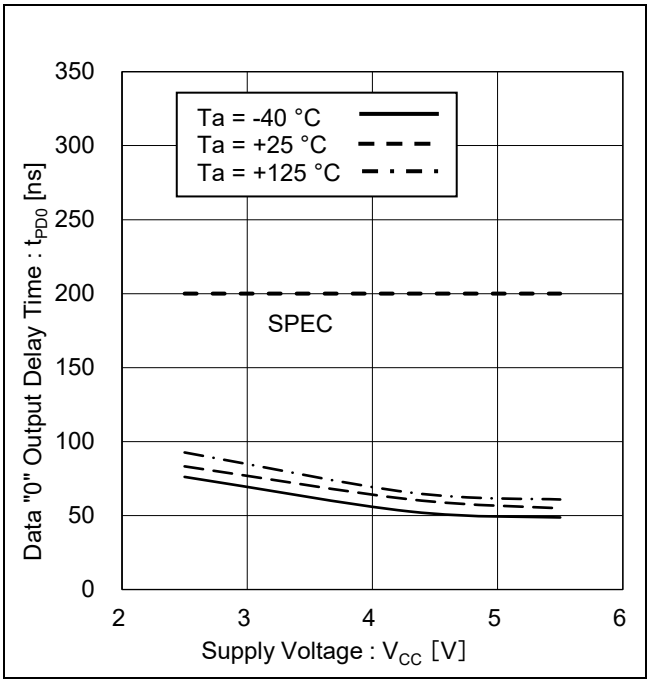

Figure 27. Data "0" Output Delay Time vs Supply Voltage

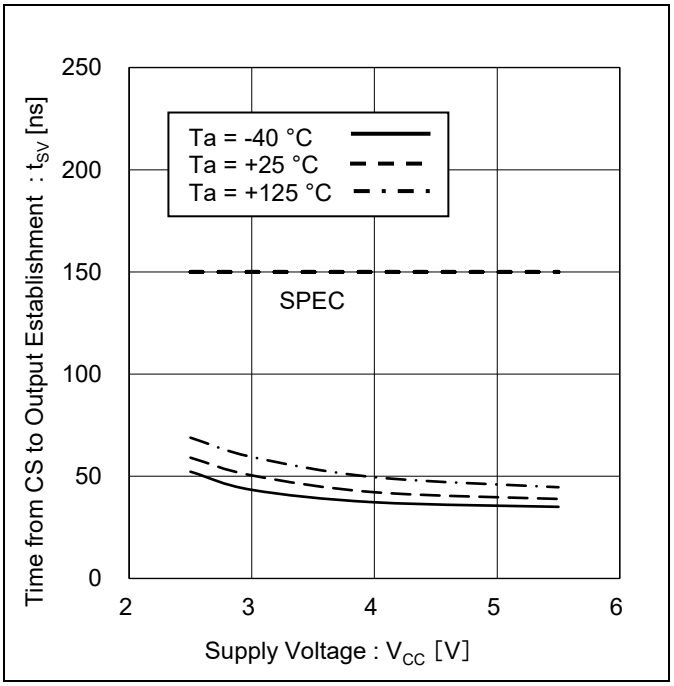

Figure 28. Time from CS to Output Establishment vs Supply Voltage

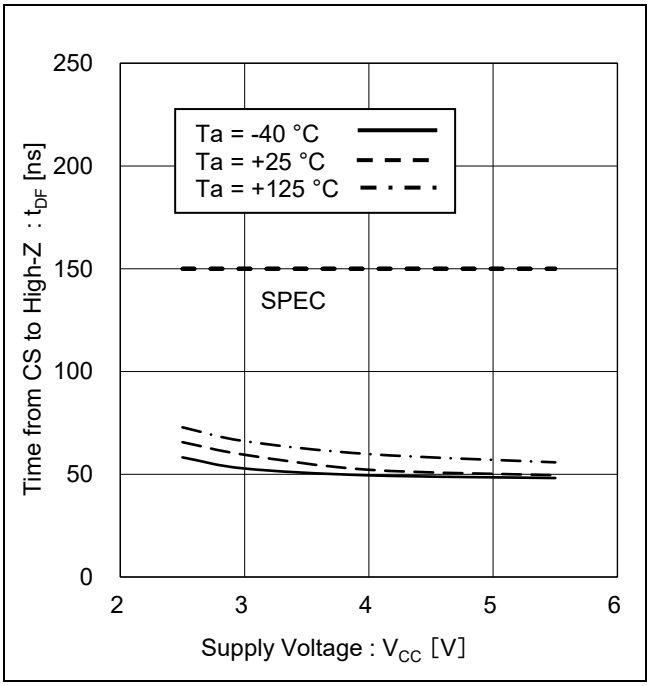

Figure 29. Time from CS to High-Z vs Supply Voltage

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Typical Performance Curves - continued

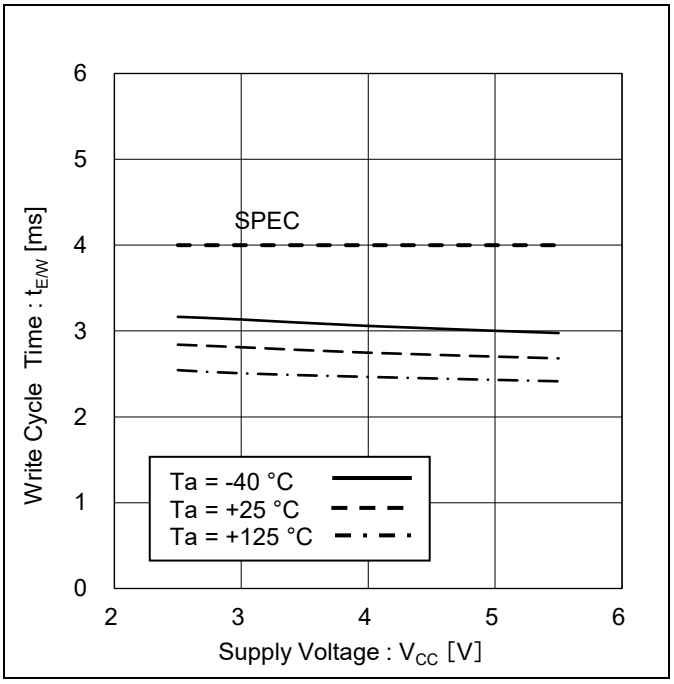

Figure 30. Write Cycle Time vs Supply Voltage

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Description of Operation

Communications of the MicroWire BUS are carried out by SK (serial clock), DI (serial data input), DO (serial data output), and CS (chip select) for device selection. In connecting one EEPROM to a microcontroller, connect it as shown in Figure 31-(a) or Figure 31-(b). And, when using the input and output common I/O port of the microcontroller, connect DI and DO via a resistor as shown in Figure 31-(b), wherein connection by 3 lines is possible. In case of using multiple EEPROM devices, refer to Figure 31-(c).

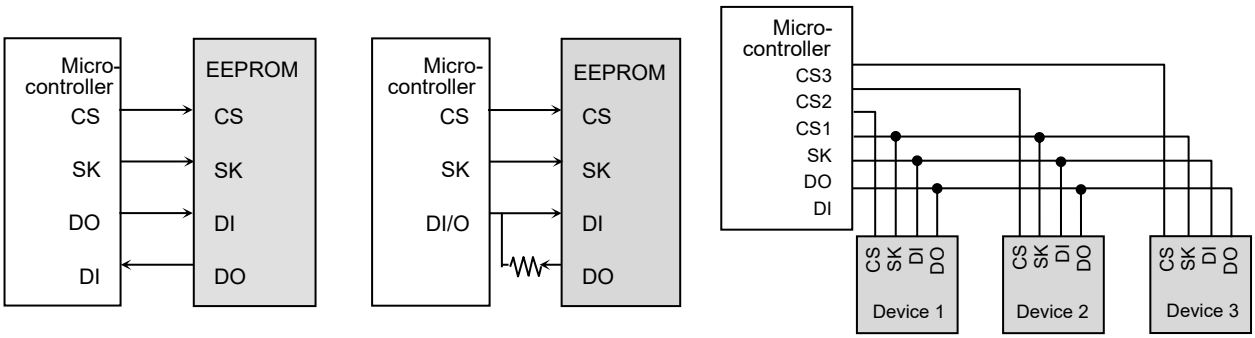

Figure 31-(a). Connection by 4 lines

Figure 31-(b). Connection by 3 lines

Figure 31-(c). Connection example of multiple devices

Figure 31. Connection Methods with Microcontroller

Communications of the MicroWire BUS are started by the first “1” input after the rise of CS. This input is called the “Start Bit”. After input of the start bit, the “Opcode”, Address, and Data are then inputted consecutively. Address and Data are all inputted with MSB first. All “0” signal inputs after the rise of CS up to the start bit is ignored. Therefore, if there is a limitation in the bit width of PIO of the microcontroller, it is possible to input “0” before the start bit to control the bit width.

Command Mode

Command	Start bit	Op code	Address	Data
Read (READ) *1	1	10	A7,A6,A5,A4,A3,A2,A1,A0	D15 to D0 (READ DATA)
Write enable (WEN)	1	00	1 1 * * * * * *	-
Write (WRITE) *2	1	01	A7,A6,A5,A4,A3,A2,A1,A0	D15 to D0 (WRITE DATA)
Write all (WRAL) *3	1	00	0 1 * * * * * B0	D15 to D0 (WRITE DATA)
Write disable (WDS)	1	00	0 0 * * * * * *	-

・Input the address and the data in MSB-first order.
・As for *, input either V_{IH} or V_{IL}.

*Start bit
Acceptance of all the commands of this IC starts at recognition of the start bit. The “Start Bit” means the first “1” input after the rise of CS.

*1 For READ, after setting the command, the data output of the selected address starts. Then, in a sequential order of addresses, the data of the next address will be output, and will continuously output data of succeeding addresses with the use of a continuous SK clock input. (Auto-Increment Function)
*2 When the WRITE command is executed, the previous data written in the selected memory cell is automatically deleted first, then the input data is written next.
*3 For the Write all command, data written in memory cell of the areas designated by B0 are automatically deleted, and input data is written in bulk.

Write All Area

B0	Write area
0	000h to 07Fh
1	080h to 0FFh

・The write all command writes data in bulk in 2 Kbit unit. The write area can be selected up to 1 bit. Confirm on the left side the settings and write areas of B0.

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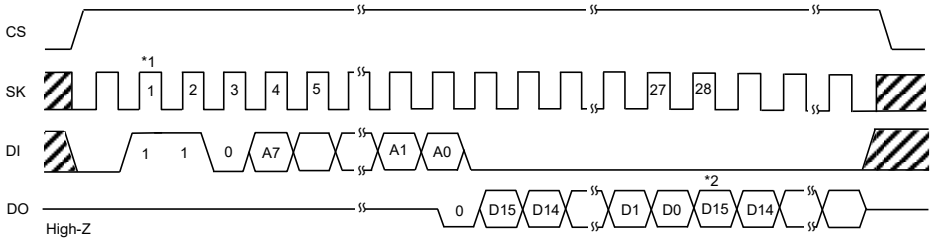
Timing Chart

1. Read Cycle (READ)



*1 Start bit
When data "1" is input for the first time after the rise of CS, this is recognized as a start bit. And, even if multiple "0" are input after the rise of CS, the first "1" input will still be recognized as the start bit, and the following operation starts. This is common to all the commands that will be discussed hereafter.
*2 The succeeding address' data output (Auto-Increment Function)

Figure 32. Read Cycle

When the READ command is recognized, the data (16 bit) of the selected address is output to serial. At that time, "0" (dummy bit) is output first, in sync with address bit A0 and with the rise of SK. After which, the main data is output in sync with the rise of SK. This IC has Address Auto Increment Function available only for READ command. wherein after executing READ command on the first selected address, the data of the next address is read. And this will continue in a sequential order of addresses with the use of a continuous SK clock input, and by keeping CS at HIGH during auto-increment.

2. Write Cycle (WRITE)

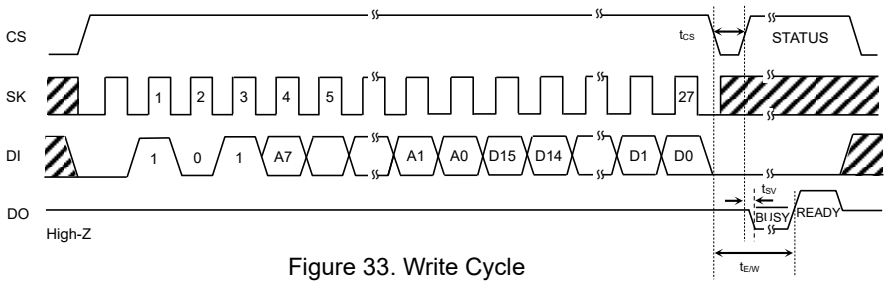


Figure 33. Write Cycle

In this command, input 16 bit data (D15 to D0) is written to a designated address (A7 to A0). The actual write starts from the fall of CS, after D0 is sampled with SK clock (27 th clock from the start bit input), to the rise of the 28 th clock. When STATUS is not detected (CS = LOW fixed), WRITE time is 4 ms (Max) in conformity with $t_{E/W}$. And when STATUS is detected (CS = HIGH), all commands are not accepted for areas where LOW (BUSY) is output from DO. Therefore, do not input any command. Write is not started if CS starts to fall after the rise of the 28 th clock.
Note: Take t_{SKH} or more from the rise of the 27 th clock to the fall of CS.

3. Write All Cycle (WRAL)

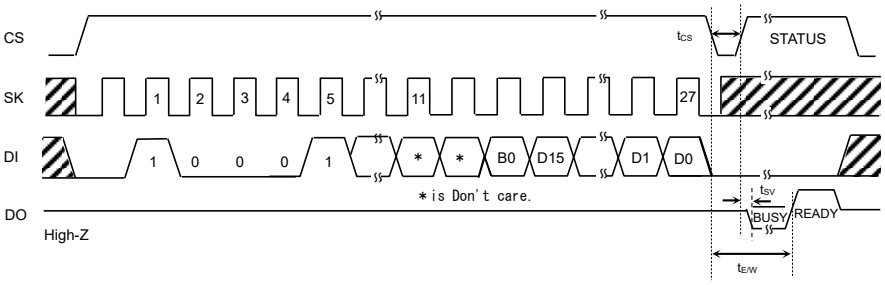


Figure 34. Write All Cycle

In this command, input 16 bit data is written simultaneously to designated block. Data is written in bulk, rather than being written sequentially one word at a time, with a write time of only 4 ms (Max) in conformity with $t_{E/W}$. When writing data to all addresses, designate each block by B0, and execute write. Write time is Max 4 ms. The actual write starts from the fall of CS, after D0 is sampled with SK clock (27 th clock from the start bit input), to the rise of the 28 th clock. If CS falls after any clock input following the rising edge of the 28 th clock, the command is canceled and no write operation is performed.
Note: Take t_{SKH} or more from the rise of the 27 th clock to the fall of CS.

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Timing Chart - continued

4. Write Enable (WEN)/Disable (WDS) Cycle

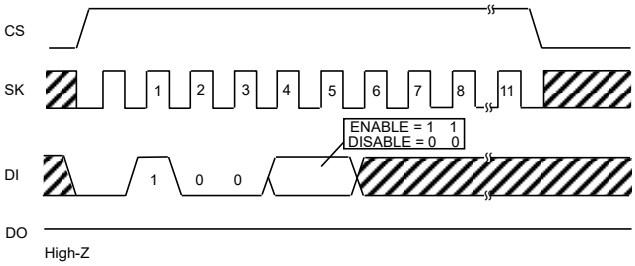

Figure 35. Write Enable (WEN)/Disable (WDS) Cycle

At power on, this IC is in Write Disable status by the internal RESET circuit. Before executing the WRITE command, it is necessary to execute the Write Enable Command first. And, once this command is executed, writing is valid until the Write Disable Command is executed or the power is turned off. However, the READ command is valid regardless of whether Write Enable/Disable command is executed. Input to SK after 6 clocks of this command is available by either HIGH or LOW, but be sure to input it. When the Write Enable Command is executed after power on, Write Enable status gets in. When the Write Disable command is executed then, the IC gets in Write Disable Status the same as at power on, and then the WRITE command is canceled thereafter in software manner. However, the READ command is still executable. In Write Enable status, even when the WRITE command is input by mistake, writing will still start. To prevent such a mistake, it is recommended to execute the Write Disable command after the completion of each WRITE execution.

Method to Cancel Each Command

1. READ
   Method to cancel : cancel by CS = LOW

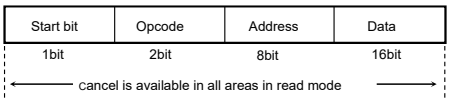

Figure 36. READ Cancel Available Timing

2. WRITE, WRAL
   a: From start bit to 27 th clock rise
   Cancel by CS = LOW.
   b: 27 th clock rise and after
   Cancellation is not available by any means.
   If V_{CC} is turned OFF in this area, designated address data is not guaranteed, therefore write once again.
   c: 28 th clock rise and after
   Cancel by CS = LOW.
   However, when write is started in b area (CS is ended), cancellation is not available by any means.
   And when SK clock is input continuously, cancellation is not available.

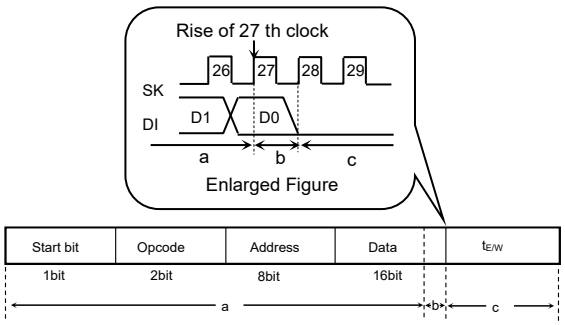

Figure 37. WRITE, WRAL Cancel Available Timing

*1) If V_{CC} is turned OFF in this area, designated address data is not guaranteed. Therefore, it is recommended to execute WRITE once again.
*2) If CS is started at the same timing as that of the SK rise, write execution/cancel becomes unstable. Therefore, it is recommended to bring CS to LOW in SK = LOW area. As for SK rise, recommend timing is t_{SKH} or more.

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Application Examples

1. READY/$\overline{\text{BUSY}}$ Status Display (DO Pin)
   This display outputs the internal status signal. When CS rises after t_{CS} (Min 200 ns) from CS fall after write command input, HIGH or LOW is output.

   R/$\overline{\text{B}}$ display = LOW ($\overline{\text{BUSY}}$) = write in progress
   (DO Status)
   After the timer circuit in the IC operates and creates the period of $t_{E/W}$, this timer circuit completes automatically. And writing to the memory cell is performed in the period of $t_{E/W}$, and during this period, other commands are not accepted.

   R/$\overline{\text{B}}$ display = HIGH (READY) = command wait status
   (DO Status)
   The memory cell write operation is completed, and the next command is accepted even within $t_{E/W}$ (Max 4 ms). Therefore, CS = HIGH in the period of $t_{E/W}$, and when signals are input to SK and DI, malfunction may occur. Therefore, set DI = LOW in the area CS = HIGH. (Especially, in the case of shared input port, attention is required.)

   *Do not input any command while status signal is output. Command input in $\overline{\text{BUSY}}$ area is canceled, but command input in READY area is accepted. Therefore, status READY output is canceled, and malfunction and write error may be made.

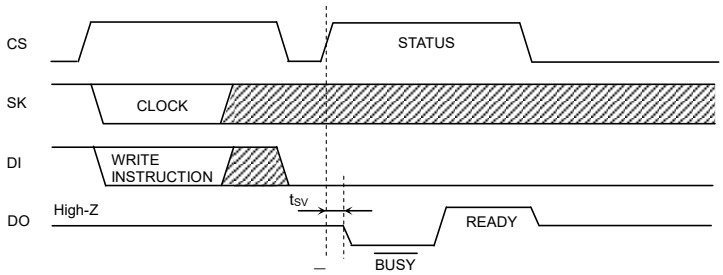
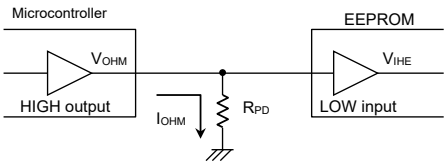


Figure 38. R/$\overline{\text{B}}$ Status Output Timing Chart

2. Pull Down CS
   By making CS = LOW at power ON/OFF, malfunction and write error are prevented. Select an appropriate pull down resistance value from microcontroller's V_{OH}, I_{OH} and this IC's V_{IH} characteristics.



V_{IHE} : EEPROM V_{IH} specifications
V_{OHM} : Microcontroller V_{OH} specifications
I_{OHM} : Microcontroller I_{OH} specifications

Figure 39. CS Pull Down Resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad (1)$$

$$V_{OHM} \geq V_{IHE} \quad (2)$$

Example) When V_{CC} = 5 V, V_{IHE} = V_{CC} x 0.7 V, V_{OHM} = 4.0 V, I_{OHM} = 2 mA, from equation (1),

$$R_{PD} \geq \frac{4.0}{2 \times 10^{-3}}$$

$$R_{PD} \geq 2.0 \ [\text{k}\Omega]$$

With the value of R_{PD} satisfying the equation above, V_{OHM} becomes 4.0 V or more, and with V_{IHE} (= 3.5 V), equation (2) is also satisfied.

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Application Examples - continued

3. Pull Up and Pull Down of DO

DO is available for both pull up and pull down. DO output is High-Z except during data output in a READ command and during READY/$\overline{\text{BUSY}}$ output timing in WRITE command. When malfunction occurs at High-Z input of the microcontroller port connected to DO, it is necessary to pull down or pull up DO. When there is no influence upon the microcontroller actions, DO may be left OPEN. If DO is OPEN during a transition of output from $\overline{\text{BUSY}}$ to READY status, and at an instance where CS = HIGH, SK = HIGH, DI = HIGH, EEPROM recognizes this as a start bit, resets READY output, and sets DO = High-Z. Therefore, READY signal cannot be detected. To avoid such output, pull up the DO pin for improvement.

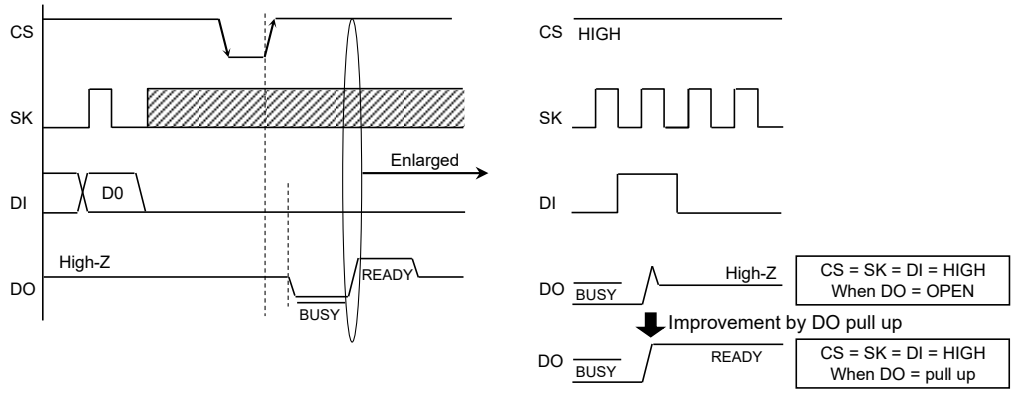
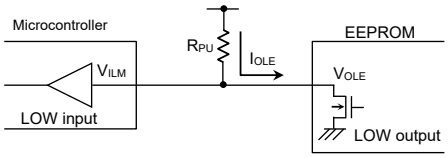


Figure 40. READY Output Timing at DO = OPEN

The values of the DO pull-up resistance R_{PU} and pull-down resistance R_{PD} should be selected appropriately according to the microcontroller's V_{IH} and V_{IL} specifications and the V_{OH}, I_{OH}, V_{OL}, and I_{OL} characteristics of this IC.



V_{OLE} : EEPROM V_{OL} specifications
V_{ILM} : Microcontroller V_{IL} specifications
I_{OLE} : Microcontroller I_{OL} specifications

Figure 41. DO Pull up Resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLE}}{I_{OLE}} \quad (3)$$

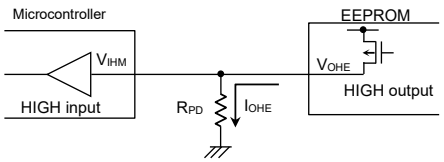
$$V_{OLE} \leq V_{ILM} \quad (4)$$

Example) When V_{CC} = 5 V, V_{OLE} = 0.4 V, I_{OLE} = 2.1 mA, V_{ILM} = 0.8 V, from the equation (3),

$$R_{PU} \geq \frac{5 - 0.4}{2.1 \times 10^{-3}}$$

$$R_{PU} \geq 2.2 \ [\text{k}\Omega]$$

With the value of R_{PU} to satisfy the above equation, V_{OLE} becomes 0.4 V or below, and with V_{ILM} (= 0.8 V), the equation (4) is also satisfied.



V_{OHE} : EEPROM V_{OH} specifications
I_{OHE} : EEPROM I_{OH} specifications
V_{IHM} : Microcontroller V_{IH} specifications

Figure 42. DO Pull down Resistance

$$R_{PD} \geq \frac{V_{OHE}}{I_{OHE}} \quad (5)$$

$$V_{OHE} \geq V_{IHM} \quad (6)$$

Example) When V_{CC} = 5 V, V_{OHE} = V_{CC} - 0.2 V, I_{OHE} = 0.1 mA, V_{IHM} = V_{CC} x 0.7 V from the equation (5)

$$R_{PD} \geq \frac{5 - 0.2}{0.1 \times 10^{-3}}$$

$$R_{PD} \geq 48 \ [\text{k}\Omega]$$

With the value of R_{PD} to satisfy the above equation, V_{OHE} becomes 4.8 V or more, and with V_{IHM} (= 3.5 V) the equation (6) is also satisfied.

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Application Examples - continued

4. When to Directly Connect DI and DO

This IC has independent input pin DI and output pin DO, signals are handled separately on timing chart. But by inserting a resistance R between the DI and DO pins, it is possible to carry out control by only 1 control line.

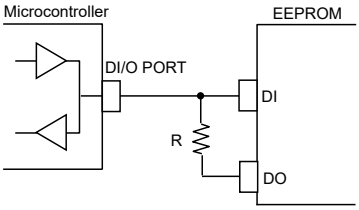

Figure 43. DI, DO Control Line Common Connection

4.1 Data collision of microcontroller DI/O output and DO output and feedback of DO output to DI input.

Drive from the microcontroller DI/O output to DI input on I/O timing, and signal output from DO output occur at the same time in the following two cases.

4.1.1 1 clock cycle to take in A0 address data at read command

Dummy bit “0” is output to the DO pin. When address data A0 = “1” input, through current route occurs.

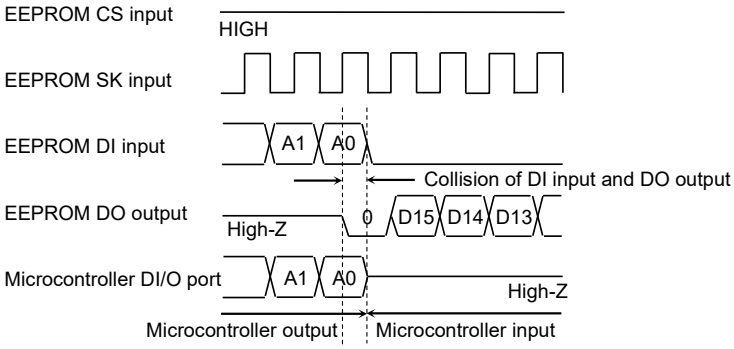

Figure 44. Collision Timing at Read Data Output at DI, DO Direct Connection

4.1.2 Timing of CS = HIGH after write command. The DO pin in READY/$\overline{\text{BUSY}}$ output

When the next start bit input is recognized, High-Z gets in. Especially, at command input after write, when CS input is rised with microcontroller DI/O output LOW, READY output HIGH is output from the DO pin, and through current route occurs. Feedback input at timing of these 4.1.1 and 4.1.2 does not cause disorder in basic operations, if resistance R is inserted.

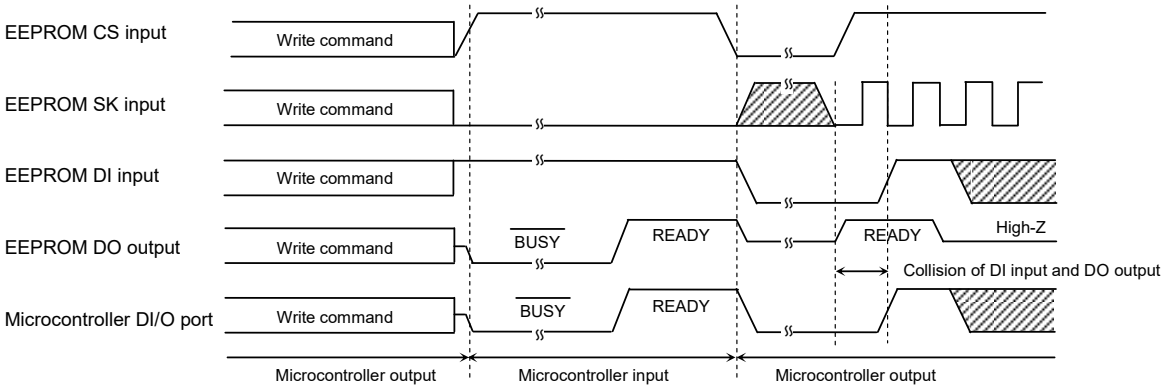

Figure 45. Collision Timing at DI, DO Direct Connection During Write Operation

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Application Examples - continued

4.2 Selection of resistance value R

The resistance R becomes through current limit resistance at data collision. When through current flows, noises of power source line and instantaneous stop of power source may occur. When allowable through current is defined as I, the following relation should be satisfied. Determine allowable current amount in consideration of impedance and so forth of power source line in set. And insert resistance R, and set the value R to satisfy EEPROM input level V_{IH}/V_{IL}, even under influence of voltage decline owing to leak current and so forth. Insertion of R will not cause any influence upon basic operations.

4.2.1 Address Data A0 = "1" Input, dummy bit "0" Output Timing

(When microcontroller DI/O output is HIGH, EEPROM DO outputs LOW, and HIGH is input to DI)

- Make the through current to EEPROM 10 mA or below.
- See to it that the input level V_{IH} of EEPROM should satisfy the following.

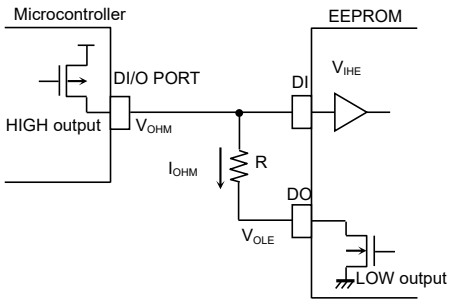

Figure 46. Circuit at DI, DO Direct Connection (Microcontroller DI/O HIGH output, EEPROM LOW output)

Condition

$$V_{IHE} \leq V_{OHM}$$

$$V_{IHE} \leq I_{OHM} \times R + V_{OLE}$$

At this moment, if V_{OLE} = 0 V,

$$V_{IHE} \leq I_{OHM} \times R$$

$$R \geq \frac{V_{IHE}}{I_{OHM}} \qquad (7)$$

- V_{IHE} : EEPROM V_{IH} specifications
- V_{OLE} : EEPROM V_{OL} specifications
- V_{OHM} : Microcontroller V_{OH} specifications
- I_{OHM} : Microcontroller I_{OH} specifications

4.2.2 DO Status READY Output Timing

(When the microcontroller DI/O is LOW, EEPROM DO outputs HIGH, and LOW is input to DI)

- Set the EEPROM input level V_{IL} so as to satisfy the following.

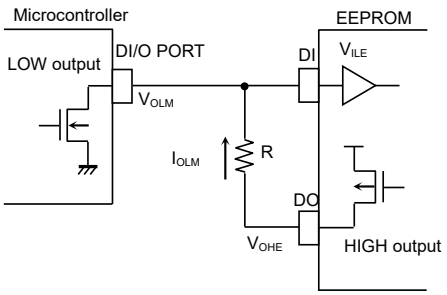

Figure 47. Circuit at DI, DO Direct Connection (Microcontroller DI/O LOW output, EEPROM HIGH output)

Condition

$$V_{ILE} \geq V_{OLM}$$

$$V_{ILE} \geq V_{OHE} - I_{OLM} \times R$$

As this moment, if V_{OHE} = V_{CC},

$$V_{ILE} \geq V_{CC} - I_{OLM} \times R$$

$$R \geq \frac{V_{CC} - V_{ILE}}{I_{OLM}} \qquad (8)$$

- V_{ILE} : EEPROM V_{IL} specifications
- V_{OHE} : EEPROM V_{OH} specifications
- V_{OLM} : Microcontroller V_{OL} specifications
- I_{OLM} : Microcontroller I_{OL} specifications

Example) When V_{CC} = 5 V, V_{IHE} = V_{CC} x 0.7 V, V_{ILE} = V_{CC} x 0.3 V, I_{OHM} = 0.4 mA, I_{OLM} = 2.1 mA,

From the equation (7),

$$R \geq \frac{V_{IHE}}{I_{OHM}}$$

$$R \geq \frac{3.5}{0.4 \times 10^{-3}}$$

$$R \geq 8.75\ [\mathrm{k\Omega}] \qquad (9)$$

From the equation (8),

$$R \geq \frac{V_{CC} - V_{ILE}}{I_{OLM}}$$

$$R \geq \frac{5 - 1.5}{2.1 \times 10^{-3}}$$

$$R \geq 1.67\ [\mathrm{k\Omega}] \qquad (10)$$

Therefore, from the equations (9) and (10),

$$R \geq 8.75\ [\mathrm{k\Omega}]$$

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I/O Equivalence Circuits

1. Input (CS)

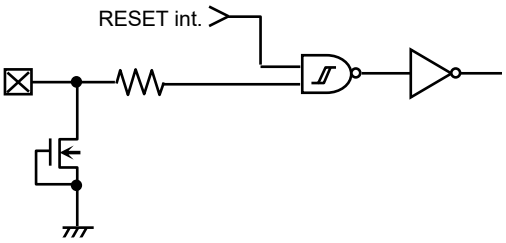

Figure 48. Input Equivalent Circuit (CS)

2. Input (SK)

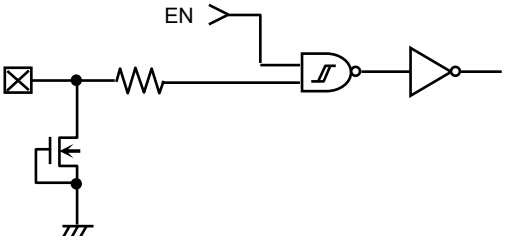

Figure 49. Input Equivalent Circuit (SK)

3. Input (DI)

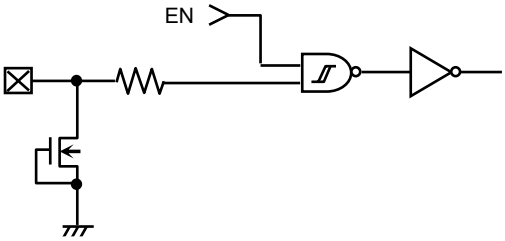

Figure 50. Input Equivalent Circuit (DI)

4. Output (DO)

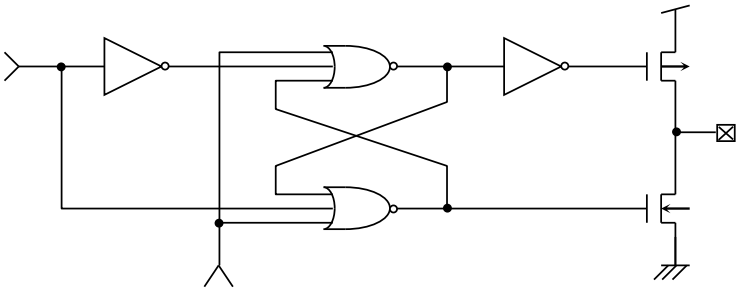

Figure 51. Output Equivalent Circuit (DO)

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Caution on Power-Up Conditions

At power-up, as the V_{CC} rises, the IC's internal circuits may go through unstable low voltage area, making the IC's internal circuit not completely reset, hence, malfunction like miswriting and misread may occur. To prevent it, this IC is equipped with Power-on Reset circuit. In order to ensure its operation, at power-up, please observe the conditions below. In addition, set the power supply rise so that the supply voltage constantly increases from V_{BOT} to V_{CC} level. Furthermore, t_{INIT} is the time from the power become stable to the start of the first command input.

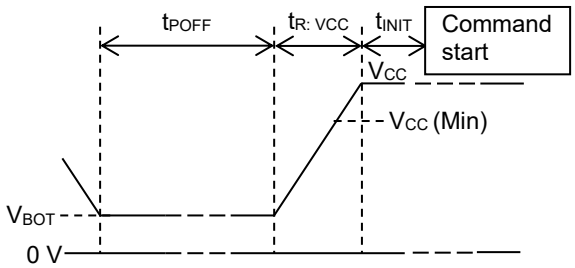

Figure 52. Rise Waveform Diagram

Power-Up Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage at Power OFF	V_{BOT}	-	-	0.3	V
Power OFF Time*(Note 10)*	t_{POFF}	1	-	-	ms
Initialize Time*(Note 10)*	t_{INIT}	0.1	-	-	ms
Supply Voltage Rising Time*(Note 10)*	$t_{R: VCC}$	0.001	-	100	ms

(Note 10) Not 100 % TESTED.

At power ON/OFF, set CS = LOW (= 0 V).
When CS is HIGH, this IC gets in input accept status (active). At power ON, set CS LOW to prevent malfunction from noise. (When CS is in LOW status, all inputs are canceled.) At power decline low power status may prevail. Therefore, at power OFF, set CS LOW to prevent malfunction from noise.

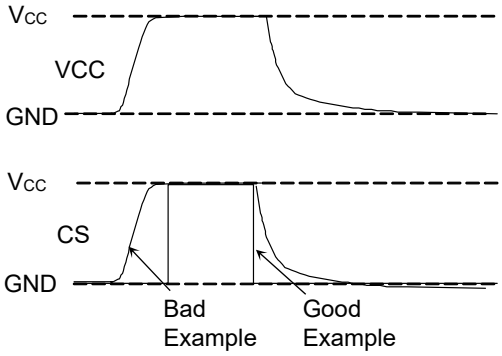

Figure 53. Timing at power ON/OFF

(Good example) The CS Pin is Low at power ON/OFF.
Set 1 ms or more to recharge at power OFF. When power is turned on without observing this condition, IC internal circuit may not be reset.

(Bad example) The CS Pin is pulled up to V_{CC}.
In this case, CS becomes HIGH (active status), EEPROM may malfunction or have write error due to noises. This is true even when CS input is High-Z.

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ = 1.5 V) or below, data rewrite is prevented.

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Noise Countermeasures

1. VCC Noise (bypass capacitor)
   When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1 μF) between IC VCC and GND. At this time, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board VCC and GND.

2. SK Noise
   When the rise time (t_R) of SK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SK input. The hysteresis width of this circuit is set about 0.2 V (V_{CC} = 5 V), if noises exist at SK input, set the noise amplitude 0.2 Vp-p or below. And it is recommended to set the rise time (t_R) of SK 100 ns or below. In the case when the rise time is 100 ns or more, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Operational Notes - continued

12. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet "Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

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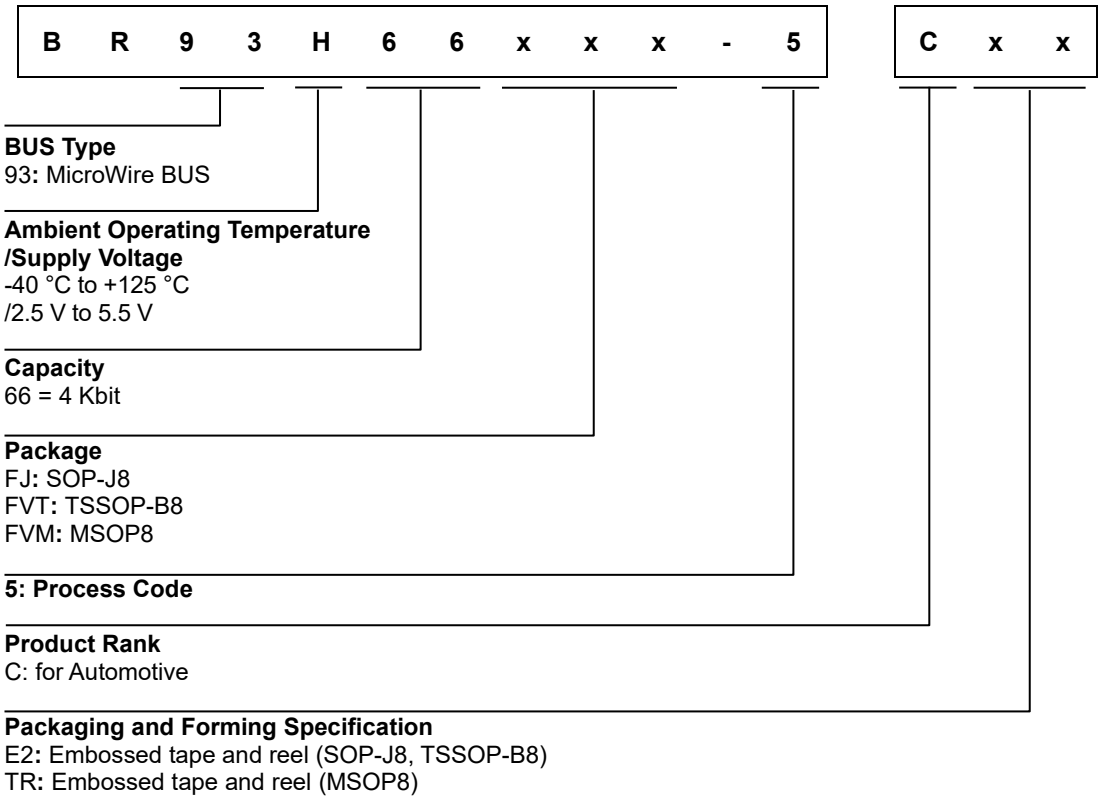
Ordering Information



Lineup

Package		Orderable Part Number	
Type	Quantity		
SOP-J8	Reel of 2500	BR93H66FJ	-5CE2
TSSOP-B8	Reel of 3000	BR93H66FVT	-5CE2
MSOP8	Reel of 3000	BR93H66FVM	-5CTR

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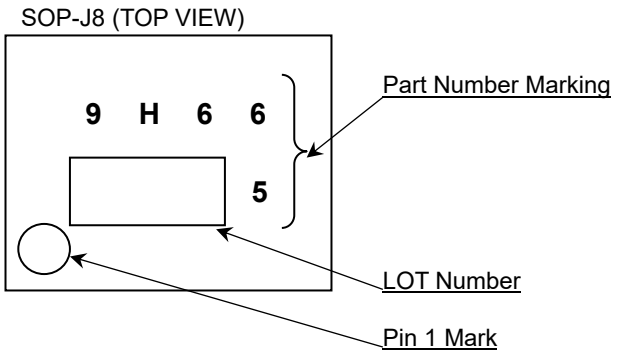
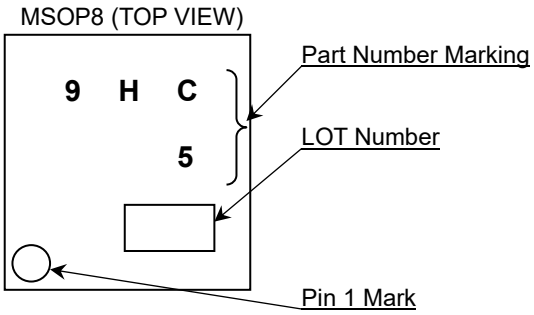
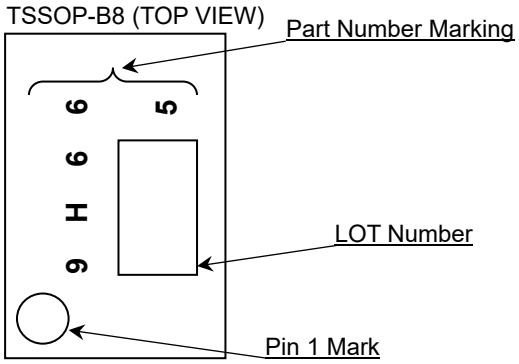
Marking Diagrams







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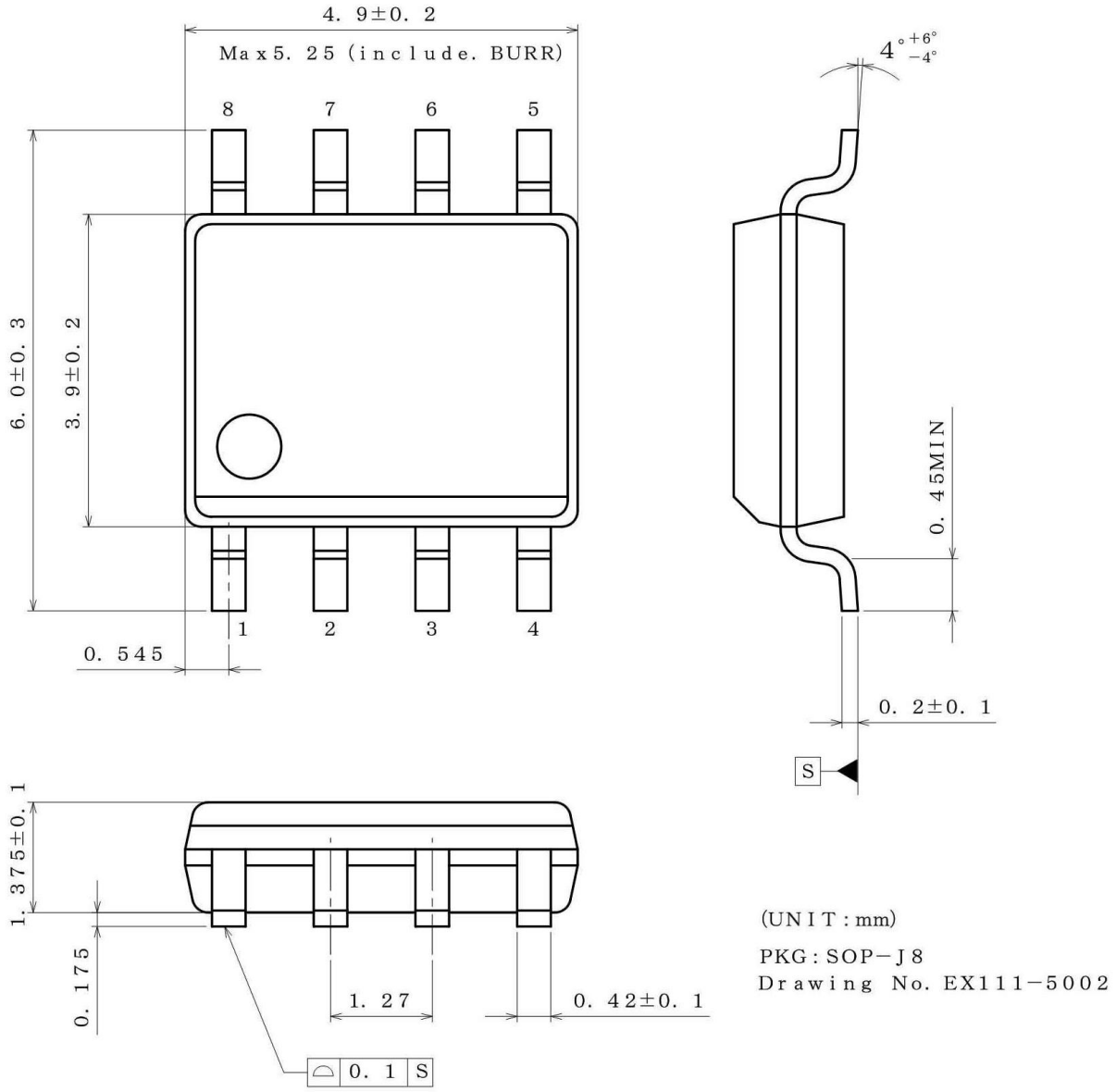
Physical Dimension and Packing Information

Package Name	SOP-J8



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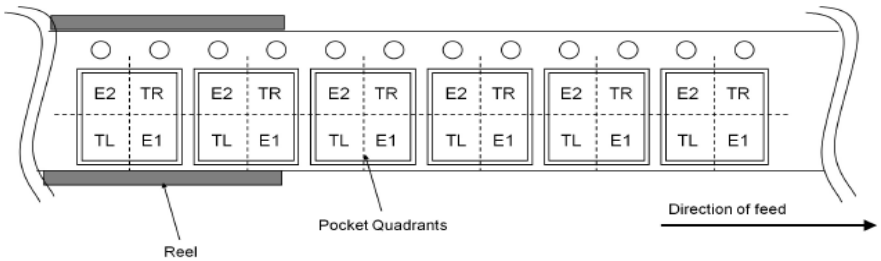
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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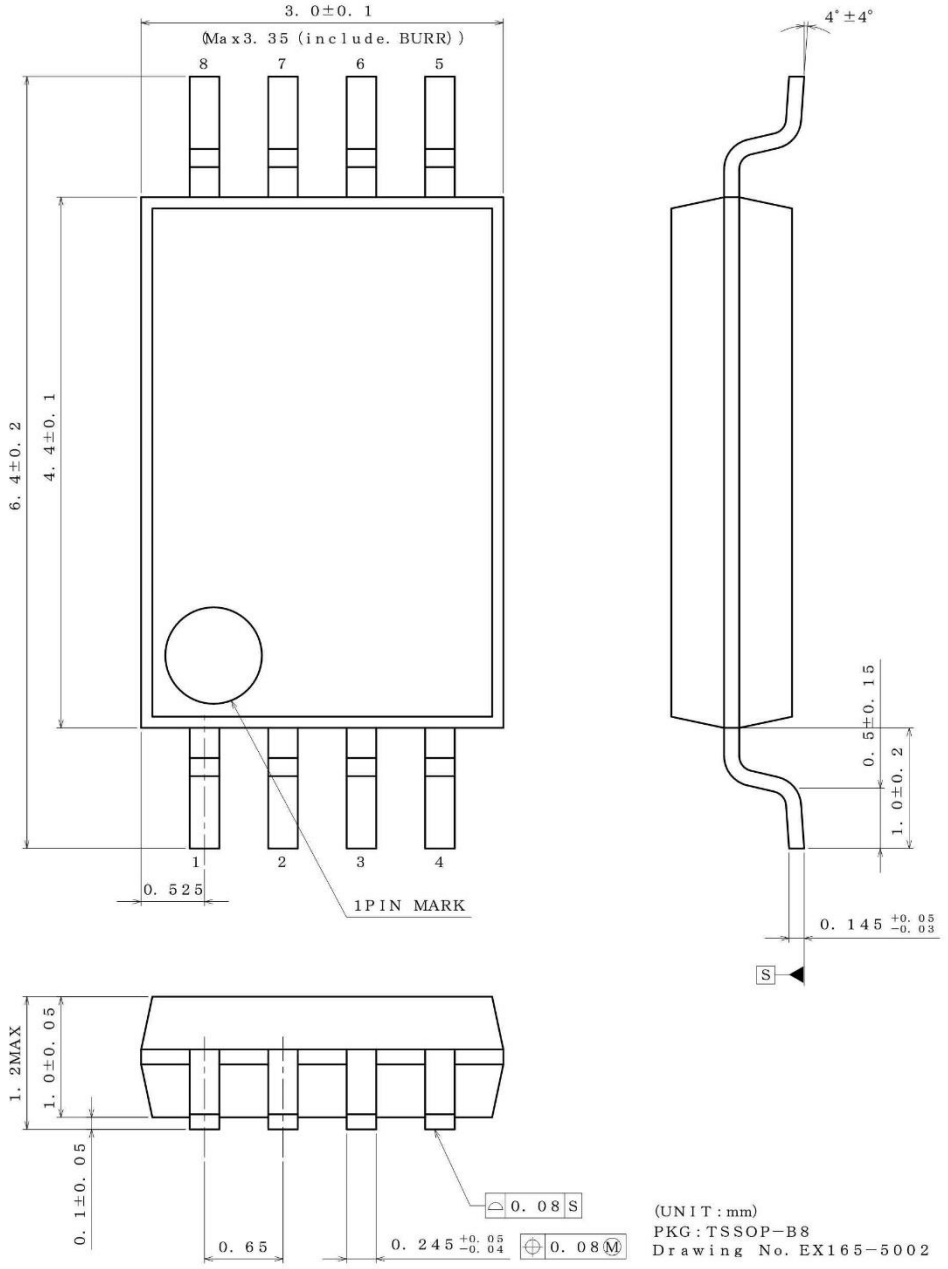
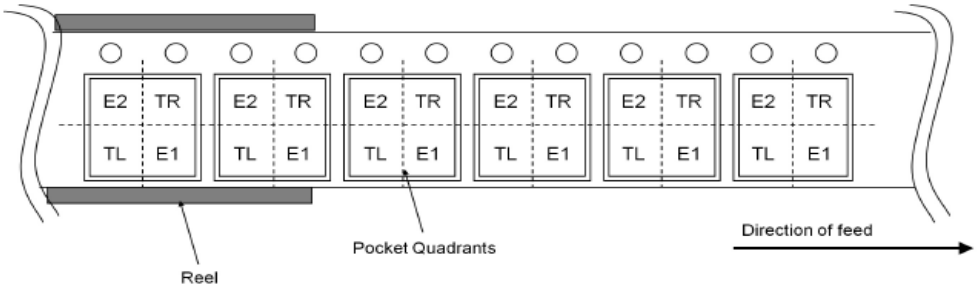
Physical Dimension and Packing Information - continued

Package Name	TSSOP-B8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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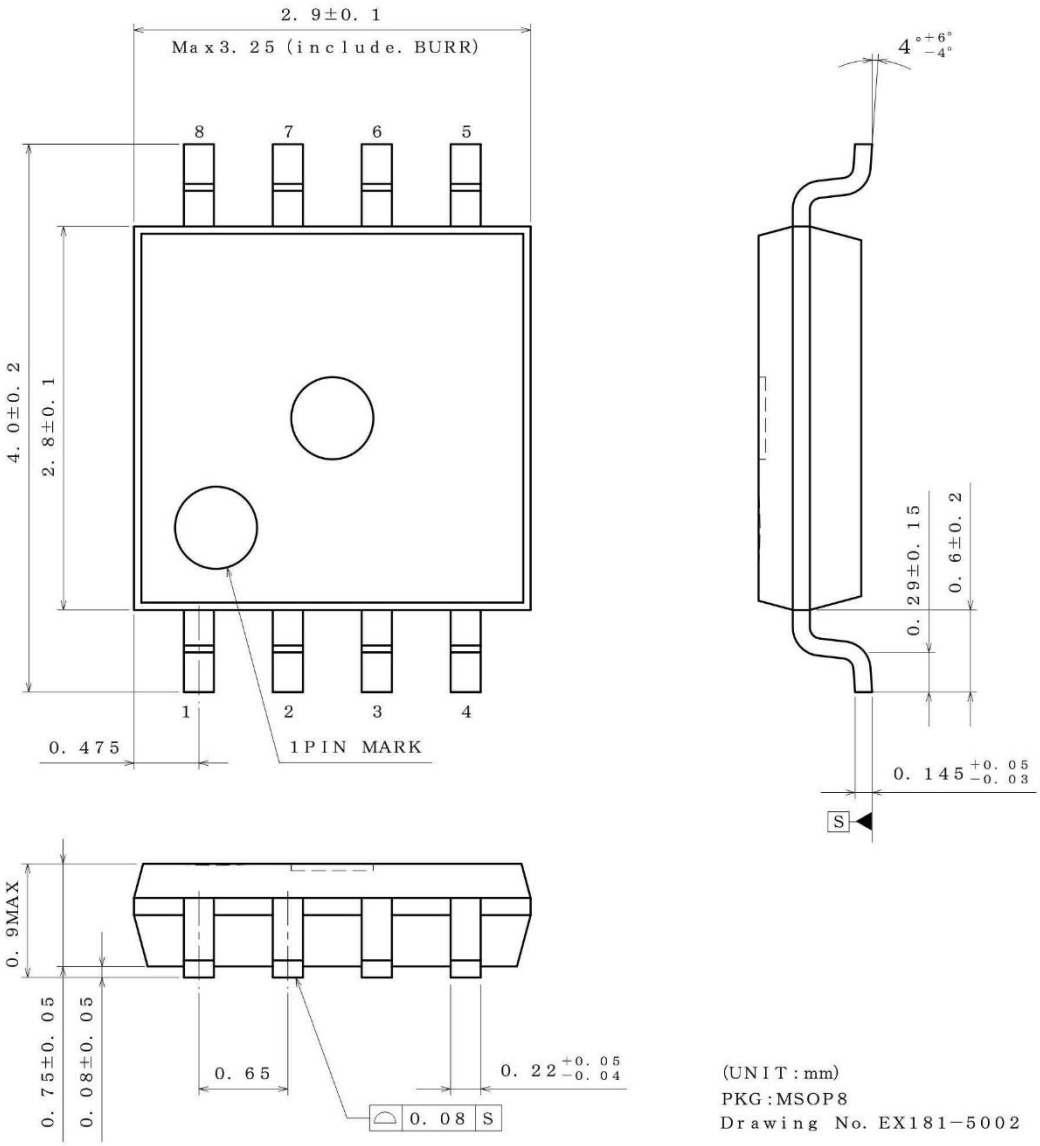
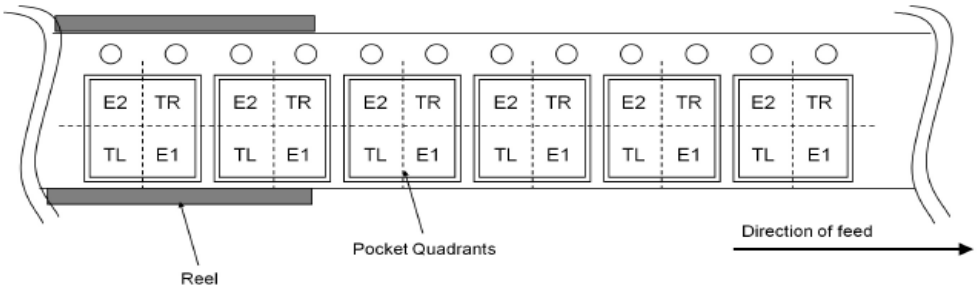
Physical Dimension and Packing Information - continued

Package Name	MSOP8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Revision	Changes
01.Jun.2026	001	New Release

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Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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