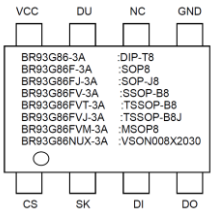
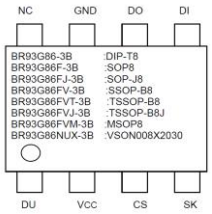
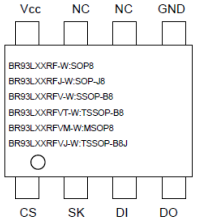
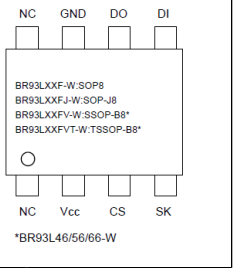
EEPROM Series

Difference between BR93G-3A/3B and BR93LR-W/L-W

Pin configuration and function

Series	Old series	Pin assignment
BR93G-3A	BR93LR-W	General (VCC=pin8/GND=pin5)
BR93G-3B	BR93L-W	Chip rotated (VCC=pin2/GND=pin7)

Pin No.	BR93G-3A			BR93G-3B			BR93LR-W			BR93L-W		
	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
1	CS	I	Chip select input	DU	–	Don't use Terminals not used may be set to any of high,low, and OPEN.	CS	I	Chip select input	NC	–	Non connected terminal Terminals not used may be set to any of high,low, and OPEN.
2	SK	I	Serial clock input	VCC	–	Supply voltage	SK	I	Serial clock input	VCC	–	Supply voltage
3	DI	I	Start bit, opcode, address, and serial data input	CS	I	Chip select input	DI	I	Start bit, opcode, address, and serial data input	CS	I	Chip select input
4	DO	O	Serial data output, READY / BUSY STATUS display output	SK	I	Serial clock input	DO	O	Serial data output, READY / BUSY STATUS display output	SK	I	Serial clock input
5	GND	–	All input / output reference voltage, 0V	DI	I	Start bit, opcode, address, and serial data input	GND	–	All input / output reference voltage, 0V	DI	I	Start bit, opcode, address, and serial data input
6	NC	–	Non connected terminal Terminals not used may be set to any of high,low, and OPEN.	DO	O	Serial data output, READY / BUSY STATUS display output	NC	–	Serial data output, READY / BUSY STATUS display output	DO	O	Serial data output, READY / BUSY STATUS display output
7	DU	–	Don't use Terminals not used may be set to any of high,low, and OPEN.	GND	–	All input / output reference voltage, 0V	NC	–	Serial data output, READY / BUSY STATUS display output	GND	–	All input / output reference voltage, 0V
8	VCC	–	Supply voltage	NC	–	Non connected terminal Terminals not used may be set to any of high,low, and OPEN.	VCC	–	Supply voltage	NC	–	Non connected terminal Terminals not used may be set to any of high,low, and OPEN.
Pin assign-ment										 *BR93L46/56/66-W		

Over/short clock cancel function

BR93G-3A, BR93G-3B, BR93L-W, BR93LR-W have short clock cancel function. This function works if the number of clocks are fewer than expected, and commands will not be accepted.

All of BR93G series have over clock cancel function. This function works if the number of clocks are more than expected, and commands will not be accepted. BR93L-W, BR93LR-W doesn't have this function except for 16Kbit products (BR93L86-W, BR93L86R-W).

Series	Over clock cancel	Short clock cancel
BR93G-3A	supported	supported
BR93G-3B	supported	supported
BR93LR-W	Not supported (except for 16Kbit products)	supported
BR93L-W	Not supported (except for 16Kbit products)	supported

Write/Erase command cancel timing

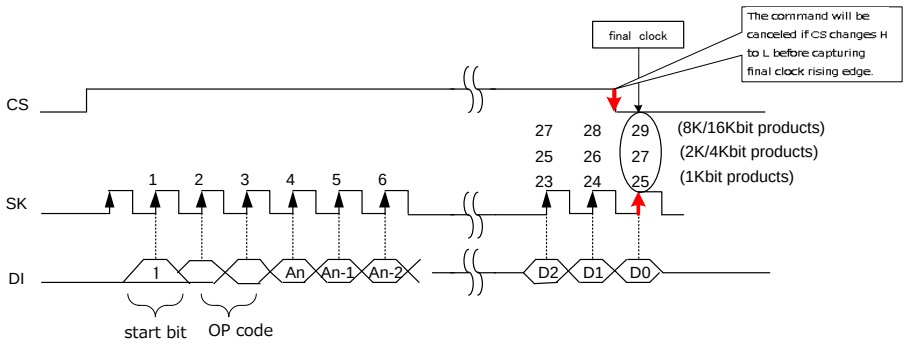
BR93G-3A, BR93G-3B, BR93L-W, BR93LR-W have short clock cancel function that cancels any command if the number of clock cycles are fewer than expected, and it will be activated at the time when the falling edge of CS signal appears before the rising edge of the final clock.
On the other hand, over clock cancel function has difference in each product as below.

BR93L46/56/66/76-W, BR93L46R/56R/66R/76R-W (without overclock cancel function)
Write and Erase commands will be effective at the timing of the final clock cycle's rising edge. After that, the IC goes into write cycle and any command cancellation will be disabled. In that case, it is necessary to switch CS from High to Low once after the final clock cycle and execute write/erase command again to write the desired data.

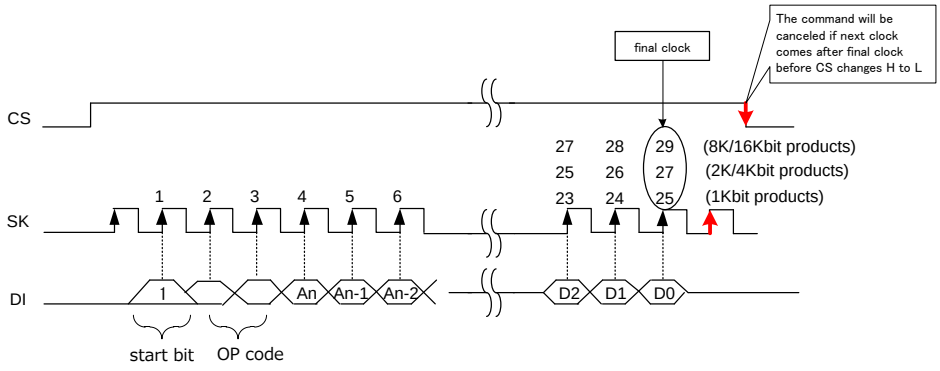
BR93L86-W, BR93L86R-W, BR93G-3A, BR93G-3B (with overclock cancel function)
Write and Erase commands will be effective at the timing of the final clock cycle's rising edge. If extra clock cycles are input after that timing, command will be cancelled as 'over clock'. After that, it can reset to the state before command input by making CS Low. Please note that if CS changes Low to High before the rising of extra clock cycles, IC goes into write cycle, and cancel is impossible.

(supplement)

・Short clock cancel function.
Any command will be cancelled if CS changes High to Low before the number of clock cycles reach a specific number.



・Over clock cancel function.
Any command will be cancelled if the clock cycles reach more than a specific number before CS changes High to Low.



Main electrical characteristics

BR93G-3A and BR93G-3B are characteristically upward compatible with BR93L-W and BR93LR-W.

Parameter		Symbol	BR93G-3A、BR93G-3B		BR93L-W、BR93LR-W	
			Limits	Condition	Limits	Condition
Recommended Operating Ratings	Power Source Voltage	VCC	1.7V to 5.5V	-	1.8V to 5.5V	-
DC characteristics	Input Low Voltage	VIL	-0.3V to 0.3VCC	1.7≦VCC≦5.5V	-0.3V to 0.8V	4.0V≦VCC≦5.5V
					-0.3V to 0.2VCC	VCC≦4.0V
	Input High Voltage	VIH	0.7VCC to VCC+1.0 V	1.7≦VCC≦5.5V	2V to VCC+0.3 V	4.0V≦VCC≦5.5V
					0.7VCC to VCC+0.3 V	VCC≦4.0V
	Supply Current (WRITE)	ICC1	<2mA	VCC=5.5V f=3MHz	<3mA	VCC=2.5 to 5.5V f=2MHz
	Supply Current (READ)	ICC2	<1mA	VCC=1.7~5.5V f=3MHz	<1.5mA	VCC=2.5 to 5.5V f=2MHz
	Supply Current (WRAL, ERAL)	ICC3	<3mA	VCC=5.5V f=3MHz	<4.5mA	VCC=2.5 to 5.5V f=2MHz
	Supply Current (WRITE) at Low Vcc	ICC1	<1.0mA	VCC=1.7V f=1MHz	<1.5mA	VCC=1.8 to 2.5V f=500kHz
	Supply Current (Read) at low Vcc	ICC2	<0.5mA	VCC=1.7~5.5V f=1MHz	<0.5mA	VCC=1.8 to 2.5V f=500kHz
	Supply Current (WRAL, ERAL) at low Vcc	ICC3	<2mA	VCC=2.5V f=1MHz	<2mA	VCC=1.8 to 2.5V f=500kHz
AC characteristics	SK frequency	fSK	<2MHz	VCC=2.5to 5.5V	<2MHz	VCC=2.5to 5.5V
	SK high time	tKH	>230ns		>230ns	
	SK low time	tSKL	>200ns		>230ns	
	CS low time	tCS	>200ns		>200ns	
	CS setup time	tCSS	>50ns		>50ns	
	DI setup time	tDIS	>100ns		>100ns	
	CS hold time	tCSH	>0ns		>0ns	
	DI hold time	tDIH	>100ns		>100ns	
	Data “1” output delay	tPD1	<200ns		<200ns	
	Data “0” output delay	tPD0	<200ns		<200ns	
	Time from CS to output establishment	tSV	<150ns		<150ns	
	Time from CS to High-Z	tDF	<100ns		<150ns	
	SK frequency	fSK	<1MHz	VCC=1.7to 5.5V	<500kHz	VCC=1.8to 2.5V
	SK high time	tKH	>250ns		>800ns	
	SK low time	tSKL	>250ns		>800ns	
	CS low time	tCS	>250ns		>1000ns	
	CS setup time	tCSS	>200ns		>200ns	
	DI setup time	tDIS	>100ns		>100ns	
	CS hold time	tCSH	>0ns		>0ns	
	DI hold time	tDIH	>100ns		>100ns	
	Data “1” output delay	tPD1	<400ns		<700ns	
	Data “0” output delay	tPD0	<400ns		<700ns	
	Time from CS to output establishment	tSV	<400ns		<700ns	
	Time from CS to High-Z	tDF	<200ns		<200ns	
Memory cell characteristics	Write cycles		>1,000,000 times	Ta=25℃	>1,000,000 times	Ta=25℃
	Data retention		> 40years	Ta=25℃	> 40years	Ta=25℃