Datasheet

Automotive Motor Driver Series

Three-phase Brushless Motor Pre-driver for Automotive

BD16851AEKV-C

General Description

BD16851AEKV-C is a pre-driver IC for in-vehicle three-phase brushless motor. It is a sensor-less drive that the hall devices for the position sensing are unnecessary and has a built-in speed control function.
Input/output protections have a self-diagnosis and self-recovery function, and it can simplify the system configuration. Also, each input/output protection states can be judged easily by the abnormal status signal output function. It improves traceability of the set.

Features

- AEC-Q100 Qualified(*Note 1*)
- Sensor-less Drive
- Speed Control (Speed Feedback)
- PWM Duty Input / DC Voltage Input Speed Control
- Built-in Two-stage Charge Pump
- Variable Output Slew Rate Control with Constant Current Output
- Rotation Pulse Signal and Abnormal Status Signal Output
- Input Protection (PWM Input Frequency)
- Output Protection (Over Voltage, Over Current, Over Temperature, Boost Voltage, Motor Lock (Low Speed and High Speed), Motor Reverse Idling)
- Under Voltage Lock Out

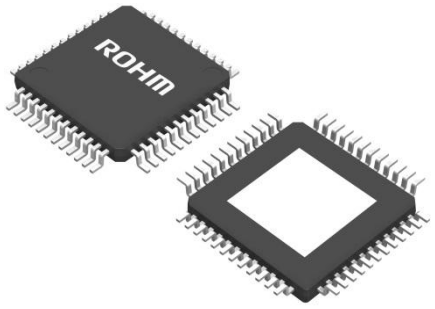
(*Note 1*) Grade 1

Key Specifications

- Supply Voltage Range: 5.5 V to 18.0 V
- Junction Temperature Range: -40 °C to +150 °C

Package

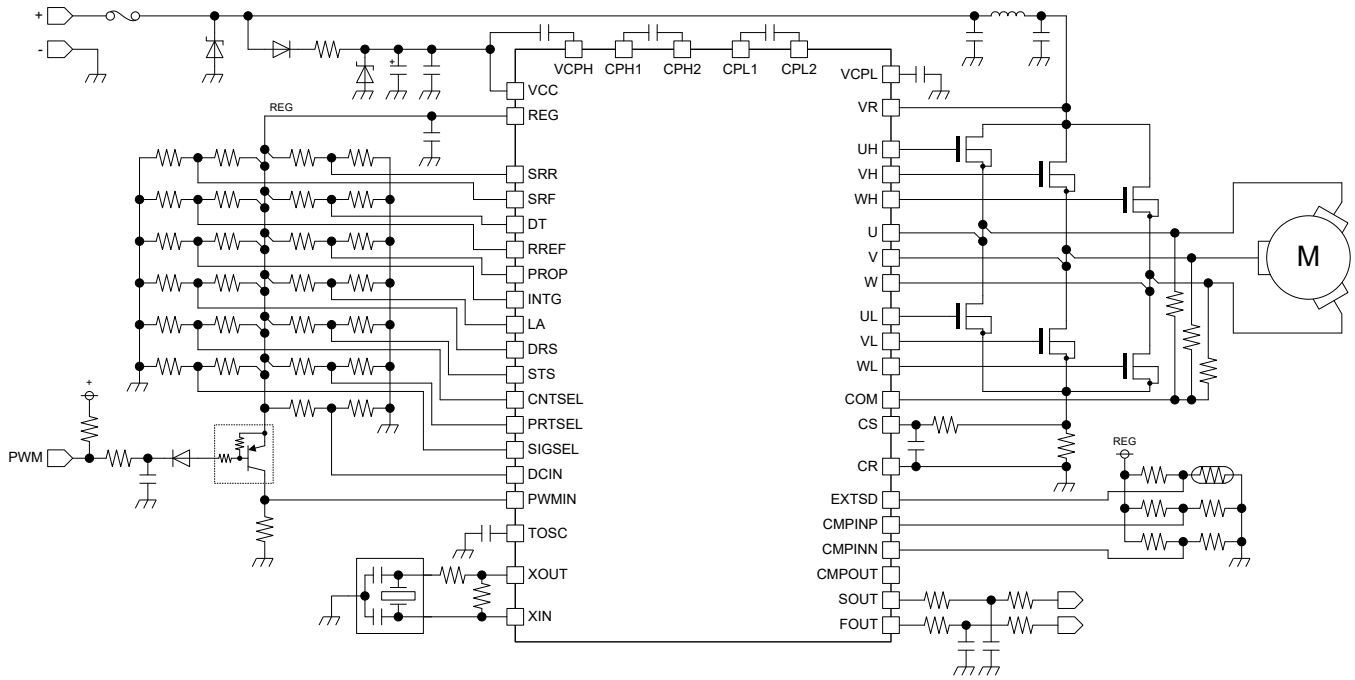
	W (Typ) x D (Typ) x H (Max)
HTQFP48V	9.0 mm x 9.0 mm x 1.0 mm



Application

- Automotive Various Pump, Fan Motor

Typical Application Circuit

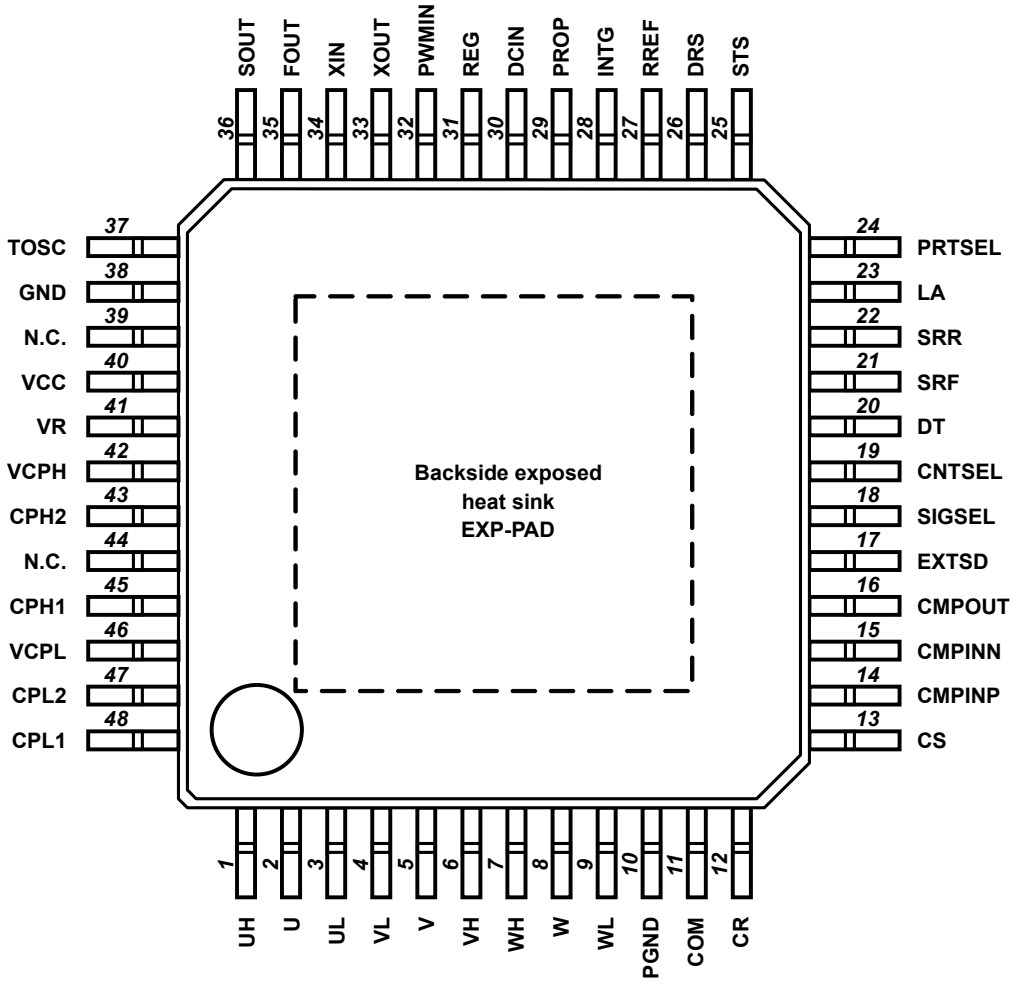


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration

(TOP VIEW)

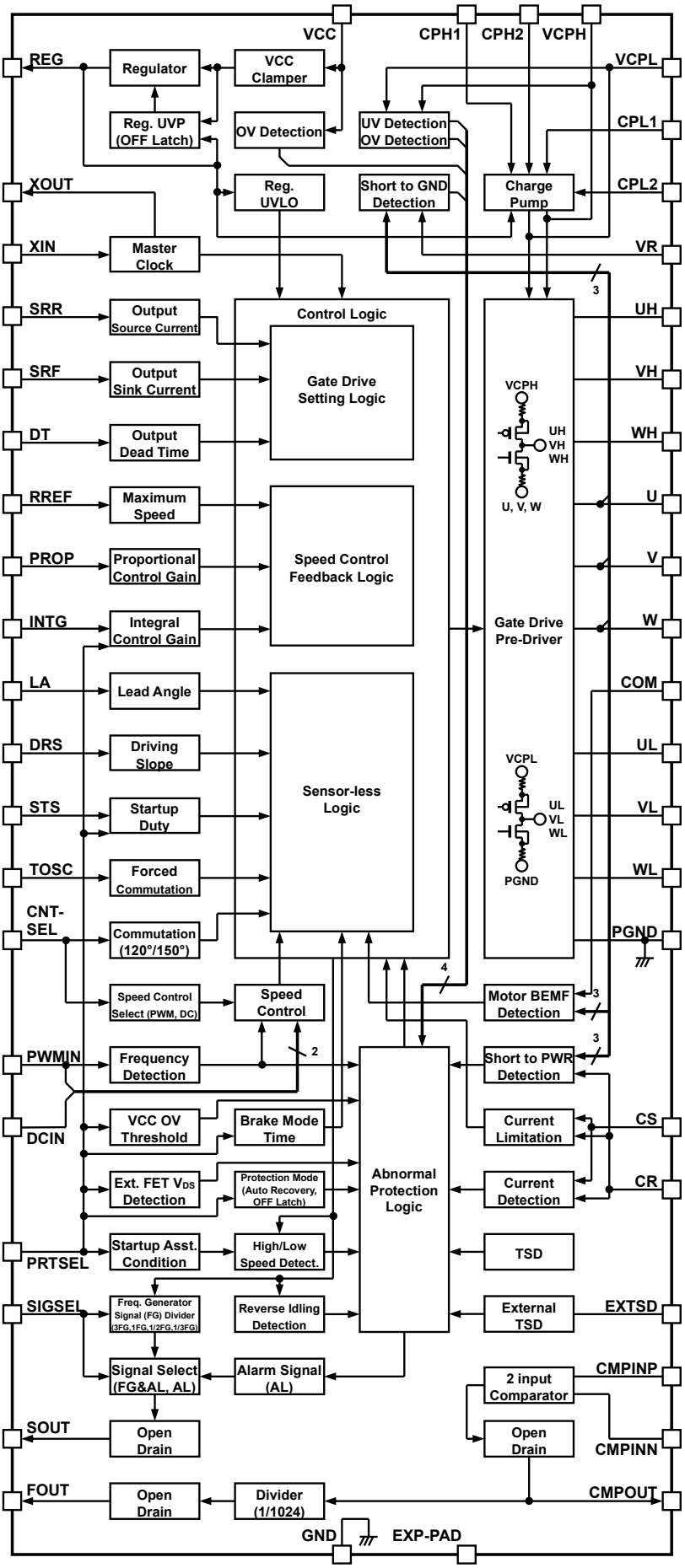


Pin Description

Pin No.	Pin Name	Function
1	UH	U phase high side gate drive output
2	U	U phase detection voltage input
3	UL	U phase low side gate drive output
4	VL	V phase low side gate drive output
5	V	V phase detection voltage input
6	VH	V phase high side gate drive output
7	WH	W phase high side gate drive output
8	W	W phase detection voltage input
9	WL	W phase low side gate drive output
10	PGND	Ground (Large current ground) input
11	COM	Motor midpoint detection voltage input
12	CR	Low side current reference voltage input
13	CS	Low side current detection voltage input
14	CMPINP	Comparator input +
15	CMPINN	Comparator input -
16	CMPOUT	Comparator output
17	EXTSD	External temperature detection voltage input
18	SIGSEL	SOUT signal output setting input
19	CNTSEL	Speed control system setting input
20	DT	Output dead time setting input
21	SRF	Gate Drive Output sink current setting input
22	SRR	Gate Drive Output source current setting input
23	LA	Lead angle setting input
24	PRTSEL	Protection system setting input

Pin No.	Pin Name	Function
25	STS	Start duty setting input
26	DRS	Drive slope setting input
27	RREF	Speed control maximum speed setting input
28	INTG	Speed control (Integral) gain setting input
29	PROP	Speed control (Proportional) gain setting input
30	DCIN	Speed control DC voltage input
31	REG	Reference voltage (5 V) output
32	PWMIN	Speed control PWM duty input
33	XOUT	External CLK output
34	XIN	External CLK input
35	FOUT	CMPOUT divided signal output
36	SOUT	Rotation pulse signal / Abnormal status signal output
37	TOSC	Capacitor connection for forced commutation period setting
38	GND	Ground (Small signal ground) input
39	N.C.	- (This pin is open on-board wiring pattern)
40	VCC	Power supply input
41	VR	Motor power supply reference voltage input
42	VCPH	Boosted voltage output for high side gate drive
43	CPH2	Capacitor connection + for high side boost
44	N.C.	- (This pin is open on-board wiring pattern)
45	CPH1	Capacitor connection - for high side boost
46	VCPL	Boosted voltage output for low side gate drive
47	CPL2	Capacitor connection + for low side boost
48	CPL1	Capacitor connection - for low side boost
-	EXP-PAD	The back-heatsink and the ground pin adjust to same electric potential

Block Diagram



Absolute Maximum Rating

Parameter		Symbol	Rating	Unit
Input Voltage	VCC	V_{CC}	-0.3 to +50	V
	PWMIN	V_{PWMIN}	-0.3 to V_{REG}	V
	EXTSD, PRTSEL, CNTSEL, SIGSEL, DCIN, RREF, INTG, PROP, STS, DRS, LA, DT, SRR, SRF	V_{EXTSD}, V_{PRTSEL}, V_{CNTSEL}, V_{SIGSEL}, V_{DCIN}, V_{RREF}, V_{INTG}, V_{PROP}, V_{STS}, V_{DRS}, V_{LA}, V_{DT}, V_{SRR}, V_{SRF}	-0.3 to V_{REG}	V
	CS, CR, TOSC	V_{CS}, V_{CR}, V_{TOSC}	-0.3 to +3	V
	XIN	V_{XIN}	-0.3 to +3	V
	CMPINP, CMPINN	V_{CMPINP}, V_{CMPINN}	-0.3 to V_{REG}	V
	U, V, W	V_{OS}	-4 to +50	V
	COM	V_{COM}	-4 to +50	V
	VR	V_{VR}	V_{CC}-0.3 to +50	V
Output Voltage	REG	V_{REG}	-0.3 to +7	V
	XOUT	V_{XOUT}	-0.3 to +3	V
	CMPOUT	V_{CMPOUT}	-0.3 to V_{REG}	V
	SOUT, FOUT	V_{SOUT}, V_{FOUT}	-0.3 to +50	V
	VCPH, CPH2	V_{VCPH}, V_{CPH2}	-0.3 to V_{CC}+13 (≤ +60)	V
	VCPL, CPH1, CPL2	V_{VCPL}, V_{CPH1}, V_{CPL2}	-0.3 to +13	V
	CPL1	V_{CPL1}	-0.3 to +7	V
	UH, VH, WH	V_{UH}, V_{VH}, V_{WH}	-0.3 to V_{VCPH}	V
	UL, VL, WL	V_{UL}, V_{VL}, V_{WL}	-0.3 to V_{VCPL}	V
Output Current	REG	I_{REG}	-10 to 0	mA
	CMPOUT	I_{CMPOUT}	0 to +10	mA
	SOUT, FOUT	I_{SOUT}, I_{FOUT}	0 to +20	mA
Maximum Junction Temperature		Tjmax	-40 to +150	°C
Storage Temperature Range		Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTQFP48V				
Junction to Ambient	θ_{ja}	73.4	30.5	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{jt}	18.0	10.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD16851AEKV-C chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol				Unit
		MIN	TYP	MAX	
Operating Supply Voltage	V_{CC}	5.5	12.0	18.0	V
PWMIN Input Frequency	f_{PWMIN}	6.8	100	1000	Hz
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics

(Unless otherwise specified Tj = -40 °C to +150 °C, V_{CC} = 5.5 V to 18 V, REG-GND = 1 µF, VCC-VCPH = 1 µF, CPH2-CPH1 = 0.1 µF, VCPL-GND = 1 µF, CPL2-CPL1 = 0.1 µF, V_{CR} = V_{CS} = 0 V, f_{XIN} = 10 MHz, REG-CMPOUT = 10 kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Overall>						
Circuit Current	I_{CC}	12	20	28	mA	
REG Reference Voltage	V_{REG}	4.8	5.0	5.2	V	I_{REG} = -10 mA
<Boost Voltage Output for Gate Drive (VCPH, VCPL)>						
VCPH Boost Voltage	V_{VCPH}	V_{CC} +6.0	V_{CC} +9.5	V_{CC} +13.0	V	
VCPL Boost Voltage	V_{VCPL}	6.0	9.5	13.0	V	
Boost Operating Frequency	f_{CP}	-	312.5	-	kHz	
<Gate Drive Output (UH, VH, WH, UL, VL, WL)>						
High Side Gate Drive Output Voltage	V_{GSH}	V_{CC} +6.0	V_{CC} +9.5	V_{CC} +13.0	V	I_O = -20 mA at Source Current -35 mA mode
Low Side Gate Drive Output Voltage	V_{GSL}	6.0	9.5	13.0	V	I_O = -20 mA at Source Current -35 mA mode
Accuracy of Output Source Current	$ACC_{ISOURCE}$	-30	-	+30	%	SRR setting (16 mode)
Accuracy of Output Sink Current	ACC_{ISINK}	-30	-	+30	%	SRF setting (16 mode) Excludes inflow to R_{GS}
Accuracy of Output Dead Time	ACC_{tDEAD}	-15	-	+15	%	DT setting (16 mode)
Speed Control Operating Frequency	f_{SPD}	-	20	-	kHz	
150° Energizing Section Operating Frequency	f_{SOFTSW}	-	78	-	kHz	
Output Pull Down Resistor	R_{GS}	8.6	15.0	21.4	kΩ	
<Signal Output (SOUT, FOUT)>						
Output Low Voltage	V_{SIGL}	-	0.1	0.3	V	I_{SOUT} = I_{FOUT} = +10 mA
Output Leak Current	I_{SIGL}	-	0	10	µA	V_{SOUT} = V_{FOUT} = 50 V
FOUT Dividing Ratio	G_{SIG}	-	1024	-	-	G_{SIG} = f_{FOUT}/f_{CMPOUT}
<Speed Control PWM Duty (PWMIN)>						
High Level Input Voltage	V_{PWMINH}	2.0	-	V_{REG}	V	
Low Level Input Voltage	V_{PWMINL}	0.0	-	0.8	V	
Input Leak Current	I_{PWMINH}	-1.2	0	+1.2	µA	V_{PWMIN} = V_{REG}
Input Bias Current	I_{PWMINL}	-70	-50	-30	µA	V_{PWMIN} = 0 V
<Forced Commutation Period Setting (TOSC)>						
High Voltage	V_{TOSCH}	1.8	2.0	2.2	V	
Low Voltage	V_{TOSCL}	0.9	1.0	1.1	V	
Charge Current	I_{CTOSC}	-48	-40	-32	µA	V_{TOSC} = 0.8 V
Discharge Current	I_{DTOSC}	32	40	48	µA	V_{TOSC} = 2.2 V
<External CLK Input (XIN)>						
High Level Input Voltage	V_{XINH}	2.0	-	3.0	V	
Low Level Input Voltage	V_{XINL}	0	-	0.8	V	
Input Bias Current	I_{XIN}	-10	-	+10	µA	
<External CLK Output (XOUT)>						
Output High Voltage	V_{XOUTH}	2.4	2.7	3.0	V	V_{XIN} = 0 V, I_{XOUT} = -2 mA
Output Low Voltage	V_{XOUTL}	0.1	0.3	0.6	V	V_{XIN} = 3 V, I_{XOUT} = +2 mA
<Speed Control Maximum Speed Setting Input (RREF)>						
Accuracy of Maximum Speed Setting	ACC_{fMAX}	-5	-	+5	%	RREF Setting (15 mode)

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC.

Electrical Characteristics - continued

(Unless otherwise specified Tj = -40 °C to +150 °C, V_{CC} = 5.5 V to 18 V, REG-GND = 1 µF, VCC-VCPH = 1 µF, CPH2-CPH1 = 0.1 µF, VCPL-GND = 1 µF, CPL2-CPL1 = 0.1 µF, V_{CR} = V_{CS} = 0 V, f_{XIN} = 10 MHz, REG-CMPOUT = 10 kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Motor EMF Detection Voltage Input (U, V, W, COM)>						
Input Offset Voltage	V_{OSOFS}	-87.5	-	+87.5	mV	
Input Bias Current (U, V, W)	I_{OSL1}	-0.35	-0.25	-0.15	mA	V_{OS} = 0 V
Input Leak Current (COM)	I_{OSL2}	-1.2	0	+1.2	µA	V_{COM} = 0 V
Input Resistor (U, V, W, COM)	R_{OS}	20	35	50	kΩ	
<Over Voltage Protection (VCC)>						
Detection Voltage1	$V_{OVPDET1}$	27	30	33	V	OVP = 30 V Setting
Hysteresis Voltage1	$V_{OVPHYS1}$	-	2.0	-	V	OVP = 30 V Setting
Detection Voltage2	$V_{OVPDET2}$	18	20	22	V	OVP = 20 V Setting
Hysteresis Voltage2	$V_{OVPHYS2}$	-	1.0	-	V	OVP = 20 V Setting
<Low Side Current Reference Voltage Input (CR)>						
Open Voltage	V_{CROPN}	1.22	1.36	1.50	V	V_{PRTSEL} = 0 V
Input Leak Current	I_{CRH}	-1.2	0	+1.2	µA	V_{CR} = V_{CROPN}
Input Bias Current	I_{CRL}	-16	-11	-6	µA	V_{CR} = V_{PRTSEL} = 0 V
<Low Side Current Detection Voltage Input (CS)>						
Input Leak Current	I_{CSH}	-1.2	0	+1.2	µA	V_{CS} = 3 V
Input Bias Current	I_{CSL}	-1.2	0	+1.2	µA	V_{CS} = 0 V
<Current Limit (CR, CS): External Shunt Resistor Detection>						
Detection Voltage	V_{CLL}	85	100	115	mV	V_{CLL} = V_{CS} - V_{CR}
<Over Current Protection (CR, CS): External Shunt Resistor Detection>						
Detection Voltage	V_{CPL}	170	200	230	mV	V_{CPL} = V_{CS} - V_{CR}
<Over Current Protection (VR, U, V, W, CR): External FET Drain-Source Voltage Detection>						
Detection Voltage 1	V_{OCP1}	1275	1500	1725	mV	OCP = 1500 mV Setting V_{OCP1} = V_{VR} - V_{OS} = V_{OS} - V_{CR}
Detection Voltage 2	V_{OCP2}	850	1000	1150	mV	OCP = 1000 mV Setting V_{OCP2} = V_{VR} - V_{OS} = V_{OS} - V_{CR}
Detection Voltage 3	V_{OCP3}	340	400	460	mV	OCP = 400 mV Setting V_{OCP3} = V_{VR} - V_{OS} = V_{OS} - V_{CR}
Detection Voltage 4	V_{OCP4}	170	200	230	mV	OCP = 200 mV Setting V_{OCP4} = V_{VR} - V_{OS} = V_{OS} - V_{CR}
<Thermal Shutdown (Tj) Internal Junction Temperature Detection>						
Detection Temperature (Reference Value)*(Note 1)*	T_{TSDDET}	150	175	200	°C	
Hysteresis Temperature (Reference Value)*(Note 1)*	T_{TSDHYS}	-	25	-	°C	
< Thermal Shutdown (EXTSD) External Temperature (External Thermistor Voltage) Detection>						
Input Leak Current	I_{EXTSDH}	-1.2	0	+1.2	µA	V_{EXTSD} = V_{REG}
Input Bias Current	I_{EXTSDL}	-1.2	0	+1.2	µA	V_{EXTSD} = 0 V
Detection Voltage	V_{EXTH}	2.3	2.5	2.7	V	
Hysteresis Voltage	V_{EXHYS}	-	0.4	-	V	

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC.

(Note 1) Reference value is design value. Evaluation done during design, but not tested in production.

Electrical Characteristics - continued

(Unless otherwise specified Tj = -40 °C to +150 °C, V_{CC} = 5.5 V to 18 V, REG-GND = 1 µF, VCC-VCPH = 1 µF, CPH2-CPH1 = 0.1 µF, VCPL-GND = 1 µF, CPL2-CPL1 = 0.1 µF, V_{CR} = V_{CS} = 0 V, f_{XIN} = 10 MHz, REG-CMPOUT = 10 kΩ)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Over Voltage Protection (VCPH, VCPL)>						
VCPH Detection Voltage	$V_{OVPDET3}$	V_{CC} +12	V_{CC} +13	V_{CC} +14	V	
VCPH Hysteresis Voltage	$V_{OVPHYS3}$	-	1.0	-	V	
VCPL Detection Voltage	$V_{OVPDET4}$	12	13	14	V	
VCPL Hysteresis Voltage	$V_{OVPHYS4}$	-	1.0	-	V	
<Under Voltage Protection (VCPH, VCPL)>						
VCPH Detection Voltage	$V_{UVPDET3}$	V_{CC} +3.0	V_{CC} +3.5	V_{CC} +4.0	V	
VCPH Hysteresis Voltage	$V_{UVPHYS3}$	-	0.5	-	V	
VCPL Detection Voltage	$V_{UVPDET4}$	3.0	3.5	4.0	V	
VCPL Hysteresis Voltage	$V_{UVPHYS4}$	-	0.5	-	V	
<Abnormal Status Signal Output Duty (SOUT)>						
DIAG Output Frequency	f_{SOUT}	-	5	-	Hz	
<Under Voltage Lock Out (REG)>						
Detection Voltage	$V_{UVLODET}$	3.5	4.0	4.5	V	
Hysteresis Voltage	$V_{UVLOHYS}$	-	0.5	-	V	
<Comparator Input (CMPINP, CMPINN)>						
Input Voltage Range	V_{RCMP}	0	-	3.5	V	
Input Offset Voltage	V_{CMPOFS}	-10	0	+10	mV	CMPINP-CMPINN = 1000 pF
Input Bias Current	I_{CMPIN}	-1.2	0	+1.2	µA	V_{CMPINP} = 0 V to 3.5 V, V_{CMPINN} = 0 V to 3.5 V
<Comparator Output (CMPOUT)>						
Output Low Voltage	V_{CMPOL}	0.1	0.2	0.4	V	I_{CMPOUT} = +5 mA
Output Leak Current	I_{CMPOH}	-10	-	+10	µA	V_{CMPOUT} = V_{REG}
Rise Time Response Delay	t_{CMPR}	0.005	0.300	1.000	µs	V_{CMPINP} = 0 V to V_{REG}, V_{CMPINN} = V_{REG}/2
Fall Time Response Delay	t_{CMPF}	0.005	0.080	0.300	µs	V_{CMPINP} = V_{REG} to 0 V, V_{CMPINN} = V_{REG}/2
High Level Input Voltage	V_{CMPOIH}	2.5	-	V_{REG}	V	
Low Level Input Voltage	V_{CMPOIL}	0	-	0.8	V	

For parameters involving current, positive notation means inflow of current to the IC while negative notation means outflow of current from the IC.

Typical Performance Curves

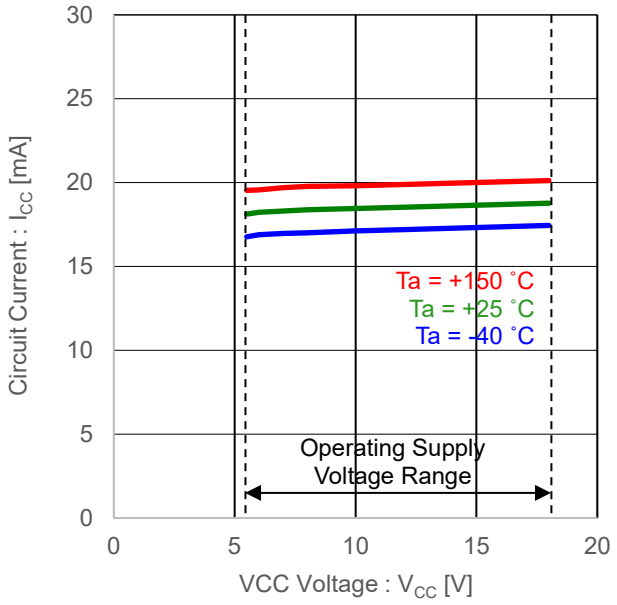


Figure 1. Circuit Current vs VCC Voltage

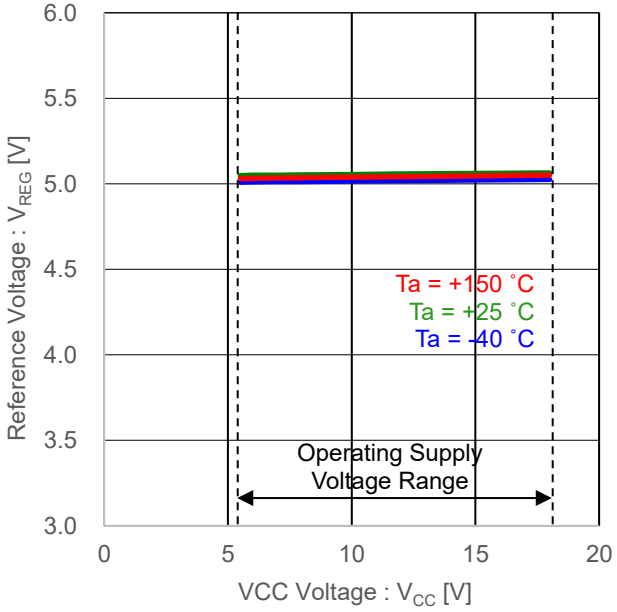


Figure 2. Reference Voltage vs VCC Voltage
(I_{REG} = -10 mA)

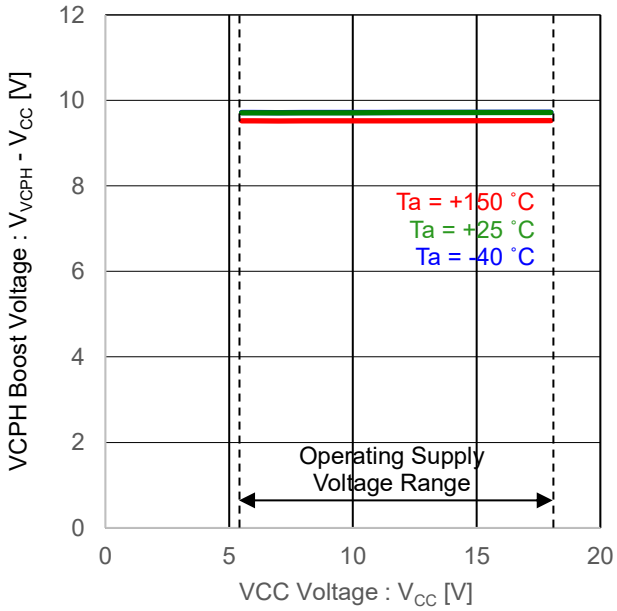


Figure 3. VCPH Boost Voltage vs VCC Voltage

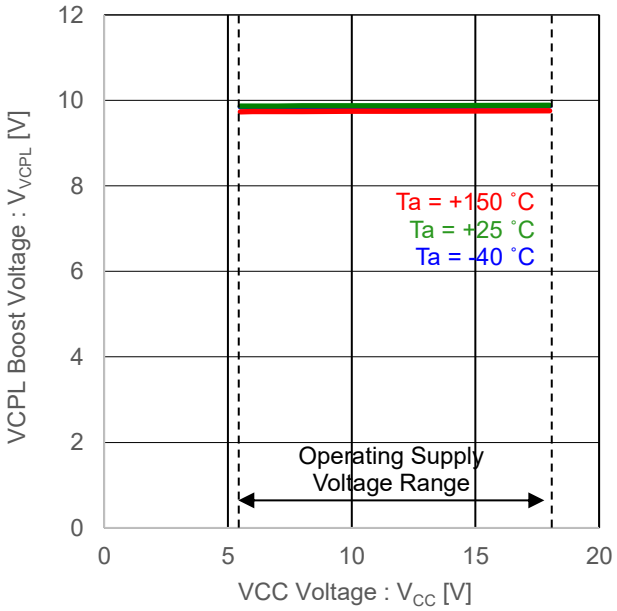


Figure 4. VCPL Boost Voltage vs VCC Voltage

Typical Performance Curves − continued

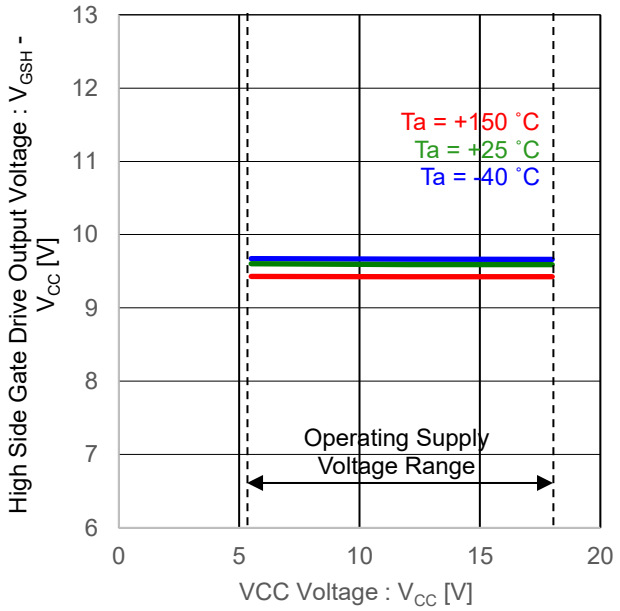


Figure 5. High Side Gate Drive Output Voltage vs VCC Voltage

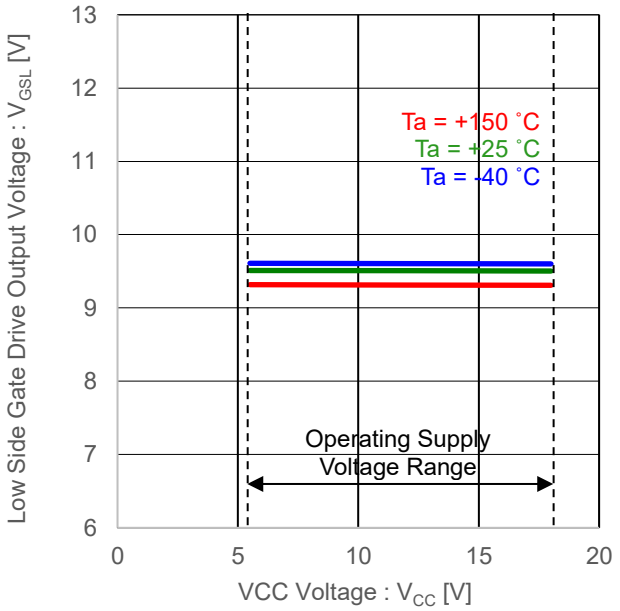


Figure 6. Low Side Gate Drive Output Voltage vs VCC Voltage

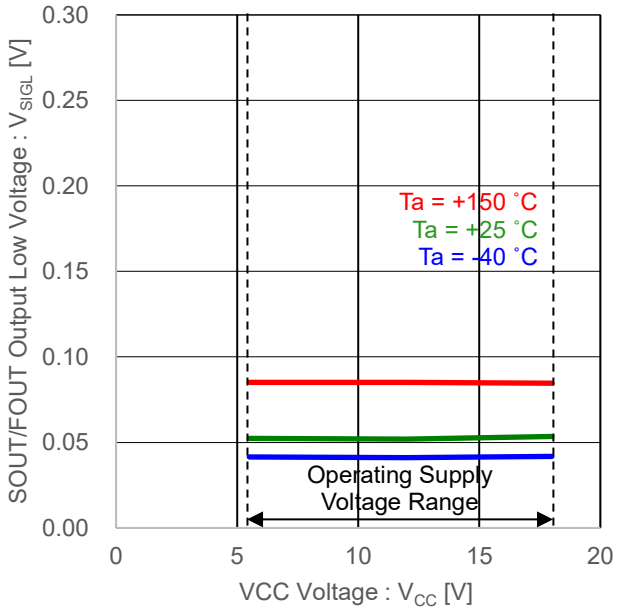


Figure 7. SOUT/FOUT Output Low Voltage vs VCC Voltage (I_{SIG} = 10 mA)

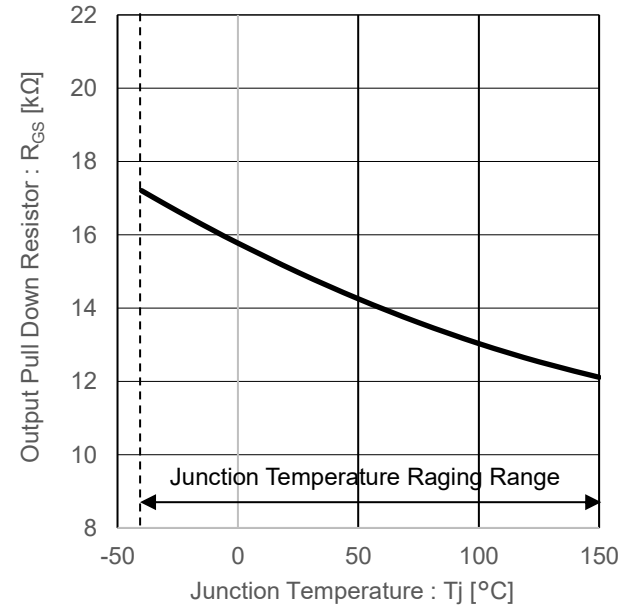


Figure 8. Output Pull Down Resistor vs Junction Temperature

Typical Performance Curves − continued

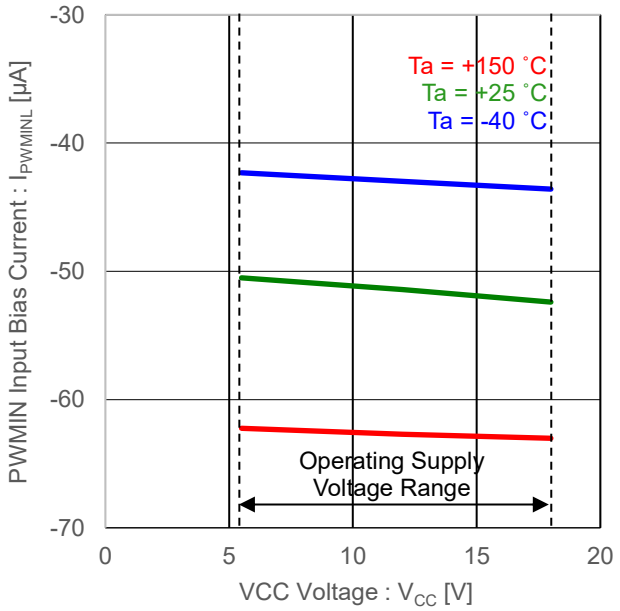


Figure 9. PWMIN Input Bias Current vs VCC Voltage
(V_{PWMIN} = 0 V)

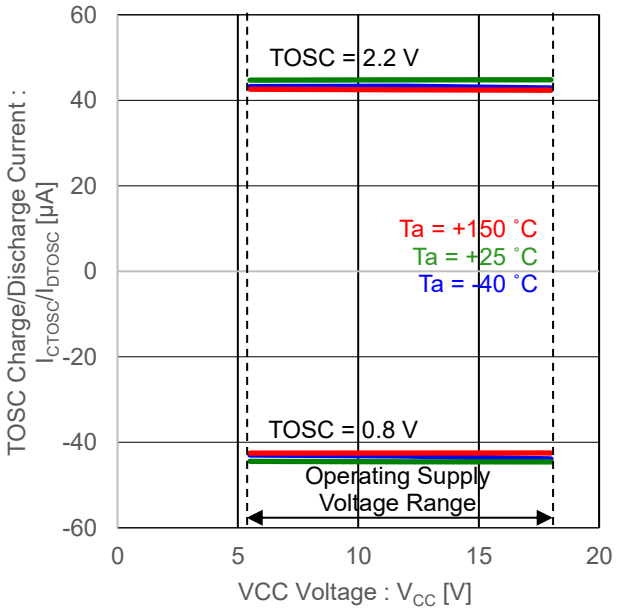


Figure 10. TOSC Charge/Discharge Current vs VCC Voltage

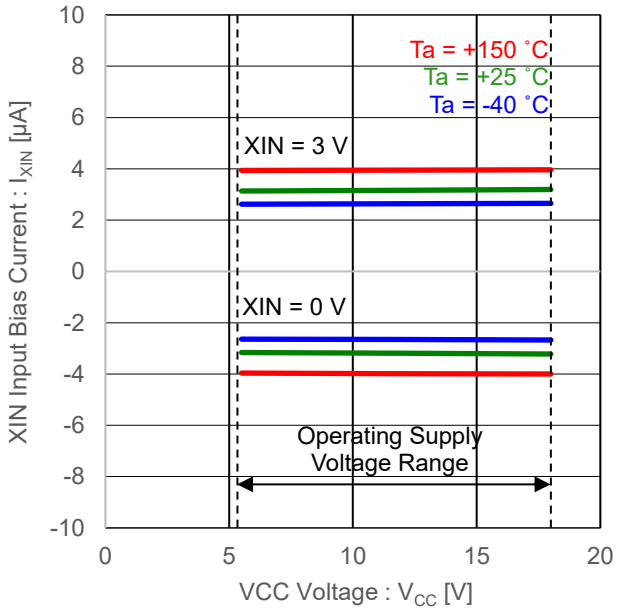


Figure 11. XIN Input Bias Current vs VCC Voltage

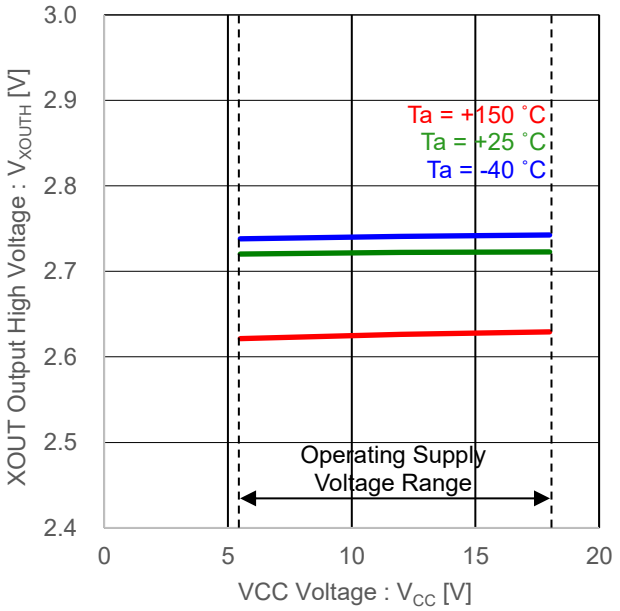


Figure 12. XOUT Output High Voltage vs VCC Voltage
(I_{XOUT} = -2 mA)

Typical Performance Curves − continued

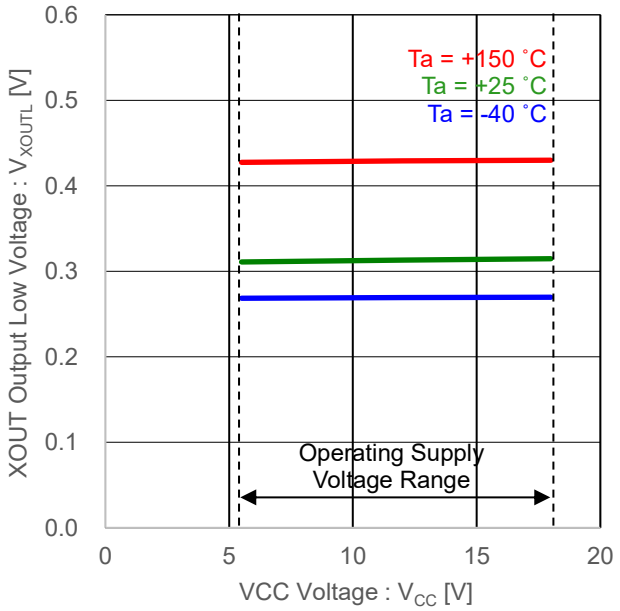


Figure 13. XOUT Output Low Voltage vs VCC Voltage
(I_{XOUT} = 2 mA)

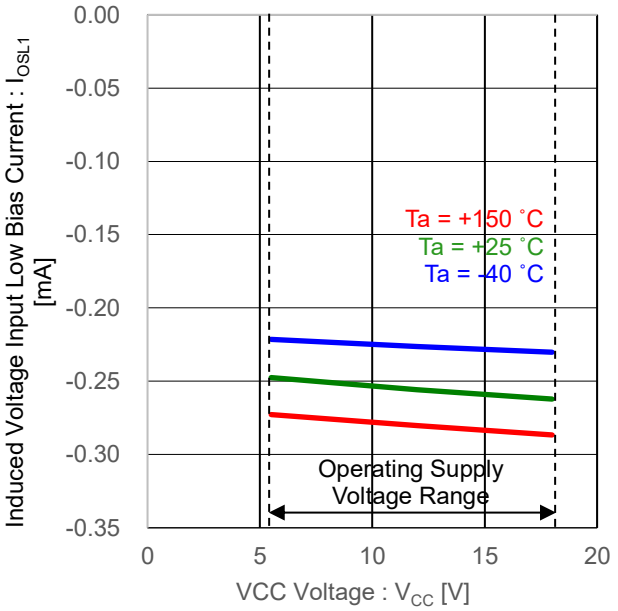


Figure 14. Induced Voltage Input Low Bias Current vs VCC Voltage
(V_U = V_V = V_W = 0 V)

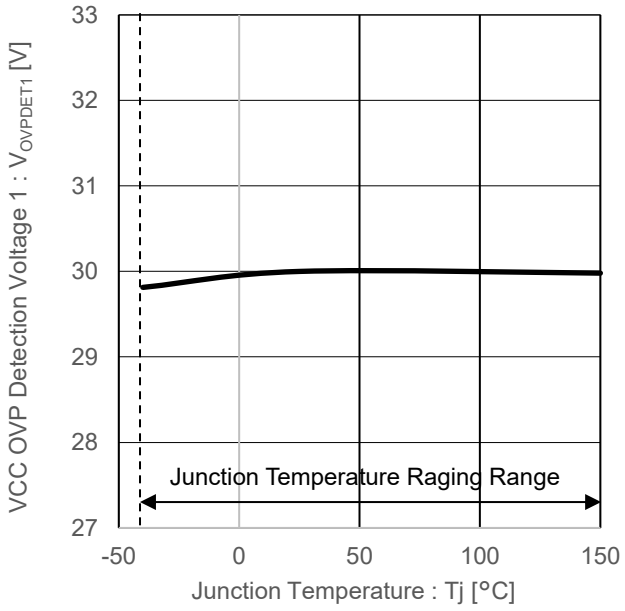


Figure 15. VCC OVP Detection Voltage 1 vs Junction Temperature
(PRTSEL Setting: Pump Application)

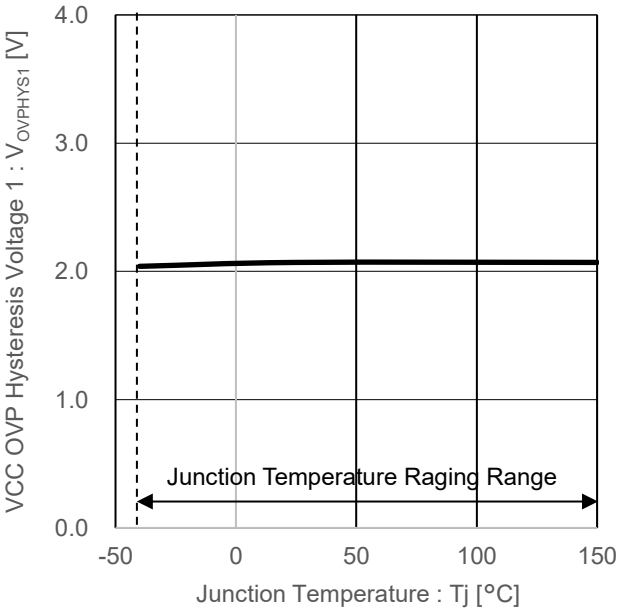


Figure 16. VCC OVP Hysteresis Voltage 1 vs Junction Temperature

Typical Performance Curves − continued

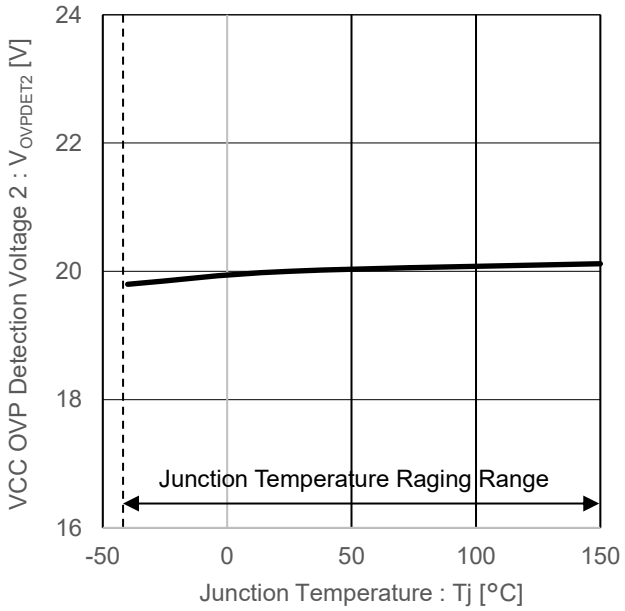


Figure 17. VCC OVP Detection Voltage 2 vs Junction Temperature
(PRTSEL Setting : Fan Motor Application)

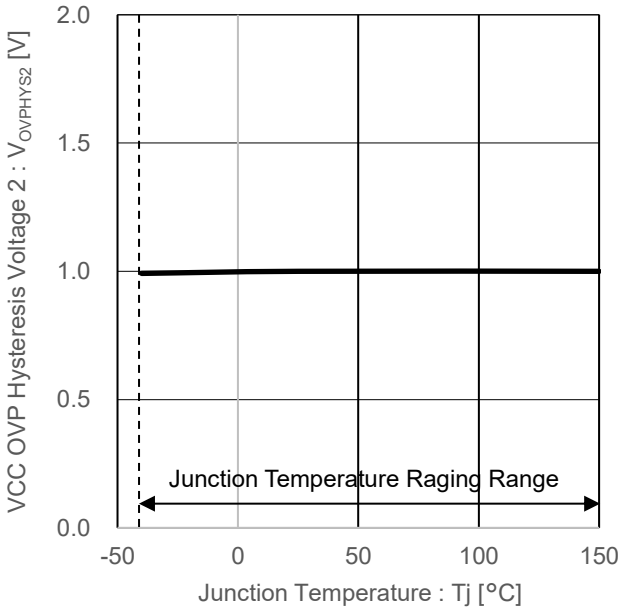


Figure 18. VCC OVP Hysteresis Voltage 2 vs Junction Temperature
(V_U = V_V = V_W = 18 V)

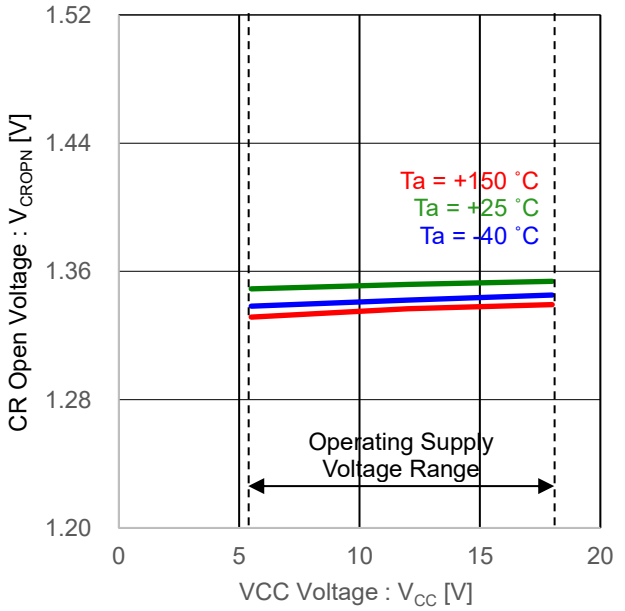


Figure 19. CR Open Voltage vs VCC Voltage
(V_{PRTSEL} = 0 V)

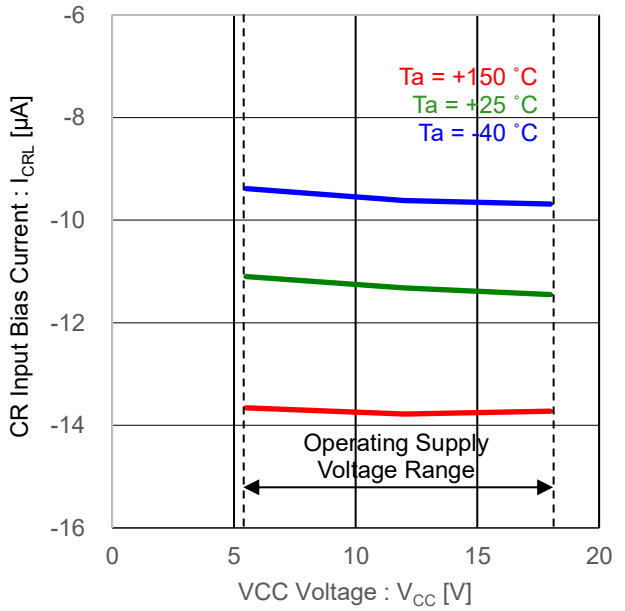


Figure 20. CR Input Bias Current vs VCC Voltage
(V_{CR} = V_{PRTSEL} = 0 V)

Typical Performance Curves − continued

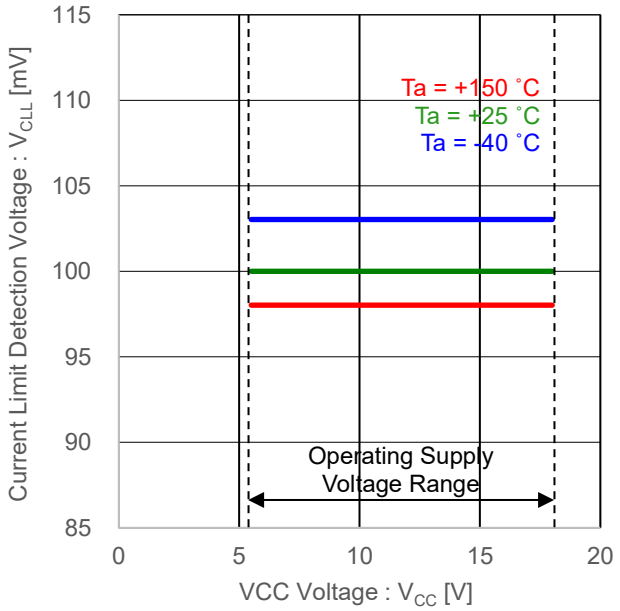


Figure 21. Current Limit Detection Voltage vs VCC Voltage

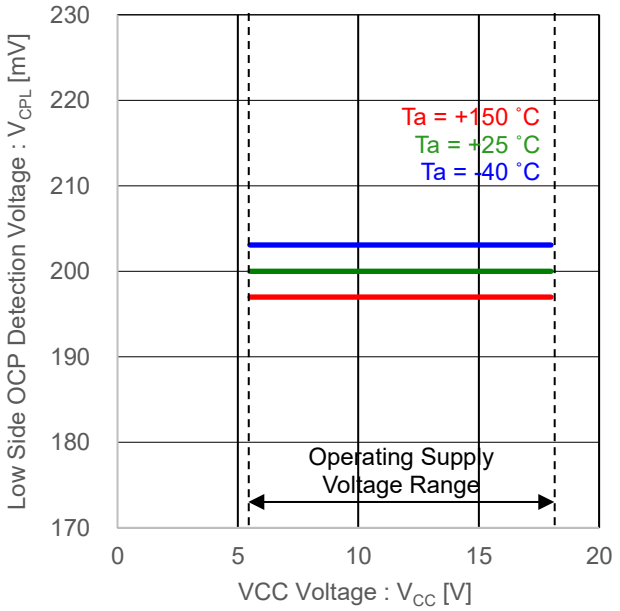


Figure 22. Low Side OCP Detection Voltage vs VCC Voltage

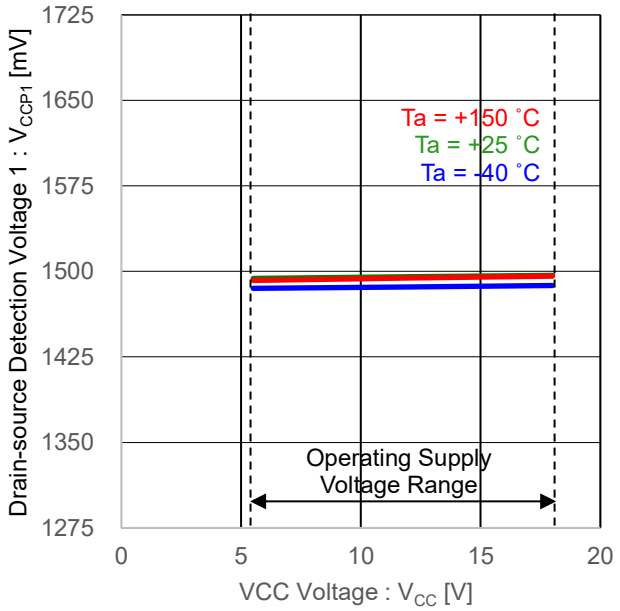


Figure 23. Drain-source Detection Voltage 1 vs VCC Voltage

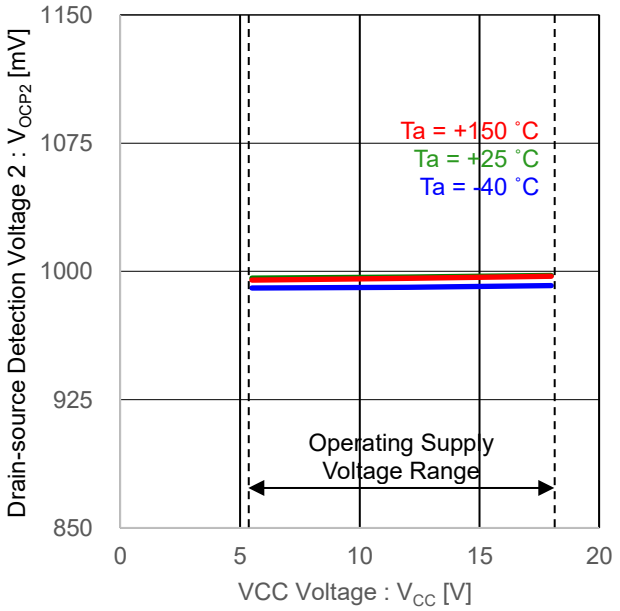


Figure 24. Drain-source Detection Voltage 2 vs VCC Voltage

Typical Performance Curves − continued

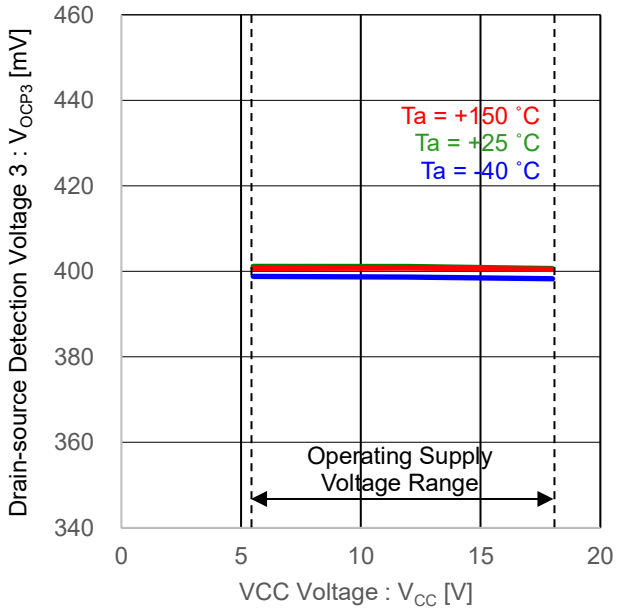


Figure 25. Drain-source Detection Voltage 3 vs VCC Voltage

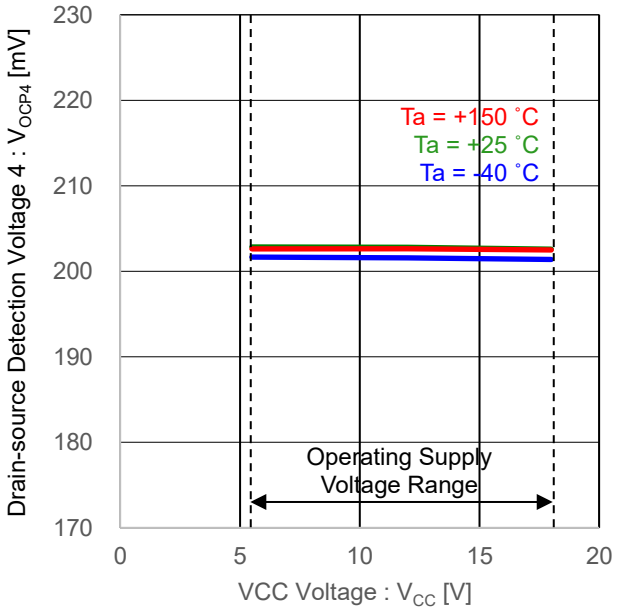


Figure 26. Drain-source Detection Voltage 4 vs VCC Voltage

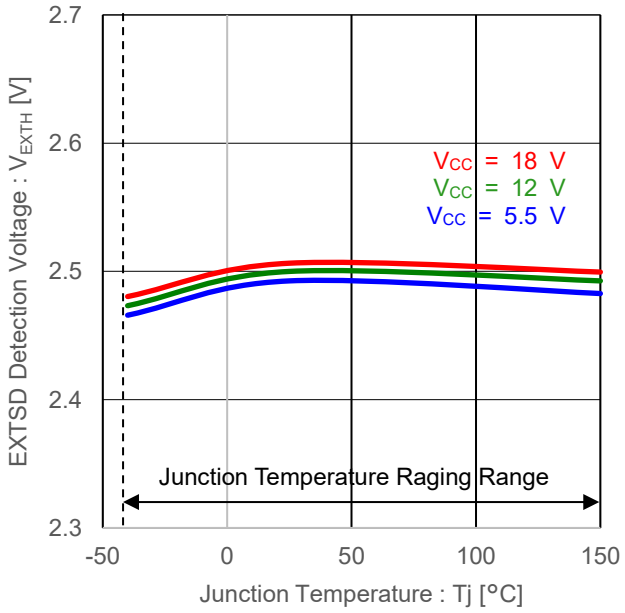


Figure 27. EXTSD Detection Voltage vs Junction Temperature

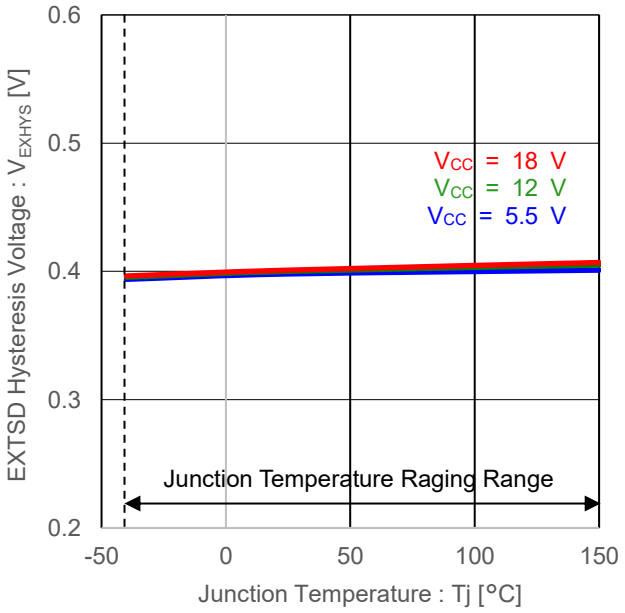


Figure 28. EXTSD Hysteresis Voltage vs Junction Temperature

Typical Performance Curves − continued

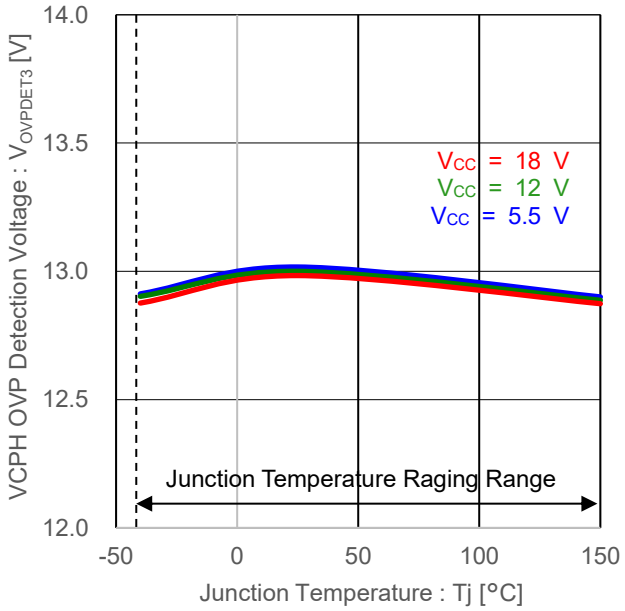


Figure 29. VCPH OVP Detection Voltage vs Junction Temperature

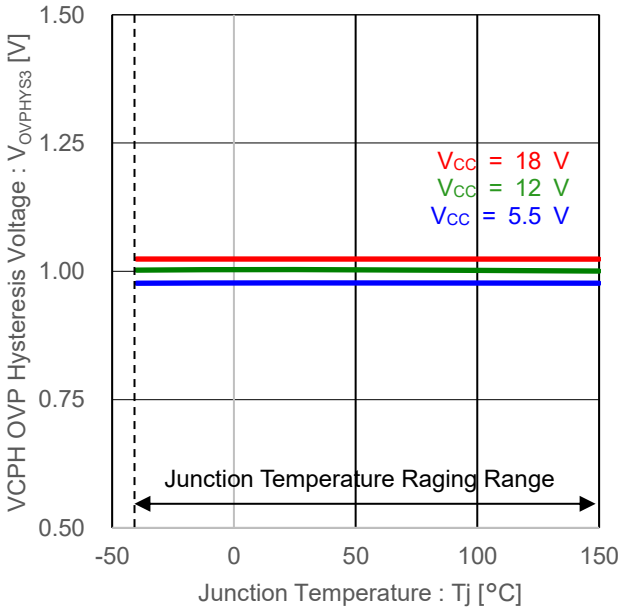


Figure 30.VCPH OVP Hysteresis Voltage vs Junction Temperature

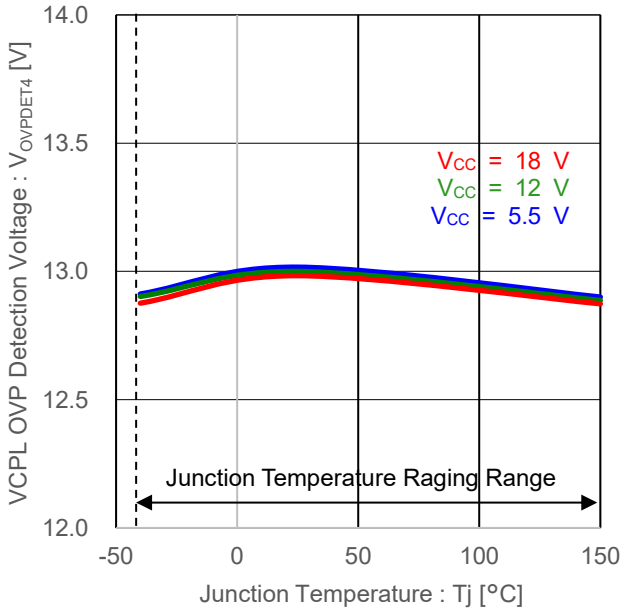


Figure 31. VCPL OVP Detection Voltage vs Junction Temperature

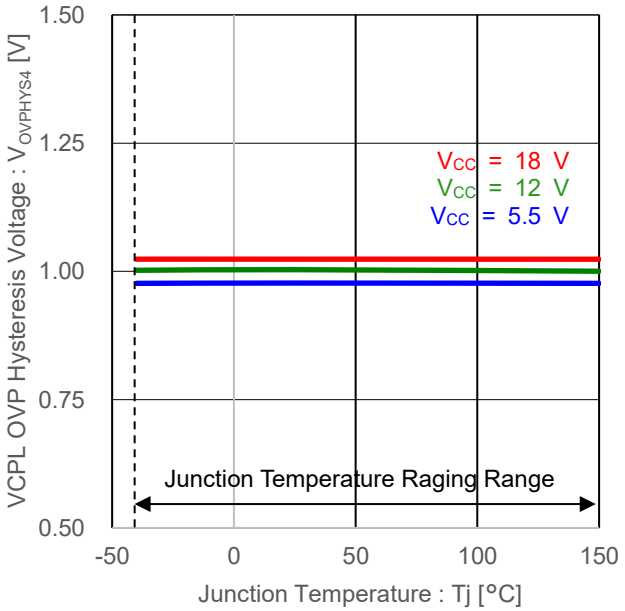


Figure 32. VCPL OVP Hysteresis Voltage vs Junction Temperature

Typical Performance Curves − continued

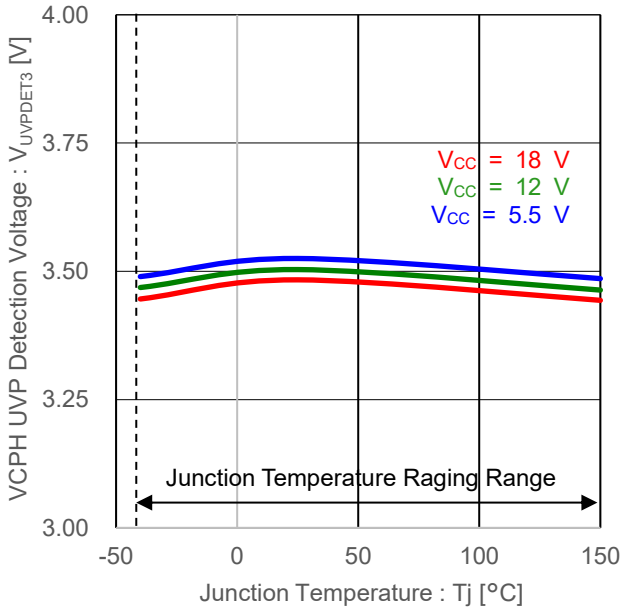


Figure 33. VCPH UVP Detection Voltage vs Junction Temperature

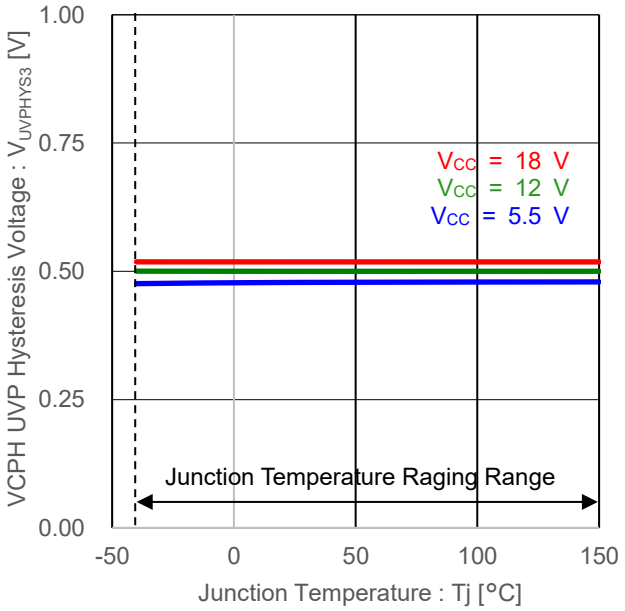


Figure 34. VCPH UVP Hysteresis Voltage vs Junction Temperature

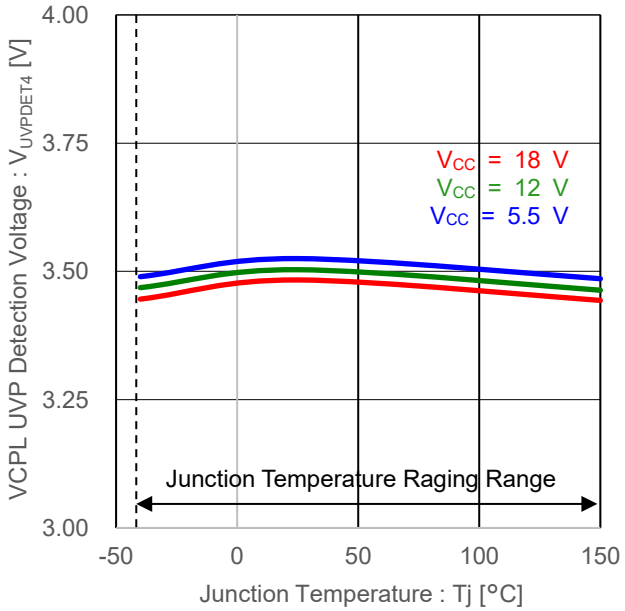


Figure 35. VCPL UVP Detection Voltage vs Junction Temperature

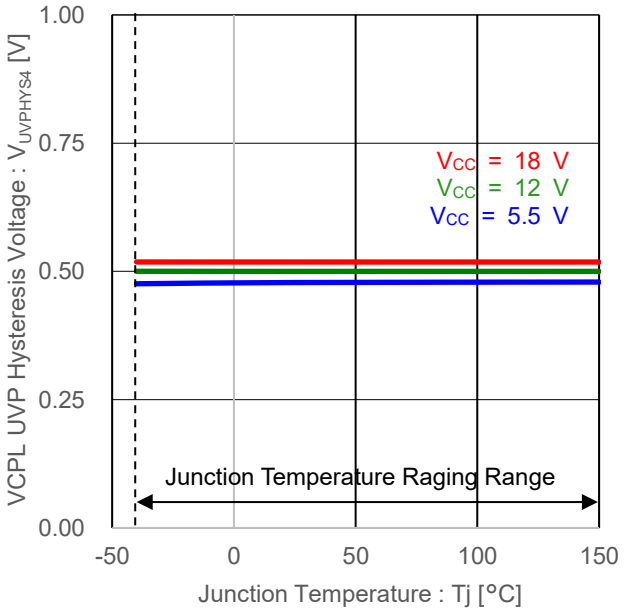


Figure 36. VCPL UVP Hysteresis Voltage vs Junction Temperature

Typical Performance Curves − continued

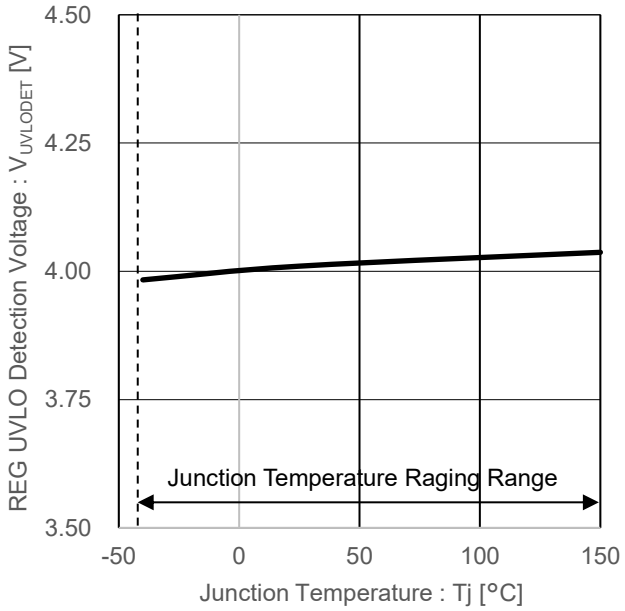


Figure 37. REG UVLO Detection Voltage vs Junction Temperature

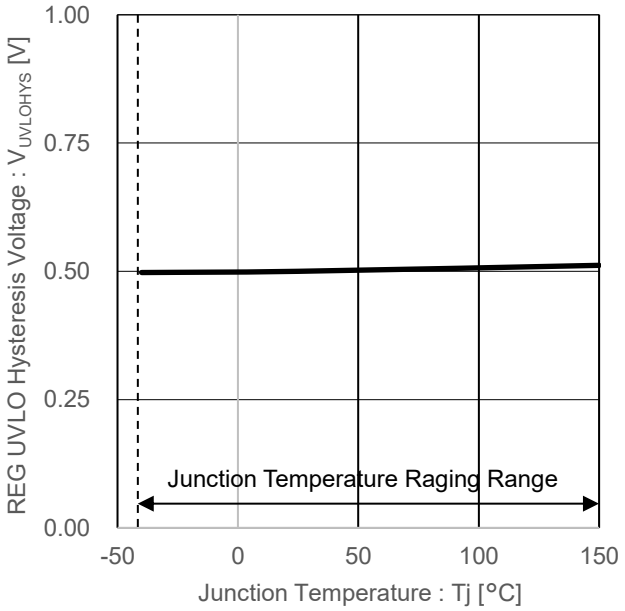


Figure 38. REG UVLO Hysteresis Voltage vs Junction Temperature

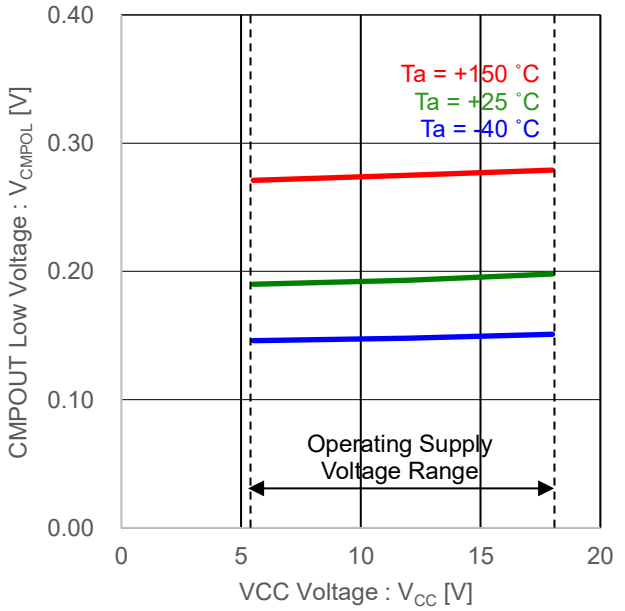


Figure 39. CMPOUT Output Low Voltage vs VCC Voltage (I_{CMPOUT} = 5 mA)

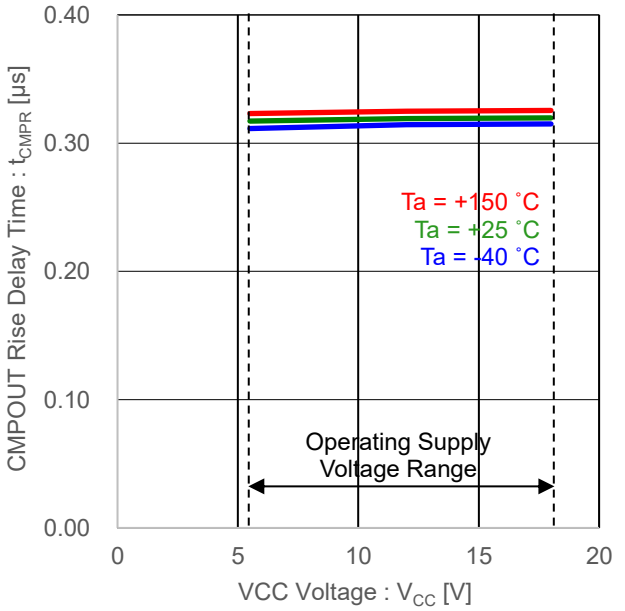


Figure 40. CMPOUT Rise Delay Time vs VCC Voltage

Typical Performance Curves − continued

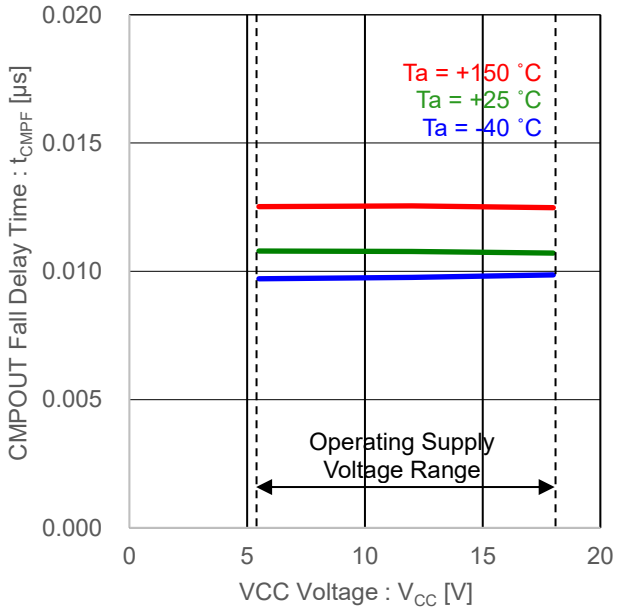


Figure 41. CMPOUT Fall Delay Time vs VCC Voltage

Application Example

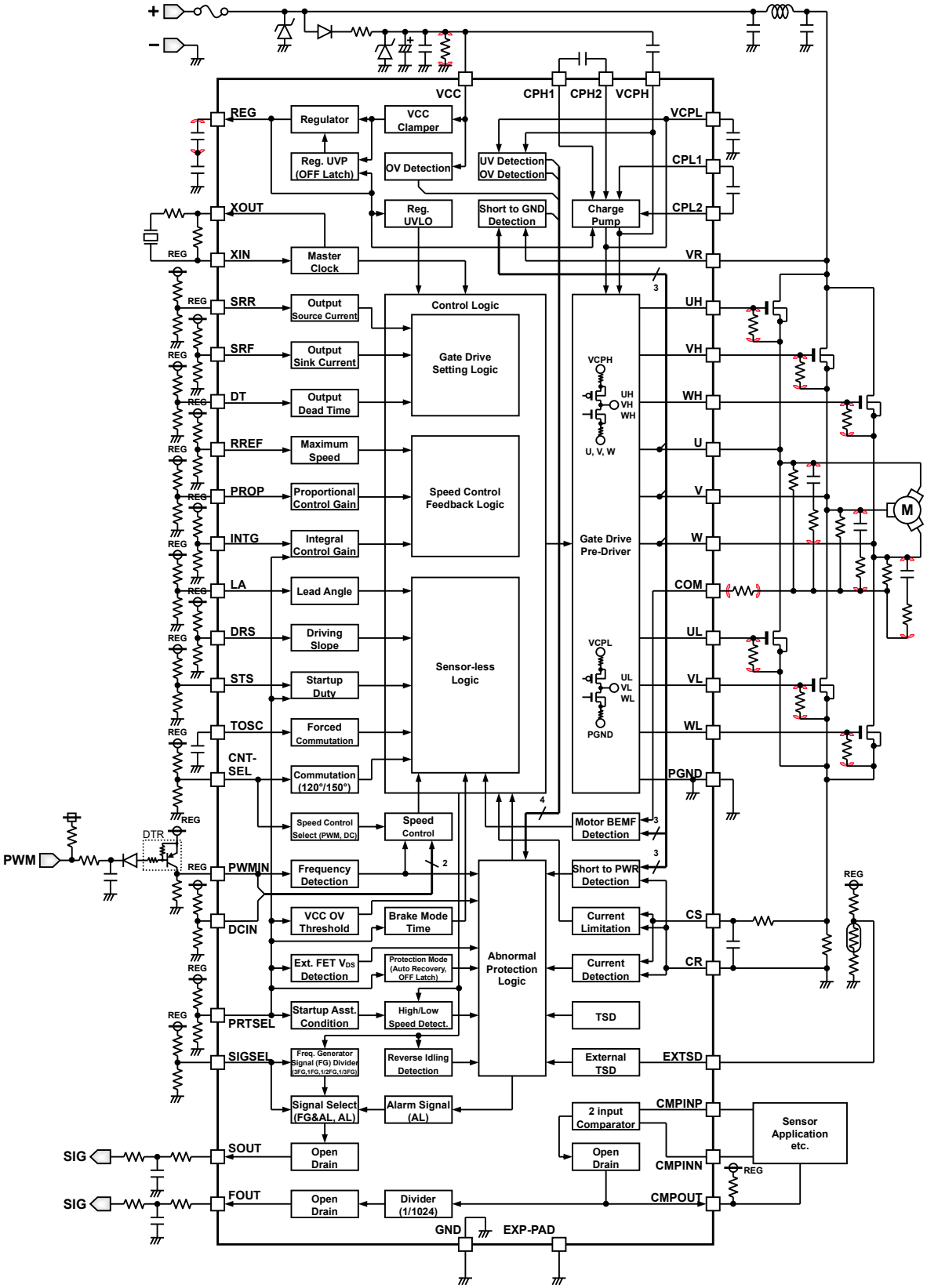


Figure 42. Speed Control Application Circuit

Board Design Note

1. The IC power supply, the IC ground, the motor outputs and the motor ground lines are made as wide as possible.
2. The IC ground is arranged to the ground connector of PCB as close as possible.
3. The bypass capacitors connected to the VCC pin and external FETs are placed as close as possible to the VCC pin and external FETs.

Application Circuit Design Note

1. **Power Supply Input Pin (VCC)**
   The motor's Back EMF and PWM switching noise may affect the VCC pin voltage. To regulate or stabilize the VCC voltage supply, place the bypass capacitor to the IC pin as close as possible. Increase the value of the bypass capacitor if the IC needs to drive higher current or if it is experiencing higher Back EMF. Note that the VCC pin voltage should not exceed the maximum absolute ratings. It is effective to add a zener diode not exceeding the absolute maximum ratings.
   To decrease the AC impedance in wide frequency bandwidth, place a ceramic capacitor (0.01 µF to 0.1 µF) in parallel with the electrolytic capacitor. Take note that reversing the voltages of the VCC pin and the GND pin may destroy the IC.

2. **Ground Input Pins (GND, PGND)**
   The GND must have impedance as low as possible and must always be maintained as the lowest voltage potential.
   This is to reduce the noise caused by the switching current, and to make the internal standard voltages stable.
   Avoid having common impedance with other devices' GND line.

3. **Boosted Voltage Output Pins for high side gate drive (VCPH, CPH2, CPH1)**
   Built-in charge pump circuit for high side external FET drive generates boost voltage VCPH = V_{CC} + 9.5 V (Typ) by connecting a capacitor of VCPH - VCC = 1 µF or more and CPH2 - CPH1 = 0.1 µF (Typ).
   Check the motor operation before deciding.

4. **Boosted Voltage Output Pins for low side gate drive (VCPL, CPL2, CPL1)**
   Built-in charge pump circuit for low side external FET drive generates boost voltage VCPL = 9.5 V (Typ) by connecting a capacitor of VCPL - GND = 1 µF or more and CPL2 - CPL1 = 0.1 µF (Typ).
   Check the motor operation before deciding.

5. **High Side Gate Drive Output Pins (UH, VH, WH)**
   The external FET high side gate drive voltage is V_{CC} + 9.5 V (Typ).
   Note that 15 kΩ (Typ) resistor is built between these pins (UH, VH, WH) and the detection voltage input pins (U, V, W) on each phase.

6. **Low Side Gate Drive Output Pins (UL, VL, WL)**
   The external FET low side gate drive voltage is 9.5 V (Typ).
   Note that 15 kΩ (Typ) resistor is built between these pins (UL, VL, WL) and the PGND pin on each phase.

7. **Detection Voltage Input Pins (U, V, W)**
   Connect these pins to the source side of external high side FET. High side external FET driver circuit generates high side pre-driver output voltage based on these pins. Do not leave these pins open, because the voltage higher than expected can be applied to the high side FET and cause destruction. Also, this pin can swing the GND potential or less under the influence of Back EMF by the motor, and cause malfunction or destruction if it reaches -4 V or less.
   Preventive measures, such as inserting schottky diodes to the GND, can avoid such unexpected IC destruction.

8. **Motor Midpoint Detection Voltage Input Pin (COM)**
   When the motor has middle point wiring, connect the wiring to the COM pin. When not so, the ideal middle point is made by connecting resistors between the U, V, and W pins and the COM pin. It is recommended that resistors are 330 Ω to 1 kΩ. After checking a motor operation, decided the values. In addition, be careful about the power dissipation of the resistors.

9. **External CLK Input Pin (XIN) / Output Pin (XOUT)**
   Connect a feedback resistor and a ceramic oscillator between XIN and XOUT, and a damping resistor between XOUT and ceramic oscillator.
   Use 10 MHz (Typ) for the ceramic resonator.

10. **Motor Power Supply Reference Voltage Input Pin (VR)**
    Connect to the drain side of the external high side FET. It serves as a reference voltage for detection of abnormal protection of the drain-source voltage of the external high side FET.

11. **Low Side Current Reference Voltage Input Pin (CR)**
    The CR must have impedance with the GND as low as possible and maintained as the lowest voltage potential. It serves as a reference voltage for detection of abnormal protection of the drain-source voltage of the external low side FET.

12. **Low Side Current Detection Voltage Input Pin (CS)**
    Connect a shunt resistor for detecting the motor drive current between the CS and CR pins and connect a low pass filter to the CS pin. Design the PCB layout with consideration for the wiring that is less affected by noise so that false detection of current limit does not occur.

Application Circuit Design Note - continued

13. Reference Voltage (5 V) Output Pin (REG)
The REG pin is 5 V (Typ) for reference voltage output. It is recommended to connect 1 µF or more capacitor to the REG pin.

14. Speed Control PWM Duty Input Pin (PWMIN)
The PWM signal duty for the PWMIN pin can control motor speed. Note that the PWMIN pin is internally pulled up to the REG pin by 110 kΩ (Typ) resistor. In addition, the active logic setting can be selected by the speed control system setting pin (CNTSEL) (See Page 34).

15. External Temperature Detection Voltage Input Pin (EXTSD)
It is possible to operate the overheat protection function at the desired temperature by arranging the thermistor resistance near the parts that require temperature protection and inputting the resistance voltage divider including the thermistor resistance. Design the PCB layout with consideration for the wiring that is less affected by noise so that false detection of over temperature protection does not occur.

16. Each Setting Input Pins (PRTSEL, CNTSEL, SIGSEL, DCIN, RREF, INTG, PROP, STS, DRS, LA, DT, SRR, SRF)
By setting 13 parameters, optimum parameter selection for various applications is possible. For details of each parameter, refer to the operation description.

17. Capacitor Connection for Forced Commutation Period Setting Pin (TOSC)
Due to the capacitance of the board, inner oscillator can do free running oscillation even if the TOSC pin is open but open setting is forbidden because this condition is unstable operation. The right capacitance value depends on the application. Check the capacitance value range for normal operation and determine the appropriate value. Normally, the bigger the magnetic poles of the motor, the smaller the value of the capacitance. And the bigger the moment of inertia of the motor, the bigger value the value of the capacitance, too. Considering to the motor characteristic, operating environment and the correlation with the STS setting practice the start-up test under sufficient conditions and choose the margin.

18. Rotation Pulse Signal/Abnormal Status Signal Output Pin (SOUT)
The SOUT pin signal setting can be selected by the signal output setting input pin (SIGSEL). It is open drain output, so this pin must be pulled up to external voltage by 1 kΩ to 100 kΩ resistors.
Note that the SOUT pin voltage and current should not exceed the maximum absolute ratings.

19. Comparator Input Pins (CMPINP, CMPINN)
It is a comparator independent of the motor drive control. When not using, fix the input logic of the CMPINP and the CMPINN pins within the input range.

20. Comparator Output Pin (CMPOUT)
The CMPOUT pin is open drain output, so this pin must be pulled up to the REG pin or external voltage by 10 kΩ to 100 kΩ resistors.
When pulling up with an external voltage, note that the CMPOUT pin voltage and current do not exceed the absolute maximum ratings.

21. CMPOUT Divided Signal Output Pin (FOUT)
The FOUT pin signal is a signal that divides the CMPOUT signal by 1024. It is open drain output, so this pin must be pulled up to external voltage by 1 kΩ to 100 kΩ resistors.
Note that the FOUT pin voltage and current should not exceed the maximum absolute ratings.

22. No Connection Pin (N.C.)
No connection pin (N.C.) is unconnected in the internal IC. But, because of unanticipated troubles such as oscillations may happen, this pin is open on-board wiring pattern.

23. Package Rear Exposed PAD (EXP-PAD)
The back-heatsink, and the ground pin adjust to same electric potential.

Description of Operation

1. Start-up Sequence

BD16851AEKV-C is a pre-driver IC for three phase brushless DC motor without using a hall sensor for position detection. After power ON and speed control input, it operates with a start duty setting (STS) until the 40th time of induced voltage detection. It then transitions to speed control with a speed control PWM duty input (PWMIN) for stable sensor less drive.

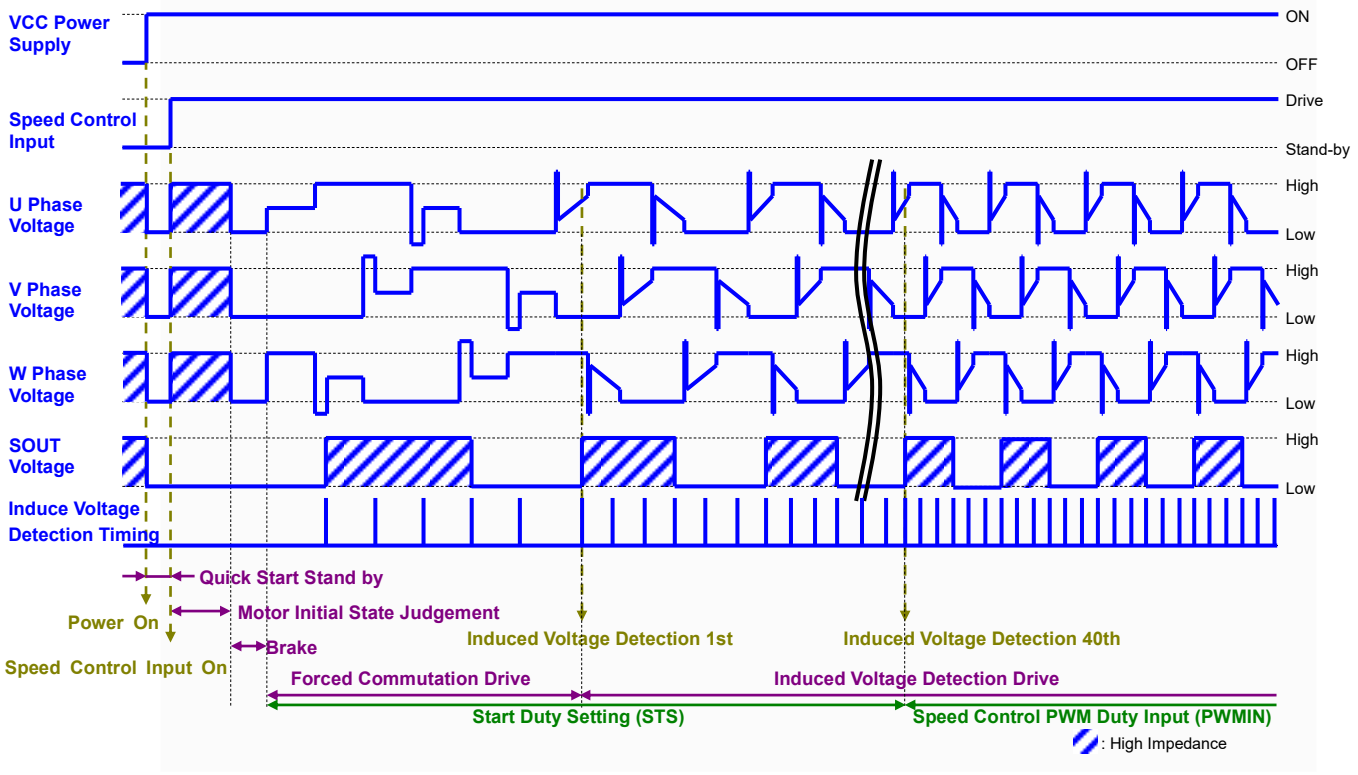


Figure 43. Start-up Sequence Summary Timing Chart
(Judge the Motor stopping and select the initial logic of SOUT signal output is Low)

(1) Quick Start Stand by

After the power ON, the motor drive output is low logic (brake) and SOUT output is the logic according to SIGSEL settings until the speed control input is ON.

(2) Motor Initial State Judgement

After power ON and speed control input, judge the Motor state (Forward rotation, Reverse rotation, Stop). The transition state differs depending on the judgment. The motor drive output is high impedance and SOUT output is the logic according to SIGSEL setting.

Table 1. Motor Initial State Judgement Table

Judgement	Condition	Transmit State
Forward	Induced Voltage (Forward rotation Logic) Detection	Induced Voltage Detection Drive
Reverse	Induced Voltage (Reverse rotation Logic) Detection	Reverse Protection
Stop	Others	Brake

(3) Brake

If motor initial state judgement is stop, make all motor driver outputs low logic (low short brake) to stabilize motor and change it to forced commutation drive. SOUT output is the logic according to SIGSEL setting.

1. Start-up Sequence − continued

(4) Forced Commutation Drive

The motor drive output logic is forced commutation in synchronization with the reference signal inside the IC. When the induced voltage generated from the motor is detected between the Min forced commutation period and the Max forced commutation period by this forced commutation drive, the mode shifts to the induced voltage detection drive. When the induced voltage cannot be detected normally, forced commutation drive is repeated with the start assist.

(a) Forced Commutation Period

The forced commutation period is determined by the oscillation period of the TOSC pin and the range of two value inside the IC. The relationship between the oscillation period by the external capacitor connected between the TOSC pin and GND and the forced commutation period (Min and Max) is as follows.

$$t_{TOSC} = \{C_{TOSC} \times (|I_{DTOSC}| + |I_{CTOSC}|) \times (V_{TOSCH} - V_{TOSCL})\}/(|I_{DTOSC} \times I_{CTOSC}|) \quad [s]$$

$$t_{OSCS} = t_{TOSC} \times 20 \quad [s]$$

$$t_{OSCL} = t_{TOSC} \times 50 \quad [s]$$

where:
t_{TOSC} is the TOSC Oscillation Period [s]
C_{TOSC} is the TOSC Capacitance Value [F]
I_{DTOSC} is the TOSC Discharge Current [A]
I_{CTOSC} is the TOSC Charge Current [A]
V_{TOSCH} is the TOSC High voltage [V]
V_{TOSCL} is the TOSC Low voltage [V]
t_{OSCS} is the Min Forced Commutation Period [s]
t_{OSCL} is the Max Forced Commutation Period [s]

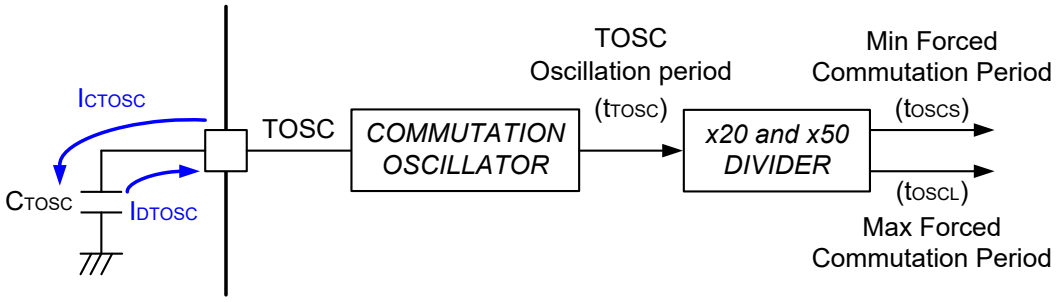


Figure 44. TOSC Internal Circuit

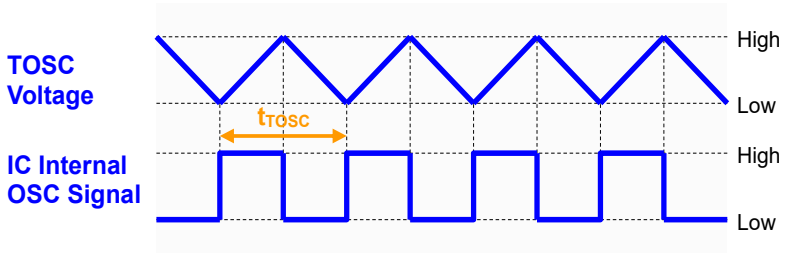


Figure 45. TOSC Timing Chart

(ex.) TOSC capacitance is 1000 pF, TOSC period is 50 µs, the min forced commutation period is as little as 1.0 ms and up to 2.5 ms.

$$t_{TOSC} = \frac{1000\times10^{-12}\times(|40\times10^{-6}|+|-40\times10^{-6}|)\times(2.0-1.0)}{(|40\times10^{-6}\times-40\times10^{-6}|)} = 50 \times 10^{-6} \quad [s]$$

$$t_{OSCS} = 50 \times 10^{-6} \times 20 = 1.0 \times 10^{-3} \quad [s]$$

$$t_{OSCL} = 50 \times 10^{-6} \times 50 = 2.5 \times 10^{-3} \quad [s]$$

(4) Forced Commutation Drive - continued

(b) TOSC Capacitance Right Value Setting

The right capacitance value depends on the application. Check the capacitance value range for normal operation and determine the appropriate value. Normally, the bigger the magnetic poles of the motor, the smaller the value of the capacitance. And the bigger the moment of inertia of the motor, the bigger value the value of the capacitance, too. Considering to the motor characteristic, operating environment and the correlation with the STS setting practice the start-up test under sufficient conditions and choose the margin.

Table 2. Forced Commutation Period Table (Reference Value)

TOSC value (C_{TOSC}) [pF]	Min Period (t_{OSCS}) [ms]	Max Period (t_{OSCL}) [ms]
100	0.10	0.25
150	0.15	0.38
220	0.22	0.55
330	0.33	0.83
470	0.47	1.18
680	0.68	1.70
1000	1.00	2.50
1500	1.50	3.75
2200	2.20	5.50
3300	3.30	8.25
4700	4.70	11.75
6800	6.80	17.00
10000	10.00	25.00

(c) Start Assist

When the induced voltage is undetected or erroneous detection after switching the motor drive output logic in forced commutation drive eight times, the forced commutation drive returns to the brake and the forced commutation drive sequence is repeated.

It can select one of the two methods of starting assist is once or continuing for 1 s by the protection system setting input (PRTSEL) (See Page 33) described later.

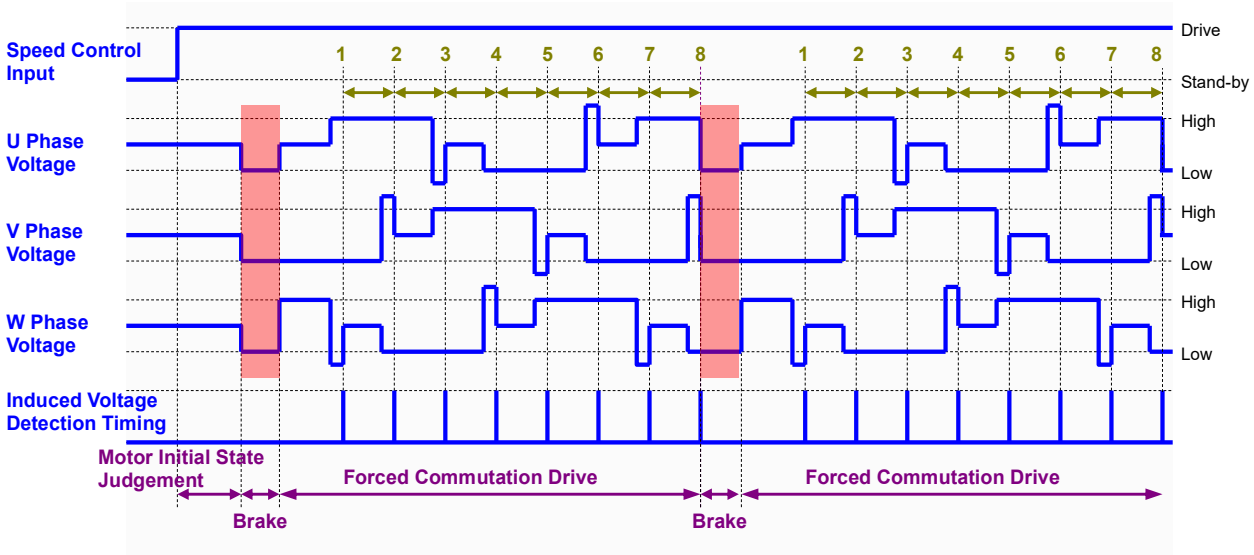


Figure 46. Start Assist Timing Chart

Description of Operation - continued

2. Sensor-less Drive

It can select one of the two methods of 120° commutation drive and 150° commutation PWM soft switching drive by the speed control setting input (CNTSEL) (See Page 34) described later.

(1) 120° Commutation Drive

Detects induced voltage and energizes every 120° electrical angle.

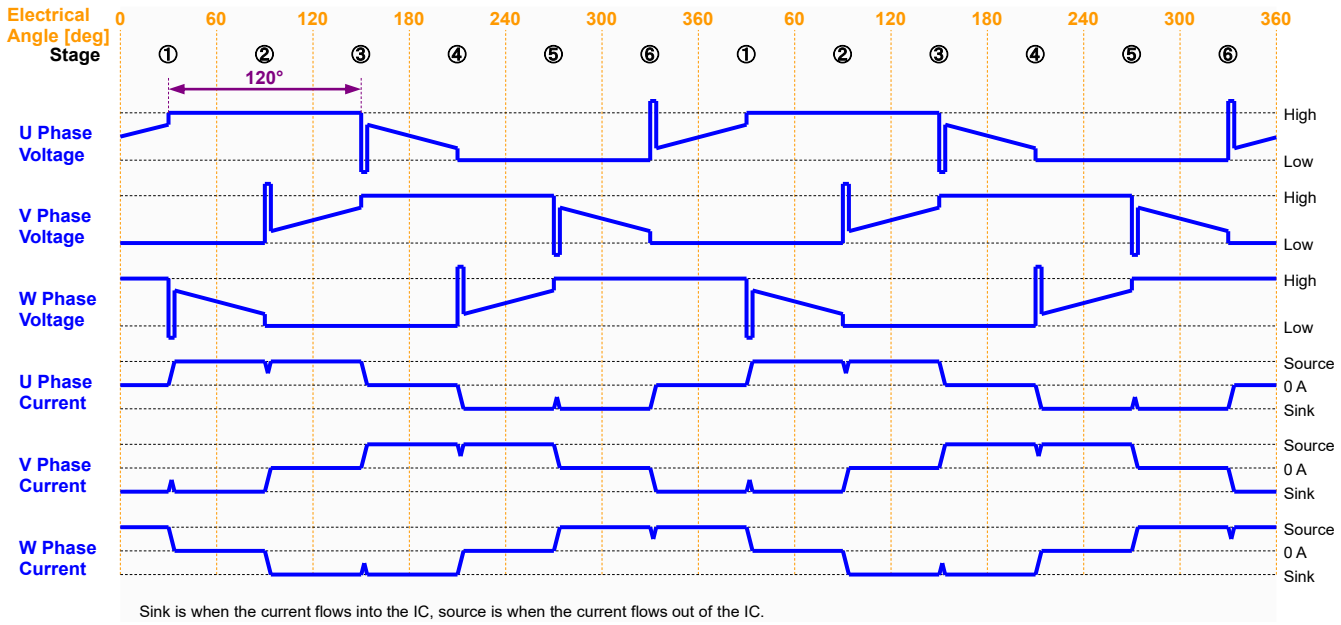


Figure 47. 120° Commutation Drive Timing Chart

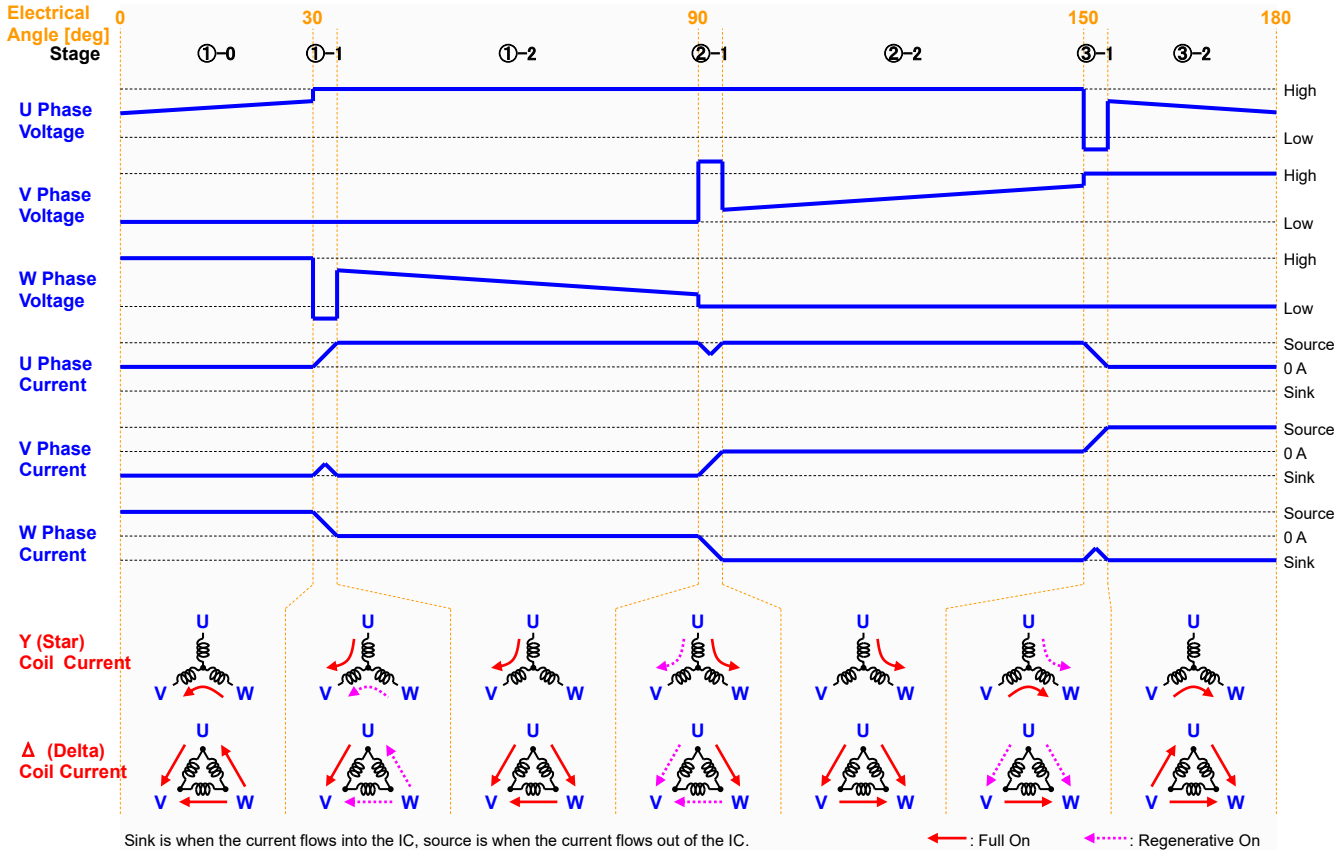


Figure 48. Motor Coil Current Change when120° Commutation Drive

2. Sensor-less Drive − continued

(2) 150° Commutation PWM Soft Switching Drive

To reduce the echo noise from motor, during motor drive output phase switching, each phase voltage will PWM drive. By gradually changing the duty, the output current is slow changing. Electrical degree becomes 150° when add up PWM soft switching section and full on section.

The PWM frequency of Soft Switching is 78 kHz (Typ).

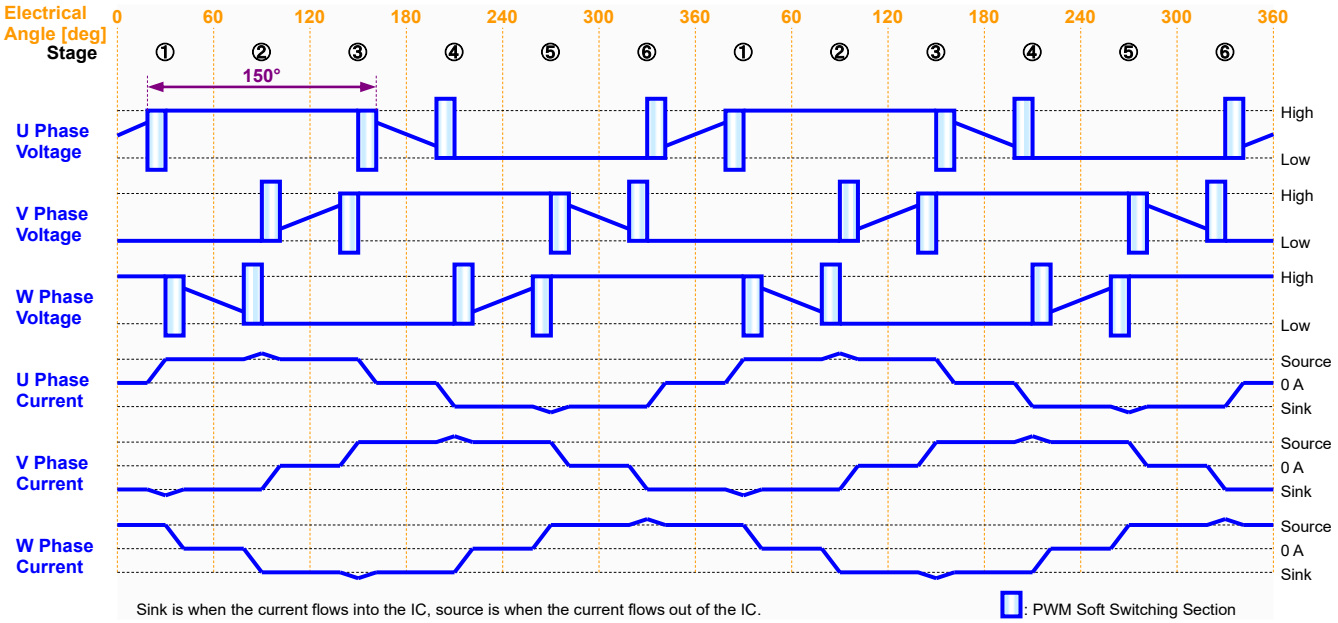


Figure 49. 150° Commutation PWM Soft Switching Drive Timing Chart

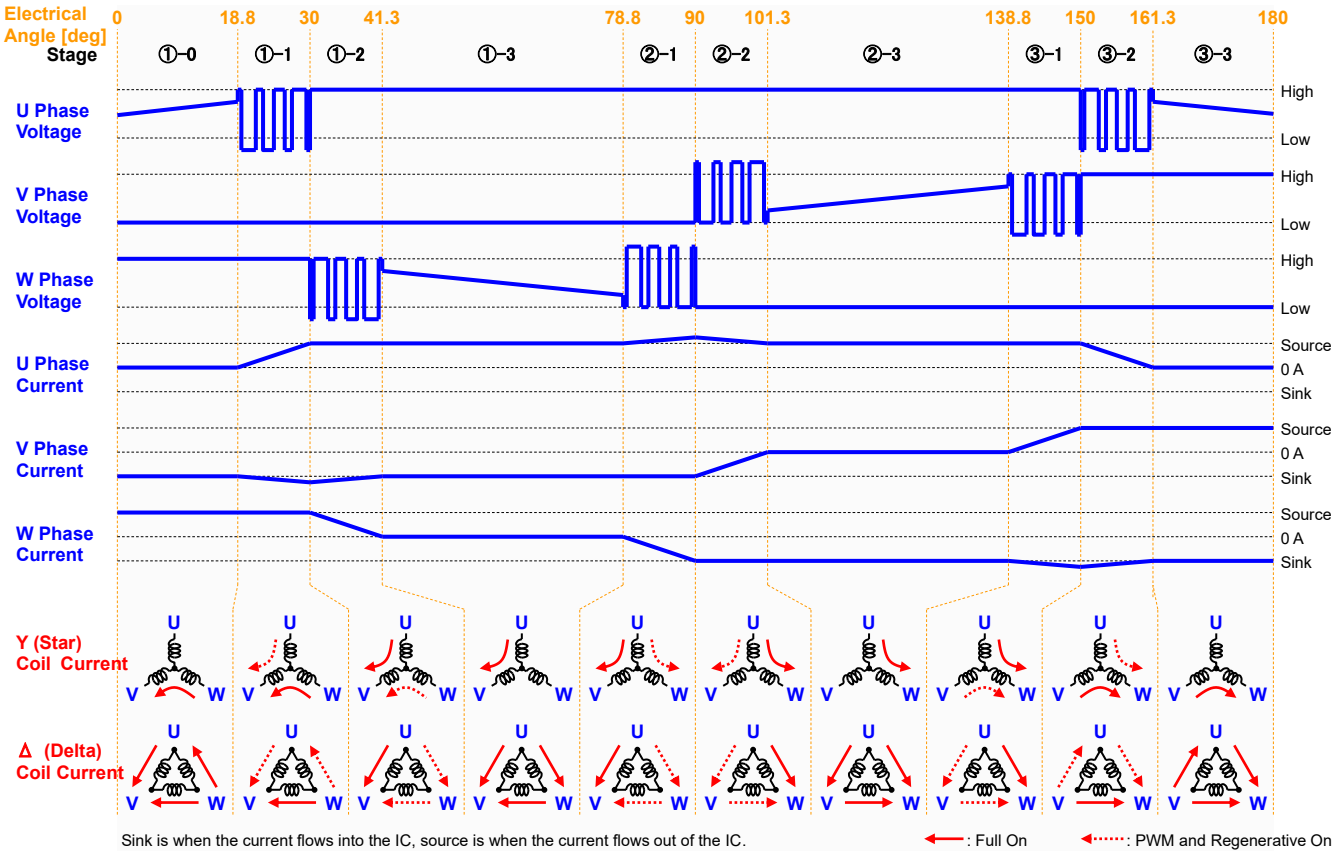


Figure 50. Motor Coil Current Change when150° Commutation PWM Soft Switching Drive
(PWM Duty Width is Conception image)

2. Sensor-less Drive − continued

(3) Motor Midpoint Detection Voltage

When not so, the ideal middle point is made by connecting resistors between the U, V, and W pins and the COM pin. It is recommended that resistors are 330 Ω to 1 kΩ. After checking a motor operation, decided the values. In addition, be careful about the power dissipation of the resistors.

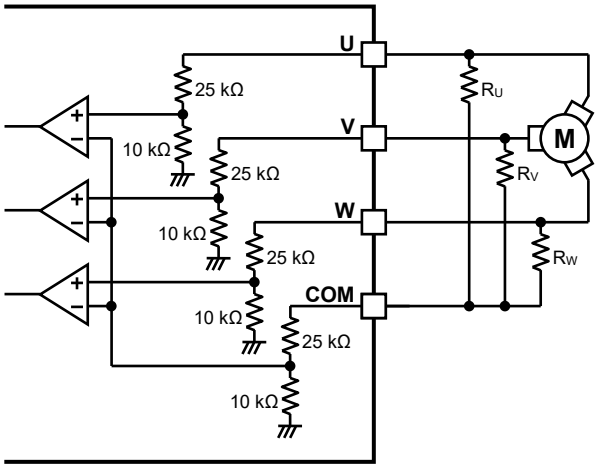


Figure 51. Motor Midpoint Detection Voltage Input

Description of Operation - continued

3. A/D Convertor Sampling

(1) Setting Value Sampling Sequence

The voltage input set by resistance voltage division is obtained by constantly cycling PRTSEL, CNTSEL, SIGSEL, DCIN, RREF, INTG, PROP, STS, DRS, LA, DT, SRR, and SRF in that order.

(2) Sampling Resolution and Number of Settings

A/D convertor is a sampling resolution of 8 bit (256 steps) in the range where the zero scale is GND and the full scale is V_{REG}.
The number of settings for each parameter is as follows.
It is recommended that the input voltage of each pin be set to the center value of the input voltage range of the setpoint.

Table 3. Number of Input Settings and Function

Pin Name	Number of Settings	Function
PRTSEL	16	Protection system setting
CNTSEL	16	Speed control system setting
SIGSEL	16	SOUT signal output setting
DCIN	256	Speed control DC voltage
RREF	16	Speed control maximum speed setting
INTG	256	Speed control (Integral) gain setting
PROP	64	Speed control (Proportional) gain setting
STS	256	Start duty setting
DRS	256	Drive slope setting
LA	16	Lead angle setting
DT	16	Output dead time setting
SRR	16	Gate Drive Output source current setting
SRF	16	Gate Drive Output sink current setting

(3) Conditions for Updating Set Values

The initial values of all parameters are acquired within 13 ms after releasing the logic reset. To update the set value, it is necessary to satisfy the two conditions of exceeding the range of ±1 LSB from the initial value and the changed value should be within the range of ±1 LSB three times.

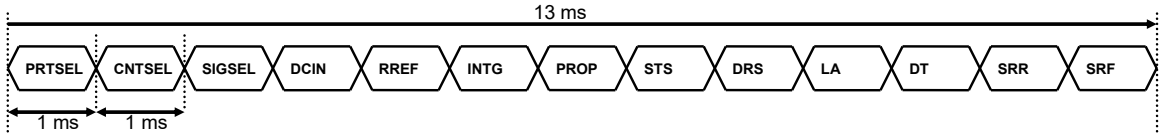


Figure 52. Parameter Setting Value Update Sequence

3. A/D Convertor Sampling − continued

(4) Protection System Setting (PRTSEL)

It can select from 16 modes according to the protection mode, select mode, and external FET characteristics.

Table 4. PRTSEL Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	Protection Mode	Select Mode	External FET Detection Voltage [mV]
16	96.86	Self-Restart	Fan Motor	1500
15	90.62			1000
14	84.36			400
13	78.12			200
12	71.86		Pump	1500
11	65.62			1000
10	59.36			400
9	53.12			200
8	46.86	OFF Latch	Fan Motor	1500
7	40.62			1000
6	34.36			400
5	28.12			200
4	21.86		Pump	1500
3	15.62			1000
2	9.36			400
1	3.12			200

Depending on the select mode, the following 6 internal configuration parameters are selected.

Table 5. Internal Parameters Linked to Select Mode

Internal Parameters	Description of Operation	Fan Motor	Pump
Over Voltage Protection Setting Voltage	12	20 V detection / 19 V release	30 V detection / 28 V release
Motor Initial State Judgement + Brake Time	1 (1), 1 (2)	50 ms + 26 ms	25 ms + 6.5 ms
Number of Start Assist	1 (4) (c)	Once	Continuing for 1 s
Speed Control (Integral) Gain Setting (INTG)	3 (9)	128 steps Setting Value x 0.5	256 steps Setting Value x 2
Speed Control (Proportional) Gain Setting (PROP)	3 (9)	64 steps Setting Value x 0.25	64 steps Setting Value x 0.25
Speed Control PWM Duty Initial Value	-	0 % (Slope Start)	100 % (Fast Start)

3. A/D Convertor Sampling − continued

(5) Speed Control System Setting (CNTSEL)

It can select from 16 modes according to the commutation mode, control signal 1.2 s after Start-up, operation in case of TEST signal input error, PWMIN active logic and speed control signal.

Table 6. CNTSEL Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	Commu-tation Mode	PWMIN Input Error	Induced voltage detections of 40 times from Start-up	Control signal up to 1.2 s from Start-up	Control signal 1.2 s after Start-up	PWMIN Active Logic
16	96.86	120°	Stop	STS	PWMIN	PWMIN	High
15	90.62						Low
14	84.36				DCIN		High
13	78.12						Low
12	71.86		DCIN Drive		PWMIN		High
11	65.62						Low
10	59.36				Full (100 %)		High
9	53.12						Low
8	46.86	150°	Stop		PWMIN		High
7	40.62						Low
6	34.36				DCIN		High
5	28.12						Low
4	21.86		DCIN Drive		PWMIN		High
3	15.62						Low
2	9.36				Full (100 %)		High
1	3.12						Low

3. A/D Convertor Sampling − continued

(6) SOUT Signal Output Setting (SIGSEL)

The initial logic of the SOUT signal output from the power on to the brake, and the SOUT signal output of normal and abnormal can be selected from 16 modes.

Table 7. SIGSEL Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	SOUT Signal Initial logic	SOUT Signal Normal	SOUT Signal Abnormal
16	96.86	Low	3FG	High
15	90.62	High		Low
14	84.36	Low		DIAG duty
13	78.12	Low	1FG	High
12	71.86	High		Low
11	65.62	Low		DIAG duty
10	59.36	Low	1/2FG	High
9	53.12	High		Low
8	46.86	Low		DIAG duty
7	40.62	Low	1/3FG	High
6	34.36	High		Low
5	28.12	Low		DIAG duty
4	21.86	High	High	Low
3	15.62			DIAG duty
2	9.36	Low	Low	High
1	3.12			DIAG duty

The rotating pulse signal is output after brake in sync with the U phase voltage. The 1FG signal outputs one cycle at an electrical angle of 360°.

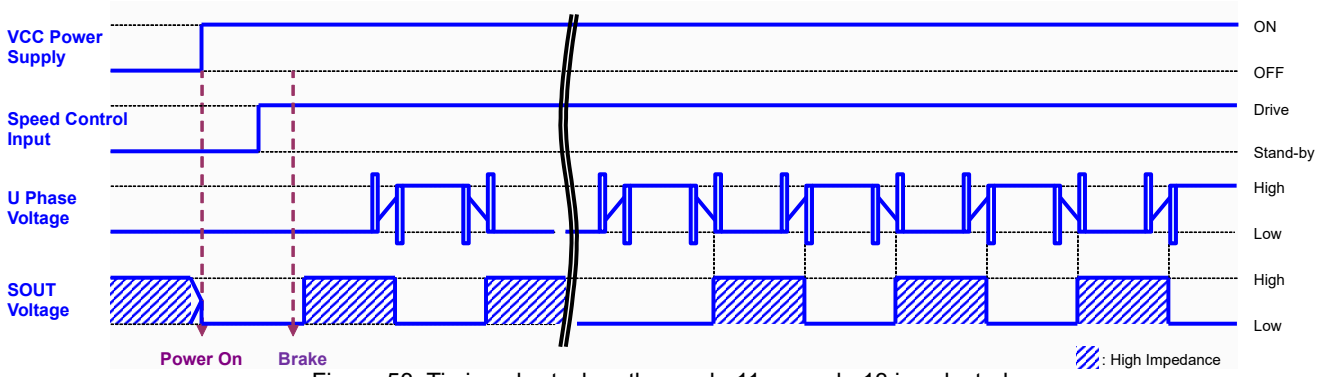


Figure 53. Timing chart when the mode 11 or mode 13 is selected

3. A/D Convertor Sampling − continued

(7) Speed Control DC Voltage (DCIN)

It can set the 256 steps in the range from GND to V_{REG}.

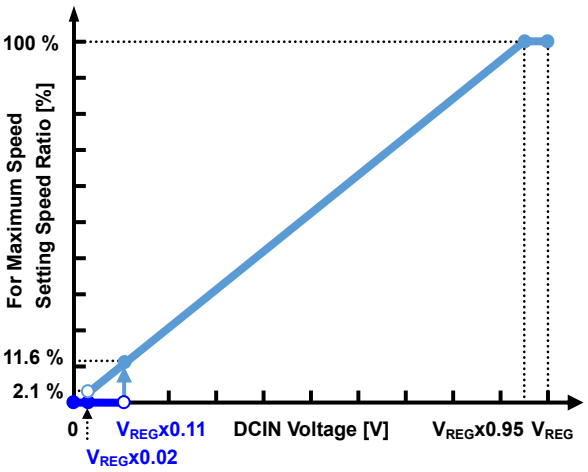


Figure 54. DCIN Control Profile

(8) Speed Control Maximum Speed Setting (RREF)

It can select from 15 modes according to the maximum speed setting (f_{MAXRPM}). When mode 1 is selected, the open control operation according to the PWMIN or DCIN control profile is performed.

Table 8. RREF Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	IC	Motor				
		f_{MAXRPM} [Hz] (1FG)	4 pole [min^{-1}]	6 pole [min^{-1}]	8 pole [min^{-1}]	10 pole [min^{-1}]	12 pole [min^{-1}]
16	96.86	800	24000	16000	12000	9600	8000
15	90.62	667	20000	13333	10000	8000	6667
14	84.36	600	18000	12000	9000	7200	6000
13	78.12	533	16000	10667	8000	6400	5333
12	71.86	467	14000	9333	7000	5600	4667
11	65.62	400	12000	8000	6000	4800	4000
10	59.36	333	10000	6667	5000	4000	3333
9	53.12	300	9000	6000	4500	3600	3000
8	46.86	275	8250	5500	4125	3300	2750
7	40.62	250	7500	5000	3750	3000	2500
6	34.36	225	6750	4500	3375	2700	2250
5	28.12	200	6000	4000	3000	2400	2000
4	21.86	175	5250	3500	2625	2100	1750
3	15.62	150	4500	3000	2250	1800	1500
2	9.36	133	4000	2667	2000	1596	1333
1	3.12	Open Control	-	-	-	-	-

3. A/D Convertor Sampling − continued

(9) Speed Control (Integral) Gain Setting (INTG), Speed Control (Proportional) Gain Setting (PROP)

It can set each setting steps in the range from GND to V_{REG}.

To prevent stalling during rapid acceleration/deceleration by speed control input, test the motor under the conditions appropriate for the motor application to be used, taking into account the motor characteristics and operating environment, and design a sufficient margin.

Table 9. INTG/PROP Parameter

PRTSEL Mode	Select Mode	INTG	PROP
1 to 4	Pump	256 steps	64 steps
9 to 12		Setting Value x 2	Setting Value x 0.25
5 to 8	Fan Motor	128 steps	64 steps
13 to 16		Setting Value x 0.5	Setting Value x 0.25

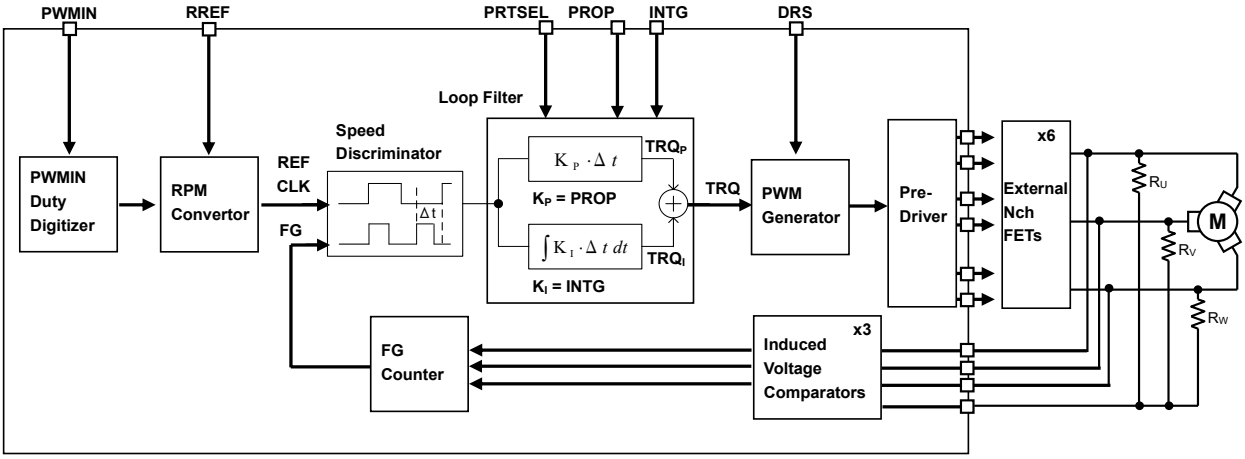


Figure 55. Speed Control Block Diagram

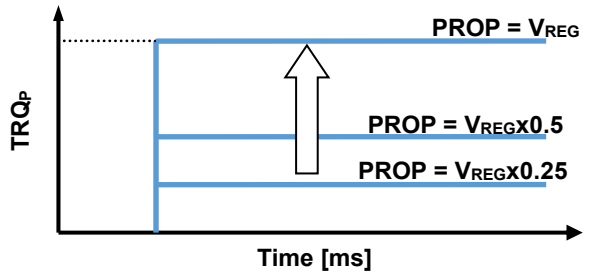


Figure 56. PROP Gain Setting Parameter Characteristics

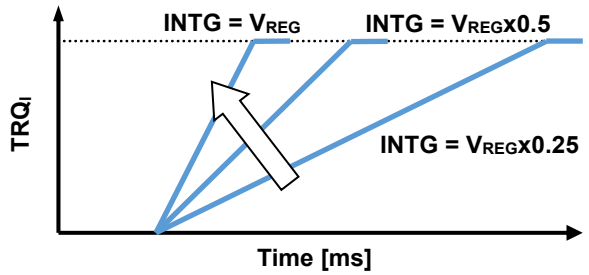


Figure 57. INTG Gain Setting Parameter Characteristics

3. A/D Convertor Sampling − continued

(10) Start Duty Setting (STS)

It can set the 256 steps in the range from GND to V_{REG}.
It can set the output duty from startup to the 40th induced voltage detection.
The lower the STS voltage, the lower the output duty and the inrush current at startup can be suppressed. On the other hand, the startup time may be long or the startup torque may be insufficient to cause startup failure.
Considering to the motor characteristic, operating environment and the correlation with the TOSC setting practice the start-up test under sufficient conditions and choose the margin.

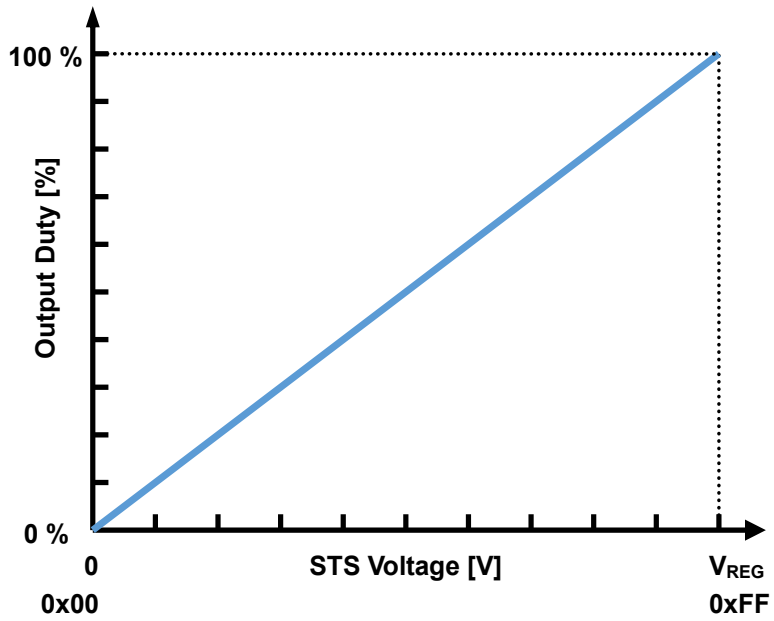


Figure 58. STS Control Profile

3. A/D Convertor Sampling − continued

(11) Drive Slope Setting (DRS)

It can set the 256 steps in the range from GND to V_{REG}.
It can set the slope setting for PWMIN input duty change after 40th induced voltage detection.
When the PWMIN input duty is changed suddenly, this is an adjustment function that prevents the output PWM duty from changing suddenly and causing the motor to step out.
The higher the DRS voltage, the longer the slope time and the slower the motor changing speed.
Considering to the motor characteristic, operating environment and the correlation with the speed control gain setting (INTG, PROP) practice the start-up test under sufficient conditions and choose the margin.

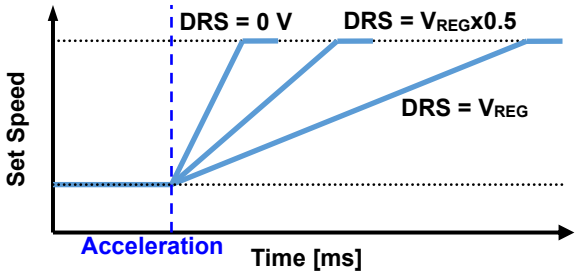


Figure 59. Change in set speed at acceleration command

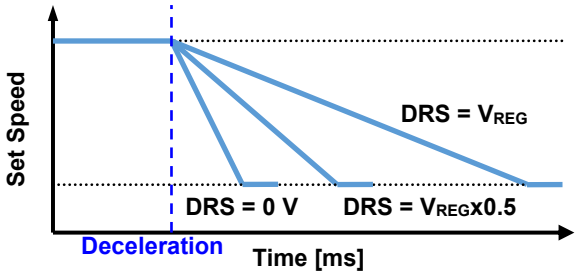


Figure 60. Change in set speed at deceleration command

(ex.) Transition time when the PWMIN input duty is changed from 50 % to 100 %.
PWM duty is resolution of 8 bit (256 steps).

$$t_{SLPMIN} = (256 - 128) \times 0.0114 = 1.459 \quad [\text{ms}]$$
$$t_{SLPMAX} = (256 - 128) \times 2.944 = 376.8 \quad [\text{ms}]$$

Table 10. Slope Time Table (Reference Value)

DRS [V]	1 step time [ms/step]	PWMIN 50 % to 100 % Transition Time [ms]
0	0.0114	1.459
V_{REG} x 0.50	1.483	189.8
V_{REG}	2.944	376.8

3. A/D Convertor Sampling − continued

(12) Lead Angle Setting (LA)

It can select from 16 modes according to the lead angle.

Table 11. LA Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	Lead Angle [°]
16	96.86	30.00
15	90.62	28.13
14	84.36	26.25
13	78.12	24.38
12	71.86	22.50
11	65.62	20.63
10	59.36	18.75
9	53.12	16.88
8	46.86	15.00
7	40.62	13.13
6	34.36	11.25
5	28.12	9.38
4	21.86	7.50
3	15.62	5.63
2	9.36	3.75
1	3.12	0.00

(13) Output Dead Time Setting (DT)

It can select from 16 modes according to the output dead time setting.
When the power supply voltage is 20 V or higher, it will automatically change to twice the set value in following table (Table 12).

Table 12. DT Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	Dead Time [µs]
16	96.86	2.0
15	90.62	1.8
14	84.36	1.6
13	78.12	1.5
12	71.86	1.4
11	65.62	1.2
10	59.36	1.0
9	53.12	0.9
8	46.86	0.8
7	40.62	0.7
6	34.36	0.6
5	28.12	0.5
4	21.86	0.4
3	15.62	0.3
2	9.36	0.2
1	3.12	0.1

3. A/D Convertor Sampling − continued

(14) Gate Drive Output Source Current Setting (SRR), Gate Drive Output Sink Current Setting (SRF)

It can select from 16 modes according to the gate drive output current for both source and sink.

Table 13. SRR/SRF Parameter

Mode	Setting (Typ)[%] (REG = 100 %)	Source Current (SRR) [mA]	Sink Current (SRF) [mA]
16	96.86	35	110
15	90.62	33	100
14	84.36	31	95
13	78.12	30	85
12	71.86	29	80
11	65.62	28	70
10	59.36	27	60
9	53.12	26	50
8	46.86	25	45
7	40.62	23	40
6	34.36	22	35
5	28.12	21	30
4	21.86	19	25
3	15.62	15	20
2	9.36	12	16
1	3.12	10	12

Description of Operation - continued

4. External CLK Input Interface

The oscillation is operated by connecting a return resistor and a ceramic resonator between XIN and XOUT, and a limiting resistor between XOUT and the ceramic resonator. Input an oscillation signal with a frequency of 10 MHz to XIN.

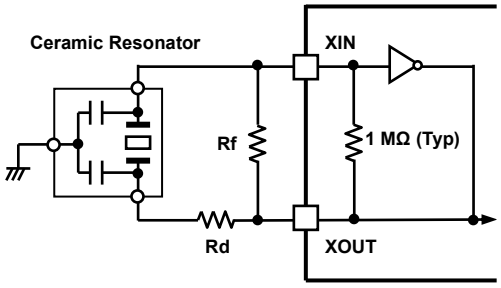


Figure 61. External CLK Input Interface Circuit

5. Regulator Output

REG output (5.0 V Typ) is built-in for resistance voltage division setting and pull-up.
Note that the REG output current should not exceed the maximum absolute ratings. For stabilization, make sure to connect the capacitor at least 1 µF against GND.
If the REG output pin is grounded, it has a function to OFF latch the REG output for protect the IC. If the OFF latch operation, it will not restart until the power is turned on again.

6. Speed Control

(1) Speed Control PWM Duty Input (PWMIN)

It can be speed controlled by the duty of the PWM signal input to PWMIN. The PWMIN pin is pulled up to the internal power supply (REG) with a resistance of 110 kΩ (Typ).
The active logic setting can be selected by the speed control system setting input (CNTSEL).
The input duty is a sampling resolution of 8 bit (256 steps).

Table 14. PWMIN Input Frequency

PWMIN Input Frequency	Operation Mode	Output
< 6.6 Hz	Protection (PWM Input Error)	OFF (Hi-Z)
6.8 Hz to 1000 Hz	Active	Normal
1050 Hz <	Protection (PWM Input Error)	OFF (Hi-Z)

Table 15. PWMIN Input Duty

	PWMIN Input Duty [%]			
	0 to 2	3 to 10	11 to 99	100
Stop	Quick Start Stand by	Quick Start Stand by	Start-up	PWM Input Error
Drive	Quick Start Stand by	Drive*(Note 1)*	Drive	PWM Input Error

(Note 1) Detect Motor Lock Protection, Quick Start Stand by at the re-start timing.

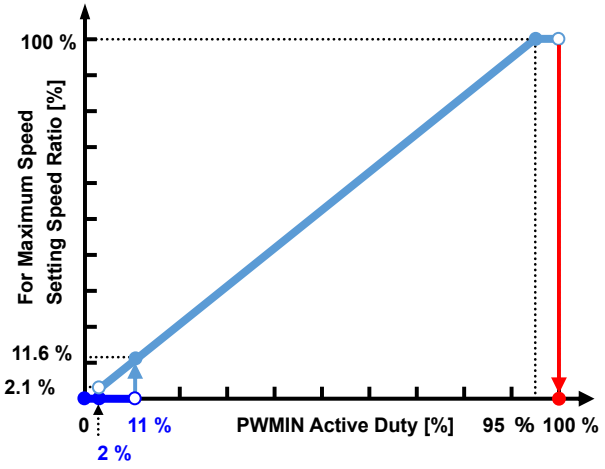


Figure 62. PWMIN Control Profile

6. Speed Control − continued

(2) Speed Control DC Voltage Input (DCIN)

It can be controlled by the DC voltage input to DCIN according to Figure 54. DCIN Control Profile.
The active mode of DCIN input can be selected by the speed control system setting pin (CNTSEL).

Table 16. DCIN Input Voltage

	DCIN Input Voltage [V]		
	0 to V_{REG} x 0.02	V_{REG} x 0.03 to V_{REG} x 0.10	V_{REG} x 0.11 to
Stop	Quick Start Stand by	Quick Start Stand by	Start-up
Drive	Quick Start Stand by	Drive*(Note 1)*	Drive

(Note 1) Detect Motor Lock Protection, Quick Start Stand by at the re-start timing.

Description of Operation - continued

7. Current Limit

By detecting the voltage at both ends of an external shunt resistor and calculating the amount of drive current, it is a function to prevent a larger current than expected from flowing through the external FET. When the voltage difference between the low side current detection voltage input (CS) and the low side current reference voltage input (CR) detects a set voltage of 100 mV (Typ) or more, at that time, the motor drive outputs that are energized are changed to High and High logic or Low and Low logic (short brake logic), and the motor drive current is shut off.

(1) Current Limit Detection and PWM Operation

After the current limit time t_{CLL}: 16 µs (Typ), if the CS voltage can't reach the V_{CLL}: 100 mV (Typ), releases the current limit and return the motor output. The current limit is PWM operation that repeats limitation (motor drive output brake) and detection (motor drive output ON).

In addition, as shown in Figure 63, in the current limit state even after the current limit time t_{CLL}, the motor drive output is turned on during the detection time t_{CLLDET}: 3.2 µs (Typ).

Until the current limit is released, the current detection and the current limit are repeated.

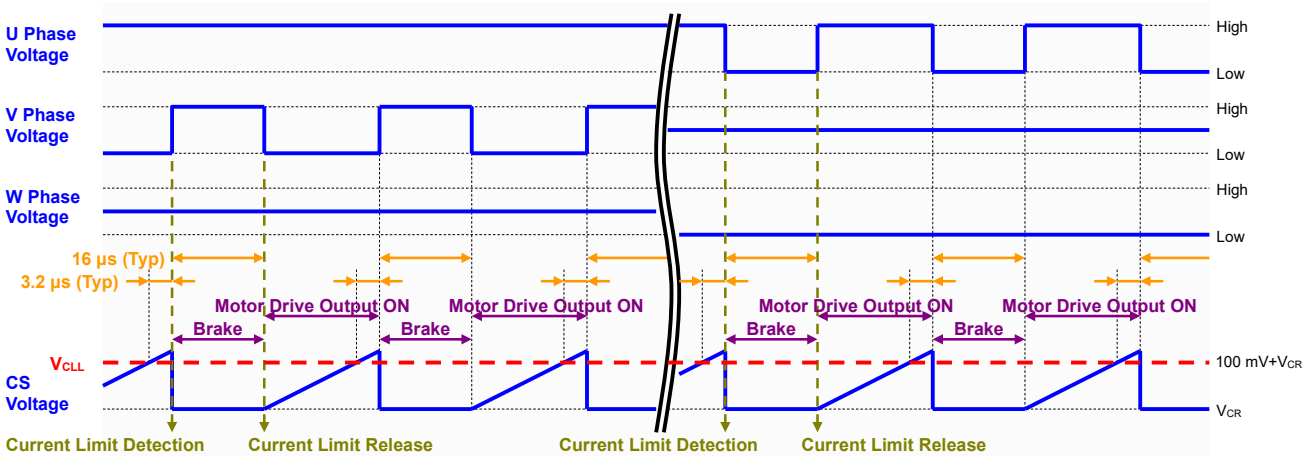


Figure 63. Current Limit PWM Operation Timing Chart 1

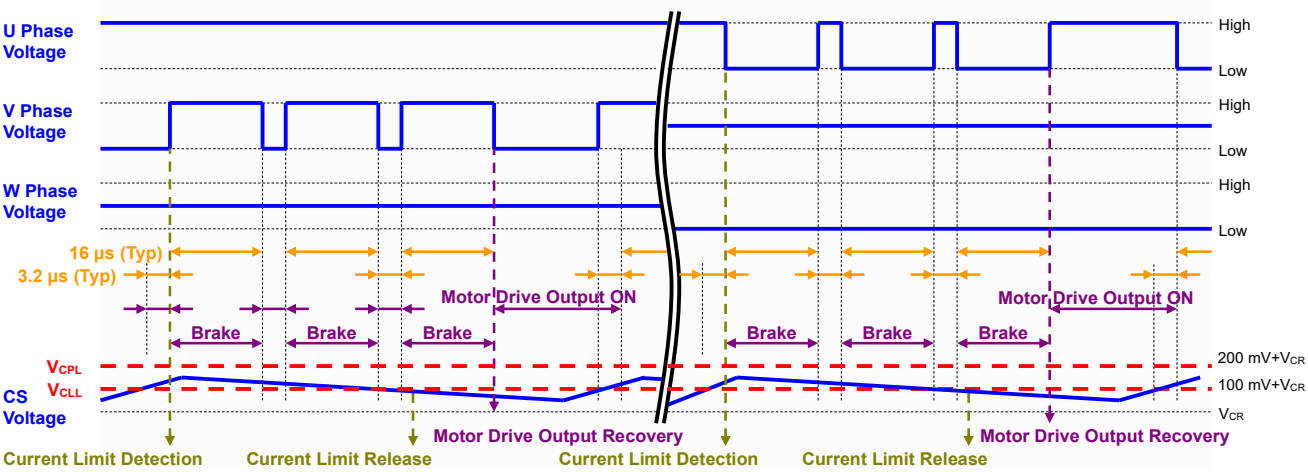


Figure 64. Current Limit PWM Operation Timing Chart 2

7. Current Limit − continued

(2) Current Limit Setting

The current limit value can be set by the motor drive current detection resistor R_1 and the current limit detection voltage inside the IC.

$$I_{CLL} = V_{CLL}/R_1 \quad [A]$$

where:
I_{CLL} is the Current Limit Setting Current [A]
V_{CLL} is the Current Limit Detect Voltage [V] (Typ 100 mV)
R_1 is the Motor Drive Current Detection Resistor [Ω]

(ex.) When the motor drive detection resistor is 10 mΩ, the current limit setting current is 10 A.

$$I_{CLL} = \frac{100\times10^{-3}}{10\times10^{-3}} = 10 \quad [A]$$

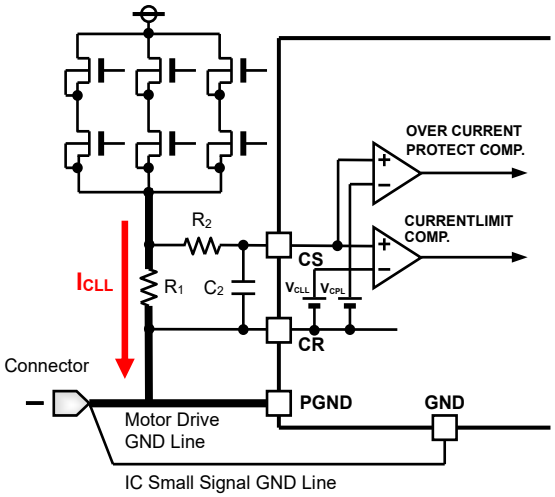


Figure 65. Current Limit Setting and GND Line

(3) Current Limit False Detection Measure

In Figure 65, R_2 and C_2 are CS voltage low pass filter.
Design the PCB layout with consideration for the wiring that is less affected by noise so that false detection of current limit does not occur.

Description of Operation - continued

8. Nch-Nch MOS FET Drive Pre-Driver

(1) Charge Pump

To support low voltage operation during cold cranking, a two-stage booster circuit is built in to drive the high side FET. By connecting a capacitor of VCPH - VCC = 1 µF and CPH2 - CPH1 = 0.1 µF, a boosted voltage of V_{CC} + 9.5 V (Typ) is generated on the VCPH pin.
Similarly, it has a booster circuit is built in to drive the low side FET. By connecting a capacitor of VCPL - GND = 1 µF and CPL2 - CPL1 = 0.1 µF, a boosted voltage of 9.5 V (Typ) is generated on the VCPL pin.
Place each capacitor as close to the pin as possible to minimize wiring impedance.
In addition to the boost voltage error, the boost operation is stopped during VCC over voltage, output GND short, output VCC short and over temperature.

(2) Constant Current Output

It is a constant current output drive system that can adjust the output slew rate with 16 modes of current value. Optimum settings for MOS FET characteristics can be simplified with 3 parameters of gate drive output source current setting input (SRR), gate drive output sink current setting input (SRF) and output dead time setting input (DT).

(3) Synchronous Rectification Drive

When in PWM operation, to increase the current efficiency, the method of motor output is synchronous rectification. The output dead time setting (DT) is used to generate the gate control timing for the high and low side outputs.

9. Signal Output

(1) Open Drain Output (SOUT)

The SOUT pin signal setting can be selected by the SOUT signal output setting input pin (SIGSEL).
The SOUT pin is open drain output, so this pin must be pulled up to external voltage by 1 kΩ to 100 kΩ resistors.
Note that the SOUT pin voltage and current should not exceed the maximum absolute ratings.

(2) Calculate Motor Rotation Speed

The relationship between 1FG frequency and motor speed is shown in the following formula.

$$N = (2 \times f)/P \times 60 \ \ [\text{min}^{-1}]$$

where:
N is the Motor Rotation Speed [min^{-1}]
f is the 1FG Output Frequency [Hz]
P is the Motor Pole Number [pole]

(ex.) For 8 pole motor drive, and FG frequency is 500 Hz, the motor rotation speed at minute is 7500 min^{-1}.

$$N = (2 \times 500)/8 \times 60 = 7500 \quad [\text{min}^{-1}]$$

(3) DIAG Duty

When the protection function is activated, the DIAG function*(Note 1)* that changes the duty of the SOUT signal operates. This signal is output from the SOUT pin when DIAG duty mode is selected with the SOUT signal output setting pin (SIGSEL).
The frequency of the SOUT signal is 5 Hz while the DIAG function is operating. The duty of the SOUT signal is different depending on each protection mode. When two or more protection functions operate at the same time, the duty of protection with higher priority is output.
(Note 1) The duty of the DIAG function is output with high active logic.

Table 17. DIAG Duty

Priority	Protection Function	DIAG Duty [%]
1	VCC Over Voltage	10
2	Output GND Short	20
3	Output VCC Short	30
4	Over Temperature	40
5	Boost Voltage Error	60
6	PWM Input Error	70
7	Motor Lock	80
8	Motor Reverse Idling	90

Description of Operation - continued

10. Analog Front End

(1) Open Drain Output Comparator

It has two comparator input pins (CMPINP, CMPINN) and an open drain output pin (CMPOUT).
The CMPOUT pin is open drain output, so this pin must be pulled up to external voltage by 10 kΩ to 100 kΩ resistor. When pulling up with an external voltage, note that the CMPOUT pin voltage and current do not exceed the absolute maximum ratings.

(2) Divider

The signal divided by 1024 from CMPOUT is output from FOUT.

(3) Open Drain Output (FOUT)

The FOUT pin is open drain output, so this pin must be pulled up to external voltage by 1 kΩ to 100 kΩ resistors.
Note that the FOUT pin voltage and current should not exceed the maximum absolute ratings.

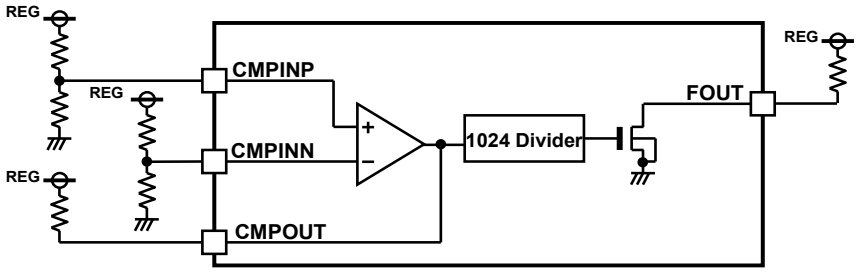


Figure 66. Analog Front End

Description of Operation - continued

11. Output Protection

(1) Protection Mode

It can select the self-restart or the OFF latch by the protection system setting input (PRTSEL).

(2) Self-Restart

It is a mode that restarts by the release condition of each protection without the release flag.
The boost operation is stopped during VCC over voltage, output GND short, output VCC short and over temperature. Therefore, after VCC over voltage, output GND short, output VCC short and the over temperature are released, the restart is performed after 600 ms of the under-voltage release condition of the boost voltage error.

Table 18. Self-Restart

Priority	Stop Mode		Protection Condition		Boost	Pre-driver Output (U, V, W Output)	
			Detection	Release		Mode	Logic
1	VCC Over Voltage	OVP = 30 V Setting	V_{CC} = 30 V (Typ) or more	V_{CC} = 28 V (Typ) or less	Stop	Open	Low (Hi-Z)
		OVP = 20 V Setting	V_{CC} = 20 V (Typ) or more	V_{CC} = 19 V (Typ) or less			
2	Output GND Short		Diff Voltage (V_{VR} - V_U, V_{VR} - V_V, V_{VR} - V_W) is V_{OCP} or more	600 ms (Typ) after detection	Stop	Open	Low (Hi-Z)
3	Output VCC Short	Drain-source Voltage	Diff Voltage (V_U - V_{CR}, V_V - V_{CR}, V_W - V_{CR}) is V_{OCP} or more	600 ms (Typ) after detection	Stop	Open	Low (Hi-Z)
		Shunt Resistor Detected	RNF Line Over Current (V_{CPL} 200 mV (Typ) ÷ Motor Drive Current Detection Resistor)				
4	Over Temper-ature	TSD	Tj = 175 °C (Typ) or more	Tj = 150 °C (Typ) or less	Stop	Open	Low (Hi-Z)
		EXTSD	V_{EXTSD} = 2.5 V (Typ) or less	V_{EXTSD} = 2.9 V (Typ) or more			
5	Boost Voltage Error	Over Voltage	V_{CPH} - V_{CC} or V_{CPL} = 13 V (Typ) or more	V_{CPH} - V_{CC} or V_{CPL} = 12 V (Typ) or less	Stop	Open	Low (Hi-Z)
		Under Voltage	V_{CPH} - V_{CC} or V_{CPL} = 3.5 V (Typ) or less	600 ms (Typ) after detection			
6	PWM Input Error	Frequency Error	1050 Hz (Typ) or more during 150 ms (Typ)	Normal Frequency (6.8 Hz to 1000 Hz) and Same duty (±0.8 %) 3 times Continuous Input	Active	Open	Low (Hi-Z)
		Duty Error	100 % duty during 150 ms (Typ)				
7	Motor Lock	High Speed Rotation	1FG = 3.3 kHz (Typ)	1 s (Typ) or 10 s (Typ) after detection	Active	Open	Low (Hi-Z)
		Low Speed Rotation	1FG = 5 Hz (Typ)				
8	Motor Reverse Idling		Reverse logic is detected 6 times in a row when Motor Initial State Judgement	1 s (Typ) after detection	Active	Brake	H/Low L/High (Low)

11. Output Protection − continued

(3) OFF Latch

It is a mode that restarts by the release flag that input OFF logic for 1 s or more to PWMIN input.

Table 19. OFF Latch

Priority	Stop Mode		Protection Condition		Boost	Pre-driver Output (U, V, W Output)	
			Detection	Release		Mode	Logic
1	VCC Over Voltage	OVP = 30 V Setting	V_{CC} = 30 V (Typ) or more	Input OFF Logic for 1 s or more to PWMIN Input	Stop	Open	Low (Hi-Z)
		OVP = 20 V Setting	V_{CC} = 20 V (Typ) or more				
2	Output GND Short		Diff Voltage (V_{VR} - V_U, V_{VR} - V_V, V_{VR} - V_W) is V_{OCP} or more		Stop	Open	Low (Hi-Z)
3	Output VCC Short	Drain-source Voltage	Diff Voltage (V_U - V_{CR}, V_V - V_{CR}, V_W - V_{CR}) is V_{OCP} or more		Stop	Open	Low (Hi-Z)
		Shunt Resistor Detected	RNF Line Over Current (V_{CPL} 200 mV (Typ) ÷ Motor Drive Current Detection Resistor)				
4	Over Temper-ature	TSD	Tj = 175 °C (Typ) or more		Stop	Open	Low (Hi-Z)
		EXTSD	V_{EXTSD} = 2.5 V (Typ) or less				
5	Boost Voltage Error	Over Voltage	V_{CPH} - V_{CC} or V_{CPL} = 13 V (Typ) or more		Stop	Open	Low (Hi-Z)
		Under Voltage	V_{CPH} - V_{CC} or V_{CPL} = 3.5 V (Typ) or less				
6	PWM Input Error	Frequency Error	1050 Hz (Typ) or more during 150 ms (Typ)	Normal Frequency (6.8 Hz to 1000 Hz) and Same duty (±0.8 %) 3 times Continuous Input	Active	Open	Low (Hi-Z)
		Duty Error	100 % duty during 150 ms (Typ)				
7	Motor Lock	High Speed Rotation	1FG = 3.3 kHz (Typ) or more	Normal Frequency (6.8 Hz to 1000 Hz) and Same duty (±0.8 %) 3 times Continuous Input	Active	Open	Low (Hi-Z)
		Low Speed Rotation	1FG = 5 Hz (Typ) or less				
8	Motor Reverse Idling		Reverse logic is detected 6 times in a row when Motor Initial State Judgement	1 s (Typ) after detection	Active	Brake	H/Low L/High (Low)

Description of Operation - continued

12. VCC Over Voltage Protection (OVP)

It is a protection function to prevent a large current from flowing to the drive FET in an over voltage condition.
When a voltage higher than the specified voltage is detected, all external FETs are turned off. At the same time, the boost operation is stopped.
The restart is performed 600 ms after releasing the VCC over voltage protection.
It can select from 2 modes according to 30 V detection / 28 V release and 20 V detection / 19 V release by the protection system setting input (PRTSEL).

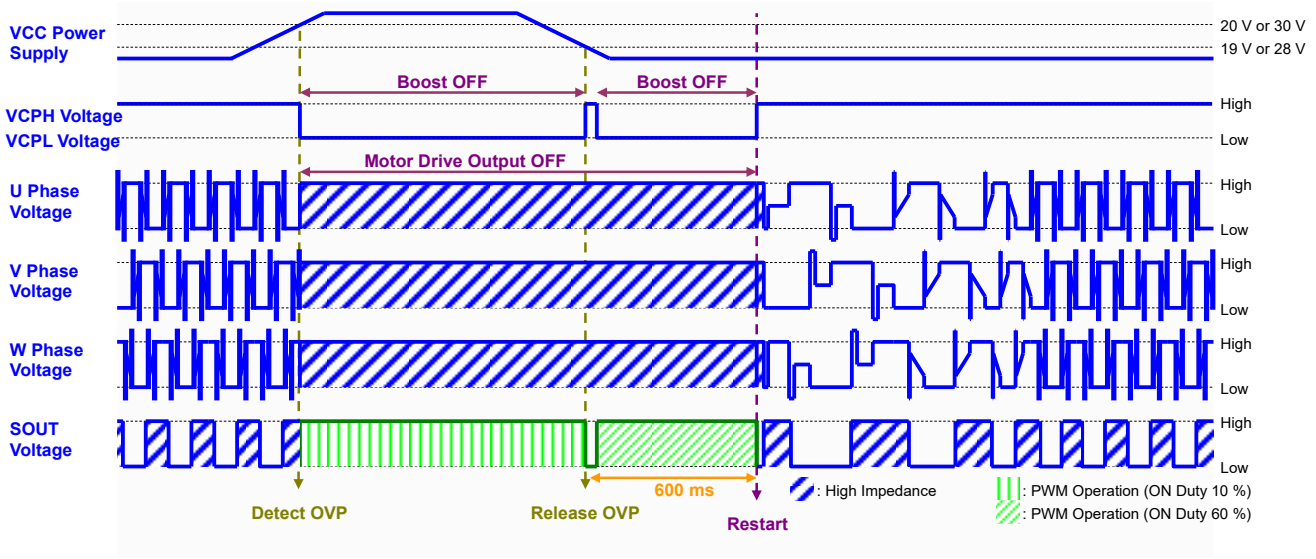


Figure 67. VCC Over Voltage Protection Timing Chart

13. Over Current Protection (OCP)

(1) External FET Drain-Source Voltage Detection

It is a protection function to prevent a large current from flowing to the drive FET by detecting the drain-source voltage of the external FET.
When a voltage higher than the setting voltage is detected, all external FETs are turned off. At the same time, the boost operation is stopped. The restart is performed 600 ms after releasing the over current protection timer.
It can select from 4 modes according to 200 mV, 400 mV, 1000 mV, 1500 mV by the protection system setting input (PRTSEL).

(a) High Side FET Drain-Source Voltage Detection

When the voltage difference between the motor power supply reference voltage input (VR) and the motor drive outputs (U, V, W) are detected to be more than the set voltage, all external FETs are turned off. This stop mode is a output GND short.

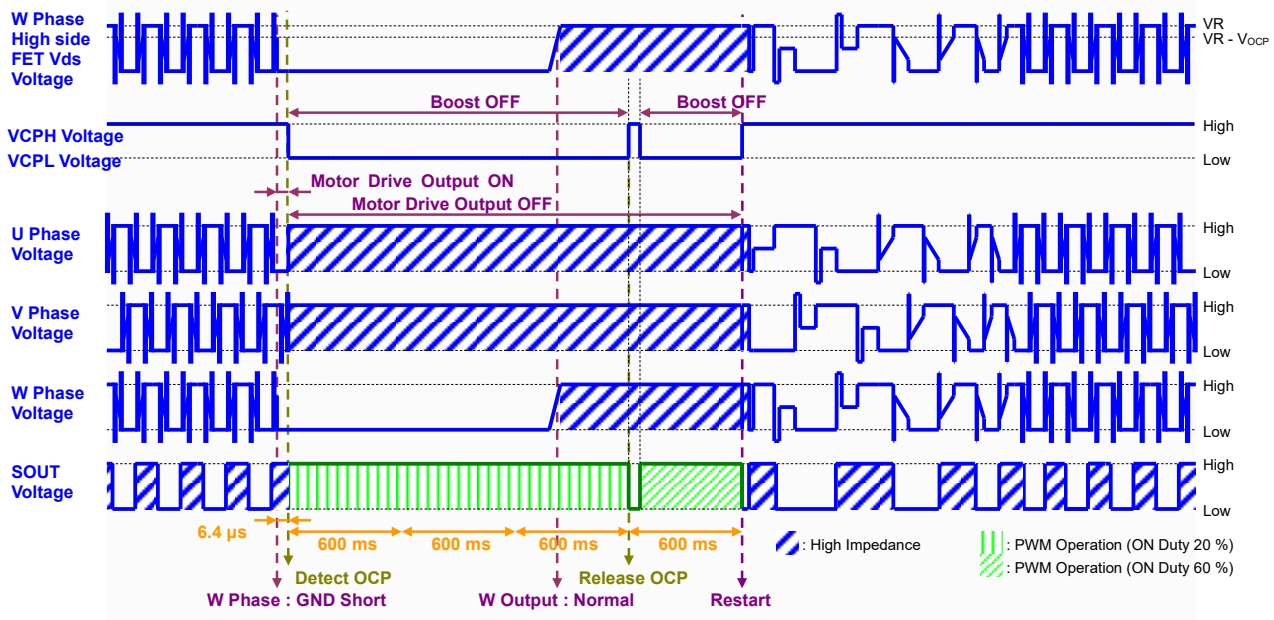


Figure 68. High Side FET Over Current Detection Timing Chart (W Phase Output is GND Short)

(1) External FET Drain-Source Voltage Detection - continued

(b) Low Side FET Drain-Source Voltage Detection

When the voltage difference between the motor drive outputs (U, V, W) and the low side current reference voltage input (CR) are detected to be more than the set voltage, all external FETs are turned off. This stop mode is a output VCC short.

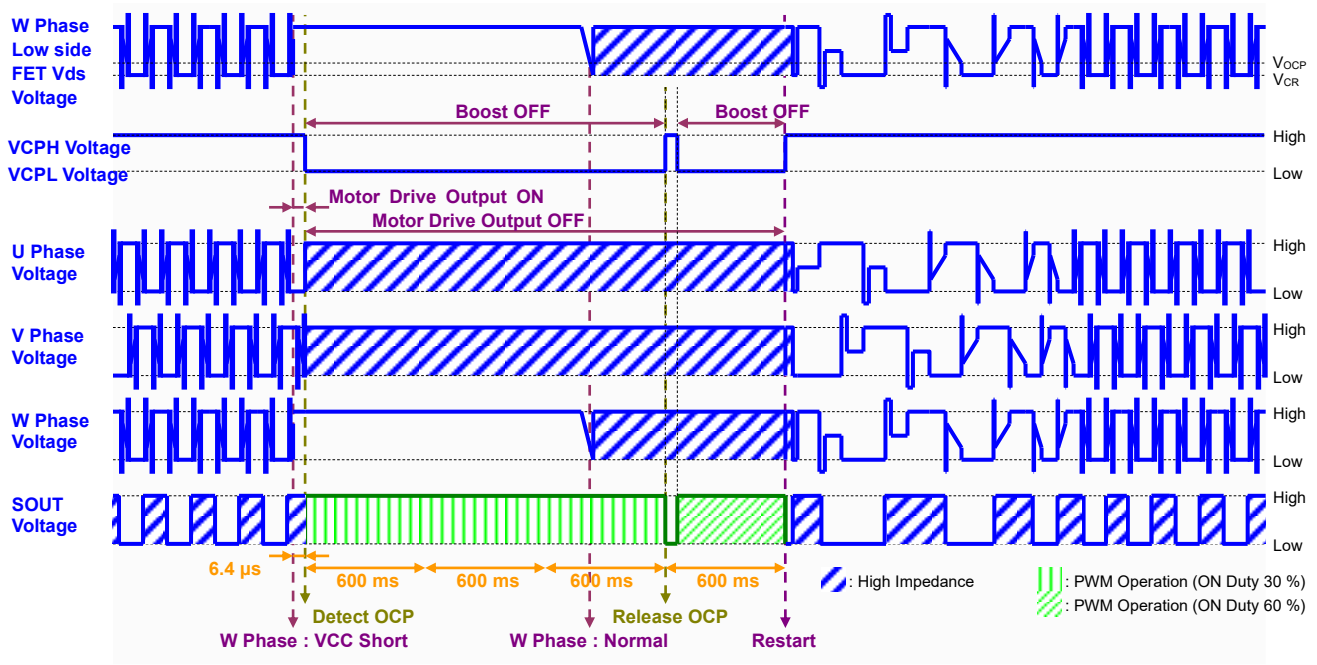


Figure 69. Low Side FET Over Current Detection Timing Chart (W Phase Output is VCC Short)

(2) External Shunt Resistor Detection

It is a protection function to prevent a large current from flowing to the drive FET by detecting the voltage across the external shunt resistor.

When the voltage difference between the low side current detection voltage input (CS) and the low side current reference voltage input (CR) detects a set voltage of 200 mV (Typ) or more, all external FETs are turned off. This stop mode is a output VCC short.

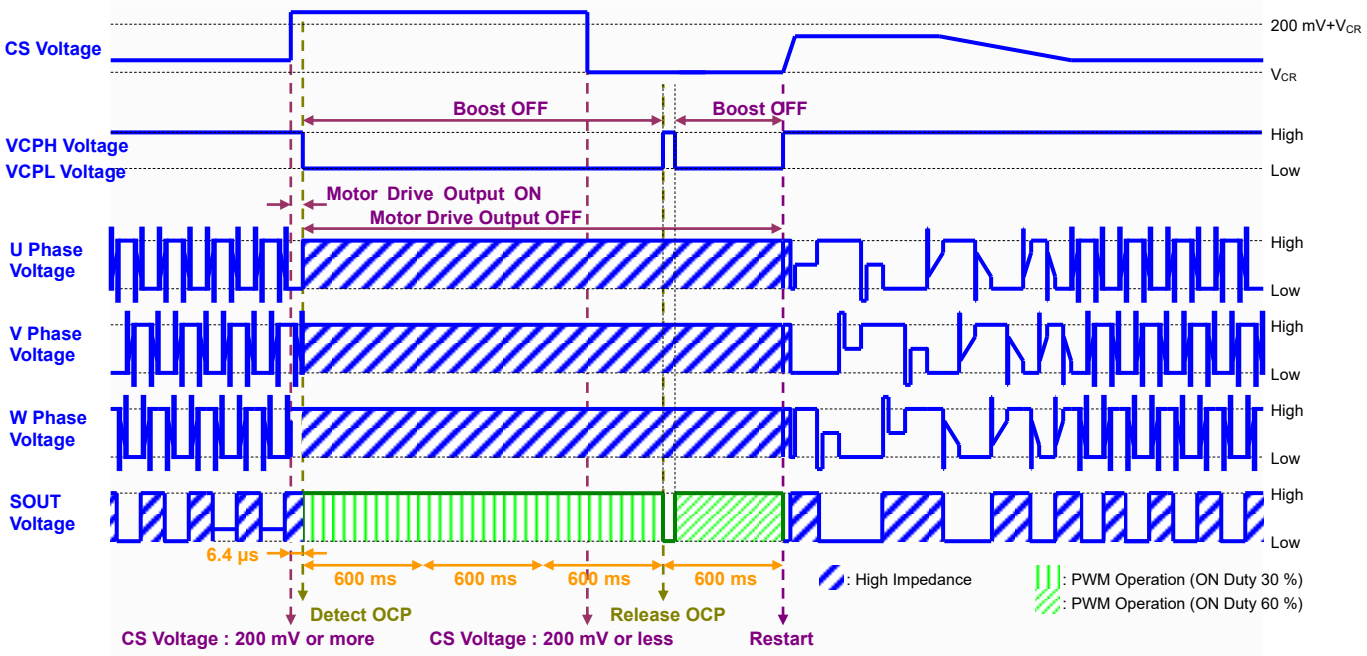


Figure 70. Over Current Protection by Detecting the External Shunt Resistor Timing Chart

Description of Operation - continued

14. Thermal Shutdown (TSD)

It is a protection function to prevent malfunction and thermal damage due to thermal runaway.
When a temperature higher than the specified junction temperature is detected, all the external FETs are turned off.

(1) Internal Over Temperature Detection

When the junction temperature is exceeded 175 °C (Typ), all external FETs are turned off.
There is a hysteresis width T_{TSDHYS}: 25 °C (Typ) between the detection temperature and the release temperature, and this protection is released when the junction temperature is below 150 °C (Typ).

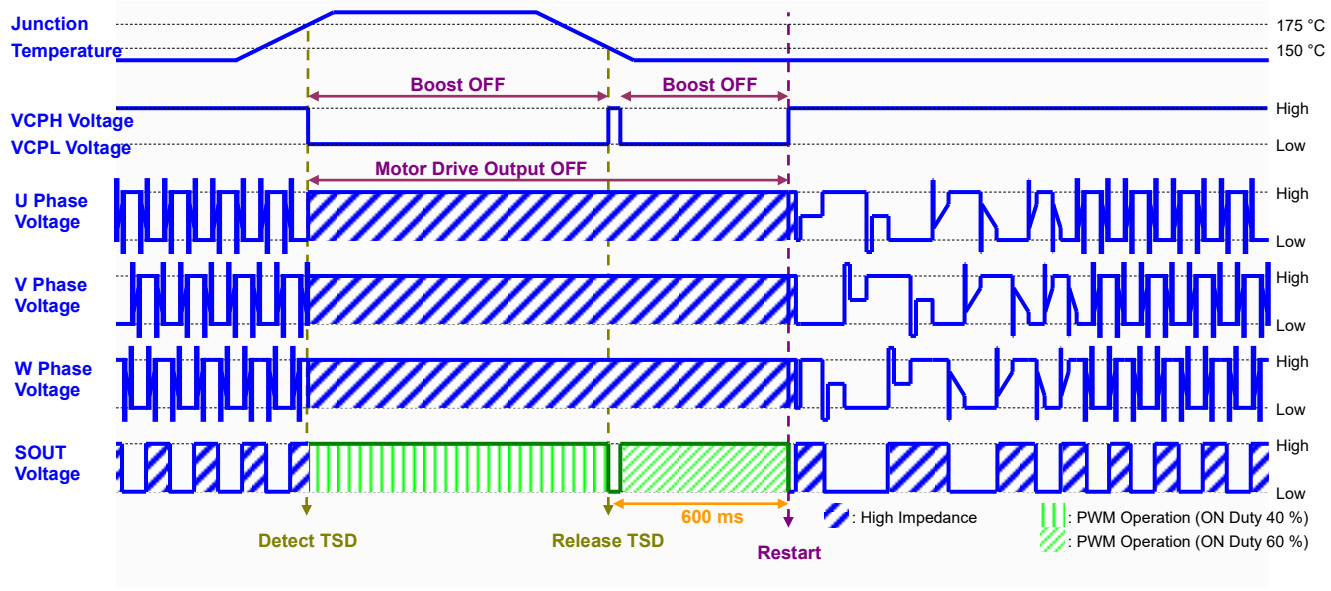


Figure 71. Thermal Shutdown by Internal Over Temperature Detection Timing Chart

(2) External Over Temperature Detection

In application utilizing the temperature characteristic of the external thermistor resistance, when the voltage applied to the external temperature detection voltage input (EXTSD) is below 2.5 V (Typ), all external FETs are turned off.
There is a hysteresis width V_{EXHYS}: 400 mV (Typ) between the detection voltage and the release voltage, and this protection is released when the voltage is exceeded 2.9 V (Typ).

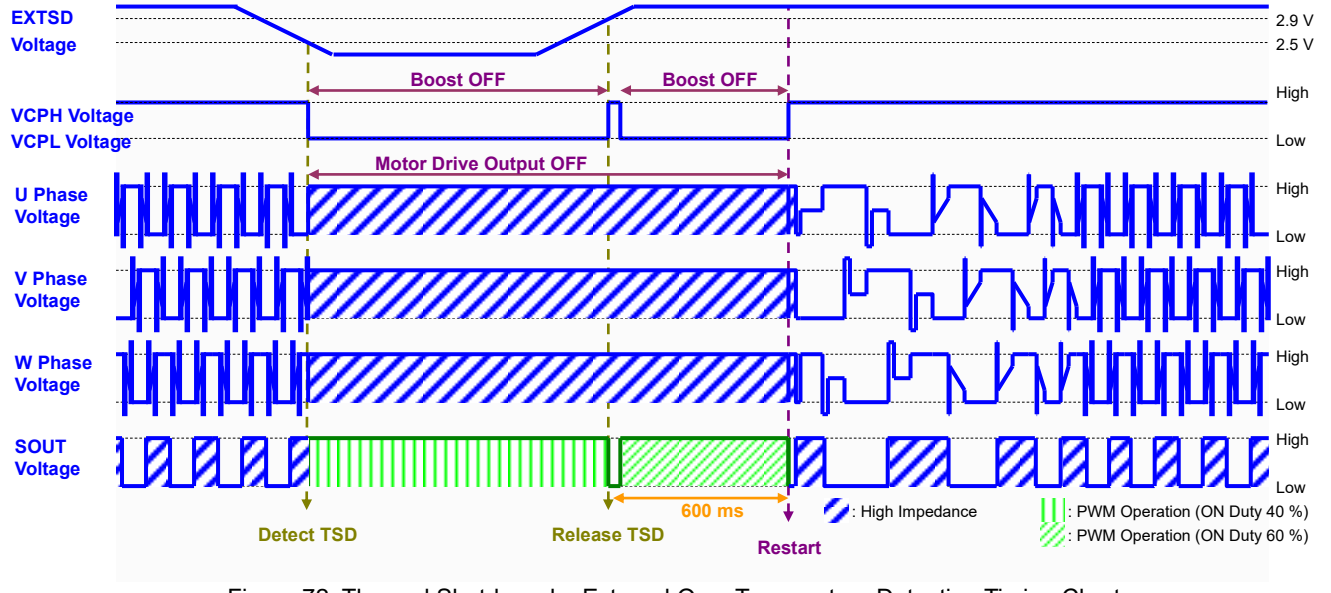


Figure 72. Thermal Shutdown by External Over Temperature Detection Timing Chart

Description of Operation - continued

15. Boost Voltage Error Protection

It is a protection function to prevent the drive FET breakdown due to abnormal voltage of the boost output (VCPH, VCPL). When over voltage or under voltage is detected, the boost operation is stopped and all external FETs are turned off. In addition, the boost operation is stopped during VCC over voltage, output GND short, output VCC short and over temperature, too.

(1) Over Voltage Detection

In the case of over voltage, the gate-source breakdown of the drive FET is assumed, so the voltage difference between the high side gate control boost voltage output (VCPH) and the power supply voltage (VCC) is exceeded 13 V (Typ), or the low side gate control boost voltage output (VCPL) is exceeded 13 V (Typ), all external FETs are turned off.
There is a hysteresis width $V_{OVPHYSx}$: 1.0 V (Typ) between the detection voltage and the release voltage, and this protection is released when the voltage is below 12 V (Typ).

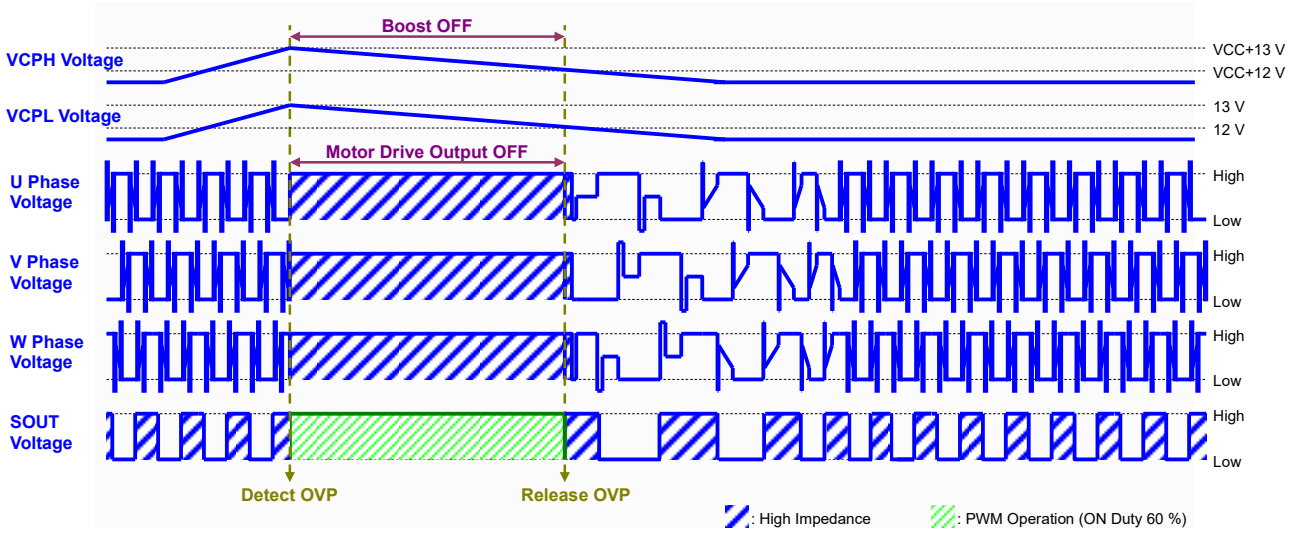


Figure 73. Boost Voltage Error Protection by Over Voltage Detection Timing Chart

(2) Under Voltage Detection

In the case of under voltage, the gate-source voltage is insufficient and on-resistance increases, thermal breakdown of the drive FET is assumed, so the voltage difference between the high side gate control boost voltage output (VCPH) and the power supply voltage (VCC) is below 3.5 V (Typ), or the low side gate control boost voltage output (VCPL) is below 3.5 V (Typ), all external FETs are turned off.
There is a hysteresis width $V_{UVPHYSx}$: 1.0 V (Typ) between the detection voltage and the release voltage, and this protection is released when the voltage is exceeded 4.5 V (Typ).

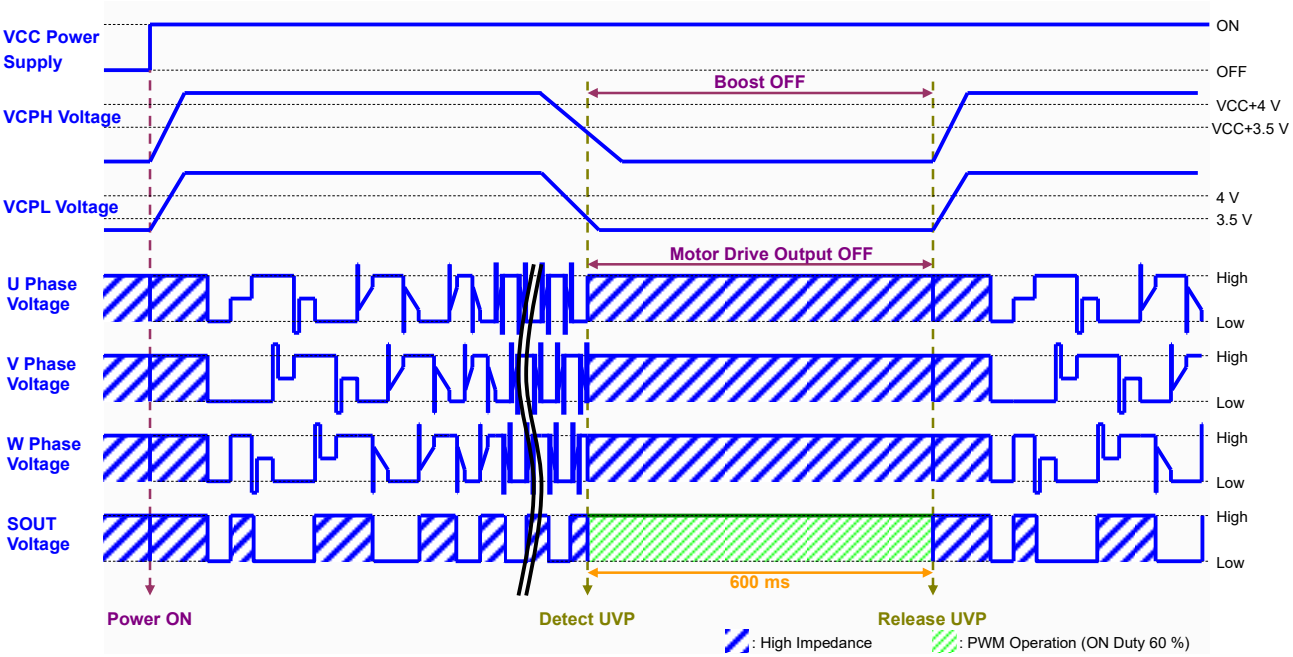


Figure 74. Boost Voltage Error Protection by Under Voltage Detection Timing Chart

Description of Operation - continued

16. PWMIN Input Error Protection

It is a protection function to detect the runaway and disconnect error signal of speed control PWM duty (PWMIN). When the error of PWM frequency and PWM duty is detected, it is switched the operation mode of the safety goal set by the speed control system setting input (CNTSEL).
In continuous operation mode; the speed control DC voltage input (DCIN) operation.
In operation stop mode; all external FETs are turned off.

(1) PWM Frequency Error

When the outside normal frequency range (6.8 Hz to 1000 Hz) input is continuously detected for 150 ms (Typ), it is judged that the PWM input error and it is switched the operation mode of the safety goal.

(2) PWM Duty Error

As shown in Figure 62. PWMIN Control Profile, when PWM = 100 % fixed is continuously detected for 150 ms (Typ), it is judged that the PWM input error and it is switched the operation mode of the safety goal.
When PWM = 0 % fixed is continuously detected for 150 ms (Typ), it is judged that the PWM stand by and it is not switched the operation mode of the safety goal.

17. Motor Lock Protection (MLP)

It is a protection function to detect the abnormal motor rotation due to external factors such as contamination and motor output disconnection. High speed rotation detection and low speed rotation detection are provided to prevent unintended motor operation such as step-out due to false detection of induced voltage.

(1) High Speed Rotation Detection

When the SOUT frequency is exceeded 3.3 kHz (Typ) (1FG frequency), all external FETs are turned off.

Table 20. Motor Rotation Upper Limit

IC	Motor				
SOUT Frequency [Hz]	4 pole [min^{-1}]	6 pole [min^{-1}]	8 pole [min^{-1}]	10 pole [min^{-1}]	12 pole [min^{-1}]
3300	99000	66000	49500	39600	33000

(2) Low Speed Rotation Detection

When the SOUT frequency is below 5 Hz (Typ) (1FG frequency), all external FETs are turned off.

Table 21. Motor Rotation Lower Limit

IC	Motor				
SOUT Frequency [Hz]	4 pole [min^{-1}]	6 pole [min^{-1}]	8 pole [min^{-1}]	10 pole [min^{-1}]	12 pole [min^{-1}]
5	150	100	75	60	50

17. Motor Lock Protection (MLP) − continued

(3) Start Asist and Motor Lock Protection

In PRTSEL setting, there are pump mode and fan motor mode, and the operation sequence is different.

(a) Pump Mode

If the induced voltage is not detected normally even after eight times of motor drive output logic switching by forced commutation drive, brake and forced commutation drive are repeated within the lock detection time t_{ON}: 1 s by start assist.

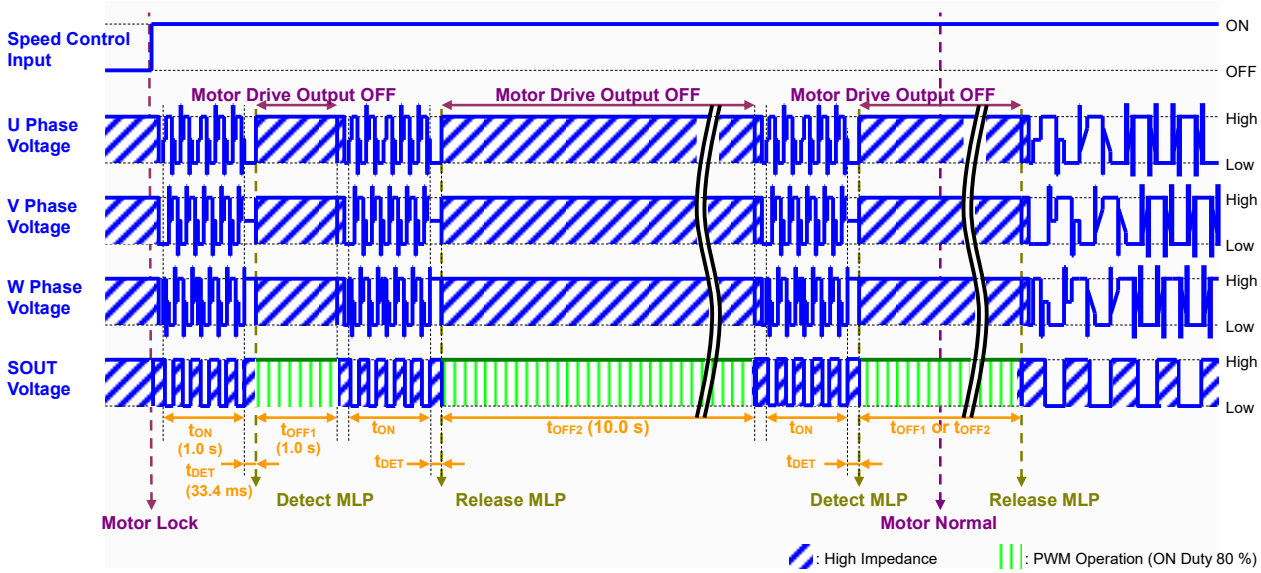


Figure 75. Motor Lock Protection Timing Chart in Pump Mode

(b) Fan Motor Mode

If the induced voltage is not detected normally even after eight times of motor drive output logic switching by forced commutation drive, braking and forced commutation drive are repeated only once by start assist.

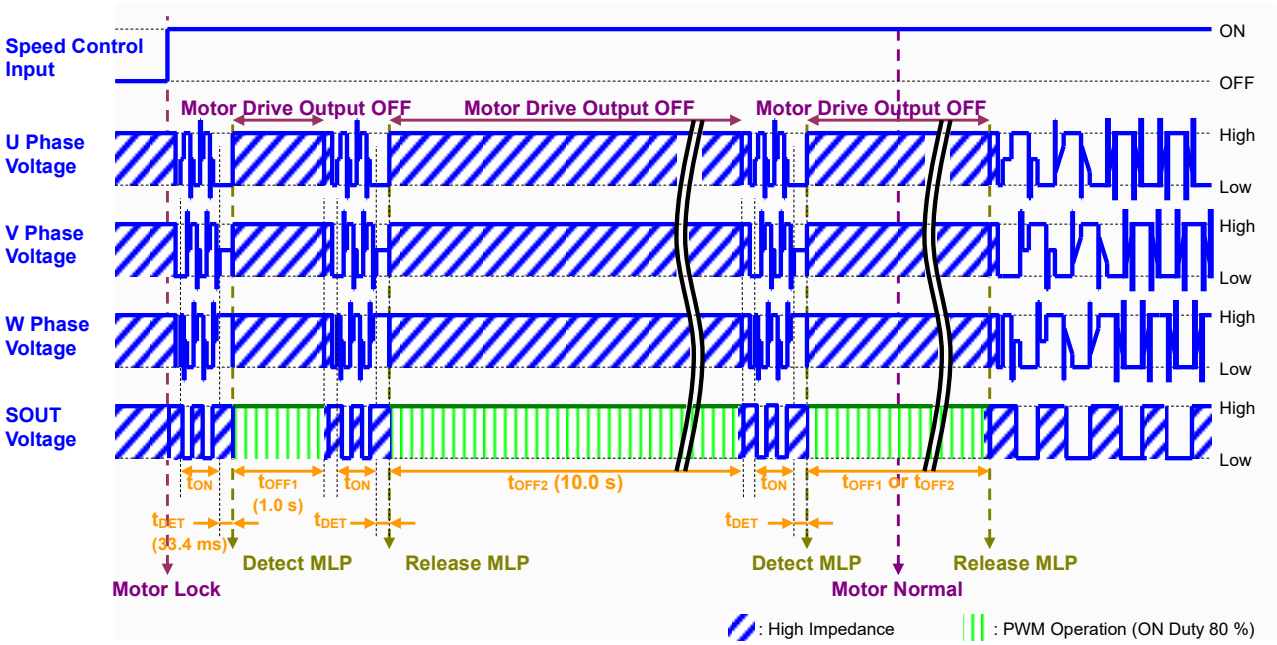


Figure 76. Motor Lock Protection Timing Chart in Fan Motor Mode

Description of Operation - continued

18. Motor Reverse Idling Protection

It is a protection function to detect the reverse idling of backflow pressure (wind pressure, water pressure, hydraulic pressure, fuel pressure) that hinders the stability of motor start-up.
Reverse idling detection is provided to prevent unintended motor operation such as step-out due to false detection of induced voltage. When the reverse logic is detected continuously 6 times during the initial state judgment, only the lower side of the external FET turns on for U, V and W phase outputs.

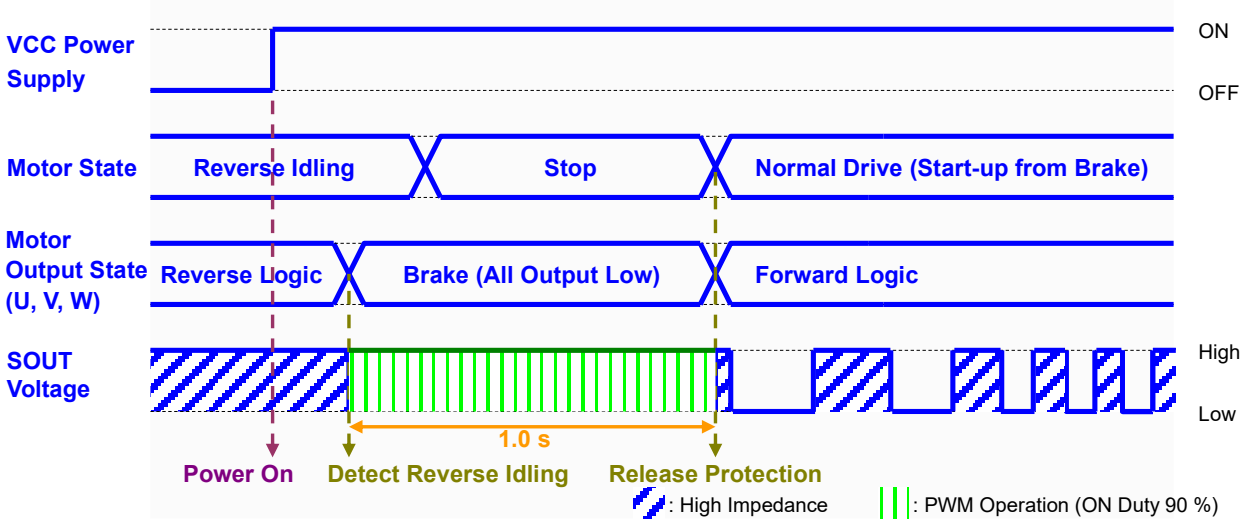


Figure 77. Motor Reverse Idling Protection Timing Chart

19. Under Voltage Lock Out (UVLO)

It is a function to prevent malfunction outside the lower limit of the IC operation range due to disturbance or abnormal cranking. When the reference voltage output (REG) is below 4.0 V (Typ), reset the logic circuit and stop the IC. At the same time, all external FETs are turned off. There is a hysteresis width $V_{UVLOHYS}$: 0.5 V (Typ) between the detection voltage and the release voltage, and this protection is released when the reference voltage output (REG) is exceeded 4.5 V (Typ).

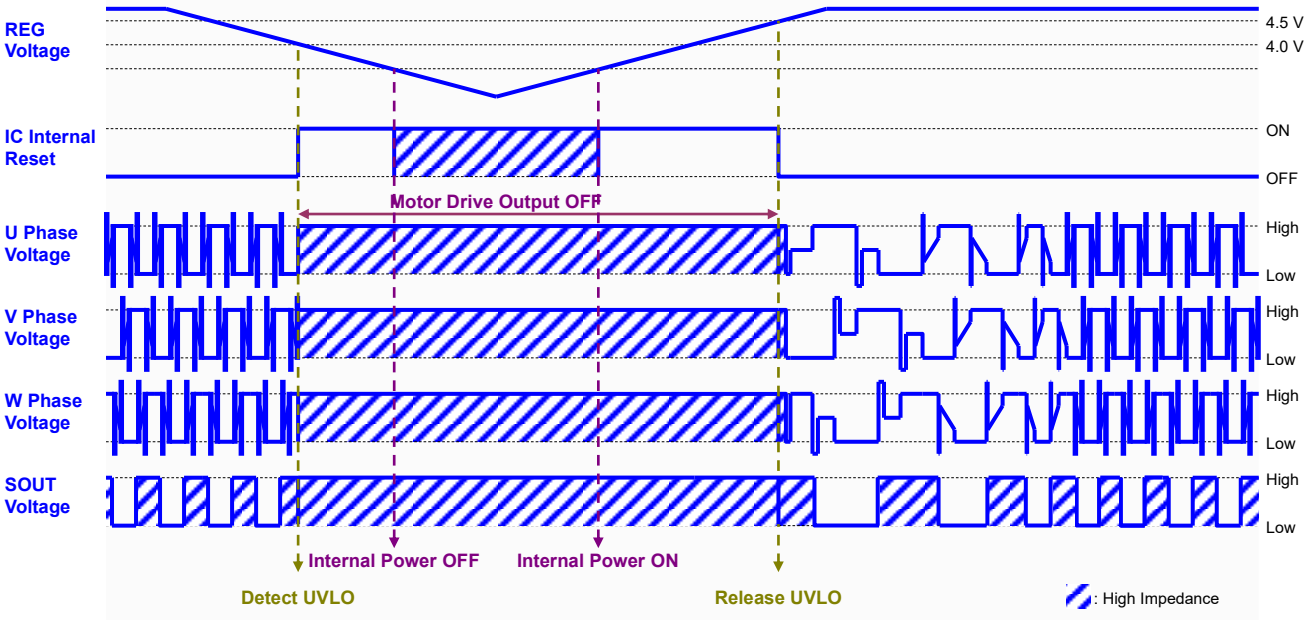
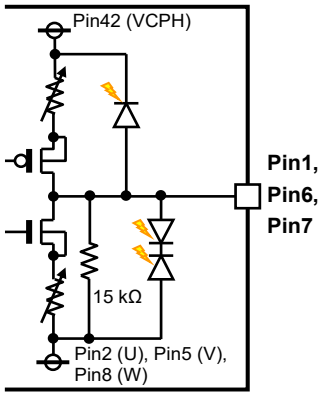


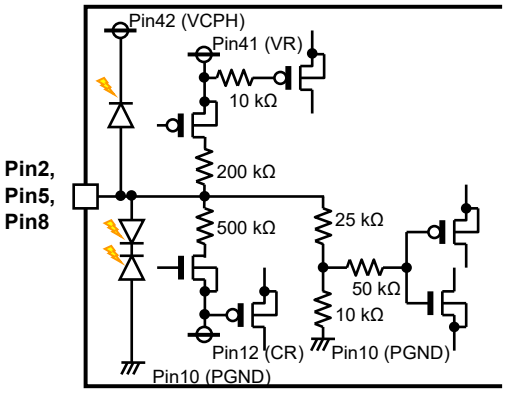
Figure 78. Under Voltage Lock Out Timing Chart

I/O Equivalence Circuit (Typical values for resistance)

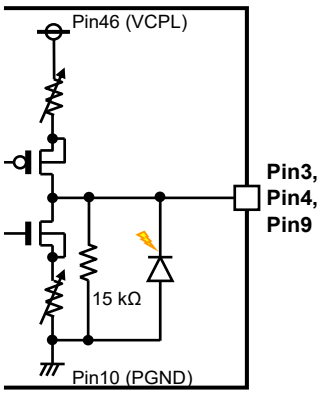
1.UH, 6.VH, 7.WH



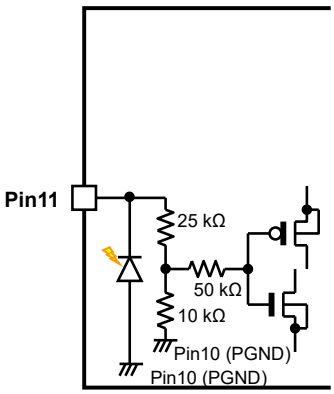
2.U, 5.V, 8.W



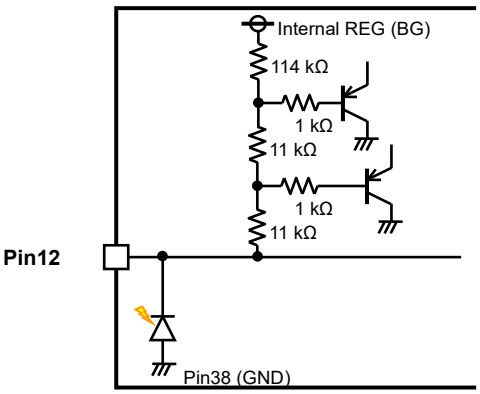
3.UL, 4.VL, 9.WL



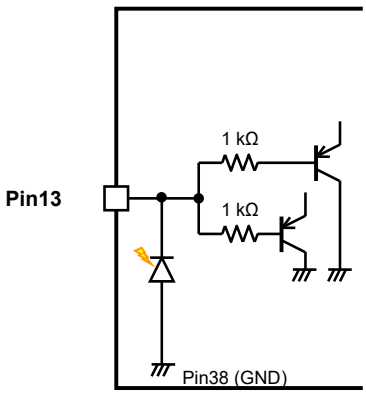
11.COM



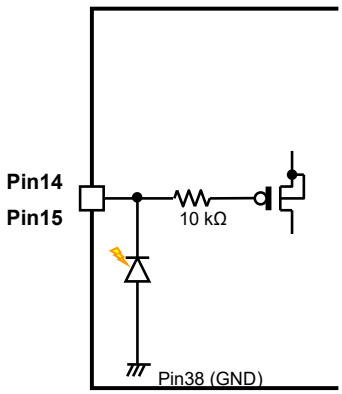
12.CR



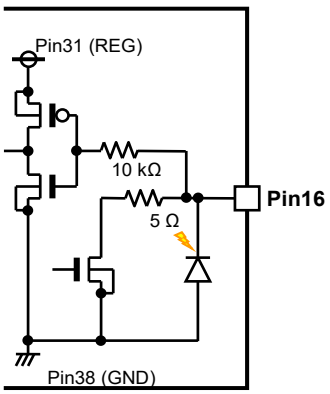
13.CS



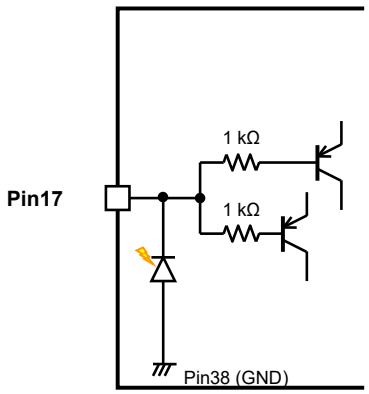
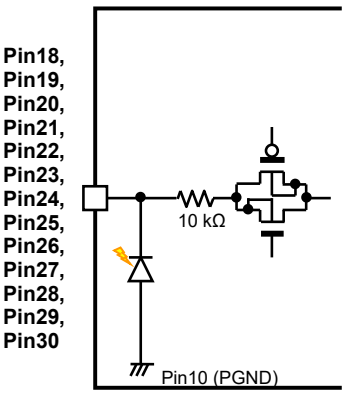
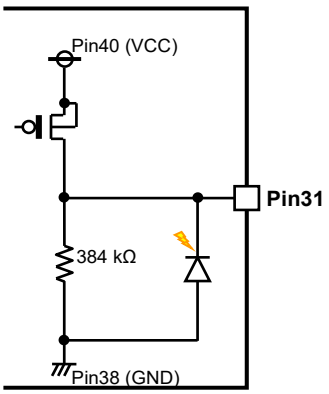
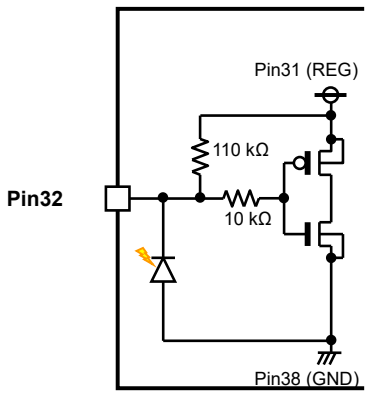
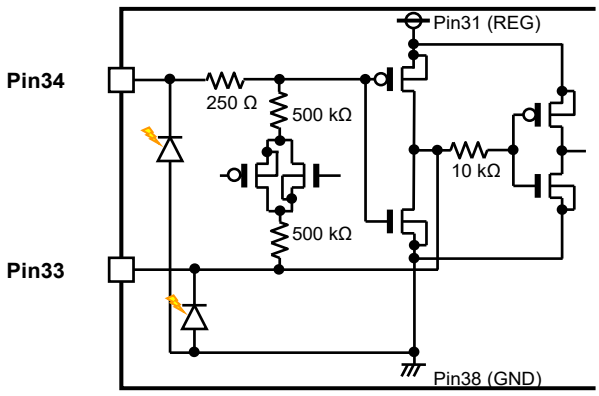
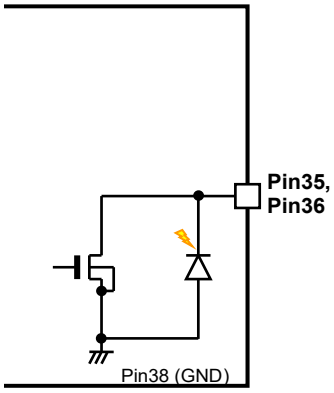
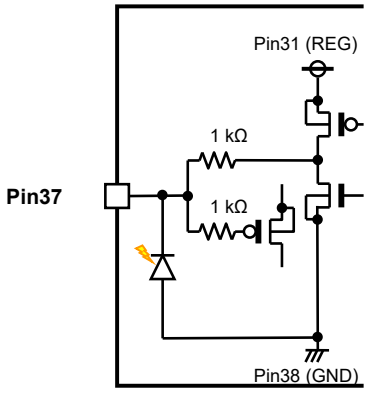
14.CMPINP, 15.CMPINN



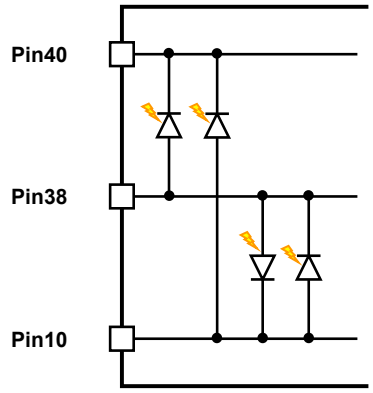
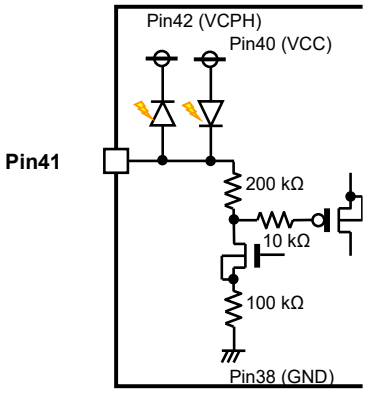
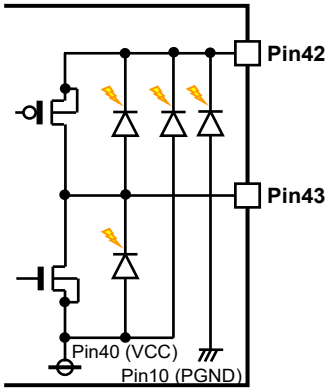
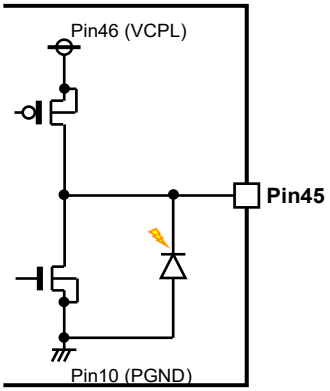
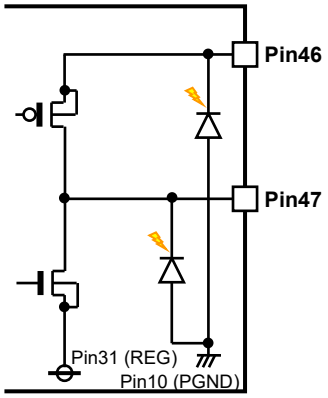
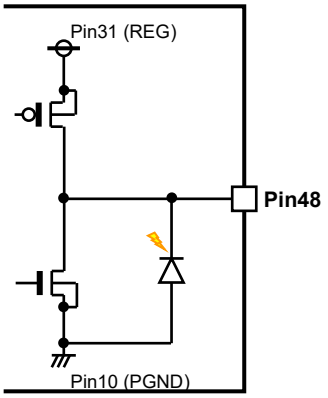
16.CMPOUT



I/O Equivalence Circuit - continued

17.EXTSD	18.SIGSEL, 19.CNTSEL, 20.DT, 21.SRF, 22.SRR, 23.LA, 24.PRTSEL, 25.STS, 26.DRS, 27.RREF, 28.INTG, 29.PROP, 30.DCIN	31.REG
		
32.PWMIN	33.XOUT, 34.XIN	
		
35.FOUT, 36.SOUT	37.TOSC	
		

I/O Equivalence Circuit - continued

10.PGND, 38.GND, 40.VCC	41.VR
	
42.VCPH, 43.CPH2	**45.CPH1**
	
46.VCPL, 47.CPL2	**48.CPL1**
	

Heat Loss

1. Thermal Resistance

Heat generated by consumed power of IC is radiated from the mold resin or lead frame of package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance. In the state of the substrate mounting, thermal resistance from the chip junction to the ambient is shown in θ_{ja} °C/W, and thermal characterization parameter from junction to the top centre of the outside surface of the component package is shown in Ψ_{jt} °C/W. Thermal resistance is classified into the package part and the substrate part, and thermal resistance in the package part depends on the composition materials such as the mold resins and the lead frames. On the other hand, thermal resistance in the substrate part depends on the substrate heat dissipation capability of the material, the size, and the copper foil area etc. Therefore, thermal resistance can be decreased by the heat radiation measures like installing a heat sink etc. in the mounting substrate. The thermal resistance model is shown in Figure 79 and thermal resistance formula is shown below.

$$\theta ja = (T_j - T_a)/P \quad [°C/W]$$
$$\psi jt = (T_j - T_t)/P \quad [°C/W]$$

where:
θja is the thermal resistance from junction to ambient [°C/W]
ψjt is the thermal characterization parameter from junction to the top centre of the outside surface of the component package [°C/W]
Tj is the junction temperature [°C]
Ta is the ambient temperature [°C]
Tt is the package outside surface (top centre) temperature [°C]
P is the power consumption [W]

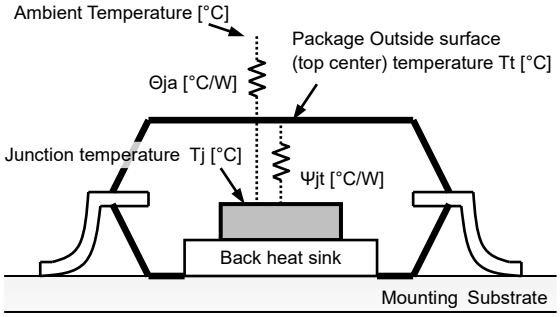


Figure 79. Thermal Resistance Model of package

Even if it uses the same package, θja and ψjt are changed depending on the chip size, power consumption, and the measurement environments of the ambient temperature, the mounting condition, and the wind velocity, etc.

2. Power Dissipation

Power dissipation (total loss) is the power that can be consumed by IC at Ta = 25 °C. The IC is heated when it consumes power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be allowed by IC chip into the package is the absolute maximum rating of the junction temperature, and depends on circuit configuration, manufacturing process, etc. The Power dissipation is determined by this maximum junction temperature, the thermal resistance in the state of the substrate mounting, and the ambient temperature. Therefore, when the power dissipation exceeds the absolute maximum rating, the operating temperature range is not a guarantee. The maximum junction temperature is in general equal to the maximum value in the storage temperature range.

3. Thermal Derating Curve

Thermal derating curve indicates power that can be consumed by the IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at the ambient temperature (25 °C) and becomes 0 W at the maximum junction temperature (150 °C). The inclination is reduced by the reciprocal of thermal resistance θja.

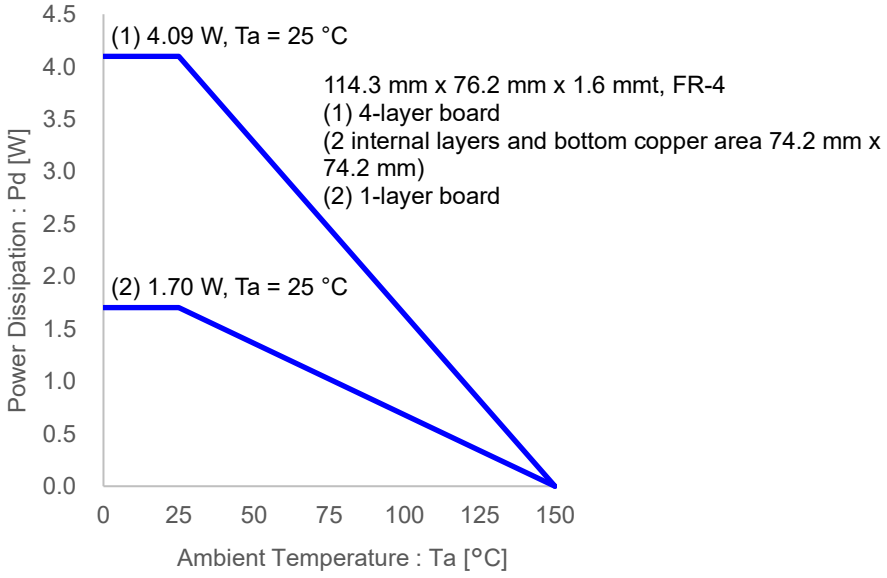


Figure 80. Derating Curve by Transient Thermal Resistance (Reference Value)

Heat Loss - continued

4. Thermal Design

The power consumption significantly changes depending on the supply voltage and motor drive output current etc.
Also, the power dissipation (Pd) will change depending on the mounting board status and surrounding etc. The thermal resistance data and excess thermal resistance data will be considered with actual operating conditions. In addition, implement thermal design with enough derating margin.

Safety Measure

1. Countermeasure Against Destruction by Reverse Connection of Power Supply

Reverse connection of the power supply causes current to flow through a path different from that in normal operation, which may result in IC destruction or deterioration. When reverse connection is possible, reverse connection protection diode must be added between power supply and VCC.

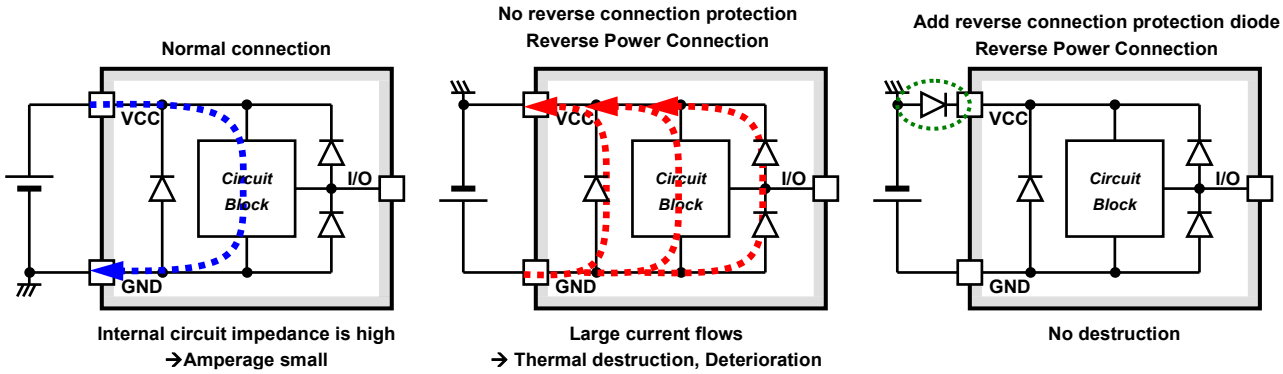


Figure 81. Flow of Current when Power Supply is Connected Reversely

The example of reverse connection protection circuit to supress power loss of application is shown below.

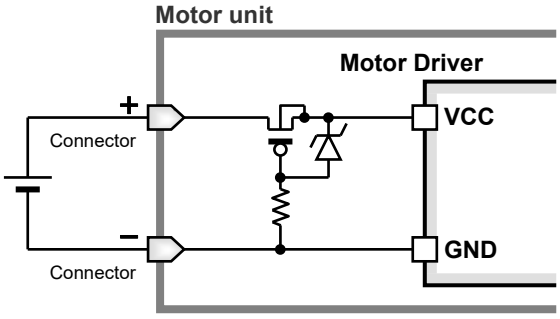


Figure 82. Reverse Connection Protection Circuit 1

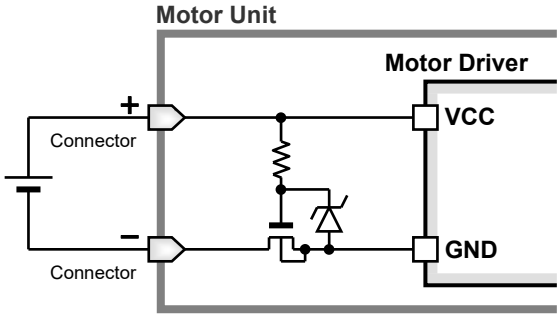


Figure 83. Reverse Connection Protection Circuit 2

2. Countermeasure Against VCC Pin Voltage Rise by Back Electromotive Force

Back electromotive force (Back EMF) generates regenerative current to power supply. However, when reverse connection protection diode is connected or the power supply does not have sufficient current absorption capability, VCC voltage and motor drive output voltage rise during regenerative braking.

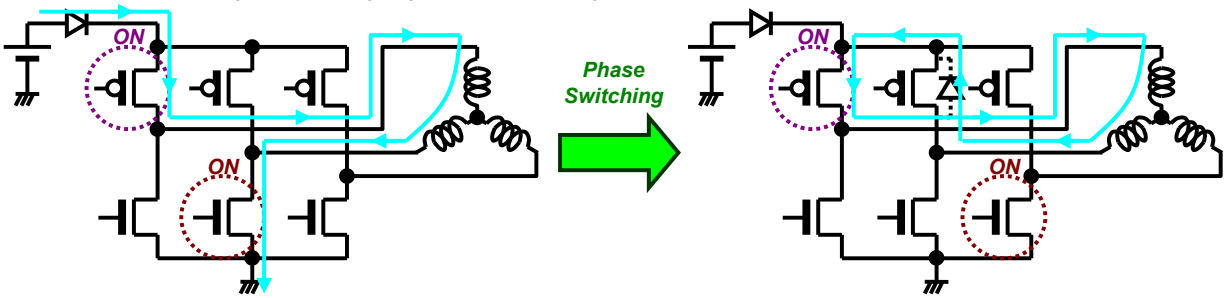


Figure 84. VCC Voltage Rise by Back Electromotive Force

When the voltage rise by back electromotive force may exceed to absolute maximum ratings, place capacitor or zener diode between VCC and GND for regenerative current route. If necessary, add both.

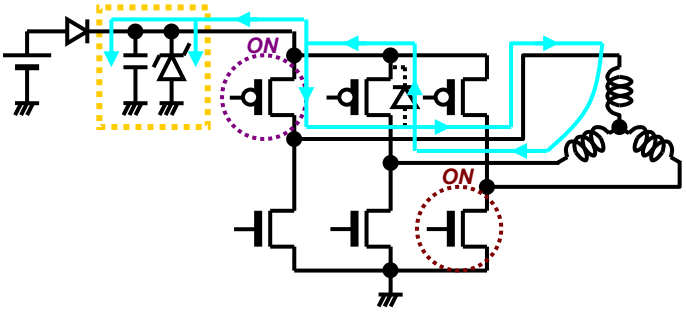


Figure 85. Prevention of VCC Voltage Rise during Regenerative Braking

Safety Measure - continued

3. VCC Pin Voltage Stabilization Measure Against Fluctuation in Power Supply

When VCC pin may exceed to absolute maximum ratings or may detect UVLO function by the fluctuation in power supply, place resistor or inductors such as ferrite beads as a filter between the power supply and VCC pin.
In the case, place a bypass capacitor together to lower the impedance of the power supply line and supply a stable voltage to the motor driver.

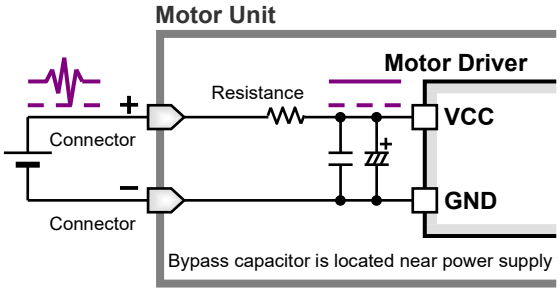


Figure 86. Power Supply Stabilization Measure (RC Filter)

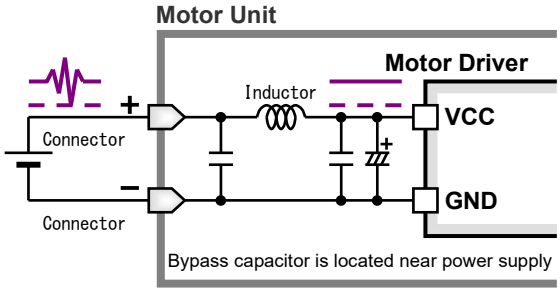


Figure 87. Power Supply Stabilization Measure (LC Filter)

4. Open Drain Pin Protection Measure

By adding the protection resistor in a motor unit, the SOUT pin and the FOUT pin can be protected from overcurrent that exceeds the absolute maximum ratings. In addition, a low-pass filter can be measure against for wrong operation.

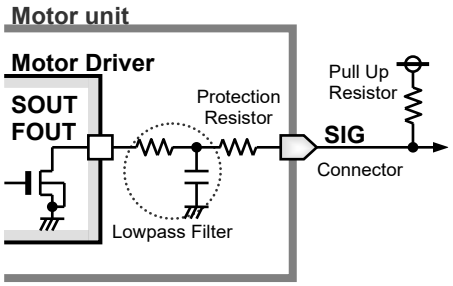


Figure 88. Open Drain Pin Protection Measure

5. GND Line PWM Switching Prohibited

Do not perform PWM switching of GND line because the GND pin potential cannot be kept to a minimum.

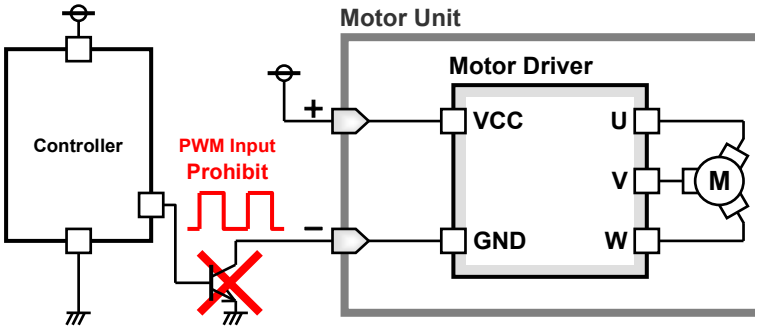


Figure 89. GND Line PWM Switching Prohibited

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

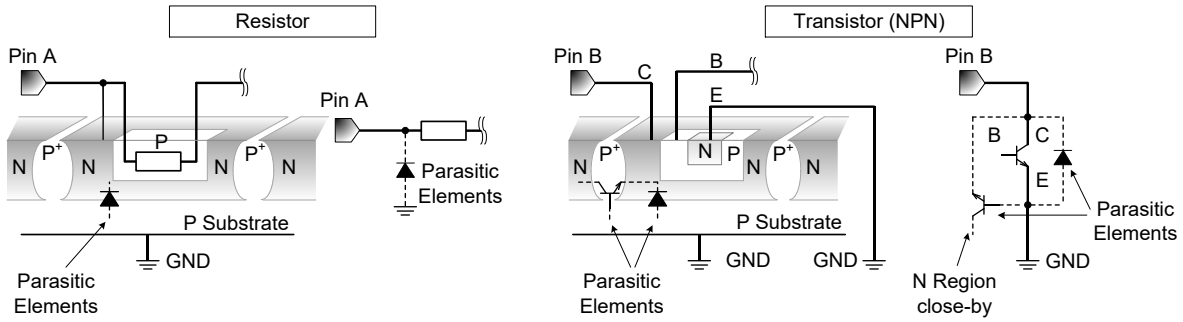


Figure 90. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins.
This IC supports two configurations, Retry Mode and Latch Mode.
When configured in Retry Mode, when the Tj falls below the TSD threshold, the outputs are automatically restored to normal operation.
When configured in Latch Mode, the TSD circuit keeps the outputs in the OFF state even if the Tj falls below the TSD threshold. The IC should be powered down and turned ON again to resume normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

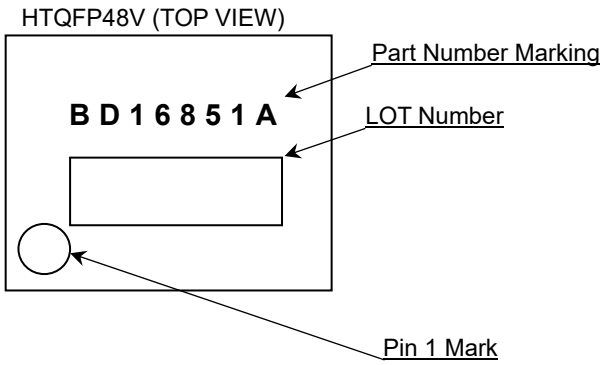
Ordering Information

B	D	1	6	8	5	1	A	E	K	V	-	CE2

Package
EKV: HTQFP48V

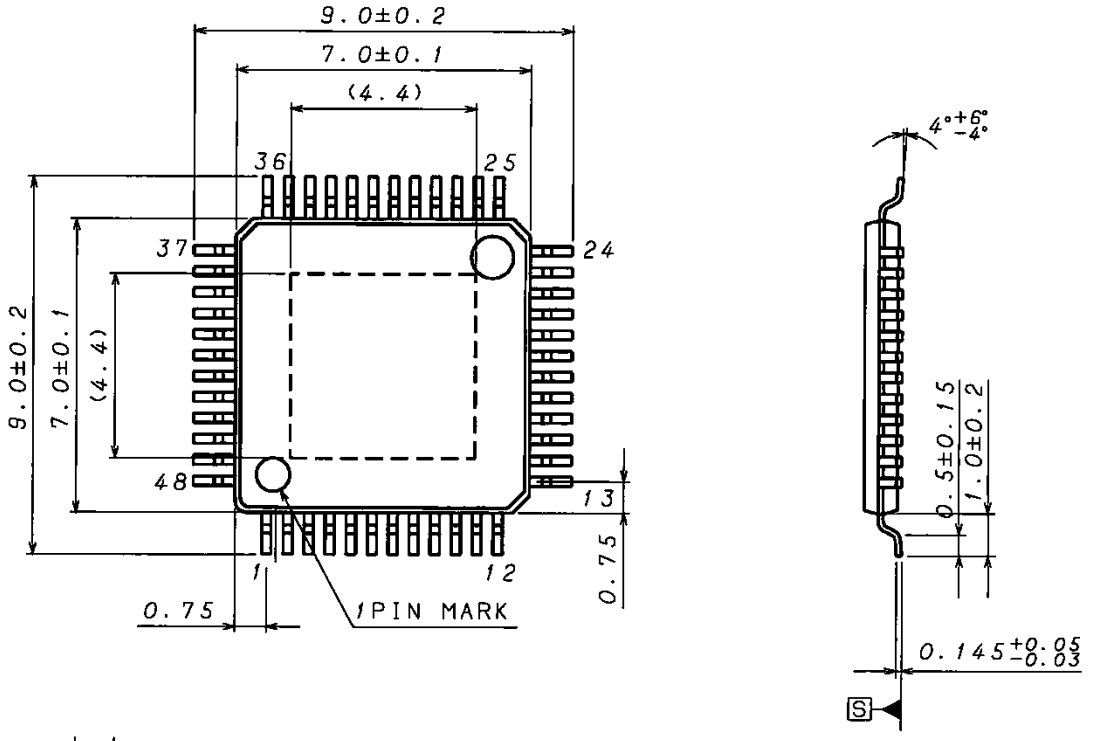
Product Rank
C: for Automotive
Packaging and Forming Specification
E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	HTQFP48V

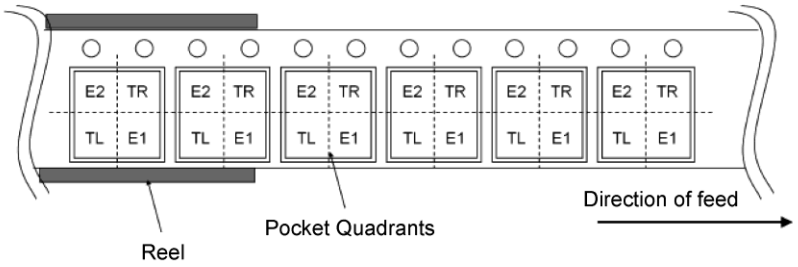


(UNIT:mm)

PKG:HTQFP48V
Drawing No.EX283-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
06.Apr.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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