

Automotive Motor Driver Series

3-phase Brushless Motor Pre-driver for Automotive

BD63034MUF-C

General Description

BD63034MUF-C is a 180° commutation sine wave pre-driver for 3-phase brushless motors. A 180° commutation sine wave drive minimizes motor drive noise. It generates a drive signal from the 3-hole sensor signal and can be PWM driven by the input control signal. This product has a lead angle control function linked to the speed for high efficiency. Also, it can support various motor controls because the lock protection time, over current limit detection value, over current protection detection value, and start-up time can be set by external constants.

Features

- AEC-Q100 Qualified^(Note 1)
- 180° Commutation Sine Wave Drive (2-phase Modulation)
- Speed Feedback/Open Control Selection
- Hall Element and Hall IC Compatible
- Speed Linked Lead Angle Control Function
- Built-in Charge Pump
- Forward Rotation/Reverse Rotation Switch Function
- Variable Speed Control (PWM/DC Input Support)
- Selectable Input-output Profile/Dead Time
- Soft Start, Soft Stop Setup Function
- Built-in Protective Functions
 - Over Voltage Protection (OVP),
 - Under Voltage Lockout (UVLO),
 - Over Current Limit (OCL),
 - Over Current Protection (OCP),
 - Motor Lock Protection (MLP),
 - Thermal Shutdown (TSD)

(Note 1) Grade 1

Key Specifications

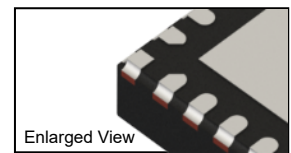
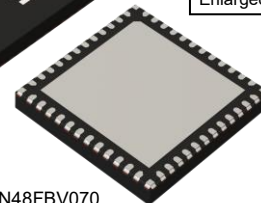
- Supply Voltage Range: 6.5 V to 18.0 V
- Bonding Temperature Range: -40 °C to +150 °C

Package

VQFN48FBV070

W (Typ) x D (Typ) x H (Max)

7.0 mm x 7.0 mm x 1.0 mm

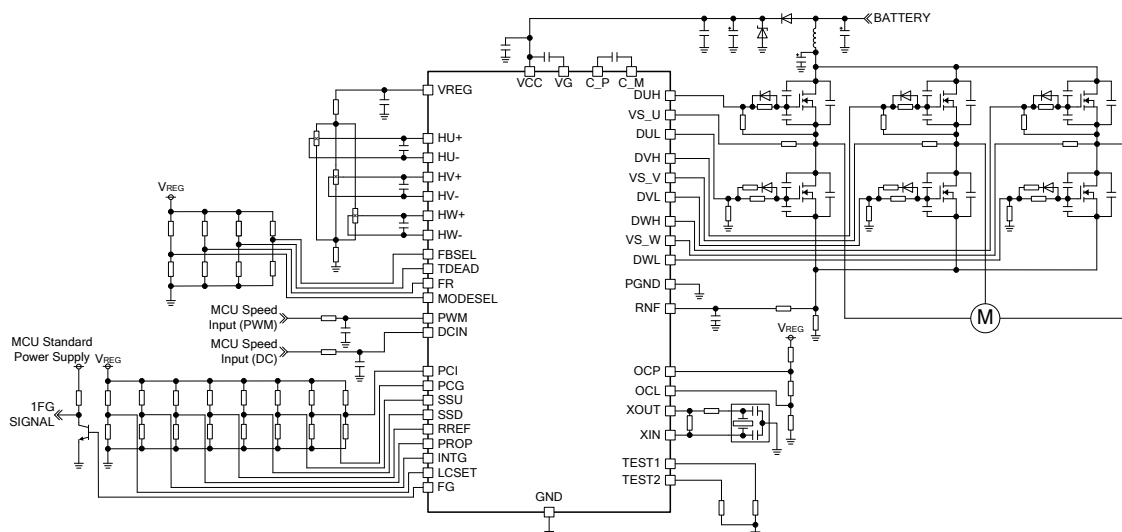


VQFN48FBV070
Wettable Flank Package

Applications

- Air Conditioning Blower Motor
- Battery Cooling Fan Motor
- Power Seat Motor

Typical Application Circuits

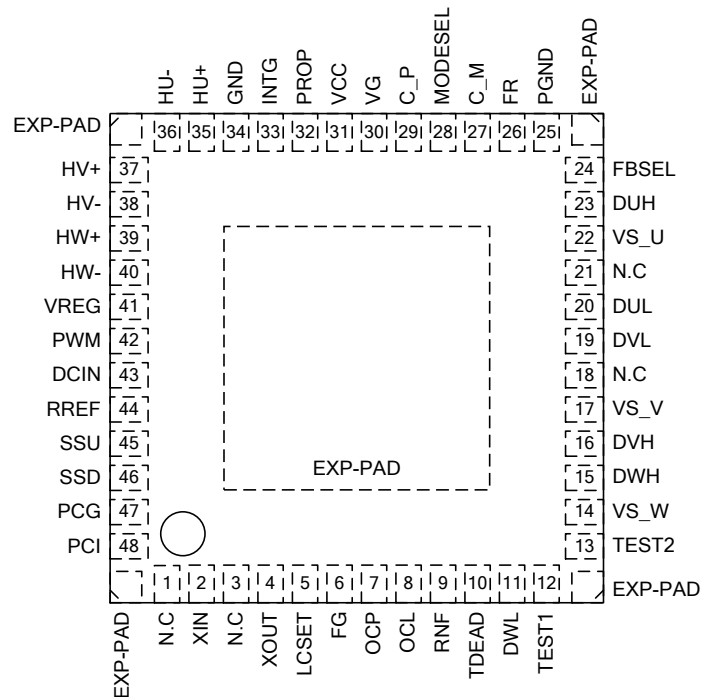


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Pin Configuration

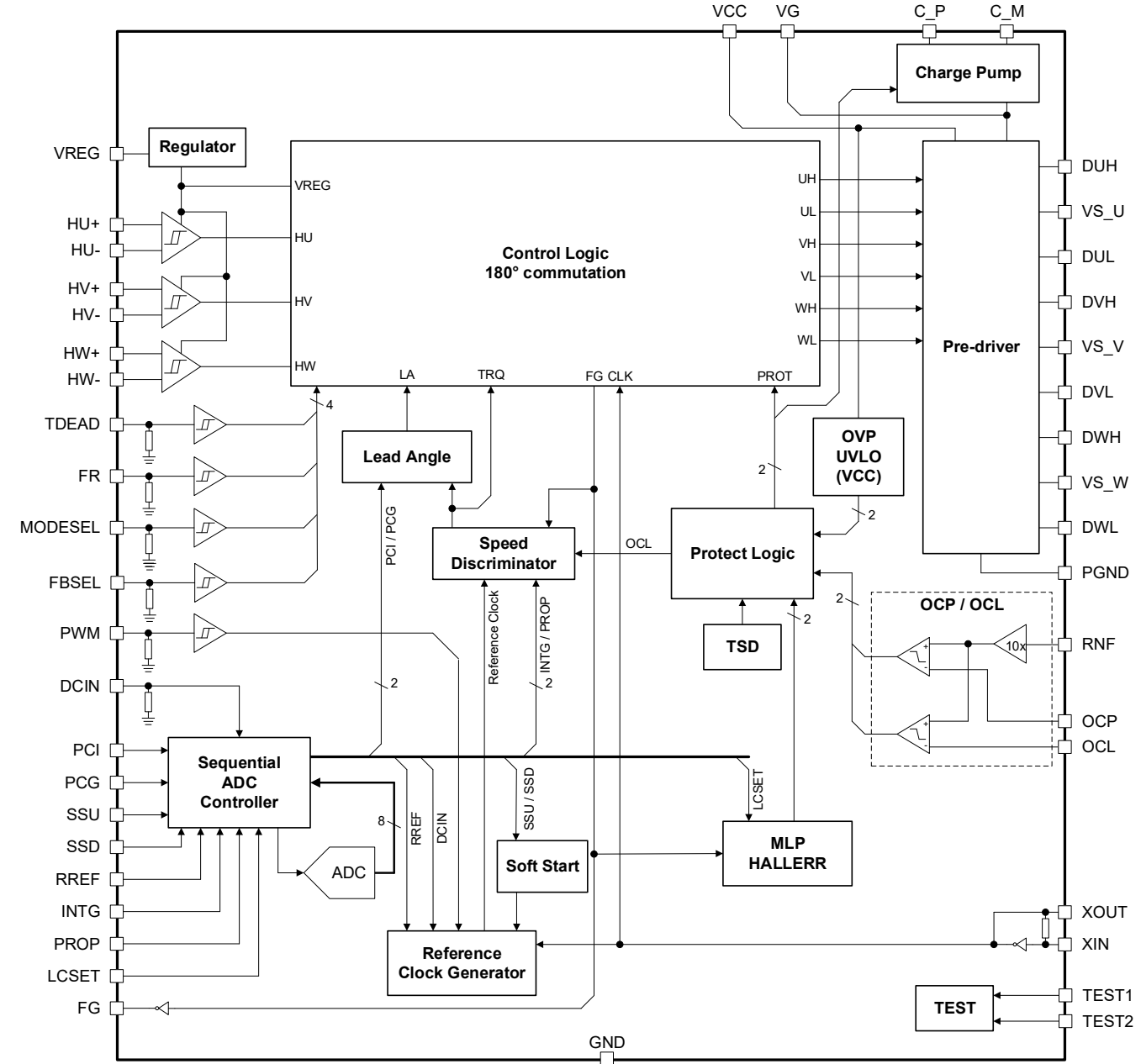
(TOP VIEW)



Pin Description

No.	Pin Name	Function	No.	Pin Name	Function
1	N.C	- (No connection)	26	FR	Forward/reverse select input
2	XIN	External CLK input	27	C_M	Charge pump capacitor minus side connection
3	N.C	- (No connection)	28	MODESEL	Input/output mode select input
4	XOUT	External CLK output	29	C_P	Charge pump capacitor plus side connection
5	LCSET	Lock protection time setup input	30	VG	Boost voltage output
6	FG	Rotational speed output	31	VCC	Power supply input
7	OCP	Over current protection setup input	32	PROP	Speed control gain setup input (proportional control)
8	OCL	Over current limit setup input	33	INTG	Speed control gain setup input (integral control)
9	RNF	Current detection input	34	GND	GND input
10	TDEAD	Dead time select input	35	HU+	U-phase plus side hall signal input
11	DWL	W-phase low side MOS-FET drive output	36	HU-	U-phase minus side hall signal input
12	TEST1	Test pin input (Connect to GND)	37	HV+	V-phase plus side hall signal input
13	TEST2	Test pin input (Connect to GND)	38	HV-	V-phase minus side hall signal input
14	VS_W	W-phase motor drive output	39	HW+	W-phase plus side hall signal input
15	DWH	W-phase high side MOS-FET drive output	40	HW-	W-phase minus side hall signal input
16	DVH	V-phase high side MOS-FET drive output	41	VREG	Reference voltage (5 V) output
17	VS_V	V-phase motor drive output	42	PWM	Rotational speed command PWM duty input
18	N.C	- (No connection)	43	DCIN	Rotational speed command DC voltage input
19	DVL	V-phase low side MOS-FET drive output	44	RREF	Speed control maximum speed setup input
20	DUL	U-phase low side MOS-FET drive output	45	SSU	Duty slope up time setup input
21	N.C	- (No connection)	46	SSD	Duty slope down time setup input
22	VS_U	U-phase motor drive output	47	PCG	Lead angle control gain setup input
23	DUH	U-phase high side MOS-FET drive output	48	PCI	Lead angle control initial torque setup input
24	FBSEL	Speed feedback/open control select input	-	EXP-PAD	The EXP-PAD of the center of product connect to GND. The EXP-PADs on the center and corner of the product are shorted inside the package.
25	PGND	POWER GND input			

Block Diagram



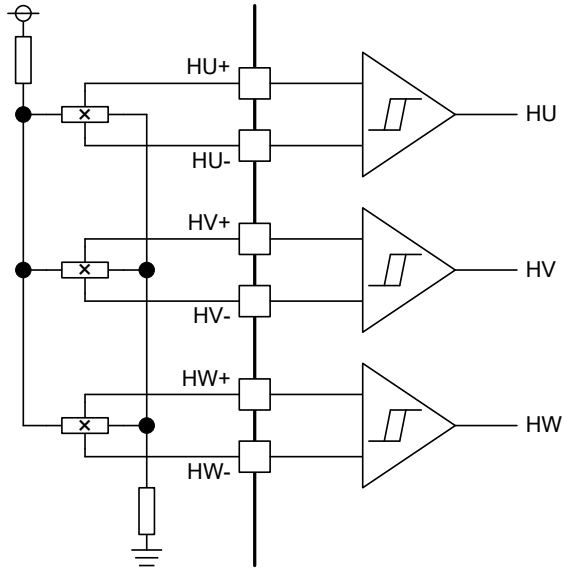
Functional Description *(Note 1)*

(Note 1) The time and frequency characteristics are when the frequency input to the XIN pin is 10 MHz.

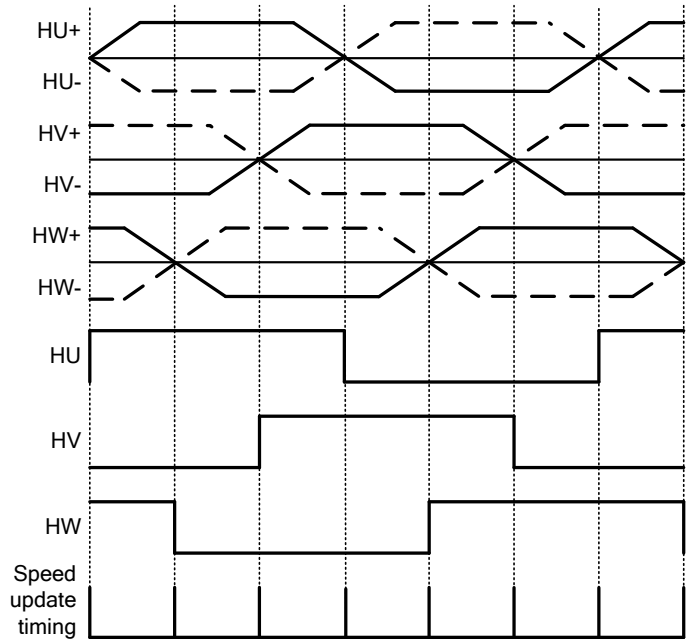
1. Overview**(1) Motor Sensing**

The motor information (rotational speed, rotational direction and phase) is detected by the 3-phase Hall signals such as U-phase, V-phase, and W-phase.

The signal of each phase (H^+/H^-) is input to Hall comparator, and the signal switching point (zero-cross point) is used as the Hall signal.



(a) Hall Signal Input Circuit



(b) Hall Signal

Figure 1. Hall Signal Input

Due to the use of zero-crossing point detection, this system is also applicable to Hall IC.

Hall Input Voltage Amplitude: Please set the bias current for the Hall element so that the minimum input voltage is 35 mVpp, and the common-mode input voltage range is 0 V to $V_{REG} - 1.2$ V. If the Hall input is affected by noise, attach a capacitor as close as possible to the input pins to eliminate the noise. Additionally, when using a Hall IC and the Hall signal is affected by noise, place a capacitor between the Hall power supply and GND to eliminate the noise.

1. Overview - continued

(2) Commutation Sequence

From startup until the motor rotation frequency reaches 1.59 Hz, 120° commutation is applied. The Hall frequency is measured every 60° electrical angle^(Note 1), and when it reaches three times 1.59 Hz or above, it switches to 180° commutation.

Upper and Lower side arms output logic for Hall input of 120° commutation and 180° commutation is in the following tables.

Input/Output Logic of 120° Commutation Drive^(Note 2) ^(Note 3)

HU	HV	HW	CW: clockwise (U to V to W)						CCW: counter-clockwise (U to W to V)					
			DUH	DUL	DVH	DVL	DWH	DWL	DUH	DUL	DVH	DVL	DWH	DWL
H	L	H	L	H	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	L	H	L	H
H	L	L	L	H	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H	L	H
H	H	L	L	H	L	H	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	L	H
L	H	L	PWM	$\overline{\text{PWM}}$	L	H	L	H	L	H	PWM	$\overline{\text{PWM}}$	L	H
L	H	H	PWM	$\overline{\text{PWM}}$	L	H	L	H	L	H	L	H	PWM	$\overline{\text{PWM}}$
L	L	H	L	H	PWM	$\overline{\text{PWM}}$	L	H	L	H	L	H	PWM	$\overline{\text{PWM}}$

Input/Output Logic of 180° Commutation Drive^(Note 3)

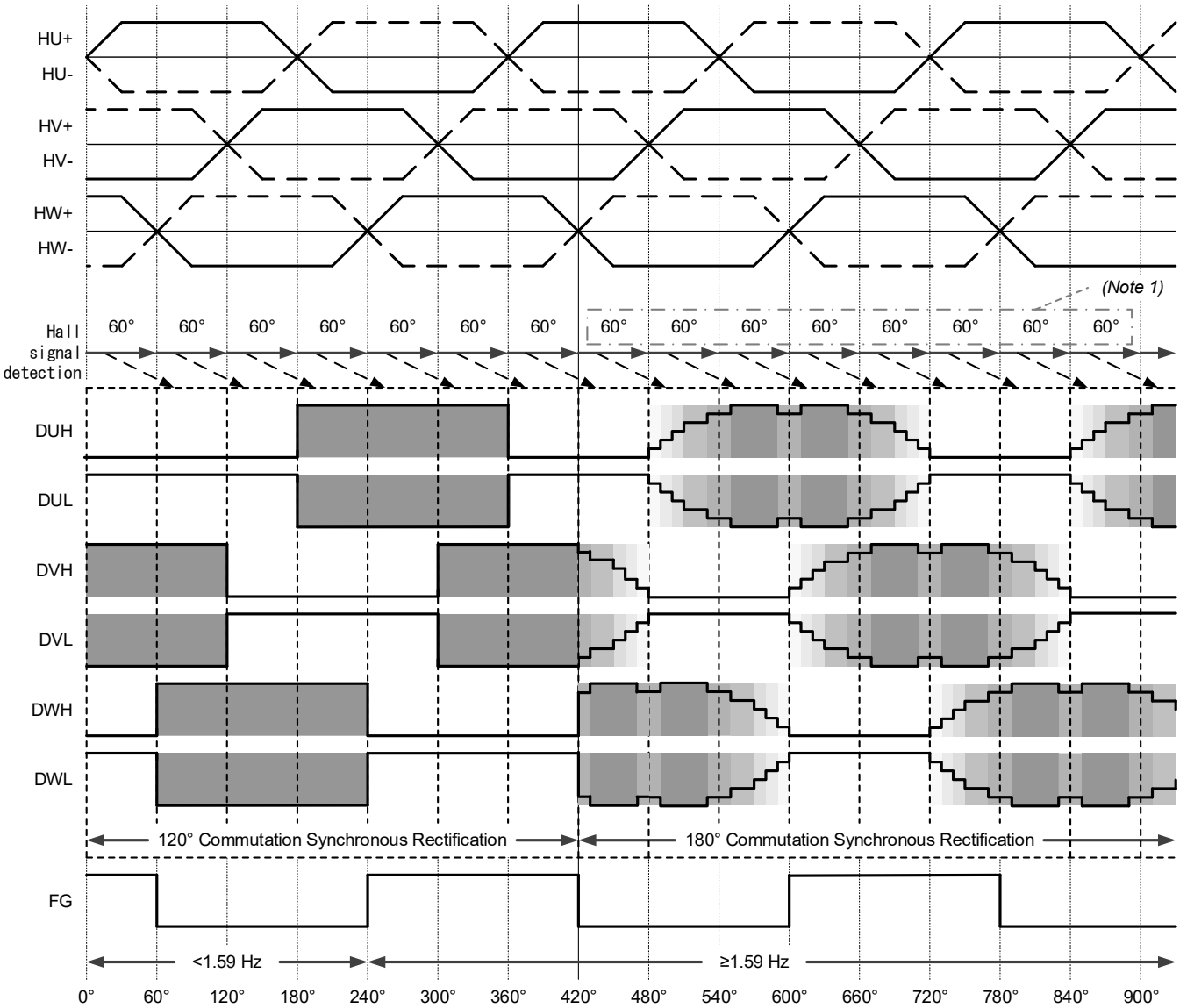
HU	HV	HW	CW: clockwise (U to V to W)						CCW: counter-clockwise (U to W to V)					
			DUH	DUL	DVH	DVL	DWH	DWL	DUH	DUL	DVH	DVL	DWH	DWL
H	L	H	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$
H	L	L	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H
H	H	L	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H
L	H	L	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$
L	H	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$
L	L	H	PWM	$\overline{\text{PWM}}$	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$	L	H	PWM	$\overline{\text{PWM}}$

(Note 1) 360° electrical angle = 1 Hall signal cycle.

(Note 2) Asynchronous rectification at reverse detection, and low output for PWM reverse output logic of the lower side arm output.

(Note 3) L means low, while H means high.

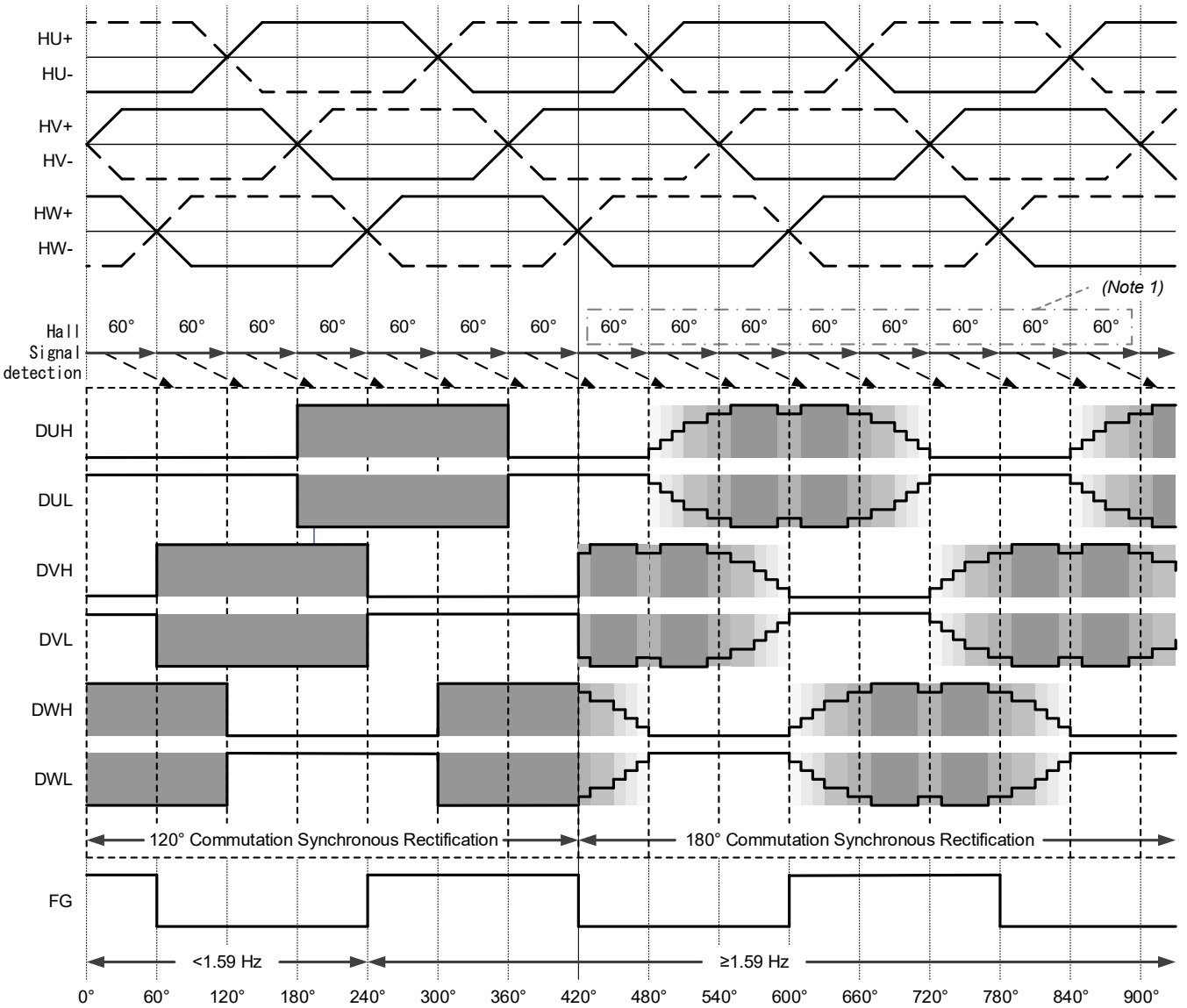
(2) Commutation Sequence – continued



(Note 1) The drive waveform is generated every 60° electrical angle even if it is switched to 180° synchronous rectification drive because it is in the accelerated state at startup.

Figure 2. Startup Timing Chart (FR = High Forward Rotation)

(2) Commutation Sequence - continued



(Note 1) The drive waveform is generated every 60° electrical angle even if it is switched to 180° synchronous rectification drive because it is in the accelerated state at startup.

Figure 3. Startup Timing Chart (FR = Low Reverse Rotation)

If the rotation direction of the FR input logic and the Hall input logic does not match, it operates with 120° commutation (asynchronous rectification drive).

		FR Input Logic	
		High (CW) CW: clockwise (U to V to W)	Low (CCW) CCW: counter-clockwise (U to W to V)
Hall Input Logic	Forward (CW)	180° commutation	120° commutation (asynchronous rectification)
	Reverse (CCW)	120° commutation (asynchronous rectification)	180° commutation

1. Overview - Continued

(3) Generation of Driving Waveform

The waveform pattern of motor drive waveform is generated and output every 360° electrical angle. Based on the falling edge of W-phase Hall signal (HW), the period of drive waveform is estimated from the period between edges, and the waveform for one period is generated. After that, the waveform pattern is output with the falling edge of W-phase Hall signal as the switching point.

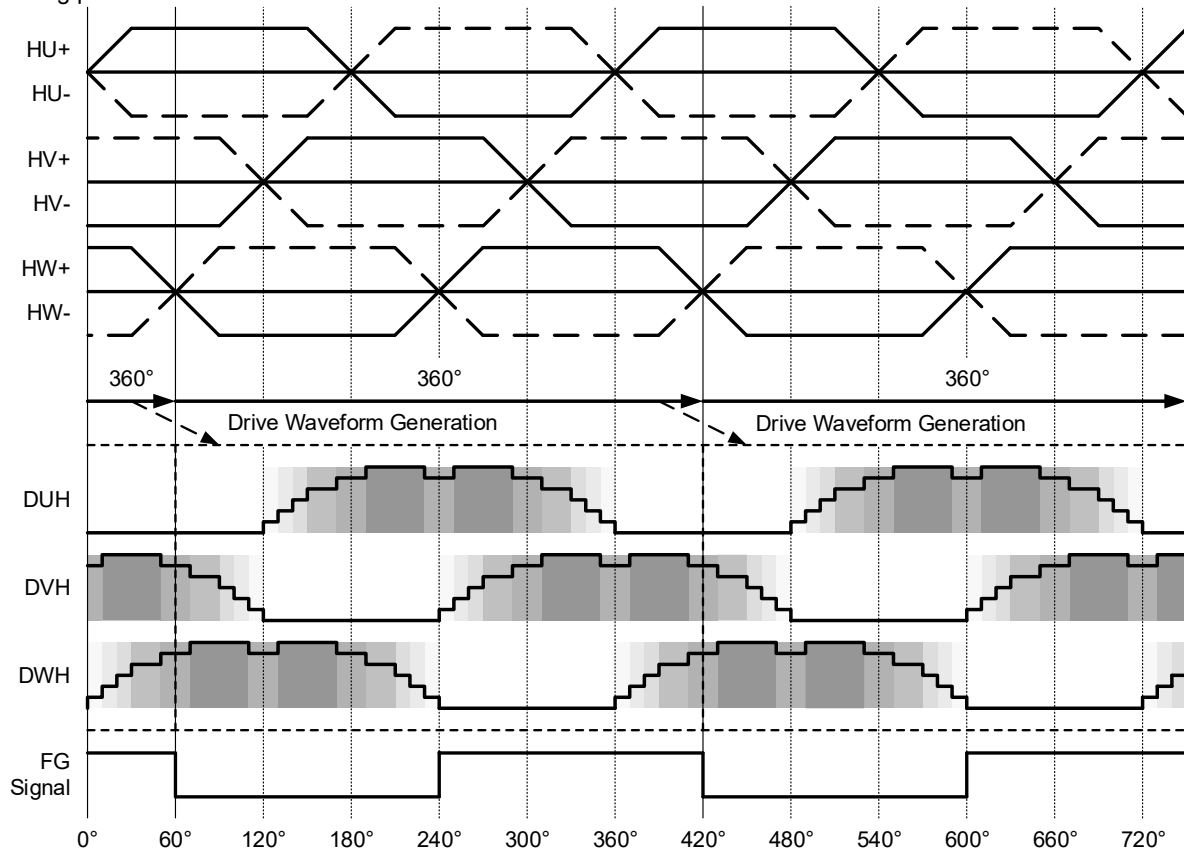


Figure 4. Drive Waveform Generation (Batch Generation Mode)

If there is a deviation between the actual phase and the phase (estimated phase) of drive waveform during acceleration/deceleration, the generation of drive waveform is changed from every 360° electrical angle (batch generation mode) to every 60° (sequential generation mode) in order to reduce current distortion.

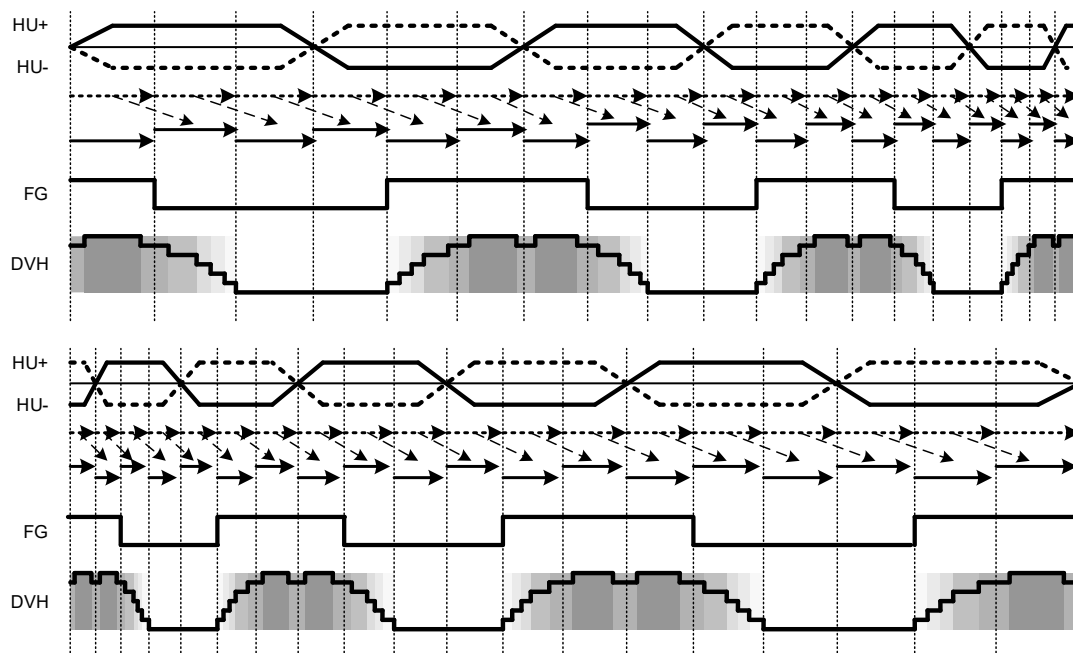


Figure 5. Drive Waveform Generation during Acceleration (top) and Deceleration (bottom) (Sequential Generation Mode)

1. Overview - Continued

(4) Phase Relation of Voltage and Current

When the lead angle on pre-driver side is set to 0° and the motor is a delta connection, the phase relation of voltage and current is shown in Figure 6 and Figure 7 depending on the FR setting. When FR = High, the output switching of DUH (Pre-driver U-phase High side output signal) starts at 120° position behind the rising edge of HU+ (U-phase Hall positive signal). When FR = Low, the output switching of DUH (Pre-driver U-phase High side output signal) starts from the rising edge of HU+ (U-phase Hall positive signal).

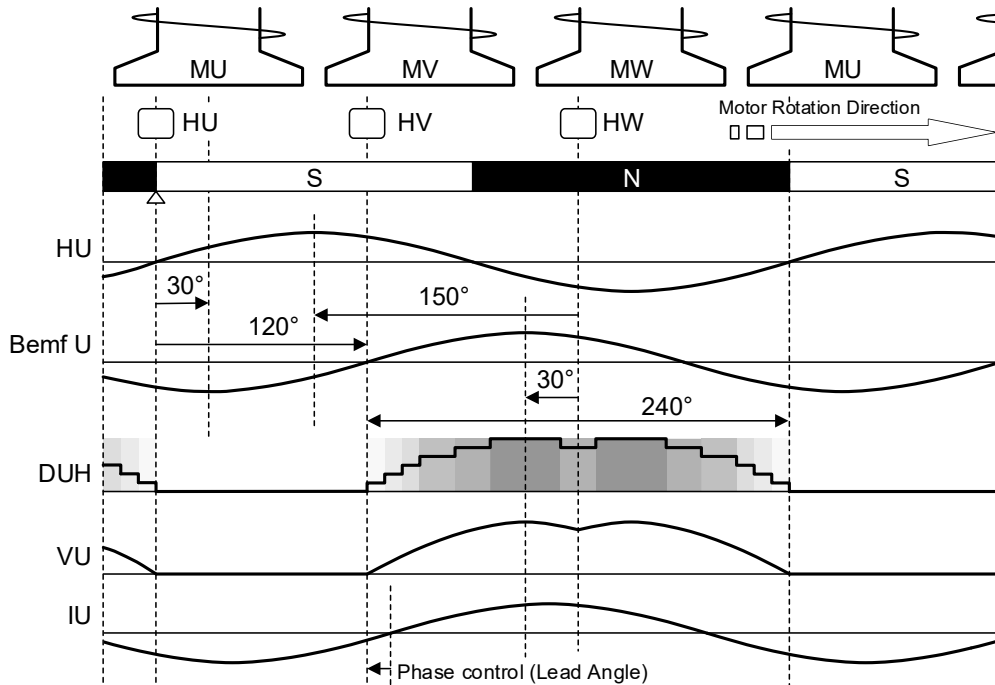


Figure 6. Phase Relation of Voltage and Current of Brushless Motor (Delta Connection Pole : Slot = 2 : 3), FR = High

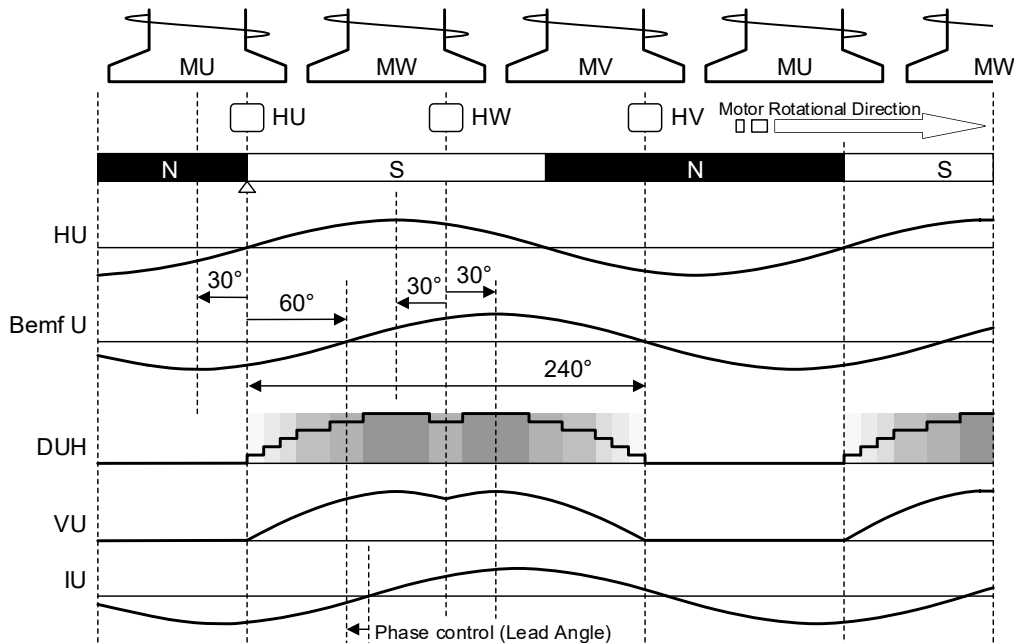


Figure 7. Phase Relation of Voltage and Current of Brushless Motor (Delta Connection Pole : Slot = 2 : 3), FR = Low

In either setting, the IU (U-phase winding current) phase is generally behind the BEMF U (U-phase inductive voltage). However, the motor power is not efficient in this state, but it can be more efficient by advancing (performing a lead angle) the phase of winding current.

(4) Phase Relation of Voltage and Current - continued

Even if the lead angle on pre-driver side is set to 0° and the motor is a star connection, the phase relation of voltage and current is shown in Figure 8 and Figure 9.

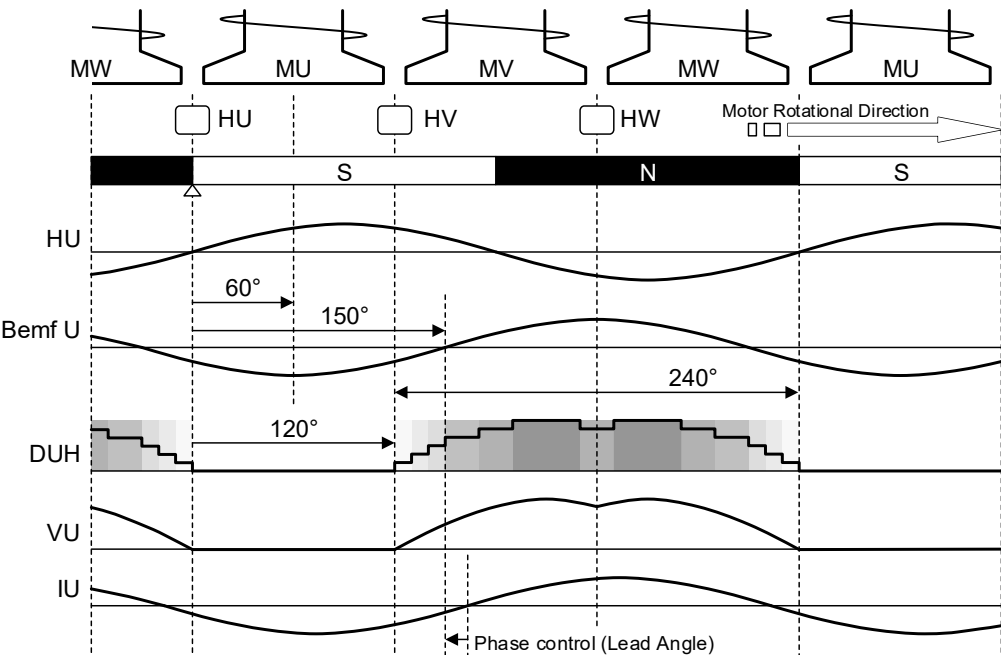


Figure 8. Phase Relation of Voltage and Current of Brushless Motor (Star Connection Pole : Slot = 2 : 3), FR = High

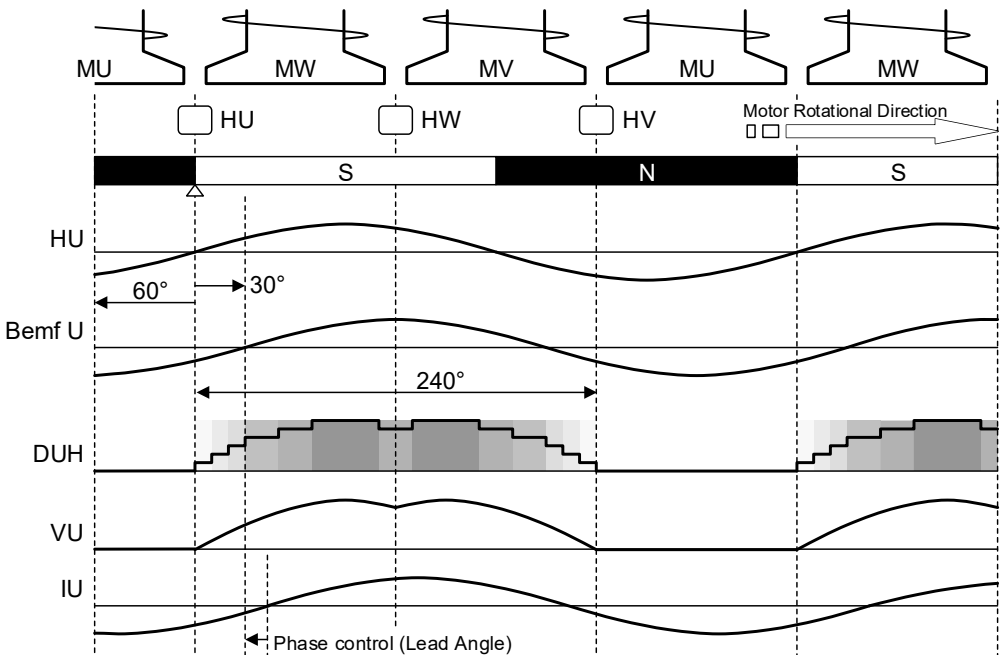


Figure 9. Phase Relation of Voltage and Current of Brushless Motor (Star Connection Pole : Slot = 2 : 3), FR = Low

1. Overview - Continued

(5) Rotational Speed command Input (PWM, DCIN)

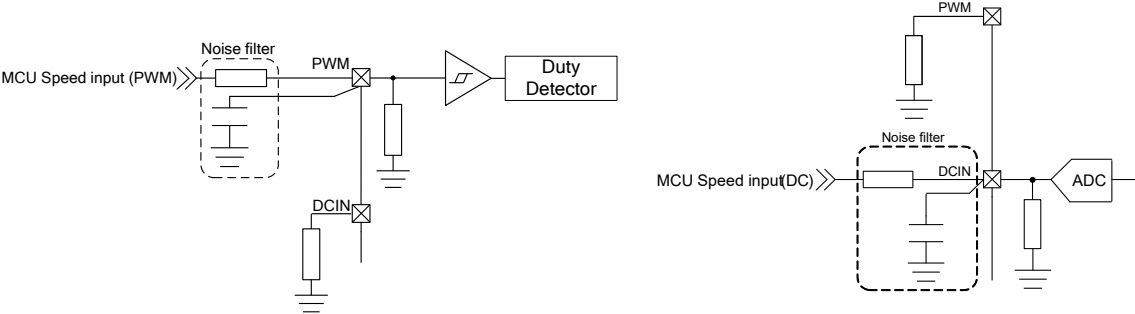
DC input or PWM input can be selected for rotational speed command.

When using PWM input, rotational speed command value is input by changing the Duty of PWM (High active input). Once a rising edge of PWM is detected, it enters ACTIVE state that driving the motor. In that case, the upper and lower gate drive outputs according to the 3-phase hall input. If frequency of $f_{PWM} \leq 19.0\text{ Hz}$, $f_{PWM} \geq 1.25\text{ kHz}$ is input into the PWM pin, it enters the IDLE state, which is a waiting state for PWM signal input.

In the IDLE state, when operating in speed feedback mode (FBSEL = Low), both the upper and lower gate drive output is Low and the charge pump is Hi-Z. When operating in open control mode (FBSEL = High), the upper gate drive output is Low, the lower gate drive output is High and the charge pump continues operate. Insert an appropriate filter^(Note 1) for the PWM pin.

When using DC input, the ratio of the DCIN voltage to the V_{REG} functions as the input parameter for the rotational speed command. In consideration of the noise between wires when applying voltage, make sure to insert an appropriate filter^(Note 1) not to exceed the rated voltage of the DCIN pin.

(Note 1) Consider the pin impedance when configuring the filter. For the pin impedance, refer to input current of each pin (PWM, DCIN) in "Electrical Characteristics".



(a) PWM Input Application Circuit Diagram (b) DC Input Application Circuit Diagram
Figure 10. Rotational Speed Command Input Application Circuit Diagram

The PWM input has priority if PWM and DCIN are input at the same time. However, such operation should be avoided as it may cause malfunction. In addition, when PWM is high and VCC power turns on, the IDLE state is maintained and the motor does not operate. Be sure to input PWM after V_{REG} reaches a stable voltage.

	PWM Pin Input				
	Open (Hi-Z) (internal pulled-down)	Fixed to Low ($f_{PWM} \leq 19.0\text{ Hz}$)	f_{PWM} (20 Hz to 800 Hz)	$f_{PWM} \geq 1.25\text{ kHz}$	Fixed to High ($f_{PWM} \leq 19.0\text{ Hz}$)
Start Up	IDLE	IDLE	ACTIVE	IDLE	IDLE
Driving	IDLE	IDLE	ACTIVE	IDLE	By MODESEL configuration

	DCIN Pin Input		
	Open (Hi-Z) (internal pulled-down)	$DCIN \leq 0.235\text{ V}$	$DCIN \geq 0.235\text{ V}$
State	IDLE	IDLE	ACTIVE

Functional Description – continued

2. Setting of Various Parameters

(6) A/D Converter

The setup to control functions such as rotational speed command (DCIN), speed control (RREF, INTG, PROP), lead angle control (PCI, PCG), duty slope (SSU, SSD) and lock protection time setup (LCSET) is available by applying the resistance voltage divider of V_{REG} ^(Note 1) to the corresponding pin. Zero scale is GND, and the full scale is V_{REG} . The applied voltage is sampled by the A/D converter with 256 levels of resolution. 1LSB is 19 mV.

Pin Name	Number of Settings	Function
DCIN	256	Rotational speed command input
RREF	32	Speed control maximum speed setup input
PROP	256	Speed control (Proportional) gain setup input
INTG		Speed control (Integral) gain setup input
PCI		Lead angle control initial torque setup input
PCG		Lead angle control gain setup input
SSU		Duty slope up time setup input
SSD		Duty slope down time setup input
LCSET		Lock protection time setup input

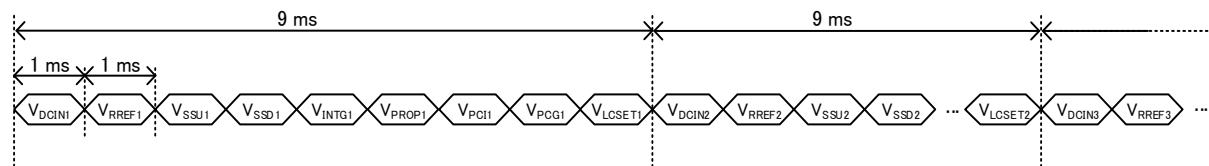


Figure 11. A/D Converter Operation Sequence

(Note 1) Set the input impedance to 5 MΩ or less.

The A/D Converter repeatedly takes samples of pin voltage in order to determine whether the parameter has been updated. The parameter does not change unless it exceeds the ±1 LSB range of initial value (similar to the timing of V_{RREF1} to V_{RREF3}). To update the set value, the following two conditions must be met:
The initial value must exceed the ±1 LSB range.

The value that exceeds the initial value must be within the ±1 LSB range^(Note 2) for three times (similar to the timing of V_{RREF7} to V_{RREF9}).

(Note 2) If input is changed by resolution less than 2 LSB, the default may not be changed due to the above specifications.

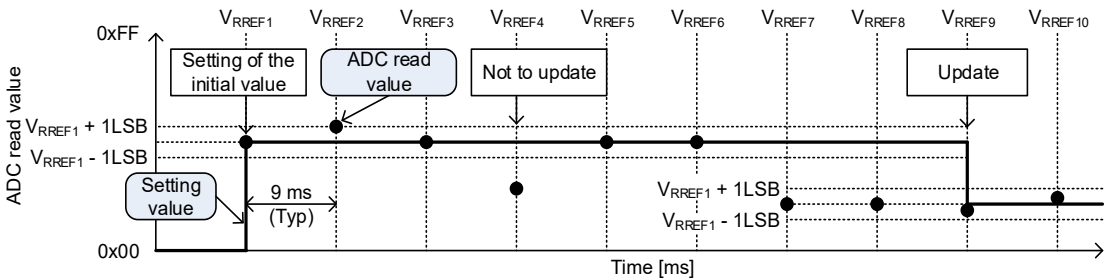


Figure 12. Update of A/D Converter Data

2. Setting of Various Parameters - continued

(7) Target RPM Setting (RREF)

The maximum rotational speed (f_{MAXRPM}) can be set by applying a voltage divided by resistance from the V_{REG} to the RREF pin.

The target of rotational speed by the feedback (REFCLK) is set with the maximum rotational speed determined by RREF and with the ratio of the rotational speed target against the maximum rotational speed determined by PWM input Duty (D_{PWM}) or the DCIN voltage relative to V_{REG} .

However, it is only a valid function for speed feedback mode (FBSEL = Low).

$$f_{MAXRPM} = (600 - 100) \times \frac{V_{RREF}}{V_{REG}} + 100 \quad [\text{Hz}]$$

$$MAXRPM = f_{MAXRPM} \times \frac{2}{Pole} \times 60 \quad [\text{min}^{-1}]$$

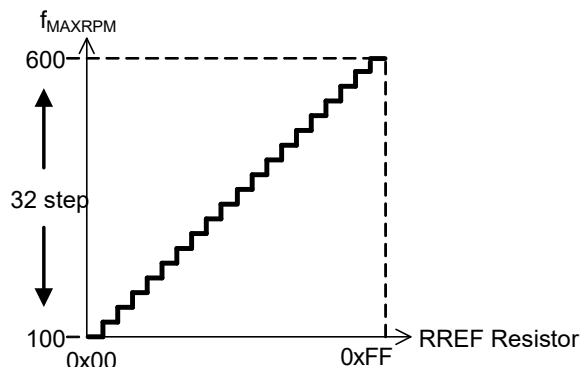


Figure 13. Maximum Rotational Speed Setup

When $D_{PWM} = 10\%$ to 95% , REFCLK is calculated with the following formula.

$$REFCLK = f_{MAXRPM} \times D_{PWM} \times \frac{100}{95} \quad [\text{Hz}]$$

$$RPM = REFCLK \times \frac{2}{Pole} \times 60 \quad [\text{min}^{-1}]$$

Example) When $f_{MAXRPM} = 470.6 \text{ Hz}$, Pole = 10, $D_{PWM} = 50\%$,

$$REFCLK = 470.6 \times 0.5 \times 100/95 = 247.7 \text{ [Hz]}$$

$$RPM = 470.6 \times 0.5 \times 100/95 \times 2/10 \times 60 = 2972 \text{ [min}^{-1}\text{]}$$

The frequency of REFCLK and FG generated in the hall comparator are compared, and the difference is input to loop filter in order to determine the torque (TRQ) of motor.

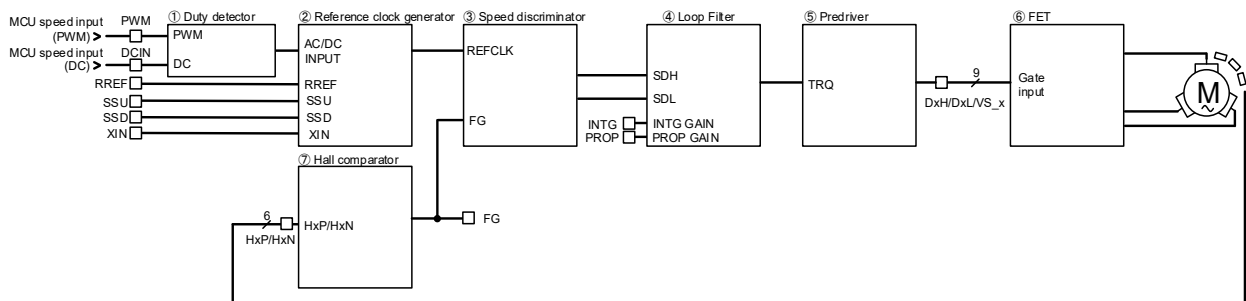


Figure 14. Configuration of Speed Control

2. Setting of Various Parameters - continued

(8) Speed Control (PROP, INTG)

The PI gain value of the speed feedback can be set by applying a voltage divided by resistance from the V_{REG} to the PROP pin and the INTG pin. However, it is only a valid function for speed feedback mode (FBSEL = Low).

The motor speed is controlled to maintain a constant speed according to the speed command input, which is provided either by the PWM input Duty cycle or the DCIN voltage. Torque (TRQ) of speed control is set as follows.

Also, the block configuration of speed control is shown below.

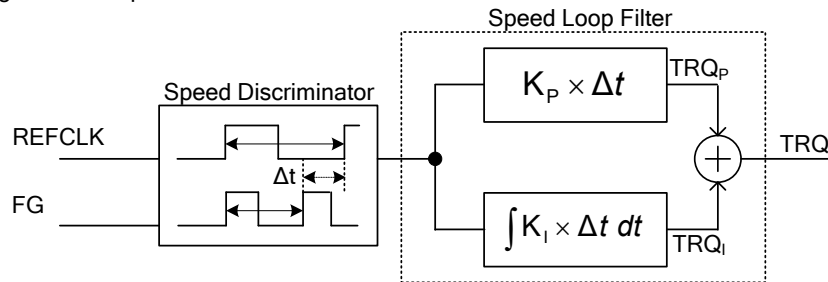


Figure 15. Block Configuration of Speed Control

Cycle difference Δt of target rotational speed (REFCLK) and actual rotational speed (FG) is counted. Based on Δt , the torque is determined by adding the torque TRQ_P calculated by the proportional control unit, and the torque TRQ_I calculated by the integral control unit.

It is calculated by the following formula.

$$TRQ = TRQ_P + TRQ_I$$

$$TRQ_P = K_P \cdot \Delta t, \quad TRQ_I = \int (K_I \cdot \Delta t) dt \quad \therefore K_P = PROP, \quad K_I = INTG$$

Time from generation of motor rotational fluctuation to stability as target rotational speed (Convergence time) is determined by the K_P (constant of proportionality) set by the PROP pin, and the K_I (constant of integration) set by the INTG pin. Torque gain is set by K_P and K_I . The TRQ_P and TRQ_I change as shown in Figure 16 follows.

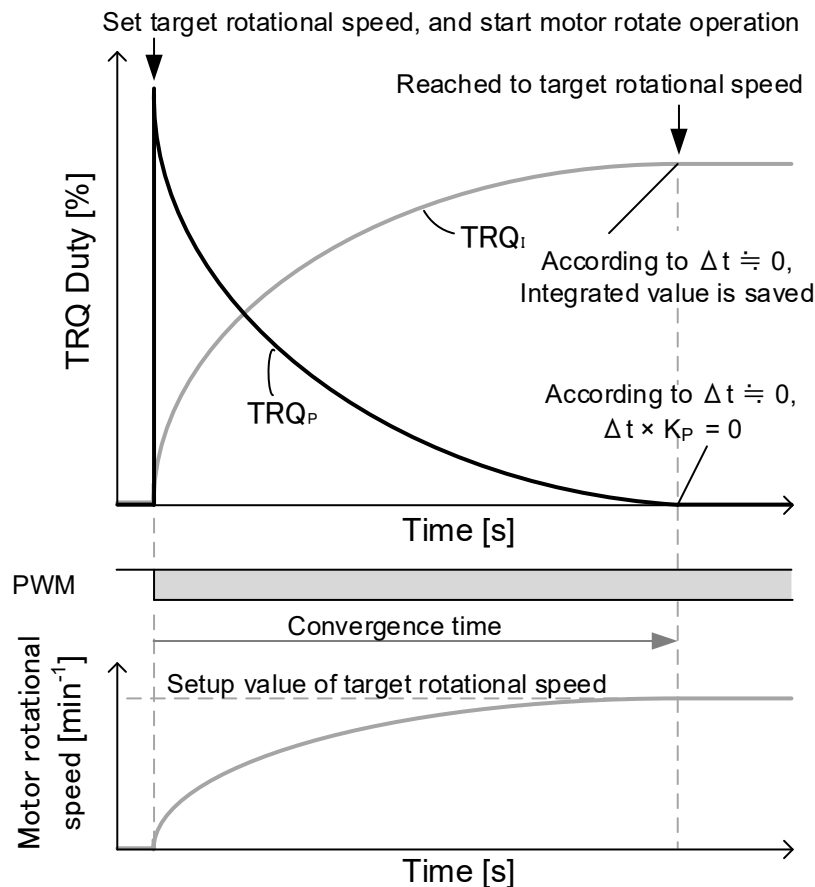


Figure 16. Transitions of TRQ_P and TRQ_I by Speed Control

(8) Speed Control - Continued

There is a torque limit function for silent start and silent operation during speed control. By placing a limit on TRQ Duty^(Note 1), excessive torque generation is suppressed. However, it is only a valid function for speed feedback mode (FBSEL = Low). The torque limit can be operated in the following two ways, depending on the rotation condition of the motor.

(Note 1) TRQ Duty refers to the ON duty ratio at the peak of the PWM pattern in the gate drive output, as shown in Figure 17.

(a) Before detecting two falling edges of the W-phase hall signal (HW) after startup

Torque is limited to TRQ Duty $\leq 15.8\%$ to suppress excessive torque during startup. Since the torque limit operates regardless of the setting speed ratio ($REFCLK/f_{MAXRPM}$), care must be taken to ensure sufficient torque for motor startup.

(b) After detecting two or more falling edges of the W-phase hall signal (HW)

The upper limit of torque restriction varies according to the speed ratio, suppressing excessive torque during speed control or SSU control^(Note 2). If the speed ratio is less than 52.6 %, the torque limit is active, so ensure sufficient torque to reach the target speed. If the speed ratio is 52.6 % or higher, the maximum TRQ Duty becomes 100 %, and torque limitation does not operate

(Note 2) Torque limit also applies to target speed with slopes applied by SSU/SSD control.

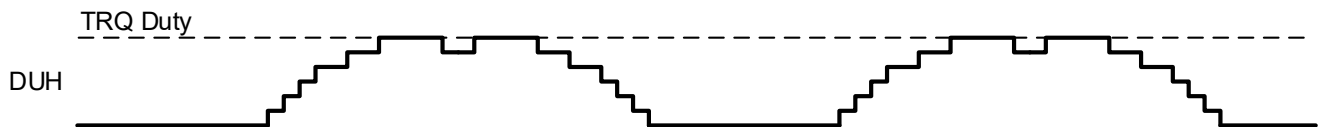


Figure 17. Relationship between Output Voltage Waveform and TRQ Duty

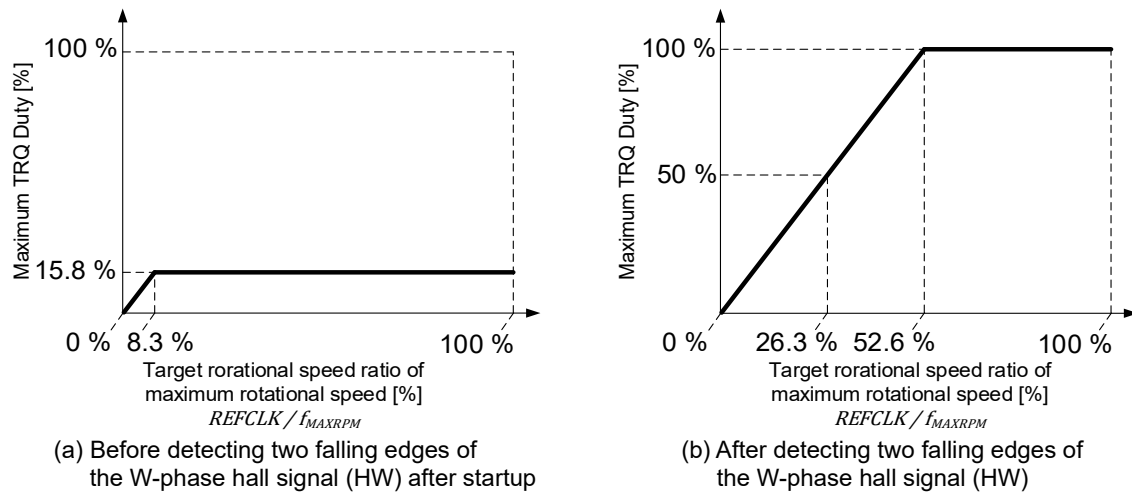


Figure 18. Speed Ratio vs Maximum TRQ Duty

2. Setting of Various Parameters - continued

(9) Lead Angle Control Setting (PCI, PCG)

The speed linked lead angle can be set by applying a voltage divided by resistance from the V_{REG} to the PCI pin and the PCG pin. The PCI pin sets the TRQ Duty point for the lead angle start, and the PCG pin sets the slope of the lead angle relative to TRQ Duty.

There are three ways to set it up:

(a) Zero lead angle setting

When set the PCI pin and PCG pin to GND and the lead angle is fixed by adjusting the stator and hole position^(Note 1) on the motor mechanism side.

(Note 1) Please refer to "(4) Phase Relation of Voltage and Current", and design the phase relation of stator and Hall positions.

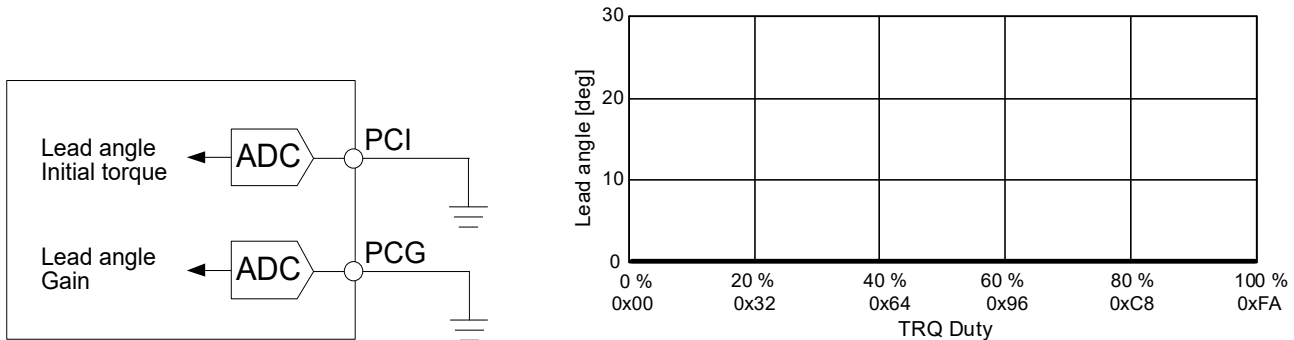


Figure 19. Zero lead angle setting

(b) Proportional lead value linked to TRQ Duty setting

When the PCI pin is GND and the PCG pin is applied at the resistive voltage of the V_{REG} .

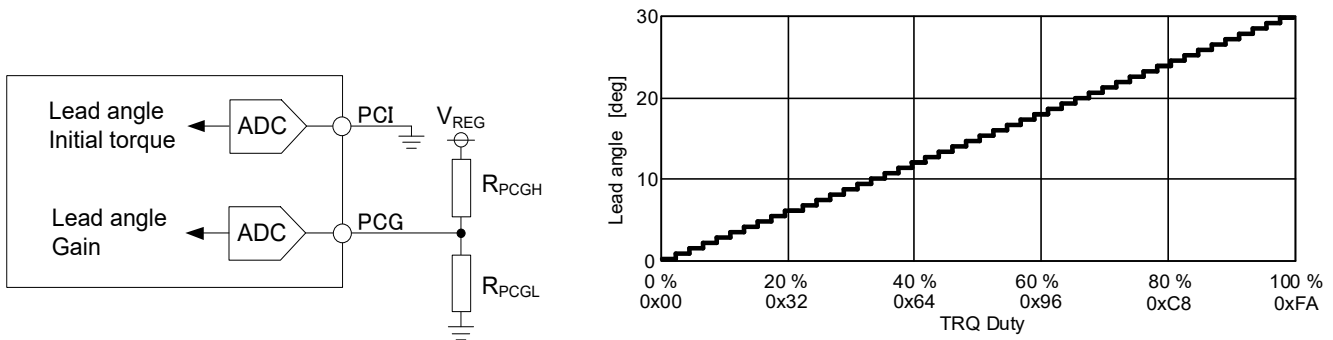


Figure 20. Proportional lead Angle Setting Linked to TRQ Duty (Example: lead Angle Start at TRQ Duty = 0%)

(c) Proportional lead value linked to TRQ Duty setting (with setting of TRQ Duty point at the start of lead angle)

When applying voltage at the resistive voltage of the V_{REG} to the PCI pin and the PCG pin.

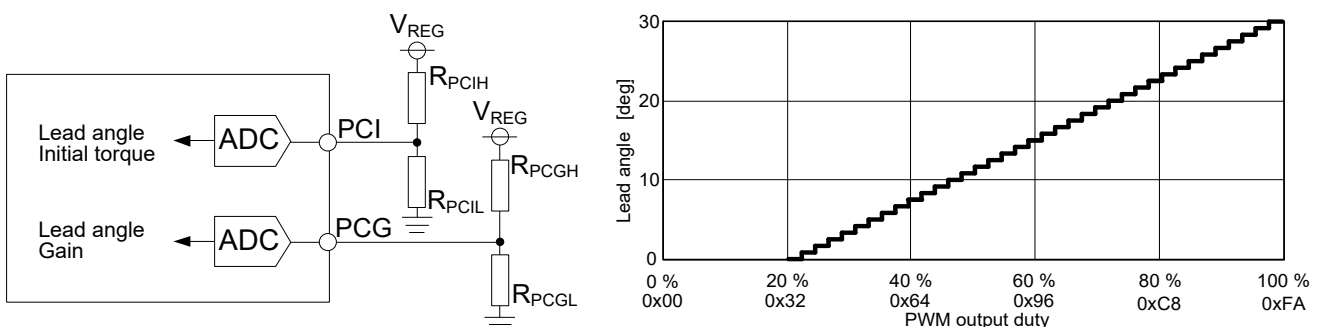


Figure 21. Proportional lead Angle Setting Linked to TRQ Duty (Example: lead Angle Start at TRQ Duty = 20 %)

(9) Lead Angle Control Setting - Continued

Maximum lead angle is 30°. Please note that the lead angle value is saturated at 30° although the lead angle value is set to more than 30° by the PCG pin.

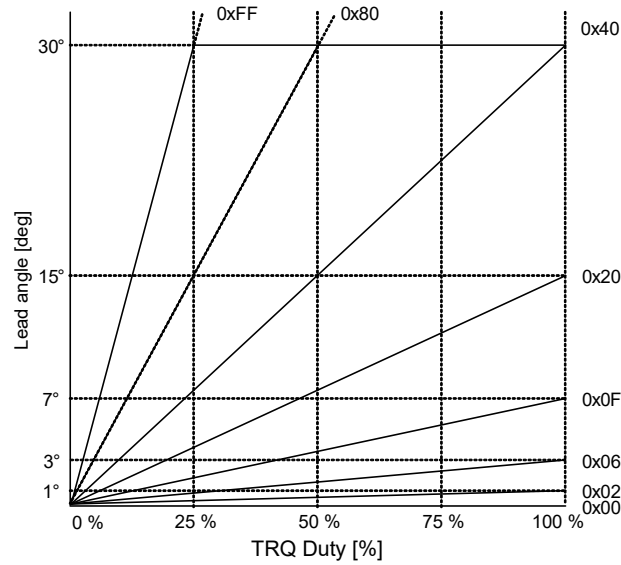


Figure 22. TRQ Duty vs PCG Setting

The lead angle amount G_{PCG} against TRQ Duty [%] is calculated using the formula below. (Note 1)

(Note 1) Minimum resolution of lead angle setup is 0.47°. Lead angle value does not change unless the lead angle value in the following formula exceeds 0.47° resolution.

$$G_{PCG} = \frac{V_{PCG}}{V_{REG}} \times 119.85 \times TRQ\ Duty \quad [deg]$$

$$\therefore G_{PCG} \leq 30 \quad [deg]$$

Example) When $\frac{V_{PCG}}{V_{REG}} = \frac{1}{2}$, TRQ Duty = 75 %,

$$G_{PCG} = \frac{1}{2} \times 119.85 \times 0.75 \geq 30, \quad \therefore G_{PCG75\%} = 30 \quad [deg]$$

With the same PGC configuration, TRQ Duty = 25 %,

$$G_{PCG} = \frac{1}{2} \times 119.85 \times 0.25 = 14.98, \quad \therefore G_{PCG25\%} = 14.57 \quad [deg]$$

The TRQ Duty D_{PCI} to start the lead angle can be calculated by using the formula below.

$$D_{PCI} = \frac{V_{PCI}}{V_{REG}} \times 100 \quad [\%]$$

Example) When $\frac{V_{PCI}}{V_{REG}} = \frac{1}{5}$, the lead angle initial TRQ Duty will be $D_{PCI} = \frac{1}{5} \times 100 = 20 \quad [\%]$.

The lead angle value is updated every eight cycles of the W-phase Hall signal. The change in value per update is 0.47° step. For example, when the lead angle setup is changed from 0° to 30°, the lead angle will be changed from 0° to 30° in 255 revolutions with 4-pole motor.

In the case of 6-pole motors and 10-pole motors, it can also be calculated using the following formula.

4-pole motor :	$\frac{30 \text{ [deg]} \times 8 \text{ [period]}}{0.47 \text{ [deg]} \times 4 \text{ [pole]}/2} = 255 \text{ [revolutions]}$
6-pole motor :	$\frac{30 \text{ [deg]} \times 8 \text{ [period]}}{0.47 \text{ [deg]} \times 6 \text{ [pole]}/2} = 170 \text{ [revolutions]}$
10-pole motor :	$\frac{30 \text{ [deg]} \times 8 \text{ [period]}}{0.47 \text{ [deg]} \times 10 \text{ [pole]}/2} = 102 \text{ [revolutions]}$

2. Setting of Various Parameters - continued

(10) Duty Slope Setting (SSU, SSD)

The speed linked slope can be set by applying a voltage divided by resistance from the V_{REG} to the SSU pin and the SSD pin. The SSU pin is set to the Spin up time, and the SSD pin is set to the Spin down time.

By applying a slope to the target rotational speed, it is possible to suppress inrush current flowing into the MOS-FET when a large torque change occurs immediately after startup or when the rotational speed command value changes due to PWM input Duty or DCIN voltage.

However, it is only a valid function for speed feedback mode (FBSEL = Low).

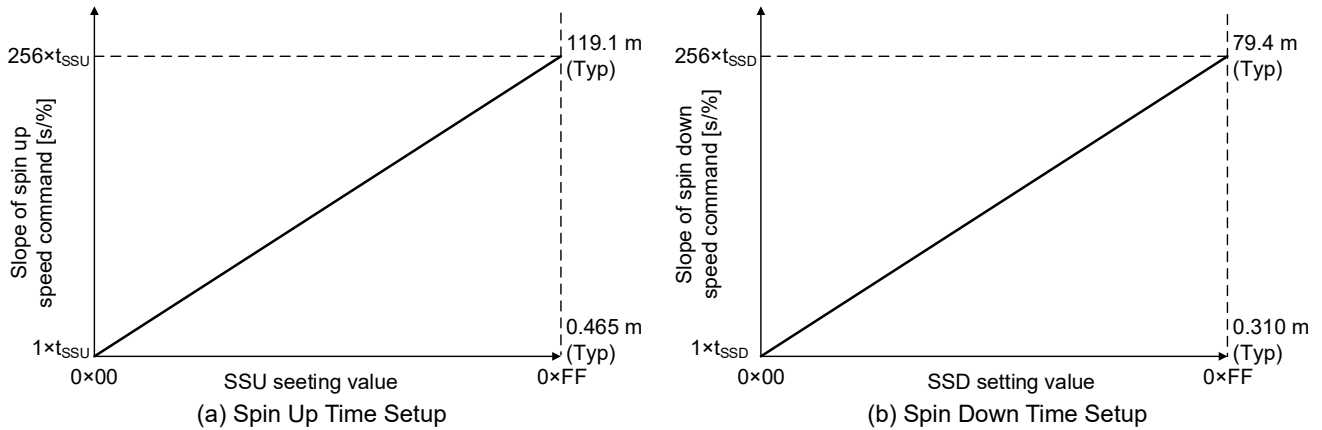


Figure 23. Spin Up/Down Time Setup

Example: When setting the slope of Spin up to 0.1 [s/%],

$$\text{SSU setting value} = \frac{0.1 \text{ [s/\%]}}{0.465 \text{ m [s/\%]}} = 215.1$$

Apply a voltage divided by resistance from the V_{REG} to the SSU pin with a resistance ratio of 215/256.

Also, when setting the slope at Spin down to 0.01 [s/%],

$$\text{SSD setting value} = \frac{0.01 \text{ [s/\%]}}{0.310 \text{ m [s/\%]}} = 32.3$$

Apply a voltage divided by resistance from the V_{REG} to the SSD pin with a resistance ratio of 33/256.

Next, the behavior of target rotational speed against time is shown in Figure 24 if Spin up time is set to 119.1 m [s/%] and Spin down time to 79.4 m [s/%].

If the rotational speed command value is input 10 % or more and spin up, soft start operates from 10.5 % of maximum rotational speed in the slope of SSU setup value. If 100 % of rotational speed command value is input at 95 %, soft down operates from 100 % of maximum rotational speed in the slope of SSD setup value.

If the rotational speed command value becomes 0 % at the PWM input or DCIN input while the motor is rotating, it will soft down due to the inclination of set value of the SSD setting, and the motor will stop.

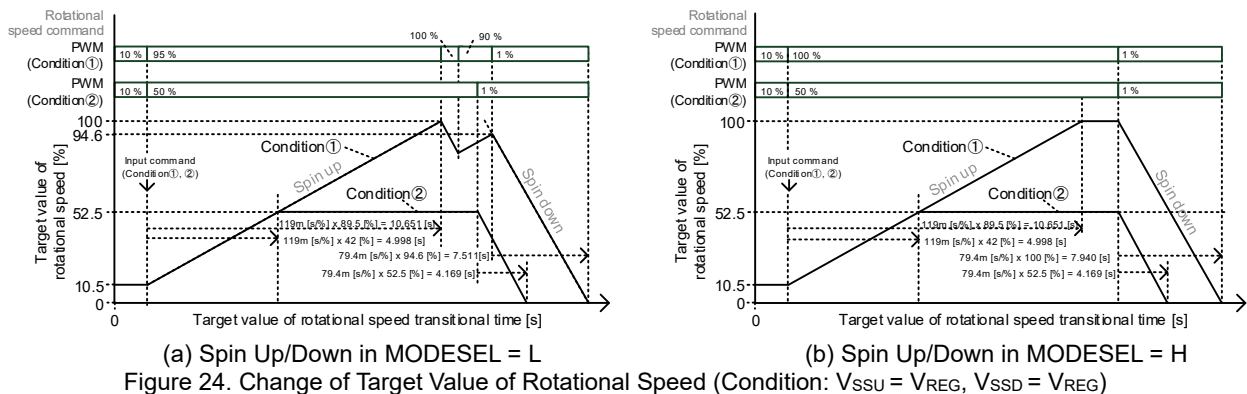


Figure 24. Change of Target Value of Rotational Speed (Condition: $V_{SSU} = V_{REG}$, $V_{SSD} = V_{REG}$)

2. Setting of Various Parameters – continued

(11) Motor Lock Protection Detection Time Setting (LCSET)

The lock detection time can be set by applying a voltage divided by resistance from the V_{REG} to the LCSET pin. It can be set from 1.68 s to 15.05 s with 256 levels of resolution (0.052 s step).

Please refer to “(27) Motor Lock Protection (MLP; Motor Lock Protection)” for details on lock protection operation.

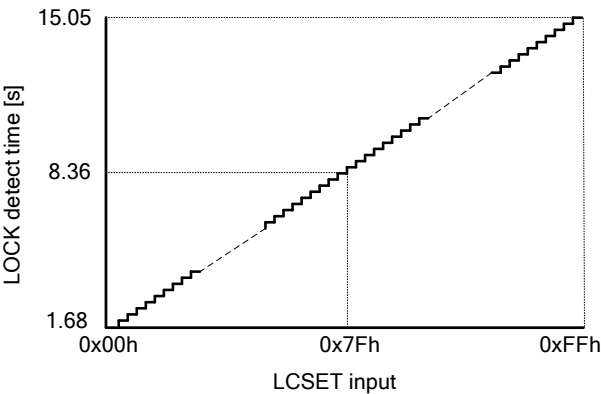


Figure 25. Setting the Motor Lock Protection Time

Functional Description – continued

3. Pin Function

(12) Control Mode Selection (FBSEL)

Between speed feedback mode and open control mode can be selected by the FBSEL pin.

In open control, the output operates according to the PWM input Duty (D_{PWM}) or DCIN voltage (V_{DCIN}).

	FBSEL Input Logic	
	Low: 0 V to $V_{REG} \times 0.2$	High: $V_{REG} \times 0.6$ to V_{REG}
Control mode	Speed Feedback	Open Control

The output TRQ Duty is calculated with the following formulas.

When operating with PWM:

$$TRQ\ Duty = D_{PWM} \times 100 \quad [\%]$$

When operating with DCIN:

$$TRQ\ Duty = \frac{V_{DCIN}}{V_{VREG}} \times 100 \quad [\%]$$

The A/D parameters and pin functions that can be set in open control mode are as follows. In this mode, the torque limit function that limit the maximum output duty and over current limit function are disabled.

Pin Name	Function
DCIN	Rotational speed command input
RREF	-
PROP	-
INTG	-
PCI	Lead angle control initial torque setup input
PCG	Lead angle control gain setup input
SSU	-
SSD	-
LCSET	Lock protection time setup input
MODESEL	-
FR	Forward/Reverse Selection
TDEAD	Dead Time Selection

3. Pin Function - Continued
(13) Input/Output Mode Selection (MODESEL)

Input/output profile during speed control can be selected by the MODESEL pin.
Please do not switch the input/output mode while the device is operating.

	MODESEL input logic	
	Low: 0 V to $V_{REG} \times 0.2$	High: $V_{REG} \times 0.6$ to V_{REG}
Output Mode (PWM Input)	I Mode	II Mode
Output Mode (DCIN Input)	-	III Mode

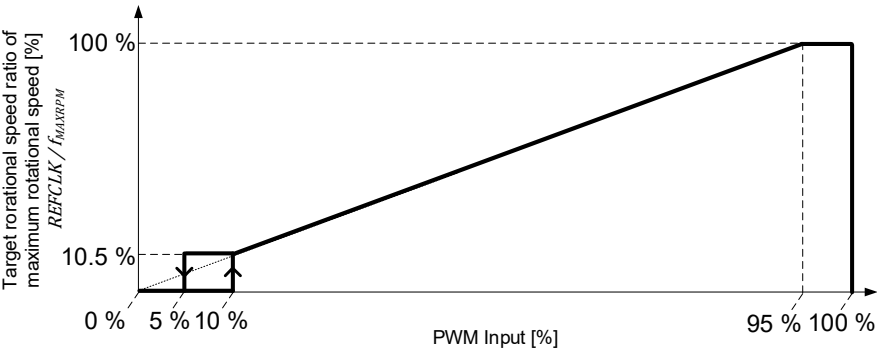


Figure 26. I Mode Target Rotational Speed vs PWM Input (Note 1)
(MODESEL = Low)

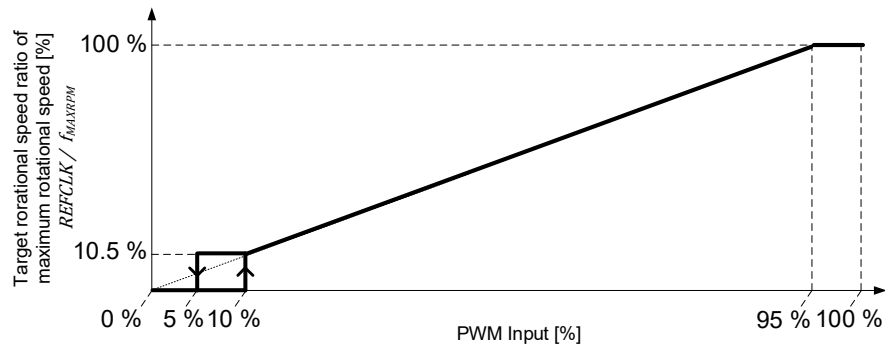


Figure 27. II Mode Target Rotational Speed vs PWM Input (Note 1)
(MODESEL = High)

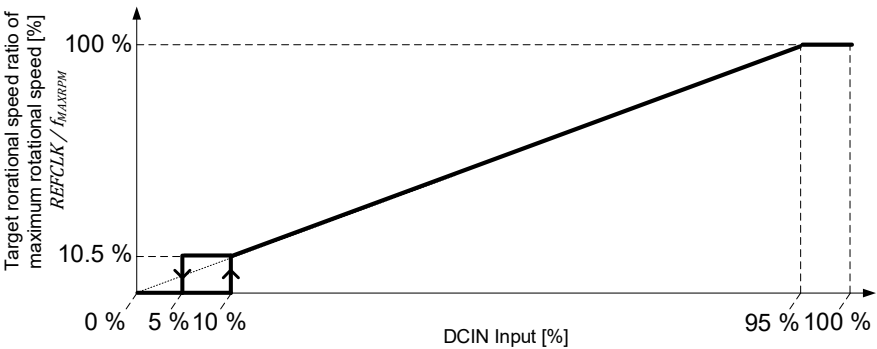


Figure 28. III. Mode Target Rotational Speed vs DCIN Input (Note 1)
(MODESEL = High)

(Note 1) The PWM input shows the pulse input Duty, and the DCIN input shows the ratio of the DCIN voltage to V_{REG} as a percentage.

3. Pin Function - Continued

(14) Forward/Reverse Selection (FR)

The direction of rotation can be selected by the FR pin.

If FR signal is switched during motor rotation, the load is applied on MOS-FET by inrush current. Consider allowable current of MOS-FET.

	FR Input Logic	
	Low: 0 V to $V_{REG} \times 0.2$	High: $V_{REG} \times 0.6$ to V_{REG}
Rotation mode	Reversing Rotation Mode (CCW)	Forward Rotation Mode (CW)

(15) Rotational Pulse Signal Output (FG)

The FG generates the W-phase signal comparator output of Hall signal.

(16) Dead Time Selection (TDEAD)

The TDEAD terminal allows you to select the dead time of the upper and lower gate drive outputs.

	TDEAD Input Logic	
	Low: 0 V to $V_{REG} \times 0.2$	High: $V_{REG} \times 0.6$ to V_{REG}
Output Dead Time	1.0 μ s (Typ)	0.5 μ s (Typ)

(17) Boost Voltage Output (VG)

A charge pump circuit to drive the external MOS-FET on the High side is built in.

Connect a 0.1 μ F capacitor between C_M and C_P. Also, connect a 0.1 μ F capacitor between VG-VCC as well. The VG voltage may drop, so attach the capacitor as close to the pin as possible.

(18) Reference Voltage Output (VREG)

The VREG pin (5.0 V Typ) is built-in for the power supply of the Hall sensor, the power supply of the resistor voltage of each set pin, and the pull-up of each pin.

Consider the maximum output current I_{VREG} when using. For stabilization, make sure to connect 1 μ F or more capacitor against GND.

If there is short failure against grounded capacitor or grounded by short between GND line and wire, the VREG pin exceeds the maximum output current. Consider to put limiting resistance, etc. if there is a grounded configuration.

(19) Oscillator Input/Output (XIN, XOUT)

Input a waveform with 10 MHz frequency into XIN.

If oscillating circuit is necessary; connect a feedback resistance and a ceramic resonator " CSTNE10M0G55A000R0 " between XIN and XOUT.

It can realize speed control according to oscillator accuracy.

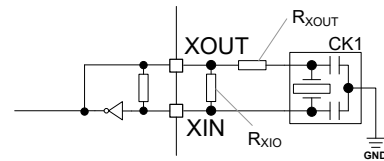


Figure 29. Example of Resonator Circuit Diagram

Functional Description – continued

4. Protection

(20) Protection Mode

The protection functions such as Over Voltage Protection (OVP), Thermal Shutdown (TSD), Hall Input Error (HALLERR), Under Voltage Lockout (UVLO), Over Current Protection (OCP), and Motor Lock Protection (MLP) are built. Additionally, Over Current Limit (OCL) is available as a function to limit torque to the motor. The operation of each function is as follows.

Protection Mode	Detection condition	Recovery condition	Gate Drive Output (D*H)	Gate Drive Output (D*L)	Charge Pump Output (C_P, C_M)	Output Priority
OVP	$30\text{ V} < V_{CC}$	$V_{CC} < 27\text{ V}$	Low	High	Hi-Z	1
TSD	$175\text{ }^{\circ}\text{C} < T_j$	$T_j < 150\text{ }^{\circ}\text{C}$	Hi-Z	Hi-Z	Hi-Z	2
HALLERR	Detect HHH/LLL	Normal Hall Input Logic	Hi-Z	Hi-Z	Hi-Z	2
UVLO	$5.5\text{ V} > V_{CC}$	$V_{CC} > 6\text{ V}$	Low	Low	PWM	3
OCP	$OCP < AMPO$	Off-Latch Release Sequence	Low	Low	PWM	3
MLP	Locked above LCSET Time	Off-Latch Release Sequence	Low	Low	PWM	3
OCL	$OCL < AMPO$	$OCL > AMPO$	Decrease Torque	Decrease Torque	PWM	-

In speed feedback mode (FBSEL = Low), the off-latch is released by applying a PWM = Low for 513 ms, after which the device recovers via PWM input. In contrast, in open control mode (FBSEL = High), the off-latch is released not by PWM input but by turning off the V_{REG} power supply. When the V_{REG} drops to 0 V, the IC enters a reset state and the off-latch is released. To ensure a reliable reset, maintain the 0 V condition for at least 1 ms. ^(Note 1)

(Note 1) Please note that the time it takes for the V_{REG} to drop to 0 V varies depending on the capacity of the VCC and VREG lines.

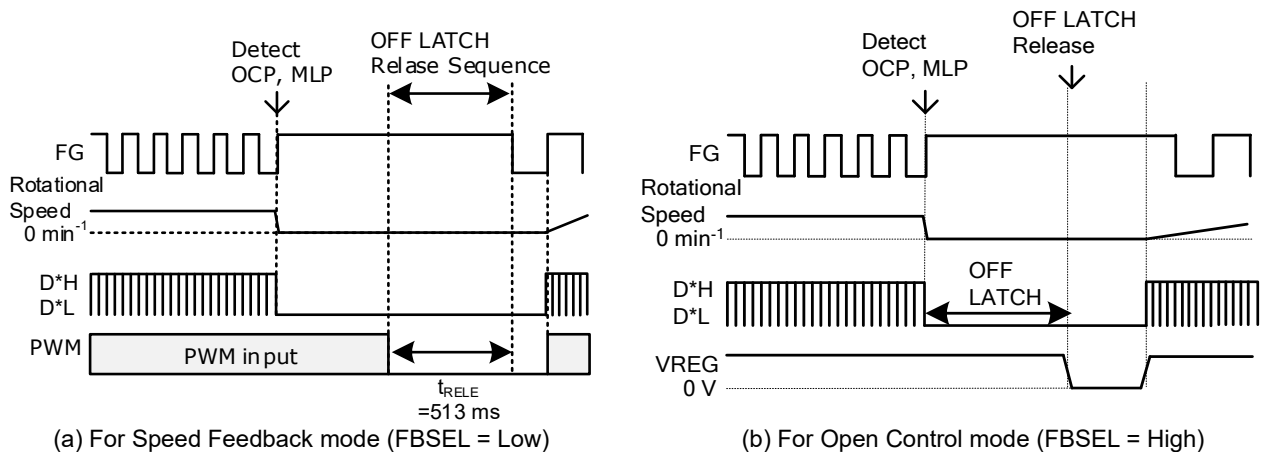


Figure 30. How to Release from Off-Latch Condition

4. Protection - Continued

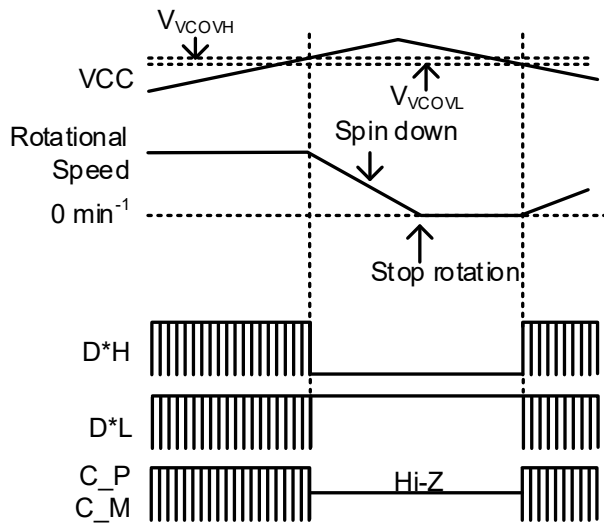
(21) Over Voltage Protection (OVP; Over Voltage Protection)

This is a protection function to prevent the motor from continuing to operate in case of over voltage.

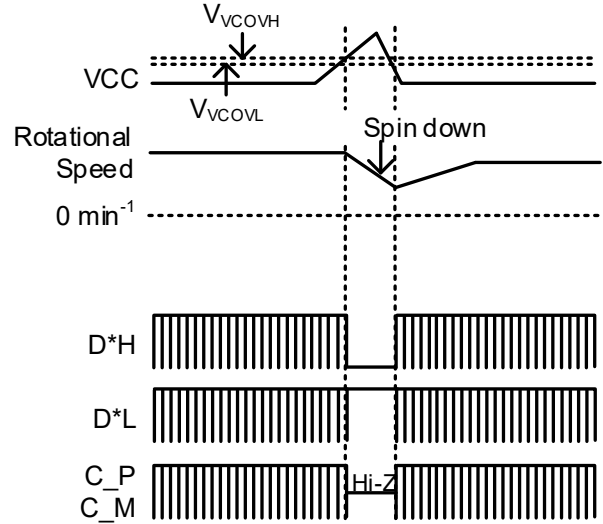
If the VCC supply voltage is increased and exceeds the specified voltage for over voltage protection detect voltage V_{VCOVH} (30 V Typ), the over voltage protection circuit is activated. At this time, the output stages of pre-driver High side are switched to Low, and Low side are switched to High. The charge pump output is switched to Hi-Z. If the VCC supply voltage is reduced and lower than the specified voltage for over voltage protection release voltage V_{VCOVL} (27 V Typ), the protection is released and return to normal operation.

Note that over voltage protection is a function that stops the pre-driver and charge pump outputs.

Make sure that the supply voltage will not to exceed the absolute maximum rating as the IC may be destroyed.



(a) Over Voltage Detection / Return Operation from Stop



(b) Over Voltage Detection / Return Operation from Rotation

Figure 31. Over Voltage Protection Operation

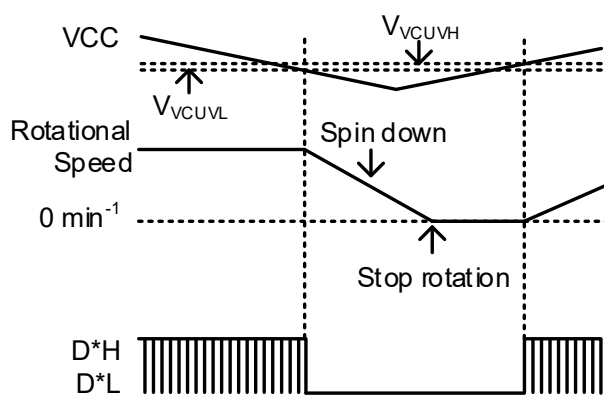
(22) Under Voltage Lockout (UVLO; Under Voltage LockOut)

This is a protection function to prevent the motor from continuing to operate in case of under voltage.

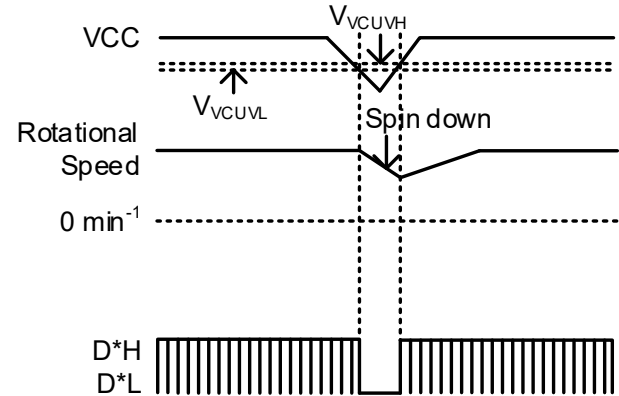
If the supply voltage is lower than the setup voltage (5.5 V Typ), the under voltage lockout protection circuit is activated.

At this time, both the high-side and low-side gate outputs are set to Low. If the supply voltage increases (6.0 V Typ), the protection is deactivated and it goes back to the normal operation.

Note that if the VCC power supply voltage falls below 4.5 V (minimum), the IC enters a reset state.



a) Under Voltage Detection / Return Operation from Stop



(b) Under Voltage Detection / Return Operation from Idling

Figure 32. Under Voltage Lockout Operation

4. Protection - Continued

(23) Hall Input Error (HALLERR; HALL Input Error)

This is a protection function to prevent the motor from continuing to operate in case of abnormal conditions of Hall input signals.

If a fault occurs in the hall element (or Hall IC) or in the circuitry around the Hall sensor, and the 3-phase logic of the Hall inputs HU, HV, and HW is detected as either LLL or HHH, the protection function is activated. At this time, both the high-side and low-side gate outputs is switched to Low, and the charge pump output is switched to Hi-Z. When the Hall input logic returns to normal, the protection is released and normal operation resumes.

(24) Thermal Shutdown (TSD; Thermal Shutdown)

This is a protective function to prevent malfunction and thermal breakdown due to thermal runaway.

If the junction temperature of driver IC increases and exceeds the specified temperature (175 °C Typ), the protection function is activated. At this time, both the high-side and low-side gate outputs are set to Low. The charge pump output is switched to Hi-Z. Once the junction temperature of the driver IC drops below 150 °C (Typ), the protection is deactivated for the normal operation.

The thermal shutdown circuit is to shutoff the driver IC from thermal runaway. The operation guaranteed temperature is exceeded when this circuit is activated. Please make sure to consider a thermal design with sufficient margin so that it is not used on the assumption of the activation of this circuit. The above set temperature is a guaranteed design value and no measurement with increasing the temperature was done.

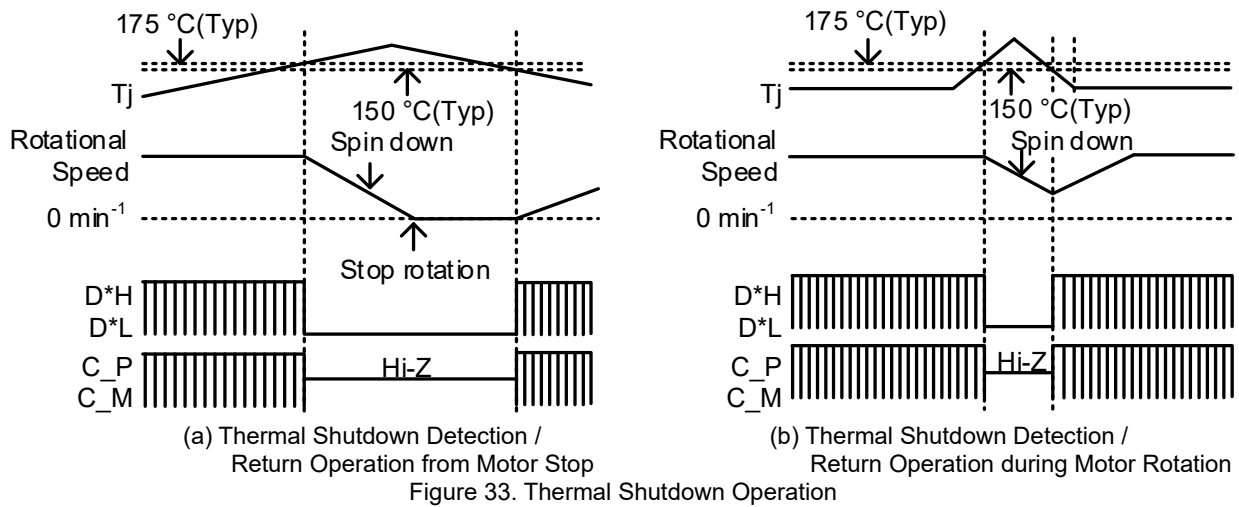


Figure 33. Thermal Shutdown Operation

4. Protection - Continued

(25) Over Current Protection (OCP; Over Current Protection)

This is a protective function to prevent large currents from flowing through the external MOS-FET.

An over current protection circuit and an over current limiting circuit can be configured with a low-resistance shunt resistor (R_{RNF} in Figure 34) for current detection which connected to the GND side of the external MOS-FET, an amplifier that amplifies the R_{RNF} voltage 10 times (Typ), and a comparator that compares with voltage between an amplifier output voltage (AMPO) and the voltage of the OCP and OCL pins.

If AMPO voltage exceeds the value set on the OCP pin due to generated voltage on R_{RNF} , the protection function is activated. At this time, both the high-side and low-side gate outputs are latched off to Low. In the case of the speed feedback mode (FBSEL = Low), the off latch is released by applying a PWM = Low for 513 ms and then returns to the PWM input, as shown below. On the other hand, in the case of an open control (FBSEL = High), the off latch is released by re-energizing the power, not via PWM input.

The filter is built in for the over current protection circuit to prevent malfunction. If the OCP comparator output is less than the noise mask time (10 μ s Typ), it is ignored (See Figure 35 (a)).

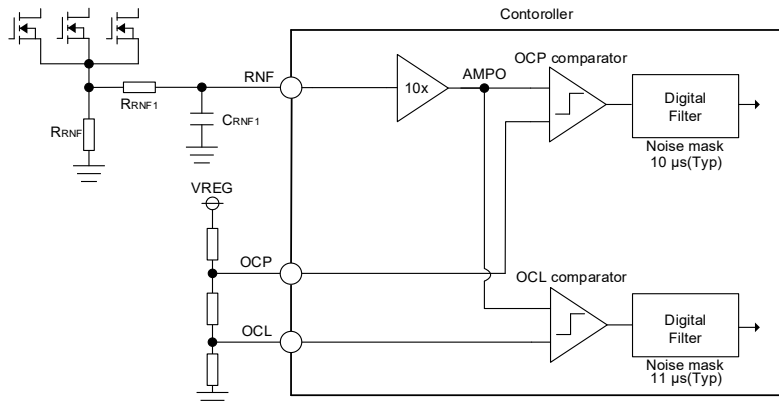


Figure 34. Over Current Protection Peripheral Circuit Diagram

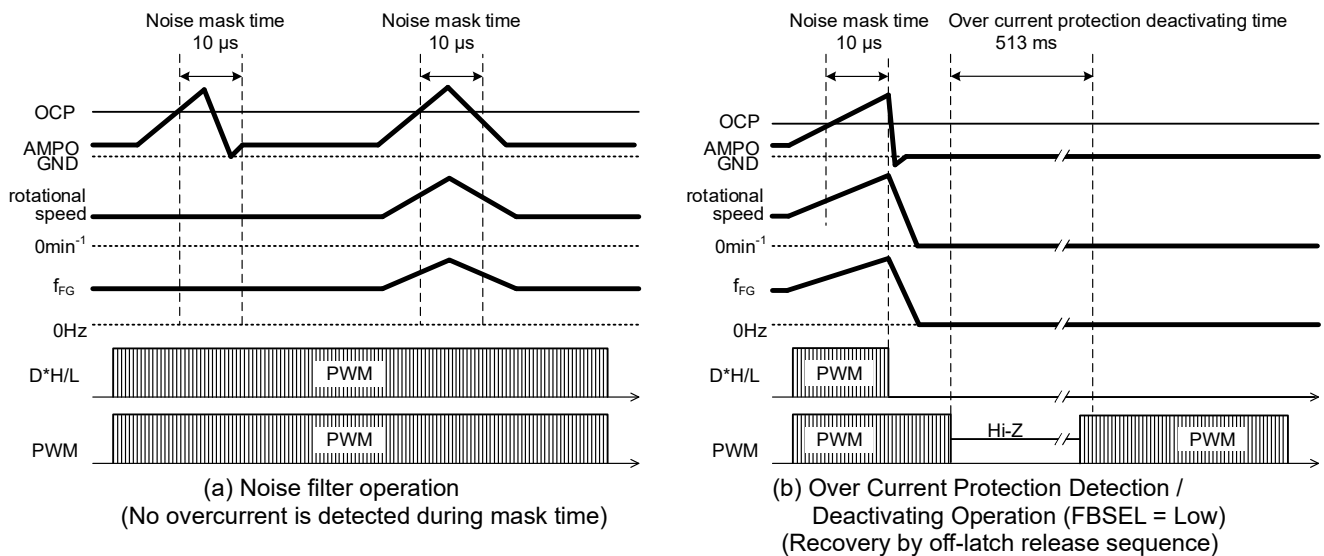


Figure 35. Over Current Protection Operation

If a malfunction occurs due to noise that exceeds the mask time, it is recommended to add an external RC filter (See Figure 34 for R_{RNF1} , C_{RNF1}) while reviewing the board pattern. In this case, the external filter will increase the delay time until the protection circuit starts to operate. Make sure not to exceed the area of safety operation (ASO) of the external output stage MOS-FET.

4. Protection - Continued

(26) Over Current Limit (OCL; Over Current Limit)

Same as over current protection, if AMPO voltage goes over the value set on the OCL pin due to generated voltage on R_{RNF} (Figure 34), over current limit function is activated to limit the torque to motor. The over current limit function reduces the internal torque signal to less than OCL voltage, speed control is disable while this function is active. Note that the rotational speed is changed if the supply voltage or load is changed.

The filter is built in for the over current limit circuit to prevent malfunction. OCL comparator output shorter than the noise mask time (11 μ s Typ) is ignored, as shown in Figure 36.

However, it is only a valid function for speed feedback mode (FBSEL = Low).

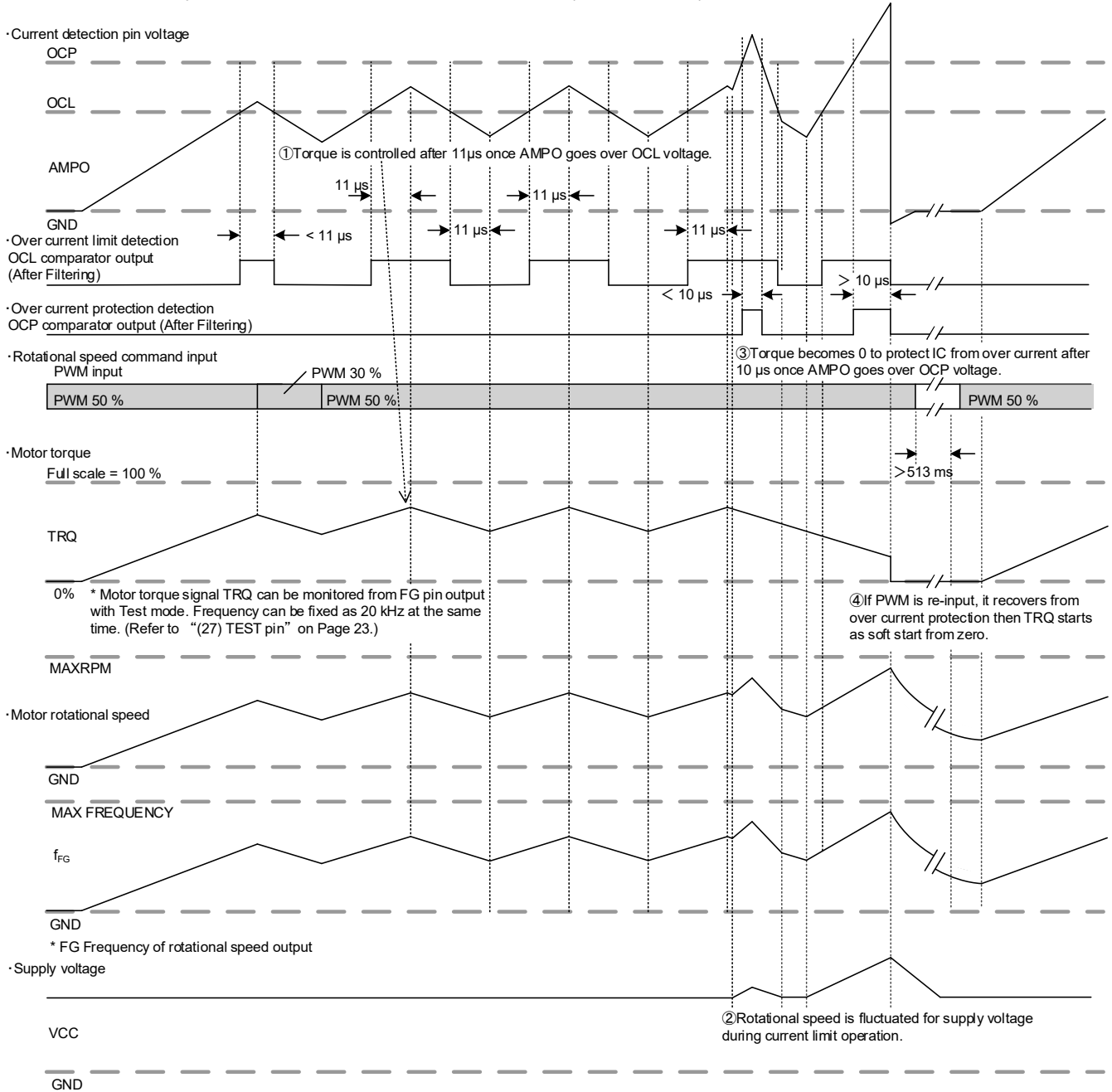


Figure 36. Over Current Limit Circuit Operation

4. Protection - Continued

(27) Motor Lock Protection (MLP; Motor Lock Protection)

This is a protection function to detect motor rotation abnormalities, such as motor locks, to prevent large currents from flowing to external MOS-FET.

If it detects that the Hall signal does not switch for the time set on the LCSET pin, the protection function is activated.

At this time, both the high-side and low-side gate outputs are latched off to Low. In the case of the speed feedback mode (FBSEL = Low), the off latch is released by applying a PWM = Low for 513 ms and then returns to the PWM input, as shown below. On the other hand, in the case of an open control (FBSEL = High), the off latch is released by re-energizing the power, not via PWM input.

In the case of the open control only, the lock protection becomes disabled when either the PWM input duty is 13 % or less, or the ratio of DCIN voltage to V_{REG} ($100 \times V_{DCIN}/V_{REG}$) is 13 % or less.

For LCSET settings, refer to “(11) Motor Lock Protection Detection Time Setting (LCSET)”.

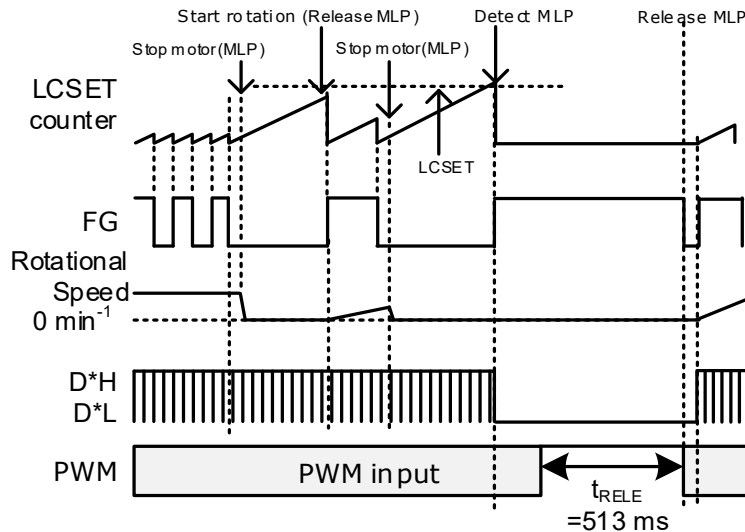


Figure 37. Lock Protection Operation (FBSEL = Low)

Functional Description – continued

5. Test Mode

(28) TEST Pins

The TEST1 and TEST2 pins are test pins with built-in pull-down resistor for shipping inspection. In order to prevent the transition to Test Mode due to noise, short with GND via resistor. When using it open, make sure that the pin voltage does not exceed the maximum low level input voltage ($V_{REG} \times 0.2$ V) so that it will not switch to Test Mode due to noise.

Also, only in the case of the speed feedback mode (FBSEL = Low), by setting TEST1 = GND and TEST2 = V_{REG} as a test mode, TRQ Duty can be monitored using FG Duty. TRQ Duty is output as the High Duty of DUH, which corresponds to the High Duty of the FG output.

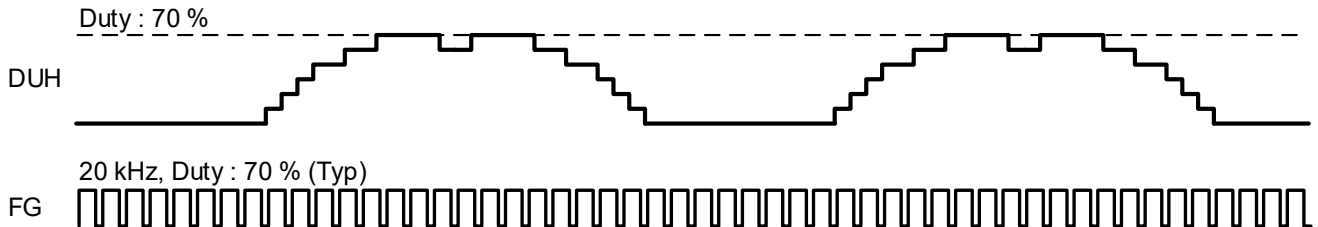


Figure 38. TRQ Duty Monitor

6. Reference Characteristics

(29) Boost Voltage Characteristics

Booster circuit is built in to drive High side N channel MOS-FET.

Boosted voltage characteristics changes according to conditions of load, voltage, temperature and element variation. Figure 39 is the characteristics of voltage and temperature without connecting load.

Considering loading conditions^(Note 1) and element variation, the Boosted Voltage V_G is:

$$V_G = 2 \times V_{CC} - 2.218 \text{ V}^{(Note 2)}$$

(Note 1) Measured value when 10000 pF capacitor is connected to the output as gate capacitance of external MOS-FET.

(Note 2) Measured value when $V_{CC} = 6.5$ V to 11.5 V. Use it as a reference.

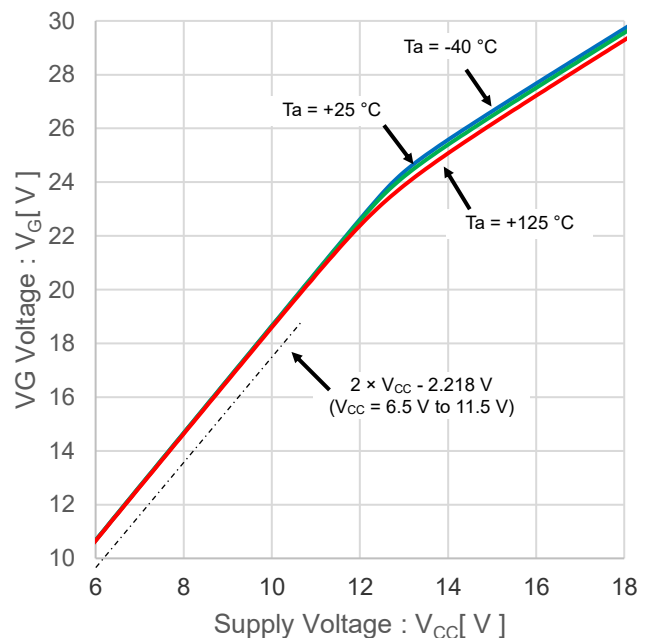


Figure 39. VG Voltage vs Supply Voltage
(Temperature and Voltage Characteristics of Boosted Voltage)

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Supply Voltage	VCC, VG	V _{CC} , V _G	50	V
Input Voltage (Note 1)	PWM, DCIN	V _{PWM} , V _{DCIN}	V _{REG}	V
	TDEAD, FR	V _{TDEAD} , V _{FR}	15	V
	MODESEL, PROP, FBSEL	V _{MODESEL} , V _{PROP} , V _{FBSEL}	50	V
	RNF, OCP, OCL, XIN	V _{RNF} , V _{OCP} , V _{OCL} , V _{XIN}	V _{REG}	V
	PCI, PCG, SSU, SSD, RREF, INTG, LCSET	V _{PCI} , V _{PCG} , V _{SSU} , V _{SSD} , V _{RREF} , V _{INTG} , V _{LCSET}		
	HU+, HU-, HV+, HV-, HW+, HW-	V _{HU+} , V _{HU-} , V _{HV+} , V _{HV-} , V _{HW+} , V _{HW-}		
	TEST1	V _{TEST1}	15	V
	TEST2	V _{TEST2}	50	V
Output Voltage	VREG	V _{REG}	6	V
	FG, XOUT	V _{FG} , V _{XOUT}	V _{REG}	V
	DUH, DVH, DWH	V _{DUH} , V _{DVH} , V _{DWH}	50	V
	VS_U, VS_V, VS_W, C_P	V _{VSU} , V _{VSV} , V _{VSW} , V _{CP}		V
	DUL, DVL, DWL, C_M	V _{DUL} , V _{DVL} , V _{DWL} , V _{CM}	15	V
Current Capability (Note 2)	VREG	I _{VREG}	-40	mA
	FG	I _{FG}	±500	μA
Storage Temperature Range		T _{stg}	-55 to +150	°C
Maximum Junction Temperature		T _{jmax}	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Configure the external circuit so that it does not exceed the VREG pin voltage, such as pulling it up to the VREG pin.

(Note 2) For the current item, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	6.5	12	18	V
Operating Temperature	T _{opr}	-40	+25	+125	°C

Thermal Resistance (Note 3)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 5)	2s2p (Note 6)	
VQFN48FBV070				
Junction to Ambient	θ _{JA}	94.1	29.9	°C/W
Junction to Top Characterization Parameter (Note 4)	Ψ _{JT}	8	8	°C/W

(Note 3) Based on JESD51-2A (Still-Air). (Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3. (Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt
Top		
Copper Pattern		Thickness
Footprints and Traces		70 μm

Layer Number of Measurement Board	Material	Board Size		Thermal Via ^(Note 7)	
				Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt		1.20 mm	Φ0.30 mm
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 7) This thermal via connect with the copper pattern of layers 1, 2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics 1 (Unless otherwise specified $V_{CC} = 6.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, $0.1 \text{ }\mu\text{F}$ between C_P to C_M , $0.1 \text{ }\mu\text{F}$ between V_G to V_{CC} , $V_{S_U} = V_{S_V} = V_{S_W} = \text{GND}$, $f_{XIN} = 10 \text{ MHz}$)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[General]						
Circuit Current	I _{CC}	-	18	35	mA	V _{DCIN} = 2.5 V, V _{PWM} = 0 V
VREG Voltage	V _{REG}	4.8	5.0	5.2	V	I _{VREG} = -40 mA
Boosted Voltage 1	V _{G1}	2 × V _{CC} - 2.0	2 × V _{CC} - 1.0	2 × V _{CC}	V	V _{CC} = 6.5 V to 11.5 V, f _{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage 2	V _{G2}	V _{CC} + 9.0	V _{CC} + 11.5	V _{CC} + 13.0	V	V _{CC} = 11.5 V to 18.0 V f _{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage Load Fluctuation	V _{G3}	-	0.8	1.3	V	I _{VG} = -5 mA, V _{CC} = 6.5 V to 11.5 V, f _{PWM} = 625 Hz (Duty = 1 %)
Boosted Voltage Load Fluctuation	V _{G4}	-	0.6	1.0	V	I _{VG} = -5 mA, V _{CC} = 11.5 V to 18.0 V, f _{PWM} = 625 Hz (Duty = 1 %)
Switching Frequency for Voltage Boost	f _{CP}	250.0	312.5	375.0	kHz	
[A/D Converter]						
ADC Cycle	t _{ADC}	8.1	9.0	9.9	ms	V _{DCIN} , V _{PCI} , V _{PCG} , V _{SSU} , V _{SSD} , V _{INTG} , V _{PROP} , V _{RREF} , V _{LCSET} is updated with t _{ADC} cycle
[HALL Input]						
Input Bias Current	I _{HALL}	-10	0	+10	μA	
Input Amplitude Voltage	V _{HALLMIN}	35	-	-	mVpp	
Common-mode Input Voltage Range	V _{HALLCM}	0	-	V _{REG} - 1.2	V	
[PWM Input]						
High Level Input Voltage	V _{PWMH}	V _{REG} × 0.8	-	V _{REG}	V	
Low Level Input Voltage	V _{PWML}	0	-	V _{REG} × 0.4	V	
High Level Input Current	I _{PWMH}	-	50	100	μA	V _{PWM} = 5 V
Low Level Input Current	I _{PWML}	-20	0	+20	μA	V _{PWM} = 0 V
Pin Open Detect Time	t _{STB}	-	513	530	ms	V _{PWM} = V _{REG} → Open
Pin Open Release Time	t _{PWM}	-	-	53	ms	V _{PWM} = Open → V _{REG}
Off-Latch Release Time	t _{RELE}	-	513	530	ms	V _{PWM} = 0 V, Open
[DCIN Input]						
Input Voltage Setup Range	V _{DCRANGE}	0	-	V _{REG}	V	
High Level Input Current	I _{DCINH}	-	50	100	μA	V _{DCIN} = 5 V
Low Level Input Current	I _{DCINL}	-20	0	+20	μA	V _{DCIN} = 0 V
[Rotation Speed Command] ^(Note 1)						
Minimum Rotation Speed Command ON Duty	D _{MINON}	8	10	12	%	V _{MODESEL} = Low, High
Minimum Rotation Speed Command OFF Duty	D _{MINOFF}	3	5	7	%	V _{MODESEL} = Low, High
Hysteresis Duty	D _{HYS}	3	5	7	%	V _{MODESEL} = Low, High
Maximum Rotation Speed Command OFF Duty	D _{MAXOFF}	98	-	100	%	V _{MODESEL} = Low, when PWM input
[Speed Control]						
Maximum Speed Setting Accuracy	ACC _{MAX}	-2.65	-	+2.65	%	

For the current parameters, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) If a rotational speed command in DCIN is input, a ratio against the V_{REG} is shown.

Electrical Characteristics 2 (Unless otherwise specified $V_{CC} = 6.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, $0.1 \text{ }\mu\text{F}$ between C_P to C_M , $0.1 \text{ }\mu\text{F}$ between V_G to V_{CC} , $V_{S_U} = V_{S_V} = V_{S_W} = \text{GND}$, $f_{XIN} = 10 \text{ MHz}$)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Selection Input : FR, MODESEL, TDEAD, FBSEL]						
High Level Input Voltage	V _{INH}	V _{REG} × 0.60	-	V _{REG}	V	
Low Level Input Voltage	V _{INL}	0	-	V _{REG} × 0.20	V	
High Level Input Current	I _{INH}	25	50	100	μA	V _{IN} = 5 V
Low Level Input Current	I _{INL}	-10	0	+10	μA	V _{IN} = 0 V
[FG Output]						
High Level Output Voltage	V _{FGH}	4.0	-	-	V	I _{FG} = -500 μA
Low Level Output Voltage	V _{FGL}	-	-	0.3	V	I _{FG} = 500 μA
High Output Leak Current	I _{LKFGH}	-10	-	-	μA	V _{FG} = 0 V
Low Output Leak Current	I _{LKFGL}	-	-	10	μA	V _{FG} = 5 V
[XOUT Output]						
XOUT High Voltage	V _{XOH}	V _{REG} - 1.0	V _{REG} - 0.2	V _{REG}	V	V _{XIN} = 0 V, I _{XOUT} = -1 mA
XOUT Low Voltage	V _{XOL}	0.0	0.3	0.5	V	V _{XIN} = 5 V, I _{XOUT} = 1 mA
[Duty Slope Setting Input : SSU, SSD]						
Rotation Command Rise Time (Note 1)	t _{SSU}	-	0.465	-	ms	V _{SSU} = GND, V _{RREF} = V _{REG}
Rotation Command Fall Time (Note 1)	t _{SSD}	-	0.310	-	ms	V _{SSD} = GND, V _{RREF} = V _{REG}
[Lead Angle Control : PCG, PCI]						
Lead Angle Gain Setup (Note 2)	G _{PCG}	14	15	16	°	V _{PCG} = V _{REG} /4, V _{PCI} = GND, f _{PWM} = 625 Hz (Duty = 50 %), TRQ Duty = 50 %
Lead Angle Initial Torque Setup	T _{PCI}	46	50	54	%	V _{PCI} = V _{REG} /2, V _{PCG} = V _{REG} /2
Maximum Lead Angle	P _{MAX}	29	30	31	°	V _{PCG} = V _{PWM} = V _{REG} , V _{PCI} = GND

For the current parameters, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) The time required for rotational command to fluctuate 1 % is defined.

In addition, the reference value is a design value that has been evaluated and confirmed for the workmanship, and is not inspected for shipment.

(Note 2) The reference value is a design value that has been evaluated and confirmed for the workmanship, and is not inspected for shipment.

Electrical Characteristics 3 (Unless otherwise specified $V_{CC} = 6.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, $0.1 \text{ }\mu\text{F}$ between C_P to C_M , $0.1 \text{ }\mu\text{F}$ between V_G to V_{CC} , $V_{S_U} = V_{S_V} = V_{S_W} = \text{GND}$, $f_{XIN} = 10 \text{ MHz}$)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Pre-driver Output] <i>(Note 1)</i>						
D*H/D*L Output Oscillating Frequency	f _{OSC}	18	20	22	kHz	f _{XOUT} = 10 MHz
D*H High Voltage1	V _{OUTH1}	27.0	-	31.0	V	V _{CC} = 18.0 V
D*H Low Voltage1	V _{OUTL1}	-	0	0.2	V	V _{CC} = 18.0 V
D*L High Voltage1	V _{OUTLH1}	9.0	-	13.0	V	V _{CC} = 18.0 V
D*L Low Voltage1	V _{OUTLL1}	-	0	0.2	V	V _{CC} = 18.0 V
D*H High Voltage2	V _{OUTH2}	11.0	-	13.0	V	V _{CC} = 6.5 V
D*H Low Voltage2	V _{OUTL2}	-	0	0.2	V	V _{CC} = 6.5 V
D*L High Voltage2	V _{OUTLH2}	4.5	-	7.0	V	V _{CC} = 6.5 V
D*L Low Voltage2	V _{OUTLL2}	-	0	0.2	V	V _{CC} = 6.5 V
D*H Slew Rate Rising 1	V _{OHUSR1}	10	-	55	V/μs	V _{CC} = 18.0 V
D*H Slew Rate Falling 1	V _{OHDSR1}	30	-	120	V/μs	V _{CC} = 18.0 V
D*L Slew Rate Rising 1	V _{OLUSR1}	2	-	40	V/μs	V _{CC} = 18.0 V
D*L Slew Rate Falling 1	V _{OLDSR1}	8	-	85	V/μs	V _{CC} = 18.0 V
D*H Slew Rate Rising 2	V _{OHUSR2}	6	-	45	V/μs	V _{CC} = 6.5 V
D*H Slew Rate Falling 2	V _{OHDSR2}	6	-	70	V/μs	V _{CC} = 6.5 V
D*L Slew Rate Rising 2	V _{OLUSR2}	1	-	10	V/μs	V _{CC} = 6.5 V
D*L Slew Rate Falling 2	V _{OLDSR2}	6	-	55	V/μs	V _{CC} = 6.5 V
Diode Voltage Between VS_U / VS_V / VS_W to GND	V _{DI}	-1.35	-0.80	-0.40	V	I _{SINK} = -50 mA
D*H Output Upper Side ON Resistance	R _{OHPON}	-	9	18	Ω	I _o = -20mA
D*H Output Lower Side ON Resistance	R _{OHNON}	-	4	8	Ω	I _o = +20mA
D*L Output Upper Side ON Resistance	R _{OLPON}	-	6	12	Ω	I _o = -20mA
D*L Output Lower Side ON Resistance	R _{OLNON}	-	1	2	Ω	I _o = +20mA
[Output Dead Time] <i>(Note 2)</i>						
Dead Time 1	t _{DT1}	0.55	1.00	1.45	μs	V _{TDEAD} = Low
Dead Time 2	t _{DT2}	0.05	0.50	0.95	μs	V _{TDEAD} = High

For the current parameters, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

(Note 1) Slew rate parameters are the rated value when 10000 pF capacitor is connected to output as a gate capacity of external MOS-FET.

(Note 2) Pull down DUH and DUL at $10 \text{ k}\Omega$ to specify the time that the output changes from 10% to 90% or from 90% to 10% .

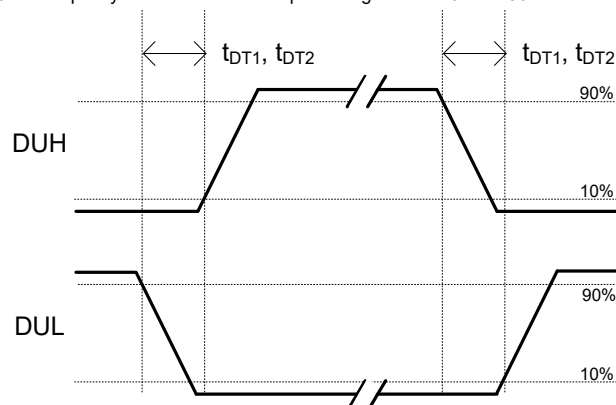


Figure 40. Dead Time Limit

Electrical Characteristics 4 (Unless otherwise specified: $V_{CC} = 6.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^{\circ}\text{C}$ to $+150 \text{ }^{\circ}\text{C}$, $0.1 \text{ }\mu\text{F}$ between C_P to C_M , $0.1 \text{ }\mu\text{F}$ between V_G to V_{CC} , $V_{S_U} = V_{S_V} = V_{S_W} = \text{GND}$, $f_{XIN} = 10 \text{ MHz}$)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
[Over Voltage Protection]						
OVP Detect Voltage	V _{VCOVH}	25.9	30.0	34.1	V	
OVP Release Voltage	V _{VCOVL}	23.4	27.0	30.6	V	
OVP Hysteresis Voltage	V _{VCOVHYS}	1.5	3.0	4.5	V	
[Under Voltage Lockout]						
UVLO Release Voltage	V _{VCUVH}	5.5	6.0	6.5	V	
UVLO Detect Voltage	V _{VCUVL}	5.0	5.5	6.0	V	
UVLO Hysteresis Voltage	V _{VCUVHYS}	0.3	0.5	0.7	V	
[Over Current Protection]						
Input Voltage Setup Range	V _{OCPRNG}	1.0	-	3.5	V	
Over Current Protection Detect Voltage	V _{RNF1}	V _{OCP} × 0.084	V _{OCP} × 0.100	V _{OCP} × 0.123	V	V _{RNF} = Sweep, 1.0 V ≤ V _{OCP} ≤ 3.5 V
OCP Detect Time	t _{OCPON}	5	10	35	µs	
[Over Current Limit]						
Input Voltage Setup Range	V _{OCLRNG}	1.0	-	3.5	V	
Over Current Limit Detect Voltage	V _{RNF2}	V _{OCL} × 0.084	V _{OCL} × 0.100	V _{OCL} × 0.123	V	V _{RNF} = Sweep, 1.0 V ≤ V _{OCL} ≤ 3.5 V
OCL Detect Time	t _{OCLON}	5	11	35	µs	
OCL Release Time	t _{OCCLOFF}	5	11	35	µs	

For the current parameters, the current inflow into the IC is indicated as a positive notation, and the current outflow from the IC as a negative notation.

Typical Performance Curves

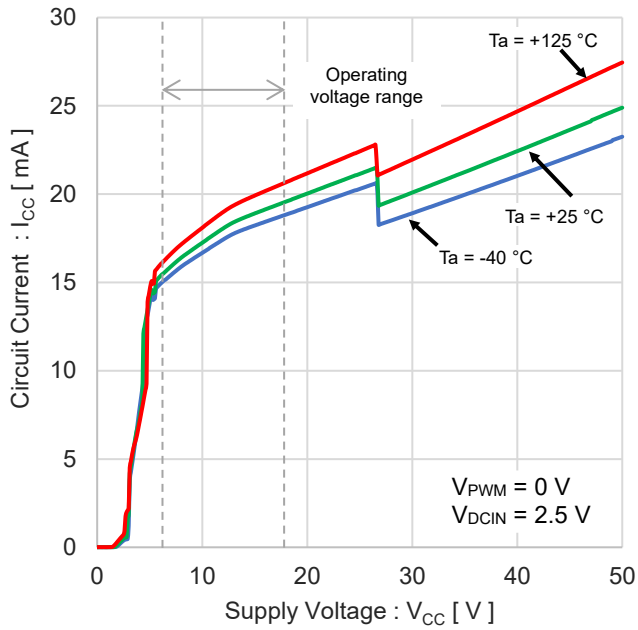


Figure 41. Circuit Current vs Supply Voltage (Circuit Current)

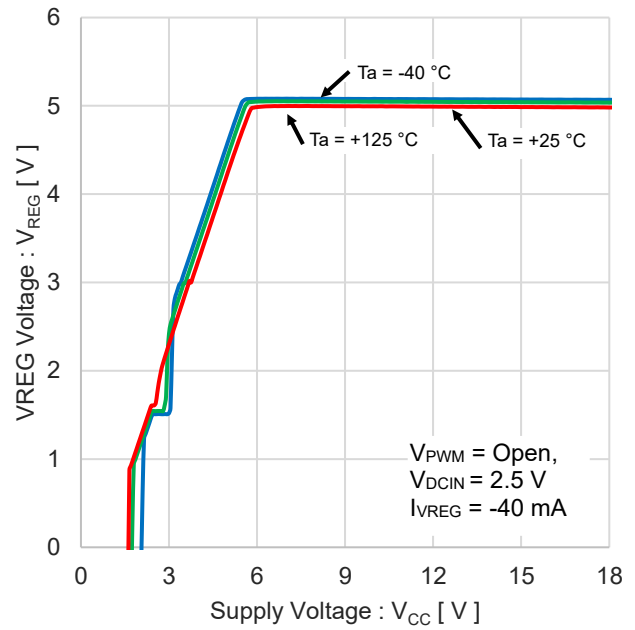


Figure 42. VREG Voltage vs Supply Voltage (VREG Voltage)

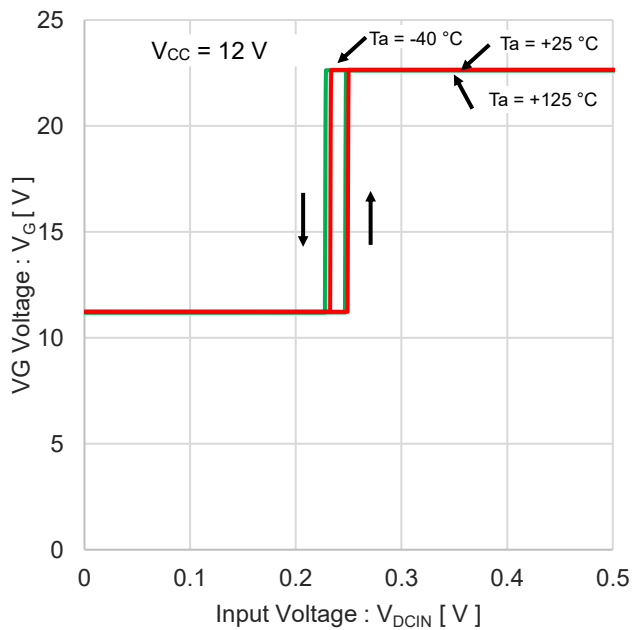


Figure 43. VG Voltage vs DCIN Voltage at Speed Feedback (The DCIN Voltage at Speed Feedback / VG Voltage)

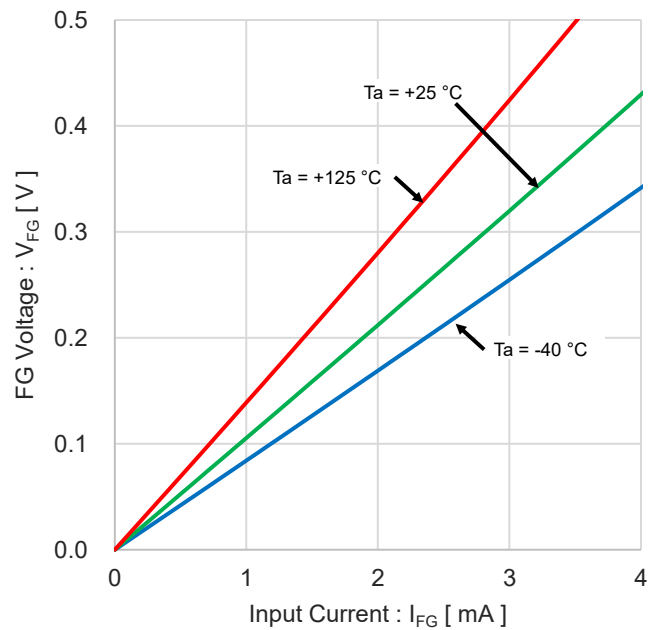


Figure 44. FG Voltage vs Input Current (The FG Pin Low Level Output Voltage)

Typical Performance Curves - Continued

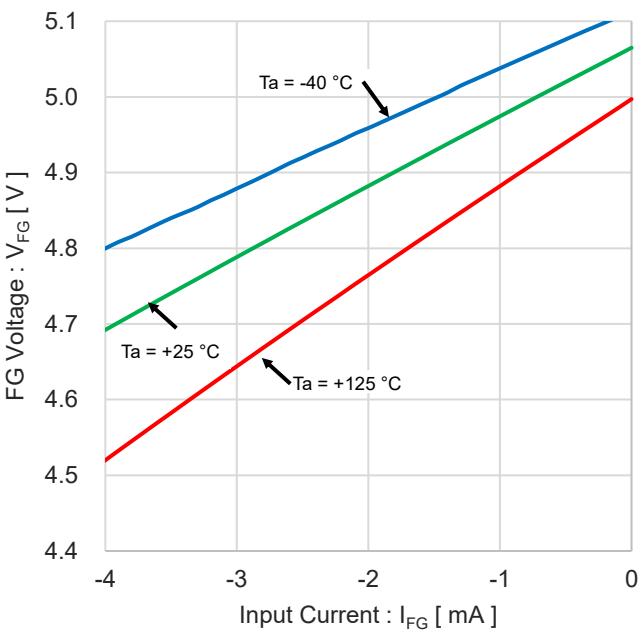


Figure 45. FG Voltage vs Input Current
(The FG Pin High Level Output Voltage)

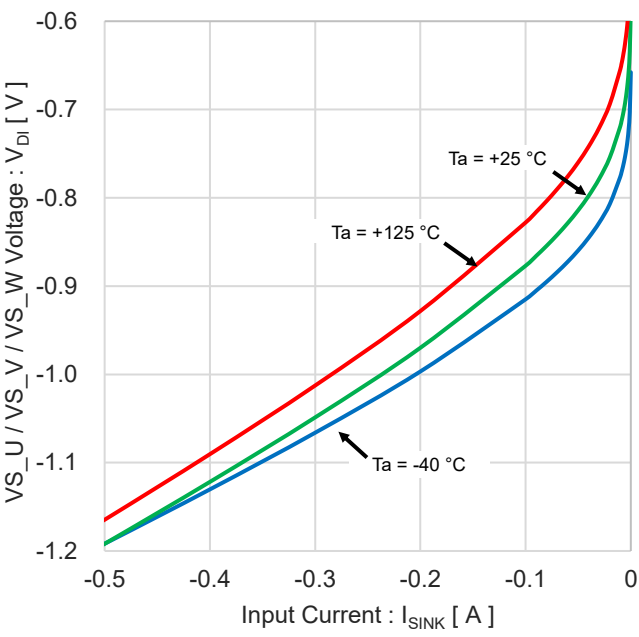
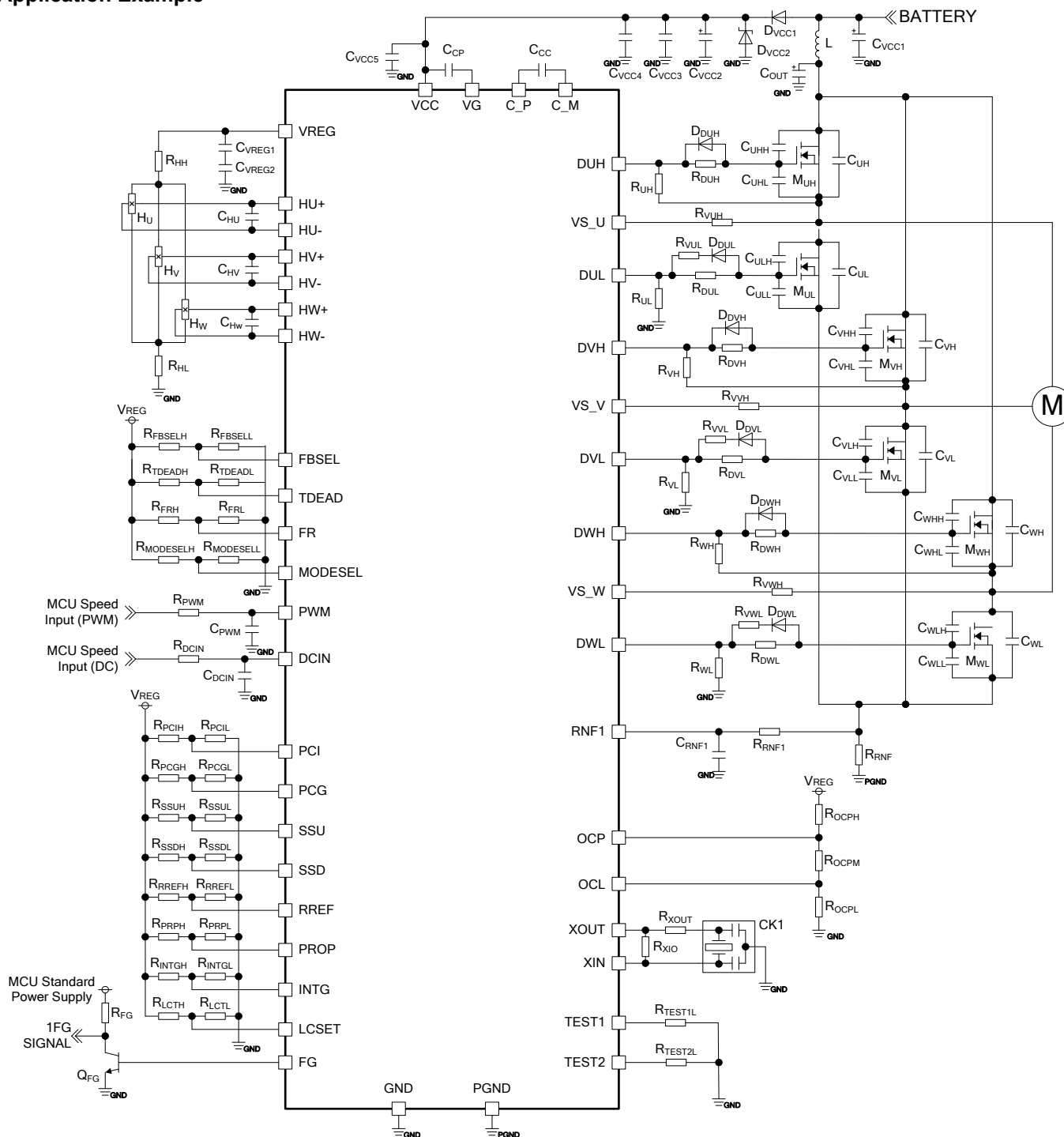


Figure 46. VS_U / VS_V / VS_W Voltage vs Input Current
(Diode Voltage between VS_U / VS_V / VS_W and GND)



Application Designing Notes

1. Absolute Maximum Ratings

While careful attention is paid to quality control for this product, an excess in the absolute maximum ratings such as supply voltage and voltage range of operating conditions may damage the IC, thus making it impossible to identify the breaking mode, such as a short circuit or an open circuit. In cases where the IC is expected to be used in a special mode in which it may exceed the absolute maximum ratings, consider taking physical safety measures such as using a fuse.

2. GND Potential

Depending on the heat generation conditions, supply voltage, motor used, etc. of this IC, problems such as malfunction may occur if the potential of output pin is large and swings to a potential below GND. In that case, take measures to prevent such failure by adding Schottky diode between the output and GND. Make sure to keep the potential of the GND pin at the minimum potential in any operating conditions.

3. Back Electromotive Force

The back electromotive force may be changed due to the operating condition, environment and characteristics of each motor. Make sure to thoroughly check that the IC operation is not affected by the back electromotive force.

4. GND Wiring

The connecting destinations of PGND and GND of each component are shown as recommendations. Pay thorough attention when wiring as high current flows into PGND.

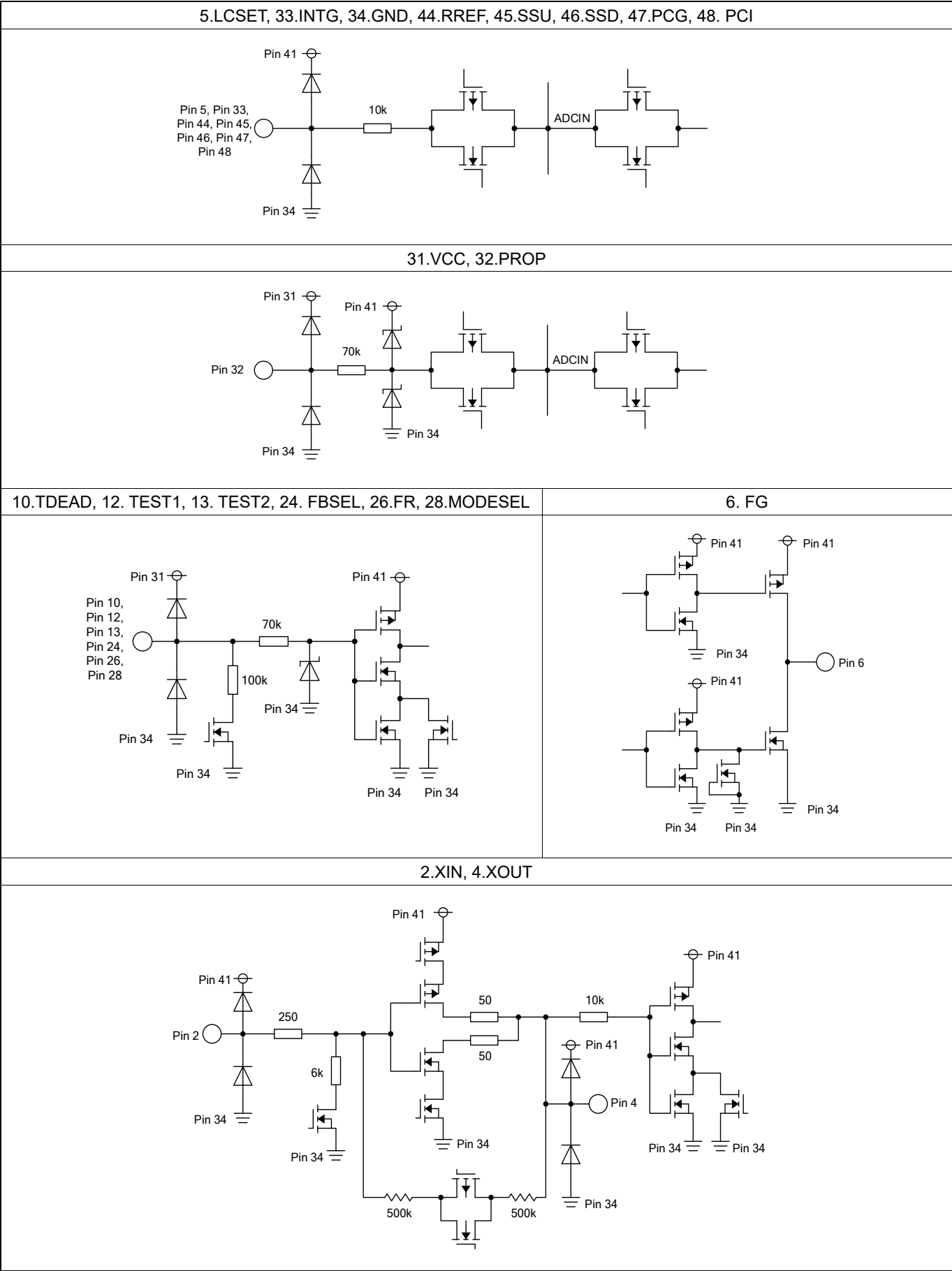
5. TDEAD, FBSEL, FR, MODESEL

The TDEAD, the FBSEL, the FR, and the MODESEL pins are each connected to GND with 100 k Ω . When connecting these to the VREG pin, set the resistance value to 10 k Ω to 100 k Ω .

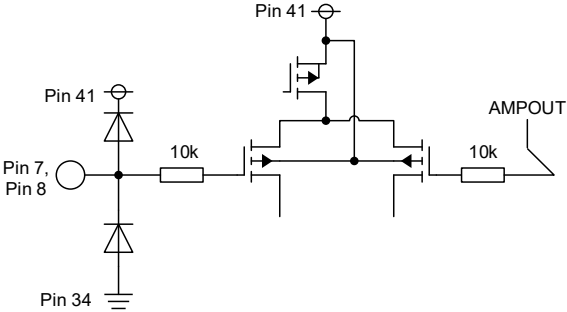
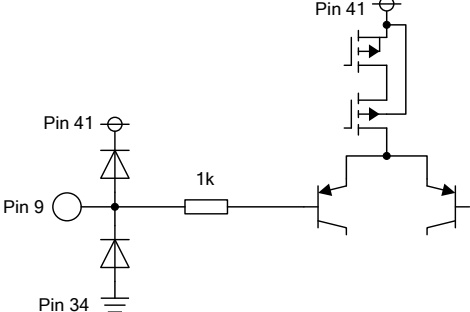
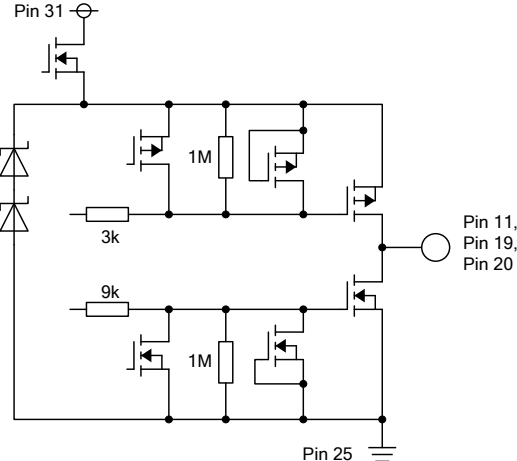
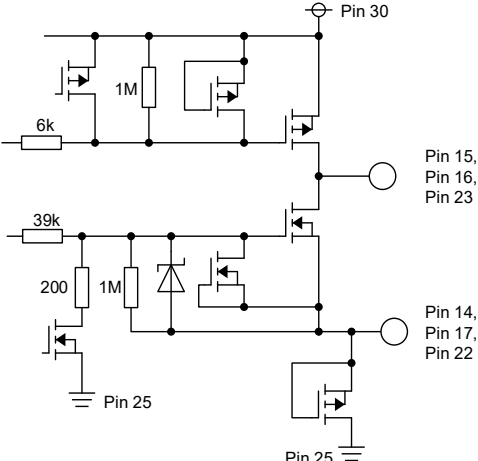
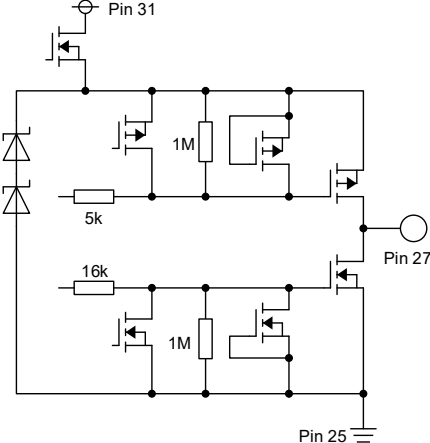
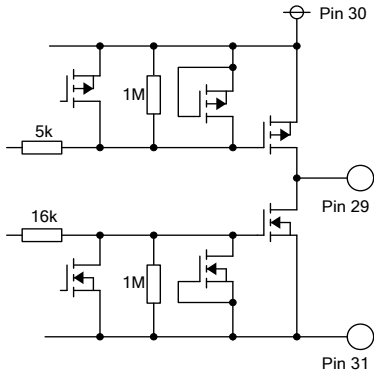
6. Thermal Design

If the product is used in a temperature that exceeds the maximum junction temperature, the original properties of the IC will deteriorate due to the rise in chip temperature. If the maximum junction temperature described in Absolute Maximum Ratings of this specifications is exceeded, take measures such as increasing the board size, increasing the area of copper foil for heat dissipation, and using a heat dissipation plate to avoid going over the maximum junction temperature.

I/O Equivalence Circuit (Typical Values of Resistance and Capacitance)



I/O Equivalence Circuit – continued

7.OCP, 8.OCL 	9. RNF 
11.DWL, 19.DVL, 20.DUL, 25. PGND 	14.VS_W, 15.DWH, 16.DVH, 17.VS_V, 22.VS_U, 23.DUH 
27.C_M 	29. C_P, 30.VG 

I/O Equivalence Circuit – continued

35.HU+, 36. HU-, 37. HV+, 38. HV-, 39. HW+, 40. HW-	41.VREG
42. PWM	43.DCIN

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

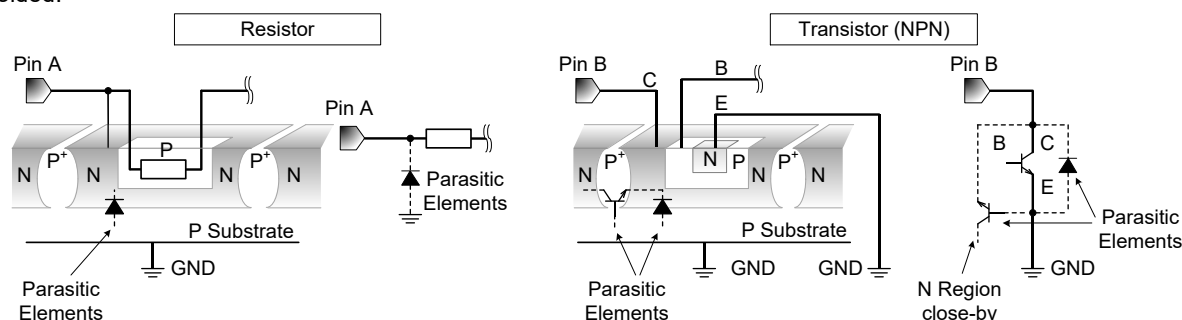


Figure 48. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

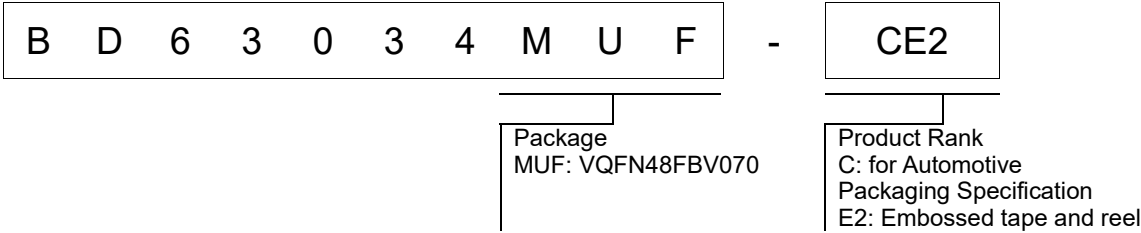
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

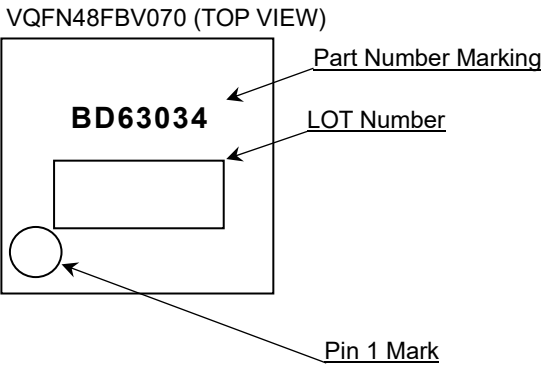
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

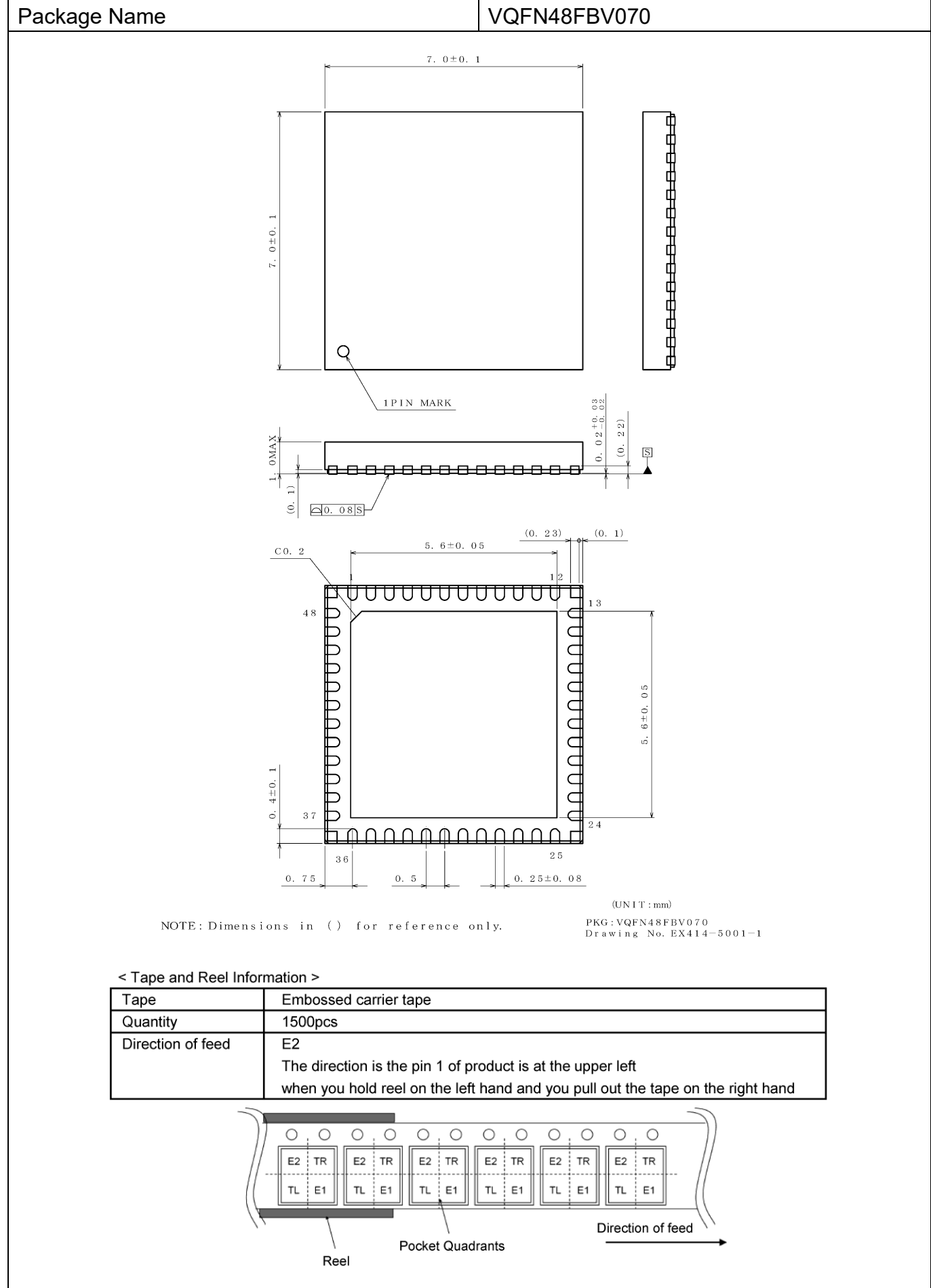
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Contents
15.Apr.2026	001	New Create

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
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 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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