Datasheet

Gate Driver for Mobility and Power Tool

TriC3™ 4.5 V to 60 V, Three-phase Brushless DC Motor Gate Driver

BD67871MWV-Z

General Description

BD67871MWV-Z is mounted an Innovative Active Gate Drive (TriC3™) which suppresses EMI and reduces heat generation of MOSFET power devices in motor drive systems. TriC3™ achieves these functions by monitoring various voltages around the MOSFET power device and using this voltages information to intelligently control the gate drive current of the MOSFET power device.
It is a gate driver IC designed for three-phase brushless DC motor applications. It can drive three half-bridges consisting of six N-Channel power MOSFETs up to 60 V. It has synchronous rectification function during bootstrap capacitor charging for efficiency.
Despite the TriC3™ being a type of constant-current drive, it enables 100 % PWM Duty Cycle and high-impedance by trickle charge pumping.

Features

- Innovation Active Gate Drive (TriC3™)
  - Multi Level Gate Drive Current Control
  - Real Time Gate Current Control Based on Information Sensed from the Output State
  - Dead Time Adjustment Control
- 60 V Three-phase Brushless DC Motor Gate Driver
  - Wide 4.5 V to 60 V Input Voltage Range
- Bootstrap based Gate Driver Architecture
  - Synchronous Rectification Function during Bootstrap Capacitor Charging
  - Bootstrap Gate Driver with Current Source Circuit for 100 % Duty Cycle Operation and High-impedance (Hi-Z) State
- Super Low I_{VCCQ} (< 1 µA at Sleep Mode)
- Supports 3.3 V, and 5 V Logic Inputs
- Supports Negative Transients up to -5 V on *_SH
- Supports IN/IN, and EN/IN Mode by UART
- Compact QFN Packages and Footprints
- UART Communication Protocol
- TriC3™ Base Current can be selected as External Resistor or Internal Constant Current
- Gate Driver Power Supply (V_{REG}) has LDO and Charge Pump Functions
- SHUNT pin allows Current Detection with External Resistors
- Integrated Protection Features
  - V_{CC} UVLO Protection
  - Bootstrap ($V_{*\_BST-*\_SH}$) UVLO Protection
  - V_{REG} UVLO Protection
  - Thermal Shutdown
  - Fault Condition Indicator (xFAULT)

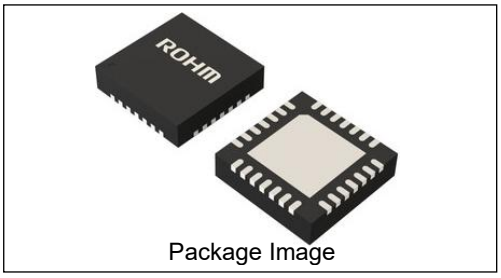
Applications

- Three-phase, Brushless, DC Motors
- Permanent Magnet Synchronous Motors
- Power Tools
- E-Bikes, Mobility

Key Specifications

V_{CC} Range	4.5 V to 60 V
Gate Driver Strength (Source)	0.7 A (Typ)
Gate Driver Strength (Sink)	1.0 A (Typ)
V_{CC} UVLO	3.8 V (Typ)
Maximum Junction Temperature	+150 °C

Package	W (Typ) x D (Typ) x H (Max)
UQFN28AV040A	4.0 mm x 4.0 mm x 1.0 mm



Package Image

Typical Application Circuits

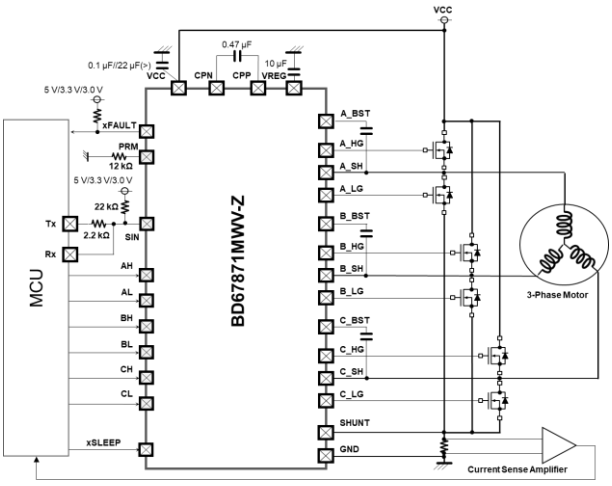


Figure 1. Application Example

Pin Configurations

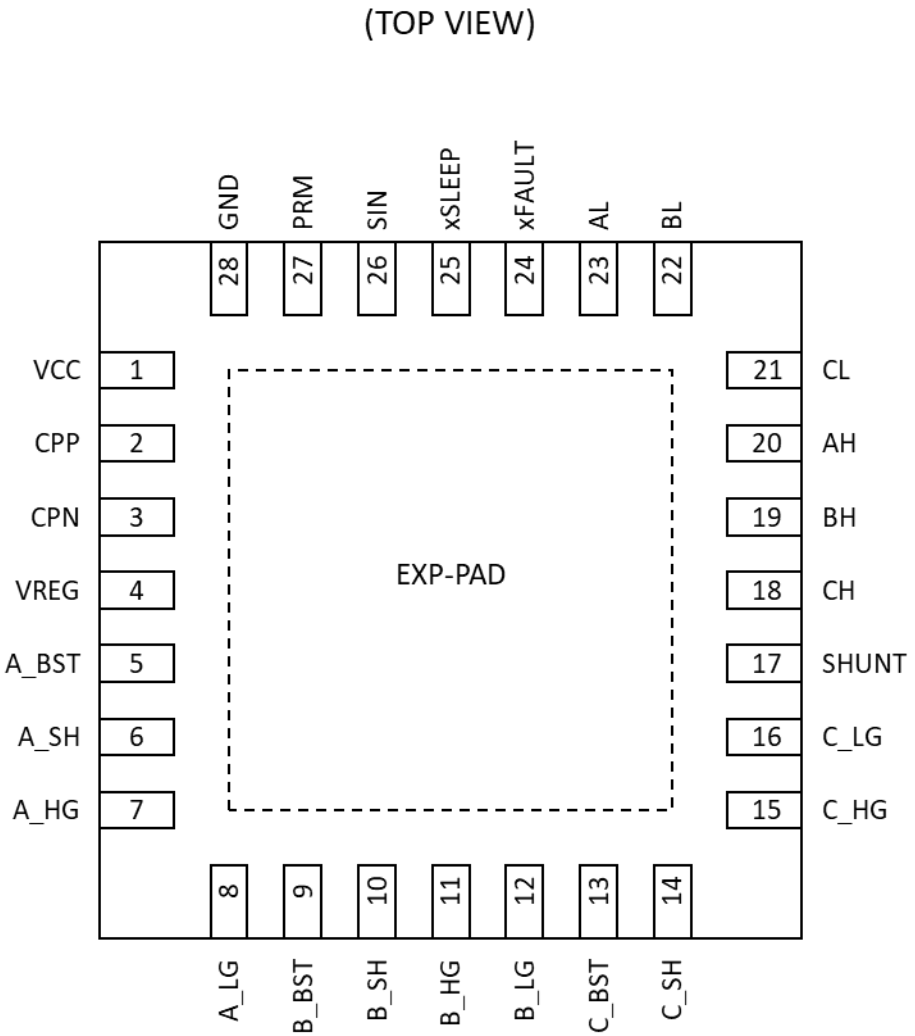


Figure 2. Package Reference

Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Input supply voltage. Bypass VCC to ground with a ceramic and electrolytic capacitor. 0.1 µF ceramic capacitor and 22 µF or more electrolytic capacitor are recommended. Apply the same voltage as the drain voltage of the High-side MOSFET.
2	CPP	Charge pump capacitor. Connect a ceramic capacitor between CPP and CPN. Ceramic capacitor is recommended. See component selection guide for recommended value.
3	CPN	
4	VREG	Gate drive supply output. Connect a ceramic capacitor between VREG and ground.
5	A_BST	Bootstrap phase A. Connect a ceramic capacitor to A_SH. See component selection guide for recommended value.
6	A_SH	High-side source connection phase A.
7	A_HG	High-side gate drive output phase A.
8	A_LG	Low-side gate driver output phase A.
9	B_BST	Bootstrap phase B. Connect a ceramic capacitor to B_SH. See component selection guide for recommended value.
10	B_SH	High-side source connection phase B.
11	B_HG	High-side gate driver output phase B.
12	B_LG	Low-side gate drive output phase B.
13	C_BST	Bootstrap phase C. Connect a ceramic capacitor to C_SH. See component selection guide for recommended value.
14	C_SH	High-side source connection phase C.
15	C_HG	High-side gate driver output phase C.
16	C_LG	Low-side gate driver output phase C.
17	SHUNT	Return path for low-side driver.
18	CH	Phase C high-side input.
19	BH	Phase B high-side input.
20	AH	Phase A high-side input.
21	CL	Phase C low-side input.
22	BL	Phase B low-side input.
23	AL	Phase A low-side input.
24	xFAULT	Fault indication. Open-drain output and it is logic low when in a fault condition.
25	xSLEEP	When the xSLEEP pin is driven to ground, the gate driver is put into sleep mode.
26	SIN	Half duplex Serial Interface to change internal parameters. UART protocol can be used.
27	PRM	Analog parameter definition resistor. Gate Drive current is adjusted with this resistor. Gate Drive current is adjusted by the connected resistor. Please pull-down with 12 kΩ.
28	GND	Ground.
-	EXP-PAD	Connect exposed pad to GND.

Block Diagram

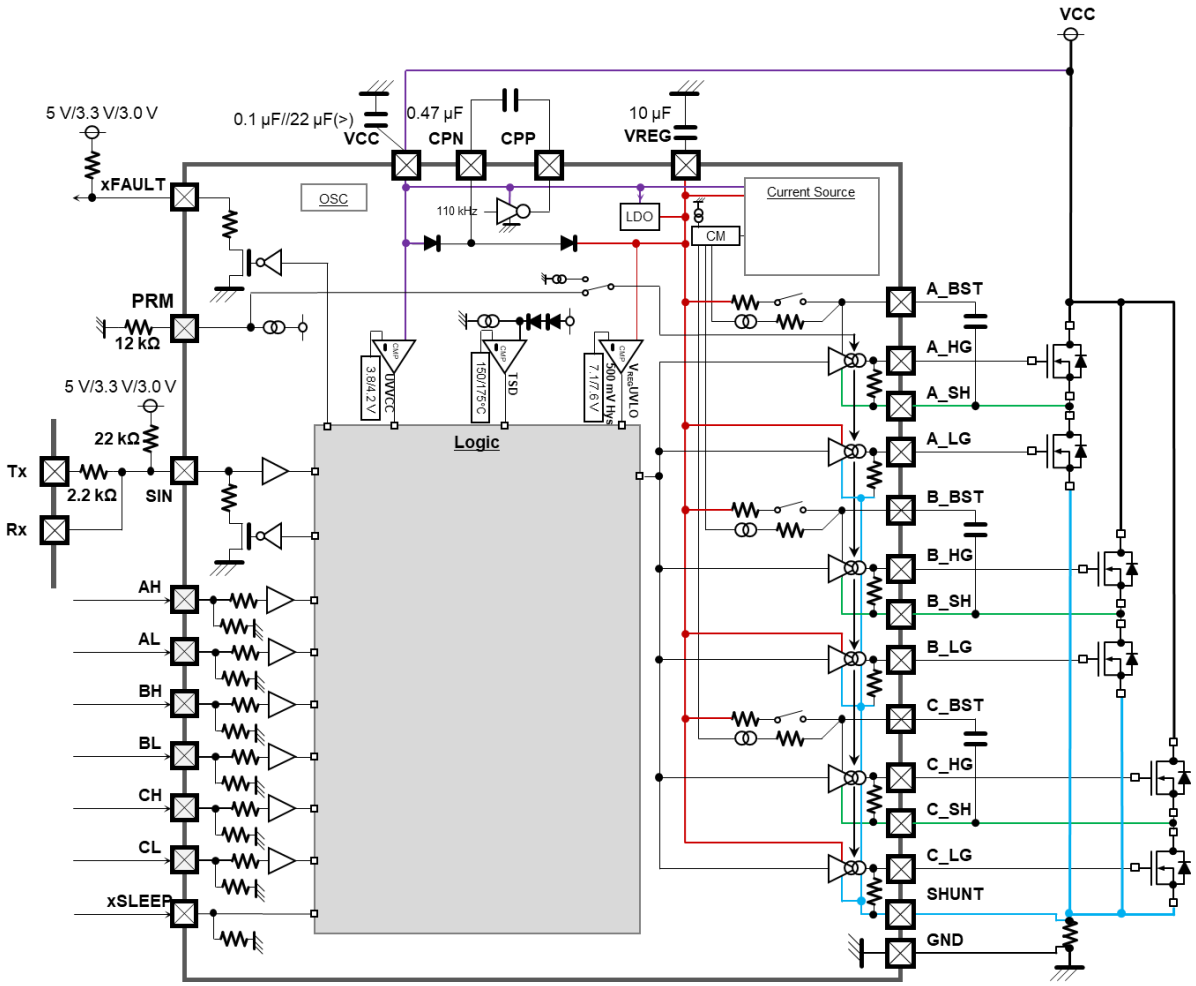


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (respect to GND unless otherwise noted.)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{CC}	-0.3 to +65.0	V
CPP Pin Input Voltage	V_{CPP}	-0.3 to +15.5	V
CPN Pin Input Voltage	V_{CPN}	-0.3 to +15.5	V
VREG Pin Input Voltage	V_{REG}	-0.3 to +15.0	V
*_BST-*_SH (* = A, B, C) *(Note 1)*	$V_{*\_BST-*\_SH}$	-0.3 to +15.0	V
*_BST-*_HG (* = A, B, C) *(Note 1)*	$V_{*\_BST-*\_HG}$	-0.3 to +15.0	V
_BST (= A, B, C) *(Note 1)*	V_{*_BST}	-0.3 to +80.0	V
_HG (= A, B, C) *(Note 1) (Note 2)*	V_{*_HG}	-5.0 to +80.0	V
_LG (= A, B, C) *(Note 1)*	V_{*_LG}	-0.3 to +15.0	V
_SH (= A, B, C) *(Note 1) (Note 2)*	V_{*_SH}	-5.0 to +65.0	V
VCC-*_SH (* = A, B, C) *(Note 1) (Note 2)*	V_{VCC-*_SH}	-1.0 to + (V_{CC} + 5.0)	V
SHUNT Pin Input Voltage	V_{SHUNT}	-0.3 to +1.0	V
PRM Pin Input Voltage	V_{PRM}	-0.3 to +2.0	V
xSLEEP Pin Input Voltage	V_{xSLEEP}	-0.3 to +6.5	V
SIN Pin Input Voltage	V_{SIN}	-0.3 to +6.5	V
Logic Input Voltage	V_{IN}	-0.3 to +6.5	V
xFAULT Pull-up Voltage	V_O	-0.3 to +6.5	V
xFAULT Sink Performance	I_O	5	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) A,B and C is one of 3outputs name
(Note 2) Acceptable time duration of Negative Voltage depends on external capacitor value placed between *_BST and *_SH. (V*_BST-V*_SH must be ≤15 V). As a reference, it would be covered over 2 µs if the capacitor value is 1 µF

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{CC}	4.5	-	60	V
Input Voltage Ramp Rate at Power Up	$V_{CC\_RAMP\_UP}$	-	-	30.0	V/µs
Input Voltage Ramp Rate During Operation	$V_{CC\_RAMP\_ope}$	-	-	4.0	V/µs
Slew Rate on *_SH Pins	V_{SH_SR}	-	-	4.0	V/ns
PRM Pin Input Voltage	V_{PRM}	0.0	-	1.0	V
xSLEEP Pin Input Voltage	V_{xSLEEP}	0.0	-	5.5	V
SIN Pin Input Voltage	V_{SIN}	0.0	-	5.5	V
xFAULT Pull-up Voltage	V_O	0.0	-	5.5	V
Logic Input Voltage	V_{IN}	0.0	-	5.5	V
Minimum Pulse Input Width of xSLEEP	t_{W_SLP}	20	-	-	µs
Operating Temperature	Topr	-40	-	+125	°C
Operating Junction Temperature	Tj	-40	-	+150	°C

Thermal Resistance *(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
UQFN28AV040A				
Junction to Ambient	θ_{JA}	113.00	44.10	°C/W
Junction to Top Characterization Parameter *(Note 4)*	Ψ_{JT}	14.00	9.00	°C/W

(Note 3) Based on JESD51-2A (Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics (Unless otherwise specified V_{CC} = 24 V, Topr = 25 °C) *(Note 8)*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power Supply						
Input Supply Voltage	V_{CC}	4.5	-	60	V	
Quiescent Current	I_{VCC}	5.0	7.5	10	mA	V_{xSLEEP} ≥ 2.0 V (active mode) (A_SH, B_SH, C_SH) = (H, Z, L) R_{PRM} = 12 kΩ, Without TCP
	I_{VCC1}	-	7.6	-	mA	V_{xSLEEP} ≥ 2.0 V (active mode) xH, xL is 20 kHz Switching R_{PRM} = 12 kΩ
	I_{VCCQ}	-	-	1	μA	V_{xSLEEP} ≤ 0.6 V (sleep mode)
Control Logic						
Input Logic Low Threshold	V_{IL}	-	-	0.8	V	
Input Logic High Threshold	V_{IH}	2.0	-	-	V	
xSLEEP Input Low Threshold	V_{IL_xSLEEP}	-	-	0.6	V	
xSLEEP Input High Threshold	V_{IH_xSLEEP}	2.0	-	-	V	
SIN Input Low Threshold	V_{IL_SIN}	-	-	0.8	V	
SIN Input High Threshold	V_{IH_SIN}	2.0	-	-	V	
SIN Input Baud Rate	BR_{SIN}	103.7	115.2	126.7	kbps	
Logic Input Current	$I_{IN(H)}$	3	6	10	μA	V_{IN} = 5.0 V
	$I_{IN(L)}$	-10	+1	+10	μA	V_{IN} = 0.8 V
Internal Pull-down Resistance	R_{PD}	640	800	960	kΩ	6 control pins
Open-drain Outputs						
xFAULT Low Voltage	V_{OL_FAULT}	-	-	0.5	V	I_O = 5.0 mA
xFAULT High Leakage Current	I_{OH_FAULT}	-	-	1	μA	V_O = 3.3 V
SIN Low Voltage	V_{OL_SIN}	-	-	0.5	V	I_O = 5.0 mA
SIN High Leakage Current	I_{OH_SIN}	-	-	10	μA	V_O = 5.0 V
SIN Internal Pull-down Resistance	R_{PD_SIN}	640	800	960	kΩ	
Protection Circuit						
V_{CC} Voltage as OK to Active	V_{CC_GOOD}	3.9	4.2	4.5	V	
V_{CC} UVLO Detecting Voltage	V_{CC_NG}	3.6	3.8	4.0	V	
V_{CC} Hysteresis	V_{CC_HYS}	0.2	0.4	0.6	V	
V_{REG} Threshold	V_{REG_GOOD}	7.2	7.6	8.0	V	
V_{REG} UVLO Detecting Voltage	V_{REG_NG}	6.7	7.1	7.5	V	
V_{REG} Hysteresis	V_{REG_HYS}	0.3	0.5	0.7	V	
V_{BST-SH} UVLO Detecting Voltage	V_{BST-SH_NG}	3.0	3.8	4.5	V	
TSD Detecting Temperature	T_{TSDON}	-	175	-	°C	
TSD Temperature as OK to Active	T_{TSDOFF}	-	150	-	°C	
TSD Hysteresis	T_{TSDHYS}	-	25	-	°C	
V_{REG} Start Up Delay	t_{REG}	-	850	-	μs	
Wake Up Time	t_{WAKEUP}	-	1	-	ms	V_{xSLEEP} ≥ 2.0 V (active mode)
Turn Off Time	t_{SLEEP}	-	4	-	μs	V_{xSLEEP} ≤ 0.6 V (sleep mode)

(Note 8) Voltage is measured from GND unless otherwise noted.

Electrical Characteristics - continued (Unless otherwise specified V_{CC} = 24 V, Topr = 25 °C) *(Note 8)*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Gate Drive						
Bootstrap Diode Forward Voltage	V_{FBOOT}	-	-	0.9	V	I_F = 5 mA
V_{REG} Output Voltage	V_{REG}	10.0	12.5	13.5	V	V_{CC} = 6.25 V to 60 V
		2 x V_{CC}-1	-	2 x V_{CC}		V_{CC}= 4.5 V to 6.25 V
Constant Current Setting Voltage	V_{PRM}	0.75	0.80	0.85	V	R_{PRM} = 12 kΩ
HS Constant Current on 1st Step	I_{HSON1}	63	90	117	mA	*_HG - *_SH = 0 V *(Note 9)*
HS Constant Current on 2nd Step	I_{HSON2}	32	45	59	mA	*_HG - *_SH = 0 V *(Note 9)*
HS Constant Current on 3rd Step	I_{HSON3}	-	260	-	mA	*_HG - *_SH = 0 V *(Note 9)*
HS Constant Current on 3rd Step Minimum	$I_{HSON3-M}$	21	30	39	mA	*_HG - *_SH = 0 V *(Note 10)*
HS Constant Current off 2nd Step	I_{HSOFF2}	32	45	59	mA	*_HG - *_SH = 12.5 V *(Note 9)*
HS Constant Current off 3rd Step	I_{HSOFF3}	-	360	-	mA	*_HG - *_SH = 12.5 V *(Note 9)*
HS Constant Current off 3rd Step Minimum	$I_{HSOFF3-M}$	32	45	59	mA	*_HG - *_SH = 12.5 V *(Note 10)*
LS Constant Current on 1st Step	I_{LSON1}	63	90	117	mA	*_LG - SHUNT = 0 V *(Note 9)*
LS Constant Current on 2nd Step	I_{LSON2}	32	45	59	mA	*_LG - SHUNT = 0 V *(Note 9)*
LS Constant Current on 3rd Step	I_{LSON3}	-	250	-	mA	*_LG - SHUNT = 0 V *(Note 9)*
LS Constant Current on 3rd Step Minimum	$I_{LSON3-M}$	19	28	37	mA	*_LG - SHUNT = 0 V *(Note 10)*
LS Constant Current off 2nd Step	I_{LSOFF2}	32	45	59	mA	*_LG - SHUNT = 12.5 V *(Note 9)*
LS Constant Current off 3rd Step	I_{LSOFF3}	-	350	-	mA	*_LG - SHUNT = 12.5 V *(Note 9)*
LS Constant Current off 3rd Step Minimum	$I_{LSOFF3-M}$	29	42	53	mA	*_LG - SHUNT = 12.5 V *(Note 10)*
Gate Driver Strength (source)	I_{SRC}	-	0.7	-	A	Pulse width < 200 ns, Full on
Gate Driver Strength (sink)	I_{SNK}	-	1	-	A	Pulse width < 200 ns, Full on
HS Gate Drive Pull-up Resistance	R_{HS-UP}	2	5	8	Ω	I_D = 100 mA
HS Gate Drive Pull-down Resistance	R_{HS-DN}	1.0	3.0	5.5	Ω	I_D = 100 mA
HS Semiactive Pull-down Resistance	$R_{HS-SADN}$	-	-	16	kΩ	*_HG - *_SH = 2 V
LS Gate Drive Pull-up Resistance	R_{LS-UP}	2	5	8	Ω	I_D = 100 mA
LS Gate Drive Pull-down Resistance	R_{LS-DN}	1.0	3.0	5.5	Ω	I_D = 100 mA
LS Semiactive Pull-down Resistance	$R_{LS-SADN}$	-	-	16	kΩ	*_LG - SHUNT = 2 V
LS Automatic Turn-on Time	t_{LS}	-	0.5	-	µs	After $V_{REG} \geq V_{REG\_GOOD}$
Charge Pump Frequency	f_{CP}	-	110	-	kHz	
Turn On/Off Delay from 6inputs to 6outputs	t_{RISEHS}	-	40	-	ns	Rise Delay (*_SH = 0 V, *_LG - SHUNT = 0 V)
	t_{RISELS}	-	40	-	ns	Rise Delay (*_SH = 0 V, *_HG - *_SH = 0 V)
	t_{FALLHS}	-	40	-	ns	Fall Delay (*_SH = 0 V, *_LG - SHUNT = 0 V)
	t_{FALLLS}	-	40	-	ns	Fall Delay (*_SH = 0 V, *_HG - *_SH = 0 V)
Matching Propagation Delay per Phase to Phase	$t_{PD\_MATCH\_PP}$	-	+/-1	-	ns	
Maximum Frequency of 6inputs	f_{MAX_6IN}	-	-	1000	kHz	R_{PRM} = 12 kΩ
Minimum Pulse Width	t_{W_6IN}	45	-	-	ns	V_{CC} = 4.5 V

(Note 8) Voltage is measured from GND unless otherwise noted.
(Note 9) UART register in default state, R_{PRM} = 12 kΩ. Please see Gate Driver Current Setting for details.
(Note 10) UART register in 1st and 2nd step minimum setting and 3rd step minimum + 1 LSB setting at R_{PRM} = 12 kΩ.

Operation and Functionality

The BD67871MWV-Z is three-phase Brushless DC Motor gate driver that can drive external N-channel MOSFET in half-bridge configuration with 0.8 A sourcing and 1.2 A sinking capability. Adjustability of the gate drive current is achieved through a combination of an external PRM resistor and registers to further adjust the current levels via UART serial interface. The gate driver operates over a wide input voltage range of 4.5 V to 60 V while also supporting up to 100 % duty cycle output gate drive. A nominal gate drive voltage of 12.5 V allows operation of external N-channel MOSET for lower RDSON and lowering power losses. The gate drive features protection features such as input voltage under voltage lockout, bootstrap voltage under voltage lockout, gate driver power supply voltage under voltage lockout and internal thermal shutdown. Additionally, an adjustable dead time control circuit allows robust system operation.

Timing Chart

The timing chart of power up is shown in Figure 4, while power down is shown in Figure 5.
Power-up sequence starts after the voltage on V_{CC} is V_{CC} UVLO threshold (V_{CC_GOOD}) or above. After this the gate driver power supply V_{REG} starts to power-on. V_{REG} voltage must be V_{REG} UVLO (V_{REG_GOOD}) or above before the gate driver output is active and follow the input logic.
When xSLEEP pin is pulled below the input logic low level, the chip will enter sleep mode. After this point the gate driver will stop to follow the input logic signal.

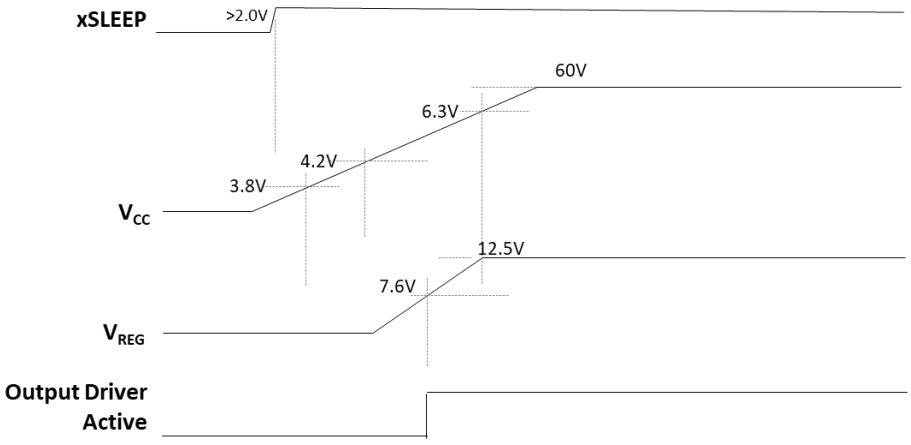


Figure 4. Timing Chart (power supply turn-on)

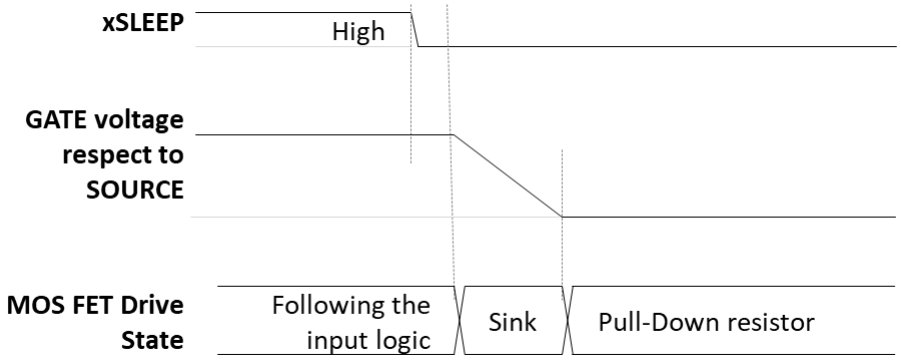


Figure 5. Timing Chart (xSLEEP pulled low)

Operation and Functionality - continued

Gate Drive Architecture

The gate driver chip has both an internal high-side push-pull and an internal low-side push-pull current driver to drive external N-channel MOSFETs. Input pin AH, BH, CH directly provide logic input signal for the high-side driver, while the AL, BL, CL pin provide logic input signal for the low-side driver. The gate driver has two modes of driving the gate from the phase control input pins. The low-side driver is powered directly from the VREG pin and referenced to the SHUNT pin. The high-side driver on the other hand is powered by a bootstrap circuitry that includes an internal bootstrap diode and an external bootstrap capacitor. The bootstrap circuitry operates by taking power from VREG pin and, relying on the switching operation of the switching node, will create a floating supply between A_BST, B_BST, C_BST and A_SH, B_SH, C_SH pins. However, at very high output duty cycle operation there will not be enough off-time on the switching node to allow the bootstrap diode to recharge the external bootstrap capacitor thus causing the bootstrap capacitor to eventually lose charge. To circumvent this, an internal Current Source circuit is dedicated to always provide a small amount of charging current to the A_BST, B_BST, C_BST pin directly from the VCC pin thus allowing external Bootstrap capacitor to not discharge and allowing 100 % output duty cycle operation. Additionally, both the high-side driver and the low-side driver includes an internal pulldown resistor between the gate pin and the return pin to ensure the external MOSFET is not accidentally turned on when the respective gate driver does not have sufficient power.

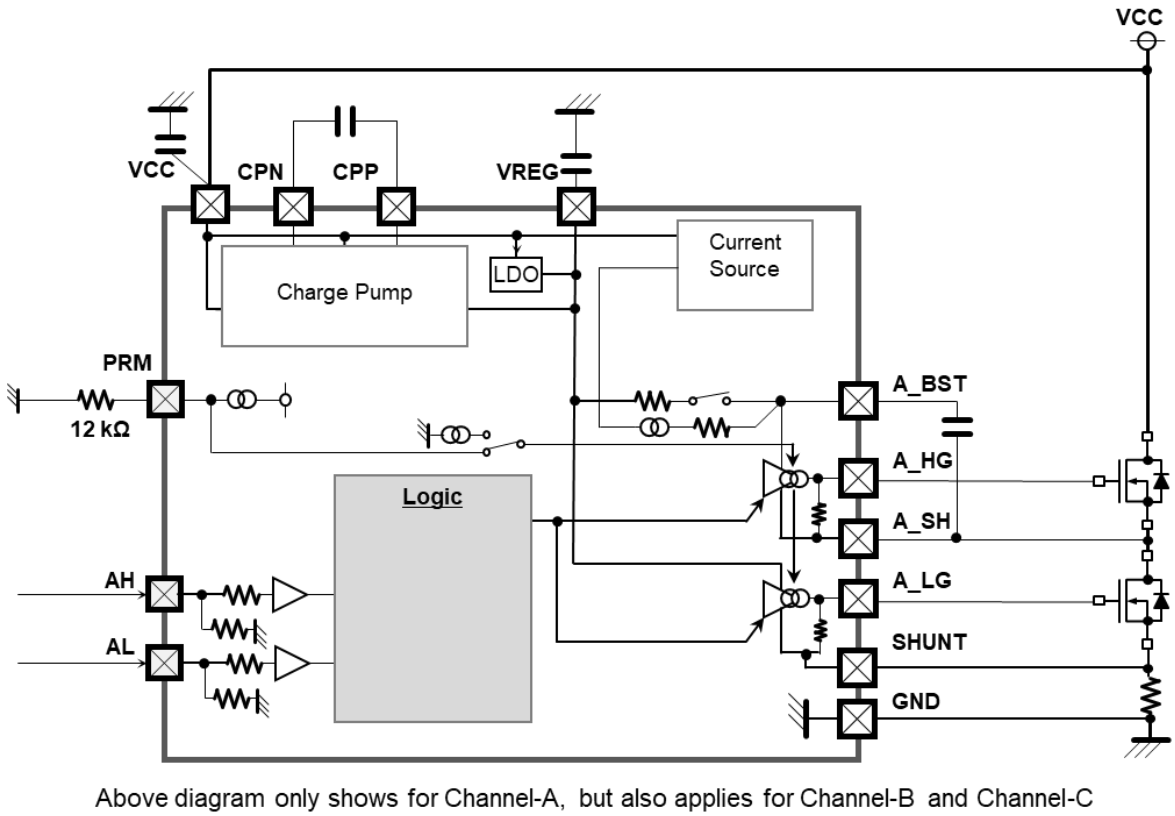


Figure 6. Gate Driver Architecture

Operation and Functionality - continued

Gate Drive Power Supply (V_{REG})

The gate driver block is powered from the VREG pin. The VREG pin is powered from a combination of internal voltage converters (Table 1). Figure 27 shows V_{REG} Voltage vs Input Voltage at Different Load Currents. This measurement circuit is designed to evaluate the source capability of the V_{REG}. Placing a sink current at the load to check if the V_{REG} voltage can be maintained. The load for the V_{REG} are the low-side output and the charging path of the bootstrap capacitor.

Table 1. V_{REG} Operation (No Load)

V_{CC} Voltage [V]	Typical V_{REG} Output Voltage [V]	V_{REG} Operation Mode
14.5 < V_{CC}	12.5	LDO
6.25 < V_{CC} ≤ 14.5	11.3 to 12.5	Charge Pump and LDO
4.5 ≤ V_{CC} ≤ 6.25	(2 x V_{CC}-1) to (2 x V_{CC})	Charge Pump

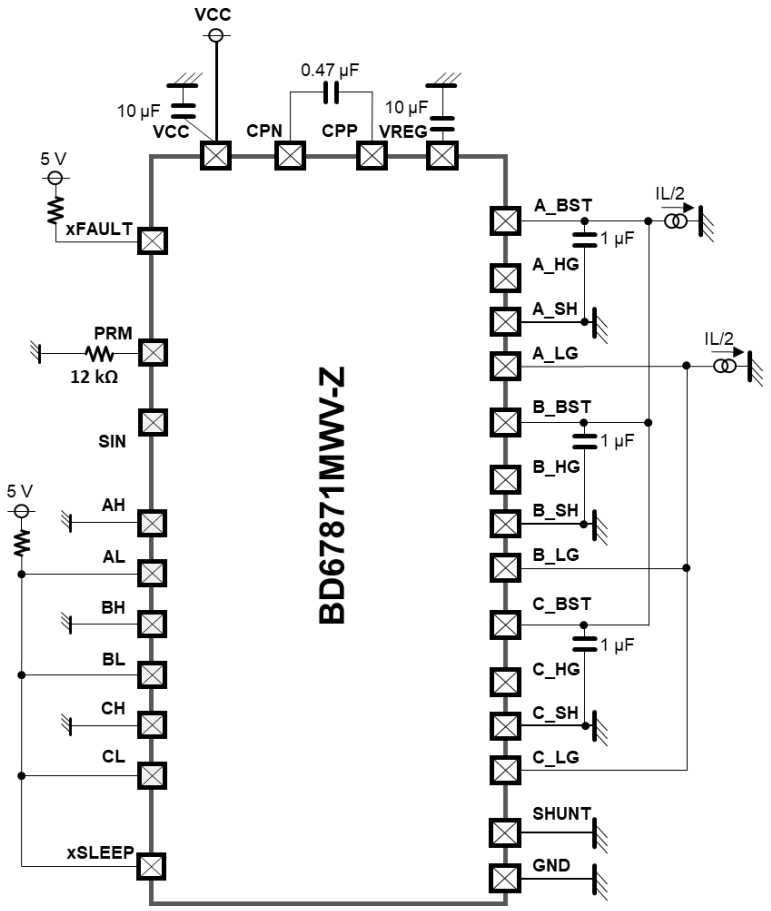


Figure 7. Measurement Circuit

Operation and Functionality - continued

Input Logic

Input mode of 6 inputs pins can be changed by PWM_MODE bit programmed via UART.
When this bit is programmed = 1, then AH, BH, CH and AL, BL, CL input signals directly control the state of the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive signal if xSLEEP is a logic 1. When AH, BH, CH and AL, BL, CL input signals are logic 1 at the same time, the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive signals are forced low to prevent cross conduction of external N-channel MOSFET.
When this bit is programmed = 0, then the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive will follow the logic of AH, BH, CH input signal if both xSLEEP and AL, BL, CL is a logic 1. In all other combination the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive will be low causing A_SH, B_SH, C_SH pin to be in a high impedance state.
It is recommended to use EN/IN mode for having a good power consumption.

Table 2. BD67871MWV-Z Input Logic Truth Table

xSLEEP	PWM_MODE (Address 0x03 Bit 4)	AH (BH / CH)	AL (BL / CL)	A_HG (B_HG / C_HG)	A_LG (B_LG / C_LG)	A_SH (B_SH / C_SH)
0	X	X	X	L	L	Hi-Z
1	1: IN/IN (Default)	0	0	L	L	Hi-Z
		0	1	L	H	GND
		1	0	H	L	V_{CC}
		1	1	L	L	Hi-Z
	0: EN/IN (Recommend)	X	0	L	L	Hi-Z
		0	1	L	H	GND
		1	1	H	L	V_{CC}

Cross Conduction Prevention

Input logic pins AH, BH, CH and AL, BL, CL is provided externally and controls the gate signal directly, there is a cross conduction prevention function that prevents both external N-channel MOSFET from turning on when both AH, BH, CH and AL, BL, CL input signals are a Table 2. BD67871MWV-Z will output both high-side drive signal A_HG, B_HG, C_HG and low-side drive signal A_LG, B_LG, C_LG to be low thus turning off.

Sleep Mode (xSLEEP input pin)

When the xSLEEP pin is driven to ground, the gate driver device is put into sleep mode and consumes little quiescent current in order to reduce power consumption from the input VCC pin. At this state, all the internal circuitry is disabled, and all the input logic pins are ignored. The gate driver output is put into high-impedance mode. When xSLEEP pin is driven high, the gate driver will start the power up sequence.

Operation and Functionality - continued

Protection

The BD67871MWV-Z has features to protect against input voltage V_{CC} under voltage lockout (V_{CC} UVLO), regulated driver voltage supply V_{REG} under voltage lockout (V_{REG} UVLO), bootstrap voltage $V_{*\_BST-*\_SH}$ under voltage lockout ($V_{*\_BST-*\_SH}$ UVLO) and internal Thermal Shutdown (TSD).
For V_{CC} UVLO, the gate driver will turn off and all output drive voltages whenever the input voltage V_{CC} drops below V_{CC_NG} threshold. The gate driver will recover and turn back on when input voltage V_{CC} rises above V_{CC_GOOD}.
For both V_{REG} UVLO and TSD, the behavior of the output drive voltage, the xFAULT pin condition as well as the recovery method is shown in the Table 3. For $V_{*\_BST-*\_SH}$ UVLO, it turns off the output drive independently with ABC. Please refer to Table 4.

Table 3. Behavior of V_{REG} UVLO and Internal Thermal Shutdown Protection Features

Fault	Condition	xFAULT	Output	Recovery
V_{REG} UVLO	$V_{REG} \leq V_{REG\_NG}$	Pulled Low	Hi-Z	Auto / xSLEEP = L
	$V_{REG} \geq V_{REG\_GOOD}$	Hi-Z	Active	
Thermal Shutdown	Internal die temperature ≥ T_{TSDON}	Pulled Low	Hi-Z	Auto / xSLEEP = L
	Internal die temperature ≤ T_{TSDOFF}	Hi-Z	Active	

Table 4. Behavior of $V_{BST\ -\ SH}$ UVLO Protection Features
(*) denotes “A/B/C”

Fault	Condition	PWM_MODE (Address 0x03 Bit 4)	*H	*L	xFAULT	Output	Recovery
V_{BST-SH} UVLO	$V_{*\_BST-*\_SH} \leq V_{BST-SH\_NG}$	1: IN/IN	1	0	Pulled Low	Hi-Z	Auto / xSLEEP = L
			Other		Hi-Z	Active	
		0: EN/IN	1	1	Pulled Low	Hi-Z	
			Other		Hi-Z	Active	
	$V_{*\_BST-*\_SH} > V_{BST-SH\_NG}$	Don’t Care			Hi-Z	Active	-

Table 5. Example of V_{BST-SH} UVLO Protection

Condition	PWM_MODE (Address 0x03 Bit 4)	Input Logic	xFAULT	Output	Recovery
$V_{A\_BST-A\_SH} \leq V_{BST-SH\_NG}$ $V_{B\_BST-B\_SH} \leq V_{BST-SH\_NG}$ $V_{C\_BST-C\_SH} > V_{BST-SH\_NG}$	1: IN/IN	AH = 1, AL = 0 BH = 0, BL = 1 CH = 1, CL = 0	Pulled Low	A_SH = Hi-Z B_SH = GND C_SH = V_{CC}	Auto / xSLEEP = L

xFAULT Pin

xFAULT indicates that a fault condition occurred in the gate driver. A pull-up resistor to an externally supplied 5 V (depends on the Controller side input range) voltage is required to be connected to the xFAULT pin.
Normally xFAULT pin is in Hi-Z condition. If either an Under Voltage Lockout on V_{REG} or $V_{*\_BST-*\_SH}$ voltage occurs, or a Thermal Shutdown (TSD) event occurs, the xFAULT pin on the device will be pulled low by an internal pulldown device. The xFAULT pin will only be pulled low during the duration of the fault condition.

De-glitcher for FAULT Condition

A 3 µs (Typ) de-glitching filter is employed to avoid any false detection of fault conditions that may be caused by noise conditions.

Operation and Functionality - continued

The Architecture of Trickle Charge Pump

Operation of Trickle Charge Pump

Trickle Charge Pump (TCP) supports the operations of 100 % PWM duty and Hi-Z state.
When 100 % PWM Duty or Hi-Z state continues for 200 µs or above, TCP is enabled for each channel. When TCP is enabled, the circuit current of high-side gate driver changes to smaller.
For example, TCP is disabled at 20 kHz PWM operation and normal bootstrap operation is used. Figure 8 shows a timing chart of TCP.

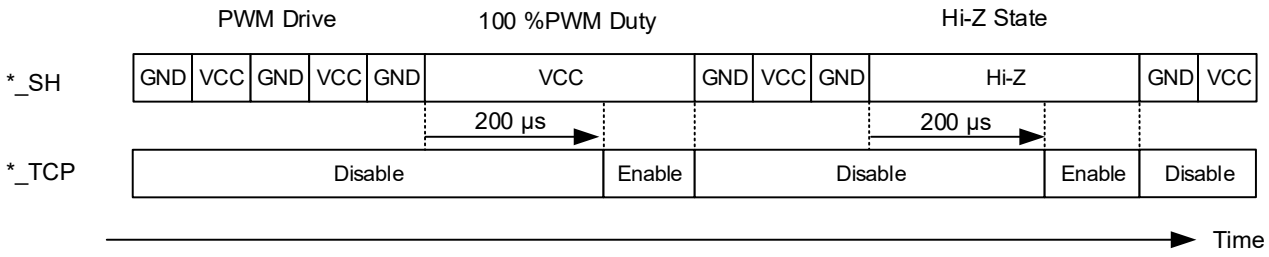


Figure 8. Timing Chart of TCP

Current Capability of Trickle Charge Pump

Figure 9 shows a block diagram of TCP. The TCP current is the internal constant current minus the amount consumed by the high-side gate driver.
Note that the current capability of TCP is several 10 µA (Table 6).

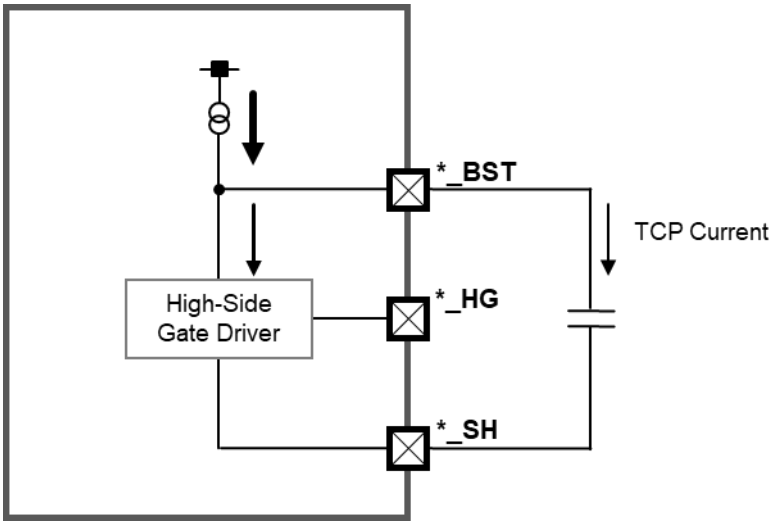


Figure 9. Block Diagram of TCP

Table 6. Current Capability of TCP

TCP Current	*_BST - *_SH Voltage	Condition
0 µA	12 V	Typical
≥ 5 µA	10 V	Worst

Operation and Functionality - continued

The Architecture of Active Gate Drive (TriC3™)

In BD67871MWV-Z employs a method to turn on and off the gate of the external MOSFET by going through different steps where the current drive strength is adjusted accordingly. Adjustment of gate current drive strength is done via a combination of UART register.

Figure 10 shows the circuit configuration of TriC3™. Four sensors are used to actively monitor various voltages, and the information is then used to control the gate drive voltage. The four sensors are the Gate-Source (GS) sensor of the high-side MOSFET, the GS sensor of the low-side MOSFET, the low-side potential sensor of the OUT voltage and the high-side potential sensor of the OUT voltage. These sensors are required to perform at high speed, as this speed of operation significantly impacts their efficiency. To reduce the overall power consumption of the gate driver, these sensors are configured to keep their current consumption low.

Figure 11 shows circuit configuration of TriC3™ drive block. This block is divided into two parts to ensure smooth active gate drive. One is for the 2nd step, and the rest is for the other steps.

*_SH pin support down to -5 V, TriC3™ can also do negative voltage suppression without loss of efficiency.

Depending on the environment, if the current value of the 1st step is increased, the 1st and 2nd steps may repeat. In this case, reduce the 1st step current setting.

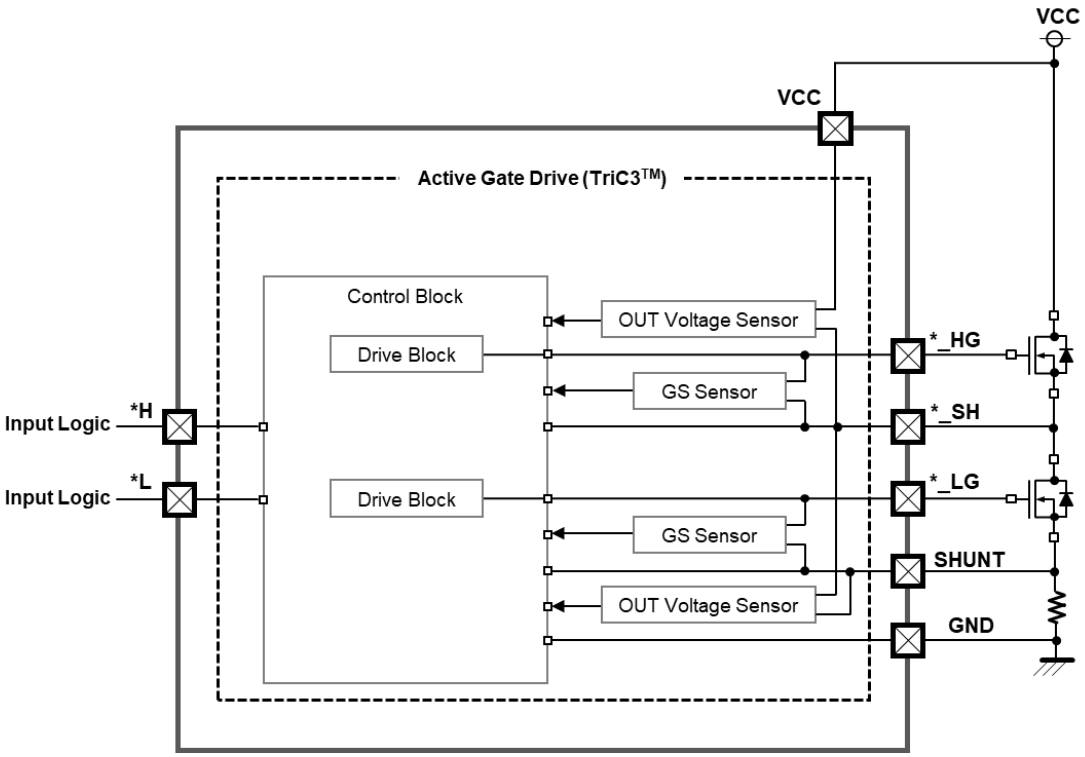


Figure 10. Circuit Configuration of TriC3™

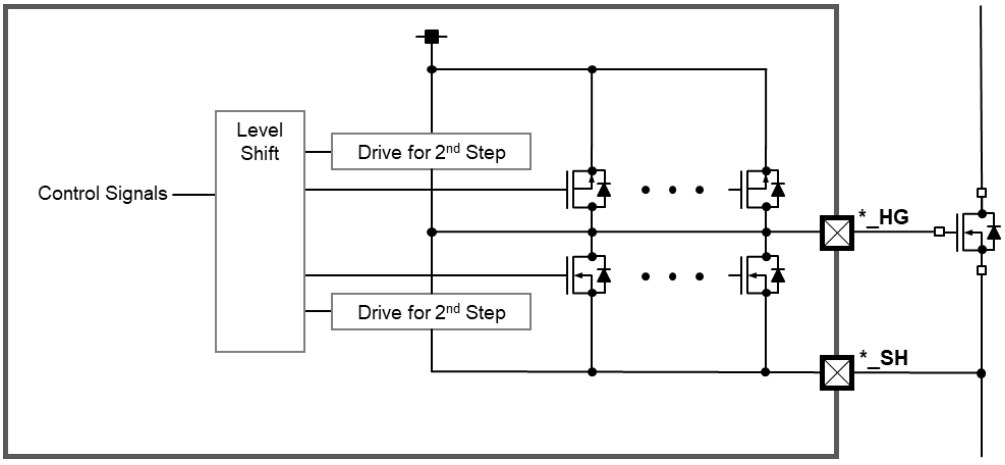


Figure 11. Circuit Configuration of TriC3™ Drive Block

The Architecture of Active Gate Drive (TriC3™) - continued

Figure 13 shows a zoom up of Figure 12, Figure 15 shows a zoom up of Figure 14.
The GS sensor of the high-side MOSFET is used from 1st step to 2nd step and the OUT voltage sensor is used from 2nd step to 3rd step. This configuration is one of the features of TriC3™.
At Time2, the gate drive current is reduced because of the timing of large power supply current deviation. This has the effect of suppressing power supply current deviation and avoiding excessive ringing during body diode reverse recovery.
At Time3, the gate drive current is increased because the timing of the power supply current change is small. This has the effect of reducing the switching losses of the MOSFETs.

Dead Time Adjustment

The TriC3™ has a built-in function to monitor the gate-source voltage of external MOSFETs.
Consider the timing when the low-side MOSFET turns OFF and the high-side MOSFET turns ON in Figure 13.
When the VGS voltage of the low-side MOSFET falls below the GS sensor threshold voltage, a STRONG OFF state occurs and the gate of the low-side MOSFET is pulled down by a low impedance and turn off. At the same time, the gate current of the high-side MOSFET is supplied. The high-side MOSFET starts at VGS = 0 V and therefore does not turn on until the threshold of the high-side MOSFET
In this way, the dead time is optimized and minimized by sensing the gate voltage and controlling gate current ensuring that it does not turn on simultaneously under changing environmental conditions, product variations and operating conditions.
Please set the dead time of the MCU to ZERO regardless of whether you are using IN/IN mode or EN/IN mode, because BD67871MWV-Z manages dead time by monitoring output pins

The Architecture of Active Gate Drive (TriC3™) - continued

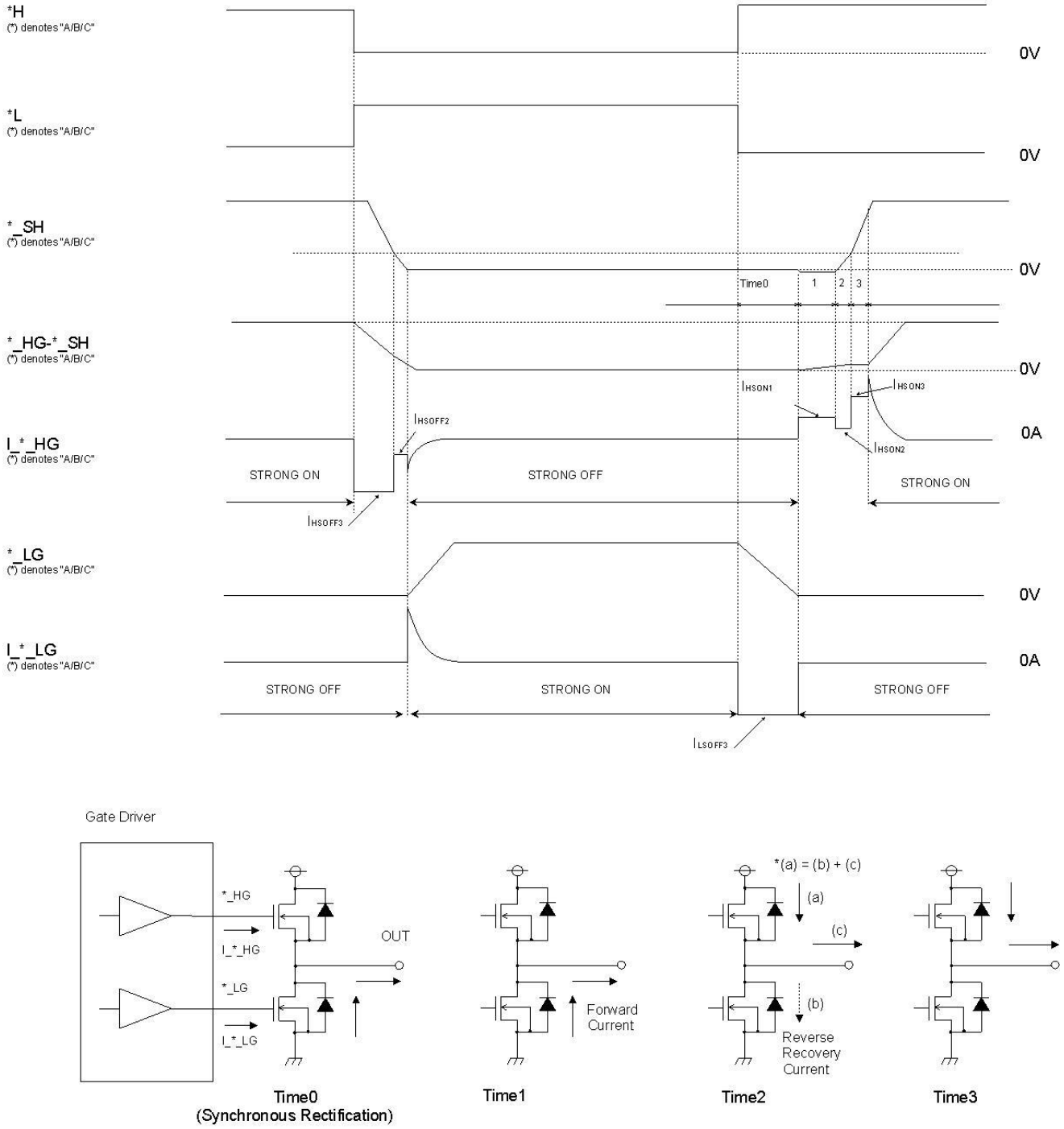


Figure 12. The Waveform of TriC3™ (IN/IN Mode, Current Source Condition)

The Architecture of Active Gate Drive (TriC3™) - continued

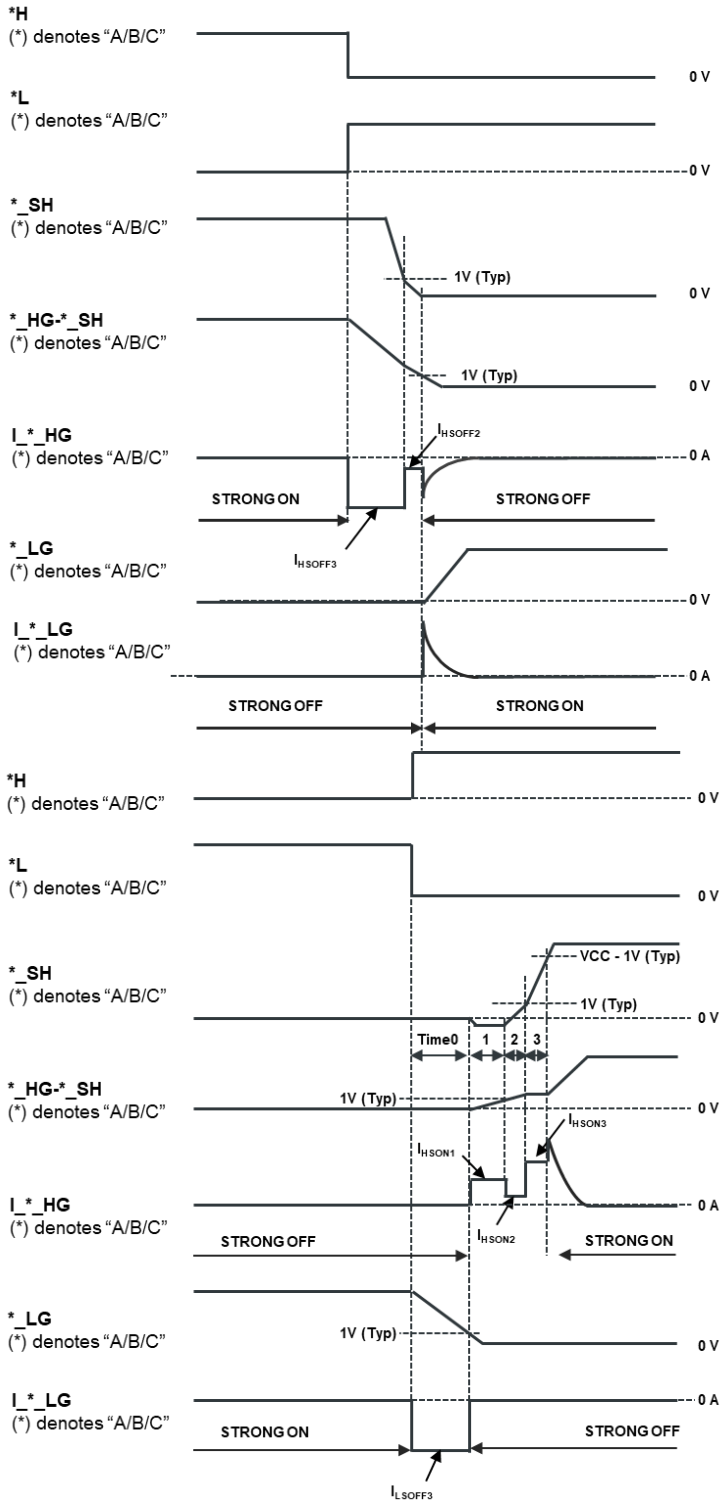


Figure 13. The Waveform of TriC3™ (IN/IN Mode, Current Source Condition) Zoom

The Architecture of Active Gate Drive (TriC3™) - continued

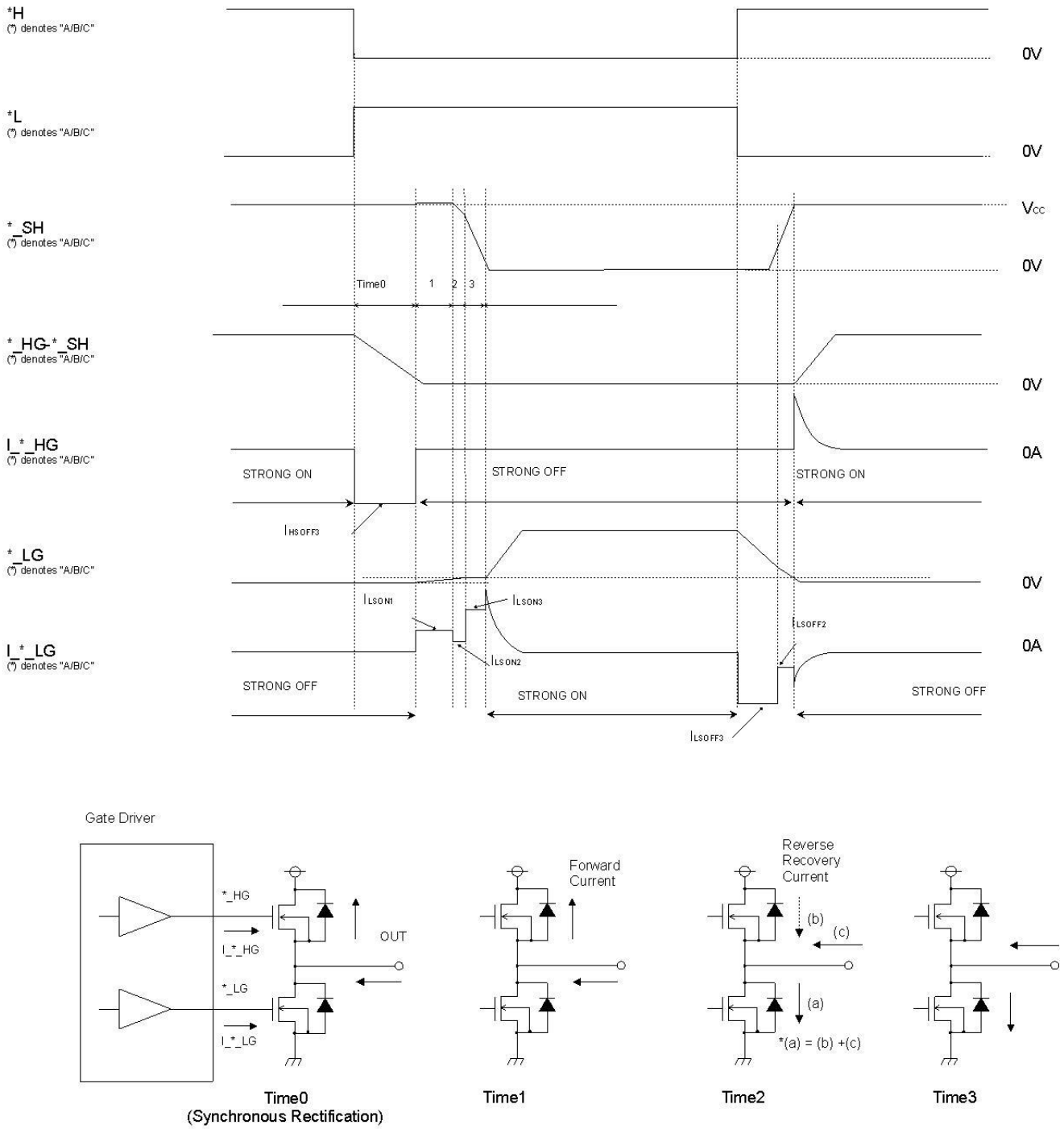


Figure 14. The Waveform of TriC3™ (IN/IN Mode, Current Sink Condition)

The Architecture of Active Gate Drive (TriC3™) - continued

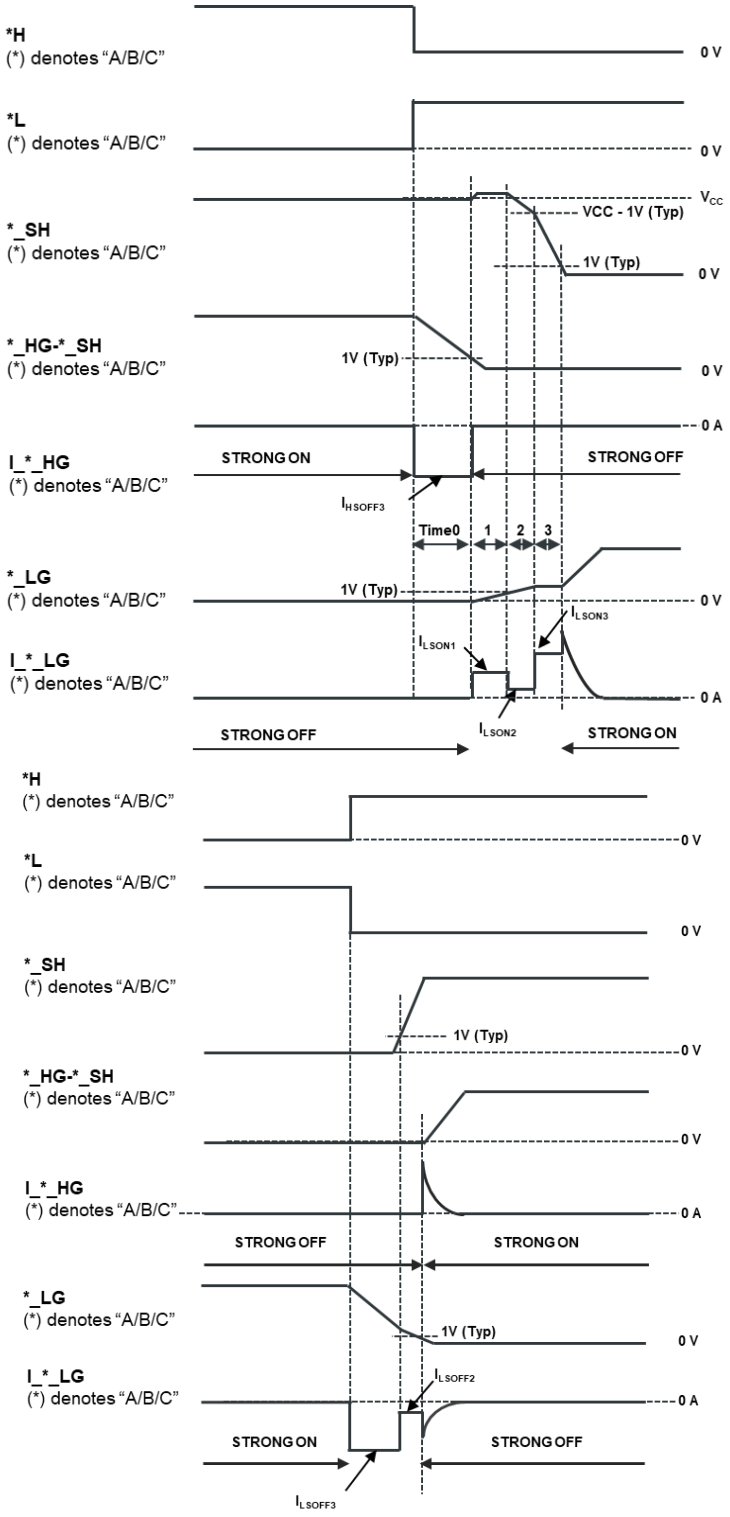


Figure 15. The Waveform of TriC3™ (IN/IN Mode, Current Sink Condition) Zoom

The Architecture of Active Gate Drive (TriC3™) - continued

Gate Driver Current Setting

Figure 16 shows a relationship between the gate driver current setting and UART register setting. The STRONG ON/OFF setting cannot be configured via the UART register and is fixed at the maximum setting of the 3rd step.

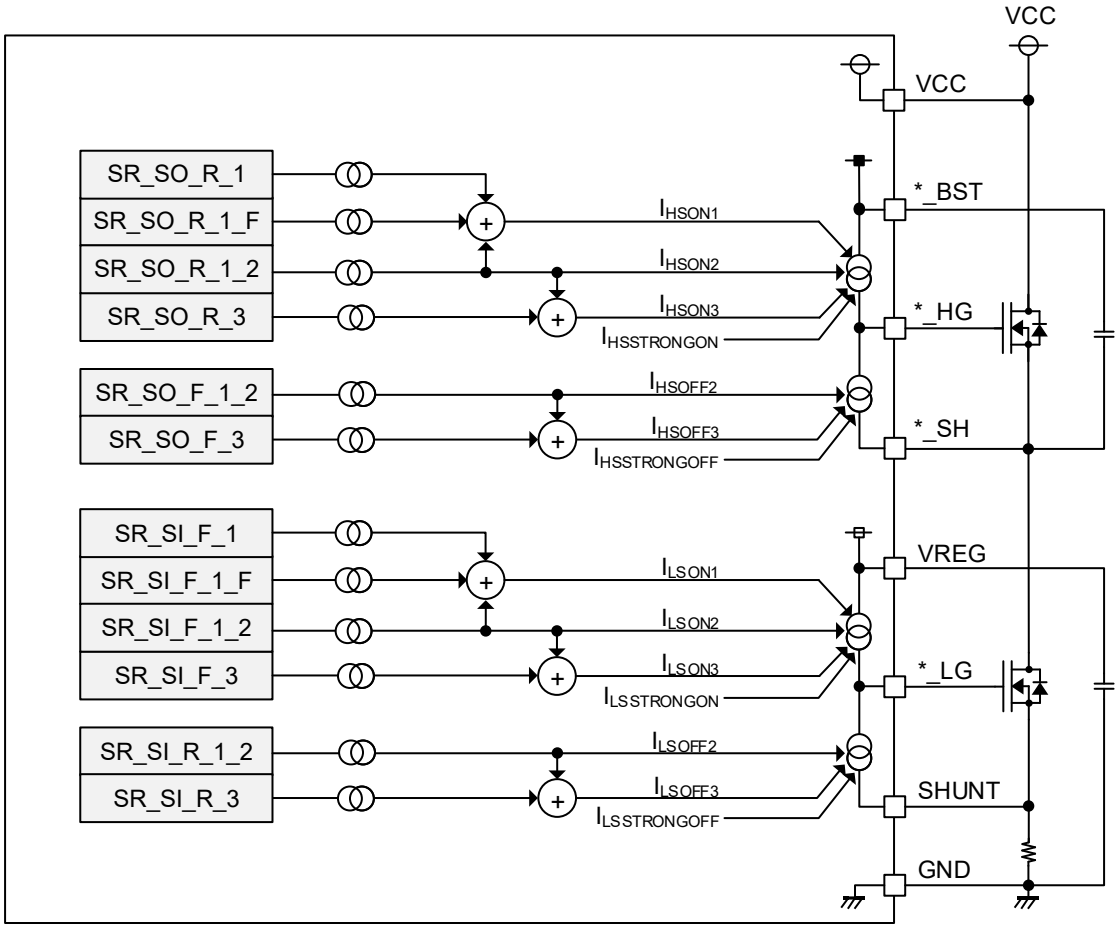


Figure 16. Gate Driver Current Setting and UART Register Setting

Gate Driver Current Setting - continued

Table 7 shows the formulas for calculating each gate current.
Table 8 shows the design values of the current range for each UART register setting. These values assume the moment when current begins to flow to the gate of the external MOSFET, with the PRM pin pull-down by external 12 kΩ resistor.

Table 7. Formulas for Calculating Gate Driver Current

Symbol	Calculation
I_{HSON1}	SR_SO_R_1 + SR_SO_R_1_F + SR_SO_R_1_2
I_{HSON2}	SR_SO_R_1_2
I_{HSON3}	SR_SO_R_1_2 + SR_SO_R_3
$I_{HSSTRONGON}$	Fixed at the maximum setting of the 3rd step (No setting).
I_{HSOFF2}	SR_SO_F_1_2
I_{HSOFF3}	SR_SO_F_1_2 + SR_SO_F_3
$I_{HSSTRONGOFF}$	Fixed at the maximum setting of the 3rd step (No setting).
I_{LSON1}	SR_SI_F_1 + SR_SI_F_1_F + SR_SI_F_1_2
I_{LSON2}	SR_SI_F_1_2
I_{LSON3}	SR_SI_F_1_2 + SR_SI_F_3
$I_{LSSTRONGON}$	Fixed at the maximum setting of the 3rd step (No setting).
I_{LSOFF2}	SR_SI_R_1_2
I_{LSOFF3}	SR_SI_R_1_2 + SR_SI_R_3
$I_{LSSTRONGOFF}$	Fixed at the maximum setting of the 3rd step (No setting).

Table 8. Design Values of the Current Range for UART Register Setting

Symbol	Current Range	Figure	Condition
SR_SO_R_1 [5:0]	3.8 mA (LSB) to 215 mA (MSB) 1 LSB = 3.36 mA	Figure 28	*_HG - *_SH = 0 V
SR_SO_R_1_2 [5:0]			
SR_SO_F_1_2 [5:0]			*_HG - *_SH = 12.5 V
SR_SI_F_1 [5:0]			*_LG - SHUNT = 0 V
SR_SI_F_1_2 [5:0]			
SR_SI_R_1_2 [5:0]			*_LG - SHUNT = 12.5 V
SR_SO_R_1_F [4:0]	0 mA (LSB) to 818 mA (MSB) 1 LSB = 2.64 mA	Figure 29	*_HG - *_SH = 0 V
SR_SO_R_3 [4:0]			
SR_SO_F_3 [4:0]	0 mA (LSB) to 1240 mA (MSB) 1 LSB = 3.99 mA	Figure 30	*_HG - *_SH = 12.5 V
SR_SI_F_1_F [4:0]	0 mA (LSB) to 762 mA (MSB) 1 LSB = 2.46 mA	Figure 31	*_LG - SHUNT = 0 V
SR_SI_F_3 [4:0]			
SR_SI_R_3 [4:0]	0 mA (LSB) to 1160 mA (MSB) 1 LSB = 3.76 mA	Figure 32	*_LG - SHUNT = 12.5 V

Gate Driver Current Setting - continued

Guidelines for Replacing from Constant Voltage or Current Gate Drivers to TriC3™

Table 9 shows the current setting guidelines for TriC3™.

When replacing from constant voltage or current gate driver to TriC3™, adjust the 2nd step current to match the current of constant voltage or current gate driver.

Figure 17 shows the comparison waveform between assuming constant current gate driver (I_{HSON1} = I_{HSON2} = I_{HSON3}) and default settings of TriC3™.

Figure 18 shows the comparison waveform between assuming constant voltage gate driver and default settings of TriC3™.

Table 9. Current Setting Guideline

Symbol	Setting
I_{HSON1}	Normally 2 times of I_{HSON2}. *(Note 11)*
I_{HSON2}	Adjust the current when the output of constant voltage or constant current gate driver is at 1 V.
I_{HSON3}	Normally 4 times of I_{HSON2}.
$I_{HSSTRONGON}$	No setting
I_{HSOFF2}	Adjust the current when the output of constant voltage or constant current gate driver is at 1 V.
I_{HSOFF3}	Normally 4 times of I_{HSOFF2}.
$I_{HSSTRONGOFF}$	No setting
I_{LSON1}	Normally 2 times of I_{LSON2}. *(Note 11)*
I_{LSON2}	Adjust the current when the output of constant voltage or constant current gate driver is at V_{CC} -1 V.
I_{LSON3}	Normally 4 times of I_{LSON2}.
$I_{LSSTRONGON}$	No setting
I_{LSOFF2}	Adjust the current when the output of constant voltage or constant current gate driver is at V_{CC} - 1 V.
I_{LSOFF3}	Normally 4 times of I_{LSOFF2}.
$I_{LSSTRONGOFF}$	No setting

(Note 11) Depending on the environment, if the current value of the 1st step is increased, the 1st and 2nd steps may repeat. In this case, reduce the 1st step current setting.

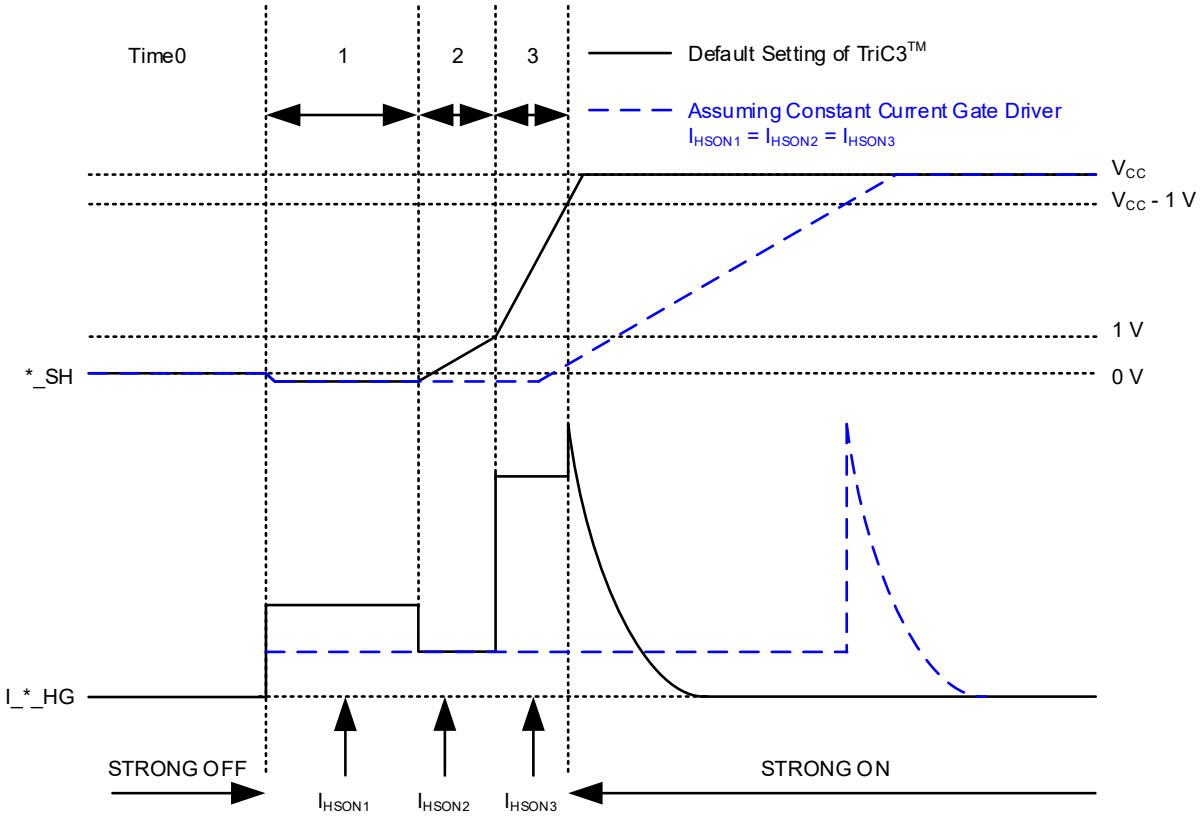


Figure 17. Comparison between assuming Constant Current Gate Driver (I_{HSON1} = I_{HSON2} = I_{HSON3}) and Default Settings of TriC3™ (High-side Turn On with Current Source Condition)

Guidelines for Replacing from Constant Voltage or Current Gate Drivers to TriC3™ - continued

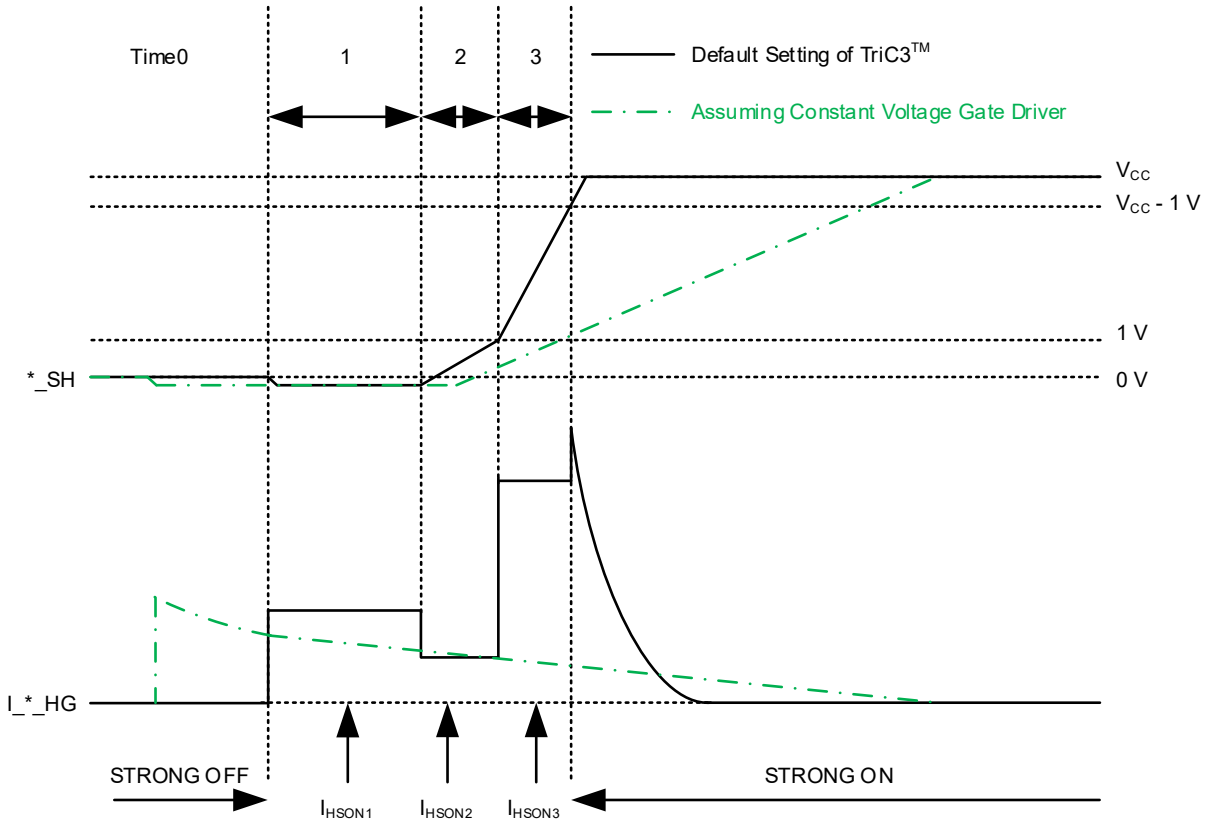


Figure 18. Comparison between assuming Constant Voltage Gate Driver and Default Settings of TriC3™ (High-side Turn On with Current Source Condition)

Operation and Functionality - continued

Serial Interface

BD67871MWV-Z has a serial interface to change current drive parameters. The serial interface is called half duplex serial interface based on UART protocol. Baud rate is expected to be 115.2 kbps.

UART Frame Structure

The UART frame in BD67871MWV-Z consists of a start bit, data bits, and stop bit. There is no parity bit. The frame structure is shown Figure 19.

Data Bits

The data bits consist of 7 bits of address and 1 bit used for baud rate measurement, or 8 bits of data. The 1 bit used for baud rate measurement is not a common requirement in UART protocol.

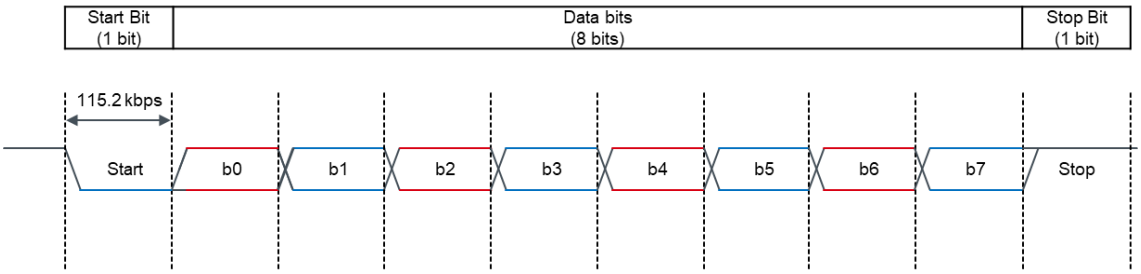


Figure 19. UART Frame Structure

Serial Interface - continued

Tx Data Frame

The Tx data frame consists of 2 bytes, which are the register address and the register data.
If you set the bit 6 of the address (A6 in Figure 20) to 0, the register will be updated with the Tx data, and the updated value will be returned. If you set it to 1, the register will not be updated with the Tx data, and the current register value will be returned.

Rx Data Frame

The Rx data frame consists of 1 byte of register data. If BD67871MWV-Z receives the Tx data frame correctly, it returns the 1 byte register data received more than 1 bit after the stop bit of the Tx data frame.

Example of UART Communication

Figure 20 shows an example of communication between the controller and the BD67871MWV-Z.
Figure 21 shows an example when reading the SR_SO_R_1 register.
Figure 22 shows an example when setting the SR_SO_R_1 register to 0x00.

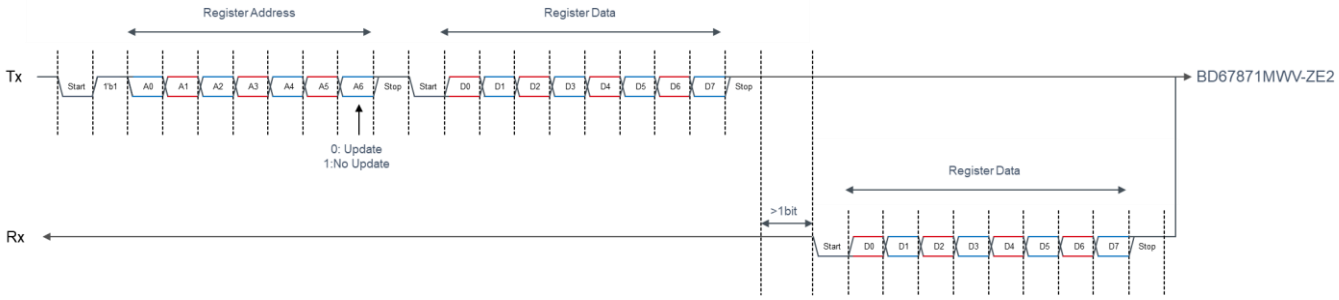


Figure 20. The Example of UART Communication

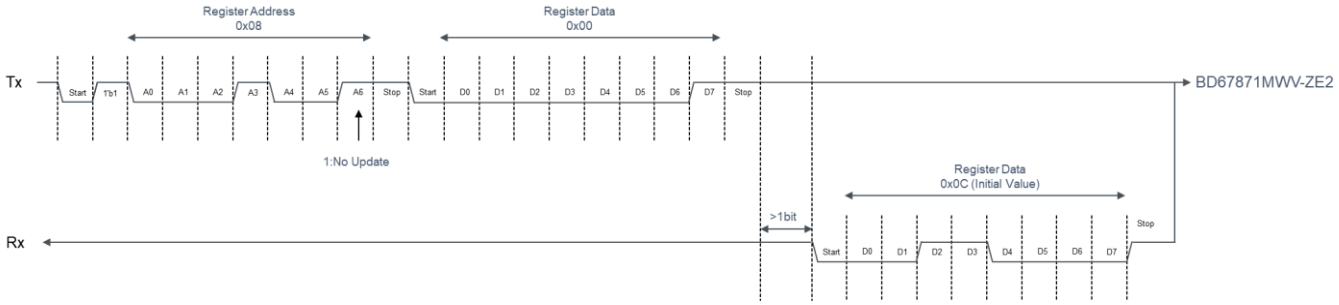


Figure 21. Reading the SR_SO_R_1 Register

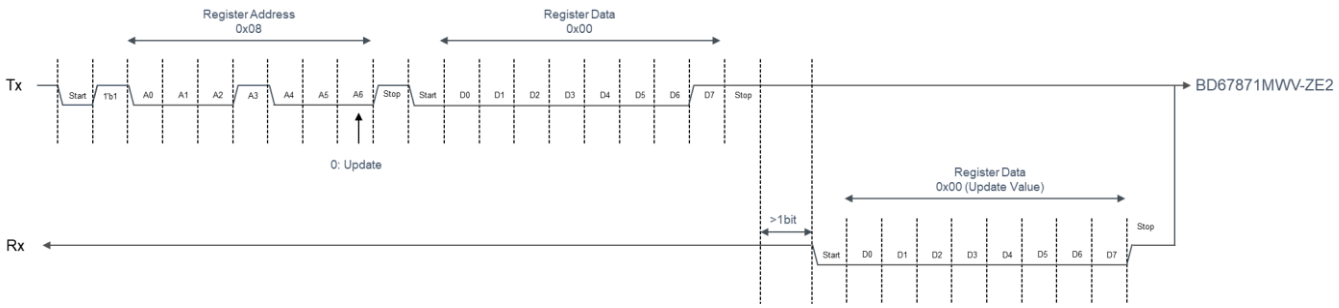


Figure 22. Setting the SR_SO_R_1 Register to 0x00

Serial Interface - continued

Register Map

The register map is shown in Table 10.

Table 10. Register Map
(R: read only register, W/R: write and read register, -: write-protected due to reserved register)

Address	W/R	Initial Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	R	0x71	PRODUCT							
0x01	-	-	-	-	-	-	-	-	-	-
0x02	-	-	-	-	-	-	-	-	-	-
0x03	W/R	0x10	-	-	-	PWM_MODE	-	-	-	-
0x04	-	-	-	-	-	-	-	-	-	-
0x05	-	-	-	-	-	-	-	-	-	-
0x06	R	0x70	-	BSTUV_A	BSTUV_B	BSTUV_C	-	-	-	-
0x07	W/R	0x00	SR_SET_SEL	-	-	-	-	-	-	-
0x08	W/R	0x0C	-	-	SR_SO_R_1					
0x09	W/R	0x0C	-	-	SR_SO_R_1_2					
0x0A	W/R	0x08	-	-	-	SR_SO_R_3				
0x0B	W/R	0x00	-	-	-	SR_SO_R_1_F				
0x0C	W/R	0x0C	-	-	SR_SO_F_1_2					
0x0D	W/R	0x08	-	-	-	SR_SO_F_3				
0x0E	W/R	0x00	-	-	-	SR_SI_F_1_F				
0x0F	W/R	0x0C	-	-	SR_SI_R_1_2					
0x10	W/R	0x08	-	-	-	SR_SI_R_3				
0x11	W/R	0x0C	-	-	SR_SI_F_1					
0x12	W/R	0x0C	-	-	SR_SI_F_1_2					
0x13	W/R	0x08	-	-	-	SR_SI_F_3				

Serial Interface - continued

Description of Registers

The definitions of each bit in the registers are as follows.

0x00: Product

Bit	Symbol	W/R	Initial Value	Description
[7:0]	PRODUCT	R	0x71	Return product name.

0x03: PWM Mode

Bit	Symbol	W/R	Initial Value	Description
4	PWM_MODE	W/R	1b	Change the PWM MODE. For more details, please refer to Table 2. 0: EN/IN (Recommend) 1: IN/IN (Default)

0x06: BSTUV

Bit	Symbol	W/R	Initial Value	Description
6	BSTUV_A	R	1b	The status of $V_{A\_BST-A\_SH}$ under voltage lockout. For more details, please refer to Table 4. 0: $V_{A\_BST-A\_SH}$ under voltage lockout 1: Default
5	BSTUV_B	R	1b	The status of $V_{B\_BST-B\_SH}$ under voltage lockout. For more details, please refer to Table 4. 0: $V_{B\_BST-B\_SH}$ under voltage lockout 1: Default
4	BSTUV_C	R	1b	The status of $V_{C\_BST-C\_SH}$ under voltage lockout. For more details, please refer to Table 4. 0: $V_{C\_BST-C\_SH}$ under voltage lockout 1: Default

0x07: Reference Current

Bit	Symbol	W/R	Initial Value	Description
7	SR_SET_SEL	W/R	0b	Switches between setting the reference current for the gate current using the external PRM resistor or using internal constant current. 0: External (Default) 1: Internal

0x08: Current Setting of I_{HSON1}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SO_R_1	W/R	0x0C	Adjusting the current setting of I_{HSON1}. For more details, please refer to Table 7.

0x09: Current Setting of I_{HSON1}, I_{HSON2} and I_{HSON3}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SO_R_1_2	W/R	0x0C	Adjusting the current setting of I_{HSON1}, I_{HSON2} and I_{HSON3}. For more details, please refer to Table 7.

0x0A: Current Setting of I_{HSON3}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SO_R_3	W/R	0x08	Adjusting the current setting of I_{HSON3}. For more details, please refer to Table 7.

0x0B: Current Setting of I_{HSON1}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SO_R_1_F	W/R	0x00	Adjusting the current setting of I_{HSON1}. For more details, please refer to Table 7.

Description of Registers - continued

0x0C: Current Setting of I_{HSOFF2} and I_{HSOFF3}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SO_F_1_2	W/R	0x0C	Adjusting the current setting of I_{HSOFF2} and I_{HSOFF3}. For more details, please refer to Table 7.

0x0D: Current Setting of I_{HSOFF3}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SO_F_3	W/R	0x08	Adjusting the current setting of I_{HSOFF3}. For more details, please refer to Table 7.

0x0E: Current Setting of I_{LSON1}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SI_F_1_F	W/R	0x00	Adjusting the current setting of I_{LSON1}. For more details, please refer to Table 7.

0x0F: Current Setting of I_{LSOFF2} and I_{LSOFF3}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SI_R_1_2	W/R	0x0C	Adjusting the current setting of I_{LSOFF2} and I_{LSOFF3}. For more details, please refer to Table 7.

0x10: Current Setting of I_{LSOFF3}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SI_R_3	W/R	0x08	Adjusting the current setting of I_{LSOFF3}. For more details, please refer to Table 7.

0x11: Current Setting of I_{LSON1}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SI_F_1	W/R	0x0C	Adjusting the current setting of I_{LSON1}. For more details, please refer to Table 7.

0x12: Current Setting of I_{LSON1}, I_{LSON2} and I_{LSON3}

Bit	Symbol	W/R	Initial Value	Description
[5:0]	SR_SI_F_1_2	W/R	0x0C	Adjusting the current setting of I_{LSON1}, I_{LSON2} and I_{LSON3}. For more details, please refer to Table 7.

0x13: Current Setting of I_{LSON3}

Bit	Symbol	W/R	Initial Value	Description
[4:0]	SR_SI_F_3	W/R	0x08	Adjusting the current setting of I_{LSON3}. For more details, please refer to Table 7.

Application and Implementation Guide

Recommended External Component for Typical Application

Table 11. Recommended External Components
(*) denotes “A/B/C”

Components	PIN 1	PIN 2	Recommended
VCC Bypass Bulk Capacitor	VCC	GND	≥ 22 µF, > 2 x V_{CC} rated Bulk Capacitor
VCC Bypass Ceramic Capacitor	VCC	GND	≥ 0.1 µF, > 2 x V_{CC} rated X5R or X7R Ceramic Capacitor
Charge Pump Capacitor	CPP	CPN	470 nF, V_{CC} rated X5R or X7R Ceramic Capacitor
Regulator Bypass Capacitor	VREG	GND	≥ 10 µF, > 25 V rated X5R or X7R Ceramic Capacitor
Pull-up Resistor of xFAULT	xFAULT	≤ 5.5 V	Pull-up Resistor for suitable voltage for the Controller
Base Current Adjustment Resistor	PRM	GND	Connect to GND with 12 kΩ
Bootstrap Capacitor	*_BST	*_SH	Bootstrap Capacitor
Pull-up Resistor of SIN	SIN	≤ 5.5 V	Pull-up to the Controller Power Supply with 1.5 kΩ ~ 47 kΩ
Series Resistor for Tx pin of Controller	SIN	Tx	The Resistance to 1/10 of Pull-up Resistor of SIN. For example, the Pull-up Resistor of SIN is 22 kΩ, set the Resistor to 2.2 kΩ. If you are not using UART communication, please leave it open

Input Power Supply Capacitor Recommendation

Two types of capacitors are recommended to be used on input power supply line VCC. A electrolytic bulk capacitor 22 µF or above that has voltage rating is 2 x V_{CC} or above voltage should be placed near the main connection point of the power supply. A ceramic capacitor (X5R or X7R) 0.1 µF or above with voltage rating 2 x V_{CC} or above voltage should be placed in parallel to supply high frequency components. In addition, it is recommended to place similar ceramic capacitors in between the drain of each high-side MOSFET to the source of the low-side MOSFET for each leg of the 3 phase half-bridges.

Application and Implementation Guide - continued

Bootstrap Capacitor and VREG Capacitor Calculation

Bootstrap Capacitor hold the electrical charge to drive the high-side MOSFET while it is turning on. The charge of the bootstrap capacitor will be used towards charging to high-side MOSFET gate capacitor. It is recommended to follow the below equation:

$$C_{BOOST} \geq 10 \times Qg \qquad [nF]$$

Where:

C_{BOOST}	[nF]	is the capacitance of the bootstrap capacitor.
Qg	[nC]	is the total MOSFET gate charge.

For example, when the high-side MOSFET Qg = 100 nC, select a bootstrap capacitor of value ≥ 1 µF with a voltage rating ≥ 2x V_{REG} (ie. 25 V). This Bootstrap capacitor is driven by current limiting driver, and it has an ability of Min 30 mA. It has to be considered about Bootstrap sequence time duration for enough charging up time.
VREG capacitor holds the charge to supply all of the high-side drivers and low-side drivers. The value should be larger than 6 times or above of the bootstrap capacitor. It is recommended to follow the below equation:

$$C_{VREG} \geq 6 \times C_{BOOST} \qquad [nF]$$

Where:

C_{VREG}	[nF]	is the capacitance of the VREG capacitor.

For example, when C_{BOOST} = 1 µF, then select the capacitor on V_{REG} is 6 µF or above. However, we recommend 10 µF for this because the actual capacitance value will be affected by DC biasing. Also select the VREG capacitor voltage rating to be 25 V or above. This VREG capacitor is driven by current limiting driver, depends on V_{CC} range (Please refer to Table 1)

Application and Implementation Guide - continued

Parallel MOSFET Configuration

For higher current applications, it may be necessary to connect MOSFET in parallel. For such designs, it is important to pay attention to certain aspect of circuit and PCB design. In particular, issues such as current crowding causing to one path heating up more than the other, and self-excited oscillations may occur.

The Figure 23 below shows parasitic components such as drain inductance, source inductance, and gate inductance that if not paid attention to may lead to self-excited oscillations. In general rule, all these inductances should be minimized by using thicker and shorter PCB paths. In addition, individual gate resistors should be used for each parallel MOSFET to ensure more symmetrical current flow.

Additionally, the value of bootstrap capacitor and VREG pin capacitor should be scaled up appropriately to take into account a larger total gate charge that the chip needs to drive.

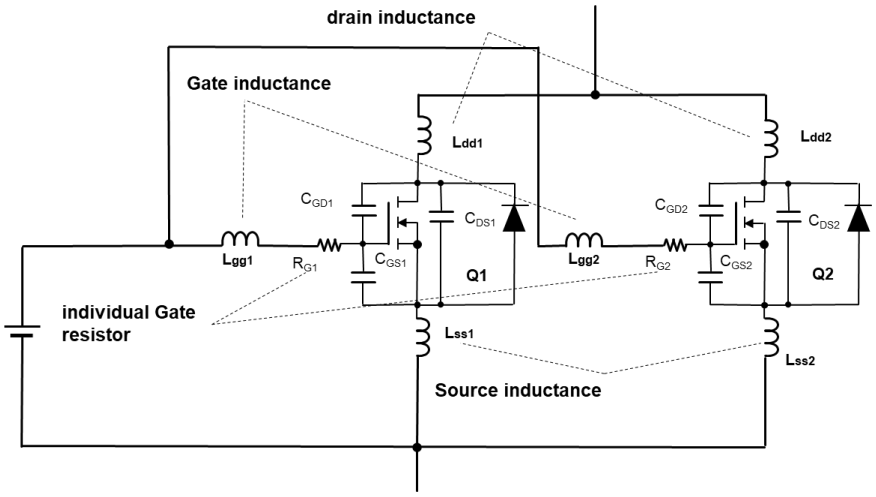


Figure 23. Parasitic Components when Designing for Parallel MOSFET Configuration

PCB Layout Guidelines

High current switching gate driver application require that PCB layout guidelines be followed to ensure optimal performance. In general, below are some important points to consider:

Parasitic inductances should be minimized as they will cause unwanted voltage spikes due to high di/dt current slew rates. This is particularly important on the traces where switching currents operate: drain of power MOSFET, source of power MOSFET, and gate driver output connection to the MOSFET gate. To reduce parasitic PCB trace inductance, use wide copper traces for all the high switching current paths.

1. Place all power supply capacitors (charge pump capacitors, input filter capacitor for VCC pin, capacitor on VREG pin) as close as possible to their respective pins. Route the ground side of the VCC and VREG capacitors to the GND pin of the gate driver device.

2. Separate the path for the input V_{CC} voltage into the gate driver chip from the V_{CC} voltage going to the 3 half-bridges. The path going to the half-bridges is a high current path and as such PCB trace should be wide and if possible connected on multiple layers. Place a bulk electrolytic capacitor near the VCC pin and also a local ceramic capacitors near to the high-side MOSFET drains.

3. Place the bootstrap capacitors for the high-side gate drivers as close as possible to the gate driver chip and when possible on the same layer as the gate driver chip to avoid any vias that introduce parasitic inductance.

4. Layout the high current paths from the VCC pin towards the 3 phases of the half-bridges and towards the return GND path symmetrically to avoid any current crowding and to allow each leg to flow current in a balanced manner.

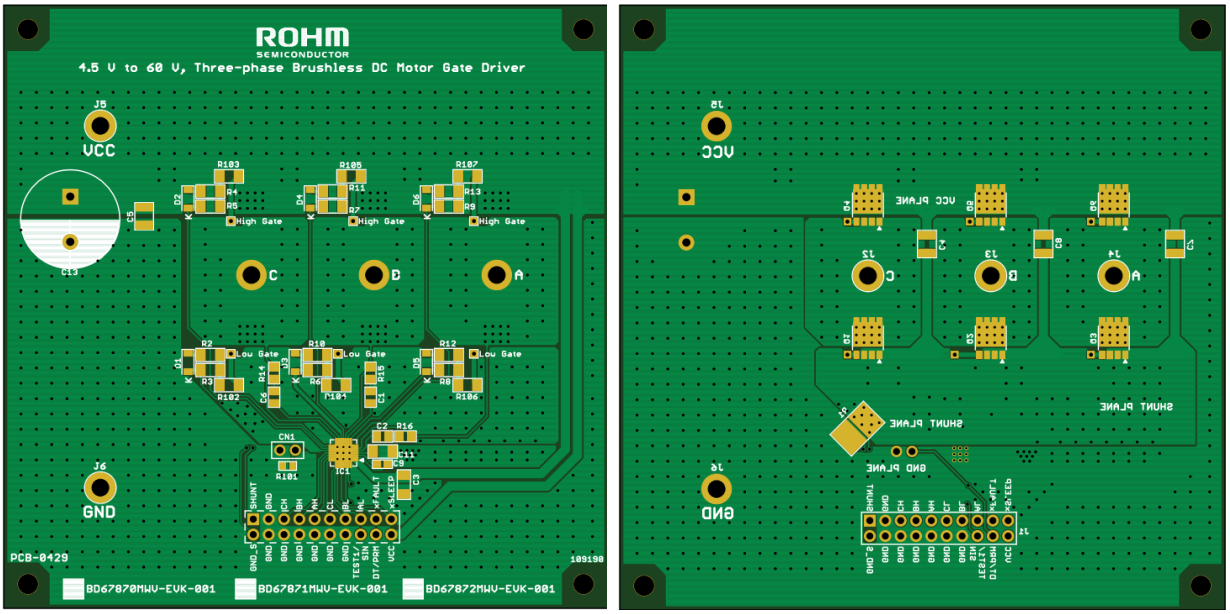


Figure 24. Top View of Recommended PCB Layout (100 mm x 100 mm)

Typical Performance Curves (Reference Data)

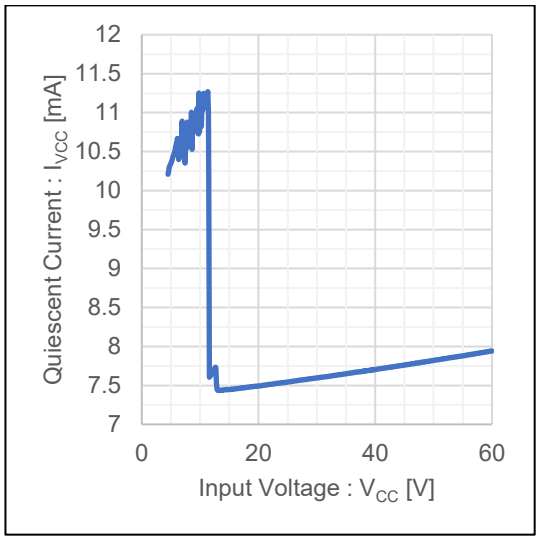


Figure 25. Quiescent Current vs Input Voltage

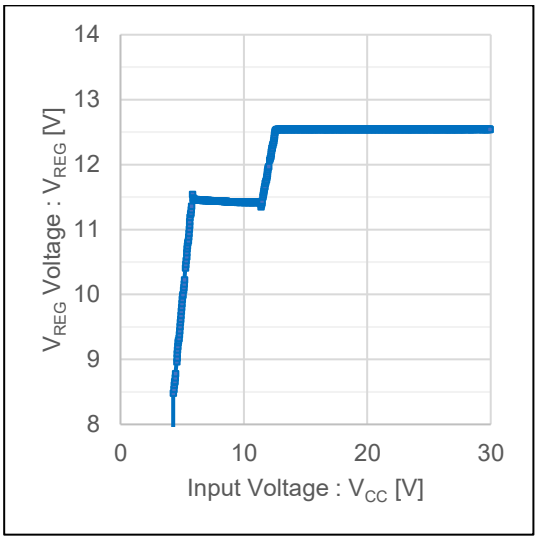


Figure 26. V_{REG} Voltage vs Input Voltage

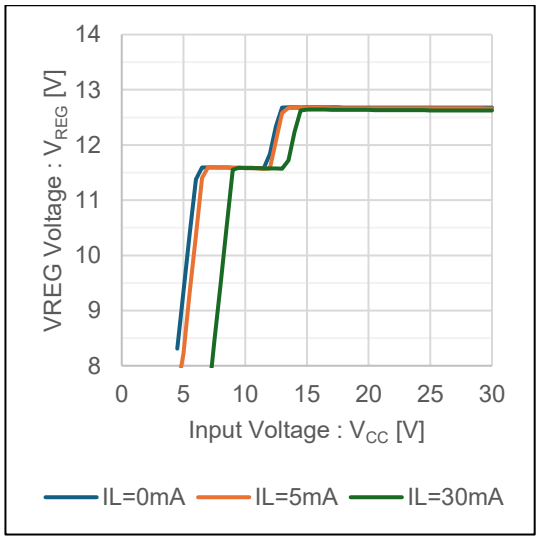


Figure 27. V_{REG} Voltage vs Input Voltage at Different Load Currents

Typical Performance Curves (Reference Data) - continued

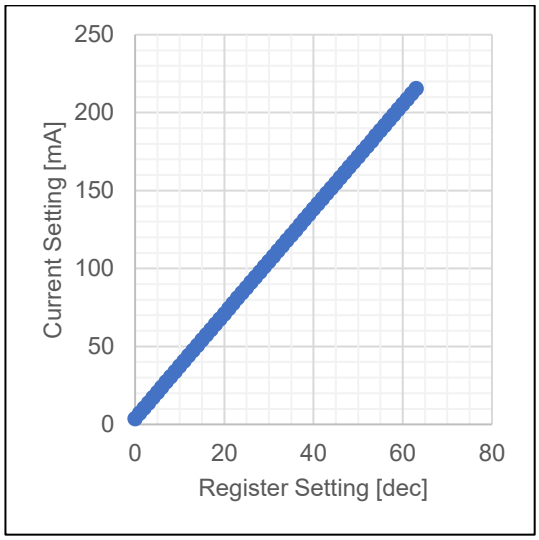


Figure 28. Current Setting vs Register Setting (SR_SO_R_1, SR_SO_R_1_2, SR_SO_F_1_2, SR_SI_F_1, SR_SI_F_1_2 and SR_SI_R_1_2)

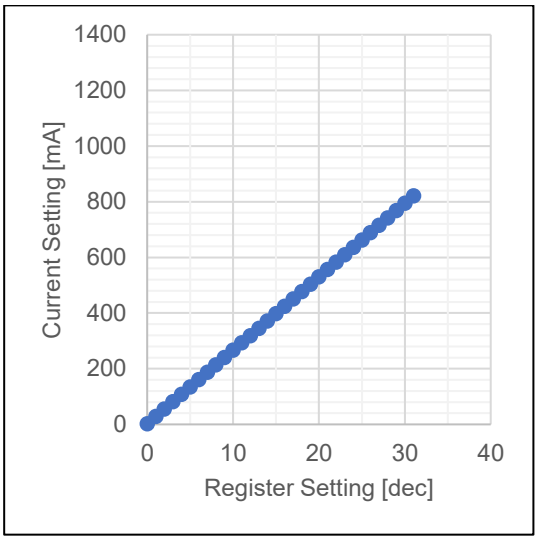


Figure 29. Current Setting vs Register Setting (SR_SO_R_1_F and SR_SO_R_3)

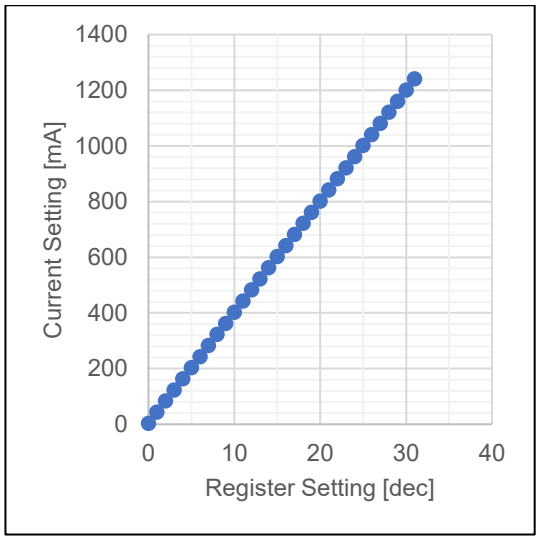


Figure 30. Current Setting vs Register Setting (SR_SO_F_3)

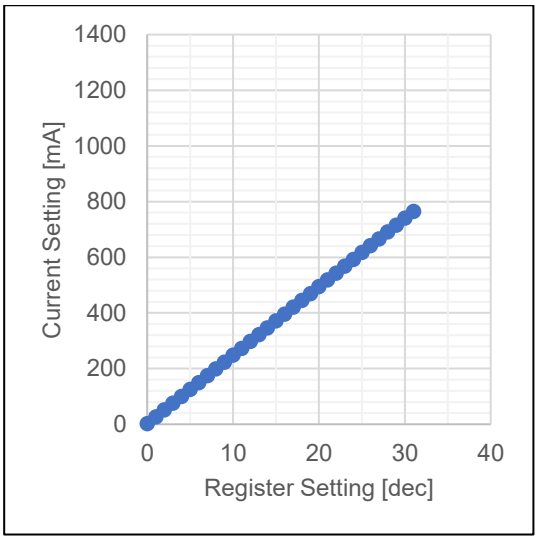


Figure 31. Current Setting vs Register Setting (SR_SI_F_1_F and SR_SI_F_3)

Typical Performance Curves (Reference Data) - continued

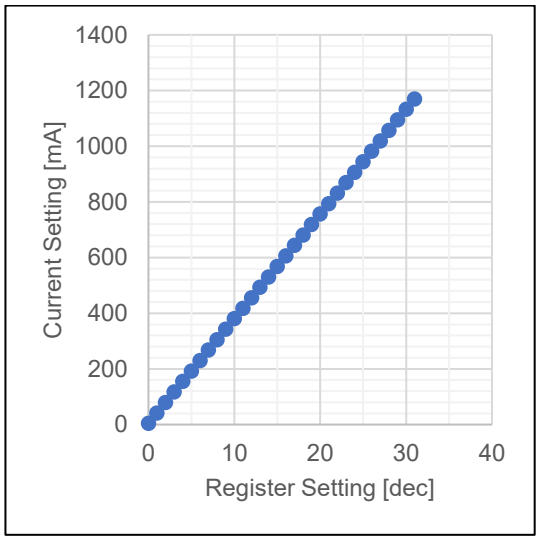


Figure 32. Current Setting vs Register Setting (SR_SI_R_3)

Characteristic Data (Reference Data)

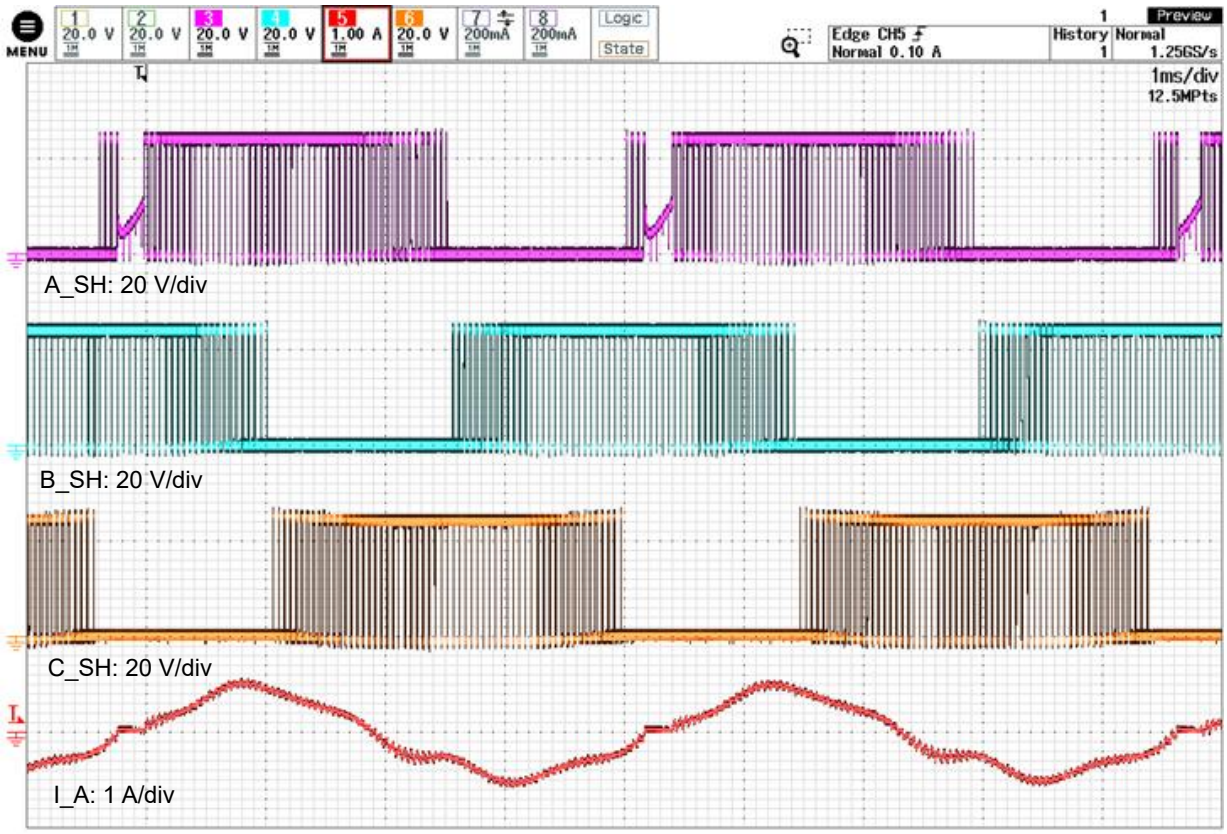


Figure 33. Sinusoidal Motor Control
(PWM frequency = 20 kHz, V_{CC} = 24 V)

Characteristic Data (Reference Data) – Continued

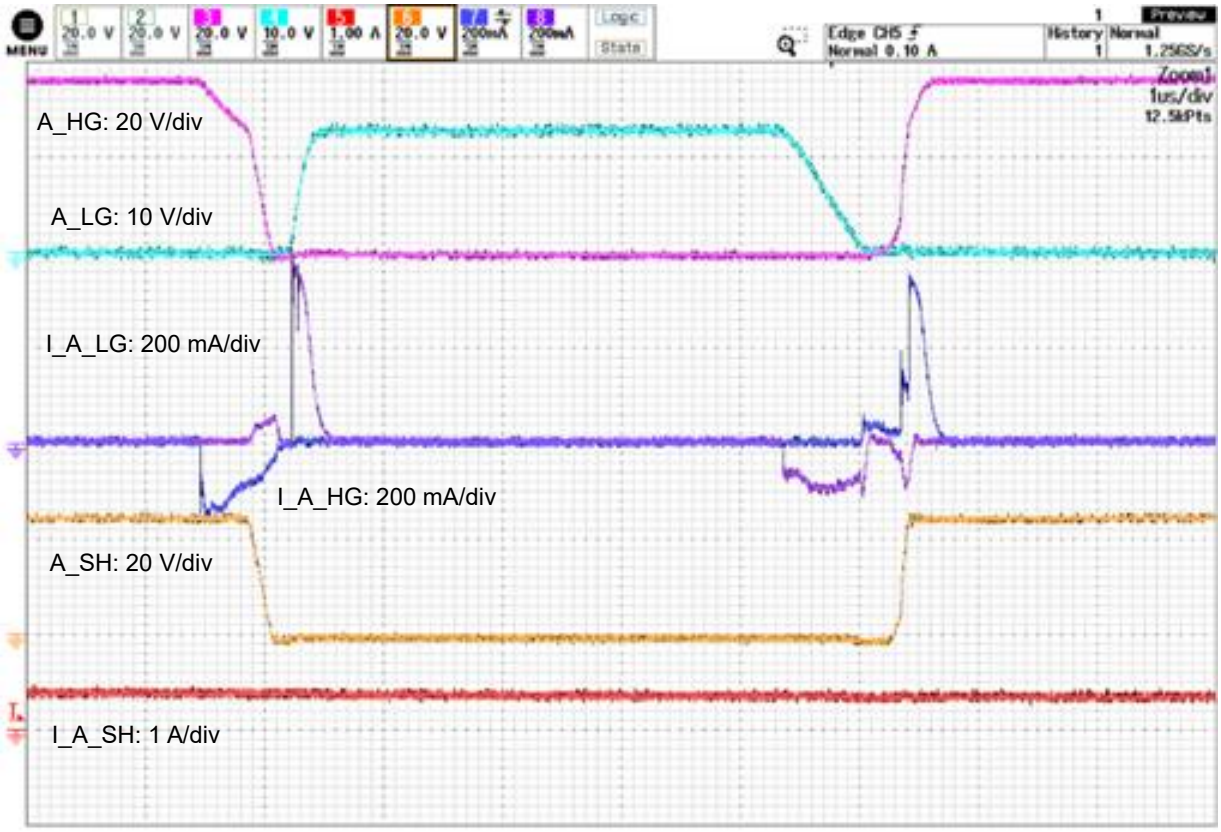


Figure 34. Gate Drive Signals of Phase A fall

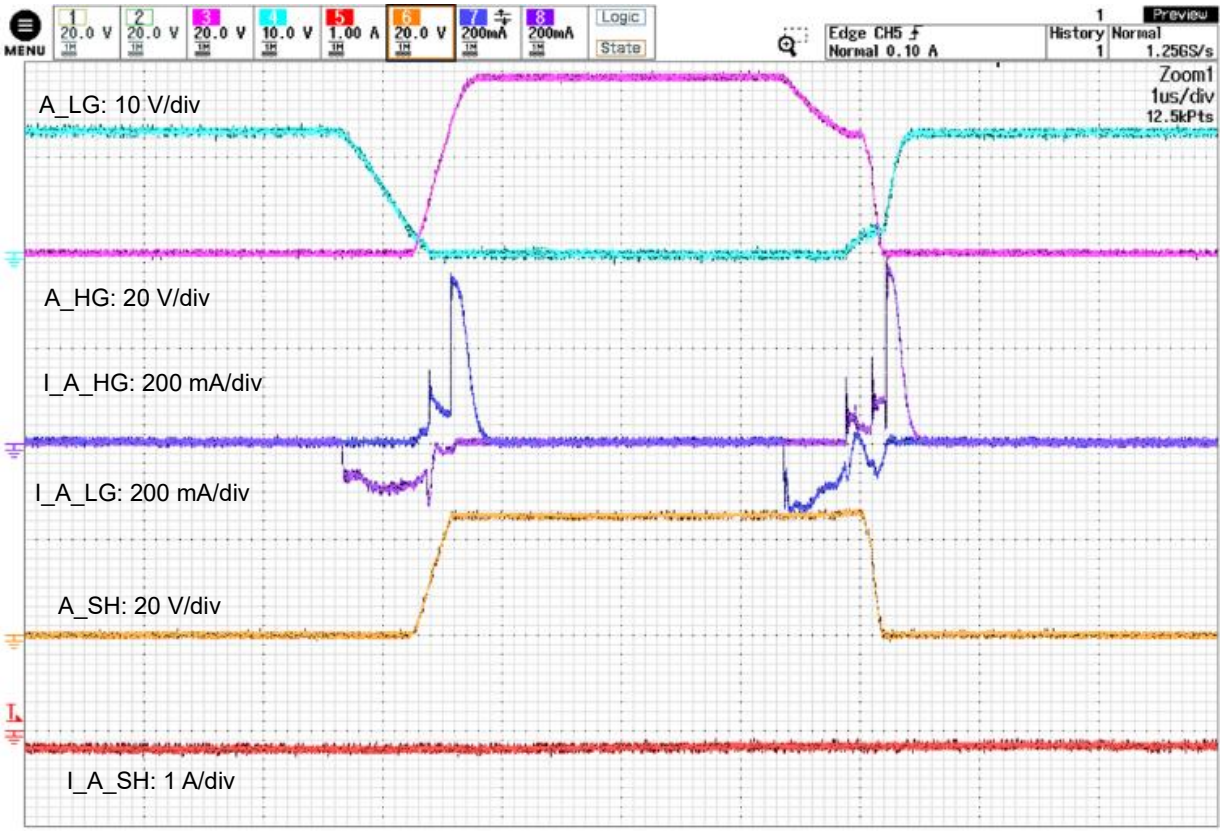


Figure 35. Gate Drive Signals of Phase A rise

Characteristic Data (Reference Data) - continued

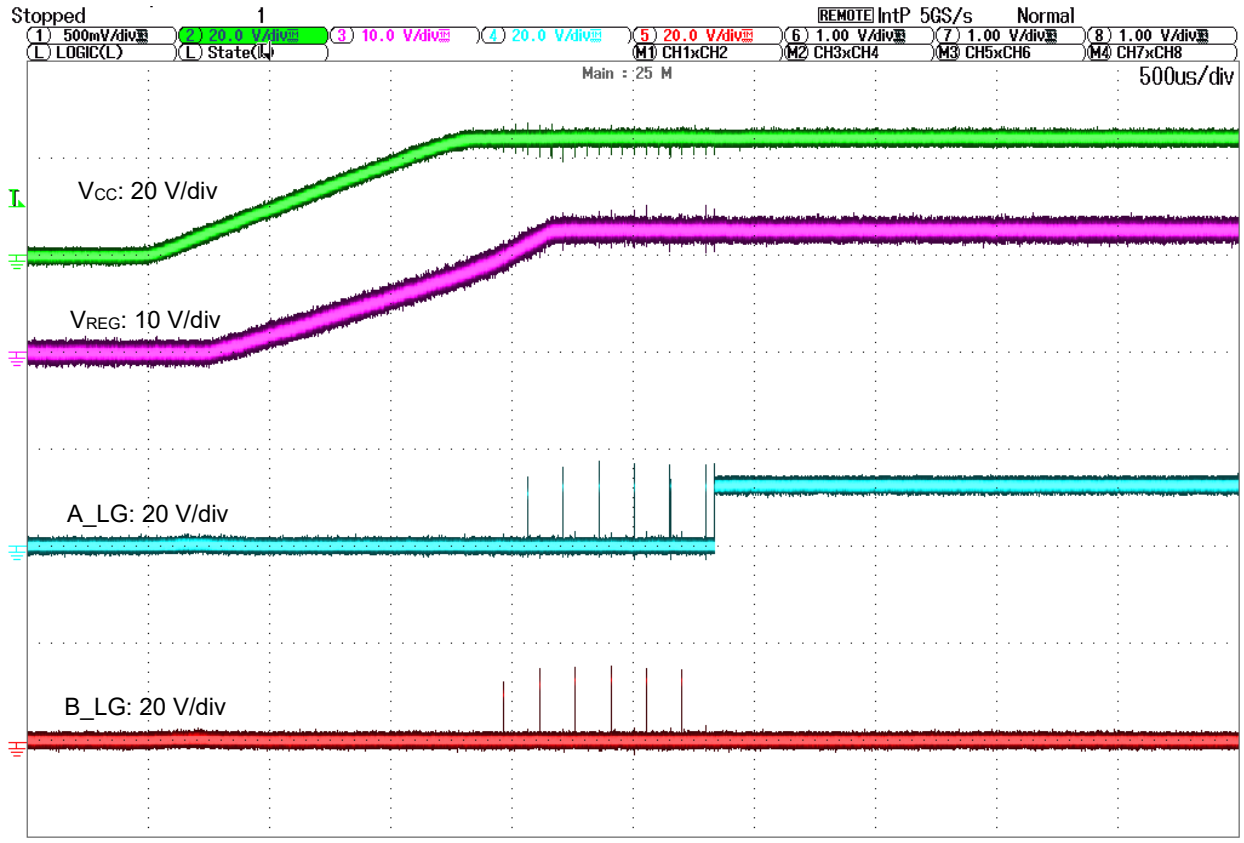


Figure 36. Start-up Sequence on Slow V_{CC}

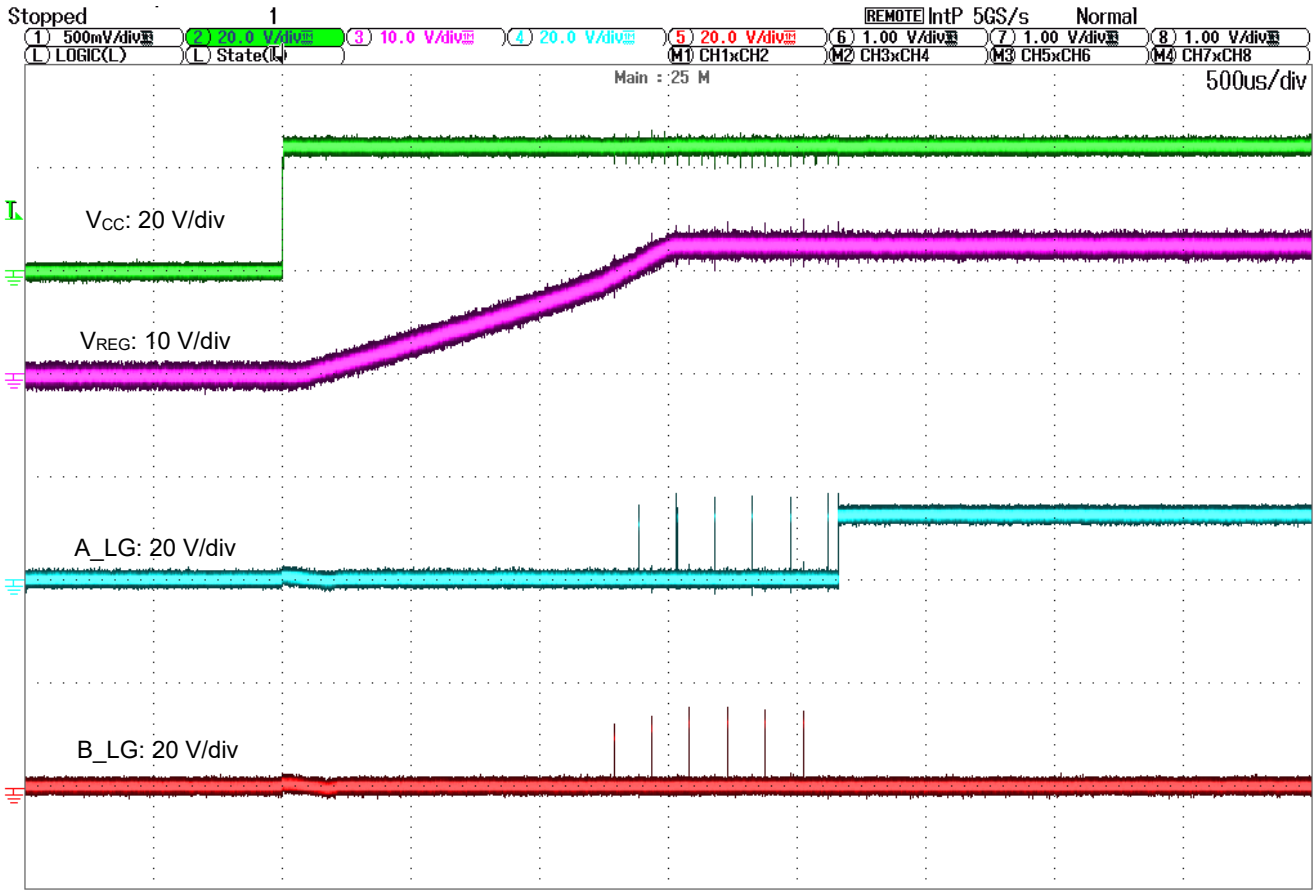


Figure 37. Start-up Sequence on Fast V_{CC}

Characteristic Data (Reference Data) - continued

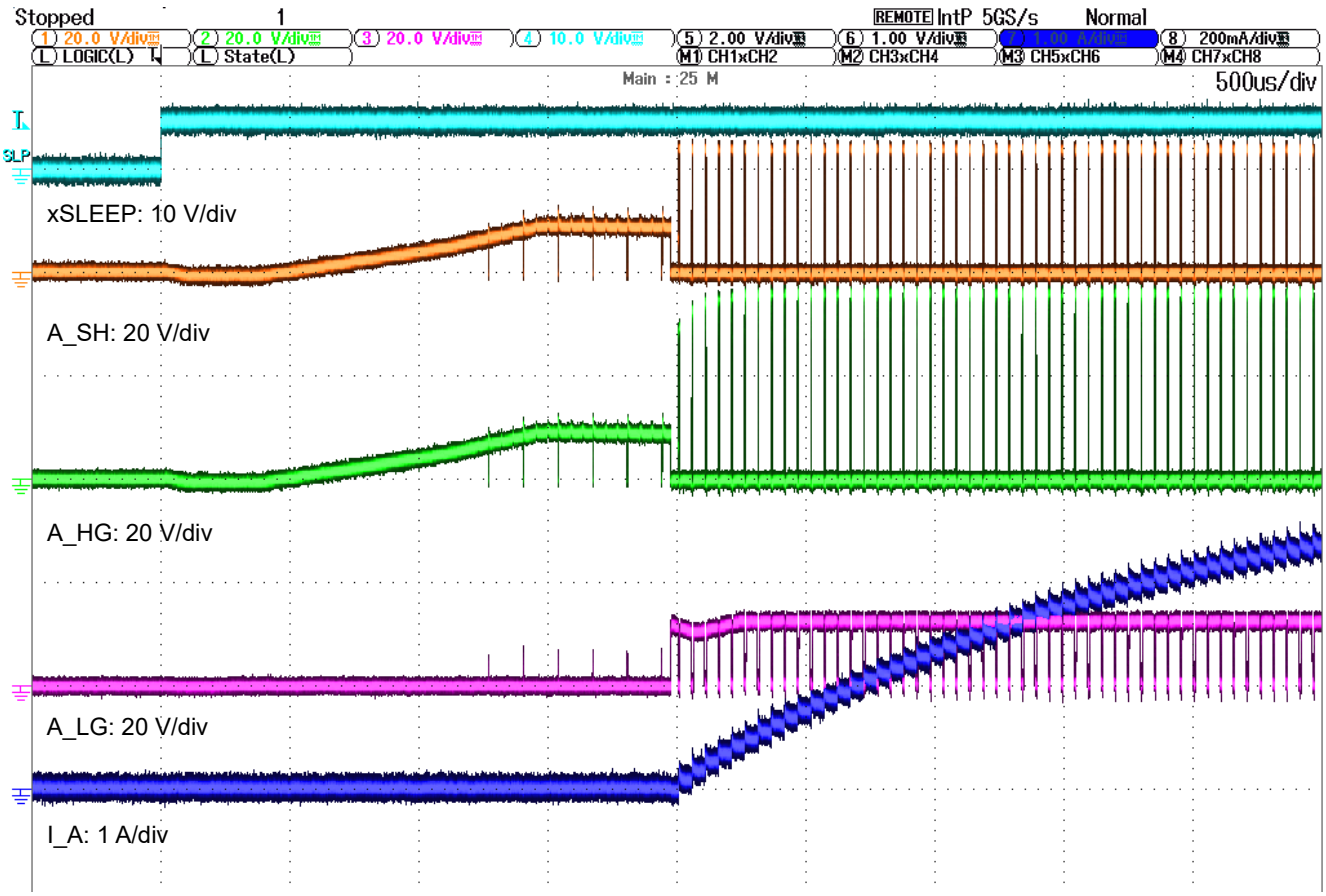


Figure 38. Sleep Recovery

ESD Ratings

Item	Value	Unit
Human Body Model (HBM)	+/-2000	V
Charged Device Model (CDM)	+/-750	V

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes - continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

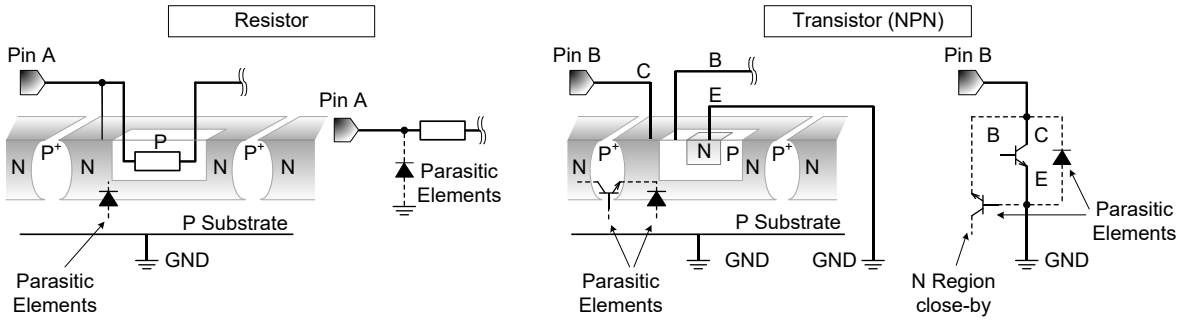


Figure 39. Example of Monolithic IC Structure

11. Ceramic Capacitor

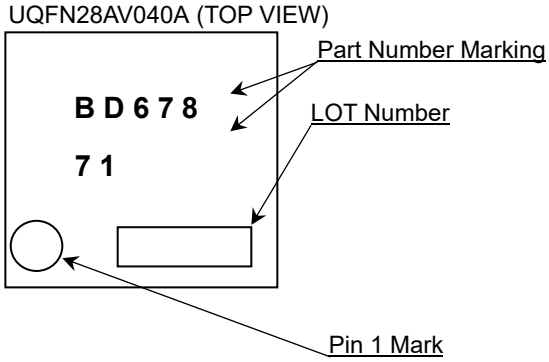
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

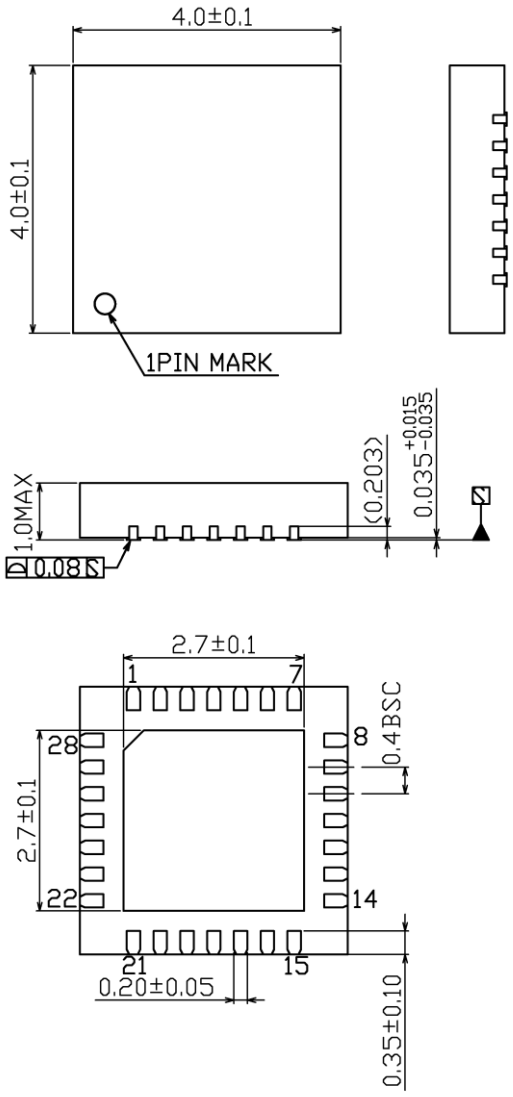
Ordering Information

Marking Diagram



Physical Dimension and Packing Information

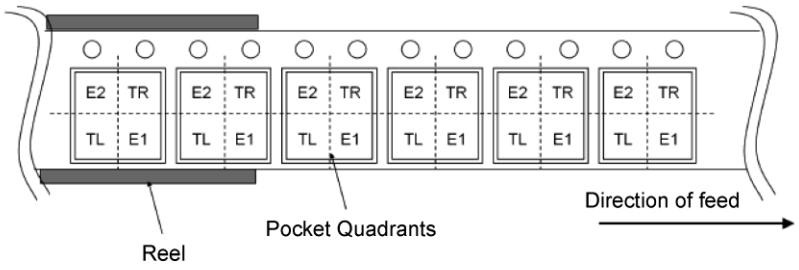
Package Name	UQFN28AV040A



(UNIT:mm)
PKG:UQFN28AV040A
Drawing No.EX001-0129

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
17.Jun.2025	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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