Datasheet

Automotive Motor Driver Series

Three-phase Brushless Motor Pre-driver for Automotive

BM16853MUF-C

General Description

BM16853MUF-C is a pre-driver IC for automotive three-phase brushless motors. This is a sensorless sinusoidal drive that eliminates the need for a Hall element for position detection. In addition, the built-in memory (OTP) enables various parameter settings to reduce the number of components required for the application.

Features

- AEC-Q100 Qualified(Note 1)
- Sensorless Sinusoidal Drive
- Speed Control (Speed Feedback)
- PWM Duty Input Speed Control
- Built-in Charge Pump
- Automatic Lead Angle Control
- Current Limit
- Rotation Direction Setup
- Various Parameter Setting with the built-in OTP
- Various Protection Functions (Motor Lock [MLP], Over Voltage [OVP], Under Voltage [UVLO, UVGP], Thermal Shutdown [TSD], Over Current [OCP], Error Frequency [EFP])

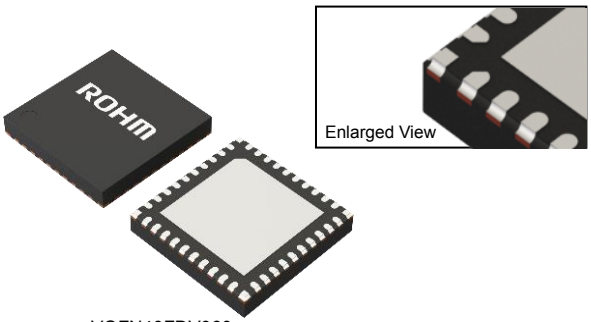
(Note 1) Grade 1

Key Specifications

- Operating Supply Voltage: 8 V to 18 V
- Output PWM Frequency: 20 kHz (Typ)
- Operating Temperature: -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
VQFN40FDV060	6.0 mm x 6.0 mm x 1.0 mm

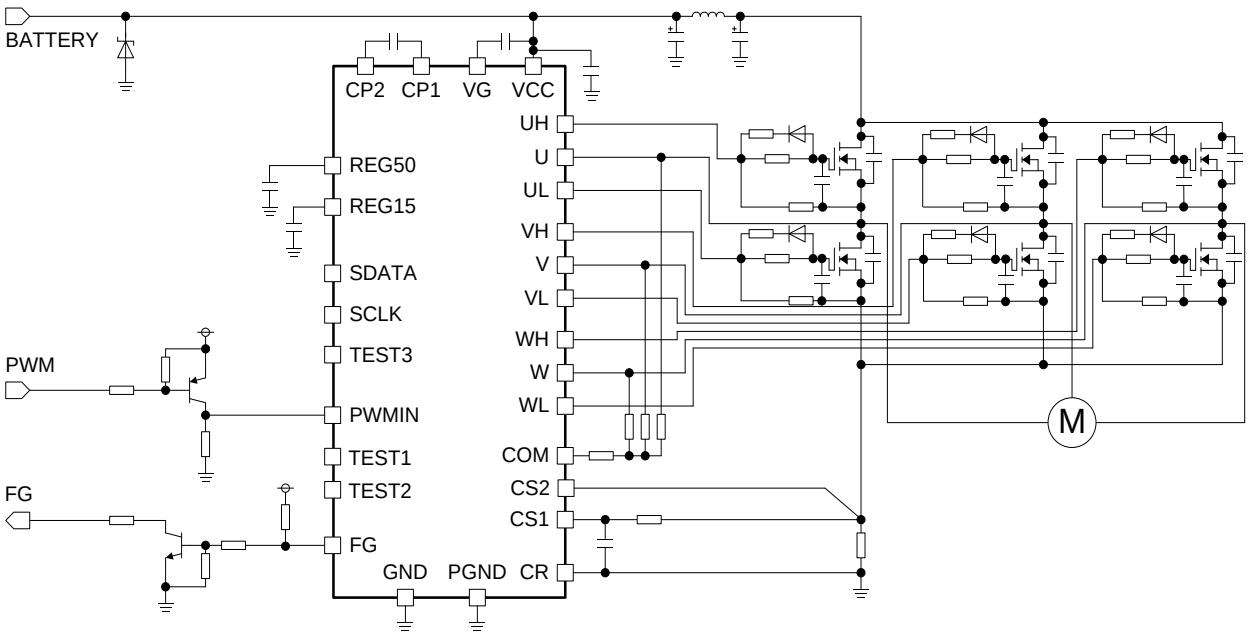


VQFN40FDV060
Wettable Flank Package

Application

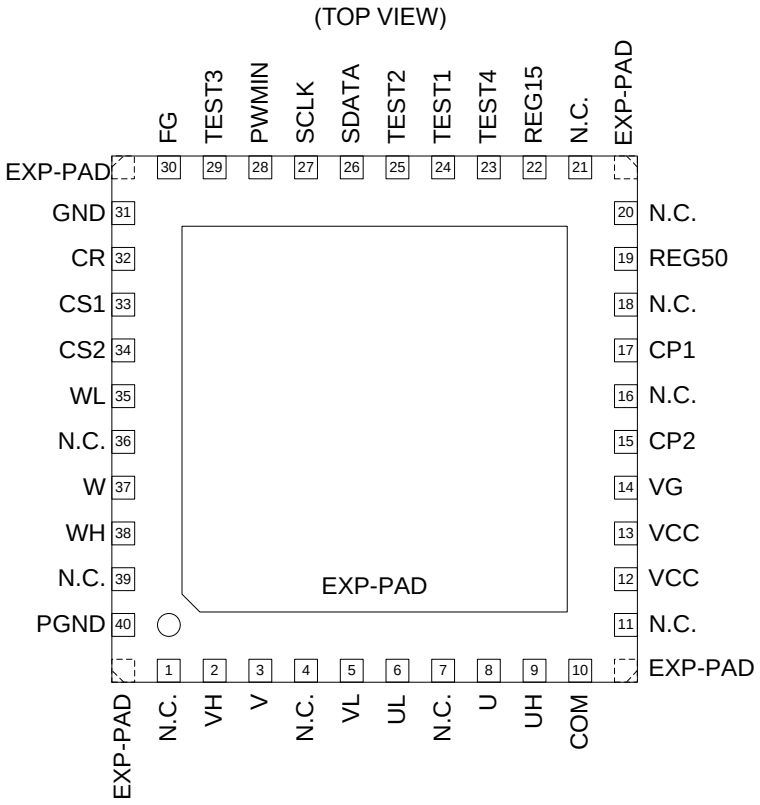
- Battery Cooling Fan Motor
- Water Pump

Typical Application Circuit



Contents

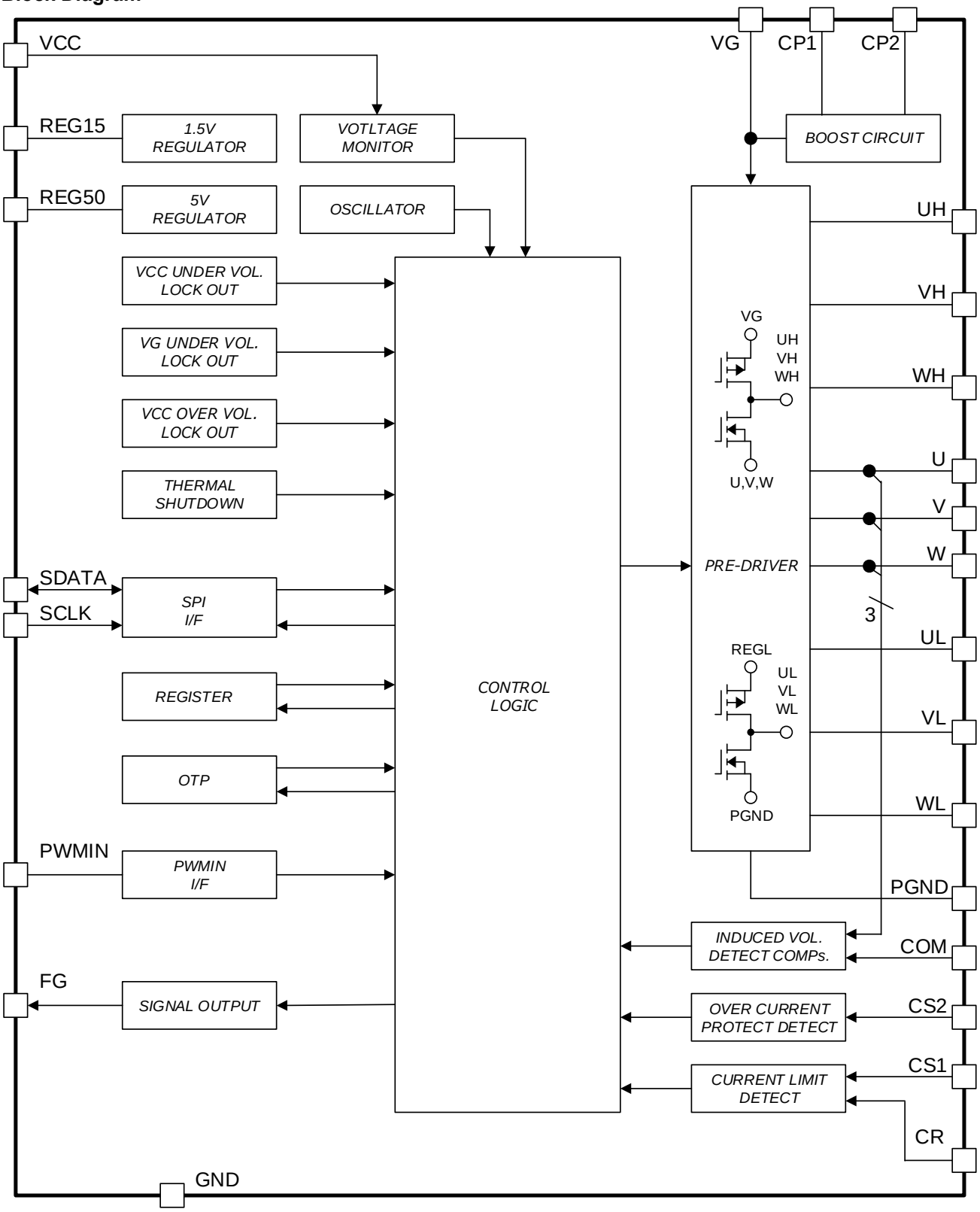
Pin Configuration



Pin Description

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	N.C.	- (This pin is open on-board wiring pattern)	21	N.C.	- (This pin is open on-board wiring pattern)
2	VH	V phase high side gate drive output	22	REG15	Reference voltage (1.5 V) output
3	V	V phase detection voltage input	23	TEST4	Test input (This pin is open on-board wiring pattern)
4	N.C.	- (This pin is open on-board wiring pattern)	24	TEST1	Test input (This pin is open on-board wiring pattern)
5	VL	V phase low side gate drive output	25	TEST2	Test input (This pin is open on-board wiring pattern)
6	UL	U phase low side gate drive output	26	SDATA	2-wire SPI data input/output
7	N.C.	- (This pin is open on-board wiring pattern)	27	SCLK	2-wire SPI clock input
8	U	U phase detection voltage input	28	PWMIN	Speed control PWM duty input
9	UH	U phase high side gate drive output	29	TEST3	Test input (This pin is open on-board wiring pattern)
10	COM	Motor midpoint voltage input	30	FG	Rotation pulse signal / Abnormal status signal output
11	N.C.	- (This pin is open on-board wiring pattern)	31	GND	Ground (small signal ground) input
12	VCC	Power supply input	32	CR	Current limit reference voltage input
13	VCC	Power supply input	33	CS1	Current limit detection voltage input
14	VG	Boost voltage output	34	CS2	Over current protection detection voltage input
15	CP2	Boost capacitor positive side connection	35	WL	W phase low side gate drive output
16	N.C.	- (This pin is open on-board wiring pattern)	36	N.C.	- (This pin is open on-board wiring pattern)
17	CP1	Boost capacitor negative side connection	37	W	W phase detection voltage input
18	N.C.	- (This pin is open on-board wiring pattern)	38	WH	W phase high side gate drive output
19	REG50	Reference voltage (5 V) output	39	N.C.	- (This pin is open on-board wiring pattern)
20	N.C.	- (This pin is open on-board wiring pattern)	40	PGND	Ground (high current ground) input
-	EXP-PAD	Connect the center EXP-PAD to GND. The center EXP-PAD and the corner EXP-PAD are shorted inside the package.			

Block Diagram



Absolute Maximum Rating

Parameter		Symbol	Rating	Unit
Power Supply Voltage	VCC	V_{CC}	-0.3 to +40	V
Input Voltage	SDATA, SCLK, CR	V_{SDATA}, V_{SCLK}, V_{CR}	-0.3 to V_{REG50} + 0.3 ≤ +7	V
	PWMIN *(Note 1)*	V_{PWMIN}		
	TEST1, TEST3	V_{TEST1}, V_{TEST3}		
	U, V, W, COM	V_{OS}, V_{COM}	-0.3 to +40	V
	CS1	V_{CS1}	-0.3 to +7	V
	CS2	V_{CS2}	-0.3 to +14.5	V
Output Voltage	REG50	V_{REG50}	-0.3 to +7	V
	REG15	V_{REG15}	-0.3 to +2	V
	SDATA, FG, TEST2, TEST4	V_{SDATA}, V_{FG}, V_{TEST2}, V_{TEST4}	-0.3 to V_{REG50} + 0.3 ≤ +7	V
	CP2, VG	V_{CP2}, V_G	V_{CC} - 0.3 to V_{CC} + 14 ≤ +49	V
	UH, VH, WH	V_{UH}, V_{VH}, V_{WH}	-0.3 to V_G + 0.3 ≤ +49	V
	UL, VL, WL, CP1	V_{UL}, V_{VL}, V_{WL}, V_{CP1}	-0.3 to +14	V
Output Current *(Note 2)*	REG50	I_{REG50}	-30 to 0	mA
	FG	I_{FG}	0 to +10	mA
	UH, VH, WH, UL, VL, WL (Average)	I_{UHA}, I_{VHA}, I_{WHA}, I_{ULA}, I_{VLA}, I_{WLA}	±10	mA
	UH, VH, WH, UL, VL, WL *(Note 3)*	I_{UH}, I_{VH}, I_{WH}, I_{UL}, I_{VL}, I_{WL}	±220	mA
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Configure external circuitry so that REG50 pin voltage is not exceeded, such as by pulling up to REG50 pin.

(Note 2) For the current items, the current inflow to IC is expressed in positive and the current outflow from IC is expressed in negative.

(Note 3) UH, VH, WH, UL, VL, WL: Pulse Width ≤ 1 µs, Pulse Duty ≤ 10 %, Tj = -40 °C to +125 °C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	8	12	18	V
Operating Temperature	Topr	-40	+25	+125	°C

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
VQFN40FDV060				
Junction to Ambient	θ_{JA}	85.5	28.1	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	10.0	7.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air). It uses a BM16853MUF-C Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5,7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics 1

(Unless otherwise specified, V_{CC} = 8 V to 18 V, Ta = -40 °C to +125 °C, CP1 - CP2 = 0.1 µF, VG - VCC = 0.1 µF)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Overall]						
Circuit Current	I_{CC}	4.5	10	20	mA	
REG50 Voltage	V_{REG50}	4.5	5.0	5.5	V	
REG15 Voltage *(Note 1)*	V_{REG15}	1.35	1.50	1.65	V	
[Booster circuit]						
VG Voltage 1	V_{G1}	2 x V_{CC} - 4.0	2 x V_{CC} - 3.0	2 x V_{CC}	V	V_{CC} = 8.0 V to 14.0 V
VG Voltage 2	V_{G2}	V_{CC} + 9.0	V_{CC} + 11.0	V_{CC} + 13.0	V	V_{CC} = 14.0 V to 18.0 V
[Pre-driver output]						
High Side Output High Voltage1	V_{OHH1}	11.7	12.9	16.0	V	I_O = -5 mA, V_{CC} = 8 V, V_{OS} = 0 V, V_{G1} = 13 V
High Side Output Low Voltage1	V_{OHL1}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 8 V, V_{OS} = 0 V, V_{G1} = 13 V
Low Side Output High Voltage1	V_{OLH1}	5.0	6.8	8.0	V	I_O= -5 mA, V_{CC} = 8 V, V_{OS} = 0 V, V_{G1} = 13 V
Low Side Output Low Voltage1	V_{OLL1}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 8 V, V_{OS} = 0 V, V_{G1} = 13 V
High Side Output High Voltage2	V_{OHH2}	19.7	20.7	24.0	V	I_O = -5 mA, V_{CC} = 12 V, V_{OS} = 0 V, V_{G1} = 21 V
High Side Output Low Voltage2	V_{OHL2}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 12 V, V_{OS} = 0 V, V_{G1} = 21 V
Low Side Output High Voltage2	V_{OLH2}	9.0	10.8	12.0	V	I_O = -5 mA, V_{CC} = 12 V, V_{OS} = 0 V, V_{G1} = 21 V
Low Side Output Low Voltage2	V_{OLL2}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 12 V, V_{OS} = 0 V, V_{G1} = 21 V
High Side Output High Voltage3	V_{OHH3}	28.0	29.8	32.0	V	I_O = -5 mA, V_{CC} = 18 V, V_{OS} = 0 V, V_{G2} = 29 V
High Side Output Low Voltage3	V_{OHL3}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 18 V, V_{OS} = 0 V, V_{G2} = 29 V
Low Side Output High Voltage3	V_{OLH3}	10.5	12.8	13.8	V	I_O = -5 mA, V_{CC} = 18 V, V_{OS} = 0 V, V_{G2} = 29 V
Low Side Output Low Voltage3	V_{OLL3}	0	0.1	0.3	V	I_O = 5 mA, V_{CC} = 18 V, V_{OS} = 0 V, V_{G2} = 29 V
Output PWM Frequency	f_{PWM}	19	20	21	kHz	
[SCLK pin]						
Input High Current	I_{SCLKH}	-2	0	+2	µA	V_{SCLK} = V_{REG50}
Input Low Current	I_{SCLKL}	-95	-50	-5	µA	V_{SCLK} = GND
High Level Input Voltage	V_{SCLKH}	V_{REG50} - 1.2	-	V_{REG50}	V	
Low Level Input Voltage	V_{SCLKL}	0	-	0.8	V	
[SDATA pin]						
Input High Current	I_{SDATAH}	-2	0	+2	µA	V_{SDATA} = V_{REG50}
Input Low Current	I_{SDATAL}	-95	-50	-5	µA	V_{SDATA} = GND
High Level Input Voltage	V_{SDATAH}	V_{REG50} - 1.2	-	V_{REG50}	V	
Low Level Input Voltage	V_{SDATAL}	0	-	0.8	V	
[PWMIN pin]						
Input High Current	I_{PWMINH}	-2	0	+2	µA	V_{PWMIN} = V_{REG50}
Input Low Current	I_{PWMINL}	-2	0	+2	µA	V_{PWMIN} = GND
High Level Input Voltage	V_{PWMINH}	V_{REG50} - 1.2	-	V_{REG50}	V	
Low Level Input Voltage	V_{PWMINL}	0	-	0.8	V	

Unless otherwise specified, characteristic values shall be the characteristics at the state of shipment from ROHM (that is, when no data is written to OTP).
For the current items, the current inflow to IC is expressed in positive and the current outflow from IC is expressed in negative.
(Note 1) REG15 does not assume an external power supply. Therefore, operation cannot be guaranteed when external loads are connected.

Electrical Characteristics 2

(Unless otherwise specified, V_{CC} = 8 V to 18 V, Ta = -40 °C to +125 °C, CP1 - CP2 = 0.1 µF, VG - VCC = 0.1 µF)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[FG pin]						
Output Low Voltage	V_{FGL}	0	0.1	0.3	V	I_{FG} = +3 mA
Output Leak Current	I_{FGLEAK}	-	-	10	µA	V_{FG} = V_{REG50}
[Current Limit (CS1)]						
Input Current 1	I_{CS11}	1.0	4.2	8.4	µA	V_{CS1} = 1 V, V_{CR} = 0 V
Input Current 2	I_{CS12}	-2	0	+2	µA	V_{CS1} = 0 V, V_{CR} = 0 V
Detection Voltage	V_{CL}	98.9	104.1	109.3	mV	Tj = 25 °C
[Over Current Protection (CS2)]						
Input Current 1	I_{CS21}	-14	-3.9	0	µA	V_{CS2} = 1 V, V_{CR} = 0 V
Input Current 2	I_{CS22}	-15	-4.9	0	µA	V_{CS2} = 0 V, V_{CR} = 0 V
Detection Voltage	V_{OCP}	190	200	210	mV	Tj = 25 °C
[Under Voltage Lock Out (VCC)]						
Release Voltage	V_{UVVCH}	6.5	7.0	7.5	V	
Detection Voltage	V_{UVVCL}	5.5	6.0	6.5	V	
[Under Voltage Protection (VG)]						
Detection/Release Voltage	V_{UVVG}	V_{CC} + 2.0	V_{CC} + 3.0	V_{CC} + 4.0	V	
[Over Voltage Protection (VCC)]						
Release Voltage 1	V_{OVL1}	18.4	20.0	21.6	V	OVP_THR_SEL = 0h
Release Voltage 2	V_{OVL2}	26.7	29.0	31.3	V	OVP_THR_SEL = 1h
Detection Voltage 1	V_{OVH1}	20.2	22.0	23.8	V	OVP_THR_SEL = 0h
Detection Voltage 2	V_{OVH2}	28.5	31.0	33.5	V	OVP_THR_SEL = 1h
[Motor Lock Protection (MLP)]						
Detection Time	t_{LK_DET}	0.95	1.00	1.05	s	
[Various Protection]						
Protected Time*(Note 1)*	t_{PRT}	4.75	5.00	5.25	s	

Unless otherwise specified, characteristic values shall be the characteristics at the state of shipment from ROHM (that is, when no data is written to OTP).
For the current items, the current inflow to IC is expressed in positive and the current outflow from IC is expressed in negative.
(Note 1) Motor Lock Protection (MLP), Low Rotation Error Protection, High Rotation Error Protection, Over Voltage Protection (OVP), Thermal Shutdown (TSD), Over Current Protection (OCP).

Typical Performance Curves (Reference Data)

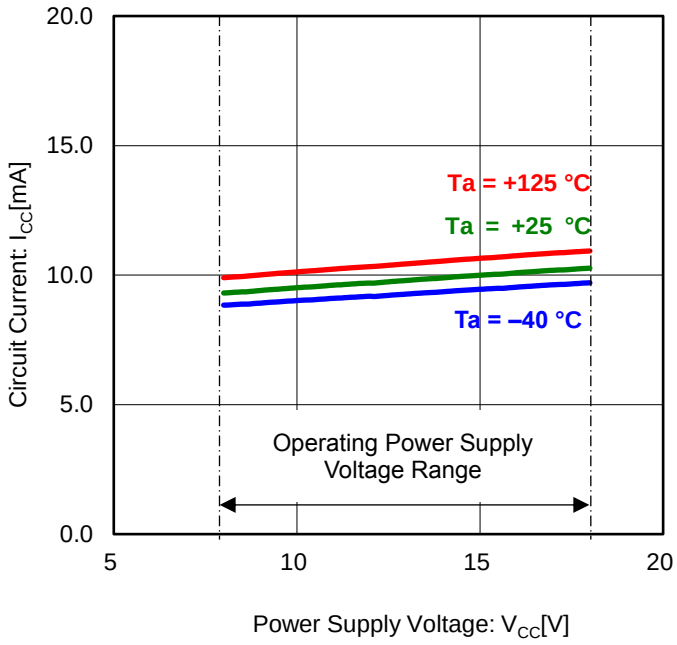


Figure 1. Circuit Current vs Power Supply Voltage

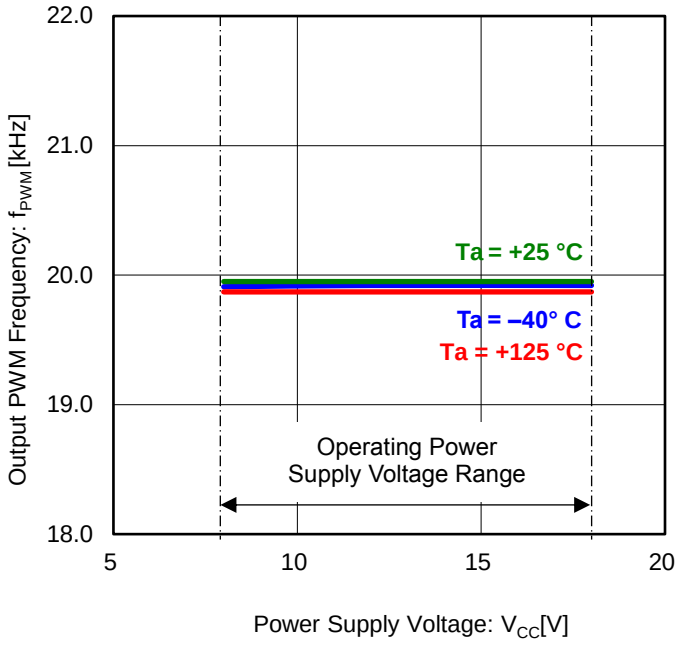


Figure 2. Output PWM Frequency vs Power Supply Voltage

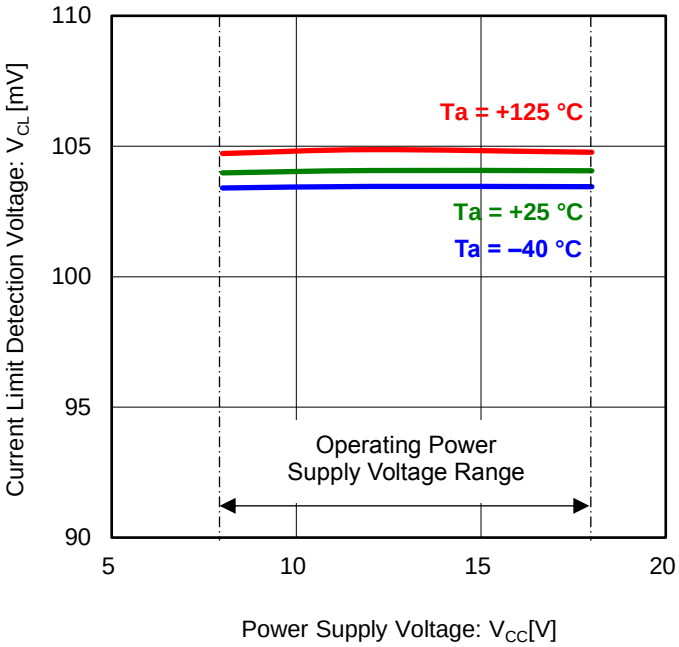


Figure 3. Current Limit Detection Voltage vs Power Supply Voltage

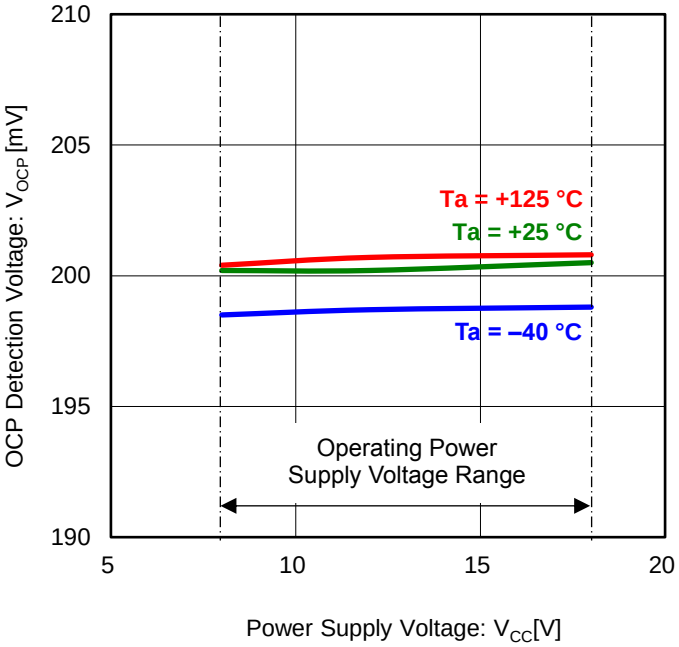
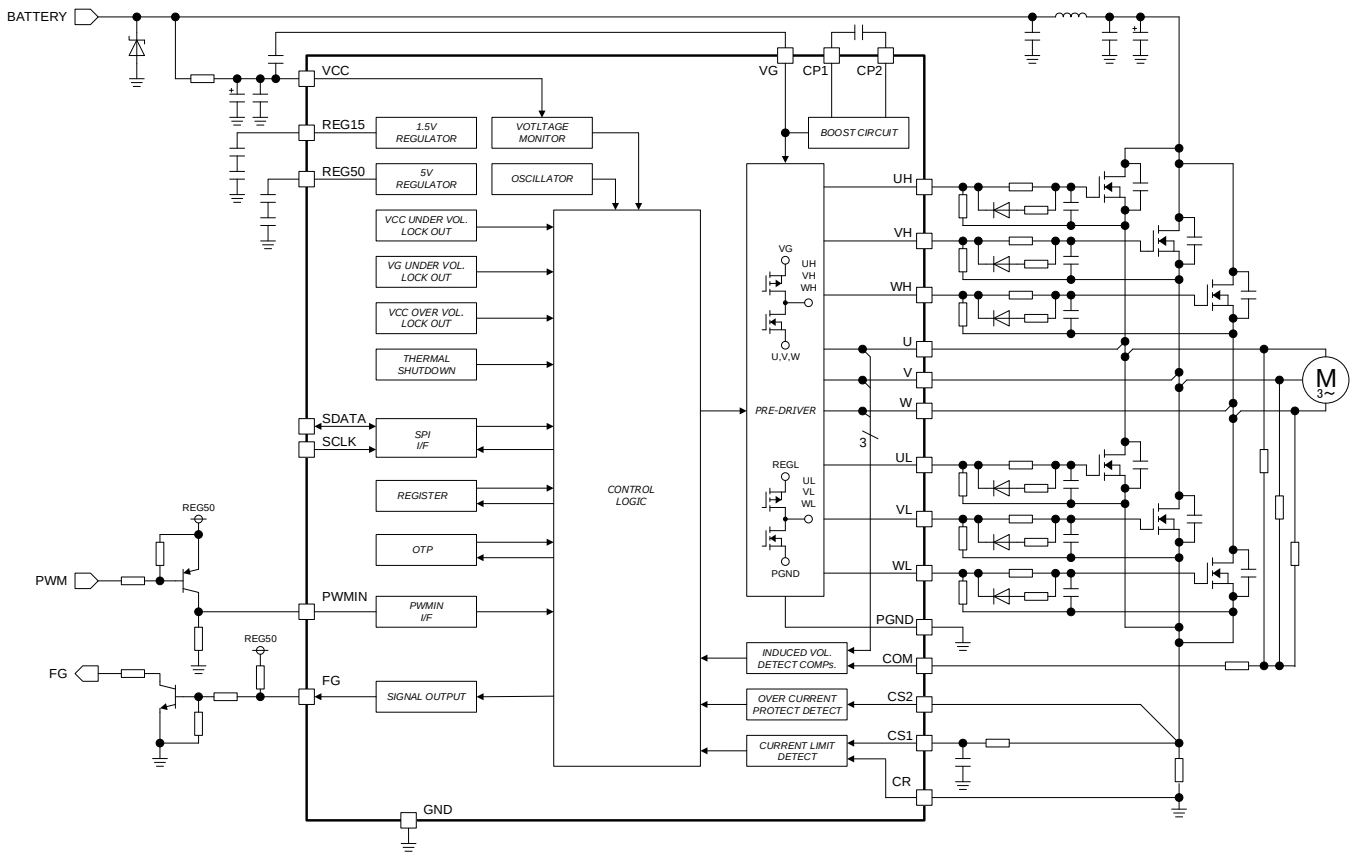


Figure 4. Over Current Protection Detection Voltage vs Power Supply Voltage

Application Example



Board Design Note

1. The IC power supply, the IC ground, the motor power, and the motor ground wires should be as thick as possible.
2. The ground wire on IC should be located near the ground connector on PCB board.
3. Place the bypass capacitor attached to VCC pin and external FET as close to VCC pin and external FET as possible.

Application Circuit Design Note

1. **Power Supply Input Pin (VCC)**
   Place a ceramic capacitor of about 0.01 µF to 0.1 µF in parallel with the electrolytic capacitor to reduce the AC impedance of the power supply over wide frequency bandwidth.
   If there is a possibility that VCC fluctuates due to the back electromotive force of the motor or PWM switching noises, etc., be sure to place a bypass capacitor as close to the pin as possible and adjust it so that VCC is stable. When using motors with large current or large counter electromotive force, increase the capacitance of the bypass capacitor as necessary. Be careful on VCC to not exceed the absolute maximum rating. It is also effective to install a Zener diode that does not exceed the absolute maximum rating. Also, note that IC may be damaged if applied voltage to VCC and GND pins are reversed.
   Place the bypass capacitor as close as possible to the VCC pin and external FET.

2. **Ground Input Pins (GND, PGND)**
   In order to reduce the noise caused by the switching current and to stabilize the internal reference voltage, the wiring impedance from this pin should be as low as possible so that it is the lowest potential in any operating condition. In addition, avoid having common-impedance with other devices' GND line. For applications, PGND and GND connection of the components are described as the recommended connection. IC power supply, IC ground, motor power, and motor ground wires should be as thick as possible. Also, IC ground wire should be located near the ground connector of the PCB board.

3. **Boosted Pins (CP1, CP2, VG)**
   A charge pump circuit is built-in for driving the upper external FET. The boost switching frequency is 125 kHz.(Typ), and by connecting a capacitor between CP1-CP2 and VCC-VG pins, boost voltage is generated at VG pin. Place the capacitor as close as possible to the VG pin to minimize voltage drop. Recommended capacitance value for each capacitor is 0.1 µF or higher.

4. **High Side Gate Drive Pins (UH, VH, WH)**
   The high side gate drive voltage of the external FET is 20.7 V (Typ). A 100 kΩ (Typ) resistor is built-in between the output pins of each phase of the high side pre-driver and the input pins of each phase detection voltage (U, V, W).

5. **Low Side Gate Drive Pins (UL, VL, WL)**
   The low side gate drive voltage of the external FET is 10.8 V (Typ). A 1000 kΩ (Typ) resistor is built-in between the output pins of each phase of the low side pre-driver and GND.

6. **Detection Voltage Input Pins (U, V, W)**
   Connect to the source-side of the high side external FET. The drive circuit of the high side external FET generates the high side pre-driver output voltage based on this pin. If this pin is used as an open circuit, an unexpected high voltage may be applied to the high side external FET which may lead to destruction. In addition, there is a possibility of swinging below GND potential because of the back electromotive force by the motor, and if it swings below -2 V, it may cause malfunction or breakdown. For preventive measures, inserting a Schottky diode into GND can avoid such unexpected IC destruction.

7. **Motor Midpoint Voltage Input Pin (COM)**
   A pseudo midpoint is created by connecting a resistor between the U, V, and W pins and the COM Pin. Recommended resistance is 390 Ω. Confirm the motor operation before deciding the resistor value. Also, consider the power dissipation of the resistor.

8. **Reference Voltage Output Pins (REG15, REG50)**
   REG50 pin is a 5 V (Typ) reference voltage output pin and REG15 pin is a 1.5 V (Typ) power supply for the logic circuits inside the IC. It is recommended to connect a capacitor of about 1 µF to 4.7 µF to both REG50 pin and REG15 pin. Do not connect anything other than a capacitor to REG15 pin.

9. **Speed Control PWM Duty Input Pin (PWMIN)**
   Speed can be controlled by the duty of PWM input to PWMIN pin. Refer to "Description of Operation: Speed Control" for the speed control setting of this product.

10. **Current Limit Detection Pins (CR, CS1)**
    CR pin and CS1 pin are the input pins for the current limit detection comparator. Design the pattern by considering the wiring with minimal noise.

11. **Over Current Detection Pin (CS2)**
    CS2 pin is the input pin for the overcurrent detection comparator. Design the pattern by considering the wiring with minimal noise.

Application Circuit Design Note - continued

12. FG output Pin (FG)

The FG signal synthesized from U, V, and W phase signal is the output from FG pin.
FG pin is an open drain output, so this pin must be pulled up to external voltage by 10 kΩ to 100 kΩ resistors.
Make sure that FG voltage and current do not exceed the absolute maximum ratings.

13. 2-wire SPI Communication Input/Output Pins (SDATA, SCLK)

Input/output pins for communicating with the IC when writing parameters to OTP.
SDATA pin is pulled up to REG50 with a 100 kΩ (Typ) resistor. SCLK pin is pulled up to REG50 with a 100 kΩ (Typ) resistor.

14. Testing Pins (TEST1, TEST2, TEST3, TEST4)

Test pin for shipment inspection.
Leave it open.

15. Non-connection Pins (N.C.)

No electrical connection with IC internal circuit.
Leave it open.

Description of Operation

1. Setting of Various Parameters and Writing of OTP (One Time Programmable Rom)

Various parameters can be set according to the characteristics of the motor and desired system behavior. The parameters can be written via one-time programming (OTP). When IC power is turned on, the data written to OTP is set in the register. If no data is written to OTP, the register default value is used. Unless otherwise specified, the following descriptions explain the operations using the initial register values.

(1) Register Map*(Note 1)*

Register Address	OTP Address	Data[15:0]																Initial
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00h	00h	-	-	-	-	-	-	-	-	PWMIN_PD	PWMIN_PU	-	-	-	PWMIN POLE	-	-	16'h0012
01h	01h	KP_0								KI_0								16'h1803
05h	05h	-	LA Position COUNT			LA Position3			LA Position2			LA Position1			LA Position0			16'h0000
08h	08h	-	-	-	-	LA ROTTH SEL2						LA ROTTH SEL1						16'h0000
09h	09h	LA Position SWEN	-	-	-	-	-	-	-	-	-	LA ROTTH SEL3						16'h0000
0Ah	0Ah	RAMP_TIMESTEP_ACC								RAMP_TIMESTEP_DEC								16'h1010
0Bh	0Bh	EC_LIMIT								-	-	RAMP_TO_PI_LEV						16'hFF04
0Ch	0Ch	-	-	-	-	-	Calc Duty 0											16'hF868
0Dh	0Dh	-	-	-	-	FR	Calc Duty 1											16'hB899
0Fh	0Fh	-	-	-	-	-	MIN*(Note 2)*											16'hF096
10h	10h	-	-	-	-	-	PWM Duty 3											16'hF0CD
11h	11h	-	-	-	-	-	MIN*(Note 3)*											16'h0096
12h	12h	-	-	-	-	-	PWM Duty 4											16'h00CD
13h	13h	-	-	-	-	-	MIN*(Note 4)*											16'h0096
14h	14h	-	-	-	-	-	RREF2IN											16'h839A
15h	15h	-	-	-	-	-	RREF2*(Note 5)*											16'h0400
17h	17h	-	-	-	-	-	RREF2*(Note 6)*											16'h0400
19h	19h	-	-	-	-	-	RREF											16'h8147
1Ah	1Ah	-	-	-	-	-	-	-	-	-	-	-	DT					16'h03CF
1Bh	1Bh	-	-	High-side PWM Mask Time						-	-	Low-side PWM Mask Time						16'h140C
1Ch	1Ch	-	-	-	-	-	-	-	-	-	-	VCL						16'h801C
1Eh	1Eh	-	-	-	Predic -tion	Min BEMF Window Width		BEMF Detect Type		Min BEMF Mask Width		MODE_SEL	START_SYNCTIMES			-	-	16'hF10D

(Note 1) The register address is used to set parameters in SPI communication. OTP address is used for OTP writing, etc.
(Note 2) Minimum speed percentage setting for Calc Duty 0.
(Note 3) Minimum speed percentage setting for PWM Duty 3.
(Note 4) Minimum speed percentage setting for PWM Duty 4.
(Note 5) Maximum speed percentage setting for RREF2IN.
(Note 6) Maximum speed percentage setting for PWM Duty 100 %.

(1) Register Map - continued

Register Address	OTP Address	Data[15:0]																Initial
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1Fh	1Fh	-	-	-	-	-	-	-	-	TOVP								16'h4032
30h	20h	TTP								TOCP								16'h3232
31h	21h	TLK								TLK_DET								16'h320A
32h	22h	-	-	-	-	-	-	-	-	TMAXRPM								16'h1032
33h	23h	-	-	-	-	-	-	-	-	TMINRPM								16'h0032
38h	28h	FG_ALEN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	16'h0F90
39h	29h	-	-	-	-	-	-	Averaging of Drive Period		-	-	-	-	-	-	-	-	16'h00B0
3Bh	2Bh	-	-	START_DUTYSLP		-	-	-	-	-	-	-	-	-	-	-	-	16'h4090
3Ch	2Ch	-	-	-	-	-	-	-	-	-	-	START_OFTIME		-	-	-	-	16'hA4F4
3Dh	2Dh	-	-	-	-	-	-	-	-	FIX_LEAD						LEAD_SET		16'h2040
3Fh	2Fh	-	-	-	-	-	-	VCLINIT										16'h01C3
42h	32h	OPEN_DSTEP								-	-	-	-	-	-	-	-	16'h3018
44h	34h	-	-	-	ROTOR_FIXTIME					-	-	-	SOSC_SET					16'h840C
46h	36h	-	-	-	-	-	-	-	-	CL_LINE_SWMASK	-	TSD_PRTMSK		OCP_PRTMSK		OVP_PRTMSK		16'h002A
47h	37h	-	-	-	-	-	-	-	-	OCP Noise Mask		OVP Noise Mask		-	-	VG_OVP_SET	OVP_THR_SEL	16'h15A0
48h	38h	-	-	-	-	-	-	-	-	-	-	MINRPMPRT_OFF		MAXRPMPRT_OFF		LKPRT_OFF		16'h80AA
49h	39h	EFP_PRTMSK	-	MIN_TIME		AR_STB_OFF	-	AL_MIN_3CYCLES	-	-	-	-	-	-	-	-	-	16'h0A07
53h	42h	-	-	-	-	-	-	CL Noise Mask		-	-	-	-	-	-	-	-	16'h1002
58h	47h	-	-	-	-	-	-	FGALTIME	FGMASKEN	-	-	-	-	-	-	-	-	16'h0158
62h	4Ah	OCP										-	-	-	-	-	-	16'hD88B

1. Parameter Setting and OTP (One Time Programmable Rom) Write - continued
(2) Parameter List

No.	Register Address [Data]	Parameter name	Function	Register Resolution
1	1Eh [5]	MODE_SEL	Normal Mode/High-Speed Startup Mode Switching Setting	1bit
2	1Eh [9:8]	BEMF Detect Type	Induced Voltage Detection Count per Electrical Angle Setting	2bit
3	1Ah [4:0]	DT	Output Dead Time Setting	5bit
4	1Bh [13:8]	High-side PWM Mask Time	Upper PWM Mask Time Setting for Induced Voltage Detection	6bit
5	1Bh [5:0]	Low-side PWM Mask Time	Lower PWM Mask Time Setting for Induced Voltage Detection	6bit
6	39h [9:8]	Averaging of Drive Period	Induced Voltage Detection Cycle Averaging Setting	2bit
7	1Eh [12]	Prediction Function of Motor Period	Induced Voltage Detection Cycle Prediction Switching	1bit
8	1Eh [11:10]	Min BEMF Window Width	Minimum Window Width Setting for Induced Voltage Detection	2bit
9	1Eh [7:6]	Min BEMF Mask Width	Minimum Mask Width Setting for Induced Voltage Detection	2bit
10	3Dh [1:0]	LEAD_SET	Automatic Lead Angle/Fixed Lead Angle Switching Setting	2bit
11	3Dh [7:2]	FIX_LEAD	Fixed Lead Angle Setting	6bit
12	05h [2:0]	LA Position0	Automatic Lead Angle Current Phase Determination Timing Setting 0	3bit
13	05h [5:3]	LA Position1	Automatic Lead Angle Current Phase Determination Timing Setting 1	3bit
14	05h [8:6]	LA Position2	Automatic Lead Angle Current Phase Determination Timing Setting 2	3bit
15	05h [11:9]	LA Position3	Automatic Lead Angle Current Phase Determination Timing Setting 3	3bit
16	09h [15]	LA Position SWEN	Current Phase Determination Timing Switching Disable Setting	1bit
17	05h [14:12]	LA Position COUNT	Current Phase Determination Timing Switching Threshold Count Setting	3bit
18	08h [5:0]	LA ROTTH SEL 1	Current Phase Determination Timing Switching Rotation Speed Setting 1	6bit
19	08h [11:6]	LA ROTTH SEL 2	Current Phase Determination Timing Switching Rotation Speed Setting 2	6bit
20	09h [5:0]	LA ROTTH SEL 3	Current Phase Determination Timing Switching Rotation Speed Setting 3	6bit
21	0Dh [11]	FR	Rotation Direction Setting	1bit
22	3Ch [5:4]	START_OFTIME	Idle Detection Time Setting	2bit
23	44h [12:8]	ROTOR_FIXTIME	Initial Position Fixation Time Setting	5bit
24	44h [4:0]	SOSC_SET	Acceleration Adjustment Setting during Forced Synchronization	5bit
25	1Eh [4:2]	START_SYNCTIMES	Forced Synchronization Cycle Count Setting	3bit
26	3Bh [13:12]	START_DUTYSLP	Output Duty Step Time Setting during Startup	2bit
27	46h [7]	CL_LINE_SWMASK	Current Limit Detection Path Switching Disable Setting	10bit
28	53h [9:8]	CL Noise Mask	Current Limit Malfunction Prevention Mask Time Setting	6bit
29	3Fh [9:0]	VCLINIT	Initial Value Setting for Current Limit	1bit
30	1Ch [5:0]	VCL	Current Limit Setting	2bit
31	00h [2]	PWMIN POLE	PWMIN Input Polarity Switching Setting	1bit
32	00h [6]	PWMIN_PU	PWMIN Internal Resistance Pull-Up Enable Setting	1bit
33	00h [7]	PWMIN_PD	PWMIN Internal Resistance Pull-Down Enable Setting	1bit
34	42h [15:8]	OPEN_DSTEP	Output Duty Step Time Setting during Drive-Off Command	8bit

(2) Parameter List - continued

No.	Register Address [Data]	Parameter name	Function	Resolution of register
35	19h [10:0]	RREF	Maximum Rotation Speed Setting	11bit
36	15h [10:0],17h [10:0]	RREF2	Second Maximum Rotation Speed Ratio Setting	11bit
37	14h [10:0]	RREF2IN	Second Maximum Rotation Speed Input Threshold Setting	11bit
38	0Fh [10:0], 11h [10:0], 13h [10:0]	MIN	Minimum Rotation Speed Ratio Setting	11bit
39	0Ch [10:0]	Calc Duty 0	PWMIN Input Drive OFF Judgment Threshold Setting	11bit
40	0Dh [10:0]	Calc Duty 1	PWMIN Input Drive ON Judgment Threshold Setting	11bit
41	10h [10:0]	PWM Duty 3	Minimum Rotation Speed Saturation Input Threshold Setting	11bit
42	12h [10:0]	PWM Duty 4	Minimum Rotation Speed Saturation Input Threshold Setting	11bit
43	0Ah [7:0]	RAMP_TIMESTEP_DEC	Deceleration RAMP Operation Step Time Width Setting	8bit
44	0Ah [15:8]	RAMP_TIMESTEP_ACC	Acceleration RAMP Operation Step Time Width Setting	8bit
45	0Bh [5:0]	RAMP_TO_PI_LEV	PI Switching Speed Error Threshold Setting	6bit
46	0Bh [15:8]	EC_LIMIT	Speed Error Limit Setting	8bit
47	01h [15:8]	KP_0	Speed PI Control Proportional Gain Setting	8bit
48	01h [7:0]	KI_0	Speed PI Control Integral Gain Setting	8bit
49	58h [8]	FGMASKEN	Forced Synchronization Startup FG Output Mask Setting	1bit
50	58h [9]	FGALTIME	FG Mask Release Condition Switching Setting	1bit
51	38h [15]	FG_ALEN	AL Signal FG Superimposition Switching Setting	1bit
52	49h [13:12]	MIN_TIME	AL Signal Minimum Output Time Switching Setting	2bit
53	49h [9]	AL_MIN_3CYCLES	AL Signal Minimum Output Condition Switching Setting	1bit
54	48h [1:0]	LKPRT_OFF	Lock Protection Disable Setting	2bit
55	48h [3:2]	MAXRPMPRT_OFF	High-Speed Abnormal Protection Disable Setting	2bit
56	48h [5:4]	MINRPMPRT_OFF	Low-Speed Abnormal Protection Disable Setting	2bit
57	31h [7:0]	TLK_DET	Motor Lock Detection Time Setting	8bit
58	31h [15:8]	TLK	Motor Lock Protection Time Setting	8bit
59	32h [7:0]	TMAXRPM	High-Speed Abnormal Protection Time Setting	8bit
60	33h [7:0]	TMINRPM	Low-Speed Abnormal Protection Time Setting	8bit
61	46h [3:2]	OCP_PRTMSK	Overcurrent Protection Disable Setting	2bit
62	62h [15:6]	OCP	Overcurrent Protection Detection Threshold Setting	10bit
63	30h [7:0]	TOCP	Overcurrent Protection Time Setting	8bit
64	47h [7:6]	OCP Noise Mask	Overcurrent Protection Malfunction Prevention Mask Time Setting	2bit
65	46h [5:4]	TSD_PRTMSK	Overheat Protection Disable Setting	2bit
66	30h [15:8]	TTP	Overheat Protection Time Setting	8bit
67	46h [1:0]	OVP_PRTMSK	Overvoltage Protection Disable Setting	2bit
68	1Fh [7:0]	TOVP	Overvoltage Protection Time Setting	8bit
69	47h [5:4]	OVP Noise Mask	Overvoltage Protection Malfunction Prevention Mask Time Setting	2bit
70	47h [0]	OVP_THR_SEL	Overvoltage Protection Threshold Setting	1bit
71	47h [1]	VG_OVP_SET	Overvoltage Protection Detection Boost Circuit Operation Setting	1bit
72	49h [15]	EFP_PRTMSK	Input Frequency Abnormal Protection Disable Setting	1bit
73	49h [11]	AR_STB_OFF	Standby OTP Auto Refresh Switching Setting	1bit

Description of Operation - continued

2. Sensorless Sinusoidal Drive

This is a sensorless Sinusoidal drive motor driver IC that uses sensorless drive, which eliminates the need for Hall elements to detect the rotor position, and converts the phase current of a three-phase brushless DC motor into a Sinusoidal waveform.

(1) Mode Selection

OTP setting: MODE_SEL

In the mode selection setting (MODE_SEL/register default [0h]: normal mode), normal mode and high-speed startup mode can be selected and has different settings for the following parameters: brake time at startup (normal mode setting: 350 ms, high-speed startup mode setting: 35 ms), fixed initial position time (see P.24), acceleration adjustment during forced synchronization (see P.26) and output duty step time at startup (see P.29).

Parameter name	Register Initial Value	Function	Description
MODE_SEL	0h	Mode selection setting	0h: Normal mode, 1h: High-speed startup mode

(2) Induced Voltage Detection Count Setting

OTP setting: BEMF Detect Type

The number of induced voltage detection in this section can be changed by setting the number of induced voltage detection per electric angle (BEMF detect Type/register default [1h]: 360°). When 0h is selected, the induced voltage detection is performed every 60° for the 64 electrical periods immediately after the forced synchronization startup interval, and then switches to detection every 360°. When 1h is selected, detection is performed every 360° so the effect of uneven magnetization is reduced. When 2h is selected, it detects every 60°, making it resistant to load fluctuations.

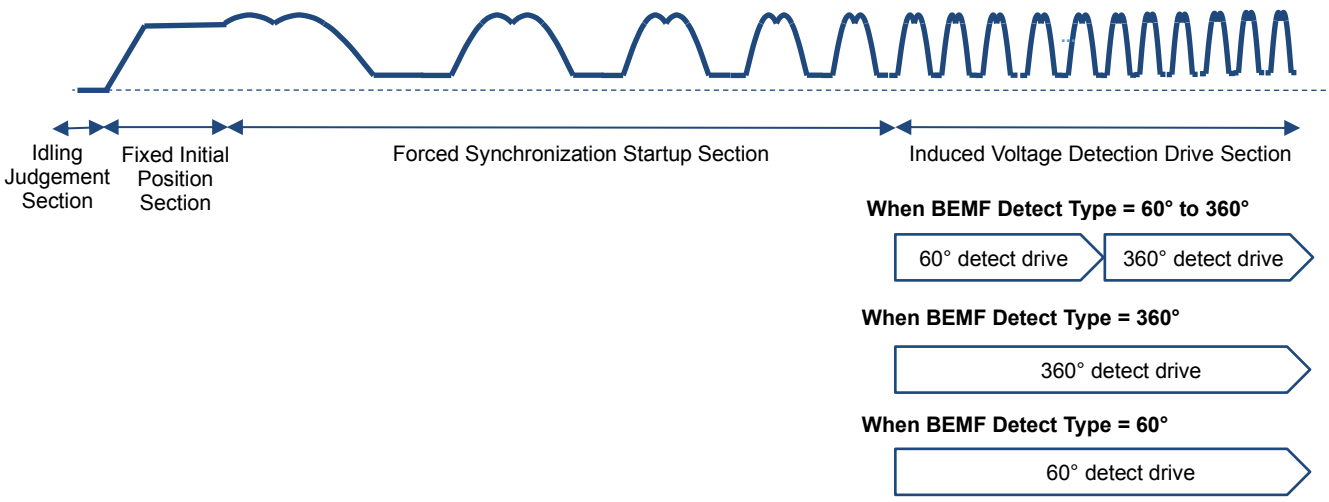


Figure 1. Number of Induced Voltage Detections at Startup

Parameter name	Register Initial Value	Function	Description
BEMF Detect Type	1h	The number of induced voltage detection per electric angle setting	0h: 60° to 360°, 1h: 360°, 2h: 60°, 3h: Prohibited setting

(2) Induced Voltage Detection Count Setting - continued

The figure below shows BEMF detection timing in the steady state drive (Back EMF Detection Driving section).

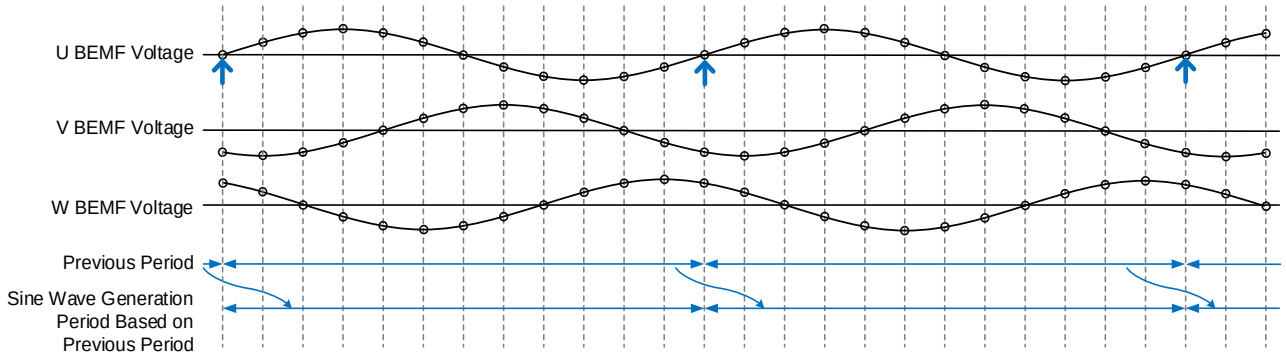


Figure 2. Number of Induced Voltage Detection during Steady State (For 360° detection)

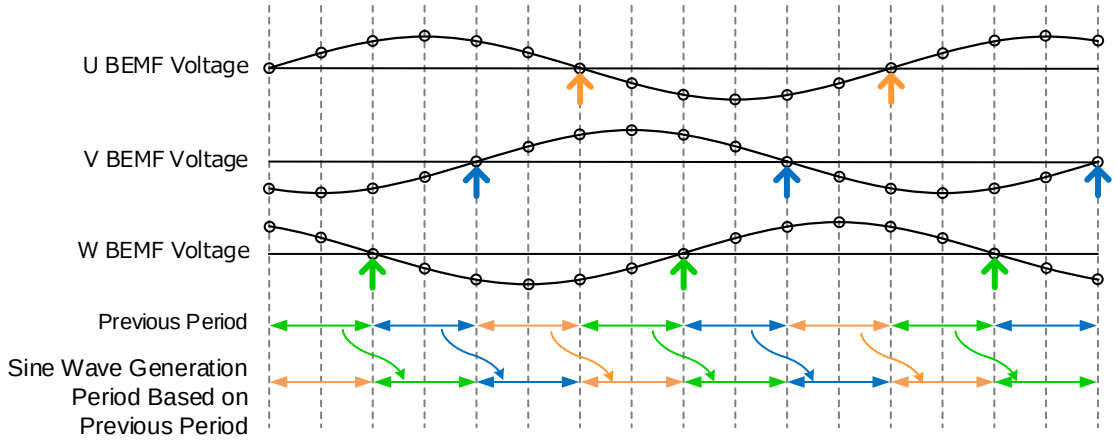


Figure 3. Number of Induced Voltage Detection during Steady State (For 60° detection)

(3) Output Dead Time Setting
OTP setting: DT

Output dead time can be set (DT/register default [0Fh]: 1.5 µs [Typ]). The configurable range is 0.5 µs to 3.1 µs, which can be set in 0.1 µs increments. The setting value follows the formula below.

$$t_{DEAD} = DT\ [4:0] \times 0.1 \geq 0.5\ \ [\mu s]$$

Setting cannot be less than 0.5 µs.
Dead time is ±15 % in the operating temperature range when set to 1.5 µs, and ±22 % in the operating temperature range when set to 1.0 µs.
Consider the operating temperature range when setting.

Parameter name	Register Initial Value	Function	Description
Dead Time (DT)	0Fh	Output dead time setting	0d to 5d: 0.5 µs 6d to 31d: 0.6 µs to 3.1 µs, 0.1 µs step

2. Sensorless Sinusoidal Drive - continued

(4) PWM Mask

OTP setting: High-side PWM Mask Time, Low-side PWM Mask Time

In the induced voltage detection section, there are PWM mask time settings that prevents induced voltage edge false detection caused by ringing when switching PWM output in other phases (High-side PWM Mask Time/register default [14h]: 4.0 µs, Low-side PWM Mask Time/register default [0Ch]: 2.4 µs). A masked section is generated at every rising and falling edge of PWM generated in the induced voltage detection section. The induced voltage detection comparator has a delay of max 5 µs. Set PWM masking time to ensure that the section from ringing convergence to 5 µs is masked. If the mask is insufficient, false detection may occur, motor operation is undesirably interrupted. Therefore, in order to ensure stable motor driving, it is necessary to identify and implement the optimum value. Since the mask time is insufficient for setting the register initial value, do not use the initial value.

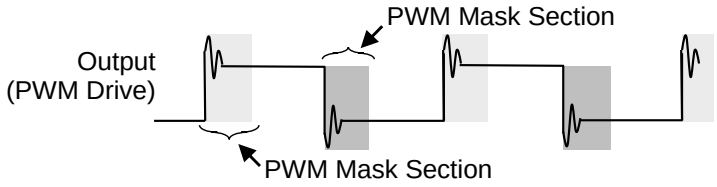


Figure 4. PWM Masking Function (Within the induced voltage detection section)

Since the induced voltage edge is detected when detection phase voltage is greater than the COM voltage, insufficient PWM masking may cause false positives during ringing. For example, detection phase is U. For High-side PWM Mask Time, assuming that VH or WH output voltage rise at IC side is 0, set it as shown in Figure 5. For Low-side PWM Mask Time, assuming that VL or WL output voltage rise at IC side is 0, set it as shown in Figure 6.

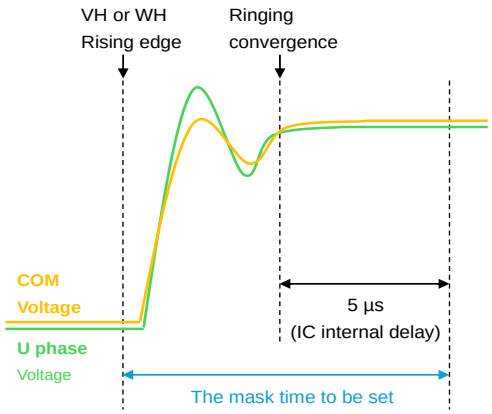


Figure 5. High-side PWM Mask Time Setting

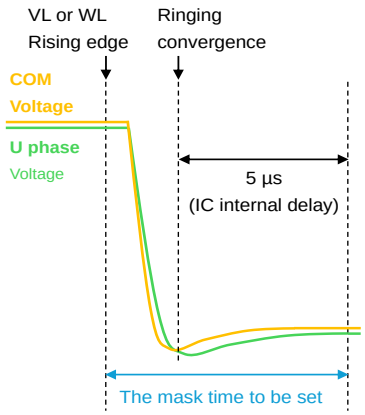


Figure 6. Low-side PWM Mask Time Setting

Parameter name	Register Initial Value	Function	Description
High-side PWM Mask Time	14h	Induced voltage detection High-side PWM mask time setting	5.0 µs to 12.6 µs, 0.2 µs step, High-side PWM Mask Time = 25d to 63d 0d to 24d: Prohibited Setting
Low-side PWM Mask Time	0Ch	Induced voltage detection Low-side PWM mask time setting	5.0 µs to 12.6 µs, 0.2 µs step, Low-side PWM Mask Time = 25d to 63d 0d to 24d: Prohibited Setting

2. Sensorless Sinusoidal Drive - continued

(5) Induced Voltage Detection Setting

OTP setting: Averaging of Drive Period, Prediction Function of Motor Period

Depending on induced voltage detection period average setting (Averaging of Drive Period/register default [0h]: no averaging), you can select whether to determine the next period from the previous induced voltage detection period or from the previous multi-period average.

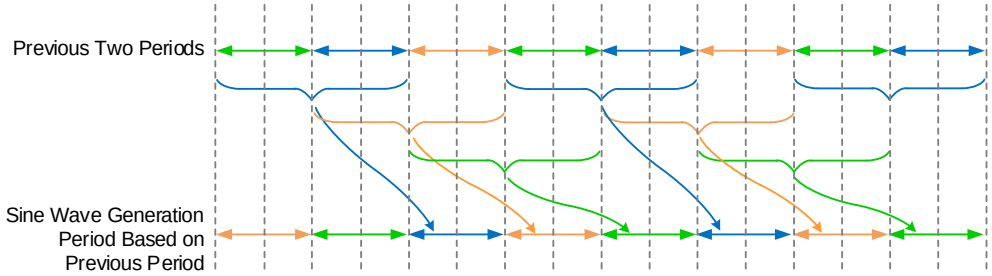


Figure 7. Induced Voltage Detection Period Average Setting (for 2-period Average)

There is a built-in function to predict the induced voltage detection period during acceleration only. The next period from the previous cycle can be selected or the acceleration trend can be predicted from the previous cycles using the induced voltage detection preiod prediction setting (Prediction Function of Motor Period/register default [1h]: Prediction enabled). Specifically, 1/2 of the difference between the last cycle and the previous cycle is subtracted from the previous cycle.

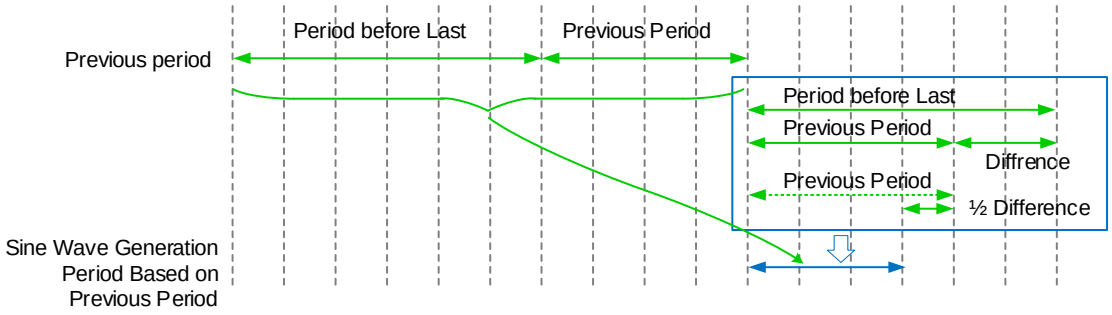


Figure 8. Drive Period Generation when Setting the Acceleration Trend Prediction

Parameter name	Register Initial Value	Function	Description
Averaging of Drive Period	0h	Induced voltage detection period averaging setting	0h: No averaging, 1h: 2-period averaging, 2h: 4-period average, 3h: 8-period average
Prediction Function of Motor Period	1h	Induced voltage detection period prediction switching	0h: Prediction disabled, 1h: Prediction enabled

2. Sensorless Sinusoidal Drive - continued

(6) Induced Voltage Detection Mask

OTP setting: Min BEMF Window Width, Min BEMF Mask Width

In the induced voltage detection window (output OFF), there are several masking settings to prevent the induced voltage edge false detection. At the beginning, there is a section for induced voltage detection mask setting that prevents the induced voltage edge false detection from coil current. During stable rotation, the mask section is automatically adjusted to the minimum mask width setting (Min BEMF Mask Width/register default [0h]: 5.625°) . The induced voltage detection window is then automatically adjusted to the minimum window width setting (Min BEMF Window Width/register default [0h]: 7.5°) or PWM3 period, whichever is greater (at stable rotation).

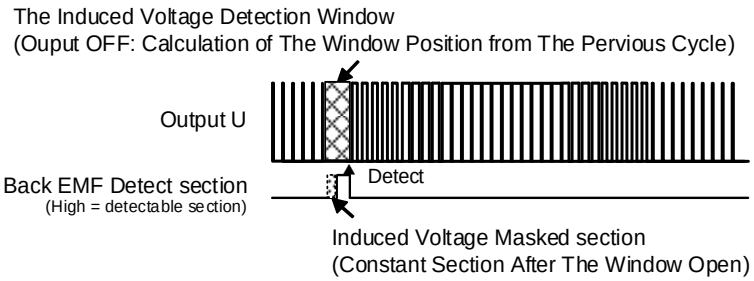
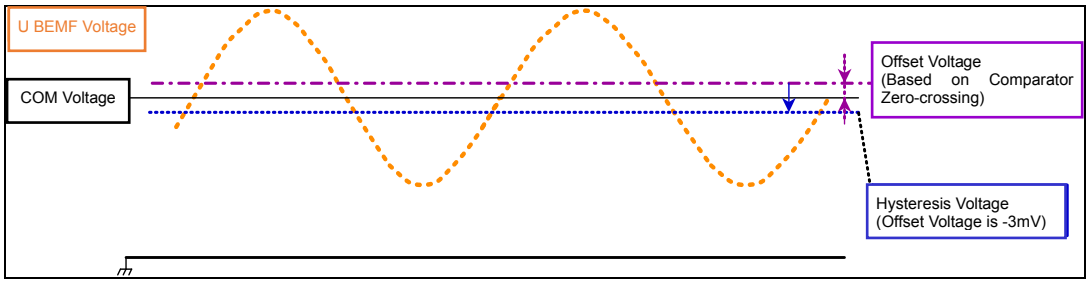


Figure 9. Induced Voltage Detection Mask Function

If a negative current remains in the coil immediately after opening the window, the U-phase voltage rises to nearly VCC. If the U-phase voltage fluctuates, false detection may occur immediately after the induced voltage detection mask is released since U voltage is greater than COM voltage used to detect the induced voltage edge. Set the induced voltage detection minimum mask width to ensure that the voltage fluctuation of the U-phase output is masked. Also, set the minimum window width greater than the minimum mask width for induced voltage detection.

Parameter name	Register Initial Value	Function	Description
Min BEMF Window Width	0h	Induced voltage detection minimum window width setting	0h, 3h: 7.5°, 1h: 11.25°, 2h: 6°
Min BEMF Mask Width	0h	Induced voltage detection minimum mask width setting	0h: 5.625°, 1h: 9.844°, 2h: 7.969°, 3h: 4.688°

The offset voltage and hysteresis voltage at Tj = 25 °C of the induced voltage detection are as comparater follows.
Use the margin below to avoid deviation in the induced voltage detection during steady rotation.



	Min	Typ	Max	Unit
Offset voltage	-10	0	+10	mV
Hysteresis voltage	-18	-3	-1	mV

Figure 10. Induced Voltage Detection Comparator Offset and Hysteresis Voltage (Reference for U-Phase)

2. Sensorless Sinusoidal Drive - continued

(7) Lead Angle Setting

OTP setting: LEAD_SET, FIX_LEAD, LA Position0, LA Position1, LA Position2, LA Position3, LA Position SWEN, LA Position COUNT, LA ROTTH SEL1, LA ROTTH SEL2, LA ROTTH SEL3

During motor drive, a built-in automatic lead angle function enables high efficiency drive by automatically matching the phase of the induced voltage generated in the coil and the phase of the coil current. From the start of the induced voltage detection section, the current phase determination timing setting (LA Position0/register default [0h]: 1/8 PWM time) determines the current polarity at the elapsed time point and adjusts the lead angle value so that it becomes zero.
For evaluation/analysis, there is a function to turn OFF the automatic lead angle setting and switch to adjustable fixed lead angle setting (LEAD_SET/register default [0h]: automatic lead angle). The lead angle adjustable range is 0° to 60° (FIX_LEAD/register default [10h]: 15.234° [Typ]).

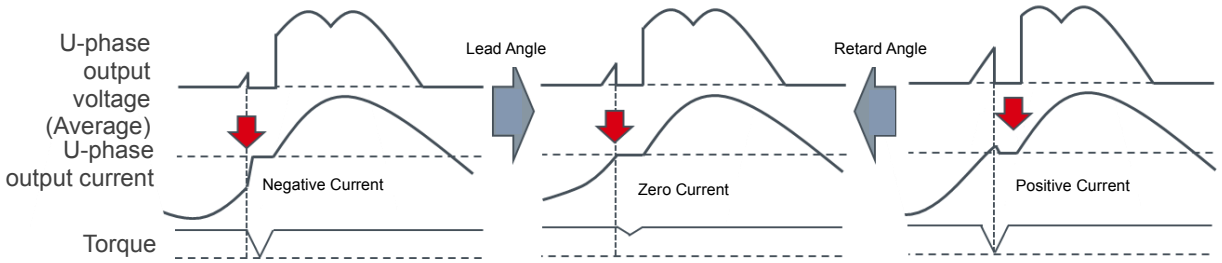


Figure 11. Automatic Lead Angle Current Phase Adjustment

The current phase determination timing can be set individually for each rotation speed region. Select the number of inflection points through the current phase determination timing switching threshold number setting (LA Position COUNT/register default [0h]: no switching), and set the number of rotations through the current phase determination timing switching rotation setting (LA ROTTH SEL1, LA ROTTH SEL2, LA ROTTH SEL3/register default [00h]: 160 rpm*(Note 1)*). The rotation speed is calculated from the induced voltage detection period. The current phase determination timing setting (LA Position1, LA Position2, LA Position3/register default [0h]: 1/8 PWM time) can be set for each divided rotation speed region.
Enable and disable of switching can be selected through current phase determination timing switching disable setting (LA Position SWEN/register default [0h]: switching disabled). When the switching is disabled, the current phase determination timing is determined by LA Position0 setting only, regardless of LA Position COUNT setting. In applications involving large load fluctuations such as sudden acceleration or deceleration, set the optimum advance angle value according to the target rotation speed.

(Note 1) The rotation speed is expressed in terms of a 10-pole motor.

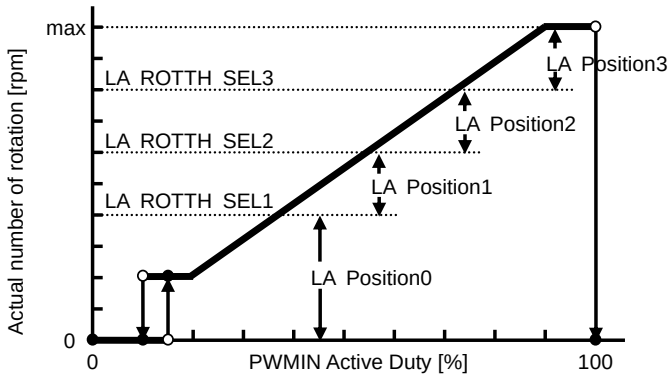


Figure 12. Current Phase Determination Timing Switching Setting

(7) Lead Angle Setting - continued

Parameter name	Register Initial Value	Function	Description
LA Type (LEAD_SET)	0h	Automatic / fixed lead angle switching setting	0h: Automatic Lead Angle, 2h: Fixed Lead Angle (Fixed at the setting of FIX_LEAD), 1h/3h: Prohibited Setting
LA Level (Fixed) (FIX_LEAD)	10h	Fixed lead angle setting	0.234° to 59.297°, 0.937° step, FIX_LEAD = 0d to 63d
LA Position0 LA Position1 LA Position2 LA Position3	0h	Automatic lead angle current phase detection timing setting	0h: 1/8 PWM time, 1h: 1/4 PWM time, 2h: 1 PWM time, 3h: 1/16 PWM time, 4h: 2 PWM time, 5h: 3 PWM time, 6h: 4 PWM time, 7h: 1/2 PWM time
LA Position SWEN	0h	Current phase determination timing switching disable setting	0h: Switching disabled, 1h: Switching enabled
LA Position COUNT	0h	Current phase determination timing switching threshold number setting	0h: No switching (Use LA Position0 only) 1h: 1 Position Switching (LA Position0 to 1) 2h: 2 Position Switching (LA Position0 to 2) 3h: 3 Position Switching (LA Position0 to 3)
LA_ROTTH_SEL1 LA_ROTTH_SEL2 LA_ROTTH_SEL3	00h	Current phase determination timing switching rotation setting	f_{ROTTHx} [Hz] = {LA ROTTH SELx + 1} * 26.666 * 2 / poles, LA ROTTH SEL1 to 3 = 0d to 63d,

2. Sensorless Sinusoidal Drive - continued

(8) Start up Sequence

OTP setting: START_OFTIME, ROTOR_FIXTIME

At startup, check the rotation of the rotor in the idle judgment section (START_OFTIME/register default [3h]: 25 ms [Typ]) and when normal rotation is detected, change the induced voltage detection drive section. When reverse rotation is detected, the output logic of the external FET is set to Low, and the rotor rotation stops. After 5 s (Typ), it will move to the idle judgment section again. Otherwise, it is judged that the rotor stopped and the fixed initial position section state is activated. In this section, the rotor is fixed at the initial position for a certain period of time (ROTOR_FIXTIME/register default [04h]: 400 ms [Typ]) after braking for 350 ms (Typ) on all phases with low output. After that, it will move to the forced synchronization startup section. In this section, the output switching cycle is gradually shortened based on the reference period for a certain number of electrical cycles*(Note 1)* and accelerates the motor. After the completion of forced synchronization startup, it transitions to the induced voltage detection drive section. In the timing chart below, the startup by turning on the power (VCC pin) is used as an example.*(Note 2)*

(Note 1) 360° electrical angle is defined as one electrical period.
(Note 2) There are two types of command that start the motor from stopped state: startup by the speed command input at normal frequency (PWMIN pin) and return from the state where the motor stopped due to the protection circuit. Both have similar behavior.

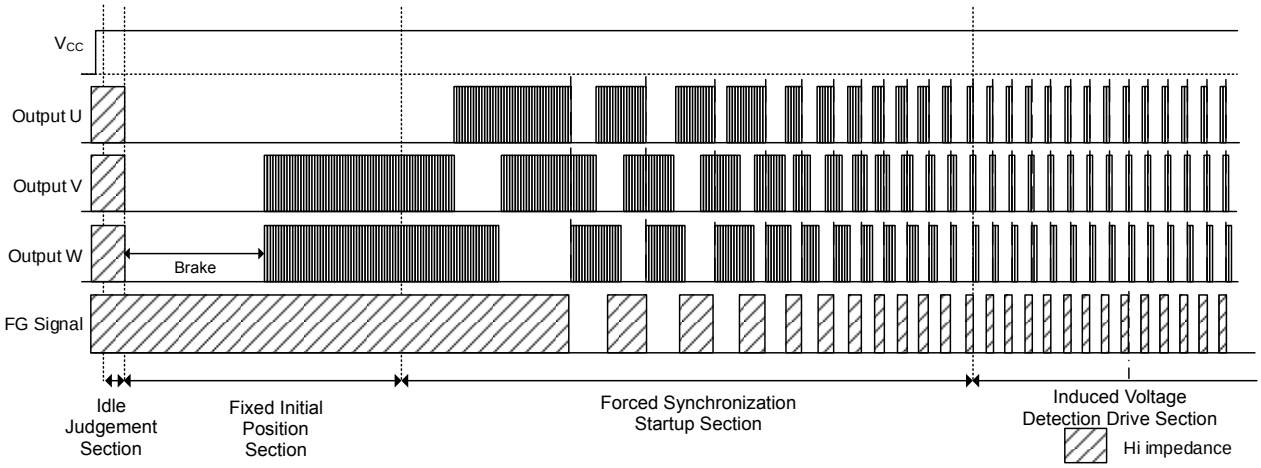


Figure 13. Output Signal (U, V, W) and FG Signal Timing Chart (FG Mask Disabled)*(Note 3)*

(Note 3) Three-phase modulation. The minimum duty section of the output signal waveform is not shown.

Driving section	Function
Idle Judgement Section	Detect rotor rotation
Fixed Initial Position Section	Fix the rotor in the initial position after braking
Forced Synchronization Startup Section	Gradually shorten the output switching cycle to a fixed number of electrical cycles to accelerate the motor
Induced Voltage Detection Drive Section	Normal operation by induced voltage detection

Parameter name	Register Initial Value	Function	Selection mode	Description
Max Rotation Judge Time (START_OFTIME)	3h	Idle judgment time setting	Normal mode High-speed startup mode	0h: 12.5 ms, 1h: 6.25 ms, 2h: 18.75 ms, 3h: 25 ms
Rotor Fix Time (ROTOR_FIXTIME)	04h	Fixed initial position time setting	Normal mode (MODE_SEL = 0h)	0 ms to 3.1 s, 100 ms step, ROTOR_FIXTIME = 0d to 31d
			High-speed startup mode (MODE_SEL = 1h)	0 ms to 344 ms, 11.1 ms step, ROTOR_FIXTIME = 0d to 31d

(8) Start up Sequence - continued

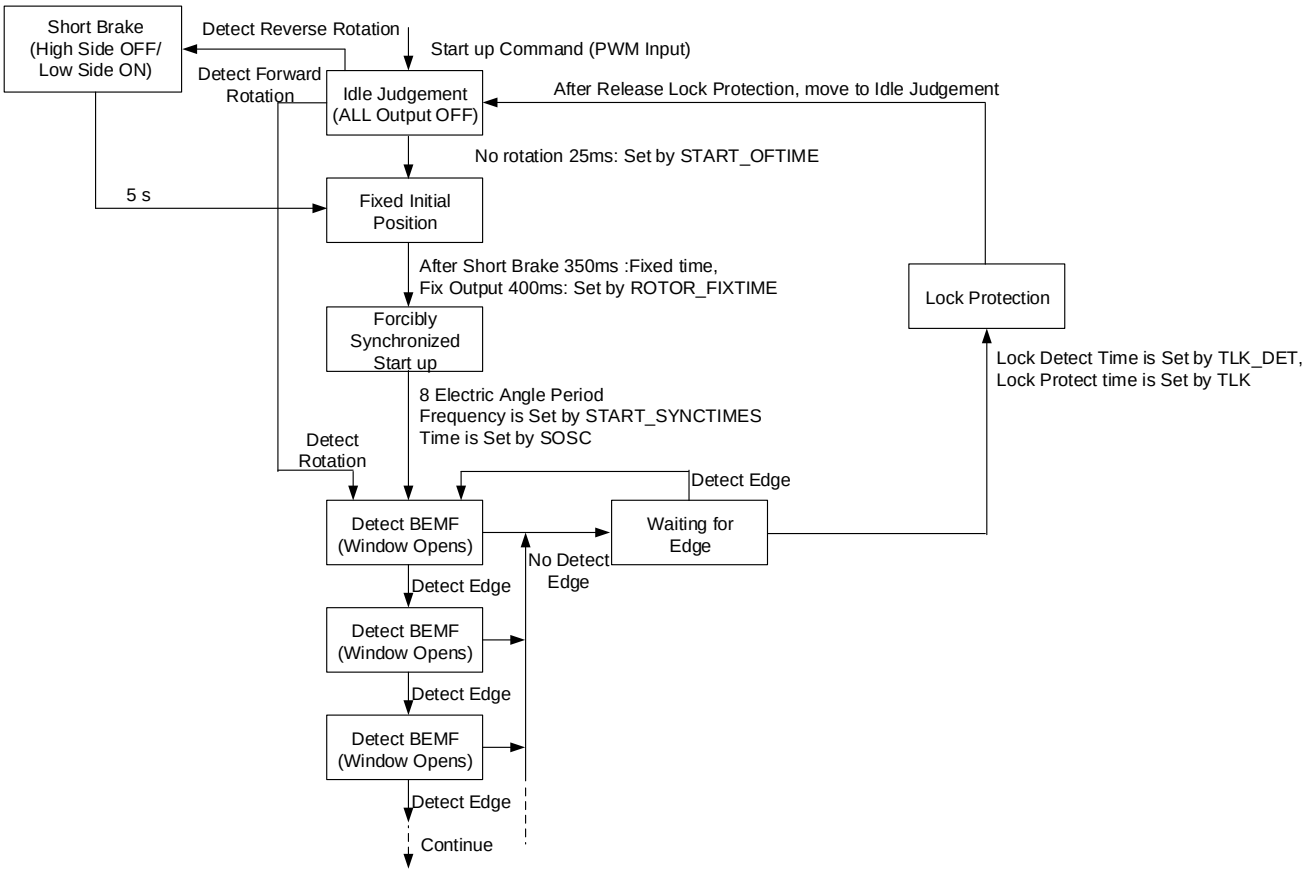


Figure 14. Startup State Diagram and Flow Chart

2. Sensorless Sinusoidal Drive - continued

(9) Frequency Setting in Forced Synchronization Startup Section

OTP setting: SOSC_SET, START_SYNCTIMES

The acceleration of the forced synchronization startup section is set by the reference period (SOSC_SET/register default [0Ch]: 5.2 µs [Typ]) and the number of electrical periods (START_SYNCTIMES/register default [3h]: 8 periods]). The acceleration depends on various characteristic parameters of the motor. Select the optimum value to ensure stable motor startup.

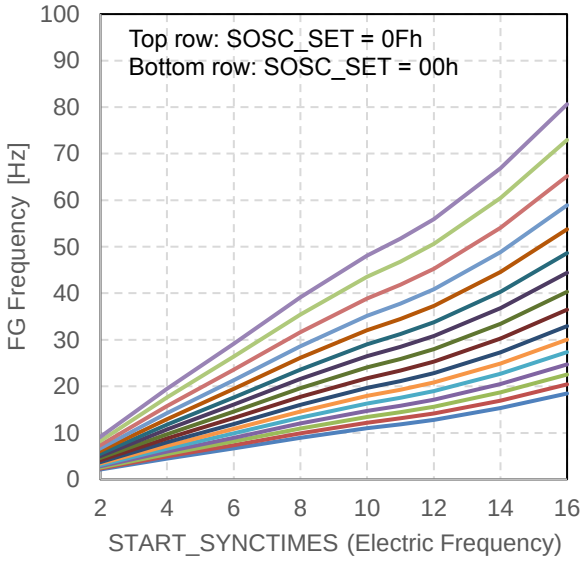


Figure 15. START_SYNCTIMES vs FG Frequency (SOSC_SET = 00h to 0Fh) (Normal mode)

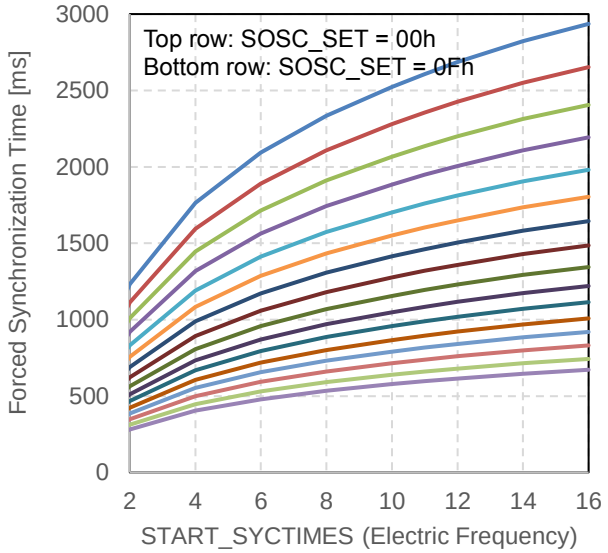


Figure 16. START_SYNCTIMES vs Forced Synchronization Time (SOSC_SET = 00h to 0Fh) (Normal mode)

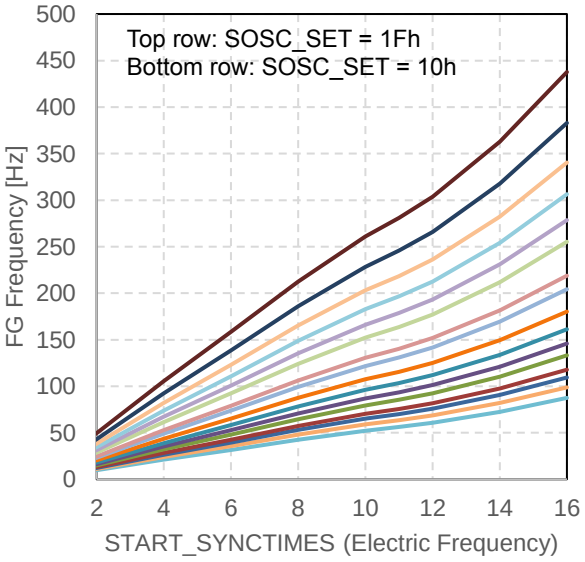


Figure 17. START_SYNCTIMES vs FG Frequency (SOSC_SET = 10h to 1Fh) (Normal mode)

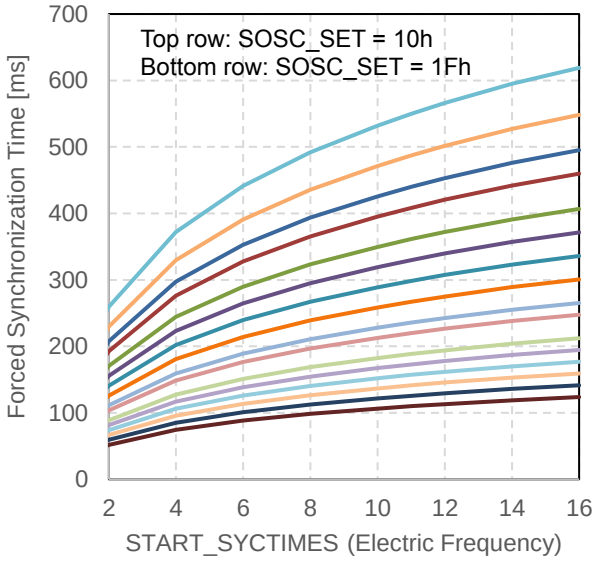


Figure 18. START_SYNCTIMES vs Forced Synchronization Time (SOSC_SET = 10h to 1Fh) (Normal mode)

(9) Frequency Setting in Forced Synchronization Startup Section - continued

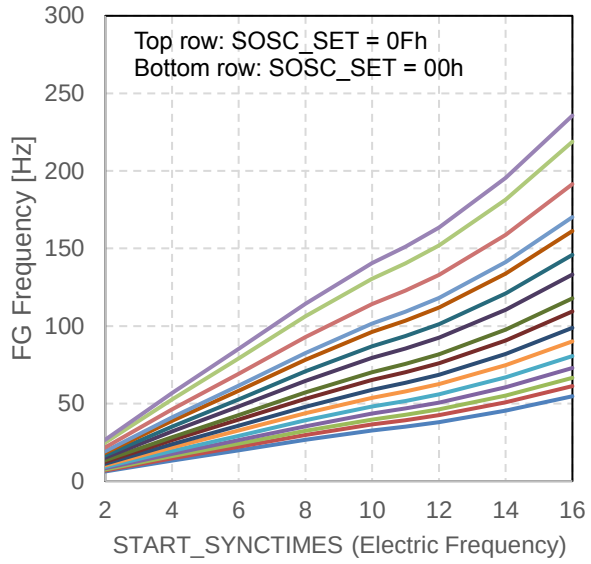


Figure 19. START_SYNCTIMES vs FG Frequency
(SOSC_SET = 00h to 0Fh)
(High-Speed Startup Mode)

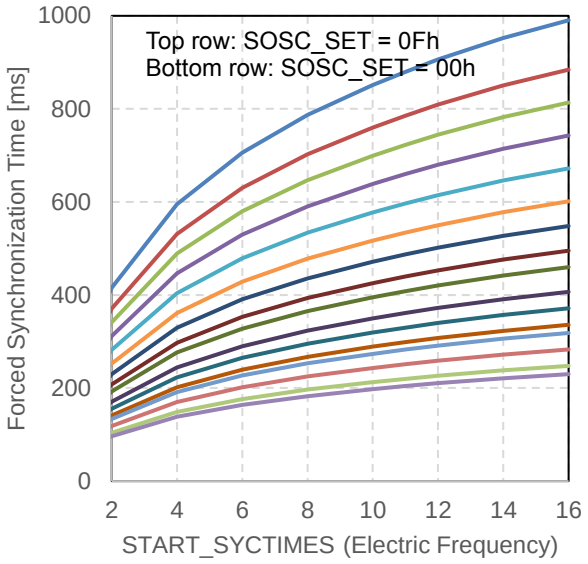


Figure 20. START_SYNCTIMES vs Forced Synchronization Time
(SOSC_SET = 00h to 0Fh)
(High-Speed Startup Mode)

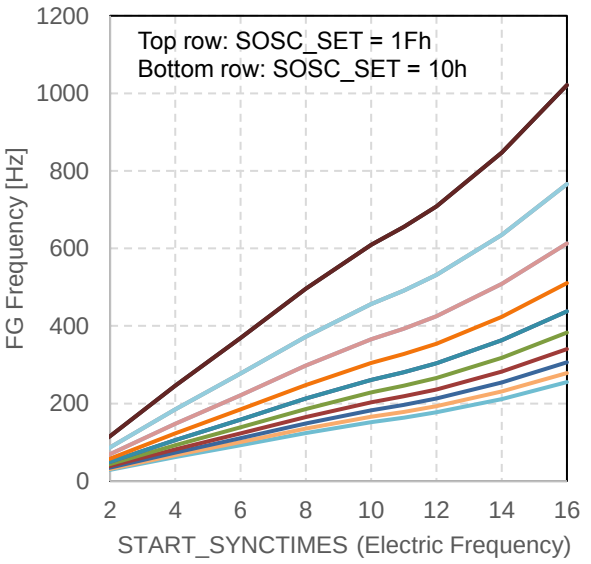


Figure 21. START_SYNCTIMES vs FG Frequency
(SOSC_SET = 10h to 1Fh)
(High-Speed Startup Mode)

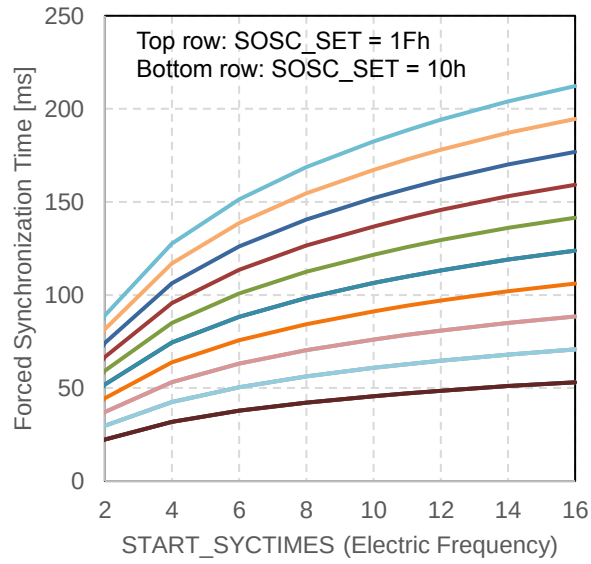


Figure 22. START_SYNCTIMES vs Forced Synchronization Time
(SOSC_SET = 10h to 1Fh)
(High-Speed Startup Mode)

(9) Frequency Setting in Forced Synchronization Startup Section - continued

Parameter name	Register Initial Value	Function	Selection mode	Description
Startup Slope (SOSC_SET)	0Ch	Acceleration adjustment setting for forced synchronization	Normal mode (MODE_SEL = 0h)	00h: 16.5 µs, 01h: 15.0 µs, 02h: 13.6 µs, 03h: 12.4 µs, 04h: 11.2 µs, 05h: 10.2 µs, 06h: 9.3 µs, 07h: 8.4 µs, 08h: 7.6 µs, 09h: 6.9 µs, 0Ah: 6.3 µs, 0Bh: 5.7 µs, 0Ch: 5.2 µs, 0Dh: 4.7 µs, 0Eh: 4.2 µs, 0Fh: 3.8 µs, 10h: 3.5 µs, 11h: 3.1 µs, 12h: 2.8 µs, 13h: 2.6 µs, 14h: 2.3 µs, 15h: 2.1 µs, 16h: 1.9 µs, 17h: 1.7 µs, 18h: 1.5 µs, 19h: 1.4 µs, 1Ah: 1.2 µs, 1Bh: 1.1 µs, 1Ch: 1.0 µs, 1Dh: 0.9 µs, 1Eh: 0.8 µs, 1Fh: 0.7 µs
			High-speed startup mode (MODE_SEL = 1h)	00h: 5.5 µs, 01h: 5.0 µs, 02h: 4.6 µs, 03h: 4.2 µs, 04h: 3.8 µs, 05h: 3.4 µs, 06h: 3.1 µs, 07h: 2.8 µs, 08h: 2.6 µs, 09h: 2.3 µs, 0Ah: 2.1 µs, 0Bh: 1.9 µs, 0Ch: 1.8 µs, 0Dh:1.6 µs, 0Eh: 1.4 µs, 0Fh: 1.3 µs, 10h: 1.2 µs, 11h: 1.1 µs, 12h: 1.0 µs, 13h: 0.9 µs, 14h: 0.8 µs, 15h to 16h: 0.7 µs, 17h: 0.6 µs, 18h to 19h: 0.5 µs, 1Ah to 1Ch: 0.4 µs, 1Dh to 1Fh: 0.3 µs
Startup Section (START_SYNCTIMES)	3h	Forced synchronization cycle number setting	Normal mode High-speed startup mode	0h: 2 periods, 1h: 4 periods, 2h: 6 periods, 3h: 8 periods, 4h: 10 periods, 5h: 12 periods, 6h: 14 periods, 7h: 16 periods

2. Sensorless Sinusoidal Drive - continued

(10) Output Duty in Fixed Initial Position Section to Forced Synchronization Startup Section

OTP setting: START_DUTYSLP, VCLINIT, VCL, CL_LINE_SWMASK

After braking in the fixed initial position section, the output duty is increased by the slope setting (START_DUTYSLP/register default [0h]: 204.8 µs / 0.1 % [Typ]), and the output duty is latched during current limit detection. The motor is accelerated at a constant output duty between the fixed initial position section and the forced synchronization startup section. Note that after the output duty latch, the current limit is disabled until the forced synchronization section ends. When the forced synchronization startup is complete, it is followed by the induced voltage detection drive section. Here, the setting changes from the initial current limit setting (VCLINIT/register default [1C0h]: 104.1 mV [Typ]) to the current limit setting with adjustment function during steady state driving (VCL/register default [1Ch]: 104.1 mV [Typ]).

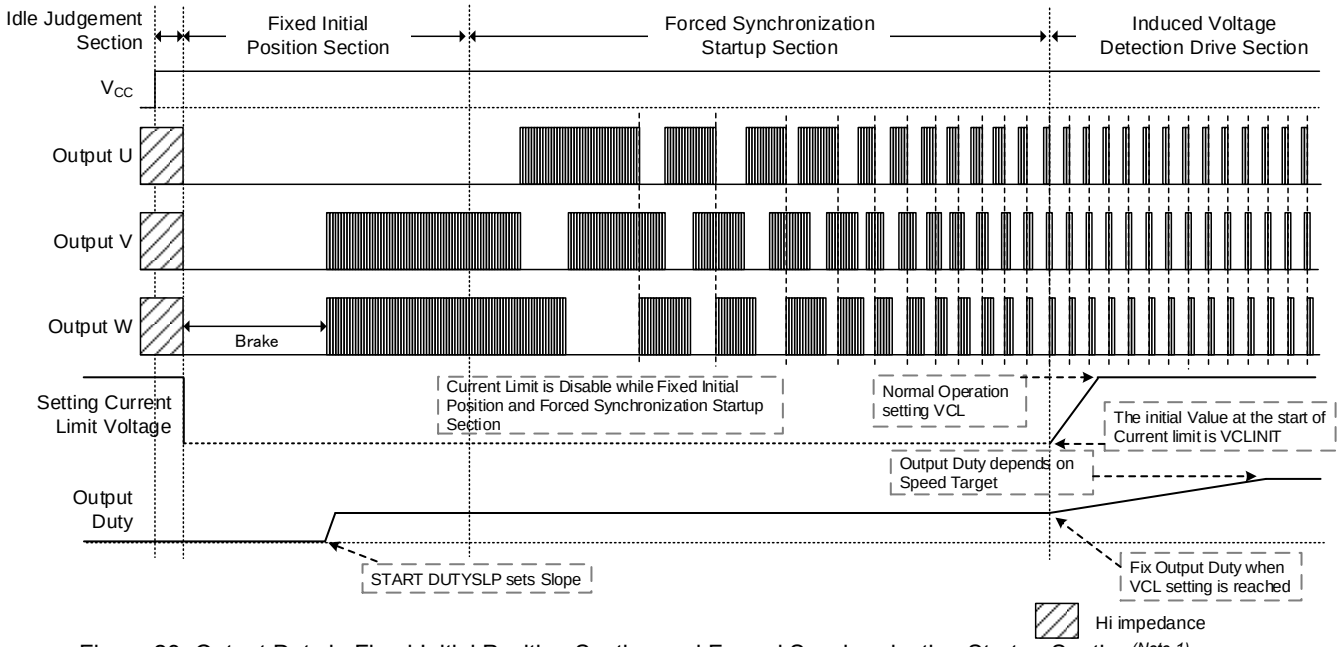


Figure 23. Output Duty in Fixed Initial Position Section and Forced Synchronization Startup Section *(Note 1)*

(Note 1) Three-phase modulation. The minimum duty section of the output signal waveform is not shown.

Parameter name	Register Initial Value	Function	Selection mode	Description
Startup Duty Slope (START_DUTYSLP)	0h	Start-up output duty step time setting	Normal mode (MODE_SEL = 0h)	0h: 204.8 µs / 0.1 %, 1h: 102.4 µs / 0.1 %, 2h: 409.6 µs / 0.1 %, 3h: 819.2 µs / 0.1 %
			High-speed startup mode (MODE_SEL = 1h)	0h: 20 µs / 0.1 %, 1h: 10 µs / 0.1 %, 2h: 40 µs / 0.1 %, 3h: 80 µs / 0.1 %
CL Level for Initial (VCLINIT)	1C0h	Initial current limit setting	Normal mode High-speed startup mode	44 mV to 191 mV, 0.23 mV step, VCLINIT = 192d to 832d, 0d to 191d/833d to 1023d Prohibited setting
VCL	1Ch	Current limit setting	Normal mode High-speed startup mode	44 mV to 191 mV, 3.70 mV step, VCL = 12d to 52d, 0d to 11d/53d to 63d Prohibited setting

(10) Output Duty in Fixed Initial Position Section to Forced Synchronization Startup Section - continued

The detection path is different between the current limit in the fixed initial position section and induced voltage detection drive section.
For fixed initial position section, current limit is detected through CS2 pin. For induced voltage detection drive section, current limit is detected through CS1 pin. As shown in the figure below, only one switch turns ON for the path of CS1 and CS2 pin while path to CR pin is switched ON at all times.
Furthermore, the path switching function can be disabled through the current limit detection path switching disable setting (CL_LINE_SWMASK/register default [1h]: Switching enabled). When the switch is disabled, current limit is detected in CS1 path at all times since the switch in CS1 path will be ON and the switch in CS2 path will be OFF.

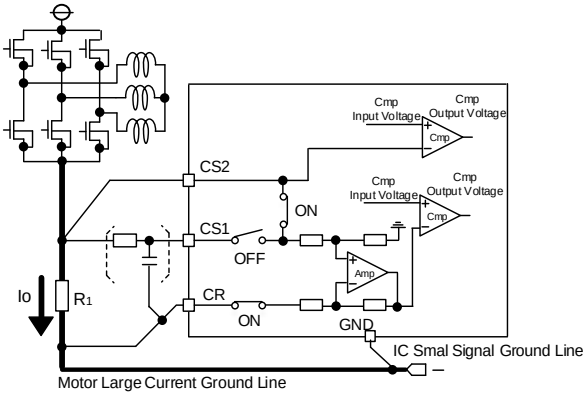


Figure 24. Fixed Initial Position Section Current Limit Detection Path

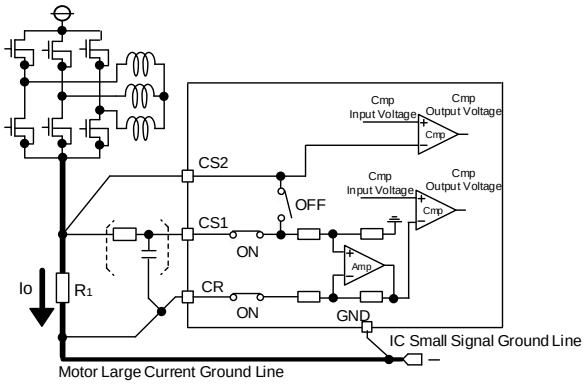


Figure 25. Induced Voltage Detection Drive Section Current Limit Detection Path

Parameter name	Register Initial Value	Function	Selection mode	Description
CL_LINE_SWMASK	0h	Current limit detection path switching disable setting	Normal mode High-speed startup mode	0h: Switching enabled, 1h: Switching disabled

2. Sensorless Sinusoidal Drive - continued

(11) Current Limit

OTP setting: CL Noise Mask

When the low-side motor current exceeds the current limit, the output duty is limited to suppress the current. At the next PWM (ON) timing, if the low-side motor current falls below the current limit setting (VCL/register default [1Ch]: 104.1 mV), normal operation will resume. The set current value I_O at which the current limit operates is determined by CS1 pin voltage V_{CS1}, CR pin voltage V_{CR} and the low-side motor current detection resistor R_1. The following equation is for R_1 = 39 mΩ:

$$I_O\ [\mathrm{A}] = (V_{CS1}\ [\mathrm{V}] - V_{CR}[\mathrm{V}]) / R_1\ [\Omega]$$
$$= 0.1041 / 0.039$$
$$= 2.67\ \mathrm{A}$$

$$P_C\ [\mathrm{W}] = (V_{CS1}\ [\mathrm{V}] - V_{CR}[\mathrm{V}]) \times I_O\ [\mathrm{A}]$$
$$= 0.1041 \times 2.67$$
$$= 0.28\ \mathrm{W}$$

When the current limit function is not used, short the CS1 pin to GND. Large current flows through resistor R_1 to detect the low-side motor current. The power dissipation P_C is calculated using the equation above. Pay attention to the power dissipation.

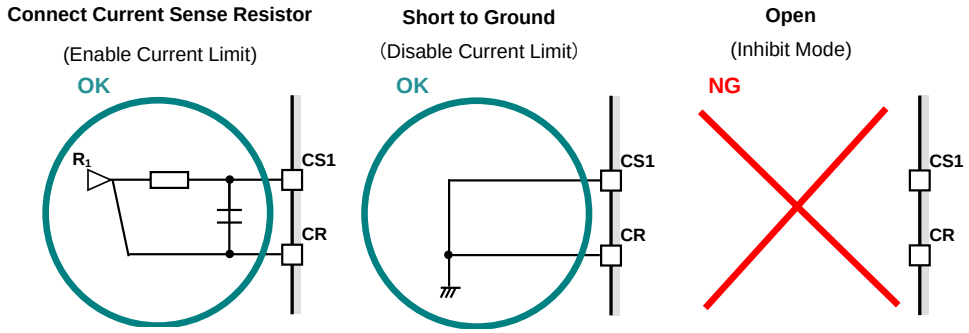


Figure 26. CS1 Pin Configuration

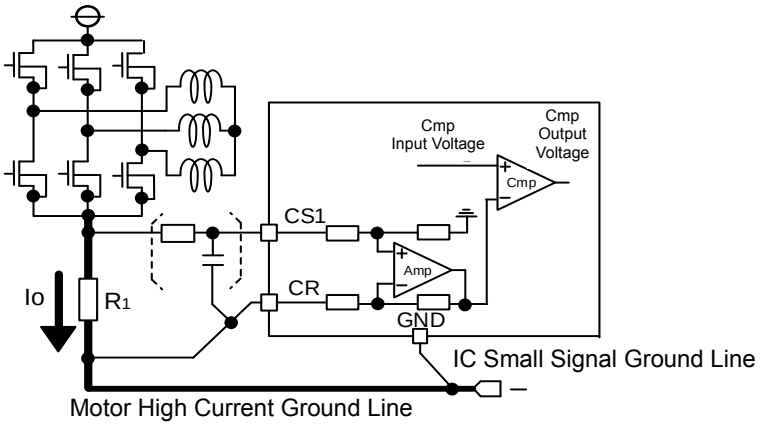


Figure 27. Small Signal and Large Current Ground Line Isolation

When designing PCB layout, the small signal ground line of the IC should be separated from the large current ground line of the motor to which R_1 is connected, as shown in Figure 27.

A noise mask function (CL Noise Mask/register default [0h]: 1 µs [Typ]) is built-in to prevent current limit false detection.

Parameter name	Register Initial Value	Function	Description
CL Noise Mask	0h	Current limit malfunction prevention mask time setting	0h: 1 µs, 1h: 2 µs, 2h: 4 µs, 3h: 0 µs

Description of Operation - continued

3. Speed Control

The IC has a built-in speed control that keeps the motor speed constant. The output duty is controlled so that the target rotation set by PWMIN pin and the internal reference FG detected by driving the motor become equal. Figure 28 shows the configuration diagram of the speed control block.

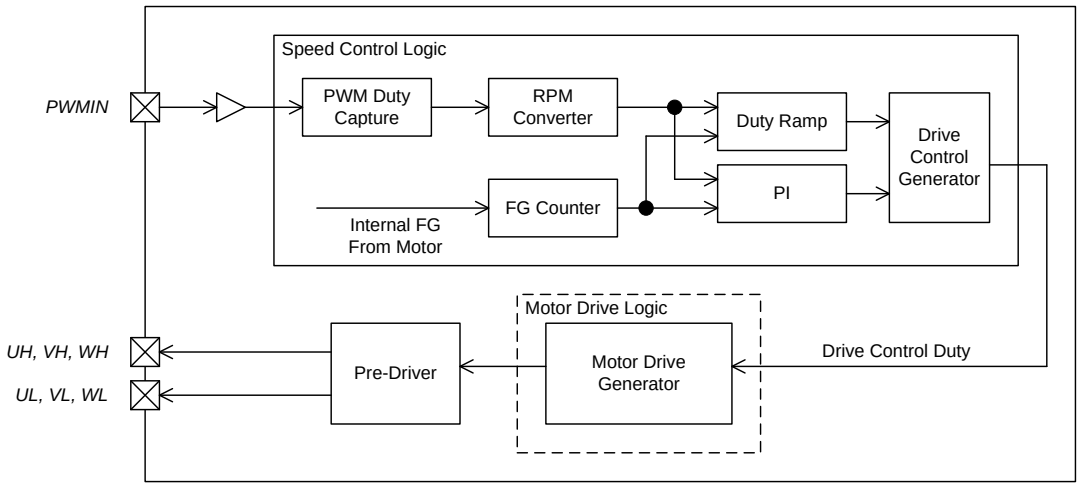


Figure 28. Speed Control Block Diagram

(1) Relation Between PWMIN Duty and Target Rotation

OTP setting: PWMIN POLE, OPEN_DSTEP
RREF, RREF2, RREF2IN, MIN, Calc Duty 0, Calc Duty 1, PWM Duty 3, PWM Duty 4

Target RPM for input PWMIN Duty is shown in Figure 29 and Figure 30. Note that PWMIN input polarity (PWMIN POLE/register default [0h]: positive logic*(Note 1)*) is positive logic, and the 0 % and 100% of the x-axis are inverted in the case of negative logic. The Target RPM (Max) is the motor frequency f_{MAXRPM} at the maximum target rotation speed defined by the maximum rotation speed setting value (RREF/register default [147h] = [327d]). When PWMIN duty = 100 % is set, the drive is judged as OFF, and output duty decreases by 0.1 % (Typ) per unit time (OPEN_DSTEP/register default [30h]: 4.9 ms [Typ]), and the motor.

(Note 1) Expressed as high logic duty

$$poles = 10$$

$$\begin{aligned} Target\ RPM\ (Max) &= f_{MAXRPM}[Hz] \times 60[s] \\ &= \{RREF + 1\} \times 1.041 \times \frac{2}{poles} \times 60 \\ &= (327 + 1) \times 1.041 \times \frac{2}{10} \times 60 \\ &= 4097\ \text{min}^{-1} \end{aligned}$$

Furthermore, the 2nd maximum rotation speed can be set to a rotation speed of 100 % or less as a percentage of the maximum target rotation speed (RREF2/register default [400h]: 100 %). The 2nd maximum rotation speed is maintained with the input PWMIN duty at the 2nd maximum rotation speed input threshold (RREF2IN/register default [39Ah]: 90.0 %) or higher.

The minimum rotation speed can be set as a percentage (MIN/register default [096h] = [150d]: 14.6 %) of the maximum target rotation speed ([400h] = [1024d]: 100 %). The minimum rotation speed is maintained with the input PWMIN duty below minimum rotation speed saturation threshold (PWM Duty 3, PWM Duty 4/register default [0CDh]: 20.0 %).

$$\begin{aligned} Target\ RPM\ (Min) &= Target\ RPM\ (Max) \times 150 \div 1024 \\ &= 600\ \text{min}^{-1} \end{aligned}$$

When the input PWMIN duty is set below the drive OFF judgment threshold (Calc Duty 0/register default [068h]: 10.2 % [Typ]), the motor will stop (all external FET outputs are OFF), and when the input is set above the drive ON judgment threshold (Calc Duty 1/register default [099h]: 14.9 % [Typ]), the motor will rotate.

(1) Relation Between PWMIN Duty and Target Rotation - continued

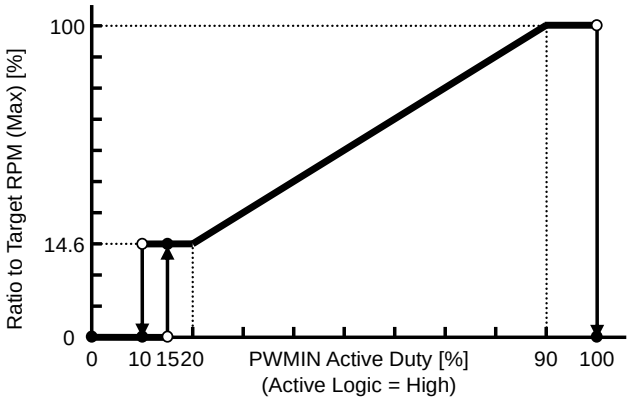


Figure 29.
Relationship between PWMIN Duty and Target Rotation to Maximum Rotation (Default Register Values)

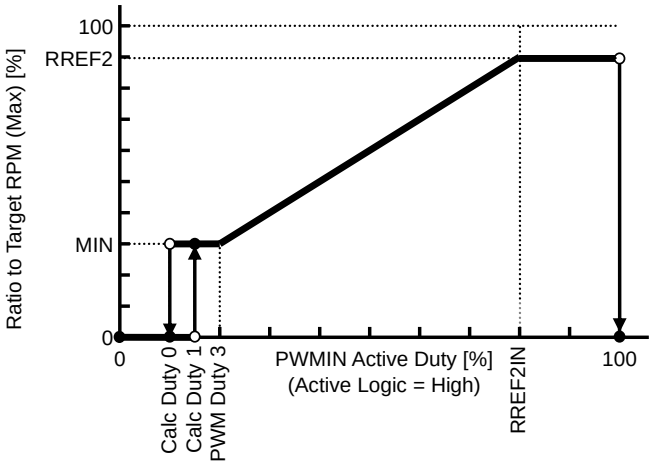


Figure 30.
Relationship between PWMIN Duty and Target Rotation to Maximum Rotation (Register Names)*(Note 1)*

Parameter name	Register Initial Value	Function	Description
PWMIN POLE	0h	PWMIN input polarity switching setting*(Note 2)*	0h: Positive logic, 1h: Negative logic
OPEN_DSTEP	30h	Output duty step time setting at drive-off command	0 ms to 26.112 ms, 102.4 µs step, OPEN_DSTEP = 0d to 255d
RREF	147h	Maximum rotation speed setting (100 % RPM)	f_{MAXRPM} [Hz] = {RREF + 1} * 1.041 * 2 / poles, RREF = 0d to 1024d, 1025d to 2047d Prohibition setting
RREF2	400h	2nd maximum rotation speed ratio setting	$f_{MAXRPM2}$ [Hz] = f_{MAXRPM} [Hz] * {RREF2} / 1024, RREF2 = 0d to 1024d, 1025d to 2047d Prohibition setting
RREF2IN	39Ah	2nd maximum rotation speed input threshold setting	$D_{MAXRPM2}$ [%] = {RREF2IN} / 1024, RREF2IN = 1d to 1024d, 0d, 1025d to 2047d Prohibition setting
MIN	096h	Minimum rotation speed ratio setting	f_{MINRPM} [Hz] = f_{MAXRPM} [Hz] * {MIN} / 1024, MIN = 0d to 1024d, 1025d to 2047d Prohibition setting
Calc Duty 0	068h	PWMIN input drive OFF judgement threshold setting	$D_{Calc\ Duty\ 0}$ [%] = {Calc Duty 0} / 1024, Calc Duty 0 = 1d to 1024d, 0d, 1025d to 2047d Prohibition setting
Calc Duty 1	099h	PWMIN Input Drive ON judgement threshold setting	$D_{Calc\ Duty\ 1}$ [%] = {Calc Duty 1} / 1024, Calc Duty 1 = 1d to 1024d, 0d, 1025d to 2047d Prohibition setting
PWM Duty 3	0CDh	Minimum rotation speed saturation input threshold setting*(Note 1)*	$D_{PWM\ Duty3}$ [%] = {PWM Duty 3} / 1024, PWM Duty 3 = 1d to 1024d, 0d, 1025d to 2047d Prohibition setting
PWM Duty 4	0CDh	Minimum rotation speed saturation input threshold setting*(Note 1)*	$D_{PWM\ Duty4}$ [%] = {PWM Duty 4} / 1024, PWM Duty 4 = 1d to 1024d, 0d, 1025d to 2047d Prohibition setting

(Note 1) The parameter PWM Duty 3 and PWM Duty 4 must be set to the same value.
(Note 2) High logic duty is the positive logic, and low logic duty is the negative logic.

3. Speed Control - continued

(2) PWMIN Pin Configuration Setting

OTP setting: PWMIN_PD, PWMIN_PU

Internal resistor pull-up or resistor pull-down for the PWMIN pin can be set. This is determined by the settings of PWMIN_PD (initial value [0h]: resistor pull-down disable) and PWMIN_PU (initial value [0h]: resistor pull-up disable). Since both are disabled by default, the logic is not fixed inside the IC. To prevent the PWMIN input from becoming unstable, please use a resistor pull-down or resistor pull-up in the application circuit. If you use the IC without placing a resistor outside it, be sure to change one of the settings to fix the logic.

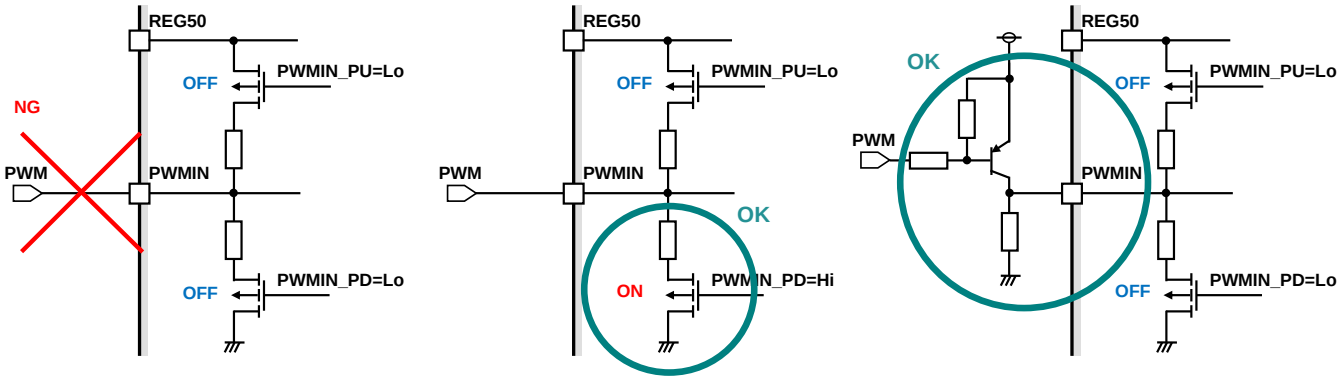


Figure 25. PWMIN Pin Internal Pull-up / Pull-down Setting

Parameter name	Register Initial Value	Function	Description
PWMIN_PD	0h	PWMIN internal resistor pull-down enable setting	0h: Resistor pull-down disable , 1h: Resistor pull-down enable (Prohibit during PWMIN_PU = 1h)
PWMIN_PU	0h	PWMIN internal resistor pull-up enable setting	0h: Resistor pull-up disable , 1h: Resistor pull-up enable (Prohibit during PWMIN_PD = 1h)

3. Speed Control - continued

(3) Motor Speed Measurement

The motor rotation speed is compared with the half period of the internal FG signal generated from the measured value of the induced voltage detection period and the half period of the target period calculated from the target rotation speed, and the difference is taken as the speed error value. If the half period of the internal FG signal is longer (slower than the target rotation speed), the speed error value is negative. Conversely, if it is shorter (faster than the target rotation speed), the speed error value is positive.

(4) Motor Speed Control Setting

It is driven by RAMP control drive and PI control drive. The motor speed control settings are shown in the table below.

Startup / Acceleration / Deceleration Operation	Steady Operation
RAMP control drive	PI control drive

(5) RAMP Control

OTP setting: Ramp Step Time Dec, Ramp Step Time Acc, RAMP_TO_PI_LEV

If the speed error value is negative (slower than the target rotation speed), the output duty is gradually increased. If it is positive (faster than the target rotation speed), it is gradually decreased so that the actual motor speed approaches the target speed. As shown in Figure 33, output duty changes by 0.1 % (Typ) every step. The step time width at acceleration (Ramp Step Time Acc/register default [10h]: 13.9 ms [Typ]) and step time width at deceleration (Ramp Step Time Dec/register default [10h]: 13.9 ms [Typ]) can be set individually.

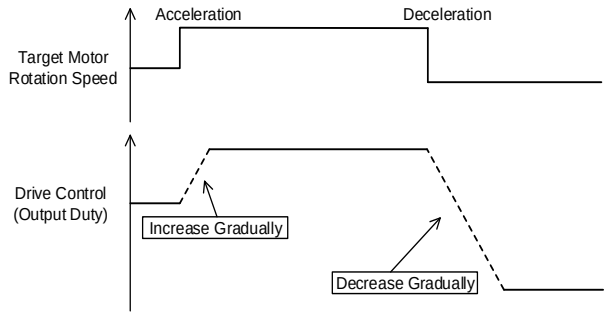


Figure 32. RAMP Control

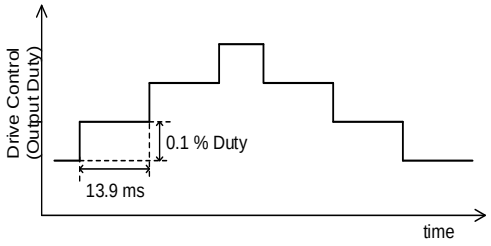


Figure 33. RAMP Step

Parameter name	Register Initial Value	Function	Description
Ramp Step Time Dec (RAMP_TIMESTEP_DEC)	10h	RAMP operation step time width setting during deceleration	0.819 ms to 209.6 ms, 0.819 ms step t_{RAMP} [ms] = {RAMP_TIMESTEP_DEC +1} * 0.819 [ms], Ramp Step Time Dec = 0d to 255d
Ramp Step Time Acc (RAMP_TIMESTEP_ACC)	10h	RAMP operation step time width setting during acceleration	0.819 ms to 209.6 ms, 0.819 ms step t_{RAMP} [ms] = {RAMP_TIMESTEP_ACC +1} * 0.819 [ms], Ramp Step Time Acc = 0d to 255d

(5) RAMP Control - continued

RAMP control switches to PI control when the speed error value for the target rotation speed is within the threshold value (RAMP_TO_PI_LEV/register default [04h]: 1.57 % [Typ]). In the area where the speed error value is large, the actual motor rotation speed approaches the target rotation speed through RAMP control. When the speed error decreases, PI control starts to adjust the parameters easily.

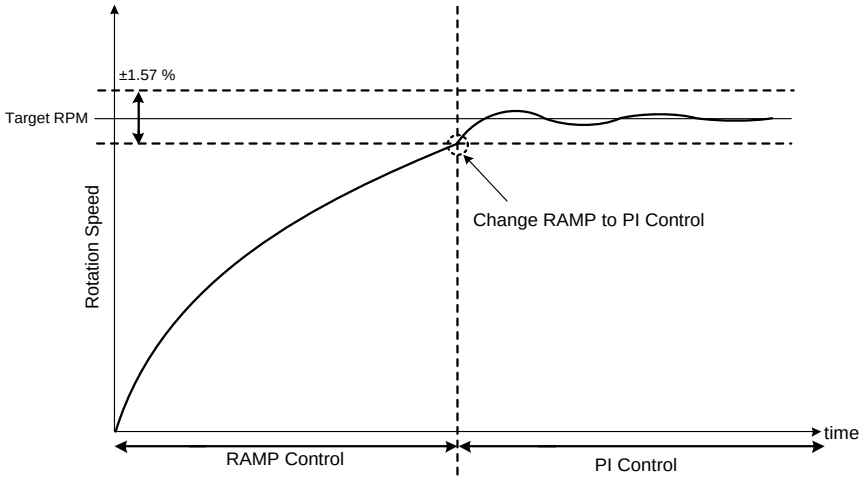


Figure 34. RAMP Control to PI Control

Parameter name	Register Initial Value	Function	Description
Ramp to PI Change Level (RAMP_TO_PI_LEV)	04h	PI switching speed error threshold setting	0 % to 24.609 %, 0.391 % step, RAMP_TO_PI_LEV = 0d to 63d

(6) PI Control

OTP setting: EC_LIMIT, KP_0, KI_0

Performs closed loop speed control using PI control. The output duty is calculated using the speed error value measured by the internal reference period after applying the error limit, (EC_LIMIT / register default [FFh]: 100 %), and using the proportional gain (KP_0 / register default [18h]: 0.375) and the integral gain (KI_0 / register default [03h]: 0.012). Figure 35 shows PI control block diagram.

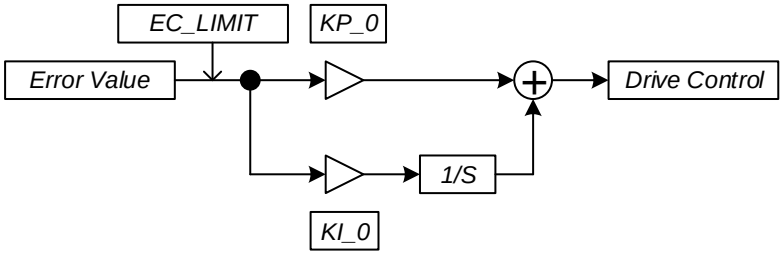


Figure 35. PI Control Block Diagram

Parameter name	Register Initial Value	Function	Description
Speed Error Limit (EC_LIMIT)	FFh	Speed error limit setting	0 % to 100 %, 0.781 % step, EC_LIMIT = 0d to 128d, 129d to 255d: 100 %
P Value of PI (KP_0)	18h	Speed PI control proportional gain setting	KP = {KP_0} * 0.01564, KP_0 = 0d to 255d
I Value of PI (KI_0)	03h	Speed PI control integral gain setting	KI = {KI_0} * 0.00391, KI_0 = 0d to 255d

Description of Operation - continued

4. Signal Output

(1) Startup Stable Judgment Output Setting (FG Mask)

OTP setting: FGMASKEN, FGALTIME

FG signal is masked (FGMASKEN/register default [1h]: Mask Enabled) from the idle detection section to the forced synchronization section (FG Mask 1) and immediately after the start of the induced voltage detection drive section (FG Mask 2), startup stability is determined. Output starts from the timing (FGALTIME/register default [0h]: After 5 consecutive induced voltage stability detection is established).

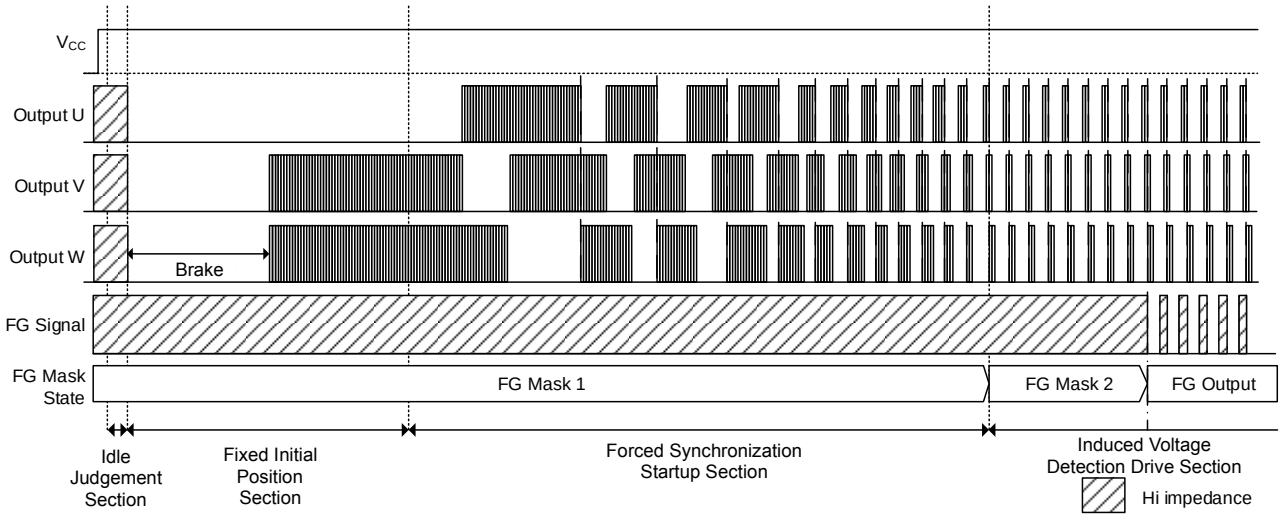


Figure 36. Output Signal (U, V, W) and FG Signal Timing Chart (FG Masking Enable)*(Note 1)*

(Note 1) Three-phase modulation. The minimum duty section of the output signal waveform is not shown.

Parameter name	Register Initial Value	Function	Description
Initial FG Mask (FGMASKEN)	1h	FG output mask setting at forced synchronization startup	0h: Masking Disabled (FG output), 1h: Mask Enabled (Masked after FGALTIME setting condition is met)
FG Mask Count (FGALTIME)	0h	FG mask release condition switching setting (Startup stability judgment condition)	0h: After 5 consecutive induced voltage stability detection is established, (FG output from the 6th time of induced voltage stability detection) 1h: After 9 consecutive induced voltage stability detection is established, (FG is outputted from the 10th time of the induced voltage stability detection)

Startup stability is judged immediately after the start of the induced voltage detection drive section (FG Mask 2), if FG mask release condition at startup occurs continuously for the number of times specified in FGALTIME setting (no sudden acceleration and lock protection detection condition will occur).

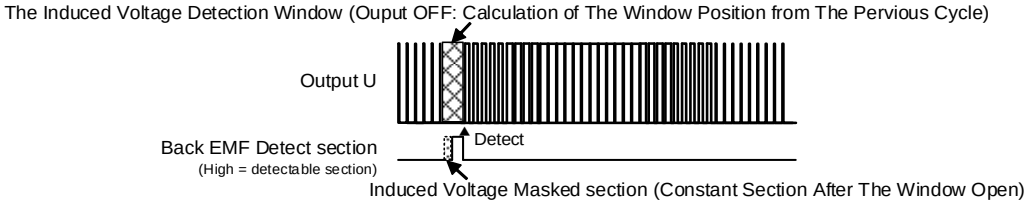


Figure 37. FG Mask Release Condition at Startup (FGALTIME setting count consecutively met): Output Signal Waveform When Induced Voltage Stability is Detected

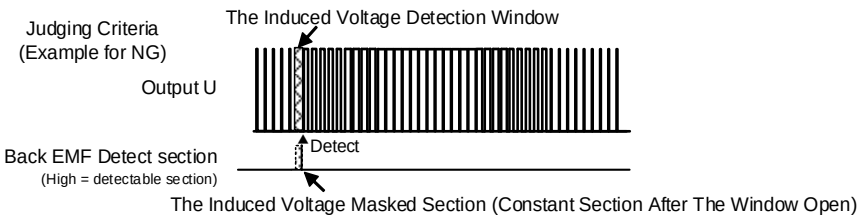


Figure 38. Conditions for FG Mask Continuation at Startup: In Case of Rapid Acceleration and Motor Lock

4. Signal Output - continued

(2) Abnormality Detection Output (AL)

OTP setting: FG_ALEN, MIN_TIME, AL_MIN_3CYCLES

When abnormality detection output setting (FG_ALEN/register default [0h]: AL disabled) is enabled, during error detection and protection time, an error detection specific frequency signal (1 Hz [Typ] to 5 Hz [Typ]) will be the output from FG pin. After an abnormality is detected, the frequency signal for each abnormality detection continues to be output, and the output condition (AL_MIN_3CYCLES/register default [1h]: 3-period output) from the last abnormality detection can be selected. Also, there is a setting selection for output time (MIN_TIME/register default [0h]: 3 s).

Parameter name	Register Initial Value	Function	Description
FG_ALEN	0h	AL signal FG superimposition switching setting	0h: AL signal disabled, 1h: AL signal enabled
MIN_TIME	0h	AL signal minimum output time switching setting*(Note 1)*	0h: 3 s, 1h: 5 s, 2h: 7 s, 3h: 14 s
AL_MIN_3CYCLES	1h	AL signal minimum output condition switching setting	0h: MIN_TIME setting time output, 1h: 3-period output (MIN_TIME setting disabled)

(Note 1) Valid only when FG_ALEN = 1h and AL_MIN_3CYCLES = 0h.

Description of Operation - continued

5. Protection Function

The protection functions includes Over current protection (OCP), Over temperature protection (TSD), Motor lock protection (MLP), Input abnormal frequency protection (EFP), Over voltage protection (OVP), and VCC under voltage protection (UVLO) and VG under voltage protection (UVGP).
All these protection functions are the automatic reset type and operate under the following conditions and priority order.

Priority Ranking	Protection Function	Operating Conditions		Boost Circuit Output	External FET Output	Abnormal Detection Output Frequency
		Detection	Release			
1	Under voltage (VCC)	V_{CC} ≤ 6 V (Typ)	V_{CC} ≥ 7 V (Typ)	Mute	OFF (Hi-Z)	0 Hz (Low logic)
2	Under voltage (VG)	V_G ≤ V_{CC} + 3 V (Typ)	V_G ≥ V_{CC} + 3 V (Typ)	Active *(Note 1)*		- *(Note 2)*
3	Over current	Detected voltage between CS2 and GND pin (OTP setting) or more	Detection voltage or less after the protection time has elapsed			1 Hz (Typ)
4	Over temperature	Tj ≥ 175 °C (Typ)	Tj ≤ 150 °C (Typ) after the protection time elapsed			2 Hz (Typ)
5	Over voltage	V_{CC} ≥ 22 V (Typ) / 31 V (Typ)	V_{CC} ≤ 20 V (Typ) / 29 V (Typ) after the protection time elapsed	Mute/ Active *(Note 3)*		3 Hz (Typ)
6	Motor lock	(1)Induced voltage edge not detected (OTP setting) (2)High rotation error detection (Max rotation speed × 1.5 times (Typ), Immediate detection) (3)Low rotation error detection (80 min^{-1} (Typ) or less, immediate detection)*(Note 4)*	After the protection time elapses	Active		4 Hz (Typ)
7	Input abnormal frequency	150 ms (Typ) continuous abnormal frequency input	Input frequency within normal range in 15 consecutive cycles			5 Hz (Typ)

(Note 1) If the boost circuit output is muted when an overvoltage error is detected, the output boost circuit remains muted until the overvoltage error is cleared even if the higher priority error is detected.
(Note 2) When under voltage (VG) error is detected, the output frequency is maintained when a lower order priority error is detected.
(Note 3) It can be selected using the register "VG_OVP_SET".
(Note 4) The rotation speed is expressed in terms of a 10-pole motor.

5. Protection Functions - continued

(1) Motor Lock Protection (MLP: Motor Lock Protection)

(a) Motor Lock

OTP setting: LKPRT_OFF, TLK_DET, TLK

When the motor is locked or stalled due to a mechanical disturbance, the motor lock protection function is activated, and all external FET outputs are turned OFF during the protection time (TLK/register default [32h]: 5 s [Typ]). The induced voltage edge is detected when the motor is rotating, but not when the motor is locked. When the induced voltage edge is not detected for a certain period (TLK_DET/register default [0Ah]: 1 s [Typ]), it is determined that the motor is locked. Since the lock judgment starts from the induced voltage detection section of the sinusoidal waveform generated based on the previous period, it depends on the setting of the number of times of induced voltage detection per electric angle and the motor rotation speed.

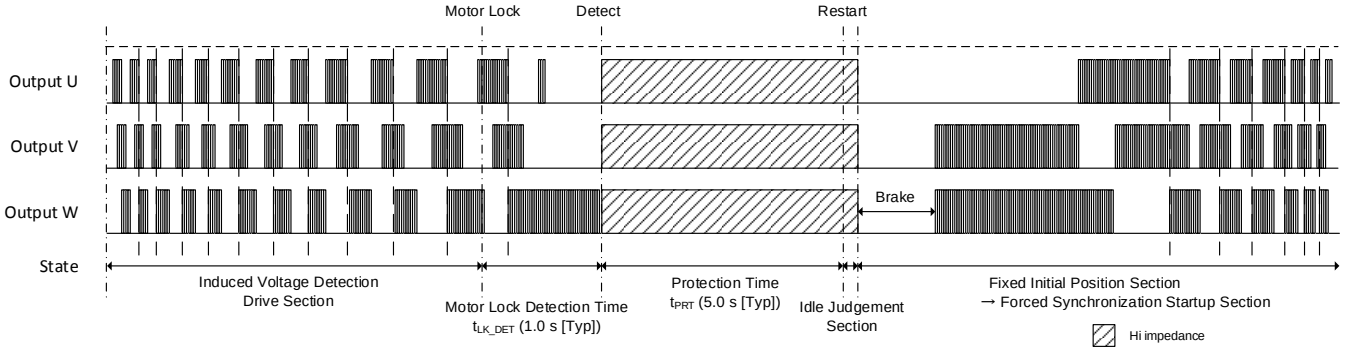


Figure 39.Operation during Motor Lock Protection Detection and Release

Parameter name	Register Initial Value	Function	Description
LKPRT_OFF	2h	Lock protection disable setting	1h: Protection Disabled*(Note 1)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
MLP Detect Time (TLK_DET)	0Ah	Motor lock detection time setting	0 s to 25.5 s, 100 ms step TLKDET = 1d to 255d, 0d: Disable setting
MLP Time (TLK)	32h	Motor lock protection time setting	0 s to 25.5 s, 100 ms step TLK = 0d to 255d

(Note 1) Protection disable is enabled only when the register in OTP is changed.

(1) Motor Lock Protection (MLP: Motor Lock Protection) - continued

(b) High Rotation Error

OTP setting: MAXRPMPRT_OFF, TMAXRPM

When the motor exceeds 1.5 times (Typ) of the maximum rotation speed setting due to disturbance, the motor lock protection function will be activated, and all external FET outputs are turned OFF during the protection time (TMAXRPM/register default [32h]: 5 s [Typ]). Motor lock protection is released after the protection time has elapsed. The detection depends on the number of induced voltage detection per electric angle (BEMF Detect Type/register default [1h]: 360°).

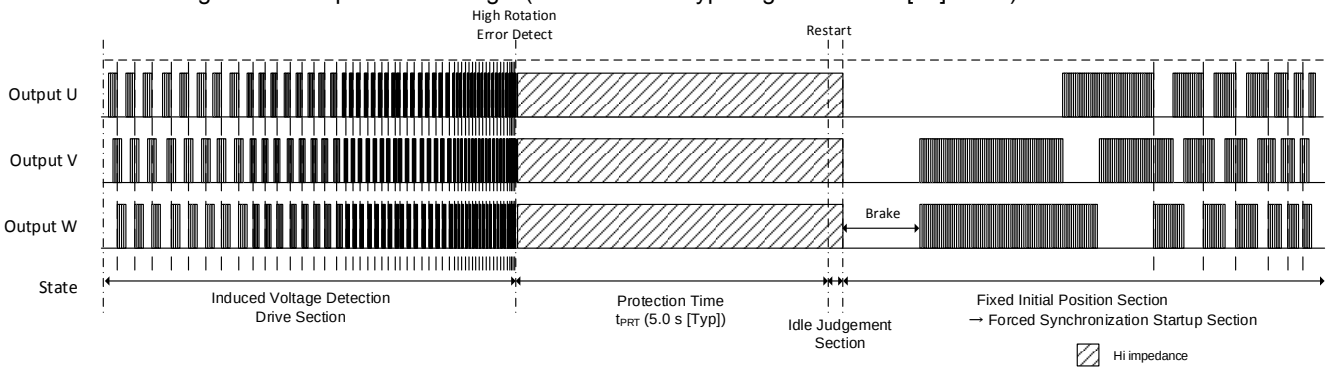


Figure 40. Operation during High Rotation Error Detection and Release

Parameter name	Register Initial Value	Function	Description
MAXRPMPRT_OFF	2h	High rotation error protection disable setting	1h: Protection Disabled*(Note 1)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
Max RPM Protect Time (TMAXRPM)	32h	High rotation error protection time setting	0 s to 25.5 s, 100 ms step TMAXRPM = 0d to 255d

(Note 1) Protection Disable is only enabled when changing register values with OTP

(1) Motor Lock Protection (MLP: Motor Lock Protection) - continued

(c) Low Rotation Error*(Note 1)*

OTP setting: MINRPMPRT_OFF, TMINRPM

When the period of induced voltage detection falls below the time equivalent to a motor rotation speed of 80 min^{-1} (Typ) due to disturbances, the motor lock protection function will be activated, and all external FET outputs are turned OFF during the protection time (TMINRPM/register default [32h]: 5 s [Typ]). Motor lock protection is released after the protection time has elapsed. The detection depends on the number of induced voltage detection per electric angle (BEMF Detect Type/register default [1h]: 360°).

(Note 1) The rotation speed is expressed in terms of a 10-pole motor.

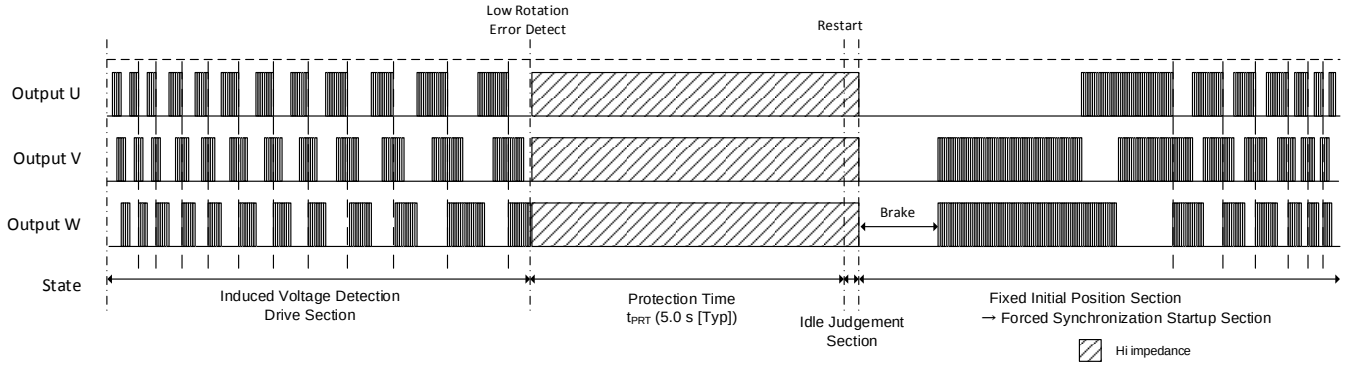


Figure 41. Operation during Low Rotation Error Detection and Release

Parameter name	Register Initial Value	Function	Description
MINRPMPRT_OFF	2h	Low rotation error protection disable setting	1h: Protection Disabled*(Note 1)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
Min RPM Protect Time(TMINRPM)	32h	Low rotation error protection time setting	0 s to 25.5 s, 100 ms step TMINRPM = 0d to 255d

(Note 1) Protection Disable is only enabled when changing register values with OTP

5. Protection Functions - continued

(2) Current Protection (OCP: Over Current Protection)

OTP setting: OCP_PRTMSK, OCP, TOCP, OCP Noise Mask

The IC has a built-in overcurrent protection circuit which is activated only in the event of an output short-circuit. As shown in Figure 42, it has a built-in comparator to compare the CS2 pin voltage with the detection voltage value (OCP/register default [362h]: 0.2 V [Typ]). When CS2 pin voltage exceeds the detection voltage, overcurrent protection is activated, and during the protection time (TOCP/register default [32h]: 5 s [Typ]), all external FET outputs turn OFF. If no overcurrent is detected after the protection time has elapsed, the protection is released. In addition, a mask time function (OCP Noise Mask/ register default [2h]: 3 µs [Typ]) is provided to prevent malfunction. The OCP comparator output during the masking time is ignored as shown in Figure 43 (a). In addition to the masking time, there is a response time (5.5 µs Max) until the pre-driver output goes Low. Therefore, as shown in Figure 43 (b), the pre-driver output goes Low after the time that the masking time and response time has elapsed from the point when CS2 pin voltage exceeded the detection voltage.

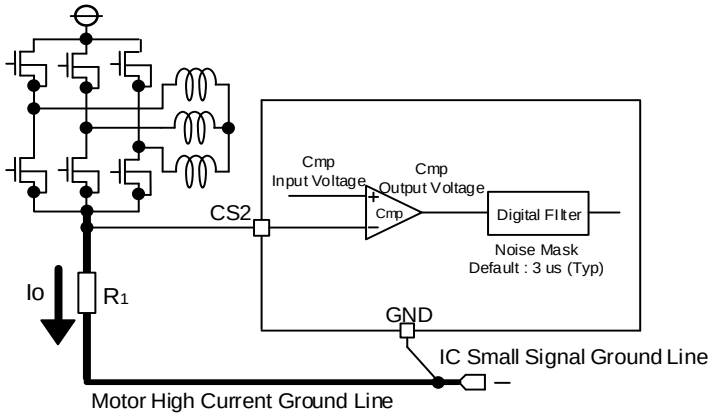
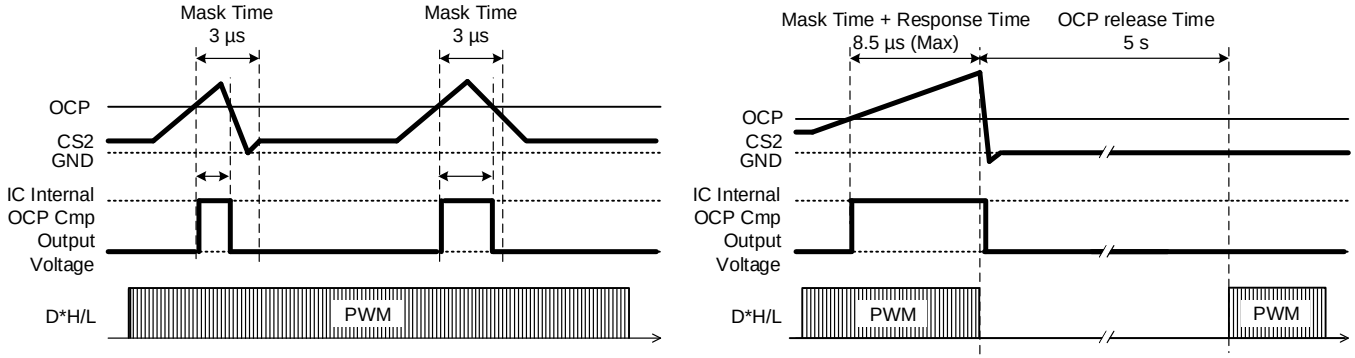


Figure 42. Overcurrent Protection Peripheral Circuit



(a) Noise Filter Operation (OCP Noise Mask = 2h) (No overcurrent detected during mask time)

(b) Protection Detection/Release Operation (OCP Noise Mask = 2h)

Figure 43. Overcurrent Protection Operation

Parameter name	Register Initial Value	Function	Description
OCP_PRTMSK	2h	Overcurrent protection disable setting	1h: Protection Disabled*(Note 1)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
OCP Level (OCP)	362h	Overcurrent protection detection threshold setting	44 mV to 210 mV, 0.23 mV step, OCP = 192d to 909d, 0d to 191d/910d to 1023d Prohibited setting
OCP Time (TOCP)	32h	Overcurrent protection time setting	0 s to 25.5 s, 100 ms step, TOCP = 0d to 255d
OCP Noise Mask	2h	Overcurrent protection malfunction prevention mask time setting	0h: 0 µs, 1h: 1 µs, 2h: 3 µs, 3h: 7 µs

(Note 1) Protection disable is enabled only when the register in OTP is changed.

5. Protection Functions - continued

(3) Over Temperature Protection (TSD: Thermal Shutdown)

OTP setting: TSD_PRTMSK, TTP

When the chip temperature exceeds 175 °C (Typ), the TSD protection is activated and all external FET output are turned OFF during the protection time (TTP/register default [32h]: 5 s [Typ]). The TSD protection circuit has a hysteresis width of 25 °C (Typ) and the TSD protection is released when the chip temperature is below 150 °C (Typ) after the protection time has elapsed.
The TSD protection circuit is designed prevent thermal runaway. Nevertheless, the guaranteed operating temperature range is exceeded at the time this circuit operates. Therefore, dimension the thermal management system with sufficient margin and ensure that this circuit is not used continuously after it has been activated, or that it is not used on the assumption that it will continue to operate.
In addition, the above set temperature is a design value; shipping inspection is not performed at high temperatures.

Parameter name	Register Initial Value	Function	Description
TSD_PRTMSK	2h	TSD protection disable setting	1h: Protection Disabled*(Note 1)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
TSD Time (TTP)	32h	TSD protection time setting	0 s to 25.5 s, 100 ms step TTP = 0d to 255d

(Note 1) Protection disable is enabled only when the register in OTP is changed.

(4) Over Voltage Protection (OVP: Over Voltage Protection)

OTP setting: OVP_PRTMSK, TOVP, OVP Noise Mask, OVP_THR_SEL, VG_OVP_SET

This protective function prevents large currents from flowing to the external FET in high voltage conditions. When a voltage higher than the specified power supply voltage is detected in a power supply voltage range and deviates from normal operation, all external FET are turned OFF during the protection time (TOVP/register default [32h]: 5 s [Typ]). Two settings can be selected by OVP_THR_SEL: 22 V detection, 20 V release, and 31 V detection, 29 V release. In addition, a mask time (OVP Noise Mask/register default [2h]: 3 µs [Typ]) is provided to prevent malfunction.

Parameter name	Register Initial Value	Function	Description
OVP_PRTMSK	2h	Over voltage protection disable setting	1h: Protection Disabled*(Note 2)*, 2h: Protection Enabled, 0h/3h: Prohibited setting
OVP Time (TOVP)	32h	Over voltage protection time setting	0 s to 25.5 s, 100 ms step TOVP = 0d to 255d
OVP Noise Mask	2h	Over voltage protection malfunction prevention mask time setting	0h: 0 µs, 1h: 1 µs, 2h: 3 µs, 3h: 7 µs
OVP_THR_SEL	0h	Over voltage protection threshold setting	0h: 22 V / 20 V, 1h: 31 V / 29 V
VG_OVP_SET*(Note 3)*	0h	Boost circuit operating setting at Over voltage protection	0h: Mute, 1h: Active

(Note 2) Protection disable is enabled only when the register in OTP is changed.
(Note 3) When overvoltage protection is disabled, set to Active. Over voltage abnormalities are ignored even with the Mute setting, but the external FET output is turned off by the VG undervoltage protection.

(5) Input Abnormal Frequency Protection (EFP: Error Frequency Protection)

OTP setting: EFP_PRTMSK

If the PWMIN input frequency exceeds 1025 Hz (Typ) for more than 150 ms (Typ), the error frequency protection is activated, and all external FET outputs turns OFF. If the input frequency returns within the normal range (7 Hz [Typ] to 1000 Hz [Typ]) for 15 consecutive cycles, the protection will be canceled.
If the error frequency detection duration is 150 ms (Typ) or less, the abnormal frequency is ignored and the previous duty is maintained.

Parameter name	Register Initial Value	Function	Description
EFP_PRTMSK	0h	Input abnormal frequency protection disable setting	0h: Protection Enabled, 1h: Protection Disabled

5. Protection Functions - continued

(6) V_{CC} Voltage Protection (UVLO: Under Voltage Lock Out)

This protective function prevents IC malfunction in the low voltage range that deviates from the recommended operating conditions. When V_{CC} drops to 6 V (Typ), the protection function activates and all external FET outputs turns OFF. In addition, boosted output voltage is turned OFF. The under voltage protection circuit has a 1 V (Typ) hysteresis and the protection is released when V_{CC} exceeds 7 V (Typ).

(7) V_G Under Voltage Protection (UVGP: Under VG Voltage Protection)

When V_G falls below V_{CC} + 3.0 V (Typ), the protection function activates and all external FET output turns OFF. The V_G under voltage protection function does not have hysteresis.

6. Other Functions

(1) Rotation Direction Setting

OTP setting: FR

The rotation direction can be changed in this setting (FR/register default [1h]: U→V→W).

Parameter name	Register Initial Value	Function	Description
FR	1h	Rotation direction setting	0h: U→W→V, 1h: U→V→W

Figure 44 and Figure 45 are timing charts of the output signal (U, V, W) and FG signal during normal mode.

FR = "1" setting (when U→V→W, step angle 0°)

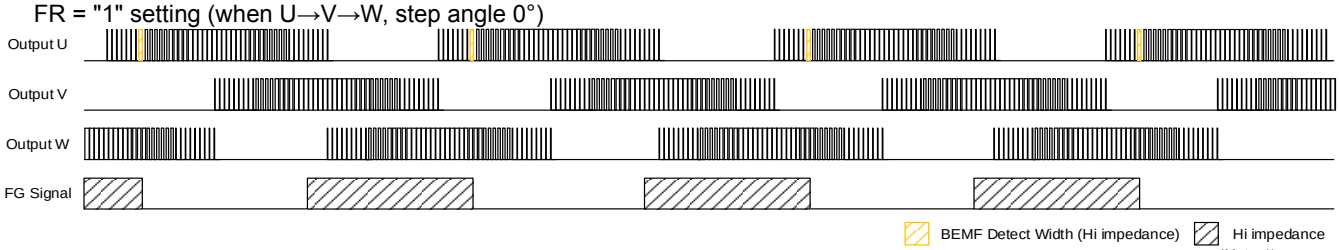


Figure 44. Timing Chart of Output Signal (U, V, W) and FG Signal during Normal Mode (FR = "1" Setting)*(Note 1)*

(Note 1) Three-phase modulation. The minimum duty section of the output signal waveform is not shown.

FR = "0" setting (when U→W→V, step angle 0°)

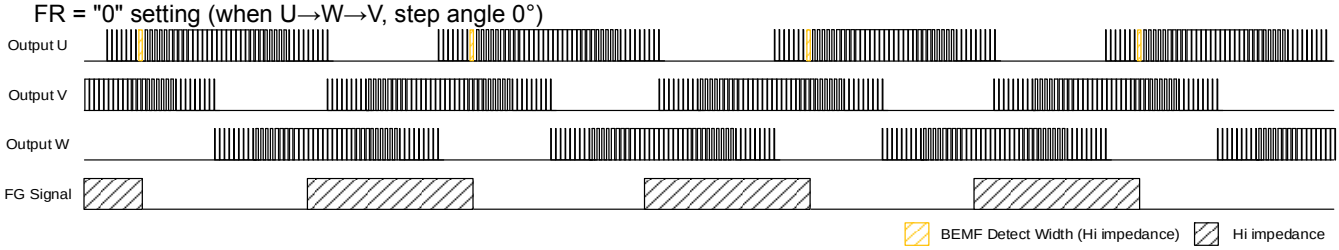


Figure 45. Timing Chart of Output Signal (U, V, W) and FG Signal during Normal Mode (FR = "0" Setting)*(Note 2)*

(Note 2) Three-phase modulation. The minimum duty section of the output signal waveform is not shown.

6. Other Functions - continued

(2) OTP Auto Refresh Function in Standby (OTP Reading)

OTP setting: AR_STB_OFF

Setting value changes other than writing to OTP register will automatically overwrite the written OTP value during IC standby mode (PWMIN input command value 0 %/100 %).
In addition, this function can be masked by the standby OTP auto refresh function mask setting (AR_STB_OFF/register default [1h]: mask enabled)

Parameter name	Register Initial Value	Function	Description
AR_STB_OFF	1h	Standby OTP Auto Refresh switching setting	0h: Mask disabled (for normal use), 1h: Mask enabled (for parameter evaluation)

(3) 2-wire Serial Communication

The formats and signal timing for communicating with IC are shown below.

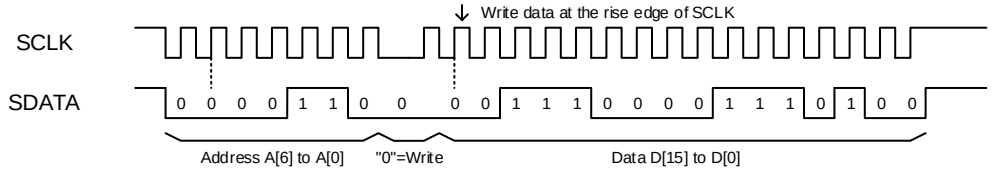


Figure 46. 2-wire Serial Communication Write Format (e.g. Register Address: 06h, Data: 3874h)

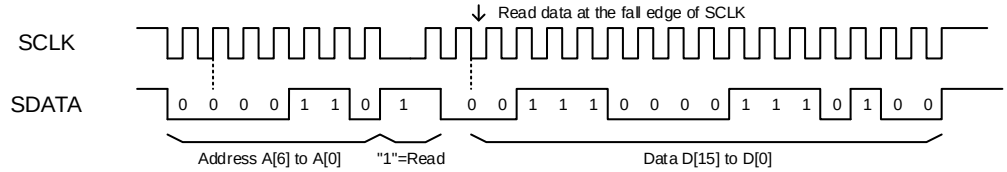


Figure 47. 2-wire Serial Communication Read Format (e.g. Register Address: 06h, Data: 3874h)

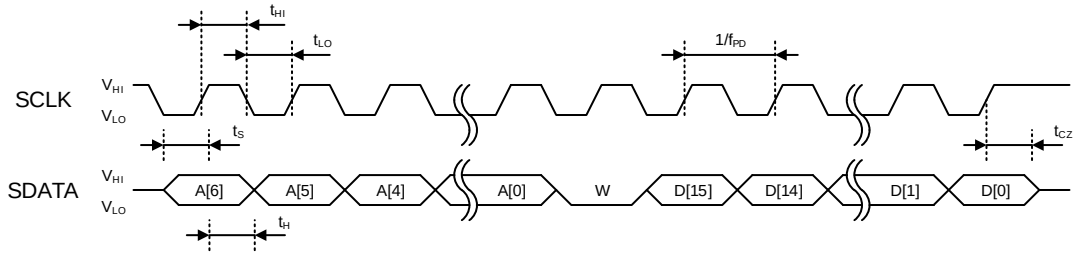


Figure 48. 2-wire Serial Communication Write Operation Timing

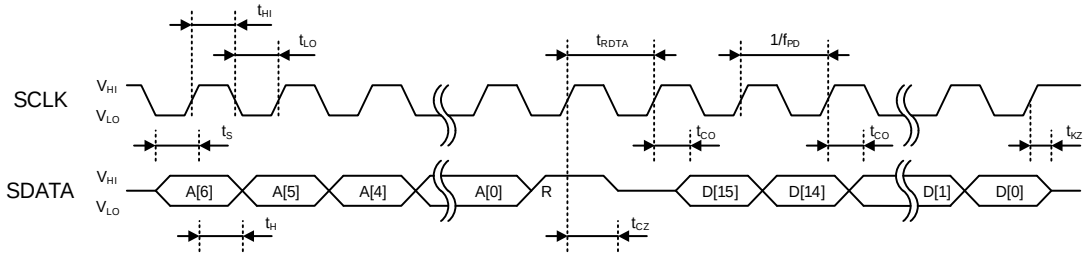


Figure 49. 2-wire Serial Communication Read Operation Timing

(3) 2-wire Serial Communication – continued

2-wire Serial Communication Operation Timing Characteristics (Design Value)

Parameter	Symbol	Min	Typ	Max	Unit
SDATA/SCLK High voltage	V_{HI}	V_{REG50} - 1.2	-	V_{REG50}	V
SDATA/SCLK Low voltage	V_{LO}	0	-	0.8	V
2-wire serial communication operating frequency	f_{PD}	300	500	700	kHz
SCLK signal High Period	t_{HI}	600	-	1400	ns
SCLK signal Low Period	t_{LO}	600	-	1400	ns
Data read switching time	t_{RDTA}	1000	-	4000	ns
Data setup time	t_S	300	-	800	ns
Data hold time	t_H	300	-	800	ns
Read data output start time	t_{CO}	-	100	-	ns
I/O switching time [Input to Hi-Z]	t_{KZ}	-	100	-	ns
I/O switching time [Hi-Z to Output]	t_{CZ}	300	-	800	ns

Description of Operation - continued

7. OTP

The IC is equipped with an OTP (One Time Programmable Rom). Each setting value in the register map can be written to OTP. Each setting written in OTP is automatically read from OTP to each register after IC power is turned on.

(1) Sample Circuit for Writing OTP

The following is a sample circuit diagram for performing write operation to OTP while external components are mounted on the board. NOTE: The user should stop the motor when writing to OTP.

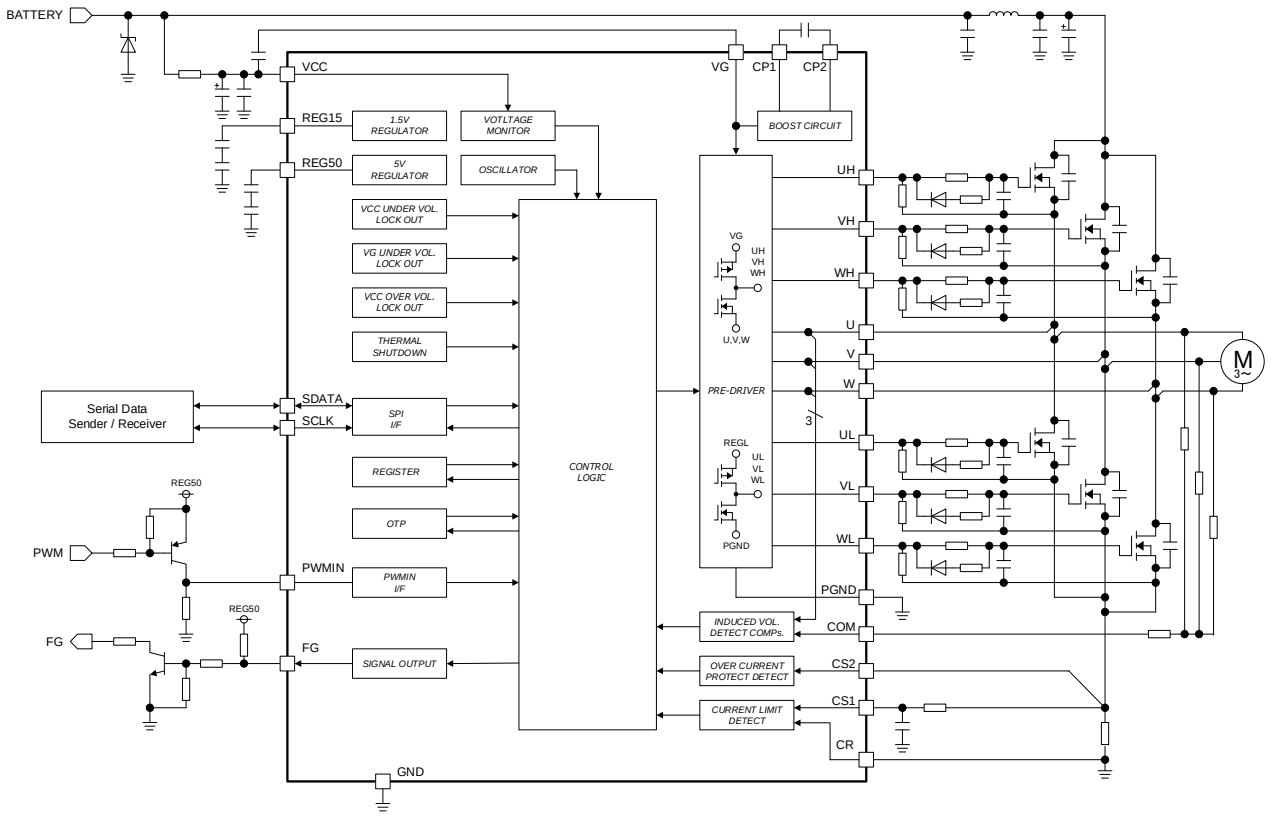


Figure 50. OTP Write Operation Circuit Diagram (External Components Mounted)

Preliminary steps for writing to OTP

1. Connect PWMIN pin to VREG50. (or apply 5 V externally)
2. Connect SCLK pin to SPI communication CLK and SDATA pin to SPI data input/output.
3. Apply 12 V (Typ) to the power supply (V_{CC}). The table below shows V_{CC} voltage ranges.
4. Follow the "OTP Write Procedures" to perform the write operation to OTP.
5. To check OTP writing contents, turn OFF the power once.

Parameter	Min	Typ	Max	Unit
VCC Applied Voltage	8	-	18	V
SCLK, SDATA Input High Voltage	4.5	-	5.6	V
SCLK, SDATA Input Low Voltage	0	-	0.8	V
PWMIN Applied Voltage	0	-	0.8	V

7. OTP - continued

(2) OTP Write Count

OTP is a memory that can be written only once to a single address. Due to the characteristic of OTP, it is not possible to test all memory cells prior to shipment. If there is an abnormality in the memory cell, the write operation to OTP may fail. Therefore, the IC can perform write operations up to three times. Also, OI_WR_STC (Register Address: 0x2C, Data: D[1:0]) stores the number of times the write operation to OTP was performed.

If OI_WR_STC = 0x3, no further write operations can be performed at that address.

CNTERR (Register Address: 0x2C, Data: D[6]) stores the result that if a further write operation is performed to an address that has already been written to OTP three times, the write operation cannot be performed. The user is advised to check these registers for the number of already performed writes and whether further write operations are possible.

Furthermore, to prevent consuming OTP memory with the same data, a function to prevent writing the same data is included. If OTP writing is executed when OTP has already been written at least once, the last written data is compared with the new data to be written, and if the values match, the writing operation to the corresponding address is automatically aborted. The comparison result is CMP_DATA_FLG (Register Address: 0x2C, Data: D[5]).

(3) Power Supply During OTP Write Operation

If the power supply voltage (V_{CC}) during a write operation to OTP is low, OTP may not be written sufficiently, and the data may be lost due to aging. This IC monitors V_{CC} when writing to OTP, and if V_{CC} is low, it outputs an error and stops writing to OTP. The voltage status of the write operation is stored in VPP28_UVLO_VCHECK (Register Address: 0x2C, Data: D[3]).

In addition, since current flows to the IC during write operation to OTP, set the current limit of the power-supply unit to 100 mA or more. Even if V_{CC} dropped due to power line impedance, the IC outputs an error and stops the write operation to OTP. So, the number of OTP writes may increase. Do not use an OTP writing on products that detects VPP28_UVLO_VCHECK.

7. OTP - continued

(4) OTP Write Procedures

The following table shows the sequence of steps for writing to OTP. Write operations to OTP are performed for each address. When writing to multiple OTP addresses, start with sequence No.1 to No.6. Next, repeat the steps from No.7-1 to No.7-7 for each address. No.7-4 sequence requires approximately 15 ms for each address. Finally, execute sequence No.8 to No.23.

・No.1 to No.6: Start Sequence

This command is set only once prior to OTP writing.

No.	Register Address [HEX]	Write = 0x0 Read = 0x1	Data [HEX]	Contents
1	0x60	0x0	0x5102	Starting sequence (OTP write setting)
-	Waiting time: 10 µs			
2	0x2F	0x0	0xAAAA	Starting sequence (OTP accessing enabled)
-	Waiting time: 10 µs			
3	0x75	0x0	0x3000	Starting sequence (OTP write checking function enable)
-	Waiting time: 10 µs			
4	0x7B	0x0	0x3001	Starting sequence (OTP setting)
-	Waiting time: 10 µs			
5	0x73	0x0	0x0800	Starting sequence (Internal power 5.4 V enable)
-	Waiting time: 200 µs			
6	0x5C	0x0	0x0000	Motor drive core operation stop sequence
-	Waiting time: 1 ms			

・No.7:OTP Write Sequence

When writing to several OTP addresses, rewrite the values of 2Ah and 2Dh and repeat No.7. Regarding the OTP write result, it is necessary to check the values of 2Ch[7:5] and [3:0] for each address to confirm that the write was performed correctly. For details on PASS/FAIL judgment, see "OTP Related Register Details [PASS/FAIL Judgment]".

No.	Register Address [HEX]	Write = 0x0 Read = 0x1	Data [HEX]	Contents
7-1	0x5B	0x1	0x0000	Check the protection status of IC. Other than 0x0000 is a fail judge.
-	Waiting time: 200 µs			
7-2	0x2A	0x0	0x■■00	Set OTP address ■■
-	Waiting time: 500 µs			
7-3	0x2C	0x1	0x0000 or 0x200X	Check initial status of OTP. (If ECC correction was performed in the previous write.) 1st time : 0x0000 2nd time : 0x0001 (or 0x2001) 3rd time : 0x0002 (or 0x2002) Other than the above result is a fail judge.
-	Waiting time: 200 µs			
7-4	0x2D	0x0	0x□□□□	Set OTP data □□□□
-	Waiting time: 15 ms			
7-5	0x2C	0x1	0x000X or 0x200X	Confirm the results written to OTP. (If ECC correction was performed in the previous write.) 1st time : 0x0001 (or 0x2001) 2nd time : 0x0002 (or 0x2002) 3rd time : 0x0003 (or 0x2003) Other than the above result is a fail judge.
-	Waiting time: 200 µs			
7-6	0x2A	0x0	0x■■00	Set OTP address ■■
-	Waiting time: 500 µs			
7-7	0x2E	0x1	0x□□□□	Confirm □□□□ data written in OTP
-	Waiting time: 200 µs			
-	When OTP write operation is performed by another address, return to No.7-1. If no write operation is performed, proceed to No.8.			

(4) OTP Write Procedures - continued

・No.8 to No.20 : Write check sequence
After the OTP is written, a 15-year read guarantee check is performed on the entire area, including areas where the OTP has not been written, in two separate areas. The results are stored in 29h [0] so check the values for each area. For details on PASS/FAIL judgment, see "OTP Related Register Details [PASS/FAIL Judgment]".

No.	Register Address [HEX]	Write = 0x0 Read = 0x1	Data [HEX]	Contents
8	0x7B	0x0	0x0001	Write check sequence (OTP setting)
-	Waiting time: 10 µs			
9	0x75	0x0	0x0020	Write check sequence (OTP all area check function enable)
-	Waiting time: 10 µs			
10	0x29	0x0	0x0420	Write check sequence (OTP all area check flag clear)
-	Waiting time: 10 µs			
11	0x29	0x0	0x4320	Write check sequence (OTP all area check ①)
-	Waiting time: 3 ms			
12	0x29	0x1	0xXXX6	Write check sequence (OTP all area confirmation ①)
-	Waiting time: 200 µs			
13	0x29	0x0	0x0540	Write check sequence (OTP all area check flag clear ①)
-	Waiting time: 10 µs			
14	0x29	0x0	0x0420	Write check sequence (OTP all area check flag clear ②)
-	Waiting time: 10 µs			
15	0x29	0x0	0x5320	Write check sequence (OTP all area check ②)
-	Waiting time: 3 ms			
16	0x29	0x1	0xXXX6	Write check sequence (OTP all area confirmation ②)
-	Waiting time: 200 µs			
17	0x29	0x0	0x0540	Write check sequence (OTP all area check flag clear ①)
-	Waiting time: 10 µs			
18	0x29	0x0	0x0170	Write check sequence (OTP power reset ①)
-	Waiting time: 10 µs			
19	0x29	0x0	0x0110	Write check sequence (OTP power reset ②)
-	Waiting time: 10 µs			
20	0x29	0x0	0x0010	Write check sequence (OTP all area confirmation check reset)
-	Waiting time: 10 µs			

・No.21 to No.23 : End sequence
This command is set only once after OTP writing. Be sure to execute "End sequence" to prevent errors in OTP writing.

No.	Register Address [HEX]	Write = 0x0 Read = 0x1	Data [HEX]	Contents
21	0x2F	0x0	0x0000	End sequence (OTP access disable)
-	Waiting time: 10 µs			
22	0x73	0x0	0x0000	End sequence (Internal power 5.4 V disabled)
-	Waiting time: 1 ms			
23	0x60	0x0	0x0000	End sequence (OTP write setting cancel)
-	Waiting time: 10 µs			

(5) Temperature Condition After Writing OTP

Non-volatile memory, including OTP, are highly temperature dependent and data may be lost when exposed to temperatures above 200 °C. If exposed to temperatures above 200 °C, temperature and time are important. One of the conditions where the temperature exceeds 200 °C after writing data to OTP is due to solder reflow during mounting, but with this product's solder reflow mounting conditions, even in an environment with an absolute maximum rating of 150 °C, data can be retained for at least 15 years.

7. OTP - continued

(6) OTP Related Register Map

Register Name	Register Address [6:0]	W/R	Data[15:0]														
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIP STATUS Command (Protection Status)	5Bh	W/R	CHIP STATUS															
			1'b0	1'b0	1'b0	-	-	-	-	-	-	-	-	-	-	-	-	-
			TSD	OCP	OVP													
OTP BIST Command (OTPBIST)	29h	W/R	OTPBIST															
			-	-	-	-	-	-	-	-	-	-	-	-	-	1'b0	1'b0	1'b0
																OI_OB_STARTED_IH	OI_OB_END_IH	OI_OB_FAIL_IH
OTP Address (OTPADDR)	2Ah	W/R	OTPADDR															
			8'b00_0000								-	-	-	-	-	-	-	-
			OI_OC_ADDR_OD[7:0]															
OTP Status Check (OTPST)	2Ch	R	OTPST															
			1'b0	-	1'b0	-	-	1'b0	1'b0	1'b0	1'b0	-	1'b0	-	-	1'b0	1'b0	1'b0
			OB_MM_FAIL		ECCERR_S			ORP	OWP	OB	ECCERR_M		CMP_DATA_FLG			OI_OB_FAIL	OI_WR_STC[1:0]	
OTP Write (OTPWR)	2Dh	W/R	OTPWR															
			16'b0000_0000_0000_0000															
			OI_OC_WDATA_OD[15:0]															
OTP Read (OTPRD)	2Eh	R	OTPRD															
			16'b0000_0000_0000_0000															
			OI_OC_RDATA_ID[15:0]															

(7) OTP Related Register Description

Register Address	Data	Register Name	Function	Judgement
5Bh	[15]	TSD	Over Temperature Protection Status Detection Flag	1'b0 : TSD Protection Inactive 1'b1 : TSD Protection Active
	[14]	OCP	Over Current Protection Status Detection Flag	1'b0 : OCP Protection Inactive 1'b1 : OCP Protection Active
	[13]	OVP	Over Voltage Protection Status Detection Flag	1'b0 : OVP Protection Inactive 1'b1 : OVP Protection Active
29h	[2]	OI_OB_STARTED_IH	All OTP area check START Flag	1'b0 : All OTP area check incomplete 1'b1 : All OTP area check ongoing
	[1]	OI_OB_END_IH	All OTP area check END Flag	1'b0 : All OTP area check incomplete or not implemented 1'b1 : All OTP area ongoing check complete
	[0]	OI_OB_FAIL_IH	All OTP area check results	1'b0 : All OTP area check - OK result 1'b1 : All OTP area check - NG result
2Ah	[15:8]	OI_OC_ADDR_OD[7:0]	OTP Address Setting	-
2Ch	[15]	OB_MM_FAIL	Existing stored data and new store data comparison check If OTP has never been stored, no comparison check is performed	1'b0 : OTP STORE Data OK (Existing data ≠ new data, or never been stored) 1'b1 : OTP STORE Data NG (Existing data = new data)
	[13]	ECCERR_S	OTP ECC Error Flag (1bit)	1'b0 : OTP ECC OK 1'b1 : OTP ECC NG
	[10]	ORP	OTP read operation ongoing check	1'b0 : OTP read operation complete or not implemented 1'b1 : OTP read operation ongoing
	[9]	OWP	OTP write operation ongoing check	1'b0 : OTP write operation complete or not implemented 1'b1 : OTP write operation ongoing
	[8]	OB	OTP operation ongoing check	1'b0 : OTP operation standby 1'b1 : OTP operation BUSY
	[7]	ECCERR_M	OTP ECC Error Flag (multiple bits)	1'b0 : OTP ECC OK 1'b1 : OTP ECC NG
	[5]	CMP_DATA_FLG	OTP write data comparison check Compare OTP write data and read data	1'b0 : OTP STORE Data OK. 1'b1 : OTP STORE Data NG
	[2]	OI_OB_FAIL	OTP BIST Practice result flag (Normal and Counter area)	1'b0 : OTP 15 years read guarantee check OK 1'b1 : OTP 15 years read guarantee check NG
	[1:0]	OI_WR_STC[1:0]	OTP write count check	2'b00 : No OTP write count 2'b01 : 1 OTP write count 2'b10 : 2 OTP write count 2'b11 : 3 OTP write count
2Dh	[15:0]	OI_OC_WDATA_OD[15:0]	OTP write data setting	-
2Eh	[15:0]	OI_OC_RDATA_ID[15:0]	OTP read data	-

7. OTP - continued

(8) OTP Related Register Details [PASS/FAIL Judgment]

5Bh Data READ PASS/FAIL Judgment

OTP Pre-Write Check

5Bh[15:13]	Judge	Detail
16'b000*_****_****_****	OK	No Active IC Protection
16'b1***_****_****_****	NG	TSD Protection Active
16'b*1**_****_****_****	NG	OCP Protection Active
16'b**1*_****_****_****	NG	OVP Protection Active
Others	NG	Others

2Ch Data READ PASS/FAIL Judgment

OTP Pre-Write Check

2Ch[10],[8],[2],[1:0]	Judge	Detail
16'b0000_0000_0000_0000	OK	No OTP Data Write
16'b00*0_0000_0000_0001	OK	1 OTP Write Count
16'b00*0_0000_0000_0010	OK	2 OTP Write Count
16'b00*0_0000_0000_0011	NG	OTP Write Count NG
16'b****_****_****_*1**	NG	OTP 15 years read guarantee NG
16'b****_*1*1_****_****	NG	OTP read operation ongoing (insufficient wait time before 2Ch read)
Others	NG	Others

OTP Write Check

2Ch[15],[13],[10:8],[7],[2],[1:0]	Judge	詳細
16'b00*0_0000_0000_0001	OK	1 OTP Write
16'b00*0_0000_0000_0010	OK	2 OTP Write
16'b00*0_0000_0000_0011	OK	3 OTP Write
16'b0010_0000_0000_00**	OK	1-bit write data error ECC data correction
16'b****_****_*00*_0000	NG	No OTP Data Write
16'b****_****_****_*1**	NG	OTP 15 years read guarantee NG
16'b****_****_**1*_****	NG	OTP Read/Write Data Comparison NG
16'b****_****_1***_****	NG	Write Data Error 2bit or more
16'b****_**11_****_****	NG	OTP write operation ongoing (insufficient wait time before 2Ch read)
16'b****_*1*1_****_****	NG	OTP read operation ongoing (insufficient wait time before 2Ch read)
16'b1***_****_****_****	NG(Note1)	Existing OTP stored data = New OTP store data
Others	NG	Others

(Note 1) Basically, store the same data is not assumed, so it is judged as NG. However, if executing OTP writing multiple times or if only some addresses contain the same data, etc, it is predetermined that the same data will be stored, please judge it as OK

29h Data READ PASS/FAIL Judgment

OTP Write Final Check

29h[2:0]	Judge	詳細
16'b****_****_****_*110	OK	All OTP area check OK
16'b****_****_****_*111	NG	All OTP area check NG
16'b****_****_****_*100	NG	All OTP area check ongoing (insufficient wait time before 29h read)
Others	NG	Others

Thermal Resistance

Heat generated by the power consumed by IC is radiated from the mold resin and lead frame of the packaging. The parameter that indicates heat dissipation (resistance to heat escape) is called thermal resistance. The thermal resistance from the chip junction to the ambient temperature is θ_{JA} (°C/W), and the thermal resistance parameter from the chip junction to the package top center is Ψ_{JT} (°C/W). The thermal resistance is divided into the package part and the substrate part, and the thermal resistance of the package part depends on the constituent materials such as mold resin and lead frame, while the thermal resistance of the substrate part depends on the substrate heat dissipation properties such as material, size and copper foil area. Therefore, the heat resistance can be reduced by heat radiation measures such as mounting a heat sink on the mounting board. The thermal resistance calculation equation is shown below, and the thermal resistance model is shown in Figure 51.

Calculation formula

$$\theta_{JA} = \frac{Tj-Ta}{P} \text{ [°C/W]}$$

$$\psi_{JT} = \frac{Tj-Tt}{P} \text{ [°C/W]}$$

θ_{JA}: Thermal Resistance (°C/W) from Junction to Ambient
ψ_{JT}: Thermal Resistance Parameter from Junction to Package Top Center (° C/W)
Tj: Junction Temperature (°C)
Ta: Ambient Temperature (°C)
Tt: Package Top Center Temperature (°C)
P: Power Consumption (W)

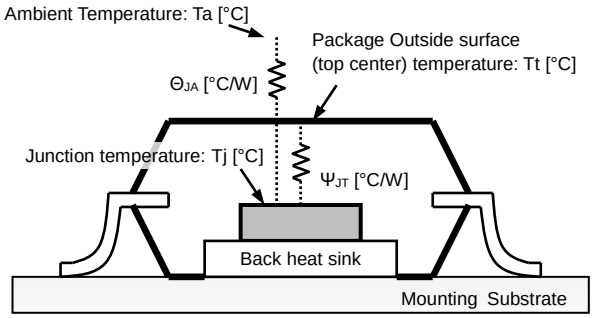
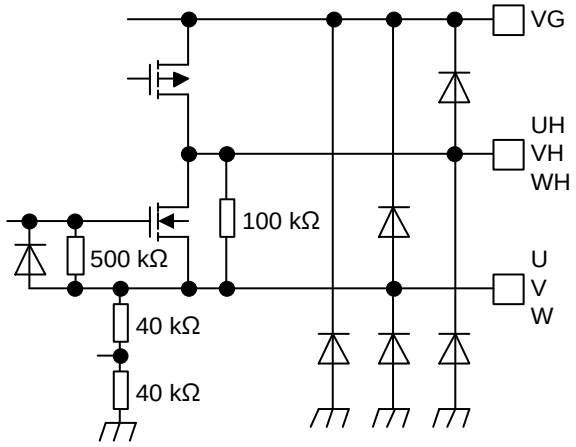
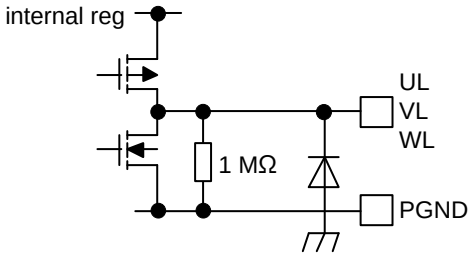
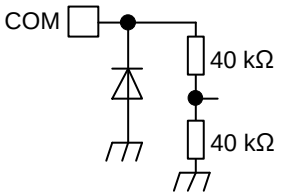
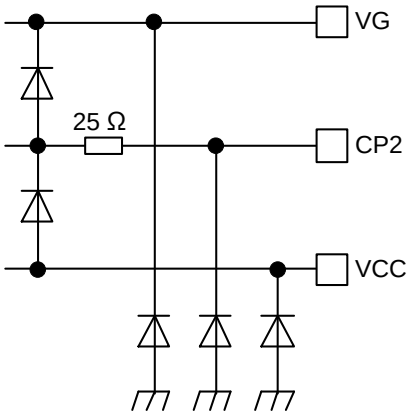
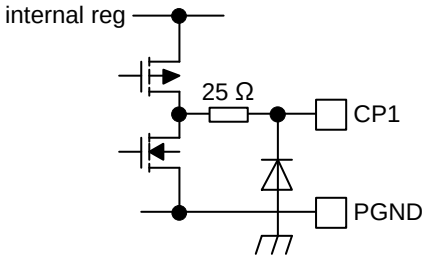
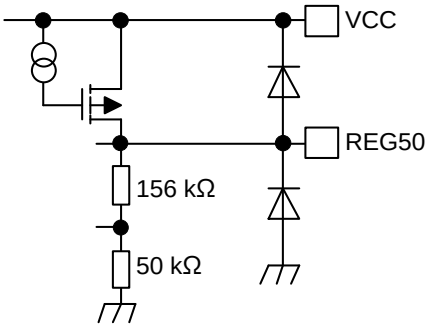


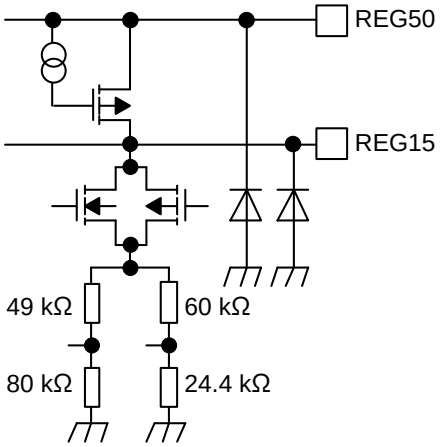
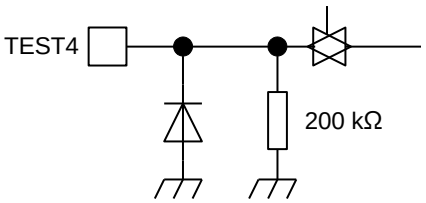
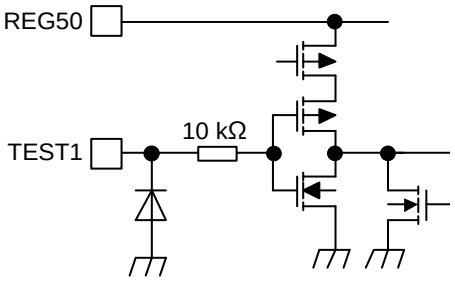
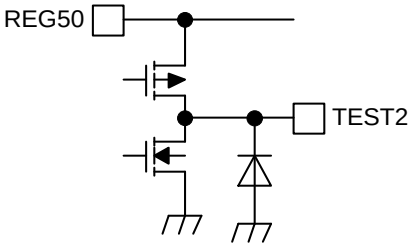
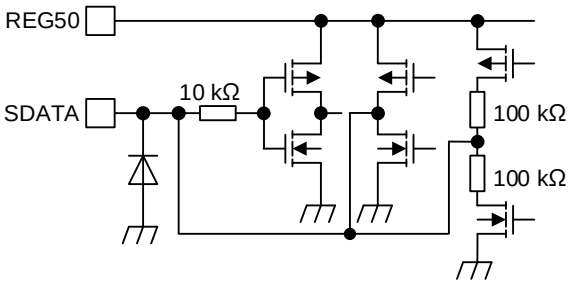
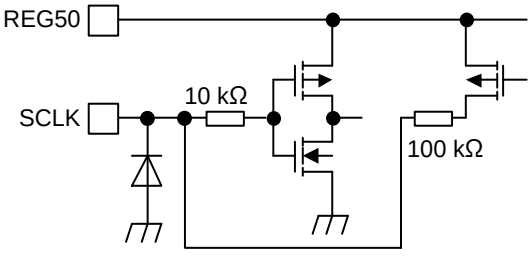
Figure 51. Thermal Resistance Model of Package

θ_{JA}, ψ_{JT} varies depending on the chip size and power consumed by the mounted IC even if it is used in the same package. It also varies depending on the measuring environment such as ambient temperature, mounting conditions, and wind speed.

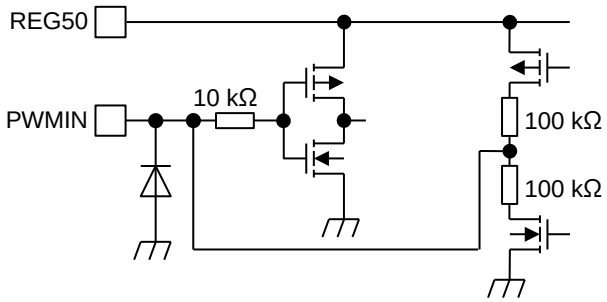
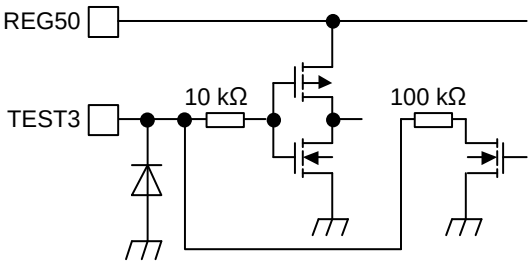
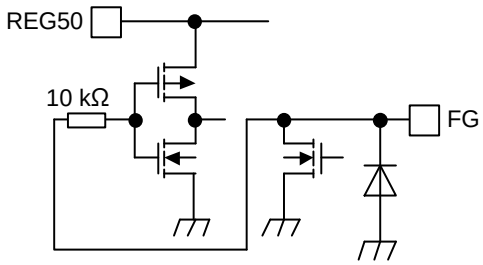
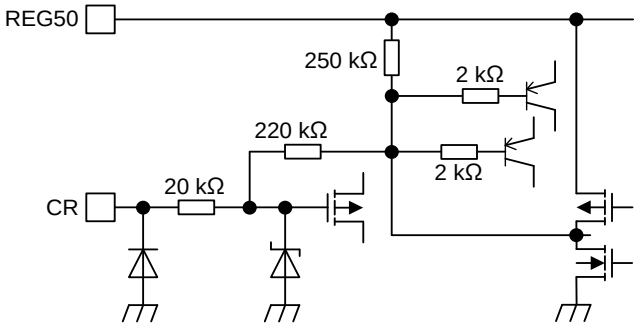
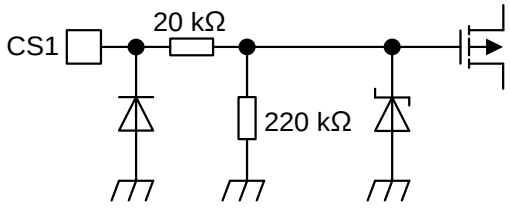
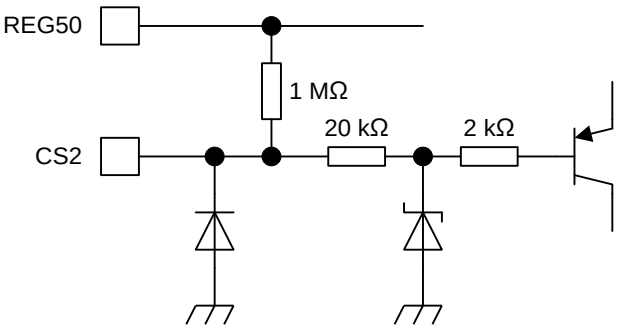
I/O Equivalence Circuit (Typical values for resistance)

2, 3, 8, 9, 37, 38	VH, V, U, UH, W, WH	5, 6, 35, 40	VL, UL, WL, PGND
			
10	COM	14, 15	VG, CP2
			
17	CP1	19	REG50
			

I/O Equivalence Circuit - continued

22	REG15	23	TEST4
			
24	TEST1	25	TEST2
			
26	SDATA	27	SCLK
			

I/O Equivalence Circuit - continued

28	PWMIN	29	TEST3
			
30	**FG**	**32**	**CR**
			
33	**CS1**	**34**	**CS2**
			

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

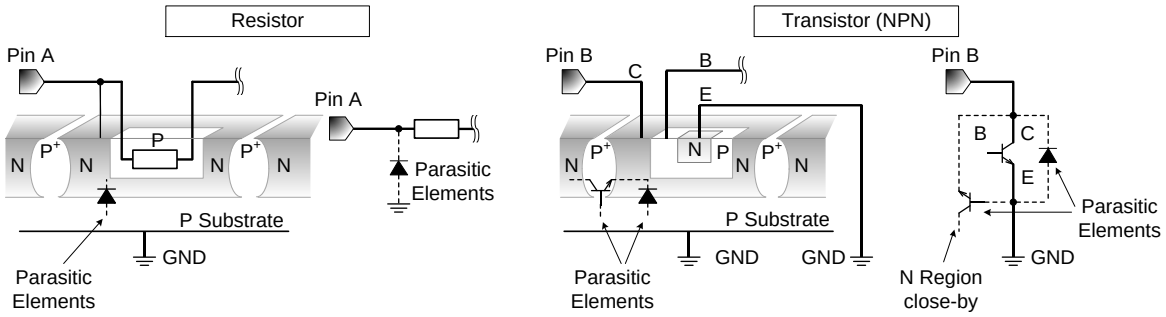


Figure 52. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

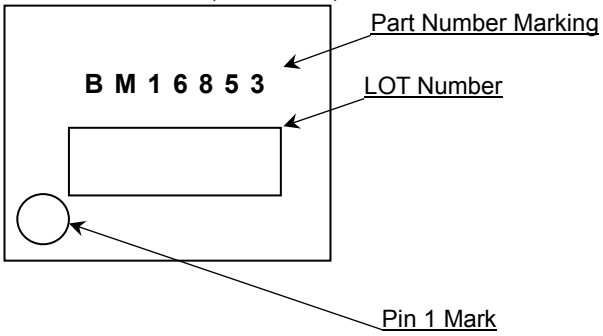
B M 1 6 8 5 3 M U F	-	CE 2

Packaging
MUF: VQFN40FDV060

Product rank
C: Automotive ranked products
Packaging and forming specifications
E2: Embossed tape and reel

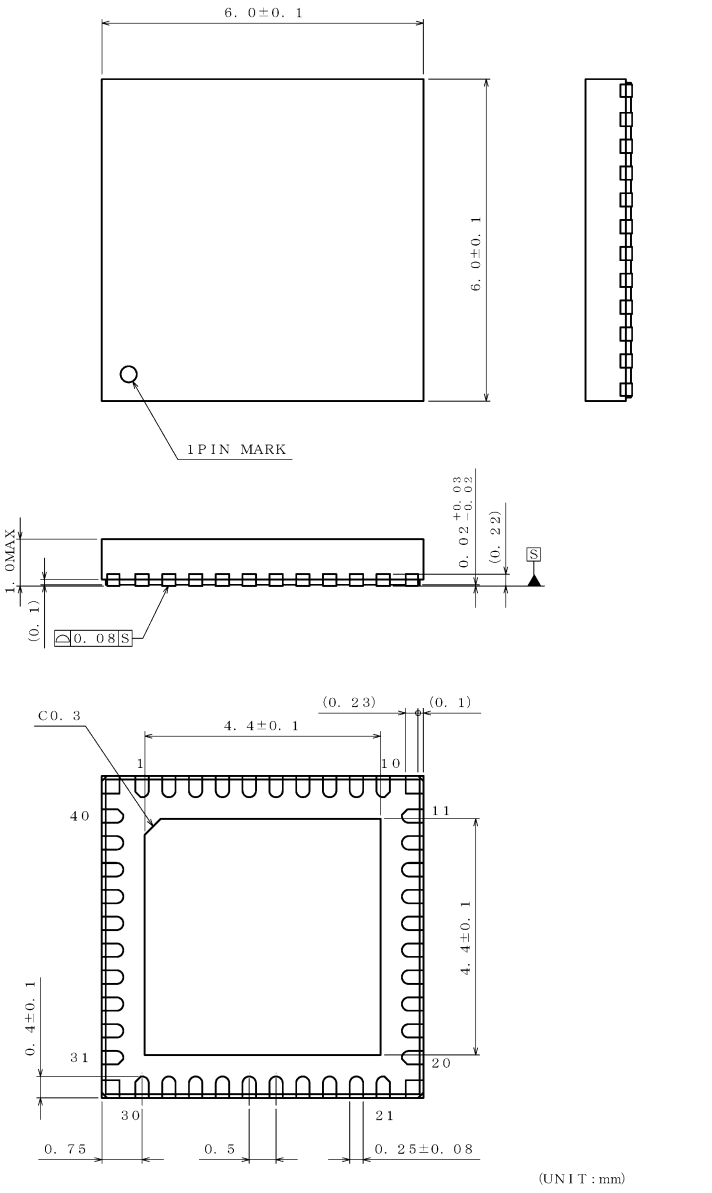
Marking Diagram

VQFN40FDV060 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN40FDV060



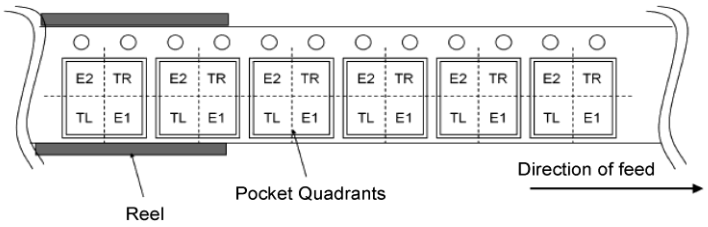
(UNIT:mm)

PKG:VQFN40FDV060
Drawing No. EX446-5001

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision history

Date	Revision	Changes
05.Mar.2025	001	New Create

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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