Automotive Motor Driver Series

14CH Half-bridge Driver with Built-in SPI for Automotive

BD16940MUF-C

General Description

BD16940MUF-C is a 14-channel half-bridge driver designed for automotive applications. This product can directly drive a small DC brush motor. Each output can be independently controlled into three modes: High output, Low output, and Hi-Z output. The 16-bit serial interface (SPI) allows control from an external MCU.
This product has a high withstand voltage (maximum rating 40 V), low ON resistance and small package. It can contribute to high reliability, low power consumption and cost reduction to product applications.

Features

- AEC-Q100 Qualified *(Note 1)*
- Functional Safety Supportive Automotive Products
- 1.0 A DMOS Half-bridge 14 Circuits
- Three Mode Output Control (High, Low & High Impedance)
- Built-in PWM Control Mode (Frequency Selectable)
- Low Standby Current
- Built-in Protection Diode Against Output Reverse Voltage
- Over Current Protection (OCP)
- Under Current Detection (UCD)
- Over Voltage Protection with OVPSEL Mode (VSOV)
- Under Voltage Lock Out (VSUV)
- Thermal Shutdown (TSD), Thermal Warning (TW)
- Static Open/Short Detection (SOS)
- Built-in Current Detection AMP (2ch)
- Direct Error Output Pin / Current Detection AMP (1ch) Selection

(Note 1) Grade 1

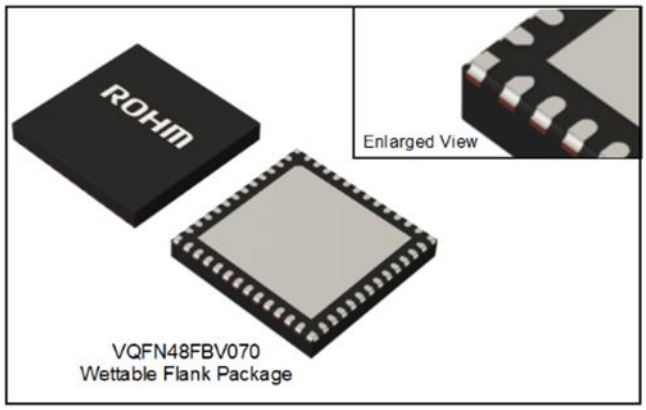
Applications

Automotive Body Electronics, HVAC, Door Mirrors, etc.

Key Specifications

- Supply Voltage (VS): 6.3 V to 32 V
- Supply Voltage (VCC): 3.0 V to 5.5 V
- Standby Current (VS): 0 µA (Typ)
- Standby Current (VCC): 0 µA (Typ)
- Output Current: 1.0 A (Max)
- Output ON Resistance (High Side): 0.85 Ω (Typ)
- Output ON Resistance (Low Side): 0.55 Ω (Typ)
- SPI Clock Frequency: 4.1 MHz (Max)
- Junction Temperature: -40 °C to +150 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN48FBV070	7.0 mm x 7.0 mm x 1.0 mm



Typical Application Circuit

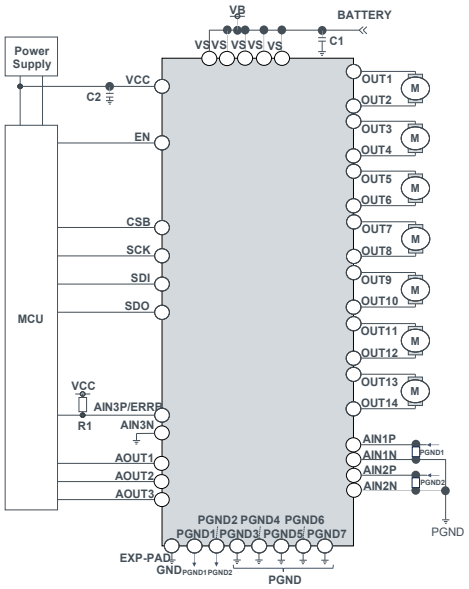


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

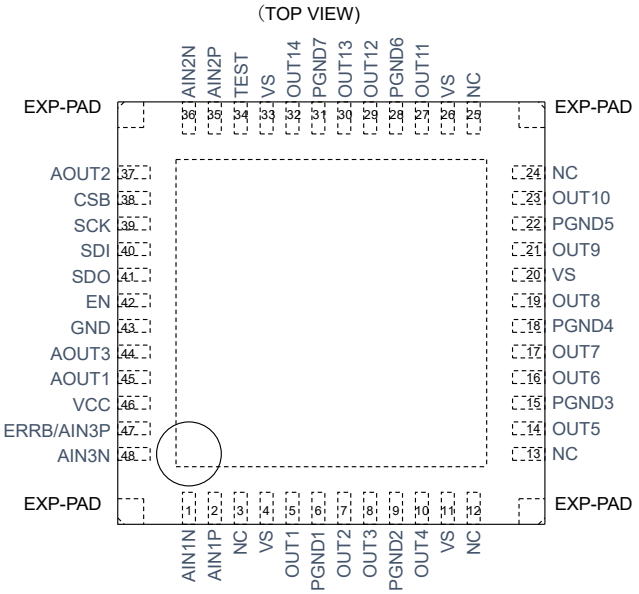


Figure 2. Pin Configuration

Block Diagram

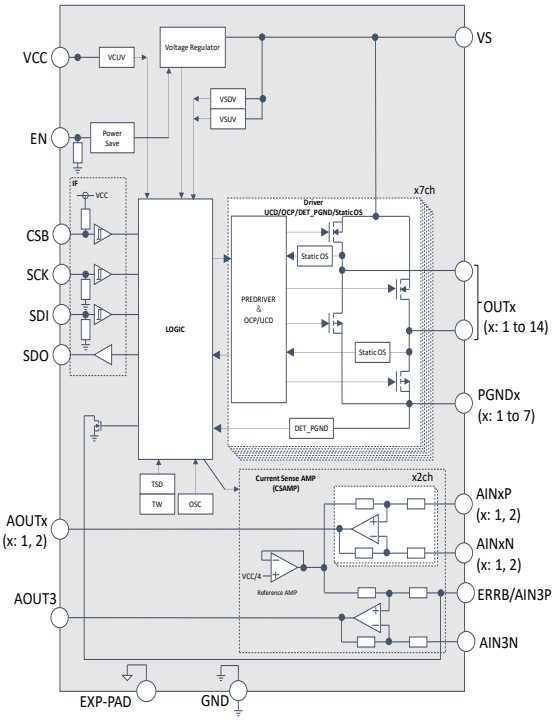


Figure 3. Block Diagram

Pin Description

No	Pin Name	Function	No	Pin Name	Function
1	AIN1N	Current sense amplifier 1 inverted input	25	NC	No connection (No internal connection)
2	AIN1P	Current sense amplifier 1 non-inverted input	26	VS	Power supply voltage input
3	NC	No connection. (No internal connection)	27	OUT11	Half-bridge output 11
4	VS	Power supply voltage input	28	PGND6	OUT11 to 12 power ground.
5	OUT1	Half-bridge output 1	29	OUT12	Half-bridge output 12
6	PGND1	OUT1 to 2 power ground.	30	OUT13	Half-bridge output 13
7	OUT2	Half-bridge output 2	31	PGND7	OUT13 to 14 power ground.
8	OUT3	Half-bridge output 3	32	OUT14	Half-bridge output 14
9	PGND2	OUT3 to 4 power ground.	33	VS	Power supply voltage input
10	OUT4	Half-bridge output 4	34	TEST	Test mode input *(Note 1)*
11	VS	Power supply voltage input	35	AIN2P	Current sense amplifier 2 non-inverted input
12	NC	No connection (No internal connection)	36	AIN2N	Current sense amplifier 2 inverted input
13	NC	No connection (No internal connection)	37	AOUT2	Current sense amplifier 2 output
14	OUT5	Half-bridge output 5	38	CSB	SPI chip selector input (Low active)
15	PGND3	OUT5 to 6 power ground.	39	SCK	SPI clock input
16	OUT6	Half-bridge output 6	40	SDI	SPI data input
17	OUT7	Half-bridge output 7	41	SDO	SPI data output
18	PGND4	OUT7 to 8 power ground.	42	EN	Enable input
19	OUT8	Half-bridge output 8	43	GND	Control unit ground
20	VS	Power supply voltage input	44	AOUT3	Current sense amplifier 3 output
21	OUT9	Half-bridge output 9	45	AOUT1	Current sense amplifier 1 output
22	PGND5	OUT9 to 10 power ground.	46	VCC	Control unit power supply
23	OUT10	Half-bridge output 10	47	ERRB/ AIN3P	Error output (Low active) / Current sense amplifier 3 non-inverted input
24	NC	No connection. (No internal connection)	48	AIN3N	Current sense amplifier 3 Inverted input
	EXP-PAD	The center EXP-PAD requires a short connection to the GND pin outside the IC. The center EXP-PAD and corner EXP-PADs are shorted inside the IC.			

(Note 1) Connect TEST to GND through a resistance.

Application Examples

Application Circuit (e.g., brushed DC motor drive, 3CH CSAMP)

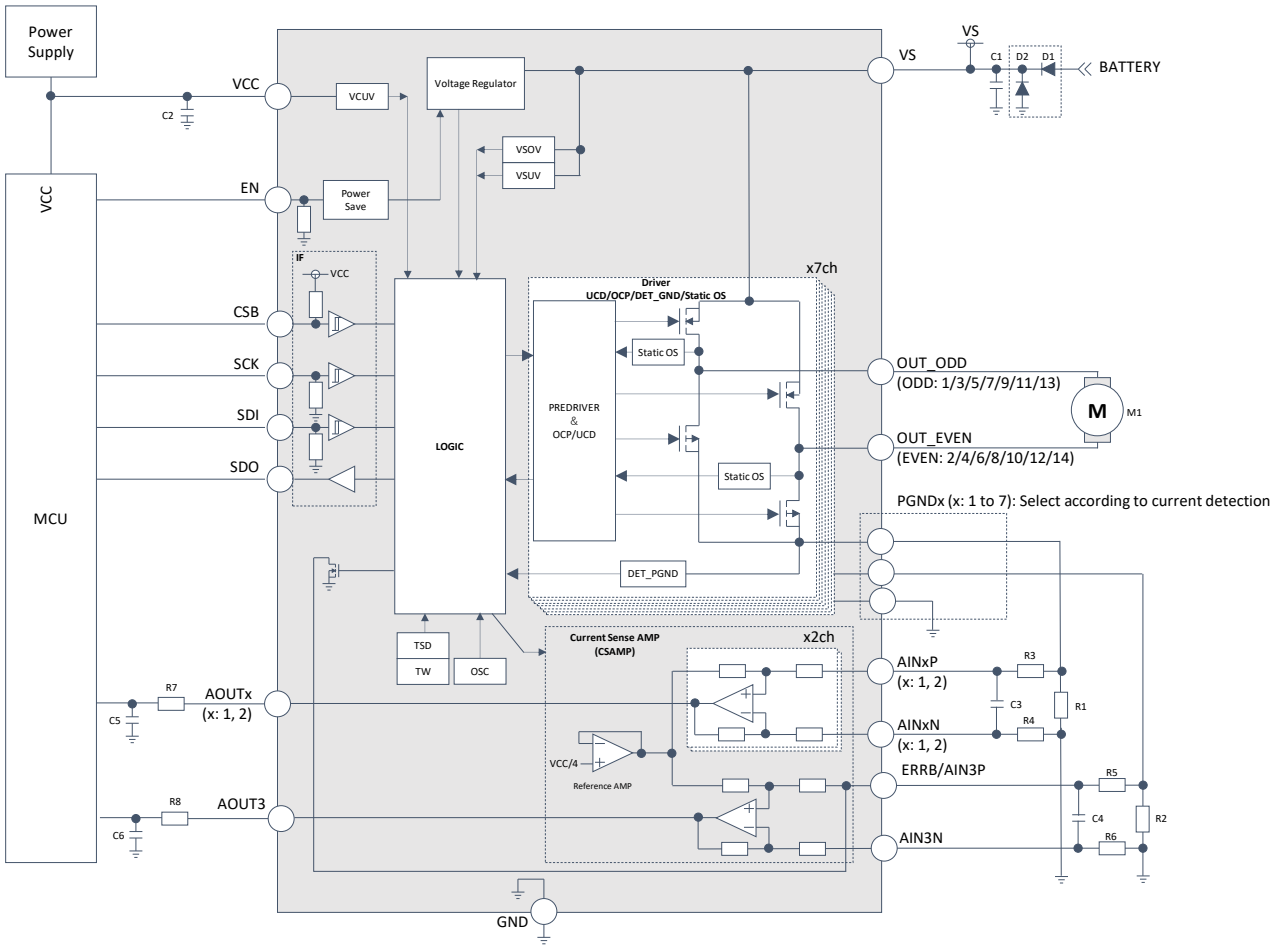


Figure 4. Application Circuit Example 1

Parts List

No.	Symbol	Function	Recommended Values	Unit	Class *(Note 1)*
1	C1	Decoupling Bypass Capacitors	10 or more	µF	A
2	C2	Decoupling Bypass Capacitors	0.1	µF	A
3	C3, C4	Input Voltage Smoothing Low-pass Filter	–	–	B
4	C5, C6	Output Voltage Smoothing Low-pass Filter	–	–	B
5	R1, R2	Shunt Resistors for Motor Drive Current Sensing	–	–	B
6	R3, R4, R5, R6	Input Voltage Smoothing Low-pass Filter	–	–	B
7	R7, R8	Output Voltage Smoothing Low-pass Filter	–	–	B
8	D1	Schottky Barrier Diode for Reverse-Battery Protection	–	–	B
9	D2	Zener Diode for Battery Voltage Clamp	–	–	B

(Note 1) Class A: Components required for the motor driver IC, Class B: Components that need to be considered for the application

Application Examples - Continued

Application Circuit (e.g., brushed DC motor drive, ERRB is used)

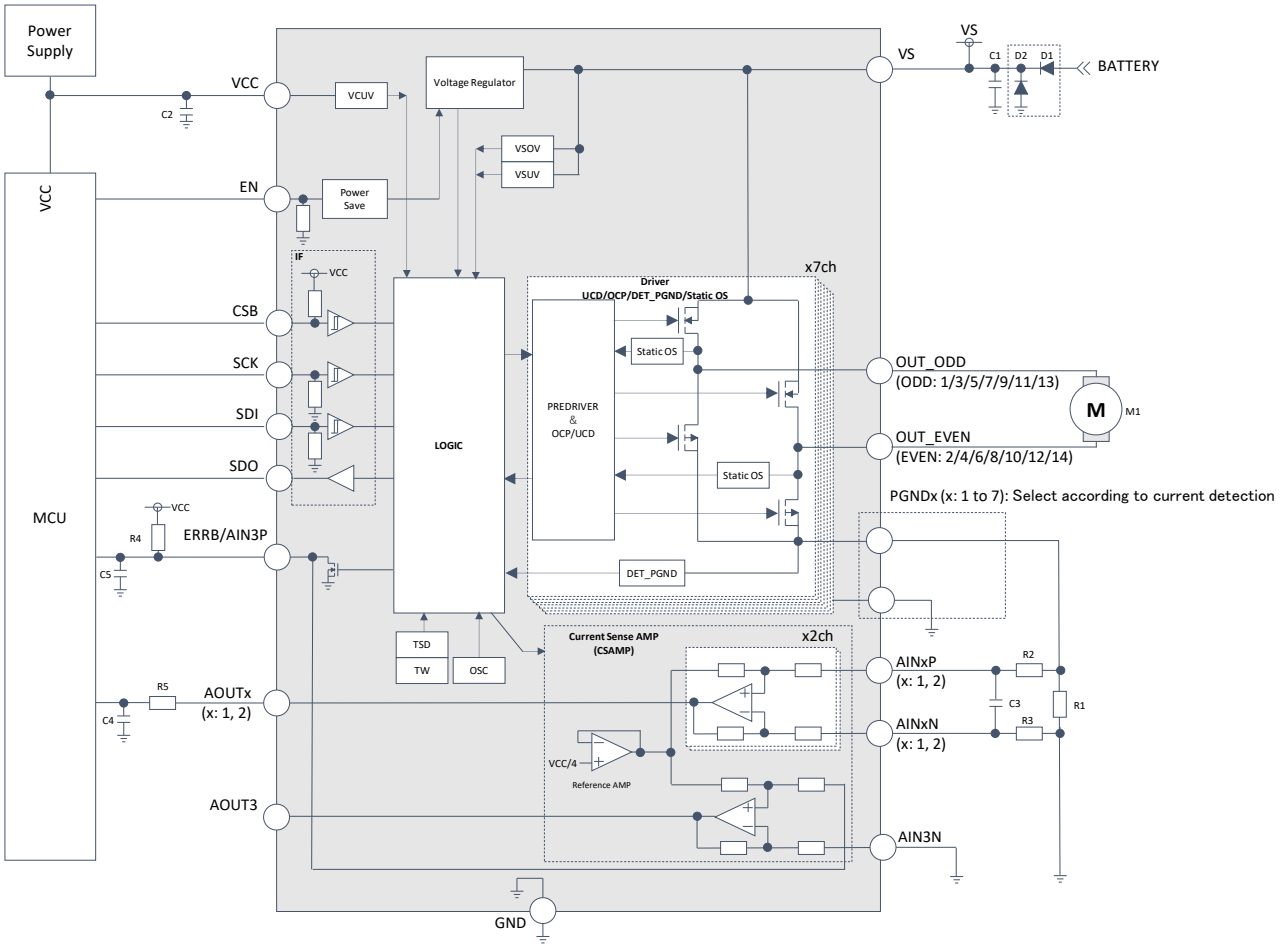


Figure 5. Application Circuit Example 2

Parts List

No.	Symbol	Function	Recommended Values	Unit	Class *(Note 1)*
1	C1	Decoupling Bypass Capacitors	10 or more	μF	A
2	C2	Decoupling Bypass Capacitors	0.1	μF	A
3	C3	Input Voltage Smoothing Low-pass Filter	–	–	B
4	C4	Output Voltage Smoothing Low-pass Filter	–	–	B
5	C5	Output Voltage Smoothing Low-pass Filter	–	–	B
6	R1	Shunt Resistor for Motor Drive Current Sensing	–	–	B
7	R2, R3	Input Voltage Smoothing Low-pass Filter	–	–	B
8	R4	Power Supply Pull-up Resistor	10	kΩ	A
9	R5	Output Voltage Smoothing Low-pass Filter	–	–	B
10	D1	Schottky Barrier Diode for Reverse-Battery Protection	–	–	B
11	D2	Zener Diode for Battery Voltage Clamp	–	–	B

(Note 1) Class A: Components required for the motor driver IC, Class B: Components that need to be considered for the application.

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power Supply Voltage	VS	V_S	-0.3 to +40	V
	VCC	V_{CC}	-0.3 to +7	V
Input Voltage	EN, CSB, SCK, SDI	V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}	-0.3 to +7 < VCC	V
	AIN1P, AIN1N, AIN2P, AIN2N, AIN3N	V_{AIN1P}, V_{AIN1N}, V_{AIN2P}, V_{AIN2N}, V_{AIN3N}	-0.3 to +7 < VCC	V
Test Input Voltage	TEST	V_{TEST}	-0.3 to +7	V
Output Voltage	OUT1 to OUT14	$V_{OUT1\ to\ 14}$	-0.3 to +40 < VS	V
	AOUT1, AOUT2, AOUT3	V_{AOUT1}, V_{AOUT2}, V_{AOUT3}	-0.3 to +7 < VCC	V
	SDO	V_{SDO}	-0.3 to +7 < VCC	V
Input/Output Voltage	ERRB/AIN3P	$V_{ERRB/AIN3P}$	-0.3 to +7 < VCC	V
PGND Voltage *(Note 2)*	PGND1, PGND2, PGND3, PGND4, PGND5, PGND6, PGND7	V_{PGND1}, V_{PGND2}, V_{PGND3}, V_{PGND4}, V_{PGND5}, V_{PGND6}, V_{PGND7}	-0.3 to +2.0	V
Output Current *(Note 1)*	OUTx (x: 1 to 14)	$I_{OUTx\ (x:\ 1\ to\ 14)}$	-1 to +1	A
	SDO	I_{SDO}	-1 to +1	mA
	ERRB/AIN3P *(Note 3)*	$I_{ERRB/AIN3P}$	0 to +1	mA
Storage Temperature Range		Tstg	-55 to +150	°C
Maximum Junction Temperature		Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) For the current item, the current inflow into the IC is positively notated, and the current outflow from the IC is negatively notated.
(Note 2) Connect the pin that does not use the current monitor AMP to PGND.
(Note 3) Current specification when using ERRB.

Recommended Operating Conditions

Parameter	Symbol	Standard Values			Unit
		Min	Typ	Max	
Operating Temperature	Topr	-40	+25	+125	°C
VS Supply Voltage *(Note 4)*	Vs	6.3	12	32	V
VCC Supply Voltage *(Note 4)*	V_{CC}	3.0	5.0	5.5	V
EN, CSB, SCK, SDI Input Voltage	V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}	0	-	VCC	V

(Note 4) It is recommended to turn on the VCC voltage after the VS voltage exceeds the minimum operating voltage range (6.3 V).
It is recommended that each logic input be applied after the VCC voltage exceeds the minimum operating voltage range (3 V).

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN48FBV070				
Junction to Ambient	θ_{JA}	72.6	30.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	12.0	12.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD16940MUF-C Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1, 2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS = 6.3 V to 32 V, VCC = 3.0 V to 5.5 V,
PGND1 = PGND2 = PGND3 = PGND4 = PGND5 = PGND6 = PGND7 = GND,
All VS pins are shorted. AIN1P = AIN2P = ERRB/AIN3P = AIN1N = AIN2N = AIN3N = GND

Parameter	Symbol	Standard Values			Unit	Conditions
		Minimum	Typical	Maximum		
Circuit Current						
VS Circuit Current 1 *(Note 1)*	I_{VS1}	-	0	5	µA	EN = 0 V, –40 °C ≤ Tj ≤ +105 °C
VS Circuit Current 2	I_{VS2}	-	-	17.5	µA	EN = 0 V, +105 °C < Tj ≤ +150 °C
VS Circuit Current 3 *(Note 2)*	I_{VS3}	-	8.7	15.6	mA	EN = 5 V, CSAMPx_EN (x: 1 to 3) = 1
VCC Circuit Current 1 *(Note 1)*	I_{VCC1}	-	0	10	µA	EN = 0 V, –40 °C ≤ Tj ≤ +105 °C
VCC Circuit Current 2	I_{VCC2}	-	-	100	µA	EN = 0 V, +105 °C < Tj ≤ +150 °C
VCC Circuit Current 3 *(Note 2)*	I_{VCC3}	-	3.4	6.8	mA	EN = 5 V, CSAMPx_EN (x: 1 to 3) = 0
VCC Circuit Current 4 *(Note 2)*	I_{VCC4}	-	4.2	8.4	mA	EN = 5 V, CSAMPx_EN (x: 1 to 3) = 1
Output Pins						
Output ON Resistance High Side 1	R_{ONH1}	-	0.85	1.70	Ω	I_{Load} = 0.1 A to 0.8 A, -40 °C ≤ Tj < +25 °C
Output ON Resistance High Side 2	R_{ONH2}	-	1.25	2.05	Ω	I_{Load} = 0.1 A to 0.8 A, +25 °C ≤ Tj ≤ +150 °C
Output ON Resistance Low Side 1	R_{ONL1}	-	0.55	1.10	Ω	I_{Load} = 0.1 A to 0.8 A, -40 °C ≤ Tj < +25 °C
Output ON Resistance Low Side 2	R_{ONL2}	-	0.90	1.45	Ω	I_{Load} = 0.1 A to 0.8 A, +25 °C ≤ Tj ≤ +150 °C
Output Leakage High Side	I_{LH}	-10	0	-	µA	EN = 0 V, OUTx (x: 1 to 14) = 0 V
Output Leakage Low Side	I_{LL}	-	0	10	µA	EN = 0 V, OUTx (x: 1 to 14) = V_S
Output Diode Voltage High Side	V_{FH}	0.2	0.8	1.4	V	I_{Load} = +0.6 A
Output Diode Voltage Low Side	V_{FL}	0.2	0.8	1.4	V	I_{Load} = -0.6 A
Enable Input (EN), SPI Input (CSB, SCK, SDI)						
Input High Voltage	V_{IH}	V_{CC} x 0.7	–	V_{CC}	V	
Input Low Voltage	V_{IL}	0	-	V_{CC} x 0.3	V	
Input High Current 1	I_{IH1}	25	50	100	µA	SDI, SCK, EN = VCC = 5 V
Input High Current 2	I_{IH2}	-	0	10	µA	CSB = VCC = 5 V
Input Low Current 1	I_{IL1}	-10	0	-	µA	SDI, SCK, EN = 0 V
Input Low Current 2	I_{IL2}	-25	–50	–100	µA	CSB = 0 V, VCC = 5 V
SPI Output (SDO), Error Output (ERRB/AIN3P)						
High Level Output Voltage (SDO)	V_{SDOH}	V_{CC} x 0.8	–	V_{CC}	V	SDO = High, I_{SDO} = -1 mA
Low Level Output Voltage (SDO)	V_{SDOL}	0	–	V_{CC} x 0.2	V	SDO = Low, I_{SDO} = +1 mA
Low Level Output Voltage (ERRB/AIN3P)	V_{ERRB}	0	-	0.4	V	CSAMP3_EN = 0, ERRB/AIN3P = Low, $I_{ERRB/AIN3P}$ = +1 mA
High Level Output Leakage Current (ERRB/AIN3P)	I_{ERRBH}	-	0	10	µA	CSAMP3_EN = 0
Low Level Output Leakage Current (SDO)	I_{SDOL}	-10	0	-	µA	
High Level Output Leakage Current (SDO)	I_{SDOH}	-	0	10	µA	

(Note 1) Design guaranteed. No shipping inspection.
(Note 2) Output is at Hi-Z setting
(Note 3) For currents, the current flow into IC is expressed as positive, and the current flow out of IC is expressed as negative.

Electrical Characteristics - Continued

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS = 6.3 V to 32 V, VCC = 3.0 V to 5.5 V,
PGND1 = PGND2 = PGND3 = PGND4 = PGND5 = PGND6 = PGND7 = GND,
All VS pins are shorted. AIN1P = AIN2P = ERRB/AIN3P = AIN1N = AIN2N = AIN3N = GND

Parameter	Symbol	Standard Values			Unit	Conditions
		Minimum	Typical	Maximum		
Internal Oscillator						
Oscillation Frequency	f_{OSC}	8	10	12	MHz	
PWM Drive						
Frequency Accuracy Error	A_{fPWM}	-20	-	+20	%	
Dead Time Delay Time	t_{ADead}	0.1	0.4	2.0	µs	PDEAD [1:0] = “0, 0”
Dead Time Accuracy (when registers are set)	A_{tDead}	-20	-	+20	%	PDEAD [1:0] = not “0, 0”
Driver Output Timing						
Propagation Delay Time	t_{propg}	-	-	3	µs	VS = 12 V, No Load PDEAD [1:0] = “0, 0”
OUT Rise Time	t_{LHR}	-	0.4	2.0	µs	VS = 12 V, No Load
OUT Fall Time	t_{HLF}	-	0.4	2.0	µs	VS = 12 V, No Load
PGNDx (x: 1 to 7) Sources Current	I_{PGNDx} (x: 1 to 7)	-200	-120	-40	µA	LSC-OUTy (y: 1 to 14) = 1 (only one channel)

(Note 1) Design guaranteed. No shipping inspection.
(Note 2) For currents, the current flow into IC is expressed as positive, and the current flow out of IC is expressed as negative.

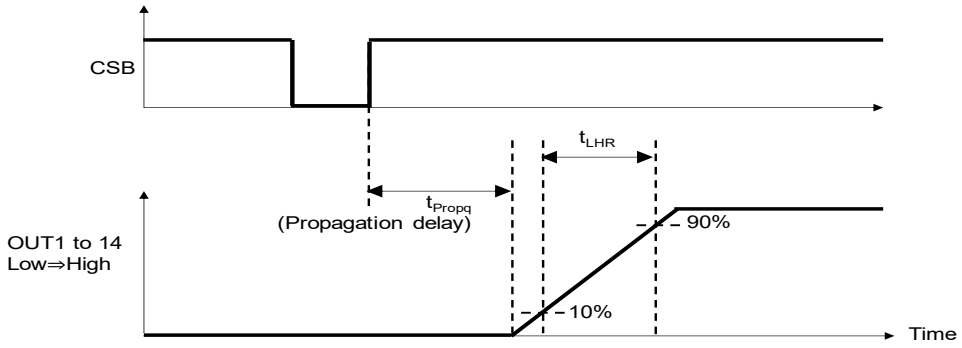


Figure 6. Driver Output Timing (Low to High)

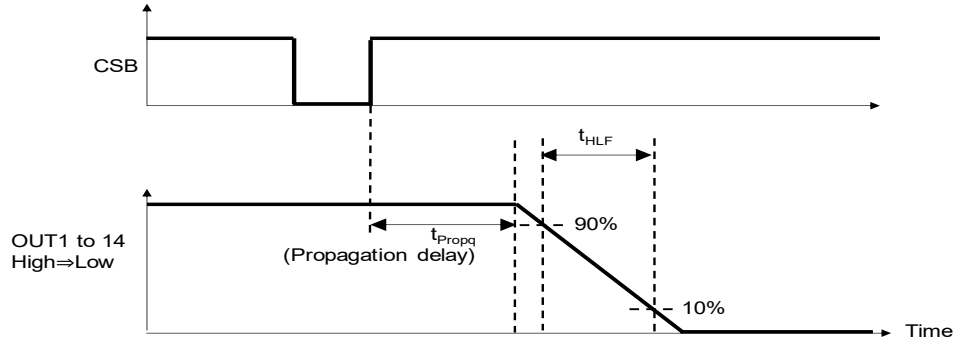


Figure 7. Driver Output Timing (High to Low)

Electrical Characteristics - Continued

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS = 6.3 V to 32 V, VCC = 3.0 V to 5.5 V,
PGND1 = PGND2 = PGND3 = PGND4 = PGND5 = PGND6 = PGND7 = GND,
All VS pins are shorted. AIN1P = AIN2P = ERRB/AIN3P = AIN1N = AIN2N = AIN3N = GND

Parameter	Symbol	Standard Values			Unit	Conditions
		Minimum	Typical	Maximum		
Current Sense Amplifiers (AIN1P, AIN1N, AIN2P, AIN2N, ERRB/AIN3P, AIN3N)						
Input Offset Voltage 1	$V_{AINOFS1}$	-15	0	+15	mV	Tj = 25 °C, AINxP in use *(Note 2)*, $V_{AINOFS} = (V_{AOx} – V_{CC}/4) / G_{AIOx}$ (x: 1 to 3)
Input Offset Voltage 2	$V_{AINOFS2}$	-20	0	+20	mV	Tj = 25 °C, PGND in use *(Note 3)*, $V_{AINOFS} = (V_{AOx} – V_{CC}/4) / G_{AIOx}$ (x: 1 to 3)
Input Offset Voltage Temperature Drift 1 *(Note 1)*	$V_{AINDRFT1}$	-20	0	+20	µV/°C	AINxP in use *(Note 2)*
Input Offset Voltage Temperature Drift 2 *(Note 1)*	$V_{AINDRFT2}$	-40	0	+40	µV/°C	PGND in use *(Note 3)*
Common-mode Input Voltage Range	V_{AINCMN}	-0.3	–	+1.0	V	
Output Voltage Range 1	V_{AO1}	0.3	–	4.4	V	VCC = 5 V
Output Voltage Range 2	V_{AO2}	0.3	–	2.7	V	VCC = 3.3 V
Input/Output Gain Accuracy 1	G_{AIO1}	-3	–	+3	%	AINxP in use *(Note 2)*
Input/Output Gain Accuracy 2	G_{AIO2}	-3	–	+3	%	PGND in use *(Note 3)*
Output Rise Time *(Note 1)*	t_{ARISE}	–	–	10	µs	AIN1P, AIN2P, ERRB/AIN3P = 0 V to +2 V/G_{AIO}, $C_{AOUTx\ (x:\ 1\ to\ 3)}$ = 25 pF load
Output Fall Time *(Note 1)*	t_{AFALL}	–	–	10	µs	AIN1P, AIN2P, ERRB/AIN3P = 2 V/G_{AIO} to 0 V $C_{AOUTx\ (x:\ 1\ to\ 3)}$ = 25 pF load
Reference Voltage Generation Amplifier Output Voltage *(Note 1)*	V_{REF}	$V_{CC}/4$ - 0.015	$V_{CC}/4$	$V_{CC}/4$ + 0.015	V	

(Note 1) Design guaranteed. No shipping inspection.
(Note 2) Characteristics when using current detection with AINxP input. VAINxP = VAINxN = GND (x: 1 to 3)
(Note 3) Characteristics when using current detection with PGND input. CSx_PGNDy_SEL = 1 (x: 1 to 3, y: 1 to 7)

Electrical Characteristics - Continued

Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS = 6.3 V to 32 V, VCC = 3.0 V to 5.5 V,
PGND1 = PGND2 = PGND3 = PGND4 = PGND5 = PGND6 = PGND7 = GND,
All VS pins are shorted. AIN1P = AIN2P = ERRB/AIN3P = AIN1N = AIN2N = AIN3N = GND

Parameter	Symbol	Standard Values			Unit	Conditions
		Minimum	Typical	Maximum		
Protections						
VS Under Voltage Detection (ON to OFF)	V_{UVDH}	5.3	5.8	6.3	V	
VS Under Voltage Detection (OFF to ON)	V_{UVDL}	5.0	5.5	6.0	V	
VS Over Voltage Detection 1 (OFF to ON)	V_{OVPH1}	32.5	36.0	39.5	V	OVPSEL = 0
VS Over Voltage Detection 1 (ON to OFF)	V_{OVPL1}	30.0	33.5	37.0	V	OVPSEL = 0
VS Over Voltage Detection 2 (OFF to ON)	V_{OVPH2}	18.0	20.0	22.0	V	OVPSEL = 1
VS Over Voltage Detection 2 (ON to OFF)	V_{OVPL2}	16.2	18.0	19.8	V	OVPSEL = 1
VCCUV Detection (ON to OFF)	V_{CCUVR}	2.55	2.75	2.95	V	
VCCUV Detection (OFF to ON)	V_{CCUVD}	2.50	2.70	2.90	V	
Over Current Detection	I_{OCP}	1.05	1.55	2.05	A	
Over Current Detection Delay Time	t_{DOC}	1.5	5.0	10.0	µs	
PGND Over Voltage Detection DET_PGNDx (x: 1 to 7)	V_{DETPG}	0.8	1.0	1.2	V	
PGND Over Voltage Detection Delay Time	t_{DETPG}	1.5	5.0	10.0	µs	
OPEN Detection (Note 1)	I_{UD}	2	11	25	mA	
OPEN Detection Delay Time	t_{DUD}	200	370	600	µs	
Thermal Warning Detection (Note 1)	T_{TW}	100	125	150	°C	
Thermal Warning Hysteresis (Note 1)	T_{TWHYS}	-	15	-	°C	
Thermal Shutdown Detection (Note 1)	T_{TSD}	155	180	205	°C	
Thermal Shutdown Hysteresis (Note 1)	T_{TSDHYS}	-	30	-	°C	
Static Open/Short Detection Comparator Judgment Voltage	V_{TH_SOS}	V_S x 0.4	V_S x 0.5	V_S x 0.6	V	
Static Open/Short Detection Pull-Up Resistor	R_{SOS}	2.5	5.0	10.0	kΩ	
Static Open/Short Detection Comparator Delay Time	t_{DSOS}	-	-	2.0	µs	

(Note 1) Design guaranteed. No shipping inspection.

Electrical Characteristics – Continued

Unless otherwise specified, –40 °C ≤ Tj ≤ +150 °C, VS = 6.3 V to 32 V, VCC = 3.0 V to 5.5 V,
PGND1 = PGND2 = PGND3 = PGND4 = PGND5 = PGND6 = PGND7 = GND,
All VS pins are shorted. AIN1P = AIN2P = ERRB/AIN3P = AIN1N = AIN2N = AIN3N = GND

Parameter	Symbol	Standard Values			Unit	Conditions
		Minimum	Typical	Maximum		
Serial interface						
SCK Frequency	f_{SCK}	-	-	4.1	MHz	
SCK Period	t_{SCK}	243	-	-	ns	
SCK High Time	t_{SCKH}	87.5	-	-	ns	
SCK Low Time	t_{SCKL}	87.5	-	-	ns	
SCK Setup Time	t_{SCKSET}	125	-	-	ns	
SCK Hold Time	t_{SCKHLD}	125			ns	
CSB Setup Time	t_{CSBSET}	125	-	-	ns	
CSB Hold Time	t_{CSBHLD}	125	-	-	ns	
CSB High Time	t_{CSBH}	2	-	-	µs	
SDI Setup Time	t_{SDISET}	50	-	-	ns	
SDI Hold Time	t_{SDIHLD}	50	-	-	ns	
SDO Valid Time	t_{SDOV}	-	-	100	ns	No Load
SDO Enable After CSB Falling Edge	t_{SDOEN}	-	-	125	ns	
SDO Disable After CSB Rising Edge	t_{SDODE}	-	-	500	ns	(Note 1)

(Note 1) Specified based on 0 % and 100 % of VCC.

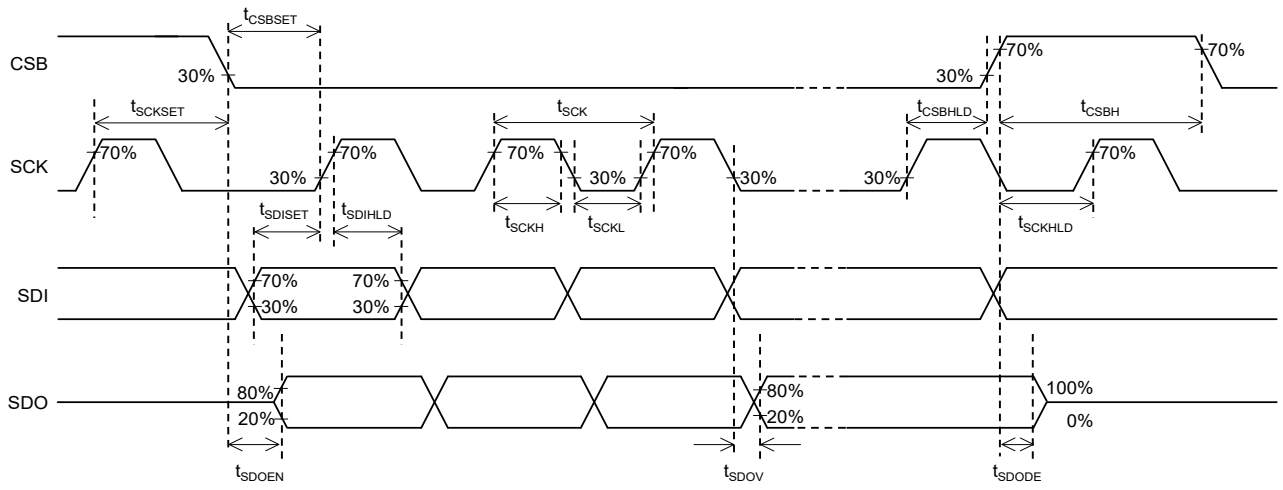


Figure 8. Serial Interface Timing

Power & Drive Sequence Timing Chart

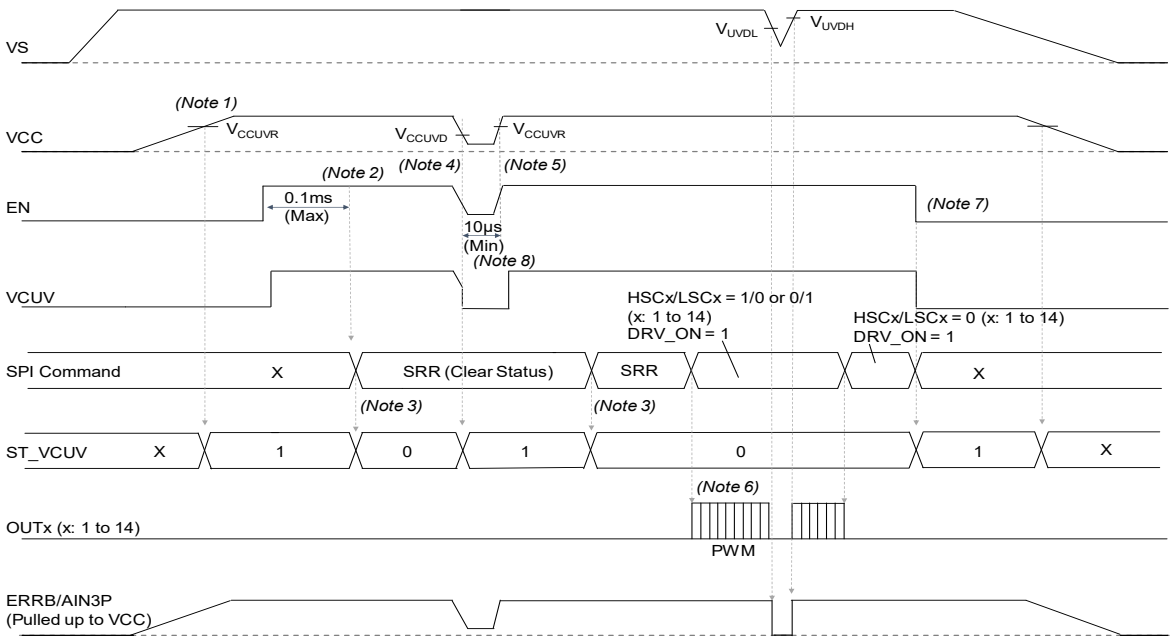


Figure 9. Power supply and drive sequence

(Note 1) The under voltage lock out function (VCCUV) monitors the VCC voltage. When the power is turned on, the ST_VCUV of the status register is set to '1' when VCC ≥ V_{CCUVR} is reached, and the value is held until it is set by SPI.

(Note 2) When EN is set to High, the circuit is activated. In addition, SPI is receivable after 0.1 ms (max).

(Note 3) If the SRR (Clear Status) register is set to '1' in the SPI, each status register is set to '0'.

(Note 4) When the VCC voltage falls below the V_{CCUVD}, the VCUV voltage goes low. At that time, the control circuit is reset, and the analog circuit turns off.

(Note 5) When the VCC voltage exceeds the V_{CCUVR}, the VCUV voltage goes high. Then, both the control circuit and the analog circuit become active.

(Note 6) After configuring Address 12h to 28h with SPI and activating DRV_ON, the OUTx outputs (x: 1 to 14) will update and start operating.

(Note 7) When EN is set to Low, the circuit turns off. SPI communication is not available.

(Note 8) If resetting by EN = Low, ensure the Low width is set to at least 10 µs.

Drive Mode

FULL ON/OFF Control

By setting OUTx_PWMSEL [2:0] = "0, 0, 0" (x: 1 to 14), ON/OFF of outputs can be controlled without using PWM output. ON/OFF control can be set for each channel using HSC-OUTx and LSC-OUTx (x: 1 to 14). And the setting is reflected in output by sending DRV_ON = '1'.

Table 1. OUTx (x: 1 to 14) configuration: Full ON/OFF control

OUTx_PWMSEL [2:0] (x: 1 to 14)	HSC-OUTx	LSC-OUTx	OUTx
“0, 0, 0”	0	0	Hi-Z
	0	1	LOW
	1	0	HIGH
	1	1	Hi-Z

PWM Control

When OUTx_PWMSEL [2:0] ≠ "0, 0, 0" (x: 1 to 14) is used, the outputs can be controlled by PWM output. It is equipped with the PWM Table Setting A to G for 7 channels, and it can set the frequency, duty, and deadtime individually. In addition, each OUT outputs PWM according to the PWM table settings selected in the OUTx_PWMSEL (x: 1 to 14). These PWM control settings are not reflected sequentially. When DRV_ON = '1' is sent, the settings are reflected all at once. However, there may be a deviation of one cycle of the PWM cycle (see Table 4. PWM Frequency Settings) until the setting is reflected.
The PWM control can be used in H-bridge, half-bridge, High Side SW, and LOW Side SW.
In addition, when PWM control is selected, synchronous control and asynchronous control can be selected (see Synchronous and Asynchronous Control).

Table 2. OUTx (x: 1 to 14) configuration: PWM control

OUTx_PWMSEL [2:0] (x: 1 to 14)	HSC-OUTx	LSC-OUTx	OUTx
Not “0, 0, 0”	0	0	Hi-Z
	0	1	PWM
	1	0	PWM
	1	1	Hi-Z

PWM Table: OUTx_PWMSEL [2:0] (x: 1 to 14)
Select the PWM table setting for each OUT output.

Table 3. PWM Table Settings

OUTx_PWMSEL [2:0] (x: 1 to 14)			PWM Table Setting
0	0	0	PWM MODE OFF
0	0	1	PWM_TABLE_A
0	1	0	PWM_TABLE_B
0	1	1	PWM_TABLE_C
1	0	0	PWM_TABLE_D
1	0	1	PWM_TABLE_E
1	1	0	PWM_TABLE_F
1	1	1	PWM_TABLE_G

PWM Frequency: PWM_FREQ_y [1:0] (y: A to G)
Configure the frequency settings for each table.

Table 4. PWM Frequency Settings

PWM_FREQ_y [1:0] (y: A to G)		frequency	unit	cycle	unit
0	0	0.1	kHz	10000	µs
0	1	0.2		5000	
1	0	2.0		500	
1	1	22.5		44.4	

PWM Control - Continued

PWM Duty: PWM_DUTY_y [5:0] (y: A to G)
Configure the Duty settings for each table.

$$PWM\_DUTY\_y\ [5:0]/63 \times 100\ [\%], (y: A\ to\ G)$$

Table 5. PWM Duty Settings

PWM_DUTY_y [5:0] (y: A to G)						Duty	unit
0	0	0	0	0	0	0.00	%
0	0	0	0	0	1	1.59	
0	0	0	0	1	0	3.17	
0	0	0	0	1	1	4.76	
:	:	:	:	:	:	:	
1	0	0	0	0	0	50.79	
1	0	0	0	0	1	52.38	
:	:	:	:	:	:	:	
1	1	1	1	1	0	98.41	
1	1	1	1	1	1	100.00	

Synchronous and Asynchronous Control

Asynchronous control or synchronous control can be selected by SYNC_EN-OUTx (x: 1 to 14).

'0': asynchronous mode

'1': synchronous mode

During asynchronous control, either GxH or GxL of the half-bridge is PWM driven. (Refer to Table 6. PWM Asynchronous Control/Synchronous control) When OUT is set to Hi-Z setting during driving, current regeneration is performed using Body Diode.

During synchronous control, both GxH and GxL of the half-bridge are synchronized and PWM driven. (Refer to Table 6. PWM Asynchronous Control/Synchronous control)

The Duty setting is applied based on the side set to '1' in HSC-OUTx and LSC-OUTx (x: 1 to 14). In addition, it is enabled only when setting OUTx_PWMSEL ≠ "0, 0, 0" (x: 1 to 14).

Table 6. PWM Asynchronous Control/Synchronous control

SYNC_EN-OUTx	HSC-OUTx	LSC-OUTx	GxH *(Note 3)*	GxL *(Note 3)*	OUTx
0	0	0	OFF	OFF	Hi-Z
0	0	1	OFF	PWM	PWM *(Note 1)* (LOW⇔Hi-Z)
0	1	0	PWM	OFF	PWM *(Note 2)* (HIGH⇔Hi-Z)
0	1	1	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	Hi-Z
1	0	1	PWMB *(Note 4)*	PWM	PWM *(Note 1)* (LOW⇔HIGH)
1	1	0	PWM	PWMB *(Note 4)*	PWM *(Note 2)* (HIGH⇔LOW)
1	1	1	OFF	OFF	Hi-Z

(Note 1) The Duty is applied based on the Low side (GxL).

(Note 2) The Duty is applied based on the High side (GxH).

(*Note 3*) It is an internal node of the IC. Refer to the Figure 10 below.

(*Note 4*) It is an inverting signal synchronized to the internal PWM signal.

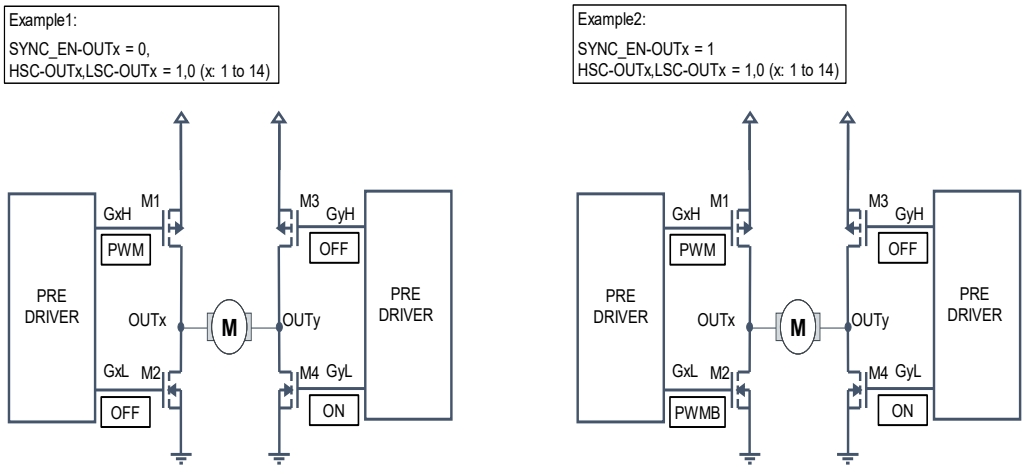


Figure 10. Examples of Synchronous and Asynchronous Control Modes

Shoot-through Current Prevention

The circuit is configured to prevent shoot-through current by monitoring the gate voltage in half-bridge units.

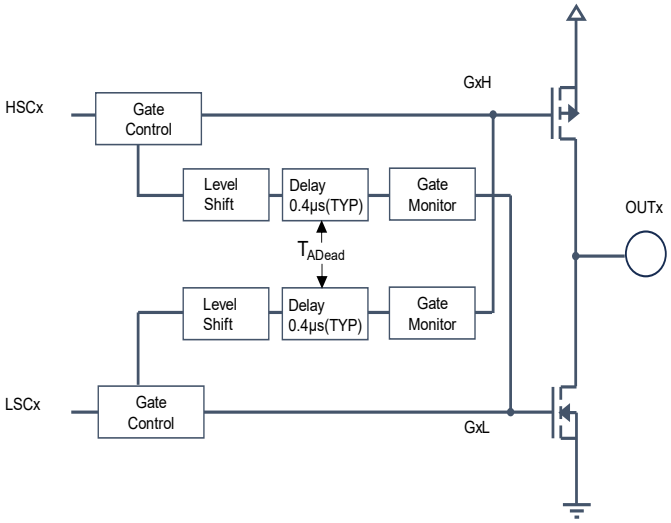


Figure 11. Shoot-through Prevention Block Configuration Diagram

In addition to the above analog circuit configuration, the Logic block can also insert a dead time for Shoot-through Current Prevention.

Shoot-through Prevention Dead Time: PDEADy [1:0] (y: A to G)
Configure the Deadtime settings for each table.

Table 7. PWM Dead Time Settings

PDEADy [1:0] (y: A to G)		SOS_EN	Deadtime	unit
0	0	0	0.4	µs
0	1	0	5	
1	0	0	10	
1	1	0	20	
*	*	1	20	

(Note) When SOS_EN = 1, Deadtime is automatically set to 20 µs.

When OUT is used in combined multiple output mode, please select dead time setting value of 5 µs (Typ) or more.

Dead Time in Combined Multiple Output Mode and Synchronous Mode

When using OUT in combined multiple output mode, it is necessary to add a dead time to prevent shoot-through current by taking into account the variation between the half-bridge outputs. For this case, set the setting time of PDEAD [1:0] to 5 µs (Typ) or more. The dead time set in the PDEAD register is inserted into OUT output when the OUT is switched. Note that the High/Low output time of the OUT is shortened by the dead time insertion.

Example: When PWM Frequency, Duty, and Dead time are set as follows,

- PWM Frequency = 22.5 kHz (period: approx. 44.4 µs)
- PWM Duty = 31.75 %
- Dead Time = 5 µs

the High output time of the OUT = 44.4 µs x 31.75 % - 5 µs = 14.1 µs - 5 µs = 9.1 µs.

Also, if the High/Low time of the OUT output is shorter than the Dead Time setting value, the High/Low of the OUT will be masked by Dead Time and cannot be output.

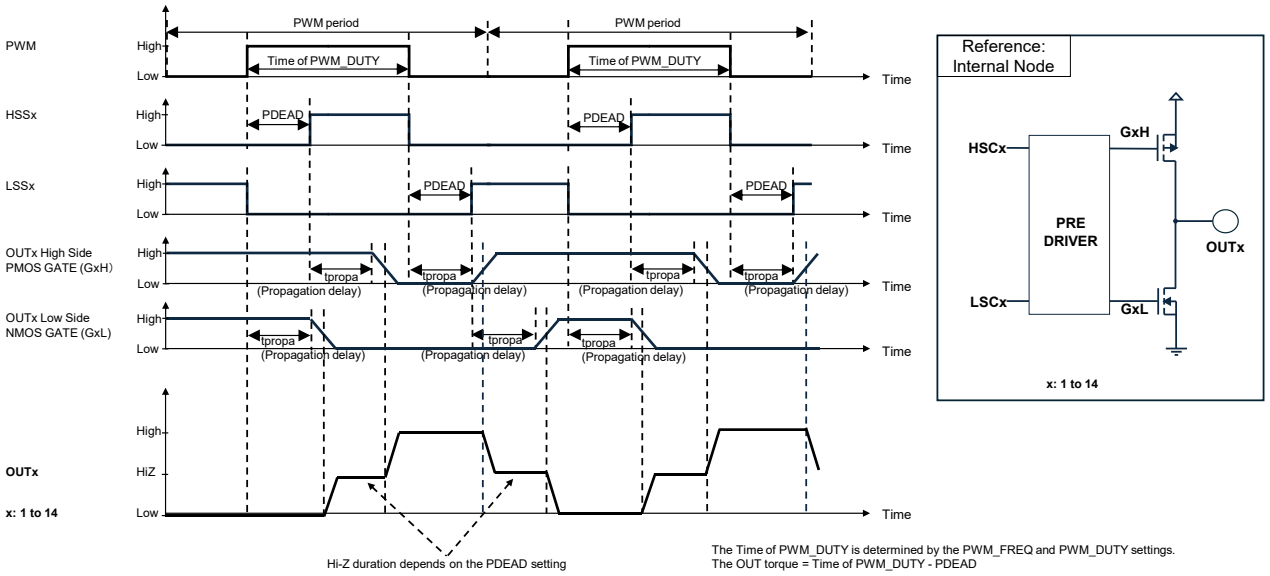


Figure 12. OUT output timing chart (H-bridge control MODE)

Protection Function

Table 8. Protection Function Table

Protection	Detect Conditions (Typ)		Protect Operation (Latch/Recovery)	Status Register	Latch setting Register
	Detect	Release			
VCCUV *(Note 1)*	V_{CC} < 2.70 V	V_{CC} > 2.75 V	-	ST_VCUV	-
TW	Tj > 125 °C	Tj < 115 °C	No effect	ST_TW	LAT_TW
UCD	OUT current ≤ 11 mA			ST_UCDHx ST_UCDLx (x: 1 to 14)	-
VSUV	V_S < 5.5 V	V_S > 5.8 V	Hi-Z (Auto recovery)	ST_VSUV	LAT_UV
VSOV	V_S > 20 V (OVPSEL = ‘1’) or V_S > 36 V (OVPSEL = ‘0’)	V_S < 18 V (OVPSEL = ‘1’) or V_S < 33.5 V (OVPSEL = ‘0’)		ST_VSOV	LAT_OV
TSD	Tj > 175 °C	Tj < 150 °C		ST_TSD	LAT_TSD
SPI_FAIL	SCK Clock Pulse ≠ 16			ST_SPI	-
OCP (High Side)	OUT output current ≥ 1.55 A		only detected OUT will Hi-Z (Latch) *(Note 2)*	ST_OCPHx (x: 1 to 14)	-
OCP (Low Side)	OUT output current ≥ 1.55 A or PGNDx > 1 V (Typ)			ST_OCPLx (x: 1 to 14)	-

(Note 1) VCCUV: VCC under voltage lock out, LOGIC RESET signal.
(Note 2) For PGND detection, it protects the OUTs corresponding to each PGND. Refer to Figure 16 for the mapping table.

Protection Function - Continued

VCC Under Voltage Protection (VCCUV)

This function is under voltage detection (VCCUV) of the VCC voltage. When VCCUV is detected, the control circuit is reset. Therefore, the IC does not operate under the low VCC voltage conditions. When the voltage is restored, the reset state is released and the IC returns to the operational state. However, since the control circuit is reset, each register is returned to its initial value.

This VCCUV detection function can detect abnormalities in VCC under voltage levels.

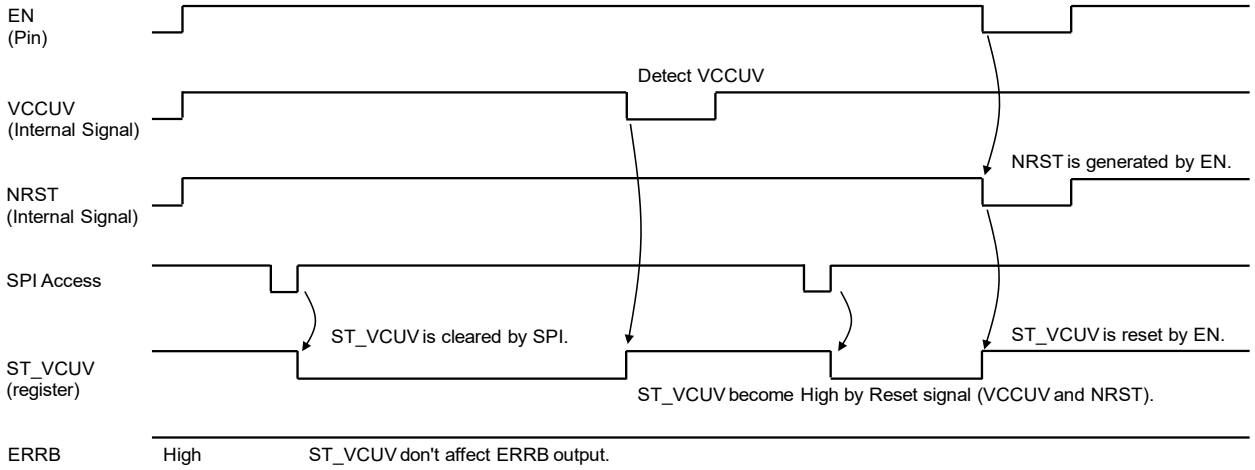


Figure 13. VCC Under Voltage Protection Timing Chart

Protection Function - Continued

VS Over Voltage Protection (VSOV)

If the voltage of VS pin equals or exceeds one of the following thresholds, VSOV condition sets all OUT outputs to Hi-Z.

- When OVPSEL = '0', the threshold is V_{OVPH1} = 36 V (Typ).
- When OVPSEL = '1', the threshold is V_{OVPH2} = 20 V (Typ).

During this condition, “ST_VSOV” register is automatically set to '1'.

If the voltage of VS pin equals or falls below one of the following thresholds, IC returns to normal operation by restoring OUT.

- When OVPSEL = '0', the threshold is V_{OVPL1} = 33.5 V (Typ).
- When OVPSEL = '1', the threshold is V_{OVPL2} = 18 V (Typ).

The behavior of ST_VSOV can be selected as either latch or auto-returning mode by setting the "LAT_OV" register.

- When LAT_OV = '1', the ST_VSOV continues to latch '1' even if VSOV condition is released. To clear the ST_VSOV, please write '1' to SRR or ST_VSOV register.
- When LAT_OV = '0', the ST_VSOV automatically cleared to '0' when VSOV condition is released.

Note that overvoltage protection does not operate when the EN pin is at the Low level. Please do not exceed the absolute maximum rating of the power supply voltage since there is a possibility of destruction of the IC.

Global Status: OVP
Status Register: ST_VSOV

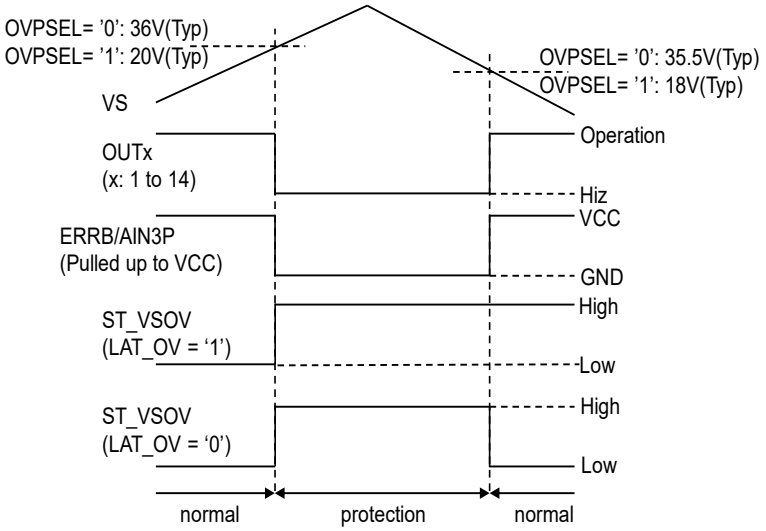


Figure 14. Over Voltage Protection Timing Chart

Protection Function - Continued

VS Under Voltage Lock Out (VSUV)

When the voltage applied to the VS pin is 5.5 V (Typ) or less, all OUT outputs are set to Hi-Z. During this condition, "ST_VSUV" register is automatically set to '1'.
When the voltage applied to the VS pin is 5.8 V (Typ) or more, IC returns to normal operation by restoring OUT.
The behavior of ST_VSUV can be selected as either latch or auto-returning mode by setting the "LAT_UV" register.

- When LAT_UV = '1', the ST_VSUV continues to latch '1' even if VSUV condition is released. To clear the ST_VSUV, please write '1' to SRR or ST_VSUV register.
- When LAT_UV = '0', the ST_VSUV automatically cleared to '0' when VSUV condition is released.

Global Status: UVP
Status Register: ST_VSUV

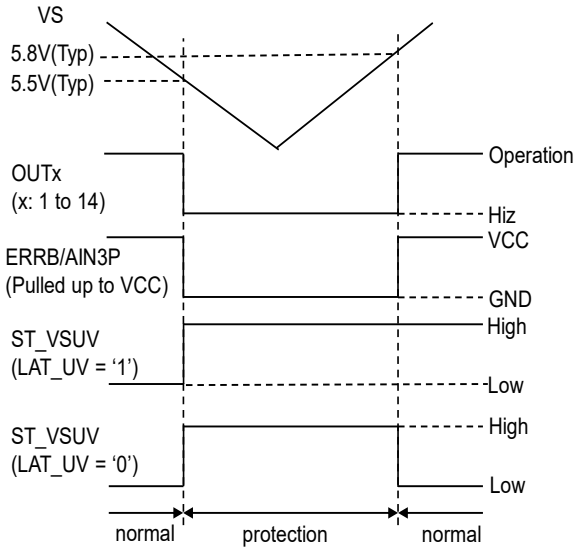


Figure 15. Under Voltage Lock Out Timing Chart

Protection Function - Continued

Over Current Protection (OCP)

Overcurrent protection performs independent fault detection and protection operation on each OUT output. In addition, to prevent noise malfunctions, the 5 µs (Typ) filter circuit is equipped.

The OCP on the High side detects overcurrent and sets the ST_OCPHx to '1' when the following two conditions are met:

- When the High side MOS of OUT is driven (HSC-OUTx (x: 1 to 14) = '1' setting or synchronization control setting)
- When the OUT current is 1.55 A (Typ) or more and it continues for 5 µs (Typ)

At this time, only the detected OUT is latched with Hi-Z.

The OCP on the LOW side detects overcurrent and sets the ST_OCPLx to '1' when the following two conditions are met:

- When the Low side MOS of OUT is driven (LSC-OUTx (x: 1 to 14) = '1' setting or synchronization control setting)
- When the OUT current is 1.55 A (Typ) or more and this condition continues for 5 µs (Typ)

Similarly, the PGND overvoltage detection sets the ST_OCPLx to '1', when the following two conditions are satisfied:

- When the low side output stage is driven (LSC-OUTx (x: 1 to 14) = '1' setting or synchronization control setting)
- When the PGND voltage is 1 V (Typ) or more and this condition continues for 5 µs (Typ)

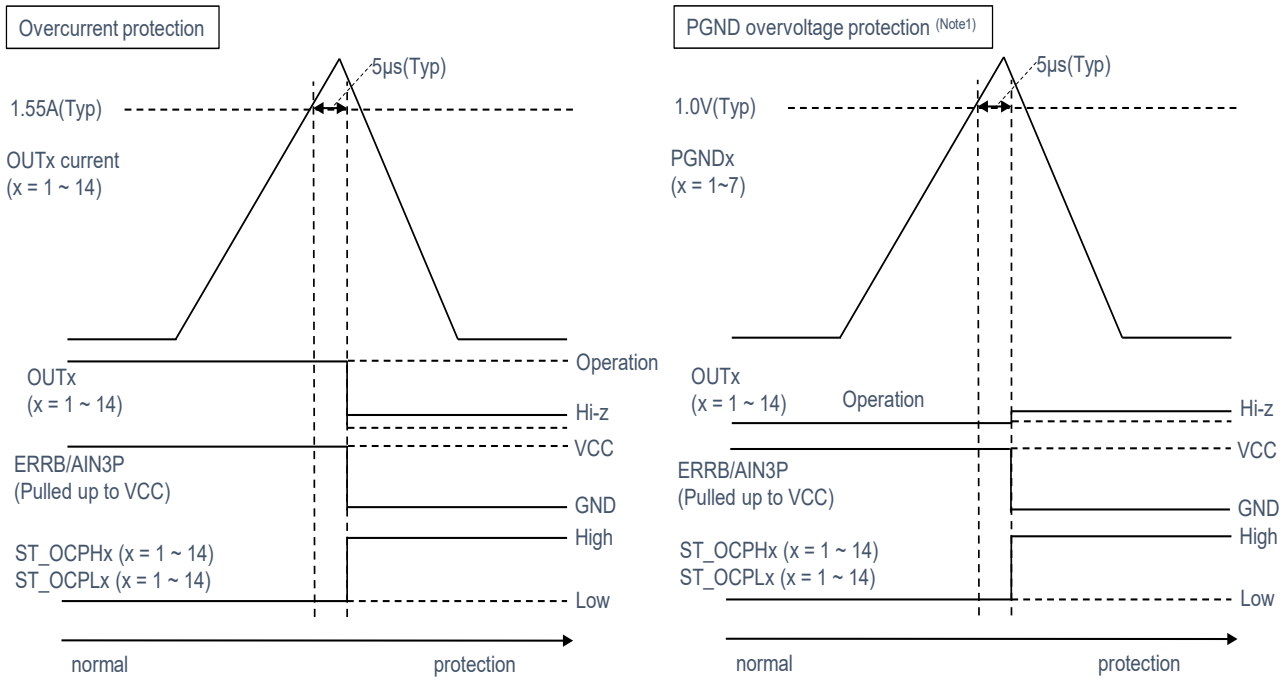
Note that only the OUT with overcurrent protection or PGND overvoltage detection is latched with Hi-Z.

To clear the status register (ST_OCPHx, ST_OCPLx), please write '1' to SRR register or to the status register.

Overcurrent protection is a function that prevents the destruction of the IC due to output short circuits, etc., but if the overcurrent condition continues, the IC may generate heat or deterioration. If the overcurrent condition continues to flow, take measures such as turning the IC into standby in the application.

Global Status: OCP
Status Register: ST_OCPHx, ST_OCPLx (x: 1 to 14)

During synchronous control, the MOS on both High and Low sides are driven, so the protection is performed in the half-bridge unit when OCP is detected. The protection operation is to turn off the MOS on both sides and to latch OUT to Hi-Z.



(Note1) PGND – OUT Pin Mapping Table

Detected PGND Over Voltage pin	PGND1	PGND2	PGND3	PGND4	PGND5	PGND6	PGND7
Hi-Z latch OUT pins	OUT1 OUT2	OUT3 OUT4	OUT5 OUT6	OUT7 OUT8	OUT9 OUT10	OUT11 OUT12	OUT13 OUT14

Figure 16. Over Current Protection/PGND Over Voltage Detection Timing Chart

Protection Function - Continued

Thermal Shutdown (TSD)/Thermal Warning (TW)

Thermal shutdown sets all OUT outputs to Hi-Z when the junction temperature rises above 175 °C (Typ). During this condition, ST_TSD register is automatically set to '1'. When the temperature drops below 150 °C (Typ), the OUTs are restored. In addition, the behavior of ST_TSD can be selected as either latch or auto-returning mode by setting the " LAT_TSD" register.

- When LAT_TSD = '1', the ST_TSD continues to latch '1' even if TSD condition is released. To clear the ST_TSD, please write '1' to SRR or ST_TSD register.
- When LAT_TSD = '0', the ST_TSD automatically cleared to '0' when TSD condition is released.

Global Status: OT
Status Register: ST_TSD

Thermal warning is set to '1' in the status register when the junction temperature rises to 125 °C (Typ) or more. Note that even if thermal warning is detected, OUT outputs do not turn off. In addition, the behavior of status register can be selected as either latch or auto-returning mode by setting the " LAT_TW" register.

- When LAT_TW = '1', the ST_TW continues to latch '1' even if TW condition is released. To clear the ST_TW, please write '1' to SRR or ST_TW register.
- When LAT_TW = '0', the ST_TW automatically cleared to '0' when TW condition is released (i.e., when the junction temperature falls below 115 °C (Typ)).

Global Status: OT
Status Register: ST_TW

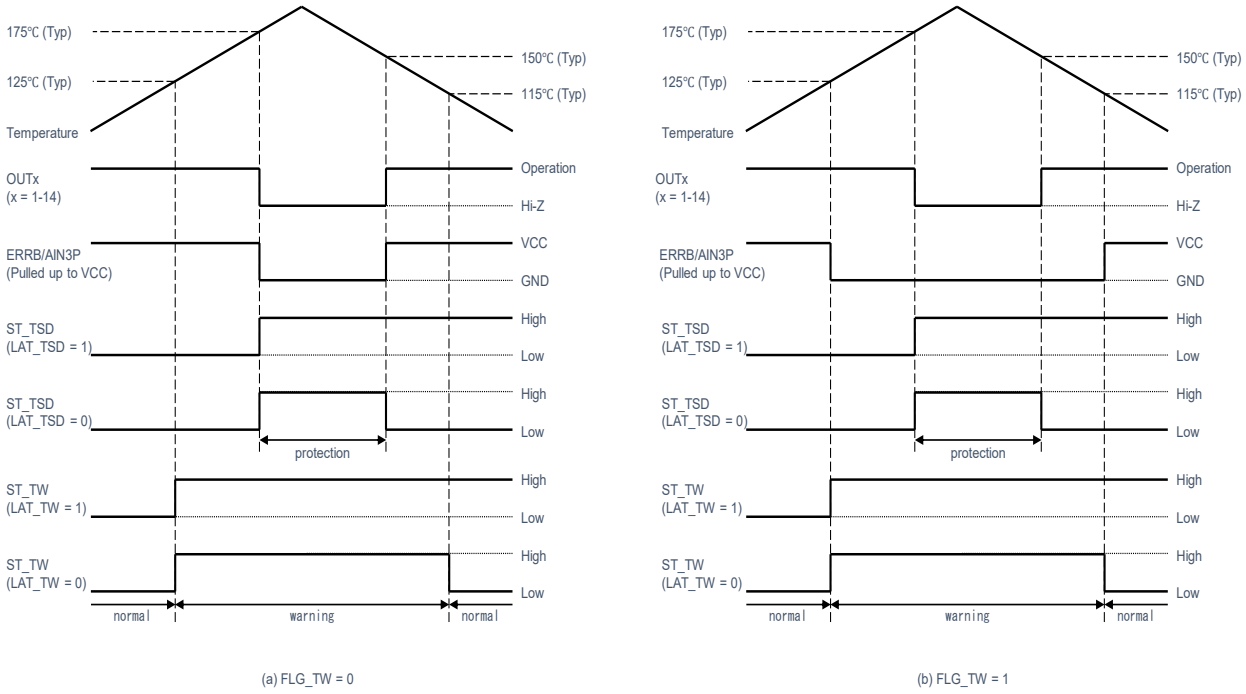


Figure 17. Thermal Shutdown and Thermal Warning Timing Chart

Protection Function - Continued

Under Current Detection (UCD)

Under current detection performs independent fault detection and protection operation on each OUT output. In addition, to prevent noise malfunctions, the 370 µs (Typ) filter circuit is equipped.

When the output pin current is 11 mA (Typ) or less and 370 µs (Typ) has elapsed, OPEN condition is detected. During this condition, the status register (ST_UCDHx / ST_UCDLx) are automatically set to '1'. Note that the OUT outputs do not turn off even if OPEN condition is detected.
To clear the status register, please write '1' to the SRR register or to the status register.
In synchronous mode, UCD sets the status register on the side that is set to '1' in HSC-OUTx or LSC-OUTx.

Global Status: UCD
Status Register: ST_UCDHx, ST_UCDLx (x: 1 to 14)

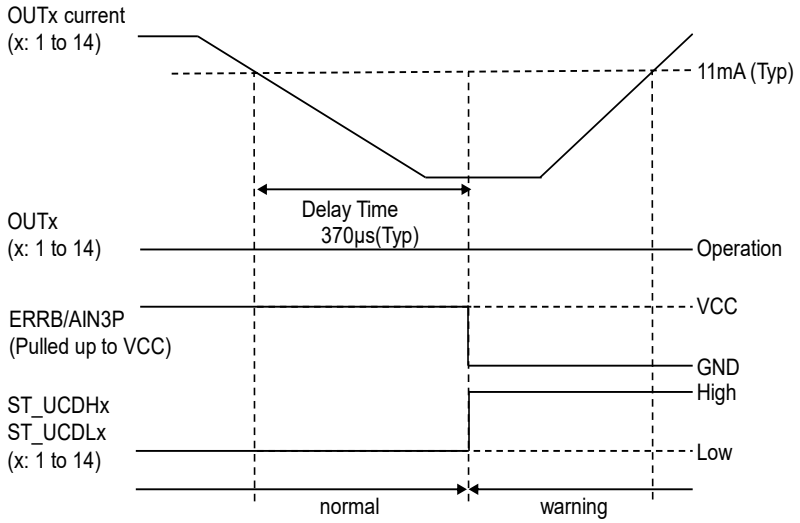


Figure 18. OPEN Detection Timing Chart 1

(Precautions for use)
When using a load that exceeds the detection time of 600 µs (Max), as shown in the figure below, please set the MASK_UCD register to 1. After the output current is stabilized, set the MASK_UCD register to '0' (ON).
For OPEN detection, make a judgment when the OUT output is fixed at High or Low.
When using PWM drive or short brake, set the MASK_UCD register to 1.

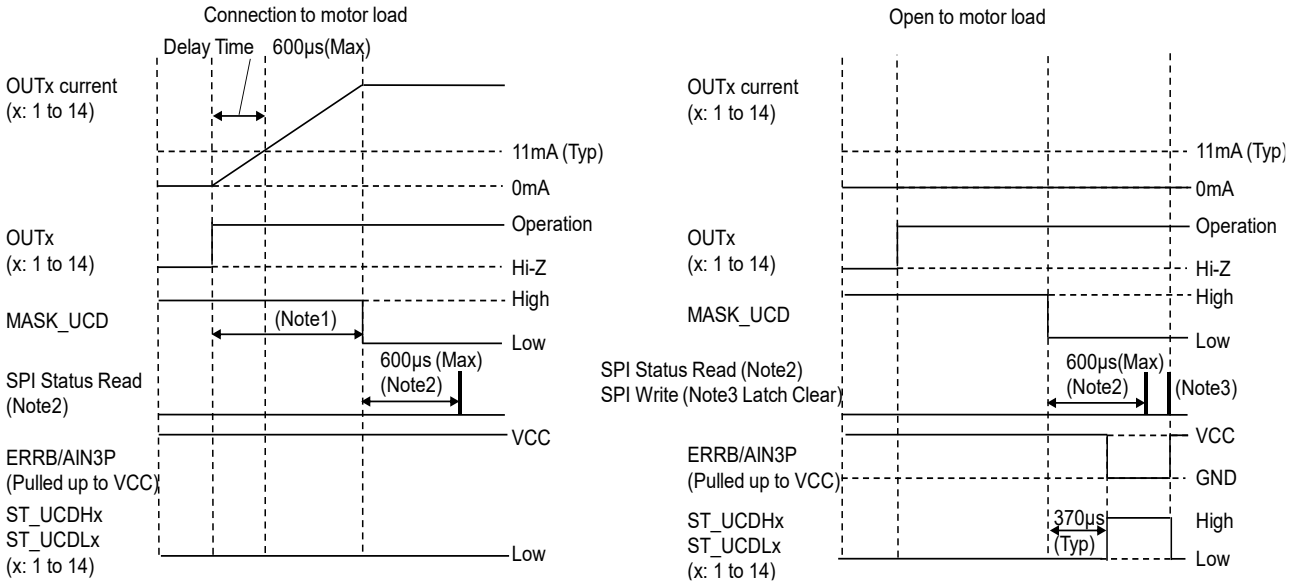


Figure 19. OPEN Detection Timing Chart 2

(Note 1) Please determine according to the response load.
(Note 2) The OPEN detection time must be at least 600 µs. Please use it with an interval of 600 µs or more.
(Note 3) When the latch is released, the counting of OPEN detection timer resumes.

Protection Function - Continued

Static Open/Short Detection (SOS)

The static open/short detection function can identify open/short states of the output MOS and the motor's open state, without needing to pass a large current before driving the motor. It is equipped with the following circuit functions:

- Switch for checking open/short: SET_SOSx (x: 1 to 14)
- Comparator for judgement the high or low of the OUTx voltage: COMPx (x: 1 to 14)
- Register to store the COMPx result: CHK_SOSx (x: 1 to 14)

Since half-bridge or H-bridge configurations can be freely combined, it is not equipped with a judgement function for open/short abnormalities. By implementing a function on the MCU side that uses open/short checking switches and performs judgment based on the comparator output result register, it is possible to check open/short condition. Make sure to implement the judgment function on the MCU side, according to each configuration.
(Refer to the following examples of H Bridge connection)

Note: The start timing of static open/short detection is determined by the charge/discharge time constant, which changes depending on the motor load. Check the response speed of the OUT output before setting the start timing of open/short detection. In addition, when static open/short detection is used, Dead Time is automatically set to 20 µs.

Static Open/Short Detection - Continued

Reference: Example of using H Bridge (OUT1, OUT2)

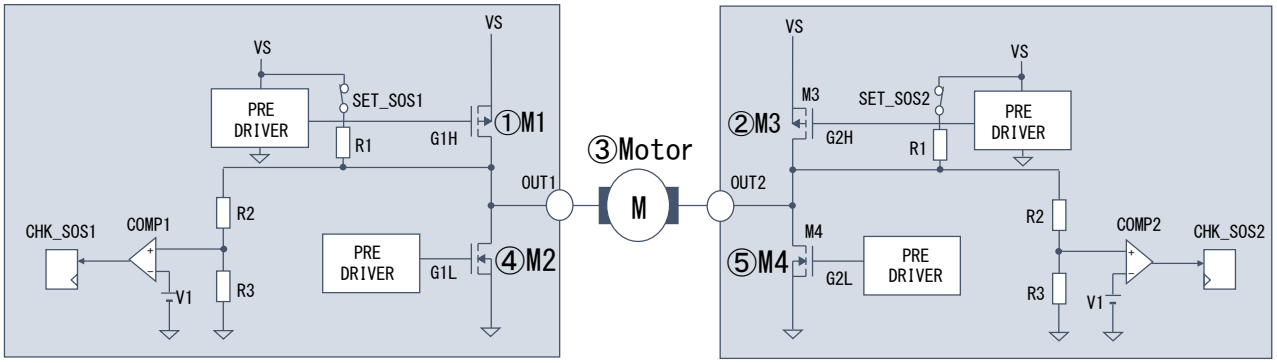


Figure 20. Open/Short Detection Block Diagram

Table 9. (Reference Example) When Using H Bridge (OUT1, OUT2) Open/Short Detection Judgment Table

	BD16940MUF-C Function								Example : H-bridge Judgement Method										
	Setting						CHK_SOS(Note 1)		Open					Short					Status
Sequence	SET_SOS1	SET_SOS2	G1H	G1L	G2H	G2L	1	2	①	②	③	④	⑤	①	②	③	④	⑤	
1	OFF	OFF	OFF	OFF	OFF	OFF	L	L											Normal
							H	H						○	○				① or ② FET Short
							Other												Illegal(Fail) (Note 2)
2	**ON**	OFF	OFF	OFF	OFF	OFF	H	H											Normal
							L	L									○	○	④ or ⑤ FET Short
							H	L			○								③ Open
							Other												Illegal(Fail) (Note 2)
3	OFF	**ON**	OFF	OFF	OFF	OFF	H	H											Normal
							L	L									○	○	④ or ⑤ FET Short
							L	H			○								③ Open
							Other												Illegal(Fail) (Note 2)
4	OFF	OFF	**ON**	OFF	OFF	OFF	H	H											Normal
							L	L	○										① Open
							Other												Illegal(Fail) (Note 2)
5	**ON**	OFF	OFF	**ON**	OFF	OFF	L	L											Normal
							H	H				○							④ Open
							Other												Illegal(Fail) (Note 2)
6	OFF	OFF	OFF	OFF	**ON**	OFF	H	H											Normal
							L	L		○									② Open
							Other												Illegal(Fail) (Note 2)
7	OFF	**ON**	OFF	OFF	OFF	**ON**	L	L											Normal
							H	H					○						⑤ Open
							Other												Illegal(Fail) (Note 2)

(Note 1) Please refer to the registers of static open/short check
(Note 2) If you check in the order of sequence 1 to 7, Illegal Fail will be an abnormal condition other than an open/short failure.

The SET_SOSx (x: 1 to 14) register can be activated only when the SOS_EN register is enabled. Please refer to the following sequence.

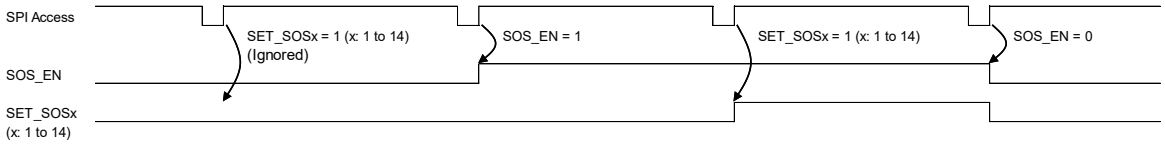


Figure 21. SOS_EN / SET_SOS Timing Chart

Protection Function - Continued

Erroneous SPI Transmission (Transmission Error: SPI_FAIL)

When CSB signal becomes Low to High it will be assumed that SPI has completed the transfer, and the internal registers will be updated. (For details on the transfer protocol, please refer to SPI Protocol.)
When SCK inputs a high pulse other than 16 while CSB is low, erroneous SPI transmission is detected. If the error is detected, ST_SPI is set to 1 and the OUT1 to OUT14 switch to high-impedance mode. The transmission error status is refreshed every time CSB rises.

Global Status: SPI_FL
Status Register: ST_SPI

Current Sense Amplifier

A current sense amplifier is included to sense the current flowing through the shunt resistor. The gain can be set by register. The current sense amplifier output voltage is given by:

$$AOUTx = (AINxP - AINxN) \times (Gain\ Setting) + \frac{1}{4} \times VCC\ [V]\ (x: 1, 2, 3)$$

Current Sense Amplifier Settings
To use current sense amplifier 1, set CSAMP1_EN = '1'.
To use current sense amplifier 2, set CSAMP2_EN = '1'.
When not used, power consumption can be reduced by setting registers CSAMP1_EN = '0' and CSAMP2_EN = '0'.

CSAMP1_EN CSAMP2_EN	Current Sense Amplifier
0	Disabled
1	Enabled

To use current sense amplifier 3, set CSAMP3_EN = '1'.
When not used, power consumption can be reduced by setting register CSAMP3_EN = '0'.
The input pin of current sense amplifier 3 is shared with the ERRB error output pin, so only one of these functions can be used at a time. (For details on the error output function, refer to ERRB/AIN3P Pin Function)

CSAMP3_EN	Current Sense Amplifier
0	Disabled (ERRB enabled)
1	Enabled (ERRB disabled)

The current sense amplifier gain can be changed by setting CS1_GAIN_SEL [1:0], CS2_GAIN_SEL [1:0], and CS3_GAIN_SEL [1:0] for each amplifier. This is the gain when using the AINxP and AINxN (x: 1 to 3) pin inputs.

CS1_GAIN_SEL [1:0] CS2_GAIN_SEL [1:0] CS3_GAIN_SEL [1:0]		Gain
0	0	16 times
0	1	24 times
1	0	32 times
1	1	48 times

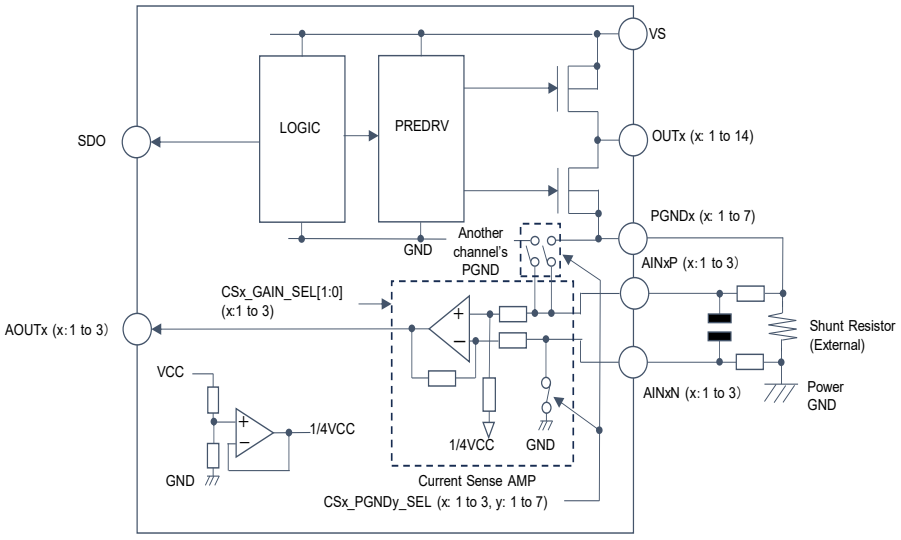


Figure 22. Current Sense Amplifier Current-Sensing Connection Diagram 1

Current Sense Amplifier - Continued

In addition, this IC also has a function to reduce the board pattern wiring between the AINxP (x: 1, 2), AINxN (x: 1, 2) input terminals and the shunt resistor, provided that the shunt resistor accuracy of the shunt resistor including the board pattern wiring resistance does not cause a problem. (Refer to Figure 23. Current Sense Amplifier Current-Sensing Connection Diagram 2.)

To use this function, select the connection from PGND using the control registers to use the wiring inside the IC.
There are three types of connection selection switches (approx. 200 Ω <Typ>):

- Type1: Between Current Sense AMP1 and PGNDx (x: 1 to 7)
- Type2: Between Current Sense AMP2 and PGNDy (y: 5 to 7)
- Type3: Between Current Sense AMP3 and PGNDz (z: 1 to 4)

The control registers corresponding to these switches are as follows:

- Type1: CS1_PGNDx_SEL (x: 1 to 7)
- Type2: CS2_PGNDy_SEL (y: 5 to 7)
- Type3: CS3_PGNDz_SEL (z: 1 to 4)

In addition to connecting only the driver current to be monitored, the current detection AMP1 can also monitor the total current of all channels by turning on all the connection switches to PGND1 to 7.

CS1_PGNDx_SEL (x: 1 to 7)	Sense Line Switches
0	Open
1	Short

CS2_PGNDy_SEL (y: 5 to 7)	Sense Line Switches
0	Open
1	Short

CS3_PGNDz_SEL (z: 1 to 4)	Sense Line Switches
0	Open
1	Short

The current sense amplifier gain can be changed by setting CS1_GAIN_SEL [1:0], CS2_GAIN_SEL [1:0], and CS3_GAIN_SEL [1:0] for each AMP. (This is the gain when using the sense line switches.)

CS1_GAIN_SEL [1:0] CS2_GAIN_SEL [1:0] CS3_GAIN_SEL [1:0]		Gain
0	0	15.8 times
0	1	23.7 times
1	0	31.6 times
1	1	47.4 times

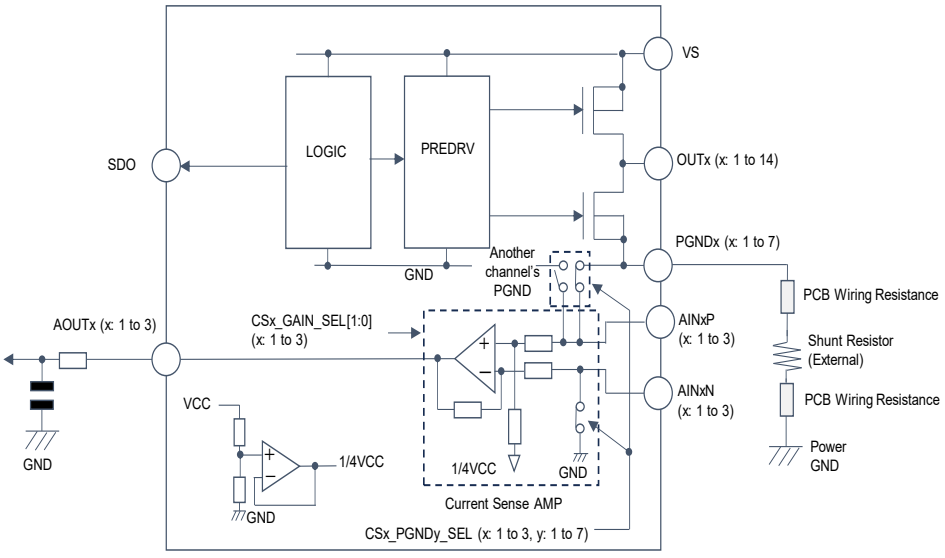


Figure 23. Current Sense Amplifier Current-Sensing Connection Diagram 2

EN Pin and Reset Operation

The following reset operations are available. Each register setting is reset and returns to the initial state.

Table 10. Reset Operation

Item	Detail
EN = Low	The IC circuit operation stops. It is initialized and starts operating when EN = High.
VCUV (VCC Undervoltage Detection)	The LOGIC circuit is in reset state. It starts operating when the low voltage state is released.
Software Reset	The LOGIC circuit is initialized when EN = High. Send data of 5Ah to register address 00h using the SPI command to immediately initialize all registers.

When resetting or restarting with EN = High→Low→High, hold at least 10 µs of the EN = Low interval.

ERRB/AIN3P Pin Function

The ERRB/AIN3P pin combines the error output (ERRB) function and the input (AIN3P) function of the current sense amplifier 3, and these functions cannot be used at the same time. Depending on the register CSAMP3_EN setting, the function is switched.

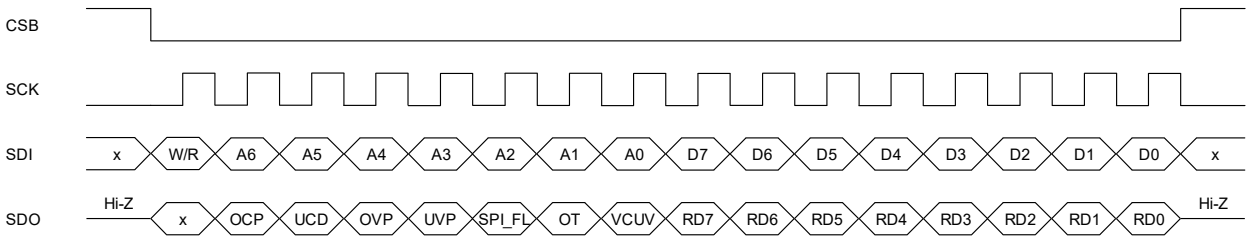
CSAMP3_EN	ERRB Function	CSAMP3 Function
0	Enabled	Disabled
1	Disabled	Enabled

The ERRB function notifies an error via the ERRB/AIN3P pin when an error is detected. For more information on timing the error output, refer to the timing chart for each protection function.

Serial Interface

SPI Protocol

The serial interface allows reading the status register and configuring each IC setting. The input pins CSB, SCK, and SDI are used. When CSB is low, serial data is accepted. Write data (SDI) consists of a total of 16 bits: an 8-bit address and 8 bits of data. SDI data is captured on the rising edge of SCK, and after all 16 bits of data have been received, it is written to the register. Read data (SDO) outputs various statuses for faults and register values of the specified address. SDO data also starts being output on the rising edge of SCK. When CSB goes from low to high, the SPI transfer is considered to be completed and the internal register starts being updated.



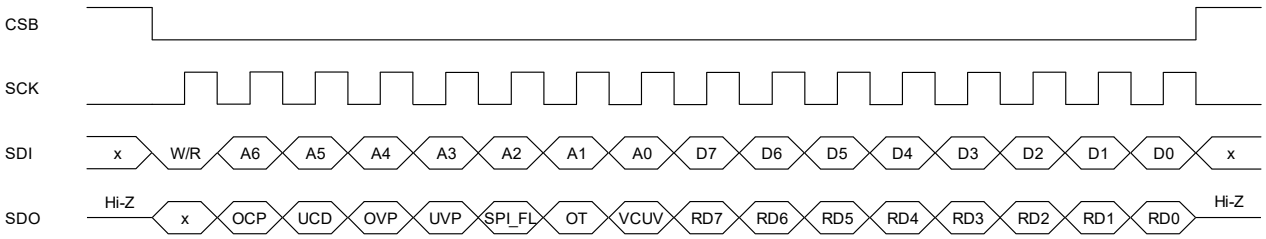
W/R: Read/Write specified bit
A6-A0: Address Data
D7-D0: Data to be written to the address specified by bits A6-A0
RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 24. SPI Protocol

SPI Protocol - Continued

Writing

To write to a register, set the W/R bit to low. The A6-A0 bits specify the address of the register to be written to, and D7-D0 specify the data to be written to the register. When writing, data is also output from SDO. The SDO output data bits OCP, UCD, OVP, UVP, SPI_FL, OT, and VCUV are called the Global status registers, and output the protection status. The RD7-RD0 bits output the register value (the value immediately before the write) of the address specified by the A6-A0 bits.

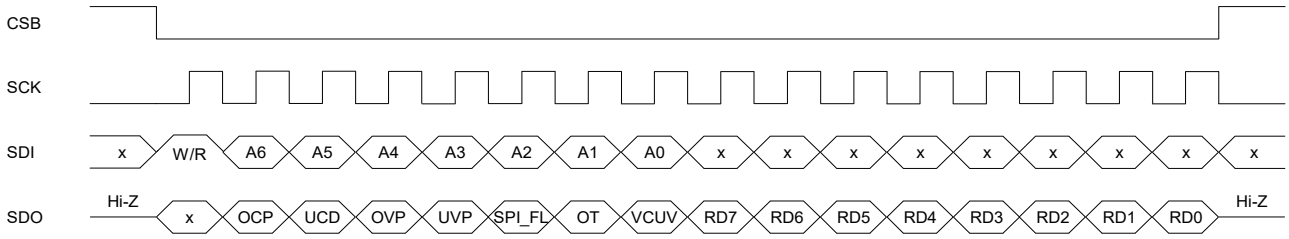


W/R: Read/Write specified bit
A6-A0: Address Data
D7-D0: Data to be written to the address specified by bits A6-A0
RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 25. Register Write Protocol

Reading

To read a register, set the W/R bit to High. The A6-A0 bits specify the address of the register to be read. Any SDI data in a correct SPI transaction thereafter is ignored. The individual register data is output from SDO. As with writing, the OCP, UCD, OVP, UVP, SPI_FL, OT, and VCUV bits of the SDO output data are global status registers and output the protection status. The RD7-RD0 bits output the register value (the value immediately before the write) of the address specified by the A6-A0 bits.



W/R: Read/Write specified bit
A6-A0: Address Data
RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 26. Register Read Protocol

Global Status Registers

The global status registers are data bits in SDO that output the protection status. These are the OCP, UCD, OVP, UVP, SPI_FL, OT, and VCUV bits of the SDO output data. It works in conjunction with the normal status register (ST_XXX) and is assigned as follows.

OCP bit : ST_OCPHx, ST_OCPLx (x: 1 to 14)
UCD bit : ST_UCDHx, ST_UCDLx (x: 1 to 14)
OVP bit : ST_VSOV
UVP bit : ST_VSUV
SPI_FL bit : ST_SPI
OT bit : ST_TW, ST_TSD
VCUV bit : ST_VCUV

The global status registers (OCP, UCD, and OT bits) to which multiple status registers are assigned outputs the OR logic of each status register, so an error is notified if any of the protections is detected. If you want to identify the location where an abnormality has occurred, check the status register.

When the value of each status register (ST_XXX) is cleared, the value of the corresponding global status register is also cleared.

Register Map

The following table lists the register maps. Each register is SPI programmable.

R/W	Address	Data								Initial Value
15	14-8	7	6	5	4	3	2	1	0	
W	00h	Software Reset								00h
R/W	01h	CSAMP			READ_SEL	-	-	DRV_ SET_CLR	SRR	00h
		3_EN	2_EN	1_EN						
R/W	02h	ST_OCP								00h
		H4	L4	H3	L3	H2	L2	H1	L1	
R/W	03h	ST_OCP								00h
		H8	L8	H7	L7	H6	L6	H5	L5	
R/W	04h	ST_OCP								00h
		H12	L12	H11	L11	H10	L10	H9	L9	
R/W	05h	-	-	-	-	ST_OCP				00h
						H14	L14	H13	L13	
R/W	06h	ST_UCD								00h
		H4	L4	H3	L3	H2	L2	H1	L1	
R/W	07h	ST_UCD								00h
		H8	L8	H7	L7	H6	L6	H5	L5	
R/W	08h	ST_UCD								00h
		H12	L12	H11	L11	H10	L10	H9	L9	
R/W	09h	-	-	-	-	ST_UCD				00h
						H14	L14	H13	L13	
R/W	0Ah	ST_VSOV	ST_VSUV	-	ST_VCUV	-	ST_SPI	ST_TW	ST_TSD	10h
R/W	0Bh	-	-	-	-	-	-	-	-	00h
R/W	0Ch	-	-	-	-	-	-	-	-	00h
R/W	0Dh	-	-	-	-	-	-	-	MASK_UCD	00h
R/W	0Eh	-	-	-	-	-	-	-	-	00h
R/W	0Fh	-	-	-	-	-	-	-	-	00h

Register Map - Continued

R/W	Address	Data								Initial Value
15	14-8	7	6	5	4	3	2	1	0	
R/W	10h	-	-	-	-	-	-	-	-	00h
R/W	11h	-	-	-	-	-	-	-	-	00h
R/W	12h	-	OUT2_PWMSEL			-	OUT1_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	13h	-	OUT4_PWMSEL			-	OUT3_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	14h	-	OUT6_PWMSEL			-	OUT5_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	15h	-	OUT8_PWMSEL			-	OUT7_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	16h	-	OUT10_PWMSEL			-	OUT9_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	17h	-	OUT12_PWMSEL			-	OUT11_PWMSEL			00h
			[2]	[1]	[0]		[3]	[1]	[0]	
R/W	18h	-	OUT14_PWMSEL			-	OUT13_PWMSEL			00h
			[2]	[1]	[0]		[2]	[1]	[0]	
R/W	19h	-	SYNC_ EN-OUT2	HSC-OUT 2	LSC-OUT 2	-	SYNC_ EN-OUT1	HSC-OUT 1	LSC-OUT 1	00h
R/W	1Ah	-	SYNC_ EN-OUT4	HSC-OUT 4	LSC-OUT 4	-	SYNC_ EN-OUT3	HSC-OUT 3	LSC-OUT 3	00h
R/W	1Bh	-	SYNC_ EN-OUT6	HSC-OUT 6	LSC-OUT 6	-	SYNC_ EN-OUT5	HSC-OUT 5	LSC-OUT 5	00h
R/W	1Ch	-	SYNC_ EN-OUT8	HSC-OUT 8	LSC-OUT 8	-	SYNC_ EN-OUT7	HSC-OUT 7	LSC-OUT 7	00h
R/W	1Dh	-	SYNC_ EN-OUT10	HSC-OUT 10	LSC-OUT 10	-	SYNC_ EN-OUT9	HSC-OUT 9	LSC-OUT 9	00h
R/W	1Eh	-	SYNC_ EN-OUT12	HSC-OUT 12	LSC-OUT 12	-	SYNC_ EN-OUT11	HSC-OUT 11	LSC-OUT 11	00h
R/W	1Fh	-	SYNC_ EN-OUT14	HSC-OUT 14	LSC-OUT 14	-	SYNC_ EN-OUT13	HSC-OUT 13	LSC-OUT 13	00h

Register Map - Continued

R/W	Address	Data								Initial Value
15	14-8	7	6	5	4	3	2	1	0	
R/W	20h	PWM_FREQ_A		PWM_DUTY_A						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	21h	PWM_FREQ_B		PWM_DUTY_B						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	22h	PWM_FREQ_C		PWM_DUTY_C						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	23h	PWM_FREQ_D		PWM_DUTY_D						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	24h	PWM_FREQ_E		PWM_DUTY_E						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	25h	PWM_FREQ_F		PWM_DUTY_F						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	26h	PWM_FREQ_G		PWM_DUTY_G						00h
		[1]	[0]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	27h	PDEAD_D		PDEAD_C		PDEAD_B		PDEAD_A		55h
		[1]	[0]	[1]	[0]	[1]	[0]	[1]	[0]	
R/W	28h	-	-	PDEAD_G		PDEAD_F		PDEAD_E		15h
				[1]	[0]	[1]	[0]	[1]	[0]	
W	29h	-	-	-	-	-	-	-	DRV_ON	00h
R/W	2Ah	-	-	-	-	-	-	-	-	00h
R/W	2Bh	OVPSEL	-	LAT_UV	LAT_OV	-	-	LAT_TW	LAT_TSD	B3h
R/W	2Ch	-	-	-	-	-	-	FLG_UCD	FLG_TW	03h
R/W	2Dh	-	CS1_PGND							00h
			7_SEL	6_SEL	5_SEL	4_SEL	3_SEL	2_SEL	1_SEL	
R/W	2Eh	-	CS2_PGND			CS3_PGND				00h
			7_SEL	6_SEL	5_SEL	4_SEL	3_SEL	2_SEL	1_SEL	
R/W	2Fh	-	-	CS3_GAIN_SEL		CS2_GAIN_SEL		CS1_GAIN_SEL		00h
				[1]	[0]	[1]	[0]	[1]	[0]	

Register Map - Continued

R/W	Address	Data								Initial Value
15	14-8	7	6	5	4	3	2	1	0	
R/W	30h	-	-	-	-	-	-	-	-	00h
R/W	31h	-	-	-	-	-	-	-	SOS_EN	00h
R/W	32h	SET_SOS								00h
		8	7	6	5	4	3	2	1	
R/W	33h	-	-	SET_SOS						00h
				14	13	12	11	10	9	
R	34h	CHK_SOS								00h
		8	7	6	5	4	3	2	1	
R	35h	-	-	CHK_SOS						00h
				14	13	12	11	10	9	
R/W	36h	-	-	-	-	-	-	-	-	00h
R/W	37h	Reserved1								00h
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	38h	Reserved2								00h
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
R/W	39h	-	-	-	-	-	-	-	-	00h
R/W	3Ah	-	-	-	-	-	-	-	-	00h
R/W	3Bh	-	-	-	-	-	-	-	-	00h
R/W	3Ch	-	-	-	-	-	-	-	-	00h
R/W	3Dh	-	-	-	-	-	-	-	-	00h
R/W	3Eh	-	-	-	-	-	-	-	-	00h
R/W	3Fh	-	-	-	-	-	-	-	-	00h

Explanation of Each Register

Address = 00h

Symbol	Bit	Description
Software Reset	[7:0]	Software Reset This initializes the digital block. All registers are initialized. You can run Software Reset by sending 5Ah data. When EN pin is "1", the Software Reset command can be used.

Address = 01h

Symbol	Bit	Description
CSAMP3_EN	7	Current Sense Amplifier 3 Enable For configuration details, please refer to Current Sense Amplifier.
CSAMP2_EN	6	Current Sense Amplifier 2 Enable For configuration details, please refer to Current Sense Amplifier.
CSAMP1_EN	5	Current Sense Amplifier 1 Enable For configuration details, please refer to Current Sense Amplifier.
READ_SEL	4	Read Operation Control for the driver setting registers (Address = 12h to 28h). READ_SEL switches the value output of the IC during a driver setting register read operation. READ_SEL = 0: Outputs the value of driver setting registers READ_SEL = 1: Outputs the value of gate drive setting (value reflected by DRV_ON)
-	3	-
-	2	-
DRV_SET_CLR	1	Driver Setting Register Clear By writing DRV_SET_CLR = 1, the drive settings set by DRV_ON = 1 are cleared. The driver configuration registers (Address = 12h to 28h) are also initialized.
SRR	0	Status Register Clear By writing SRR = 1, all status registers (Address = 02h to 0Ah) are cleared to 0. After starting the IC, please set SRR = 1 and clear the values of all status registers to confirm that the registers can be controlled by SPI communication.

Explanation of Each Register - Continued

Address = 02h

Symbol	Bit	Description
ST_OCPH4	7	Over Current Protection “OCP” Results ST_OCPHx / ST_OCPLx (x: 1 to 4) = 0: Not detected ST_OCPHx / ST_OCPLx (x: 1 to 4) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Over Current Protection (OCP).
ST_OCPL4	6	
ST_OCPH3	5	
ST_OCPL3	4	
ST_OCPH2	3	
ST_OCPL2	2	
ST_OCPH1	1	
ST_OCPL1	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_OCPXX (status register). The corresponding global status register will also be reset to 0. If ST_OCPXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Address = 03h

Symbol	Bit	Description
ST_OCPH8	7	Over Current Protection “OCP” Results ST_OCPHx / ST_OCPLx (x: 5 to 8) = 0: Not detected ST_OCPHx / ST_OCPLx (x: 5 to 8) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Over Current Protection (OCP).
ST_OCPL8	6	
ST_OCPH7	5	
ST_OCPL7	4	
ST_OCPH6	3	
ST_OCPL6	2	
ST_OCPH5	1	
ST_OCPL5	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_OCPXX (status register). The corresponding global status register will also be reset to 0. If ST_OCPXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Address = 04h

Symbol	Bit	Description
ST_OCPH12	7	Over Current Protection “OCP” Results ST_OCPHx / ST_OCPLx (x: 9 to 12) = 0: Not detected ST_OCPHx / ST_OCPLx (x: 9 to 12) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Over Current Protection (OCP).
ST_OCPL12	6	
ST_OCPH11	5	
ST_OCPL11	4	
ST_OCPH10	3	
ST_OCPL10	2	
ST_OCPH9	1	
ST_OCPL9	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_OCPXX (status register). The corresponding global status register will also be reset to 0. If ST_OCPXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Explanation of Each Register - Continued

Address = 05h

Symbol	Bit	Description
-	[7:4]	-
ST_OCPH14	3	Over Current Protection “OCP” Results ST_OCPHx / ST_OCPLx (x: 13 to 14) = 0: Not detected ST_OCPHx / ST_OCPLx (x: 13 to 14) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Over Current Protection (OCP).
ST_OCPL14	2	
ST_OCPH13	1	
ST_OCPL13	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_OCPXX (status register). The corresponding global status register will also be reset to 0. If ST_OCPXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Address = 06h

Symbol	Bit	Description
ST_UCDH4	7	Under Current Detection “UCD” Result ST_UCDHx / ST_UCDLx (x: 1 to 4) = 0: Not detected ST_UCDHx / ST_UCDLx (x: 1 to 4) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Under Current Detection (UCD).
ST_UCDL4	6	
ST_UCDH3	5	
ST_UCDL3	4	
ST_UCDH2	3	
ST_UCDL2	2	
ST_UCDH1	1	
ST_UCDL1	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_UCDXX (status register). The corresponding global status register will also be reset to 0. If ST_UCDXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Address = 07h

Symbol	Bit	Description
ST_UCDH8	7	Under Current Detection “UCD” Result ST_UCDHx / ST_UCDLx (x: 5 to 8) = 0: Not detected ST_UCDHx / ST_UCDLx (x: 5 to 8) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Under Current Detection (UCD).
ST_UCDL8	6	
ST_UCDH7	5	
ST_UCDL7	4	
ST_UCDH6	3	
ST_UCDL6	2	
ST_UCDH5	1	
ST_UCDL5	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_UCDXX (status register). The corresponding global status register will also be reset to 0. If ST_UCDXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Explanation of Each Register - Continued

Address = 08h

Symbol	Bit	Description
ST_UCDH12	7	Under Current Detection “UCD” Result ST_UCDHx / ST_UCDLx (x: 9 to 12) = 0: Not detected ST_UCDHx / ST_UCDLx (x: 9 to 12) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Under Current Detection (UCD).
ST_UCDL12	6	
ST_UCDH11	5	
ST_UCDL11	4	
ST_UCDH10	3	
ST_UCDL10	2	
ST_UCDH9	1	
ST_UCDL9	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_UCDXX (status register). The corresponding global status register will also be reset to 0. If ST_UCDXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Address = 09h

Symbol	Bit	Description
-	[7:4]	-
ST_UCDH14	3	Under Current Detection “UCD” Result ST_UCDHx / ST_UCDLx (x: 13 to 14) = 0: Not detected ST_UCDHx / ST_UCDLx (x: 13 to 14) = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Under Current Detection (UCD).
ST_UCDL14	2	
ST_UCDH13	1	
ST_UCDL13	0	

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_UCDXX (status register). The corresponding global status register will also be reset to 0. If ST_UCDXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

Explanation of Each Register - Continued

Address = 0Ah

Symbol	Bit	Description
ST_VSOV	7	VS Over Voltage Protection “VSOV” Result ST_VSOV = 0: Not detected ST_VSOV = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For more information on the protection function, please refer to VS Over Voltage Protection (VSOV).
ST_VSUV	6	VS Under Voltage Lock Out Detection Result ST_VSUV = 0: Not detected ST_VSUV = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to VS Under Voltage Lock Out (VSUV).
-	5	-
ST_VCUV	4	VCC Under Voltage “VCCUV” Detection Result ST_VCUV = 0: Not detected ST_VCUV = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 2)* For protection features, please refer to VCC Under Voltage Protection (VCCUV).
-	3	-
ST_SPI	2	Erroneous SPI Transmission Result ST_SPI = 0: Not detected ST_SPI = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Erroneous SPI Transmission (Transmission Error: SPI_FAIL).
ST_TW	1	Thermal Warning “TW” Result ST_TW = 0: Not detected ST_TW = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Thermal Shutdown (TSD)/Thermal Warning (TW).
ST_TSD	0	Thermal Shutdown “TSD” Result ST_TSD = 0: Not detected ST_TSD = 1: Detected Read and clear operations are selectable using R/W bit. *(Note 1)* For protection features, please refer to Thermal Shutdown (TSD)/Thermal Warning (TW).

(Note 1) R/W = 1: Read mode. Each abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be reset to 0 by writing 1 to each register ST_XXX (status register). The corresponding global status register will also be reset to 0. If ST_XXX = 1 is written during abnormality detection, the status register will be reset to 0 once, and then the abnormality detection result will be reflected in the status register again.

(Note 2) R/W = 1: Read mode. The abnormality detection result can be read. Writing data is ignored.
R/W = 0: Write mode. The abnormality detection result can be set to 0 by writing 1 to the ST_VCUV register (status register). The corresponding global status register will also be set to 0.
Only the register ST_VCUV has a different initial value than the other status registers. The initial value is ST_VCUV = 1 (abnormality detected), so it is necessary to set the value to ST_VCUV = 0 once. If an abnormality is detected after that, it will be reset to ST_VCUV = 1. Note that if a VCC undervoltage abnormality is detected, the entire LOGIC circuit is reset, and so the values of other abnormality detection results and settings are also reset.

Explanation of Each Register - Continued

Address = 0Dh

Symbol	Bit	Description
-	[7:1]	-
MASK_UCD	0	UCD Masking Function MASK_UCD = 0: Mask function disabled (UCD enabled) MASK_UCD = 1: Mask function enabled (UCD disabled) For protection features, please refer to Under Current Detection (UCD).

Address = 12h

Symbol	Bit	Description
-	7	-
OUT2_PWMSEL	[6:4]	OUT2 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT1_PWMSEL	[2:0]	OUT2 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Address = 13h

Symbol	Bit	Description
-	7	-
OUT4_PWMSEL	[6:4]	OUT4 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT3_PWMSEL	[2:0]	OUT3 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Address = 14h

Symbol	Bit	Description
-	7	-
OUT6_PWMSEL	[6:4]	OUT6 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT5_PWMSEL	[2:0]	OUT5 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Explanation of Each Register - Continued

Address = 15h

Symbol	Bit	Description
-	7	-
OUT8_PWMSEL	[6:4]	OUT8 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT7_PWMSEL	[2:0]	OUT7 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Address = 16h

Symbol	Bit	Description
-	7	-
OUT10_PWMSEL	[6:4]	OUT10 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT9_PWMSEL	[2:0]	OUT9 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Address = 17h

Symbol	Bit	Description
-	7	-
OUT12_PWMSEL	[6:4]	OUT12 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT11_PWMSEL	[2:0]	OUT11 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Address = 18h

Symbol	Bit	Description
-	7	-
OUT14_PWMSEL	[6:4]	OUT14 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.
-	3	-
OUT13_PWMSEL	[2:0]	OUT13 PWM Output Setting Register As shown in Table 3. PWM Table Settings, PWM MODE OFF or PWM_TABLE_x (x: A to G) can be selected.

Explanation of Each Register - Continued

Address = 19h

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT2	6	OUT2 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT2 pin is determined by selecting the state of G2H and G2L inside the IC.
HSC-OUT2	5	
LSC-OUT2	4	
-	3	-
SYNC_EN-OUT1	2	OUT1 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT1 pin is determined by selecting the state of G1H and G1L inside the IC.
HSC-OUT1	1	
LSC-OUT1	0	

Address = 1Ah

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT4	6	OUT4 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT4 pin is determined by selecting the state of G4H and G4L inside the IC.
HSC-OUT4	5	
LSC-OUT4	4	
-	3	-
SYNC_EN-OUT3	2	OUT3 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT3 pin is determined by selecting the state of G3H and G3L inside the IC.
HSC-OUT3	1	
LSC-OUT3	0	

Address = 1Bh

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT6	6	OUT6 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT6 pin is determined by selecting the state of G6H and G6L inside the IC.
HSC-OUT6	5	
LSC-OUT6	4	
-	3	-
SYNC_EN-OUT5	2	OUT5 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT5 pin is determined by selecting the state of G5H and G5L inside the IC.
HSC-OUT5	1	
LSC-OUT5	0	

Explanation of Each Register - Continued

Address = 1Ch

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT8	6	OUT8 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT8 pin is determined by selecting the state of G8H and G8L inside the IC.
HSC-OUT8	5	
LSC-OUT8	4	
-	3	-
SYNC_EN-OUT7	2	OUT7 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT7 pin is determined by selecting the state of G7H and G7L inside the IC.
HSC-OUT7	1	
LSC-OUT7	0	

Address = 1Dh

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT10	6	OUT10 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT10 pin is determined by selecting the state of G10H and G10L inside the IC.
HSC-OUT10	5	
LSC-OUT10	4	
-	3	-
SYNC_EN-OUT9	2	OUT9 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT9 pin is determined by selecting the state of G9H and G9L inside the IC.
HSC-OUT9	1	
LSC-OUT9	0	

Address = 1Eh

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT12	6	OUT12 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT12 pin is determined by selecting the state of G12H and G12L inside the IC.
HSC-OUT12	5	
LSC-OUT12	4	
-	3	-
SYNC_EN-OUT11	2	OUT11 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT11 pin is determined by selecting the state of G11H and G11L inside the IC.
HSC-OUT11	1	
LSC-OUT11	0	

Explanation of Each Register - Continued

Address = 1Fh

Symbol	Bit	Description
-	7	-
SYNC_EN-OUT14	6	OUT14 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT14 pin is determined by selecting the state of G14H and G14L inside the IC.
HSC-OUT14	5	
LSC-OUT14	4	
-	3	-
SYNC_EN-OUT13	2	OUT13 Output Setting Register As described in Synchronous and Asynchronous Control, the output of the OUT13 pin is determined by selecting the state of G13H and G13L inside the IC.
HSC-OUT13	1	
LSC-OUT13	0	

Address = 20h

Symbol	Bit	Description
PWM_FREQ_A	[7:6]	PWM_TABLE_A Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_A	[5:0]	PWM_TABLE_A Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 21h

Symbol	Bit	Description
PWM_FREQ_B	[7:6]	PWM_TABLE_B Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_B	[5:0]	PWM_TABLE_B Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 22h

Symbol	Bit	Description
PWM_FREQ_C	[7:6]	PWM_TABLE_C Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_C	[5:0]	PWM_TABLE_C Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 23h

Symbol	Bit	Description
PWM_FREQ_D	[7:6]	PWM_TABLE_D Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_D	[5:0]	PWM_TABLE_D Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 24h

Symbol	Bit	Description
PWM_FREQ_E	[7:6]	PWM_TABLE_E Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_E	[5:0]	PWM_TABLE_E Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Explanation of Each Register - Continued

Address = 25h

Symbol	Bit	Description
PWM_FREQ_F	[7:6]	PWM_TABLE_F Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_F	[5:0]	PWM_TABLE_F Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 26h

Symbol	Bit	Description
PWM_FREQ_G	[7:6]	PWM_TABLE_G Frequency Setting Register For information about the settings, please refer to Table 4. PWM Frequency Settings.
PWM_DUTY_G	[5:0]	PWM_TABLE_G Duty Setting Register For information about the settings, please refer to Table 5. PWM Duty Settings.

Address = 27h

Symbol	Bit	Description
PDEAD_D	[7:6]	PWM_TABLE_D Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.
PDEAD_C	[5:4]	PWM_TABLE_C Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.
PDEAD_B	[3:2]	PWM_TABLE_B Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.
PDEAD_A	[1:0]	PWM_TABLE_A Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.

Address = 28h

Symbol	Bit	Description
-	[7:6]	-
PDEAD_G	[5:4]	PWM_TABLE_G Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.
PDEAD_F	[3:2]	PWM_TABLE_F Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.
PDEAD_E	[1:0]	PWM_TABLE_E Dead Time Setting Register For information about the settings, please refer to Table 7. PWM Dead Time Settings.

Address = 29h

Symbol	Bit	Description
-	[7:1]	-
DRV_ON	0	Driver Settings Update Register After writing DRV_ON = 1, the IC reflects the value of the driver setting registers (Address = 12h to 28h) to the gate drives. After the settings are reflected, the IC automatically sets DRV_ON = 0. When DRV_ON = 0, the gates are driven using the setting values reflected previously.

Explanation of Each Register - Continued

Address = 2Bh

Symbol	Bit	Description
OVPSEL	7	VSOV Threshold Setting Register OVPSEL = 0 Detect: VS > 36 V (TYP) Release: VS < 33.5 V (TYP) OVPSEL = 1 Detect: VS > 20 V (TYP) Release: VS < 18 V (TYP) For protection features, please refer to VS Over Voltage Protection (VSOV).
-	6	-
LAT_UV	5	ST_VSUV Latch Setting Register LAT_UV = 0: Latch Function OFF LAT_UV = 1: Latch Function ON For protection features, please refer to VS Under Voltage Lock Out (VSUV).
LAT_OV	4	ST_VSOV Latch Setting Register LAT_OV = 0: Latch Function OFF LAT_OV = 1: Latch Function ON For protection features, please refer to VS Over Voltage Protection (VSOV).
-	[3:2]	-
LAT_TW	1	ST_TW Latch Setting Register LAT_TW = 0: Latch Function OFF LAT_TW = 1: Latch Function ON For protection features, please refer to Thermal Shutdown (TSD)/Thermal Warning (TW).
LAT_TSD	0	ST_TSD Latch Setting Register LAT_TSD = 0: Latch Function OFF LAT_TSD = 1: Latch Function ON For protection features, please refer to Thermal Shutdown (TSD)/Thermal Warning (TW).

Address = 2Ch

Symbol	Bit	Description
-	[7:2]	-
FLG_UCD	1	ST_UCDHx / ST_UCDLx (x: 1 to 14) Output Setting Register for the ERRB pin FLG_UCD = 0: ST_UCDHx / ST_UCDLx (x: 1 to 14) is not output to the ERRB pin. FLG_UCD = 1: ST_UCDHx / ST_UCDLx (x: 1 to 14) is output to the ERRB pin.
FLG_TW	0	TW Detection Output Setting Register for the ERRB pin FLG_TW = 0: The TW detection signal is not output to the ERRB pin. FLG_TW = 1: The TW detection signal is output to the ERRB pin.

Explanation of Each Register - Continued

Address = 2Dh

Symbol	Bit	Description
-	7	-
CS1_PGND7_SEL	6	Connection SW Setting Between the Current Sense Amplifier 1 and PGND1 to 7 For configuration details, refer to Current Sense Amplifier.
CS1_PGND6_SEL	5	
CS1_PGND5_SEL	4	
CS1_PGND4_SEL	3	
CS1_PGND3_SEL	2	
CS1_PGND2_SEL	1	
CS1_PGND1_SEL	0	

Address = 2Eh

Symbol	Bit	Description
-	7	-
CS2_PGND7_SEL	6	Connection SW Setting Between the Current Sense Amplifier 2 and PGND5 to 7 For configuration details, refer to Current Sense Amplifier.
CS2_PGND6_SEL	5	
CS2_PGND5_SEL	4	
CS3_PGND4_SEL	3	Connection SW Setting Between the Current Sense Amplifier 3 and PGND1 to 4 For configuration details, refer to Current Sense Amplifier.
CS3_PGND3_SEL	2	
CS3_PGND2_SEL	1	
CS3_PGND1_SEL	0	

Address = 2Fh

Symbol	Bit	Description
-	[7:6]	-
CS3_GAIN_SEL [1]	5	Current Sense Amplifier 3 Gain Setting For configuration details, refer to Current Sense Amplifier.
CS3_GAIN_SEL [0]	4	
CS2_GAIN_SEL [1]	3	Current Sense Amplifier 2 Gain Setting For configuration details, refer to Current Sense Amplifier.
CS2_GAIN_SEL [0]	2	
CS1_GAIN_SEL [1]	1	Current Sense Amplifier 1 Gain Setting For configuration details, refer to Current Sense Amplifier.
CS1_GAIN_SEL [0]	0	

Explanation of Each Register - Continued

Address = 31h

Symbol	Bit	Description
-	[7:1]	-
SOS_EN	0	Static Open/Short Detection Startup Register When SOS_EN = 1, static open/short detection is activated. For details on the detection function, refer to Static Open/Short Detection (SOS).

Address = 32h

Symbol	Bit	Description
SET_SOS8	7	Open/Short Detection Switch Control Register for Checking each OUT Pin SET_SOSx (x: 1 to 8) = 0: Each OUTx (x: 1 to 8) Attached Switch OFF SET_SOSx (x: 1 to 8) = 1: Each OUTx (x: 1 to 8) Attached Switch ON For more information about the detection feature, please refer to Static Open/Short Detection (SOS).
SET_SOS7	6	
SET_SOS6	5	
SET_SOS5	4	
SET_SOS4	3	
SET_SOS3	2	
SET_SOS2	1	
SET_SOS1	0	

Address = 33h

Symbol	Bit	Description
-	[7:6]	-
SET_SOS14	5	Open/Short Detection Switch Control Register for Checking each OUT Pin SET_SOSx (x: 9 to 14) = 0: Each OUTx (x: 9 to 14) Attached Switch OFF SET_SOSx (x: 9 to 14) = 1: Each OUTx (x: 9 to 14) Attached Switch ON For more information about the detection feature, please refer to Static Open/Short Detection (SOS).
SET_SOS13	4	
SET_SOS12	3	
SET_SOS11	2	
SET_SOS10	1	
SET_SOS9	0	

Explanation of Each Register - Continued

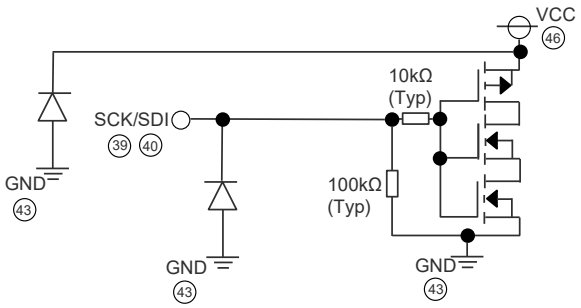
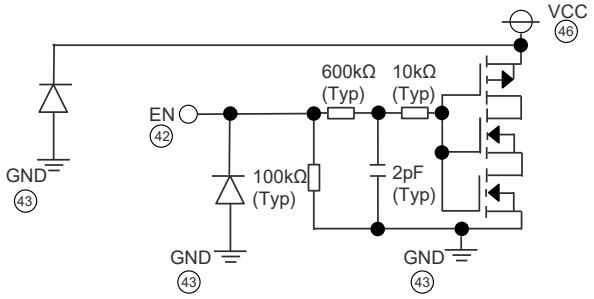
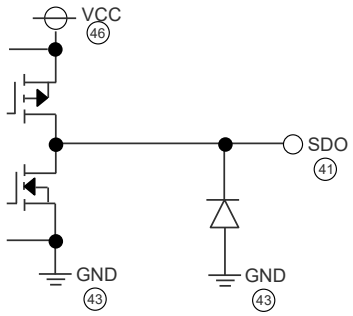
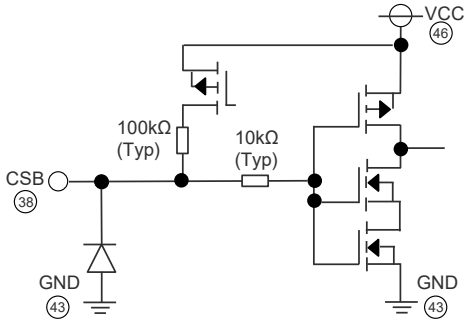
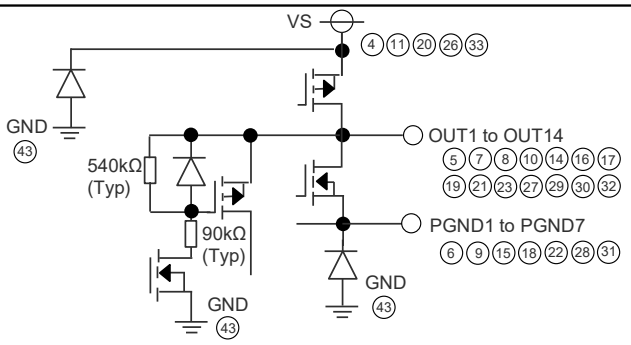
Address = 34h

Symbol	Bit	Description
CHK_SOS8	7	Open/Short Detection Result for each OUT Pin CHK_SOSx (x: 1 to 8) : Detection result of OUTx (x: 1 to 8) For details on the judgment table and detection function, please refer to Static Open/Short Detection (SOS).
CHK_SOS7	6	
CHK_SOS6	5	
CHK_SOS5	4	
CHK_SOS4	3	
CHK_SOS3	2	
CHK_SOS2	1	
CHK_SOS1	0	

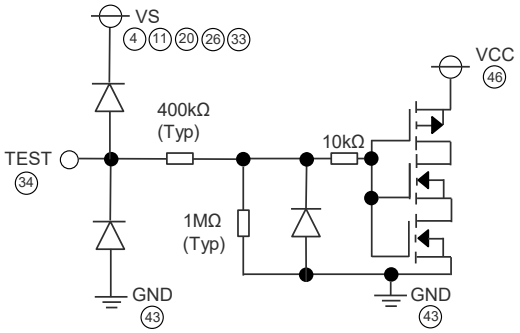
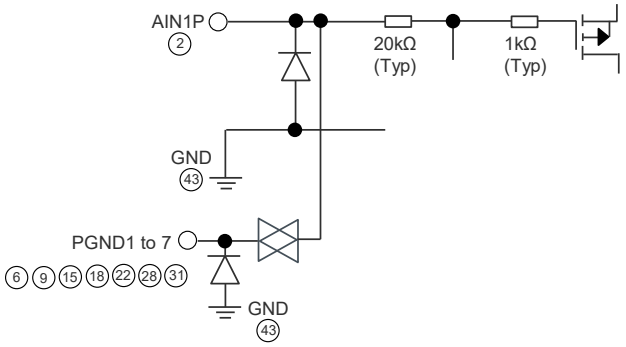
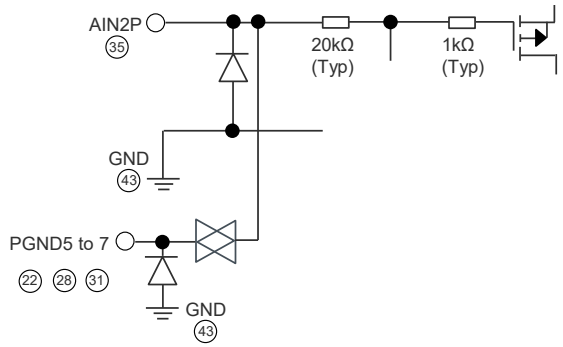
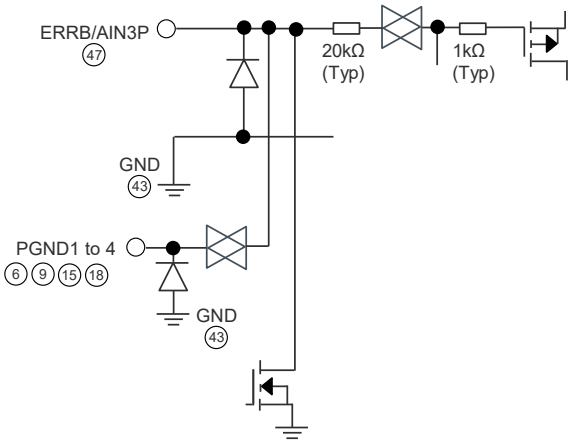
Address = 35h

Symbol	Bit	Description
-	[7:6]	-
CHK_SOS14	5	Open/Short Detection Result for each OUT Pin CHK_SOSx (x: 9 to 14) : Detection result of OUTx (x: 9 to 14) For details on the judgment table and detection function, please refer to Static Open/Short Detection (SOS).
CHK_SOS13	4	
CHK_SOS12	3	
CHK_SOS11	2	
CHK_SOS10	1	
CHK_SOS9	0	

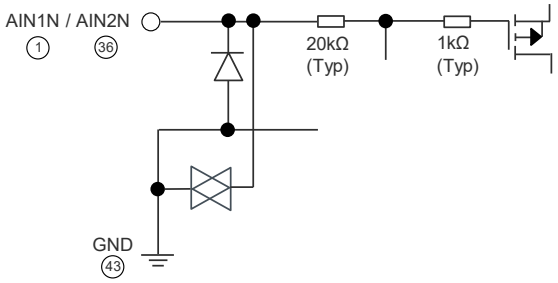
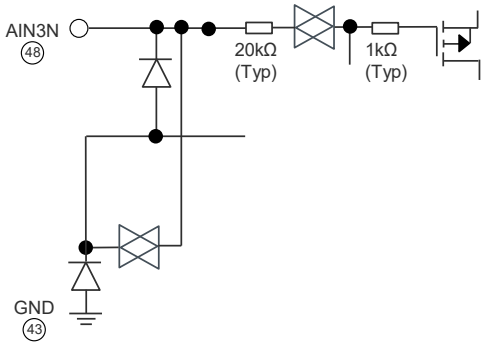
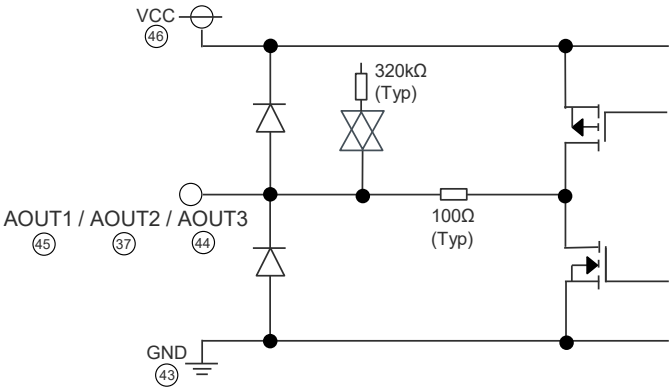
I/O Equivalence Circuits

Pin No.	Pin name	Equivalence circuit
39 40	SCK SDI	
42	EN	
41	SDO	
38	CSB	
5, 7, 8, 10, 14, 16, 17, 19, 21, 23, 27, 29, 30, 32	OUT1 ~ OUT14	

I/O Equivalence Circuits - Continued

Pin No.	Pin name	Equivalence circuit
34	TEST	
2	AIN1P	
35	AIN2P	
47	ERRB/ AIN3P	

I/O Equivalence Circuits - Continued

Pin No.	Pin name	Equivalence circuit
1 36	AIN1N AIN2N	
48	AIN3N	
45 37 44	AOUT1 AOUT2 AOUT3	

Typical Performance Curves

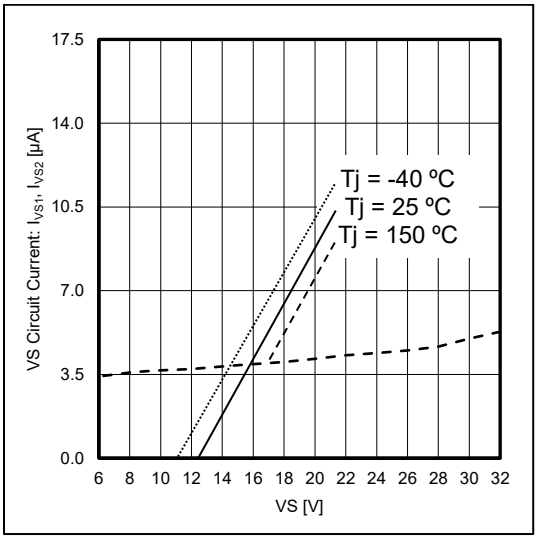


Figure 27. VS Circuit Current 1,2 vs VS

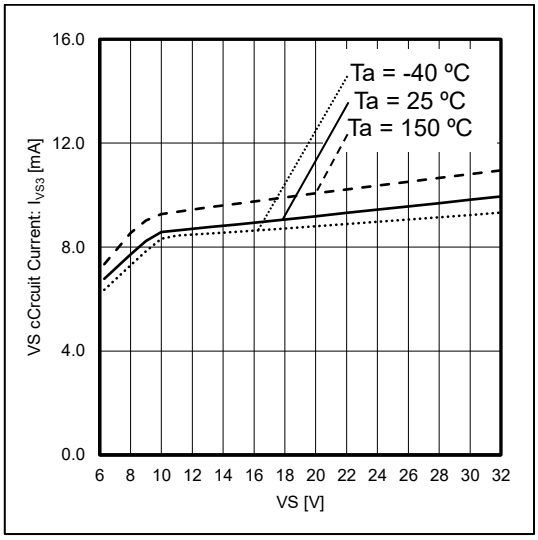


Figure 28. VS Circuit Current 3 vs VS

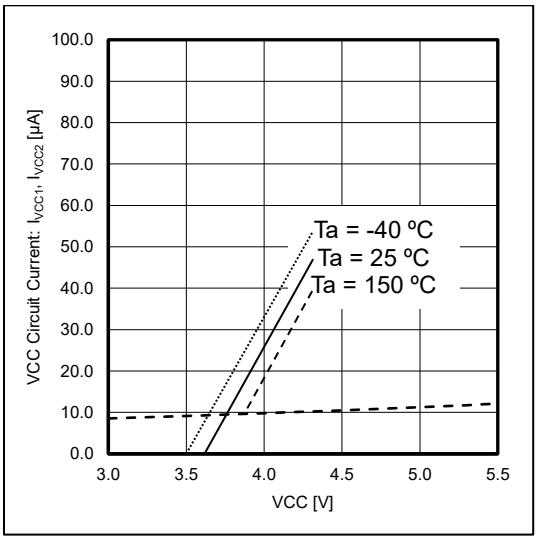


Figure 29. VCC Circuit Current 1,2 vs VCC

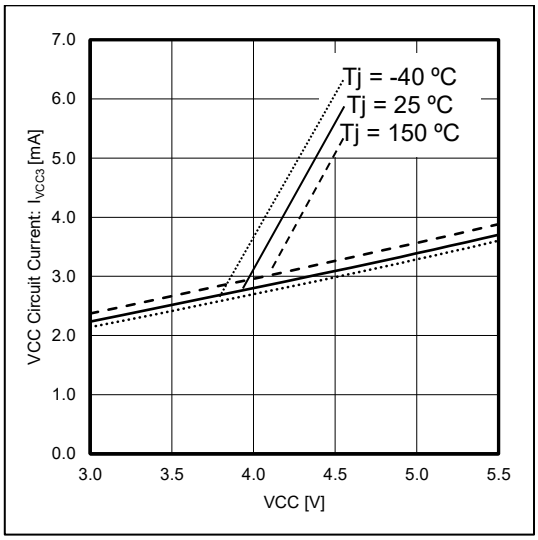


Figure 30. VCC Circuit Current 3 vs VCC

Typical Performance Curves - Continued

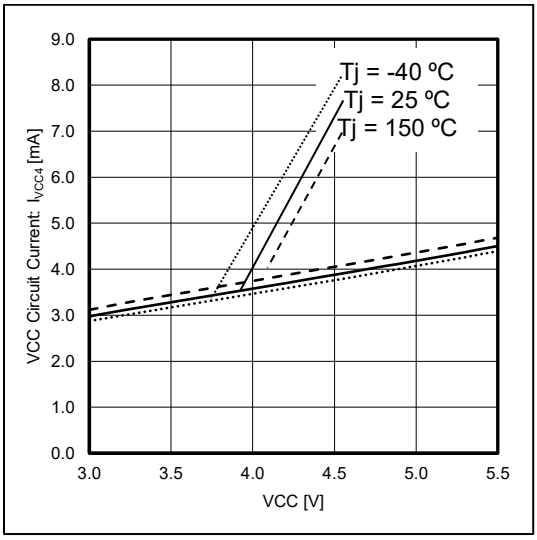


Figure 31. VCC Circuit Current 4 vs VCC

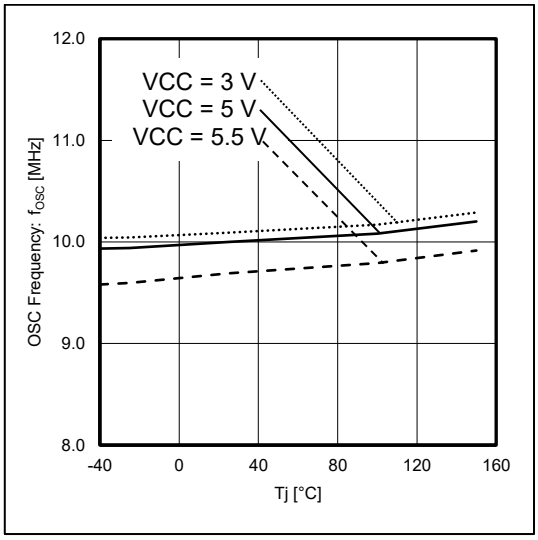


Figure 32. OSC Frequency vs Temperature

Typical Performance Curves - Continued

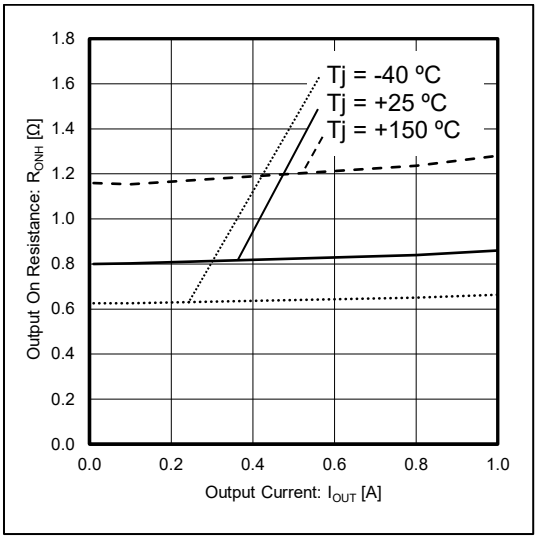


Figure 33. Output On Resistance vs Output Current (High Side, VS = 12 V)

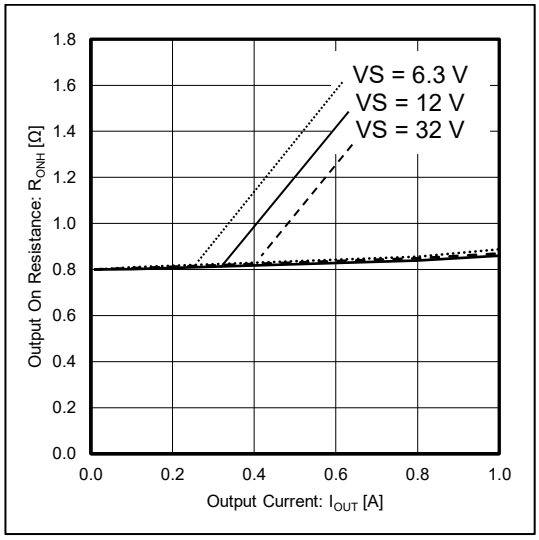


Figure 34. Output On Resistance vs Output Current (High Side, Ta = 25 ºC)

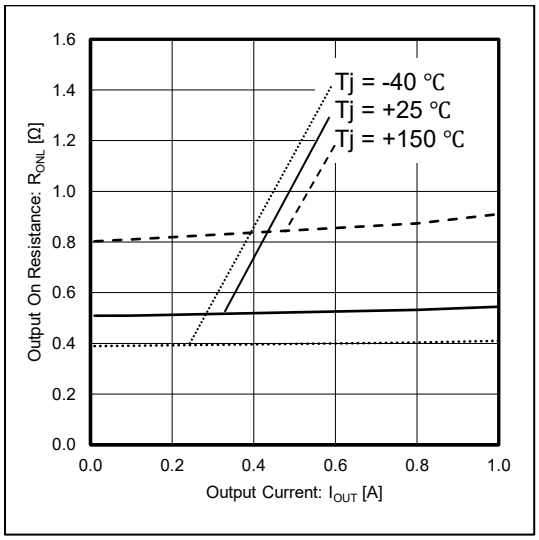


Figure 35. Output On Resistance vs Output Current (Low Side, VS = 12 V)

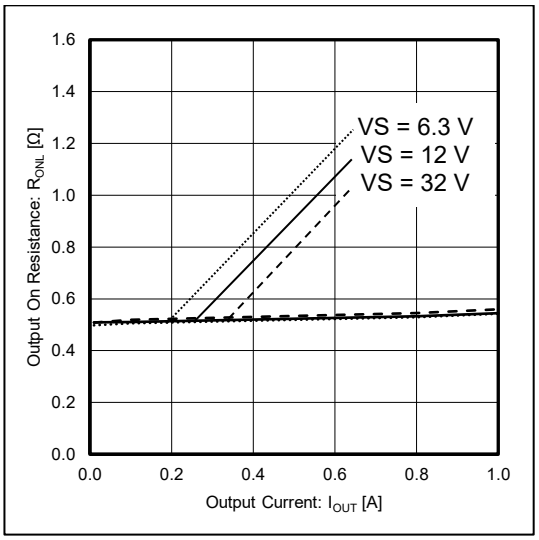


Figure 36. Output On Resistance vs Output Current (Low Side, Ta = 25 ºC)

Typical Performance Curves - Continued

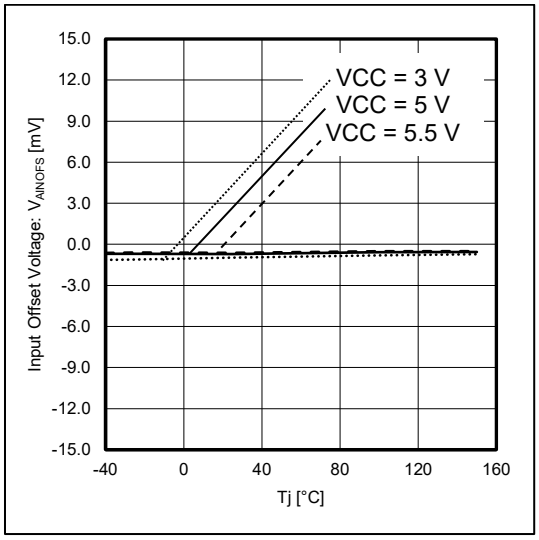


Figure 37. Input Offset Voltage vs Temperature (CS1_GAIN_SEL [1:0] = 0h)

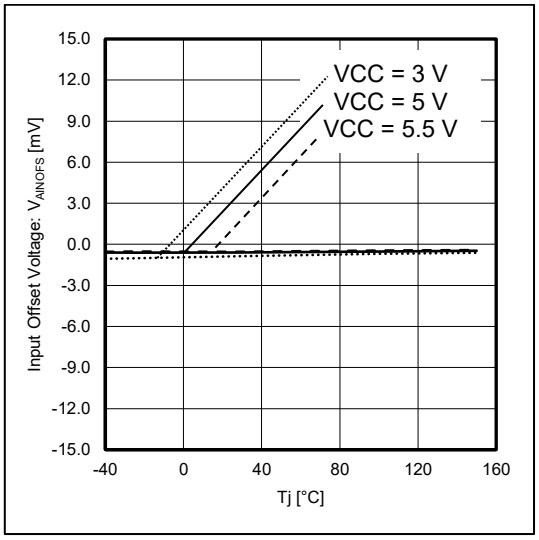


Figure 38. Input Offset Voltage vs Temperature (CS1_GAIN_SEL [1:0] = 1h)

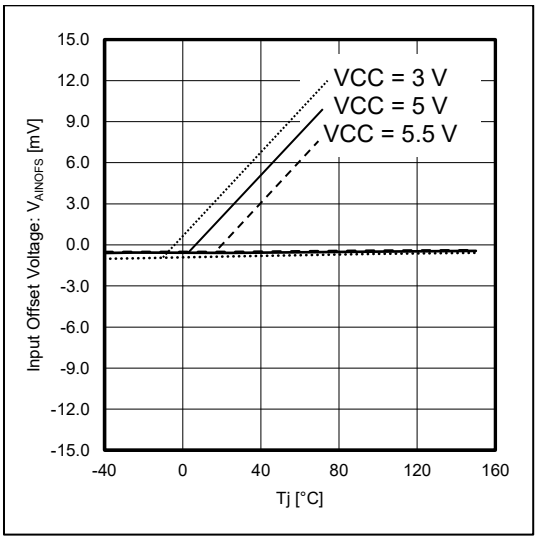


Figure 39. Input Offset Voltage vs Temperature (CS1_GAIN_SEL [1:0] = 2h)

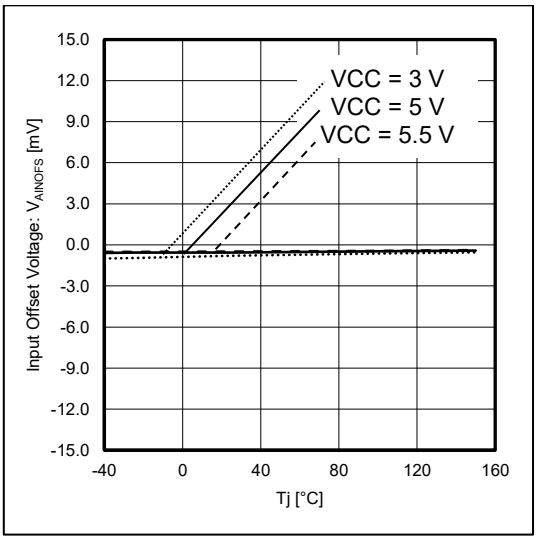


Figure 40. Input Offset Voltage vs Temperature (CS1_GAIN_SEL [1:0] = 3h)

Typical Performance Curves - Continued

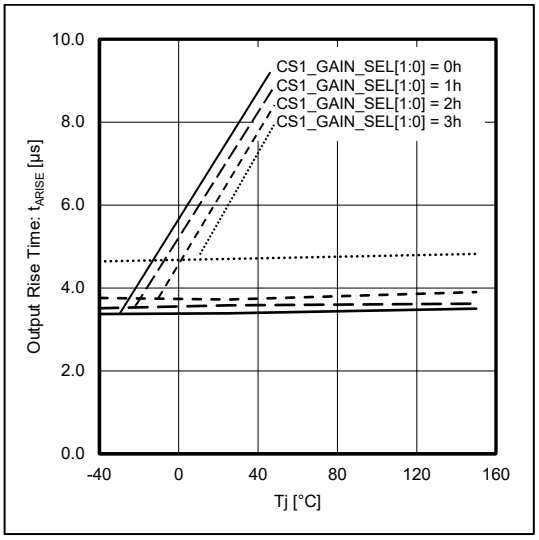


Figure 41. Output Rise Time vs Temperature
(VS = 12 V, VCC = 5 V)

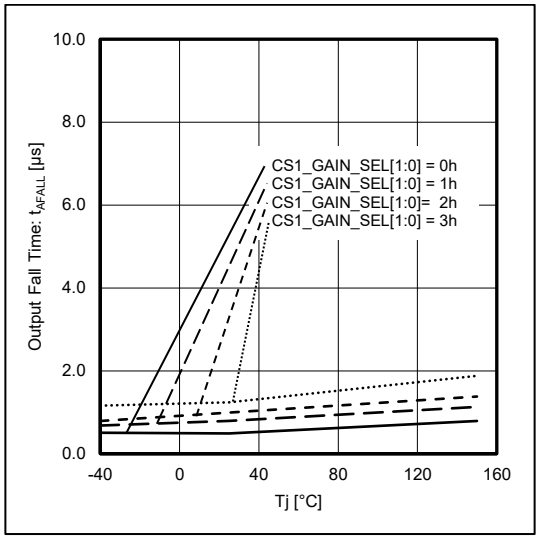


Figure 42. Output Fall Time vs Temperature
(VS = 12 V, VCC = 5 V)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

Operational Notes - Continued

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

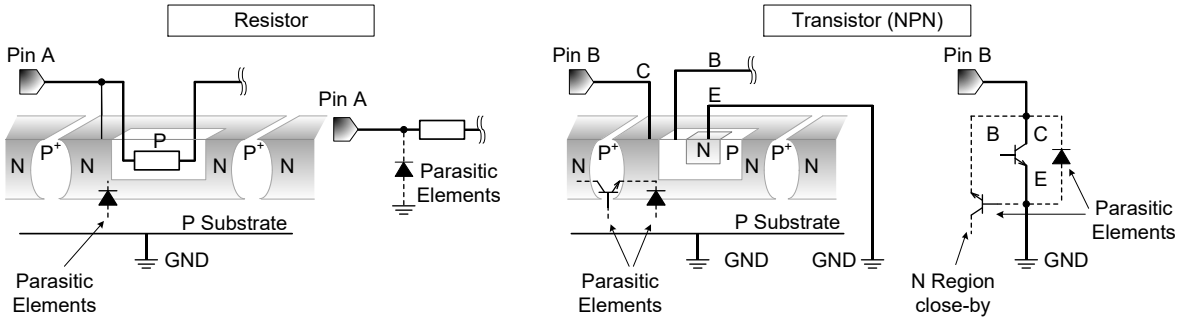


Figure 43. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins.
This IC supports two configurations, Retry Mode and Latch Mode.
When configured in Retry Mode, when the Tj falls below the TSD threshold, the outputs are automatically restored to normal operation.
When configured in Latch Mode, the TSD circuit keeps the outputs in the OFF state even if the Tj falls below the TSD threshold. The IC should be powered down and turned ON again to resume normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Operational Notes - Continued

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

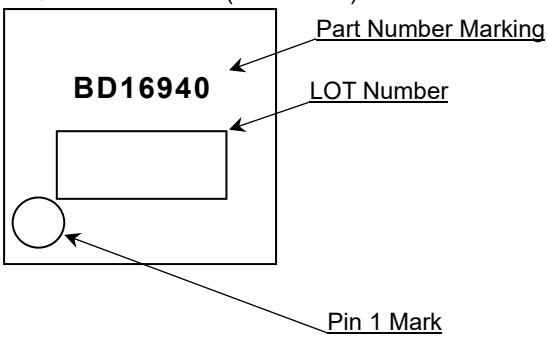
B	D	1	6	9	4	0	M	U	F	-	C E 2

package
MUF: VQFN48FBV070

Product Rank
C: Automotive Rank Products
Packaging & Forming Specifications
E2: Reel Embossed Taping

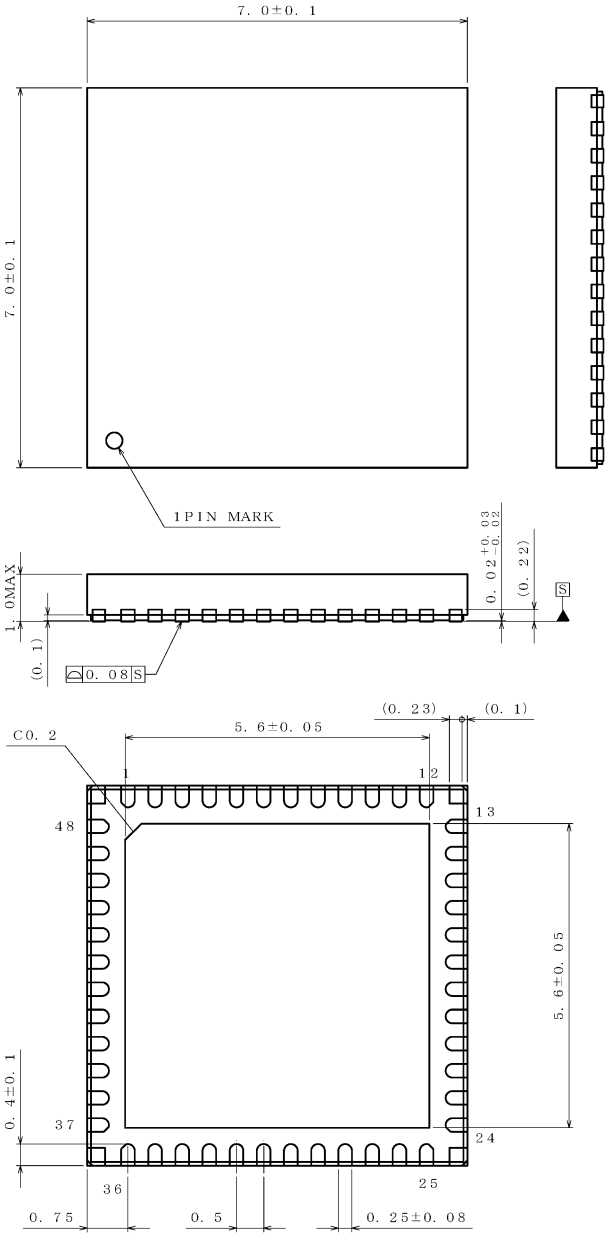
Marking Diagram

VQFN48FBV070 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN48FBV070



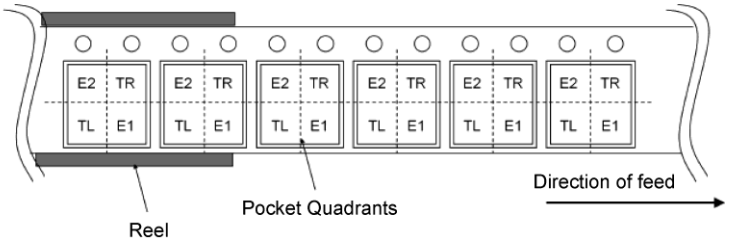
(UNIT:mm)

NOTE: Dimensions in ( ) for reference only.

PKG:VQFN48FBV070
Drawing No. EX414-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Edition	Contents
13.Mar.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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