

Automotive Motor Driver Series

2ch Half-bridge Gate Driver with 2 Built-in Current Detection Amplifiers Circuits for Automotive Applications

BD16953MUF-C

General Description

BD16953MUF-C is a half-bridge gate driver that drives external NMOS FET. The gate driver outputs are controlled by a serial communication interface and a PWM input. For error detection, detailed error results can be read out via SPI. Two built-in current detection amplifiers enable constant monitoring of the load current of each half-bridge.

Features

- AEC-Q100 Qualified (Note 1)
- Function Safety Supportive Automotive Products
- 2ch Half-bridge Gate Drivers
- Single Stage Boost Charge Pump
- Constant Current Gate Drive Output
- 16 Bit Serial Peripheral Interface (SPI)
- 2 Input PWM Control
- Enable Input
- Forced Short Brake Input
- Equipped with Current Detection Amplifier (2ch)
- Error Detection/Protection
(Overvoltage, Overcurrent, Thermal, Undervoltage)
- Static Open/Short Detection Function
- Error Output
(Note 1) Grade 1

Applications

- Automotive Brushed DC Motor
- Automotive Solenoid, Relay Switch
- Wiper, Power Window, Door Lock
- Power Seat (Slide, Reclining, Lifter)
- Power Sliding Door, Auto Closer, Power Lift Gate
- Sunroof
- Seat Belt Height Adjuster, Electric Pretensioner
- Electric Tilt Steering, Telescopic
- Electric Steering Lock
- Electric Shades, Electric Spoilers
etc.

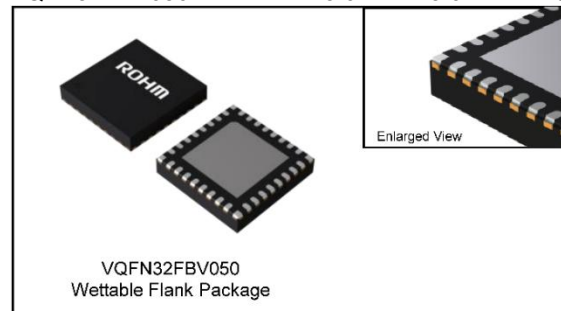
Key Specifications

- Operating Power Supply Range (VB) : 5.5 V to 30 V
- Operating Power Supply Range (VCC) : 3.0 V to 5.5 V
- Power Supply Standby Current (VB) : 0 μ A (Typ)
- Power Supply Standby Current (VCC) : 0 μ A (Typ)
- Gate Driver Output Voltage (High) : $V_B + 10.8$ V (Typ)
- Gate Driver Output Voltage (Low) : 10.3 V (Typ)
- Gate Driver Current Settings: ± 1.5 mA to ± 30 mA (Typ)
- Shoot-through Prevention Dead Time Setting:
0 μ s to 96 μ s (Typ)
- SPI Clock Frequency: 7 MHz (Max)
- Junction Temperature: -40 °C to +150 °C

Package

VQFN32FBV050

W (Typ) x D (Typ) x H (Max)
5.0 mm x 5.0 mm x 1.0 mm



Typical Application Circuit

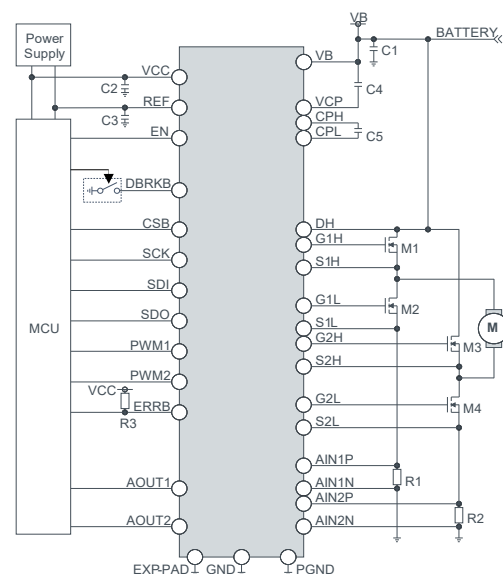


Figure 1. Typical Application Circuit

○Product structure: Silicon integrated circuit ○This product has no designated protection against radioactive rays.

Pin Configuration

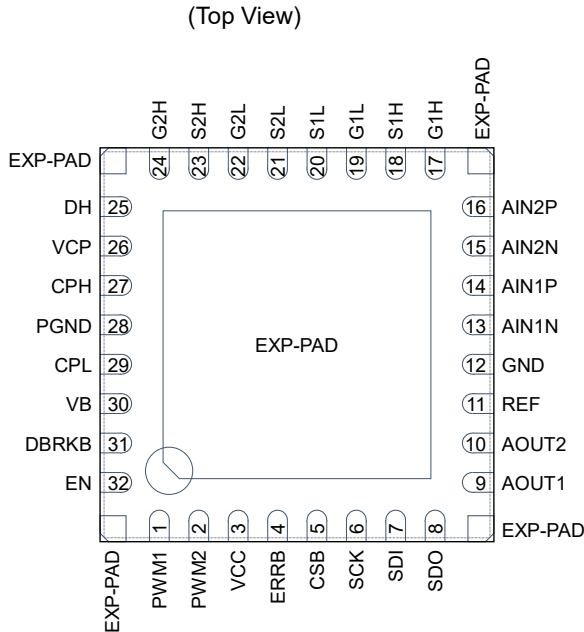


Figure 2. Pin Configuration

Block Diagram

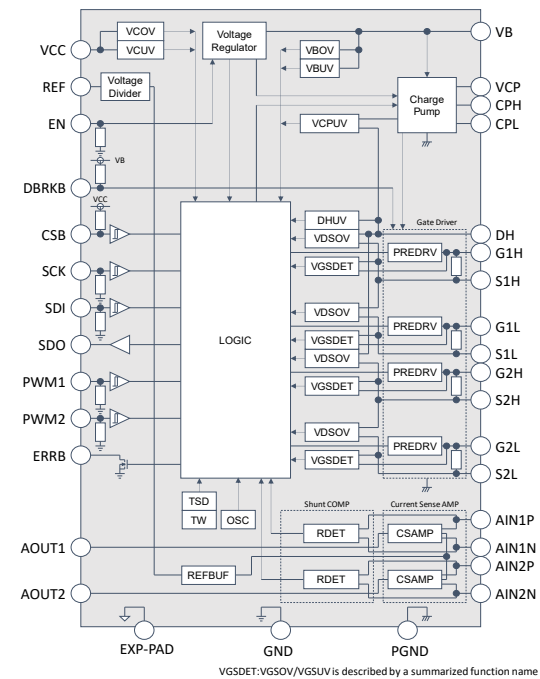


Figure 3. Block Diagram

Pin Descriptions

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PWM1	PWM input for half-bridge 1 control	17	G1H	Half-bridge 1 high-side gate driver output
2	PWM2	PWM input for half-bridge 2 control	18	S1H	Half-bridge 1 high-side source / low-side drain voltage detection input
3	VCC	3.3 V or 5 V power supply voltage input	19	G1L	Half-bridge 1 low-side gate driver output
4	ERRB	Error output (Low Active)	20	S1L	Half-bridge 1 low-side source voltage detection input
5	CSB	SPI chip select input (Low Active)	21	S2L	Half-bridge 2 low-side source voltage detection input
6	SCK	SPI clock input	22	G2L	Half-bridge 2 low-side gate driver output
7	SDI	SPI data input	23	S2H	Half-bridge 2 high-side source / low-side drain voltage detection input
8	SDO	SPI data output	24	G2H	Half-bridge 2 high-side gate driver output
9	AOUT1	Current detection amplifier 1 output	25	DH	Half-bridge 1, 2 common high-side drain voltage detection input
10	AOUT2	Current detection amplifier 2 output	26	VCP	Step-up voltage output
11	REF	Current detection amplifier 1 and 2 common reference voltage input	27	CPH	Boost capacitor connection positive input
12	GND	Small-signal ground input	28	PGND	Power ground input
13	AIN1N	Current detection amplifier 1 inverting input	29	CPL	Boost capacitor connection negative input
14	AIN1P	Current detection amplifier 1 non-inverting input	30	VB	Power supply voltage input
15	AIN2N	Current detection amplifier 2 inverting input	31	DBRKB	Forced short brake input (Low Active)
16	AIN2P	Current detection amplifier 2 non-inverting input	32	EN	Enable input (High Active)
-	EXP-PAD	The center EXP-PAD needs to be short-circuited to GND pins outside IC. The center EXP-PAD and corner EXP-PAD are short-circuited inside IC.			

Application Examples

Applied Schematic (e.g. Brushed DC Motor Drive)

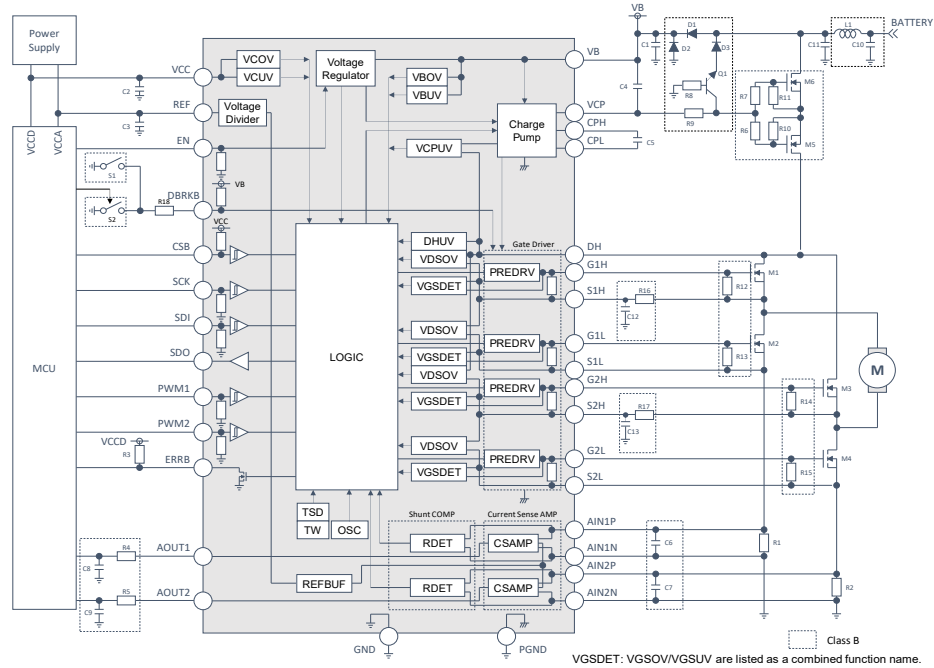


Figure 4. Application Circuit

Selection of Components Externally Connected

No.	Symbol	Function	Recommended value	Unit	Class (Note 1)
1	C1	Decoupling bypass capacitor	1.0 or higher	μF	A
2	C2, C3	Decoupling bypass capacitor	0.1	μF	A
3	C4	Step-up voltage smoothing capacitor	0.1	μF	A
4	C5	Flying capacitor for step-up voltage generation	0.1	μF	A
5	C6, C7	Differential input stabilizing capacitor	—	—	B
6	C8, C9	Part of the output voltage smoothing low-pass filter.	—	—	B
7	C10	Part of a π-type CLC filter for battery voltage smoothing.	—	—	B
8	C11	Capacitor for battery voltage smoothing	10 or higher	μF	A
9	C12, C13	Part of a MOS FET source voltage smoothing low-pass filter.	—	—	B
10	D1	Schottky barrier diode for battery reverse connection protection	—	—	B
11	D2	Zener diode for battery voltage clamp	—	—	B
12	D3	Reverse current prevention diode	—	—	B
13	L1	Part of a π-type CLC filter for battery voltage smoothing. Use inductor such as ferrite bead.	—	—	B
14	M1, M2, M3, M4	NMOS FET for motor drive	—	—	A
15	M5	NMOS FET for battery reverse connection protection	—	—	B
16	M6	NMOS FET for battery power relays	—	—	B
17	R1, R2	Shunt resistors for motor drive current detection	—	—	A
18	R3	Power supply pull-up resistor	10	kΩ	A
19	R4, R5	Part of the output voltage smoothing low-pass filter.	—	—	B
20	R6, R7, R8, R9	Current limiting resistor	—	—	B
21	R10, R11, R12, R13, R14, R15	NMOS FET gate-source pull-down resistors	—	—	B
22	R16, R17	Part of a MOS FET source voltage smoothing low-pass filter	—	—	B
23	R18	Current limiting resistor when DBRKB is set	—	—	B
24	Q1	Reverse battery protection switch	—	—	B
25	S1, S2	Switches such as NMOS FET (signal input control from other systems or MCU signal input control)	—	—	B

(Note 1) Class A: Components required for gate drivers, Class B: Components required for system consideration

Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Power Supply Voltage	VB	V_B	-0.3 to +40	V
	VCC	V_{CC}	-0.3 to +7	V
Input Voltage	REF	V_{REF}	-0.3 to +7	V
	DBRKB	V_{DBRKB}	-0.3 to +40	V
	EN, CSB, SCK, SDI, PWM1, PWM2	$V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}, V_{PWM1}, V_{PWM2}$	-0.3 to +7	V
	DH	V_{DH}	-0.3 to +40	V
	S1H, S2H	V_{S1H}, V_{S2H}	-5 to +40	V
	S1L, S2L	V_{S1L}, V_{S2L}	-2 to +2	V
	AIN1P, AIN1N, AIN2P, AIN2N	$V_{AIN1P}, V_{AIN1N}, V_{AIN2P}, V_{AIN2N}$	-5 to +7	V
Output Voltage	VCP, CPH	V_{CP}, V_{CPH}	$V_B - 0.3$ to $V_B + 20$	V
	CPL	V_{CPL}	-0.3 to $+12.3 < V_B$	V
	SDO	V_{SDO}	-0.3 to +7	V
	ERRB	V_{ERRB}	-0.3 to +7	V
	G1H, G2H	V_{G1H}, V_{G2H}	-0.3 to +60 ($V_{GXH} - V_{SXH} < 12$ V)	V
	G1L, G2L	V_{G1L}, V_{G2L}	-0.3 to +12.3	V
	AOUT1, AOUT2	V_{AOUT1}, V_{AOUT2}	-0.3 to +7	V
Output Current (Note 1)	SDO	I_{SDO}	-1 to +1	mA
	ERRB	I_{ERRB}	0 to +1	mA
	AOUT1, AOUT2	I_{AOUT1}, I_{AOUT2}	-5 to +5	mA
Storage Temperature Range		T_{stg}	-55 to +150	°C
Maximum Junction Temperature		T_{jmax}	+150	°C

(Note 1) For current items, the current inflow to the IC is described as positive and the current outflow from the IC is described as negative.

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Conditions

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Operating Temperature	T_{opr}	-40	+25	+125	°C
VB Power Supply Voltage	V_B	5.5	13.5	30.0	V
VCC Power Supply Voltage	V_{CC}	3.0	5.0	5.5	V
REF Input Voltage	V_{REF}	3.0	5.0	5.5	V
EN, CSB, SCK, SDI, PWM1, PWM2 Input Voltage	$V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}, V_{PWM1}, V_{PWM2}$	3.0	—	V_{CC}	V

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <i>(Note 3)</i>	2s2p <i>(Note 4)</i>	
VQFN32FBV050				
Junction to Ambient	θ_{JA}	103.0	39.3	°C/W
Junction to Top Characterization Parameter <i>(Note 2)</i>	Ψ_{JT}	14.0	13.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mm	1.20 mm	Φ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$, $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Overall						
VB Circuit Current 1 <i>(Note 1)</i>	I _{VB1}	—	0	10	μA	EN = GND -40 °C ≤ T _J ≤ +105 °C
VB Circuit Current 2	I _{VB2}	—	0	50	μA	EN = GND +105 °C < T _J ≤ +150 °C
VB Circuit Current 3	I _{VB3}	—	3.4	5.9	mA	Register = Initial Value
VB Circuit Current 4	I _{VB4}	—	9.8	17.2	mA	CP_EN = CS_EN = 1 DRV_GHIZ = 0 VBOV_SEL = 1
VB Circuit Current 5	I _{VB5}	140	233	410	μA	VB = 13.5 V EN = DBRKB = GND
VCC Circuit Current 1 <i>(Note 1)</i>	I _{VCC1}	—	0	10	μA	EN = GND -40 °C ≤ T _J ≤ +105 °C
VCC Circuit Current 2	I _{VCC2}	—	2	100	μA	EN = GND +105 °C < T _J ≤ +150 °C
VCC Circuit Current 3	I _{VCC3}	—	2.8	5.6	mA	CP_EN = CS_EN = 1 DRV_GHIZ = 0
Current Sense Amplifier 1 and 2 Common Reference Voltage Input (REF)						
High Level Input Current 1 <i>(Note 1)</i>	I _{REFH1}	—	0	10	μA	EN = GND -40 °C ≤ T _J ≤ +105 °C
High Level Input Current 2	I _{REFH2}	—	0	100	μA	EN = GND +105 °C < T _J ≤ +150 °C
High Level Input Current 3	I _{REFH3}	—	40	180	μA	
Low Level Input Current	I _{REFL}	-1	0	-	μA	REF = GND
Current Sense Amplifier 1 and 2 Common Reference Voltage Generation Amplifier (REFBUF)						
Reference Voltage Generation Amplifier Output Voltage 1	V _{REF1}	V _{REF} /2 - 0.025	V _{REF} /2	V _{REF} /2 + 0.025	V	A _{INxP} = A _{INxN} = GND CSAMP_REF = 0 (x = 1, 2)
Reference Voltage Generation Amplifier Output Voltage 2	V _{REF2}	V _{REF} /8 - 0.025	V _{REF} /8	V _{REF} /8 + 0.025	V	A _{INxP} = A _{INxN} = GND CSAMP_REF = 1 (x = 1, 2)
Short Brake Input (DBRKB)						
High Level Input Voltage	V _{DBRKBH}	V _B - 0.8	—	V _B	V	
Low Level Input Voltage	V _{DBRKB L}	0	—	V _B - 2.2	V	
High Level Input Current	I _{DBRKBH}	—	0	1	μA	DBRKB = VB
Low Level Input Current	I _{DBRKB L}	-0.81	-0.10	-0.02	mA	DBRKB = GND

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.
(Note 1) This is a design guarantee item and is not subject to inspection at the time of shipment.

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$, $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Enable Input (EN), SPI Input (CSB, SCK, SDI), and PWM Input (PWM1, PWM2)						
High Level Input Voltage	V _{INH}	V _{CC} x 0.7	–	V _{CC}	V	
Low Level Input Voltage	V _{INL}	0	–	V _{CC} x 0.3	V	
Input Hysteresis Voltage	V _{INHYS}	–	V _{CC} x 0.1	–	V	
High Level Input Current (EN, SCK, SDI, PWM1, PWM2)	I _{INH}	25	50	100	µA	V _{CC} = 5 V EN, SCK, SDI, PWM1, PWM2 = V _{CC}
Low Level Input Current (EN, SCK, SDI, PWM1, PWM2)	I _{INL}	-1	0	–	µA	EN, SCK, SDI, PWM1, PWM2 = GND
High Level Input Current (CSB)	I _{CSBH}	–	0	1	µA	CSB = V _{CC}
Low Level Input Current (CSB)	I _{CSBL}	-100	-50	-25	µA	V _{CC} = 5 V CSB = GND
PWM Input Frequency (PWM1, PWM2)	f _{PWM}	–	–	25	kHz	
SPI Output (SDO)						
High Level Output Voltage	V _{SDOH}	V _{CC} x 0.8	–	V _{CC}	V	I _{SDO} = -1 mA
Low Level Output Voltage	V _{SDOL}	0	–	V _{CC} x 0.2	V	I _{SDO} = +1 mA
High Level Output Leakage Current	I _{SDOH}	–	0	10	µA	SDO = V _{CC} (SDO Output is Hi-Z)
Low Level Output Leakage Current	I _{SDOL}	-10	0	–	µA	SDO = GND (SDO Output is Hi-Z)
Error Output (ERRB)						
Low Level Output Voltage	V _{ERRB}	0	–	0.4	V	I _{ERRB} = +1 mA
High Level Output Leakage Current	I _{ERRBH}	–	0	10	µA	ERRB = V _{CC} (ERRB Output is Hi-Z)
Internal Oscillator						
Oscillation Frequency	f _{OSC}	9	10	11	MHz	

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$,
 $\text{REF} = \text{EN} = \text{VCC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Charge Pump Voltage Output (VCP)						
VCP Circuit Current 1 <i>(Note 1)</i>	I _{VCP1}	—	0	10	μA	EN = GND VCP = VB -40 °C ≤ T _j ≤ +105 °C
VCP Circuit Current 2	I _{VCP2}	—	0	50	μA	EN = GND VCP = VB +105 °C < T _j ≤ +150 °C
Output Voltage 1	V _{CP1}	V _B + 10.0	V _B + 10.8	V _B + 12.5	V	VB = 13.5 V, 30 V, I _{VCP} = 0 mA
Output Voltage 2	V _{CP2}	V _B + 5.5	V _B + 6.0	V _B + 6.5	V	VB = 6 V, I _{VCP} = 0 mA
Charge Pump Output Drop Voltage 1 <i>(Note 1)</i>	V _{CP_drop1}	—	—	1	V	VB = 13.5 V, 30 V, I _{VCP} = -10 mA
Charge Pump Output Drop Voltage 2 <i>(Note 1)</i>	V _{CP_drop2}	—	—	0.5	V	VB = 6 V, I _{VCP} = -2 mA
Operating Frequency	f _{VCP}	360	400	440	kHz	CHP_FREQ_DFU_EN = 0
High-Side Drain Voltage Detection Input (DH)						
Input Current 1 <i>(Note 1)</i>	I _{DH1}	—	0	1	μA	EN = GND -40 °C ≤ T _j ≤ +105 °C
Input Current 2	I _{DH2}	—	0	10	μA	EN = GND +105 °C < T _j ≤ +150 °C
DH Circuit Input Current	V _{DH}	—	120	250	μA	

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) This is a design guarantee item and is not subject to inspection at the time of shipment.

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$, $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High-Side / Low-Side Source Voltage Inputs (S1H, S2H, S1L, S2L), High-Side / Low-Side Gate Driver Outputs (G1H, G2H, G1L, G2L)						
High-Side Source Input Current 1 (S1H, S2H)	ISxH1	-10	0	–	μA	EN = GND GxH-SxH = GND (x = 1, 2)
High-Side Source Input Current 2 (S1H, S2H) <i>(Note 1)</i>	ISxH2	-1760	-880	-440	μA	VCC = 5 V, VB = 13.5 V SxH = VB CUR_SI_HxSEL = 1 CUR_SI_Hx [2:0] = 7h GxH_SEL = 0, GxH_FIX = 1 (x = 1, 2)
High-Side Source Input Current 3 (S1H, S2H) <i>(Note 1)</i>	ISxH3	-1500	-750	-375	μA	VCC = 5 V, VB = 13.5 V SxH = GND CUR_SI_HxSEL = 1 CUR_SI_Hx [2:0] = 7h GxH_SEL = 0, GxH_FIX = 0 (x = 1, 2)
Low-Side Source Input Current 1 (S1L, S2L)	ISxL1	-10	0	–	μA	EN = GND GxL-SxL = GND (x = 1, 2)
Low-Side Source Input Current 2 (S1L, S2L) <i>(Note 1)</i>	ISxL2	-540	-360	-180	μA	VCC = 5 V, VB = 13.5 V SxH = SxL = GND CUR_SO_LxSEL = 1 CUR_SO_Lx [2:0] = 7h GxL_SEL = 0, GxL_FIX = 1 (x = 1, 2)
High-Side Gate Driver Output High 1	VGxHH1	VB + 10.0	VB + 10.8	VB + 12.0	V	VB = 13.5 V, 30 V, IVCP = 0 mA S1H = S2H = VB
High-Side Gate Driver Output High 2	VGxHH2	VB + 4.5	VB + 5.5	VB + 6.5	V	VB = 5.5 V, IVCP = 0 mA S1H = S2H = VB
Low-Side Gate Driver Output High 1	VGxLH1	9.3	10.3	11.3	V	VB = 13.5 V, 30 V
Low-Side Gate Driver Output High 2	VGxLH2	4	5	6	V	VB = 5.5 V
High-Side / Low-Side Gate Driver Output Source Current Setting Accuracy 1	AISR1	-30	–	+30	%	VB = 13.5 V, 30 V VCP = VB + 10.8 V High-Side: GxH = SxH = VB Low-Side: GxL = SxL = GND (x = 1, 2)
High-Side / Low-Side Gate Driver Output Source Current Setting Accuracy 2	AISR2	-30	–	+30	%	VB = 6.0 V, VCP = 12 V High-Side: GxH = SxH = VB Low-Side: GxL = SxL = GND (x = 1, 2)

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) Reference value specification for external flow to S_{xH} and S_{xL} pins when $V_B = 13.5\text{ V}$. ($x = 1, 2$)

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$, $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High-Side / Low-Side Source Voltage Inputs (S1H, S2H, S1L, S2L), High-Side / Low-Side Gate Driver Outputs (G1H, G2H, G1L, G2L)						
High-Side / Low-Side Gate Driver Output Sink Current Setting Accuracy 1 ^(Note 1)	A _{IS11}	-35	—	+35	%	VB = 13.5 V, 30 V VCP = VB + 10.8 V High-Side: GxH = SxH + 10.8 V Low-Side: GxL = SxL = GND (x = 1, 2) CP_EN = 0
High-Side / Low-Side Gate Driver Output Sink Current Setting Accuracy 2 ^(Note 1)	A _{IS12}	-35	—	+35	%	VB = 6.0 V, VCP = 12 V High-Side: GxH = SxH + 6.0 V Low-Side: GxL = SxL + 6.0 V (x = 1, 2) CP_EN = 0
High-Side / Low-Side Gate to Source Pull-down Resistance ^(Note 2)	R _{GSxHL}	80	160	260	kΩ	GxH-SxH = 2 V GxL-SxL = 2 V DRV_GHIZ = 1 (x = 1, 2)
Simultaneous ON Prevention Setting Error Time ^(Note 6)	t _{DEAD_err}	—	—	0.25	μs	
Synchronization Delay Time ^(Note 3)	t _{syn}	—	—	1.25	μs	
Propagation Delay Time 1 ^(Note 4)	t _{poropa1}	—	—	400	ns	SxH = VB Output Current Settings1 to 4 = All High (Initial Value)
Propagation Delay Time 2 ^(Note 5)	t _{poropa2}	—	—	2	μs	SxH = VB Output Current Settings1 to 4 = All High (Initial Value)
High-Side / Low-Side Gate to Sink Drive Output On-Resistance at Full-On	R _{GON_ds}	—	50	100	Ω	

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) High-side sink current: I_{sink} ($G1H = G2H = 11\text{ V}$, $S1H = S2H = \text{PGND}$) - Pull-down Current.

Low-side sink current: I_{sink} ($G1L = G2L = 11\text{ V}$, $S1L = S2L = \text{PGND}$) - Pull-down Current.

(Note 2) Gate driver output current = Gate driver output setting current - Gate to Source pull-down current

Ex.) Gate drive output setting current: 10 mA, the gate drive output current is 10 mA (Typ) - $13\text{ }\mu\text{A} = 9.987\text{ mA}$

(Note 3) The synchronization delay time between the PWM input signal and the LOGIC circuit.

This is a design guarantee item and is not subject to inspection at the time of shipment.

(Note 4) Internal delay time between high-side / low-side logic control signals and G_{xH}/G_{xL} output signals.

This is a design guarantee item and is not subject to inspection at the time of shipment.

(Note 5) ($G_{xH}\text{-}S_{xH}$) / ($G_{xL}\text{-}S_{xL}$) Internal delay between voltage sense signal and high-side / low-side logic signal.

This is a design guarantee item and is not subject to inspection at the time of shipment.

(Note 6) Time Delay from high-side / low-side Logic Control Signals to G_{xH} and G_{xL} Outputs.

This is a design guarantee item and is not subject to inspection at the time of shipment.

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$, $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Current Sense Amplifier (AIN1P, AIN1N, AIN2P, AIN2N, AOUT1, AOUT2)						
Input Current AINxP <i>(Note 1)</i>	I _{AINxP}	-16.8	-10.0	-5.8	μA	REF = GND (x = 1, 2)
Input Current AINxN <i>(Note 1)</i>	I _{AINxN}	-20.2	-12.0	-7.0	μA	REF = GND, RDET _x [2:0] = 7h (x = 1, 2)
Input Offset Voltage	V _{AINOFS}	-1	0	+1	mV	T _j = 25 °C, AINxP = AINxN = GND (x = 1, 2) V _{AINOFS} = (V _{AOx} - V _{REF1}) / G _{AIOy} (y = 1 to 4)
Input Offset Voltage Temperature Drift <i>(Note 2)</i>	V _{AINDRFT}	-15	0	+15	μV / °C	V _{AINxP} = V _{AINxN} = GND (x = 1, 2)
Common Mode Input Voltage Range	V _{AINCMN}	-0.3	–	+2.5	V	
Output Voltage Range 1	V _{AO1}	0.3	–	4.4	V	REF = 5.0 V
Output Voltage Range 2	V _{AO2}	0.3	–	2.7	V	REF = 3.3 V
Output Clamp Voltage	V _{CLP}	2.8	3.2	3.6	V	REF = 3.3 V
Input/Output Gain 1	G _{AIO1}	–	8	–	V/V	CSAMP_GAIN [1:0] = 0h
Input/Output Gain 2	G _{AIO2}	–	16	–	V/V	CSAMP_GAIN [1:0] = 1h
Input/Output Gain 3	G _{AIO3}	–	32	–	V/V	CSAMP_GAIN [1:0] = 2h
Input/Output Gain 4	G _{AIO4}	–	48	–	V/V	CSAMP_GAIN [1:0] = 3h
Input/Output Gain Precision	A _{GAIO_err}	–2	–	+2	%	
Common Mode Rejection Ratio 1 <i>(Note 2)</i>	CMRR _{DC1}	60	–	–	dB	Common Mode Ripple < 100 Hz CSAMP_GAIN [1:0] = 0h
Common Mode Rejection Ratio 2 <i>(Note 2)</i>	CMRR _{DC2}	67	–	–	dB	Common Mode Ripple < 100 Hz CSAMP_GAIN [1:0] = 1h
Common Mode Rejection Ratio 3 <i>(Note 2)</i>	CMRR _{DC3}	72	–	–	dB	Common Mode Ripple < 100 Hz CSAMP_GAIN [1:0] = 2h
Common Mode Rejection Ratio 4 <i>(Note 2)</i>	CMRR _{DC4}	75	–	–	dB	Common Mode Ripple < 100 Hz CSAMP_GAIN [1:0] = 3h
Common Mode Rejection Ratio 5 <i>(Note 2)</i>	CMRR _{20k1}	55	–	–	dB	Common Mode Ripple = 20 kHz CSAMP_GAIN [1:0] = 0h
Common Mode Rejection Ratio 6 <i>(Note 2)</i>	CMRR _{20k2}	64	–	–	dB	Common Mode Ripple = 20 kHz CSAMP_GAIN [1:0] = 1h
Common Mode Rejection Ratio 7 <i>(Note 2)</i>	CMRR _{20k3}	72	–	–	dB	Common Mode Ripple = 20 kHz CSAMP_GAIN [1:0] = 2h
Common Mode Rejection Ratio 8 <i>(Note 2)</i>	CMRR _{20k4}	75	–	–	dB	Common Mode Ripple = 20 kHz CSAMP_GAIN [1:0] = 3h
Power Supply Rejection Ratio 1 <i>(Note 2)</i>	PSRR _{DC1}	75	–	–	dB	Power Supply Ripple < 100 Hz 7 V ≤ V _B ≤ 30 V
Power Supply Rejection Ratio 2 <i>(Note 2)</i>	PSRR _{DC2}	50	–	–	dB	Power Supply Ripple < 100 Hz V _B = 5.5 V
Power Supply Rejection Ratio 3 <i>(Note 2)</i>	PSRR _{20k1}	70	–	–	dB	Power Supply Ripple = 20 kHz 7 V ≤ V _B ≤ 30 V
Power Supply Rejection Ratio 4 <i>(Note 2)</i>	PSRR _{20k2}	25	–	–	dB	Power Supply Ripple = 20 kHz V _B = 5.5 V
Output Rise Time	t _{ARISE}	–	–	2	μs	AINxP = -2 V/G _{AIOy} to +2 V/G _{AIOy} (y = 1 to 4) AINxN = 0 V, CSAMP_REF = 0 C _{AOUTx} = 25 pF load (x = 1, 2)
Output Fall Time	t _{AFALL}	–	–	2	μs	AINxP = +2 V/G _{AIOy} to -2 V/G _{AIOy} (y = 1 to 4) AINxN = 0 V, CSAMP_REF = 0 C _{AOUTx} = 25 pF load (x = 1, 2)

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) A bias current flows to detect an open pin.

(Note 2) This is a design guarantee item and is not subject to inspection at the time of shipment.

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $A_{INxP} = A_{INxN} = \text{GND}$,
 $\text{REF} = \text{EN} = V_{CC}$, $S_{xH} = S_{xL} = \text{PGND}$, $V_B\text{-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Error Detection/Protection						
VB Power Supply Undervoltage Protection Release Voltage	V _{BUVR}	4.5	5.0	5.5	V	
VB Power Supply Undervoltage Protection Hysteresis Voltage	V _{BUV_hys}	300	500	700	mV	Detection Voltage: V _{BUVR} - V _{BUV_hys}
VB Power Supply Undervoltage Detection Blanking Time	t _{VBUVBLK}	48	64	80	μs	
VB Power Supply Overvoltage Protection Detection Voltage 1	V _{BOVD1}	20.0	22.0	24.0	V	VBOV_SEL = 0
VB Power Supply Overvoltage Protection Detection Voltage 2	V _{BOVD2}	30.0	32.5	35.0	V	VBOV_SEL = 1
VB Power Supply Overvoltage Protection Hysteresis Voltage	V _{BOV_hys}	0.6	1.0	1.4	V	Release Voltage: V _{BOVD1, 2} - V _{BOV_hys}
VB Power Supply Overvoltage Detection Blanking Time	t _{VBOVBLK}	48	64	80	μs	
VCC Power Supply Undervoltage Protection Release Voltage	V _{CCUVR}	2.55	2.75	2.95	V	
VCC Power Supply Undervoltage Protection Hysteresis Voltage	V _{CCUV_hys}	10	50	100	mV	Detection Voltage: V _{CCUVR} - V _{CCUV_hys}
VCC Power Supply Undervoltage Detection Blanking time <i>(Note 1)</i>	t _{VCCUVBLK}	1.0	2.5	5.0	μs	VCC = 2.2 V to 3.0 V
VCC Power Supply Overvoltage Protection Detection Voltage	V _{CCOVD}	5.5	6.0	6.5	V	
VCC Power Supply Overvoltage Protection Hysteresis Voltage	V _{CCOV_hys}	50	200	400	mV	Release Voltage: V _{CCOVD} - V _{CCOV_hys}
VCC Power Supply Overvoltage Detection Blanking Time	t _{VCCOVBLK}	48	64	80	μs	
VCP Power Supply Undervoltage Protection Release Voltage	V _{CPUVR}	2.6	3.2	3.8	V	V _{CPUVR} : VCP – DH
VCP Power Supply Undervoltage Protection Hysteresis Voltage	V _{CPUV_hys}	50	200	400	mV	Detection Voltage: V _{CPUVR} - V _{CPUV_hys}
VCP Power Supply Undervoltage Detection Blanking Time	t _{VCPUVBLK}	48	64	80	μs	
DH Power Supply Undervoltage Protection Detection Voltage	V _{DHUV}	4.4	4.9	5.4	V	
DH Power Supply Undervoltage Protection Detection Blanking Time Setting Accuracy <i>(Note 1, 2)</i>	A _{tVDHUV}	-10	–	+10	%	

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) This is a design guarantee item and is not subject to inspection at the time of shipment.

(Note 2) This specifies the accuracy of the setting value set in the register. For delay times including analog delays, please refer to the register description of DHUV Blanking Setting. [Address = 1Ch <DHUV Blanking Setting>](#)

Electrical Characteristics - continued

Unless otherwise specified, $-40^{\circ}\text{C} \leq T_j \leq +150^{\circ}\text{C}$, $V_B = 5.5\text{ V}$ to 30 V , $V_{CC} = 3.0\text{ V}$ to 5.5 V , $\text{AINxP} = \text{AINxN} = \text{GND}$,
 $\text{REF} = \text{EN} = \text{VCC}$, $\text{SxH} = \text{SxL} = \text{PGND}$, $\text{VB-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Error Detection/Protection						
High-Side / Low-Side Drain-Source <i>(Note 2)</i> Overvoltage (Overcurrent) Protection Detection Voltage Setting Accuracy 1	A _{VDSOVD1}	-25	–	+25	%	VDS setting: VDS_Hx [2:0] = 0h, 1h VDS_Lx [2:0] = 0h, 1h (x = 1, 2)
High-Side / Low-Side Drain-Source <i>(Note 2)</i> Overvoltage (Overcurrent) Protection Detection Voltage Setting Accuracy 2	A _{VDSOVD2}	-15	–	+15	%	VDS setting: VDS_Hx [2:0] = 2h to 7h VDS_Lx [2:0] = 2h to 7h (x = 1, 2)
High-Side / Low-Side Drain-Source Overvoltage (Overcurrent) Protection Detection Blanking Time Setting Accuracy <i>(Note 3)</i>	A _{tVDSOVD}	-10	–	+10	%	
High-Side / Low-Side Gate-Source Undervoltage Protection Detection Voltage	V _{GSUVD}	2.1	3.0	3.9	V	GxH, GxL = High (x = 1, 2)
High-Side / Low-Side Gate-Source Undervoltage Protection Detection Blanking Time Setting Accuracy <i>(Note 3)</i>	A _{tVGSUVD}	-10	–	+10	%	
High-Side / Low-Side Gate-Source Overvoltage Protection Detection Voltage	V _{GSOVD}	0.4	1.2	2.4	V	GxH, GxL = Low (x = 1, 2)
High-Side / Low-Side Gate-Source Overvoltage Protection Detection Blanking Time Setting Accuracy <i>(Note 3)</i>	A _{tVGSOVD}	-10	–	+10	%	
Shunt Resistors Overvoltage Protection Detection Voltage Accuracy 1 <i>(Note 1)</i>	A _{VROVD1}	-35	–	+35	%	RDET setting: RDET _x [2:0] = 0h, 1h (x = 1, 2)
Shunt Resistors Overvoltage Protection Detection Voltage Accuracy 2 <i>(Note 1)</i>	A _{VROVD2}	-25	–	+25	%	RDET setting: RDET _x [2:0] = 2h to 7h (x = 1, 2)
Shunt Resistors Overvoltage Protection Detection Blanking Time Setting Accuracy <i>(Note 2)</i>	A _{tVROVD}	-10	–	+10	%	
Static open/short Detection Voltage	V _{SxHD_off}	V _{DH} X 0.4	V _{DH} X 0.5	V _{DH} X 0.6	V	S1H, S2H Monitor
Static open/short Detection Pull Down Resistor 1	R _{SxHD_off1}	0.66	1.33	2.66	kΩ	VB < 14 V
Static open/short Detection Pull Down Resistor 2	R _{SxHD_off2}	2.07	4.15	8.30	kΩ	VB < 18 V
Thermal Warning Detection Temperature <i>(Note 3)</i>	T _{TWD}	115	132.5	150	°C	
Thermal Warning Hysteresis Temperature <i>(Note 3)</i>	T _{TW_hys}	–	10	–	°C	Release Temperature: T _{TWD} - T _{TW_hys}
Thermal Protection Detection Temperature <i>(Note 3)</i>	T _{TSDD}	150	175	200	°C	
Thermal Protection Hysteresis Temperature <i>(Note 3)</i>	T _{TSD_hys}	–	15	–	°C	Release Temperature: T _{TSDD} - T _{TSD_hys}

For current values above, current flowing into the IC is indicated as a positive value, and current flowing out of the IC is indicated as a negative value.

(Note 1) Overvoltage detection COMP accuracy for the shunt resistor voltage (AINxP-AINxN [$x = 1, 2$]).

(Note 2) This specifies the accuracy of the setting value set in the register. For delay times including analog delays, please refer to the register description of VDS, VGS RDET Blanking Setting 1 and 2 address 1Ah and 1Bh respectively.

Address = 1Ah <VDS_VGS RDET Blanking Settings1>, Address = 1Bh <VDS_VGS RDET Blanking Settings2>

(Note 3) These are design values for which the performance evaluation was confirmed, and the shipment inspection is not conducted

Electrical Characteristics - continued

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_B = 5.5\text{ V to }30\text{ V}$, $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $\text{AINxP} = \text{AINxN} = \text{GND}$, $\text{REF} = \text{EN} = \text{VCC}$, $\text{SxH} = \text{SxL} = \text{PGND}$, $\text{VB-VCP} = 0.1\text{ }\mu\text{F}$, $\text{CPH-CPL} = 0.1\text{ }\mu\text{F}$ ($x = 1, 2$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
SPI I/O (CSB, SCK, SDI, SDO)						
SCK Frequency	f _{SCK}	—	—	7.0	MHz	
SCK Period	t _{SCK}	142	—	-	ns	
SCK High Time	t _{SCKH}	65	—	-	ns	
SCK Low Time	t _{SCKL}	65	—	-	ns	
SCK Setup Time	t _{SCKSET}	125	—	-	ns	
SCK Hold Time	t _{SCKHLD}	125			ns	
CSB Setup Time	t _{CSBSET}	142	—	—	ns	
CSB Hold Time	t _{CSBHLD}	142	—	—	ns	
CSB High Time	t _{CSBH}	2	—	—	μs	
SDI Setup Time	t _{SDISET}	50	—	—	ns	
SDI Hold Time	t _{SDIHLD}	50	—	—	ns	
SDO Valid Time	t _{SDOV}	—	—	60	ns	No Load
SDO Enable after CSB Falling Edge	t _{SDOEN}	—	—	125	ns	
SDO Disable after CSB Rising Edge (Note 1)	t _{SDODE}	—	—	500	ns	

(Note 1) It is specified based on 0 % and 100 % of VCC.

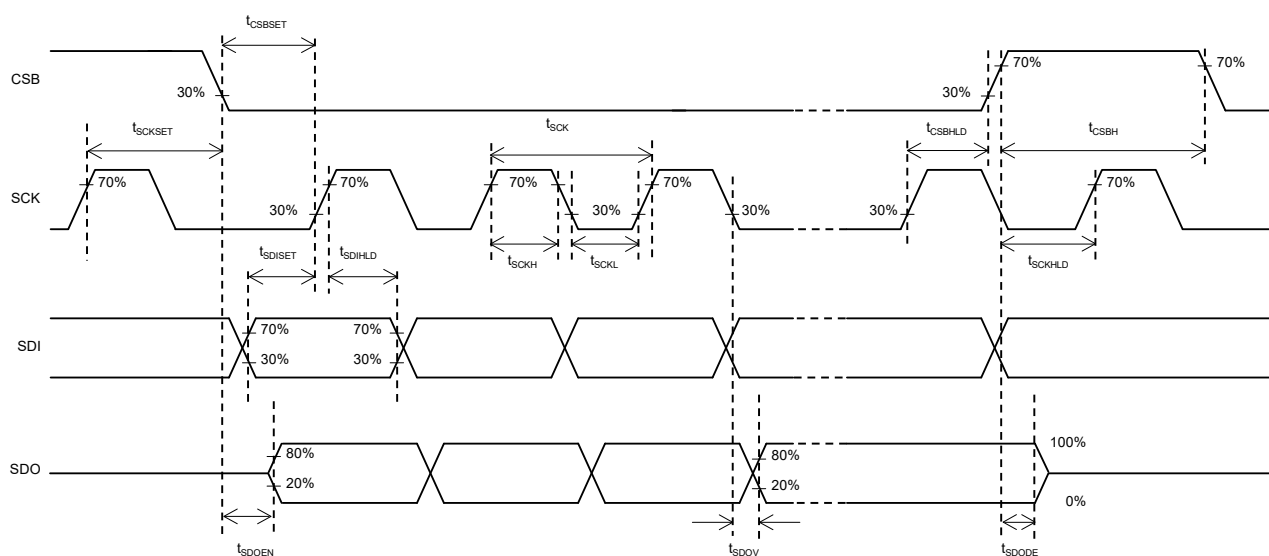


Figure 5. Serial Interface Timing Chart

Power Supply/Driver Sequence Timing Chart

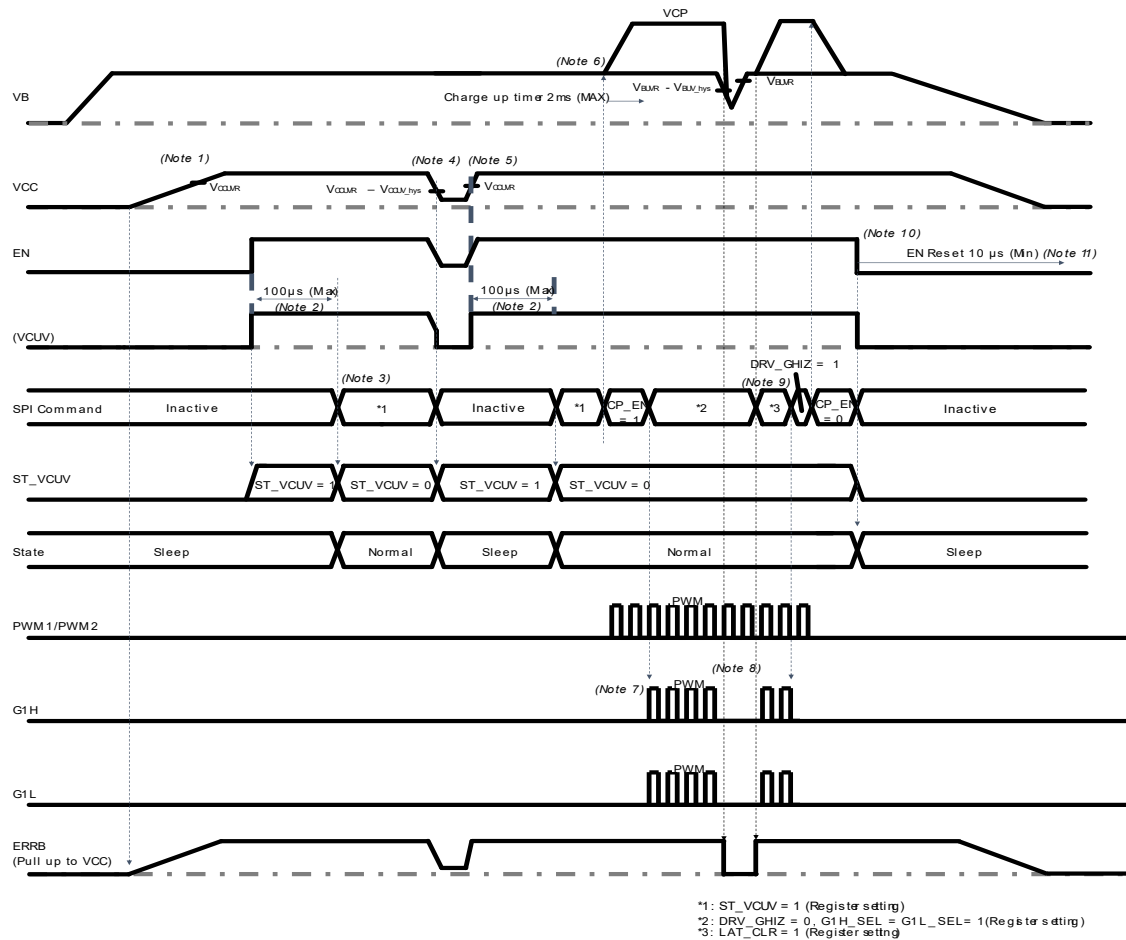


Figure 6. Power Supply Sequence

(Note 1) The undervoltage lockout function (VCUV) monitors the VCC voltage.

When power is turned on, if $VCC \geq V_{CCUVR}$ and EN = High, the status register ST_VCUV = 1 is set and the value is maintained. The VCUV circuit has a blanking time of 2.5 μs (Typ) to prevent false detection due to noise.

(Note 2) After VCC is raised, when EN = High, the device transitions to the Normal State and the analog circuit becomes active. SPI commands can be sent after 100 μs (Max). The transition time from the Sleep State to the Normal State is 100 μs (Max).

(Note 3) The value of register ST_VCUV is cleared by setting register ST_VCUV = 1 with the SPI command.

(Note 4) When the VCC voltage falls below ($V_{CCUVR} - V_{CCUV_{hys}}$) voltage, a VCUV fault is detected, the LOGIC circuit goes into reset state, and the analog circuit turns off.

(Note 5) When the VCC voltage exceeds the fault release voltage (V_{CCUVR}), the VCUV fault is released, the LOGIC circuit becomes operational, and the analog circuit becomes active.

(Note 6) When CP_EN = 1 is set, the charge pump circuit is activated. The startup time is 2 ms (Max). If the charge pump does not start up within 2 ms and VCPUV is not released, a timeout occurs and boost operation stops.

(Note 7) When DRV_GHIZ = 0, G1H_SEL = G1L_SEL = 1 are set, G1H and G1L outputs are PWM driven.

(Note 8) When VBUV fault is detected, the charge pump circuit is turned off and the G1H and G1L outputs are set to Low.

(Note 9) When VBUV fault is detected, the charge pump circuit is turned off and VCPUV is detected.

The charge pump operation and gate driver output operation can be resumed by using an SPI command to set register LAT_CLR = 1.

(Note 10) When EN = Low is set, the device goes into the Sleep State and the analog circuit is turned off. SPI communication is not possible.

(Note 11) When resetting with EN, input an EN = Low period of 10 μs or more.

Constant Current Control

The constant current control of the gate driver can be set individually using SPI register (SPI Address 10h to 13h). There are two current setting modes, which can be selected from non-linear step 1.5 mA to 10 mA (Typ) and 4.5 mA to 30 mA (Typ). The source/sink current does not include a 160 kΩ (Typ) pull-down current.

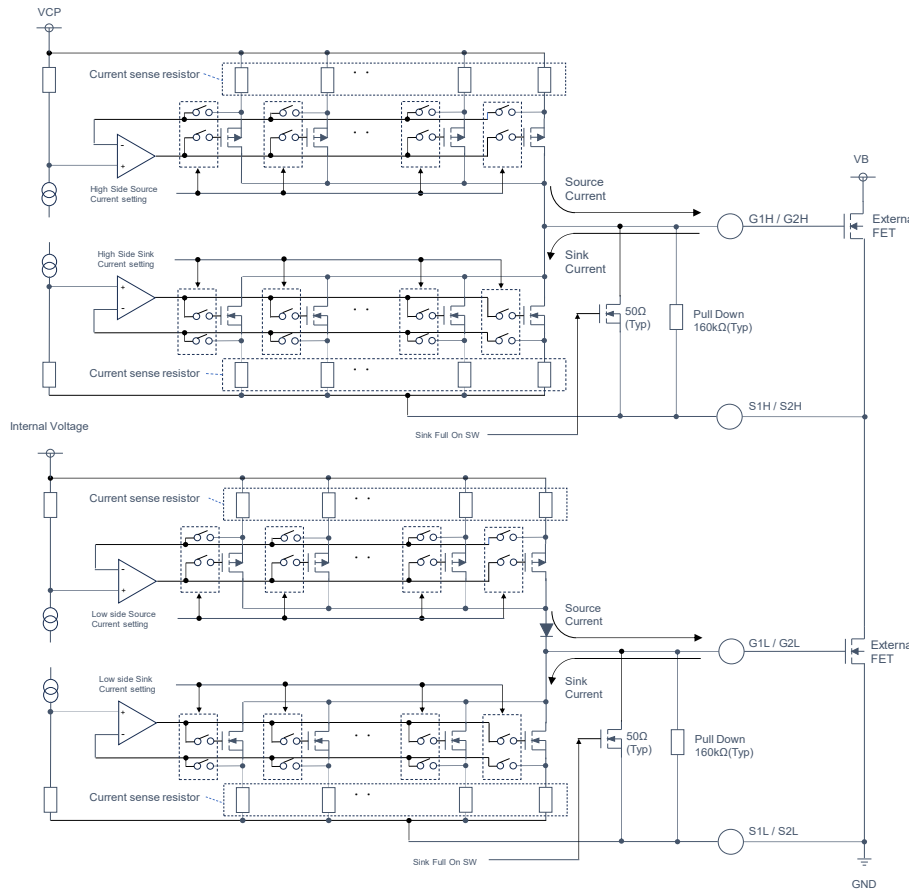
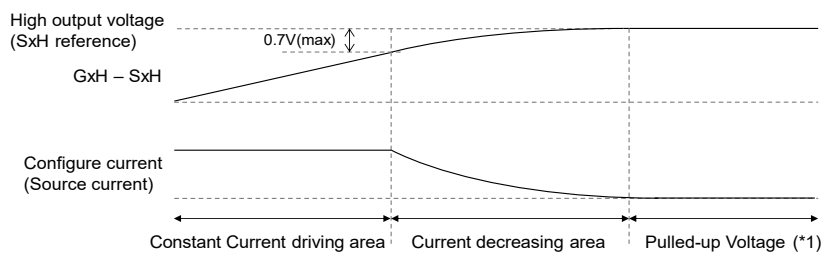


Figure 7. Constant Current Drive Circuit Diagram

High-Side Gate Driver Output Source Current Control

When the (GxH-SxH) voltage exceeds (High Output Voltage <SxH Reference>) - 0.7 V (Max), the source current decreases below the set value. Therefore, the range in which constant current drive is possible is (GxH-SxH) voltage < (High Output Voltage <SxH Reference>) - 0.7 V (Max). After constant current drive, the gate driver outputs G1H and G2H are pulled up by the current detection resistor and PMOS. (x = 1, 2)



(Note) x = 1, 2

*1 : Pulled-up Voltage determined by Current sense resistor and PMOS Ron

Figure 8. High-Side Gate Driver Output Source Current Control Waveform

Low-Side Gate Driver Output Source Current Control

When the (GxL-SxL) voltage exceeds (High output voltage <SxL reference>) - 0.7 V (Max), the source current decreases below the set value. Therefore, the range in which constant current drive is possible is (GxL-SxL) voltage < (High output voltage <SxL reference>) - 0.7 V (Max). After constant current drive, the gate driver outputs G1L and G2L are pulled up by the current detection resistor and PMOS. (x = 1, 2)

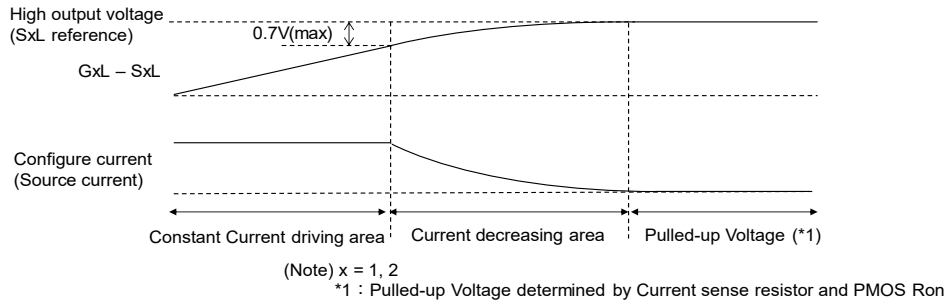


Figure 9. Low-Side Gate Driver Output Source Current Control Waveform

High-Side Gate Driver Output Sink Current Control

When the (GxH-SxH) voltage falls below SxH voltage + 0.7 V (Max), the sink current decreases below the set value. Therefore, the range in which constant current drive is possible is (GxH-SxH) voltage > SxH voltage + 0.7 V (Max). If it falls below this range, the gate driver outputs G1H and G2H are pulled down by the current detection resistor and NMOS. In addition, when the gate driver output falls below the over-voltage protection detection voltage (V_{GSOVD}) and the propagation delay time 2 (t_{propa2}) has elapsed, the NMOS for Full ON turns on and pulls down to 50 Ω (Typ). (x = 1, 2)

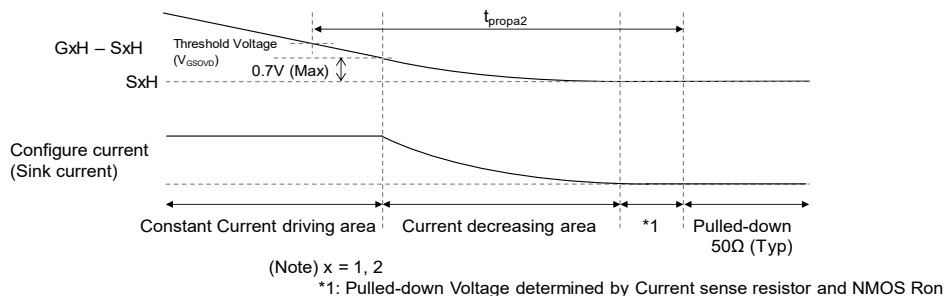


Figure 10. High-Side Gate Driver Output Sink Current Control Waveform

Low-Side Gate Driver Output Sink Current Control

When the (GxL-SxL) voltage falls below SxL voltage + 0.7 V (Max), the sink current decreases below the set value. Therefore, the range in which constant current drive is possible is (GxL-SxL) voltage > SxL voltage + 0.7 V (Max). If it falls below this range, the gate driver outputs G1L and G2L are pulled down by the current detection resistor and NMOS. In addition, when the gate driver output falls below the over-voltage protection detection voltage (V_{GSOVD}) and propagation delay time 2 (t_{propa2}) has elapsed, the Full ON NMOS turns on and pulls down to 50 Ω (Typ). (x = 1, 2)

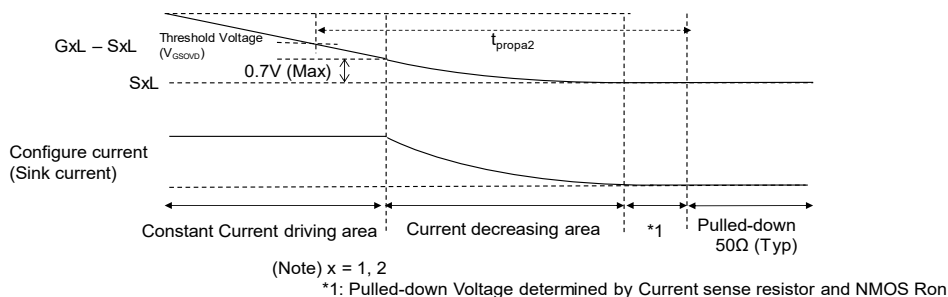


Figure 11. Low-Side Gate Driver Output Sink Current Control Waveform

Drive Modes

There are two modes of driver output control: independent control mode and H-bridge control mode. In the independent control mode, the high-side gate driver and the low-side gate driver can be controlled independently; in the H-bridge control mode, the motor is assumed to be driven with an H-bridge connection, and the high-side and low-side gate driver outputs of the same channel are controlled so that they cannot turn on simultaneously. The H-bridge control mode is designed to drive the motor with an H-bridge connection.

In addition, each driver output can be controlled either through the register setting value GxH_FIX/GxL_FIX or directly from the PWM1 or PWM2 pin. The mode can be selected by the registers GxH_SEL and GxL_SEL.

When register GxH_SEL/GxL_SEL = 0, the driver output can be controlled by the register set value.

When register GxH_SEL/GxL_SEL = 1, the driver outputs are controlled by the PWM1/PWM2 pins; the PWM1 pin controls the G1H/G1L outputs, and the PWM2 pin controls the G2H/G2L outputs. It is also possible to combine PWM control and register set value control for drive control. See [Table 6. Gate Driver Output Control Mode](#), for details on combinations.

Independent Control Mode

When register MODE_SEL = 0 is set, the independent control mode is enabled. In the independent control mode, the high-side gate driver output and the low-side gate driver output can be controlled independently of each other, enabling various drive configurations and making it possible to support a variety of applications. An example connection is shown in the figure below.

When using inductive loads, the absolute maximum ratings of the S1H and S2H pins may be exceeded. Therefore, clamp the S1H and S2H pins by connecting protective diodes as shown in the figure below. Select an appropriate clamping element according to the connected load to prevent the absolute maximum ratings from being exceeded.

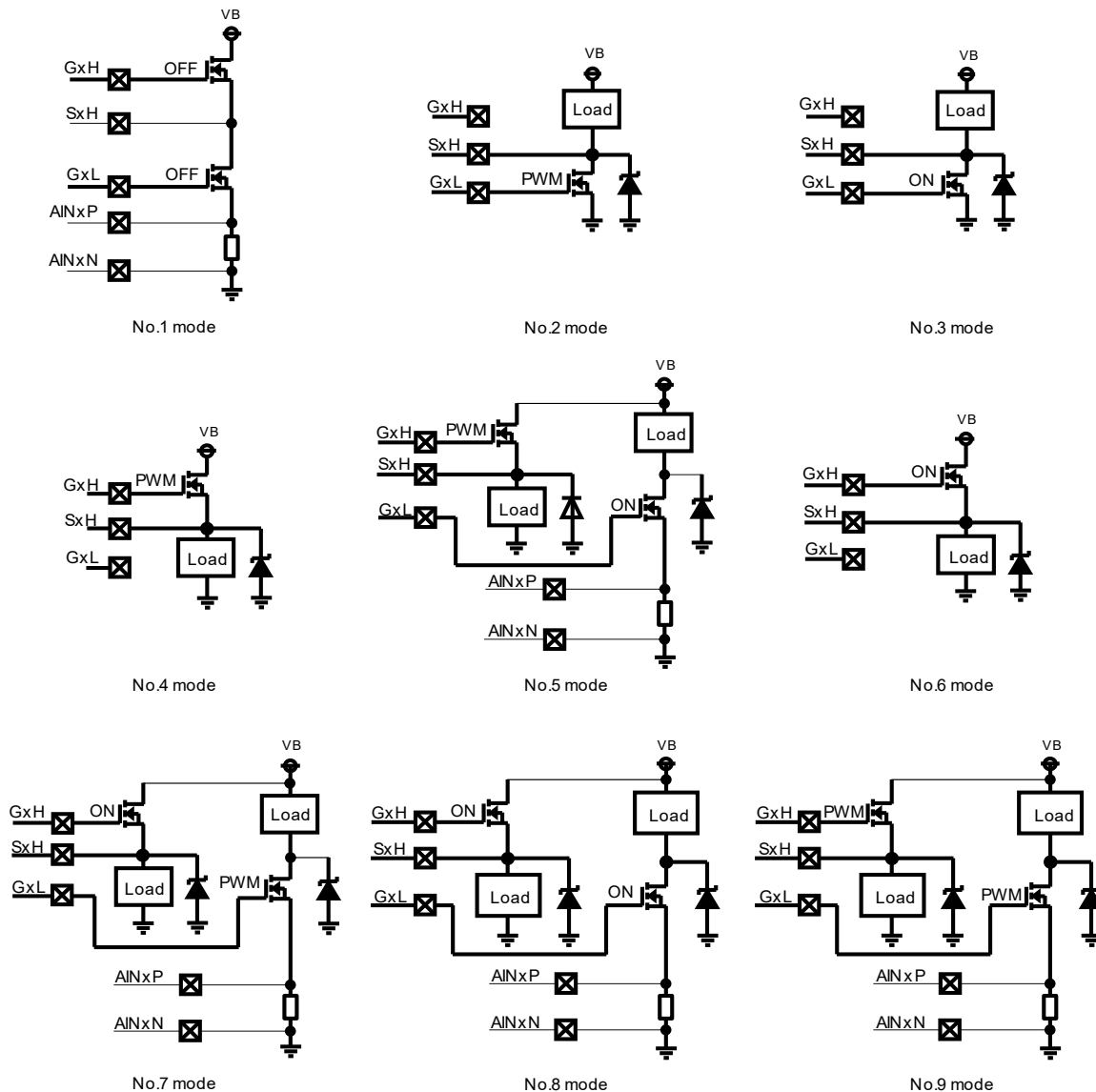


Figure 12. Independent Control Mode Circuit Example

H-bridge Control Mode

Setting register MODE_SEL = 1 places the device in H-bridge control mode; this mode assumes an H-bridge connection. The high-side / low-side gate drivers can be controlled from the register setting value or PWM1 pin input and PWM2 pin input.

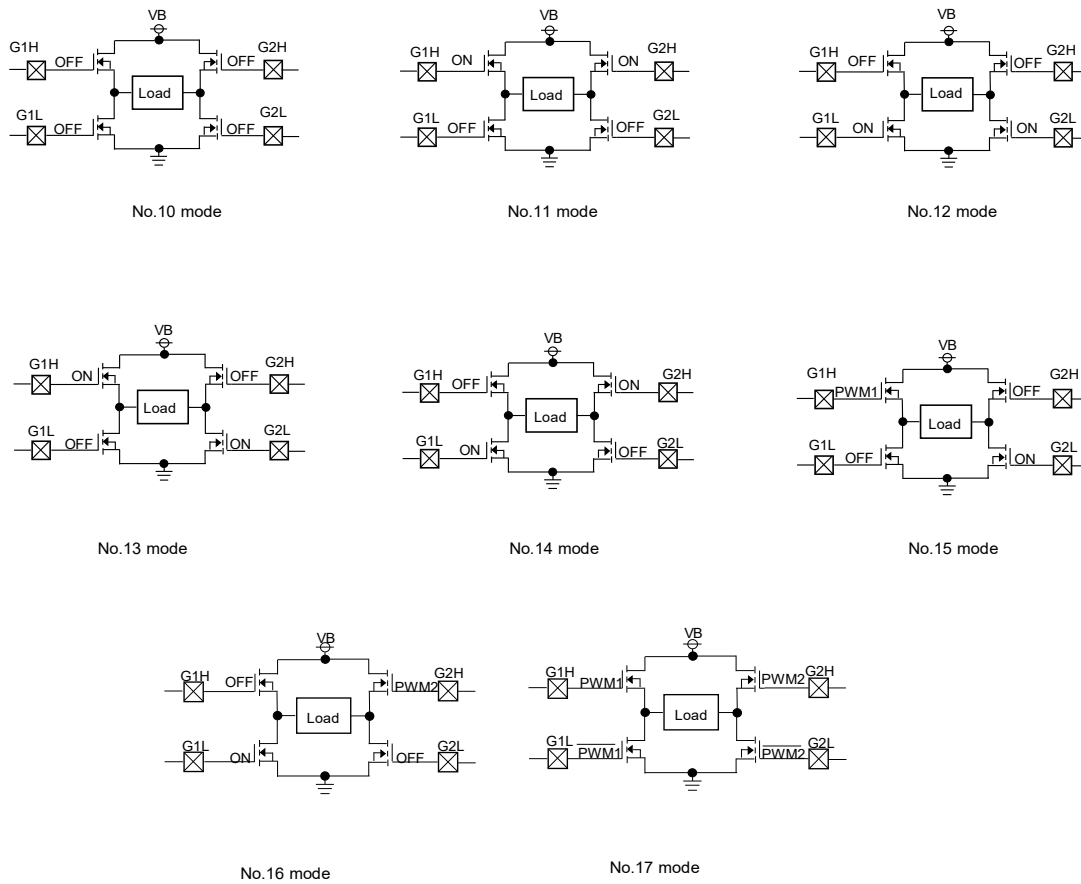


Figure 13. H-bridge Control Mode Circuit Example

PWM Control

PWM control of the gate driver output differs between independent control mode and H-bridge control mode.

In independent control mode, the high-side gate driver and low-side gate driver are controlled at the same time, but in H-bridge control mode, a Dead Time is inserted to prevent the high-side and low-side gate driver outputs from being turned on at the same time.

Independent Control Mode

The relationship between the PWMx input and the GxH, GxL output signals for independent control mode is shown in the diagram below. When the registers `MODE_SEL = 0`, `GxH_SEL = GxL_SEL = 1` are set, G1H and G1L will output High/Low with the same polarity depending on the logic input to the PWM1 pin. Similarly, G2H and G2L will output High/Low with the same polarity depending on the logic input to the PWM2 pin. Since the signal input to the PWMx pin is synchronized with the internal clock, a synchronization delay time (t_{syn}) occurs. In addition, there is a propagation delay time 1 (t_{propa1}) before GxH and GxL start output. ($x = 1, 2$)

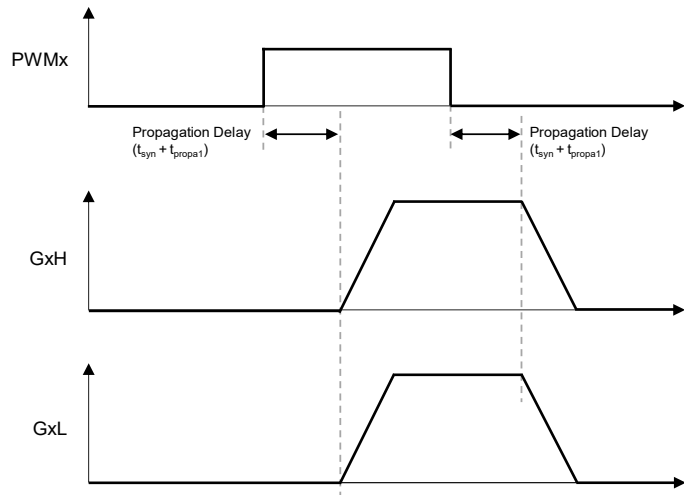


Figure 14. PWM Output Timing Chart (Independent Control Mode)

H-bridge Control Mode

The relationship between the PWMx input, GxH, and GxL output signals for H-bridge control mode is shown in the diagram below. When register `MODE_SEL = 1`, `GxH_SEL = GxL_SEL = 1`, G1H and G1L output High/Low with opposite polarity depending on the PWM1 pin input logic. Similarly, G2H and G2L output High/Low with opposite polarity depending on the PWM2 pin input logic. Since the signal input to the PWMx pin is synchronized with the internal clock, a synchronization delay time (t_{syn}) occurs. In addition, there is a propagation delay time 1 (t_{propa1}) until GxH and GxL start output. In H-bridge control mode, the gate driver voltage is monitored to prevent shoot-through current in the external MOS FET, and the Dead Time (t_{DEAD}) set in register `TDEAD [3:0]` is inserted from the time when the gate driver voltage reaches $V_{GSOVD} = 1.2\text{ V}$ (Typ) to prevent shoot-through current. ($x = 1, 2$)

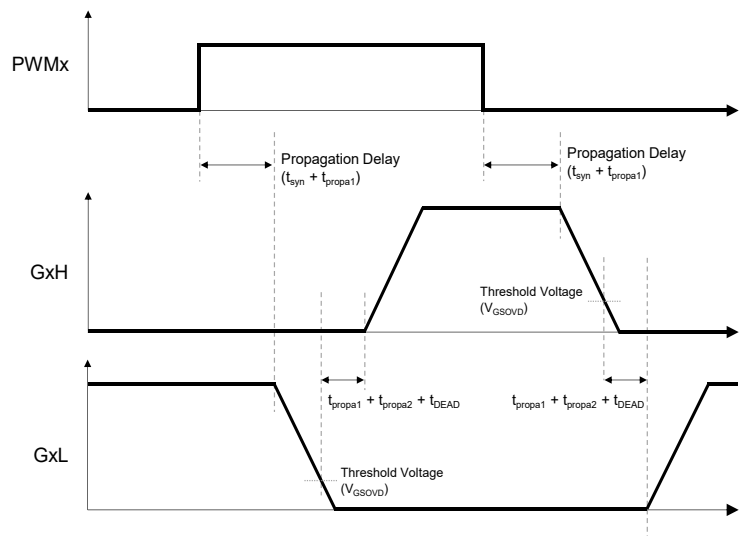


Figure 15. PWM Output Timing Chart (H-bridge Control MODE)

Charge Pump Circuit (CP)

The device is equipped with a charge pump circuit that generates the voltage to drive the gate driver of the external high-side MOS FET transistor. A 0.1 μF capacitor must be connected between the CPH and CPL pins, and a 0.1 μF capacitor must be connected between the VCP and VB pins. When there is no load or the VB power supply voltage is 13.5 V or higher, the VCP pin voltage is boosted to the VB voltage + 10.8 V (Typ). The charge pump is driven by the built-in oscillator with a 400 kHz (Typ) clock.

When register CP_EN = 0, the protection functions of VCPUV, DHUV, VGSOV (high-side), VGSUV (high-side), and VDSOV (high-side) are disabled.

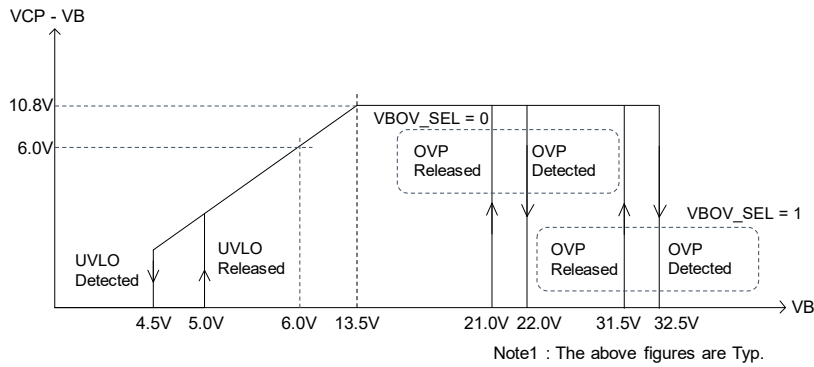


Figure 16. Charge Pump Output Potential Relationship Diagram

Current Sense Amplifier (CSAMP)

It is equipped with a current detection amplifier to detect the current flowing through the shunt resistor. The gain can be set using the register CSAMP_GAIN. The reference voltage VREF can be set using the input voltage of the REF pin and the register CSAMP_REF. The current detection amplifier output voltage is expressed by the following formula.

$$AOUT1 = (AIN1P - AIN1N) \times Gain + VREF$$

$$AOUT2 = (AIN2P - AIN2N) \times Gain + VREF$$

The current detection amplifier can be set as follows.

To use the current detection amplifier, set the register CS_EN = 1. If not using it, set the register CS_EN = 0 to reduce power consumption.

CS_EN	Current Detection Amplifier Function
0	Disable
1	Enable

Set CSAMP_GAIN [1:0] register to change the gain of the current detection amplifier.

CSAMP_GAIN [1:0]	Gain Settings
0h	x 8
1h	x 16
2h	x 32
3h	x 48

Set CSAMP_REF register to change the reference voltage VREF of the current sense amplifier.

CSAMP_REF	Reference Voltage VREF Settings
0	REF/2
1	REF/8

An open input pin of a current sense amplifier can be detected by checking for an abnormal voltage in the AOUTx voltage.

(Example) When no motor current is flowing ($AINxP = AINxN = GND$), the AOUTx output voltage is $VREF + \text{output offset voltage}$. When $AINxP$ is open, the AOUTx output goes high, and when $AINxN$ is open, the AOUTx output goes low, indicating an abnormality. ($x = 1, 2$)

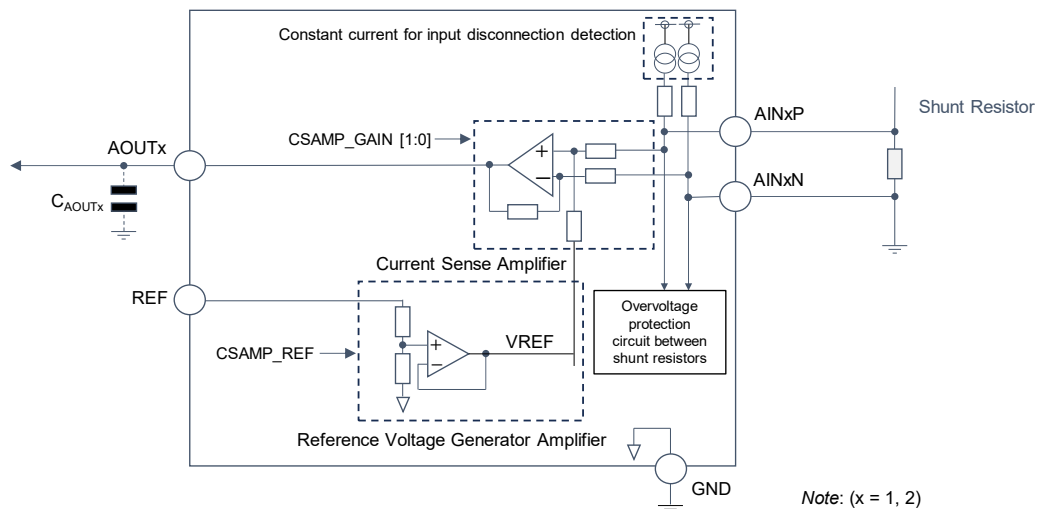


Figure 17. Current Detection Amplifier Current Detection Connection Configuration Diagram

DBRKB Function

This function forcibly puts the gate driver output into a short brake by the DBRKB pin input, without going through the internal LOGIC circuit, even in the sleep state (EN = Low) where SPI communication is not possible.

When the DBRKB pin is set to Low, the gate driver outputs G1H and G2H will be low outputs, and G1L and G2L will be high outputs. It is recommended to use this function in the sleep state (EN = Low). If used in the normal state (EN = High), a mismatch may occur between the control input and gate driver output. Please note that in such cases, the LOGIC circuit will detect various faults.

In addition, when the Sleep State (EN = Low) is set, the VB current can be reduced by inserting a pull-down resistor into the DBRKB pin and connecting it to GND. Use a pull-down resistor of 220 kΩ (Typ) or less.

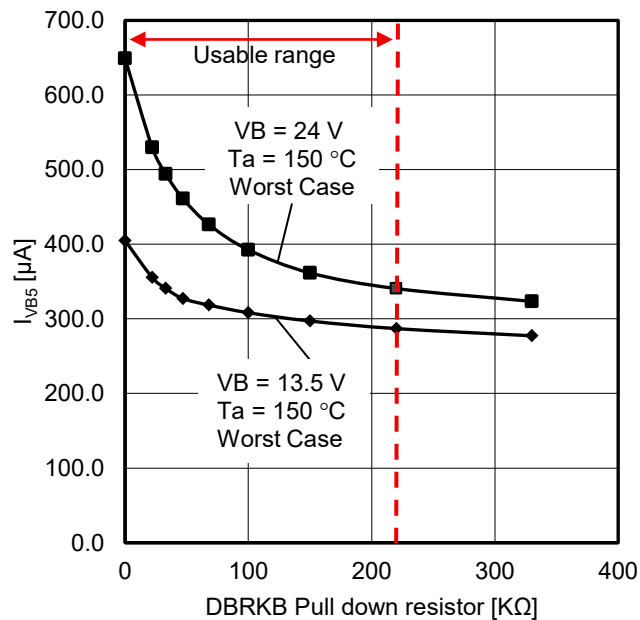


Figure 18. EN = Low, DBRKB VB Current Characteristics When Inserting Pull Down Resistor (Reference Value)

Static OPEN/SHORT Detection Function

The static open/short detection function is a function that can detect if the external MOS FET is either open or short without passing a large current before driving the motor. When using this function, be sure to start the charge pump circuit before starting. Even if an open or short state is detected, the error notification signal (ERRB) will not output low. Check the values of register ST_OSCHK_FAIL and register ST_OSCHK to see the detection result.

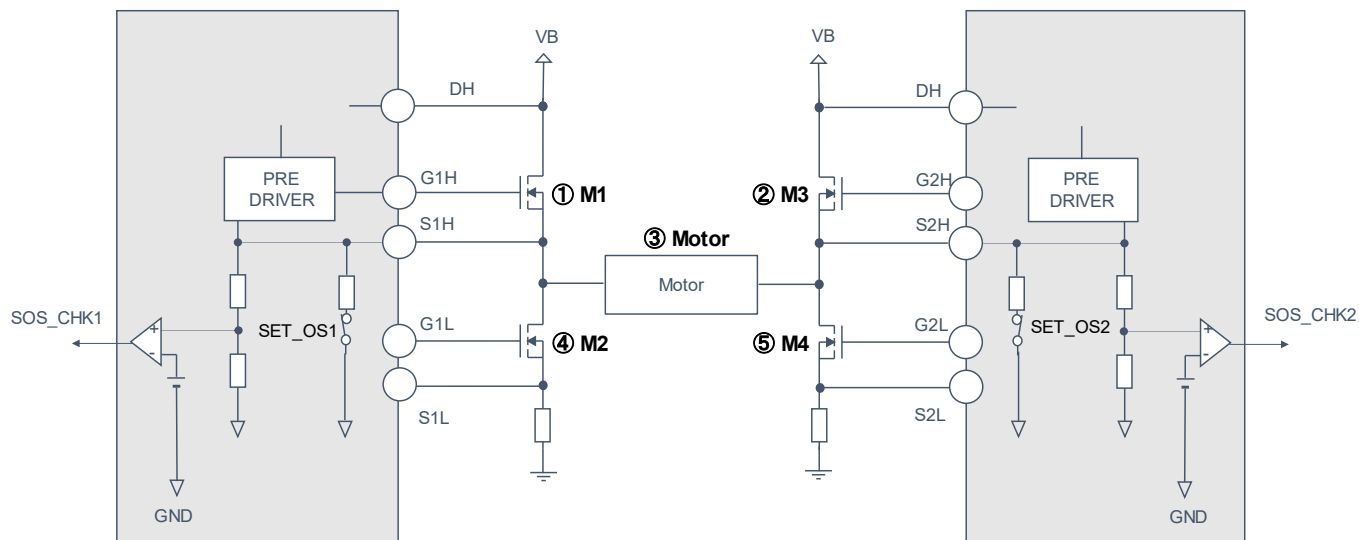


Figure 19. Static Open/Short Detection Function Block Diagram

The detection function has two modes: automatic detection mode and manual detection mode. The detection mode can be controlled by the following registers: DRV_GHIZ, OS_EN, and AUTO_OS_START.

Register Setting			Description
DRV_GHIZ	OS_EN	AUTO_OS_START	
0	X	X	Function is inactive
1	0	X	Function is inactive
1	1	1	Auto Detection mode (See Table 2)
1	1	0	Manual Detection mode (See Table 3)

When using the static open/short detection function, the VGSOV, VGSUV, and VDSOV protection functions are disabled.

Automatic Detection Mode

In automatic detection mode, the sequence in Table 2 is executed automatically in step order from 1 to 7. The step period is 2 ms (Typ). When the sequence is executed and completed, the register ST_OSCHK_END = 1 is set. If fault is detected, the check sequence is terminated at that point and the register ST_OSCHK_FAIL = 1 is set. The step value of the completed sequence is also set to the register ST_OSCHK_STEP. The registers ST_OSCHK_END and ST_OSCHK_FAIL are only valid in automatic detection mode. They are initialized when the IC starts up and when the detection sequence starts, and the results are retained after the sequence is executed. Depending on the motor load used, the change in the SxH pin voltage may be slow and fault may not be detected correctly. If the SxH pin voltage does not stabilize within 1.5 ms, use manual detection mode.

Table 2. Automatic Detection Mode Table (DRV_GHIZ = OS_EN = AUTO_OS_START = 1 setting)

Step	Setting (Note 4)						H-bridge Determination Method											
	Output Signal				Internal Switch		Detection Part										Detection Results (Status Register)	
	G2H	G2L	G1H	G1L	SET_OS2	SET_OS1	Open					Short					ST_OSCHK2 (Note 1)	ST_OSCHK1 (Note 1)
							①	②	③	④	⑤	①	②	③	④	⑤		ST_OSCHK_STEP[2:0] (Note 2)
1	L	L	L	L	0	0											0	0
																	1	0
																	Other	
2	L	L	L	L	0	1											0	0
																	0	1
																	1	0
																	Other	
3	L	L	L	L	1	0											0	0
																	0	1
																	0	1
																	Other	
4	L	L	H	L	0	1											0	0
																	1	0
																	Other	
5	H	L	L	L	1	0											0	0
																	1	1
																	Other	
6	L	L	L	H	0	0											0	0
																	1	1
																	Other	
7	L	H	L	L	0	0											0	0
																	0	1
																	Other	

(Note 1) Register Description See. [Table 19. Static OPEN/SHORT Check Results](#)

(Note 2) Register Description See. [Table 18. Static OPEN/SHORT Check Detection Step](#)

(Note 3) Illegal (Fail) refers to any fault state other than a single open/short fault such as ① to ⑤ in Figure 19.

(Note 4) In automatic detection mode, the gate output control mode (Address = 03h <Mode Settings>) setting is invalid.

Manual Detection Mode

In manual detection mode, open/short detection is possible by controlling the internal switch and gate output pins through register writing as shown in Table 3 in setting column.

In the manual detection mode, to prevent destruction of external MOS FET due to shoot-through-currents, check for failures in the order of Steps in Table 3, "Manual Detection".

Table 3. Manual Detection Mode Table (DRV_GHIZ = OS_EN = AUTO_OS_START = 0 setting)

Table 6: Manual Detection Mode Table (DRV_CH2 = OS_EN = AS16_OS_START = 0 Setting)																			
(Example) Step	Setting (Note 3)						H-bridge Determination Method												
	Output Signal				Internal Switch		Detection Part					Detection Results (Status Register)							
	G2H	G2L	G1H	G1L	SET_OS2	SET_OS1	Open					ST_OSCHK2 (Note 1)	ST_OSCHK1 (Note 1)	Remark (Note 2)					
							①	②	③	④	⑤				①	②	③	④	⑤
1	L	L	L	L	0	0								0	0	Normal			
																1	0	④ or ⑤ FET Short	
																	Other	Illegal (Fail) (Note2)	
																0	0	Normal	
2	L	L	L	L	0	1								0	1	① or ② FET Short			
																1	0	③ Open	
																	Other	Illegal (Fail)	
																0	0	Normal	
3	L	L	L	L	1	0								0	1	① or ② FET Short			
																0	1	③ Open	
																	Other	Illegal (Fail)	
																0	0	Normal	
4	L	L	H	L	0	1								1	0	① Open			
																	Other	Illegal (Fail)	
																0	0	Normal	
																1	1	② Open	
5	H	L	L	L	1	0								0	0	Normal			
																	1	1	② Open
																	Other	Illegal (Fail)	
																0	0	Normal	
6	L	L	L	H	0	0								1	1	④ Open			
																	Other	Illegal (Fail)	
																0	0	Normal	
																0	1	⑤ Open	
7	L	H	L	L	0	0								0	0	Normal			
																	0	1	⑤ Open
																	Other	Illegal (Fail)	
																0	0	Normal	

(Note 1) Static OPEN/SHORT Check register see. [Table 19. Static OPEN/SHORT Check Results](#)

(Note 2) Illegal (Fail) refers to any fault state other than a single open/short fault such as ① to ⑤ in Figure 18.

(Note 3) In manual detection mode, the external PWM control mode (GxH_SEL, GxL_SEL) setting is invalid (x = 1, 2).

After checking and taking measures against an open/short fault detected by the Static Open/Short function, recheck the status using automatic detection or manual detection mode, etc., to make sure that the open/short fault has been removed.

If you omit checking automatic detection or manual detection and turn on the gate driver output, consider the guaranteed range of the external MOS FET characteristics and set the blanking time and drive current with a margin.

EN Pin and Reset Operation

The following reset operations are available. Each register setting is reset and returns to the initial state.

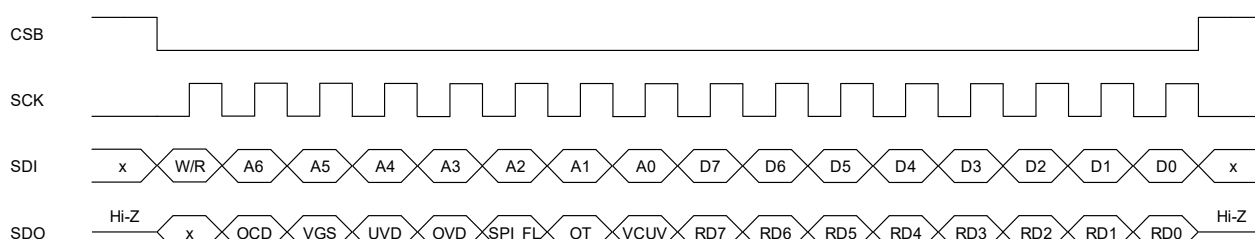
Table 4. Reset Operation

Item	Detail
EN = Low	The IC circuit operation stops. It is initialized and starts operating when EN = High.
VCUV (VCC Undervoltage Detection)	The LOGIC circuit is in reset state. It starts operating when the low voltage state is released.
Software Reset	The LOGIC circuit is initialized when EN = High. Send data of 5Ah to register address 00h using the SPI command to immediately initialize all registers.

Serial Interface

SPI Protocol

The serial interface allows reading the status register and configuring each IC setting. The input pins CSB, SCK, and SDI are used. When CSB is low, serial data is accepted. Write data (SDI) consists of a total of 16 bits: an 8-bit address and 8 bits of data. SDI data is captured on the rising edge of SCK, and after all 16 bits of data have been received, it is written to the register. Read data (SDO) outputs various statuses for faults and register values of the specified address. SDO data also starts being output on the rising edge of SCK. When CSB goes from low to high, the SPI transfer is considered to be completed and the internal register starts being updated.



W/R: Read/Write specified bits

A6-A0: Address Data

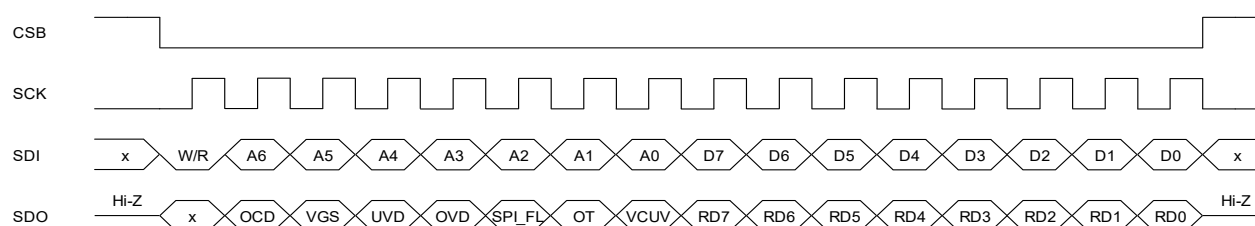
D7-D0: Data to be written to the address specified by bits A6-A0

RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 20. SPI Protocol

Write Registers

To write to a register, set the W/R bit to low. The A6-A0 bits specify the address of the register to be written to, and D7-D0 specify the data to be written to the register. When writing, data is also output from SDO. The SDO output data bits OCD, VGS, UVD, OVD, SPI_FL, OT, and VCUV are called the Global status registers, and output the protection status. The RD7-RD0 bits output the register value (the value immediately before the write) of the address specified by the A6-A0 bits.



W/R: Read/Write specified bits

A6-A0: Address Data

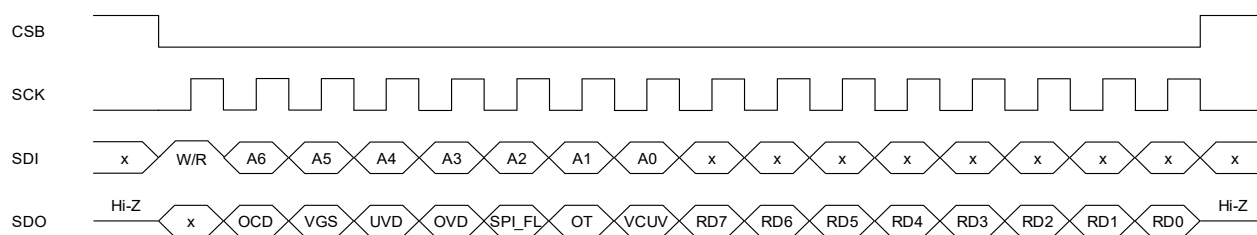
D7-D0: Data to be written to the address specified by bits A6-A0

RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 21. Register Write Protocol

Read Register

To read a register, set the W/R bit to High. The A6-A0 bits specify the address of the register to be read. Any SDI data in a correct SPI transaction thereafter is ignored. The individual register data is output from SDO. As with writing, the OCD, VGS, UVD, OVD, SPI_FL, OT, and VCUV bits of the SDO output data are global status registers and output the protection status. The RD7-RD0 bits output the register value (the value immediately before the write) of the address specified by the A6-A0 bits.



W/R: Read/Write specified bits

A6-A0: Address Data

RD7-RD0: Register value at address specified by bits A6-A0 (data immediately before writing)

Figure 22. Register Read Protocol

Global Status Register

The global status registers are data bits in SDO that output the protection status. These are the OCD, VGS, UVD, OVD, SPI_FL, OT, and VCUV bits of the SDO output data. It works in conjunction with the normal status register (ST_XXX) and is assigned as follows.

OCD bits : ST_VDS_Hx, ST_VDS_Lx, ST_VRDET_x (x = 1, 2)

VGS bits : ST_VGS_Hx_OV, ST_VGS_Lx_OV, ST_VGS_Hx_UV, ST_VGS_Lx_UV (x = 1, 2)

UVD bits : ST_VBUV, ST_VCPUV, ST_DHUV

OVD bits : ST_VBOV, ST_VCOV

SPI_FL bit : ST_SPI

OT bit : ST_TW, ST_TSD

VCUV bit : ST_VCUV

The global status register (OCD, VGS, UVD, OVD, OT bits) to which multiple status registers are assigned outputs the OR logic of each status register, so an error is notified if any of the protections is detected. If you want to identify the location where an abnormality has occurred, check the status register.

When the value of each status register (ST_XXX) is cleared, the value of the corresponding global status register is also cleared.

Error Notification Signal (ERRB)

The ERRB signal notifies you in real time when any selected protection function detects fault. This signal is an NMOS open-drain output, and outputs low when fault is detected. It can also be used in common with NMOS open-drain in other CHIPS. The items for which you want to be notified of faults with the ERRB signal can be selected using the flag setting registers (SPI Address 0Dh-0Fh). Also, if a low level is detected in the ERRB signal, you can check what fault was detected by checking the value of each status register (SPI Address 04h-06h). The ERRB signal is not released in conjunction with the value of each status register. The operation when the fault or fault behavior is released depends on the setting value of each protect function control register (LAT_XXX).

When LAT_XXX = 0, fault detection is monitored in real time and notification of ERRB signal is released in conjunction with the protect function detection state.

When LAT_XXX = 1, the fault notification of the ERRB signal continues even if the detected fault behavior is released. To release the ERRB signal and the protect function operation, set the register LAT_CLR = 1 and then reset.

The value of the register LAT_CLR is automatically initialized to LAT_CLR = 0 after LAT_CLR = 1 is set.

For each protect operation control register (LAT_XXX), refer to the operation explanation of each protection function or the explanation of each register [Address = 07h <Latch Settings1>](#), [Address = 08h <Latch Settings2>](#), [Address = 09h <Latch Settings3>](#).

Protective Function

Table 5. Protection Function Table

Protection	Detect Conditions (Typ)		Protect Operation		Status Register
	Detect	Release	Charge Pump	Gate driver output (G1H, G2H, G1L, G2L)	
VCUV	$VCC \leq 2.70 \text{ V}$	$VCC \geq 2.75 \text{ V}$	OFF	Initialize all registers Pull down all output <i>(Note 5)</i>	ST_VCUV
VCOV	$VCC \geq 6.0 \text{ V}$	$VCC \leq 5.8 \text{ V}$	ON	Outputs Low	ST_VCOV
VBUV	$VB \leq 4.5 \text{ V}$	$VB \geq 5.0 \text{ V}$	OFF	Pull down all output <i>(Note 5)</i>	ST_VBUV
VBOV	$VB \geq 22.0 \text{ V}$ (VBOV_SEL = 0) or $VB \geq 32.5 \text{ V}$ (VBOV_SEL = 1)	$VB \leq 21.0 \text{ V}$ (VBOV_SEL = 0) or $VB \leq 31.5 \text{ V}$ (VBOV_SEL = 1)	OFF	Set MODE_SEL = 0 Pull down all output <i>(Note 5)</i> Set MODE_SEL = 1 Short brake output <i>(Note 3)</i>	ST_VBOV
VCPUV	$VCP \leq 3.0 \text{ V}$ (VCP-DH)	$VCP \geq 3.2 \text{ V}$ (VCP-DH)	OFF	Set MODE_SEL = 0 G1H, G2H Outputs Low G1L, G2L Normal Operation Set MODE_SEL = 1 Short brake output <i>(Note 3)</i>	ST_VCPUV
DHUV	$DH \leq 4.9 \text{ V}$	$DH > 4.9 \text{ V}$	OFF	G1H, G2H Outputs Low G1L, G2L Normal Operation	ST_DHUV
VDSOV	(Drain-Source) <i>(Note 4)</i> $\geq V_{VDSx}$ <i>(Note 1)</i>	(Drain-Source) <i>(Note 4)</i> $< V_{VDSx}$ <i>(Note 1)</i>	ON	Only the output detected is low	ST_VDS_H1 ST_VDS_H2 ST_VDS_L1 ST_VDS_L2
RDET	$AINxP-AINxN \geq V_{RDET_x}$ <i>(Note 2)</i> (X = 1, 2)	$AINxP-AINxN < V_{RDET_x}$ <i>(Note 2)</i> (X = 1, 2)	ON	Only the Low-Side output of the detected phase is low	ST_VRDET1 ST_VRDET2
TSD	$T_j \geq 175 \text{ }^{\circ}\text{C}$	$T_j \leq 160 \text{ }^{\circ}\text{C}$	OFF	Pull down all output <i>(Note 5)</i>	ST_TSD
TW	$T_j \geq 132.5 \text{ }^{\circ}\text{C}$	$T_j \leq 122.5 \text{ }^{\circ}\text{C}$	ON	Normal Operation	ST_TW
VGSUV	(Gate-Source) <i>(Note 4)</i> $\leq 3.0 \text{ V}$	(Gate-Source) <i>(Note 4)</i> $> 3.0 \text{ V}$	ON	Only the output detected is low	ST_VGS_H1_UV ST_VGS_L1_UV ST_VGS_H2_UV ST_VGS_L2_UV
VGSOV	(Gate-Source) <i>(Note 4)</i> $\geq 1.2 \text{ V}$	(Gate-Source) <i>(Note 4)</i> $< 1.2 \text{ V}$	ON	Only the output detected is Pull down	ST_VGS_H1_OV ST_VGS_L1_OV ST_VGS_H2_OV ST_VGS_L2_OV
SPI_FAIL	SCK Pulse $\neq 16$	SCK Pulse = 16	ON	Normal Operation	ST_SPI

(Note 1) The detection voltage threshold can be set using the registers VDS_H1, VDS_H2, VDS_L1, and VDS_L2.

[Address = 17h <VDS Settings1>](#), [Address = 18h <VDS Settings2>](#)

(Note 2) The detection voltage threshold can be set using the registers RDET1 and RDET2.

[Address = 19h <RDET Settings>](#)

(Note 3) The short brake output is a mode that turns on the external low-side MOS FET.

(Note 4) Monitors the (Gate-Source) and (Drain-Source) of an external MOS FET.

(Note 5) Pulled down with 160 k Ω (Typ).

(Note) When register CP_EN = 0, the VCPUV, DHUV, VGSOV (high-side), VGSUV (high-side), and VDSOV (high-side) protection functions are disabled.

When register DRV_GHIZ = 1, the VGSOV, VGSUV, and VDSOV protection functions are disabled.

When register OS_EN = 1, the VGSOV, VGSUV, and VDSOV protection functions are disabled.

VCC Undervoltage Lock Out (VCUV)

This protect function monitors the VCC pin for fault undervoltage behavior and performs VCUV protection operation should it detect said behavior. When the applied voltage to the VCC pin falls below $(V_{CCUVR} - V_{CCUV_hys}) = 2.70\text{ V (Typ)}$, a VCUV fault is detected, and when the voltage rises above $(V_{CCUVR}) = 2.75\text{ V (Typ)}$, it is released. A blanking time of $2.5\text{ }\mu\text{s (Typ)}$ is provided to prevent false detections due to noise. When the VCUV fault is detected, the gate driver output is pulled down to $160\text{ k}\Omega\text{ (Typ)}$ and the charge pump output is also stopped. At this time, the LOGIC circuit will be in a reset state, so SPI communication is not possible and the ERRB signal will continue to output the initial value. In addition, the status register $\text{ST_VCUV} = 1$ is set. When the fault behavior is no longer detected, the LOGIC circuit starts operating again and SPI communication is enabled. The status register value can be reset by writing $\text{ST_VCUV} = 1$. Note that the status register ST_VCUV has a different initial value from the other status registers. The initial value is $\text{ST_VCUV} = 1$ (fault detected), so it is necessary to first set $\text{ST_VCUV} = 0$.

Global Status: VCUV

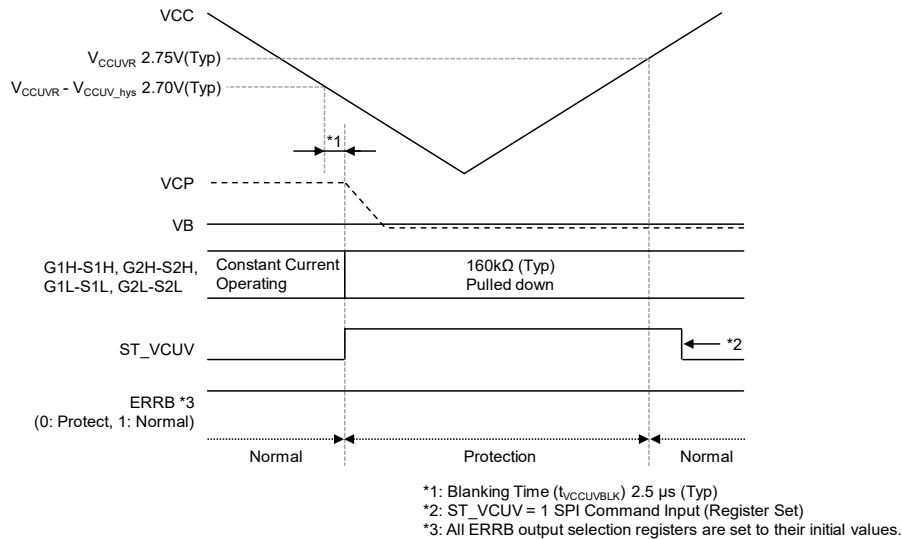


Figure 23. VCC Undervoltage Protection Timing Chart

VCC Overvoltage Protection (VCOV)

This protect function monitors VCC pin for fault overvoltage behavior and performs VCOV protection operation should it detect said fault behavior. When the applied voltage to the VCC pin exceeds (V_{CCOVD}) = 6.0 V (Typ), a VCOV fault is detected and it is released when the voltage falls below ($V_{CCOVD} - V_{CCOV_hys}$) = 5.8 V (Typ). A blanking time of 64 μ s (Typ) is provided to prevent false detections due to noise. If this fault behavior is detected, the protection operation will have the gate driver output set to low. At this time, the protect function sets the status register ST_VCOV to '1'. How the protection operation is released depends on the setting value of the register LAT_VCOV.

When the register LAT_VCOV = 0, the gate driver output will automatically recover when the VCOV is no longer detected by this protect function.

When the register LAT_VCOV = 1, the gate driver output will continue the protection operation even if VCOV is no longer detected. To release the protection operation, set the register LAT_CLR = 1 via SPI write. However, while VCOV is detected, the protection operation will not be released even if LAT_CLR = 1 is set. Also, the value of the register LAT_CLR is automatically initialized to LAT_CLR = 0 after LAT_CLR = 1 is set. The value of the status register ST_VCOV can be reset by writing ST_VCOV = 1.

Do not exceed the absolute maximum rating of the power supply voltage as it may cause destruction.

Global Status: OVD

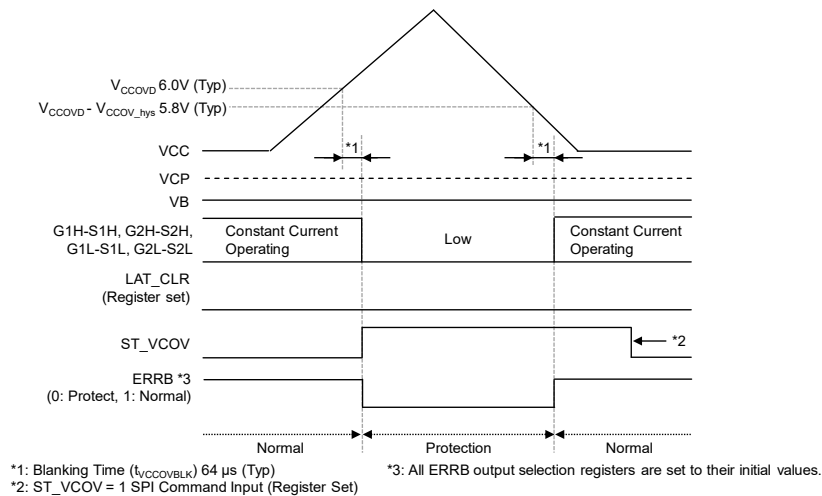


Figure 24. VCC Overvoltage Protection Timing Chart (LAT_VCOV = 0)

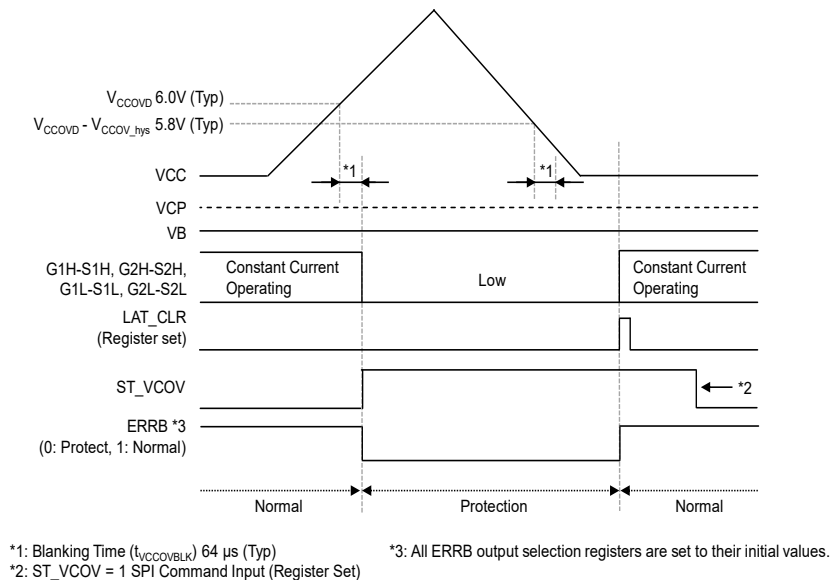


Figure 25. VCC Overvoltage Protection Timing Chart (LAT_VCOV = 1)

VB Undervoltage Protection (VBUV)

This protect function monitors the VB pin for fault undervoltage behavior and performs VBUV protection operation should it detect said fault behavior. When the voltage applied to the VB pin falls below $(V_{BUVR} - V_{BUV_hys}) = 4.5\text{ V (Typ)}$, a VBUV fault is detected, and when it rises above $(V_{BUVR}) = 5.0\text{ V (Typ)}$, it is released. A blanking time of $64\text{ }\mu\text{s (Typ)}$ is provided to prevent false detection due to noise. If this fault behavior is detected, the gate driver output is pulled down to $160\text{ k}\Omega\text{ (Typ)}$ and the charge pump output is also stopped. At this time, the protect function sets the status register ST_VBUV to '1'. How the protection operation is released depends on the setting value of the register LAT_VBUV.

When the register LAT_VBUV = 0, if the charge pump circuit does not detect a low voltage when the VBUV is no longer detected, the gate driver output will automatically recover. If the charge pump circuit detects a low voltage, the gate driver output will recover by starting the charge pump circuit. To start the charge pump circuit, the register LAT_CLR = 1 must be set. When the register LAT_VBUV = 1, the gate driver output will continue protection operation even if VBUV is no longer detected. To release the protection operation state, set the register LAT_CLR = 1 via SPI write. This will release the protection operation, start the charge pump circuit, and restore the gate driver output. However, while a VBUV is still being detected, protection operation will not be released even if LAT_CLR = 1 is set. Also, after setting LAT_CLR = 1, the register LAT_CLR is automatically initialized to LAT_CLR = 0. The value of the status register ST_VBUV can be reset by setting ST_VBUV = 1.

Global Status: UVD

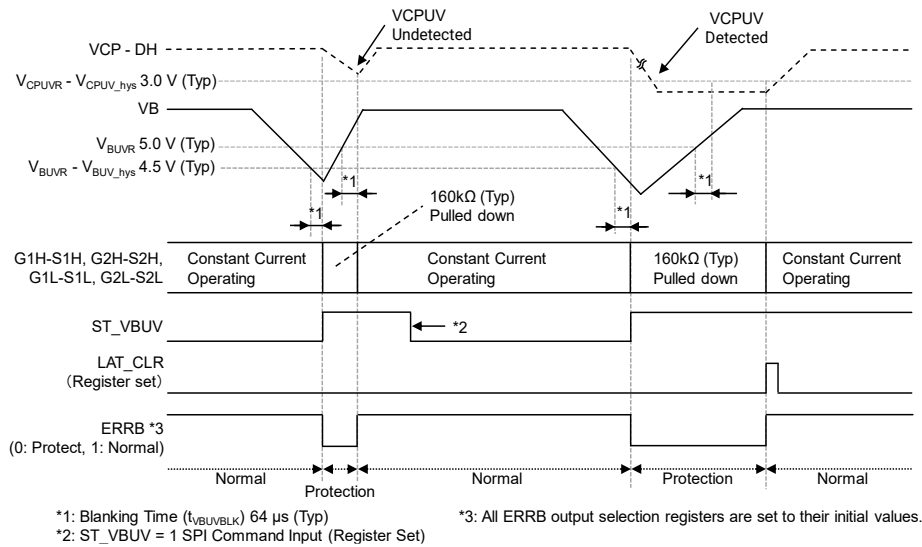


Figure 26. VB Undervoltage Protection Timing Chart (LAT_VBUV = 0)

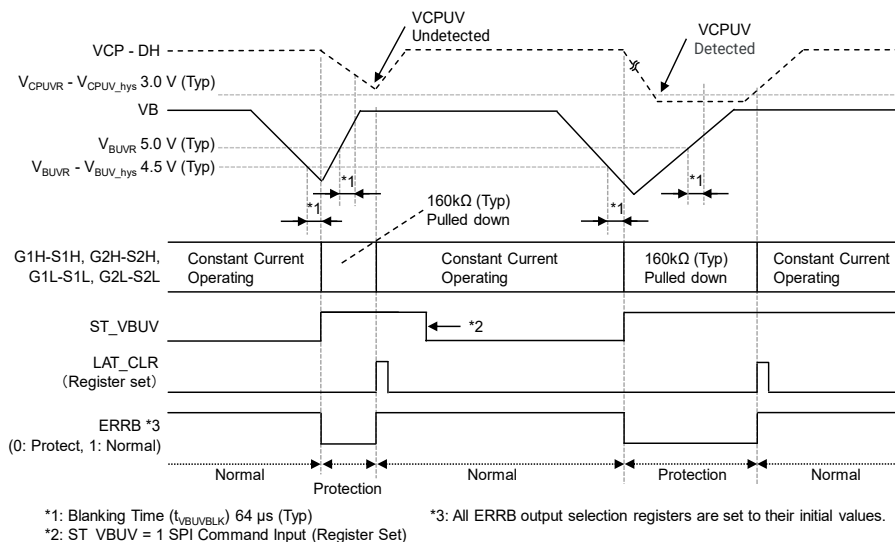


Figure 27. VB Undervoltage Protection Timing Chart (LAT_VBUV = 1)

VB Overvoltage Protection (VBOV)

This protect function monitors the VB pin for fault overvoltage behavior and performs VBOV protection operation should it detect said fault behavior. When register VBOV_SEL = 0, a VBOV fault is detected when the voltage applied to the VB pin exceeds (V_{BOVD1}) = 22.0 V (Typ), and when register VBOV_SEL = 1, a VBOV fault is detected when the voltage applied to the VB pin exceeds (V_{BOVD2}) = 32.5 V (Typ).

When register VBOV_SEL = 0, the detection is released when the voltage applied to the VB pin falls below ($V_{BOVD1} - V_{BOV_hys}$) = 21.0 V (Typ), and when register VBOV_SEL = 1, the detection is released when the voltage applied to the VB pin falls below ($V_{BOVD2} - V_{BOV_hys}$) = 31.5 V (Typ). A blanking time of 64 μ s (Typ) is provided to prevent false detection due to noise. If this fault behavior is detected, the gate driver output is protected and the charge pump output is stopped.

The gate driver output protection operation differs depending on the drive mode (set by the register MODE_SEL). When MODE_SEL = 0 (independent control mode), the gate driver output is pulled down with 160 k Ω (Typ).

MODE_SEL = 1 (H-bridge control mode), the gate driver output operates as a short brake. At this time, the protect function sets the status register ST_VBOV to '1'. How the protection operation is released differs depending on the setting value of the register LAT_VBOV.

When the register LAT_VBOV = 0, if the charge pump circuit does not detect a reduced voltage when the VBOV fault is released, the gate driver output will recover automatically. If the charge pump circuit has detected a reduced voltage, the gate driver output will recover by starting the charge pump circuit. To start the charge pump circuit, the register LAT_CLR = 1 must be set.

When the register LAT_VBOV = 1, the gate driver output will continue the protection operation even if VBOV is no longer detected. To release the protection operation state, set the register LAT_CLR = 1 via SPI write. This will release the protection operation, start the charge pump circuit, and restore the gate driver output. However, while an VBOV is still detected, the protection operation will not be released even if LAT_CLR = 1 is set. Also, after setting LAT_CLR = 1, the register LAT_CLR is automatically initialized to LAT_CLR = 0.

The value of the status register ST_VBOV can be reset by writing ST_VBOV = 1.

Global Status: OVD

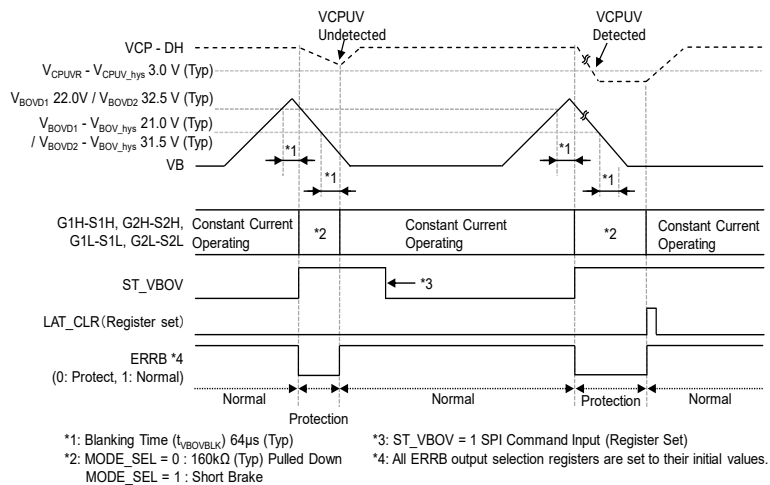


Figure 28. VB Overvoltage Protection Timing Chart (LAT_VBOV = 0)

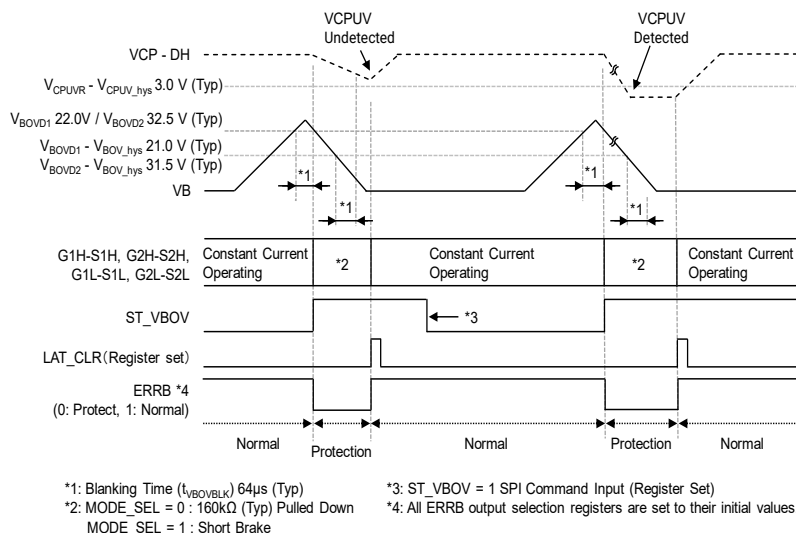


Figure 29. VB Overvoltage Protection Timing Chart (LAT_VBOV = 1)

VCP Undervoltage Protection (VCPUV)

This protect function monitors the VCP pin for fault undervoltage behavior and performs VCPUV protection operation should it detect the fault undervoltage behavior. When the voltage difference between the VCP and DH pins falls below $(V_{\text{CPUVR}} - V_{\text{CPUV_hys}}) = 3.0 \text{ V}$ (Typ), a VCPUV fault is detected, and when it rises to $(V_{\text{CPUVR}}) = 3.2 \text{ V}$ (Typ) or more, it is released. A blanking time of $64 \mu\text{s}$ (Typ) is provided to prevent false detections due to noise. If this fault behavior is detected, the gate driver output is protected and the charge pump output is stopped. The gate driver output protection operation differs depending on the drive mode (set by the MODE_SEL register).

When MODE_SEL = 0 (independent control mode), the gate driver outputs of G1H and G2H are set to Low and the charge pump output is stopped.

When MODE_SEL = 1 (H-bridge control mode), the gate driver outputs of G1H and G2H are set to Low and the gate driver outputs of G1L and G2L are set to High, and the charge pump output is stopped. At this time, the protect function sets the status register ST_VCPUV to '1'. For VCPUV, the gate driver output will continue to maintain protection even after the VCPUV detection is released. To release the protection state, set the register LAT_CLR = 1 via SPI write. This will release the protection, start the charge pump circuit, and restore the gate driver output. However, while VCPUV is still being detected, setting LAT_CLR = 1 will not release the protection. Also, after setting LAT_CLR = 1, the value of the register LAT_CLR is automatically initialized to LAT_CLR = 0. The value of the status register ST_VCPUV can be reset by writing ST_VCPUV = 1.

Global Status: UVD

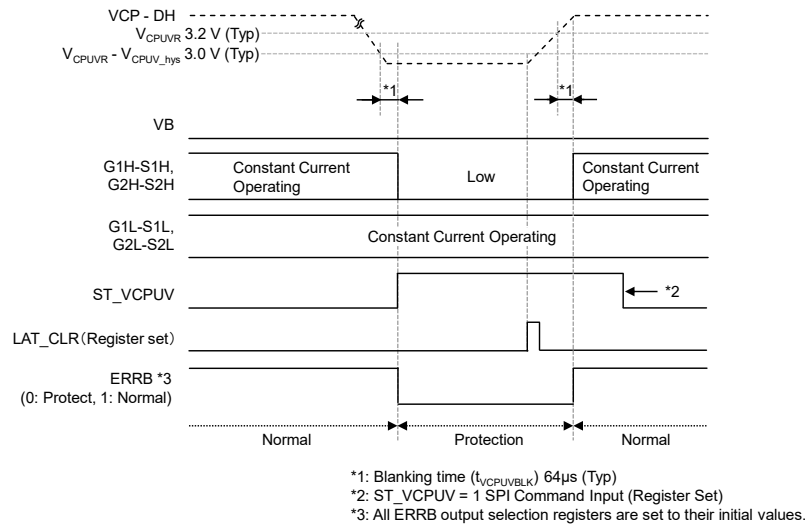


Figure 30. VCP Undervoltage Protection Timing Chart (MODE_SEL = 0)

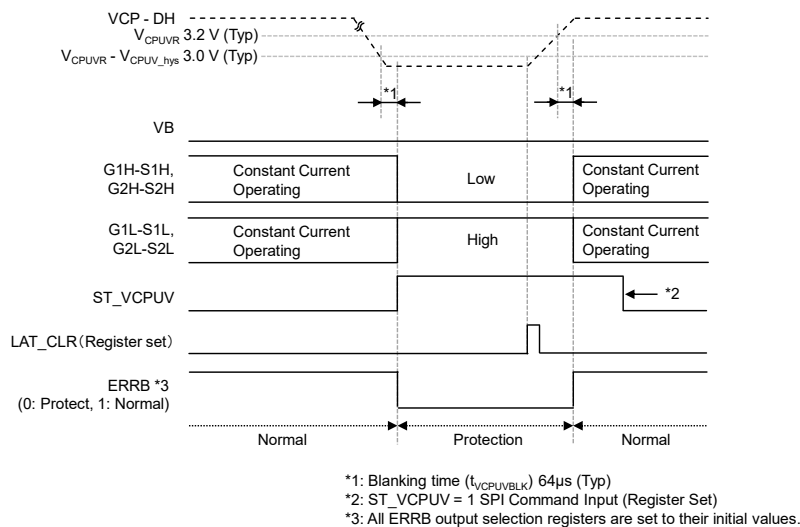


Figure 31. VCP Undervoltage Protection Timing Chart (MODE_SEL = 1)

DH Undervoltage Protection (DHUV)

This protect function monitors the DH pin for fault undervoltage behavior and performs DHUV protection should it detect the fault undervoltage behavior. If the voltage applied to the DH pin falls below ($V_{DHUV} = 4.9\text{ V (Typ)}$), a DHUV fault is detected, and if it exceeds ($V_{DHUV} = 4.9\text{ V (Typ)}$), it is released. A blanking time (set in the DHUV_FLT register) is also provided to prevent noise and false detection during gate driver output transitions. If this fault behavior is detected, the gate driver output is set to low and the charge pump output is also stopped. At this time, the protect function sets the status register ST_DHUV to '1'. After this has been detected, the gate driver output maintains the protection operation state for the time set in the Protect Period (protection operation period. Set in the DHUV_FLT register). The operation when DHUV is released depends on the setting of the LAT_DHUV register.

When the register LAT_DHUV = 0, if the fault undervoltage behavior is no longer detected and the charge pump circuit does not detect a reduced voltage after DHUV fault is released after the Protect Period, the gate driver output will recover automatically. If the charge pump circuit detects a reduced voltage, the gate driver output will recover by starting the charge pump circuit. To start the charge pump circuit, the register LAT_CLR = 1 must be set.

When the register LAT_DHUV = 1, the gate driver output and charge pump output will continue the protection operation even if the DHUV detection is released after the Protect Period. To release the protection operation state, set the register LAT_CLR = 1 via SPI write. This will release the protection operation, start the charge pump circuit, and recover the gate driver output. However, during the Protect Period or while DHUV is detected, the protection operation will not be released even if LAT_CLR = 1 is set. In addition, the value of the register LAT_CLR is automatically initialized to LAT_CLR = 0 after LAT_CLR = 1 is set. The status register ST_DHUV can be reset by writing ST_DHUV = 1.

Global Status: UVD

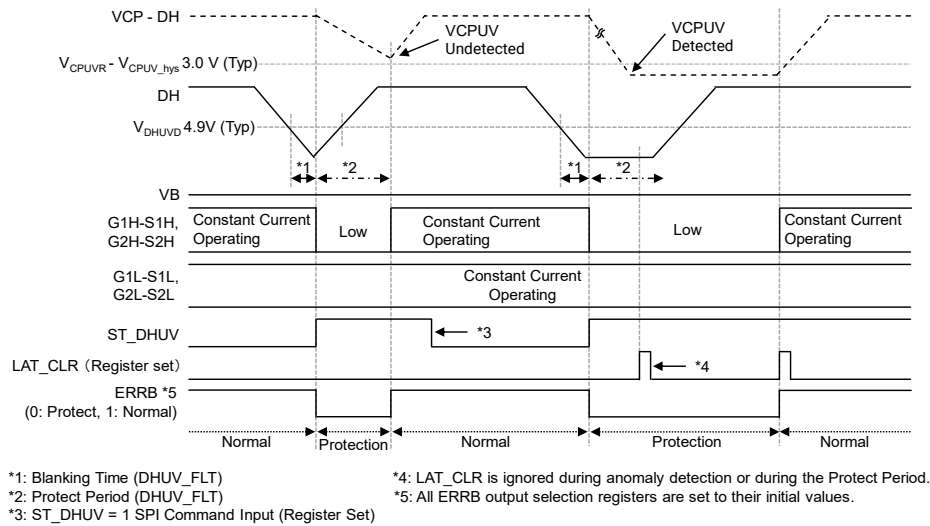


Figure 32. DH Undervoltage Protection Timing Chart (LAT_DHUV = 0)

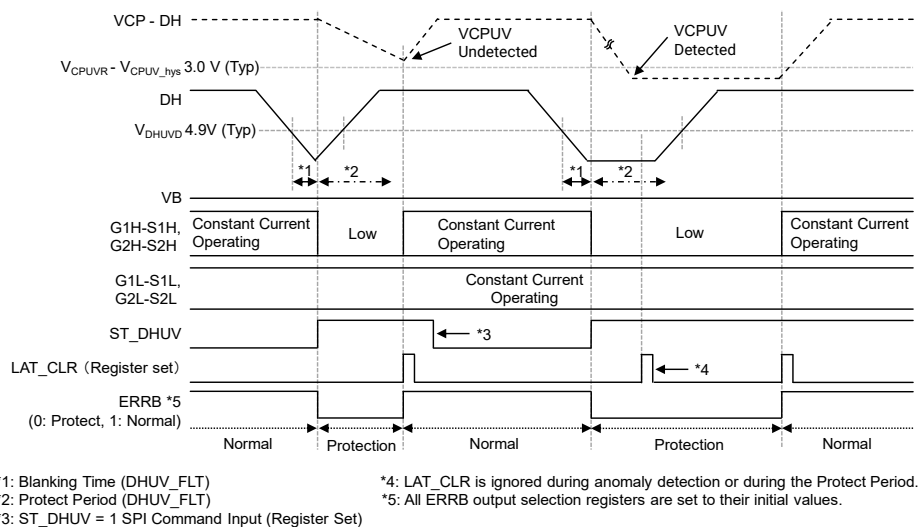


Figure 33. DH Undervoltage Protection Timing Chart (LAT_DHUV = 1)

Drain-Source Overvoltage (Overcurrent) Protection (VDSOV)

This protect function monitors the drain and source of the external MOS FET for fault overvoltage (overcurrent) behavior between and performs protective operation. The overvoltage detection and protection operation is independent for each gate driver output (G1H, G1L, G2H, G2L), and each individual protect function operates separately. When an overcurrent flows between the drain and source and the drain-source voltage exceeds the detection voltage V_{VDSx} (set by registers VDS_Hx, VDS_Lx), a VDS fault is detected, and when it falls below V_{VDSx} , it is released. In addition, a blanking time (set by registers FET_GxH_FLT, FET_GxL_FLT) is provided to prevent noise and false detection during gate driver output transitions. When this fault behavior is detected, the gate driver output of only the detected output is set to Low. At this time, the status register ST_VDS_Hx = 1 (or ST_VDS_Lx = 1) corresponding to the gate driver output where the fault behavior was detected is set. After this has been detected, the gate driver output continues protection operation for the period set in the Protect Period (protection operation period. Set using the registers FET_GxH_FLT and FET_GxL_FLT). The operation when VDSOV is released depends on the setting values of the registers LAT_VDS_Hx and LAT_VDS_Lx.

When the register LAT_VDS_Hx = 0 (or LAT_VDS_Lx = 0), the gate driver output will automatically recover if VDSOV is no longer detected after the Protect Period. When the register LAT_VDS_Hx = 1 (or LAT_VDS_Lx = 1), the gate driver output will continue protection operation even if VDSOV fault is no longer detected after the Protect Period. To release the protection operation state, set the register LAT_CLR = 1 to reset and release the protection operation.

The status register can be reset by writing ST_VDS_Hx = 1 (or ST_VDS_Lx = 1). The register LAT_CLR is automatically initialized to LAT_CLR = 0 after LAT_CLR = 1 is set. However, during the Protect Period or while VDSOV is still being detected, the protection operation will not be released even if LAT_CLR = 1 is set. (x = 1, 2)

Overcurrent protection is a function to prevent the destruction of the IC due to output shorts, etc., but if the overcurrent state continues, the IC may heat up or deteriorate, so if the overcurrent state continues, take measures such as putting the IC into standby mode.

Global Status: OCD

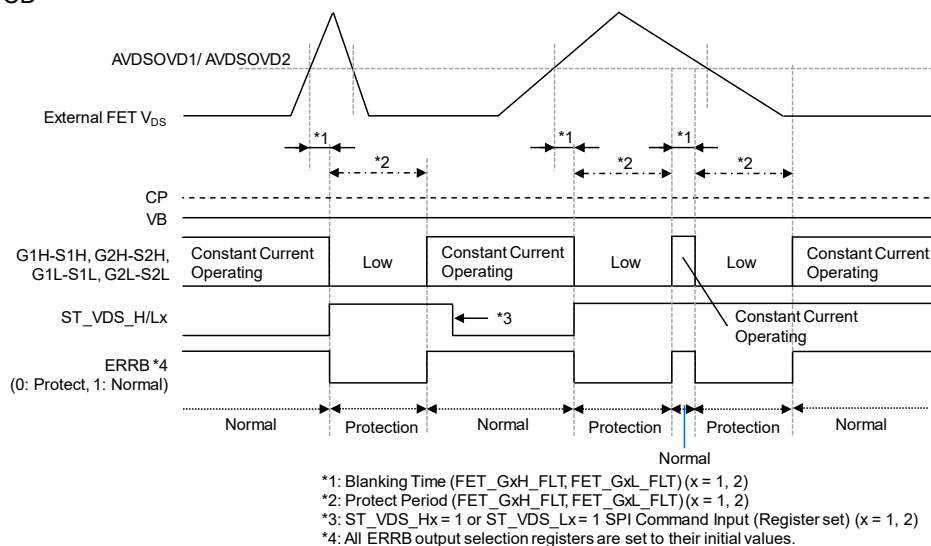


Figure 34. Drain-Source Overvoltage Protection Timing Chart (LAT_VDS_Hx = 0, LAT_VDS_Lx = 0)

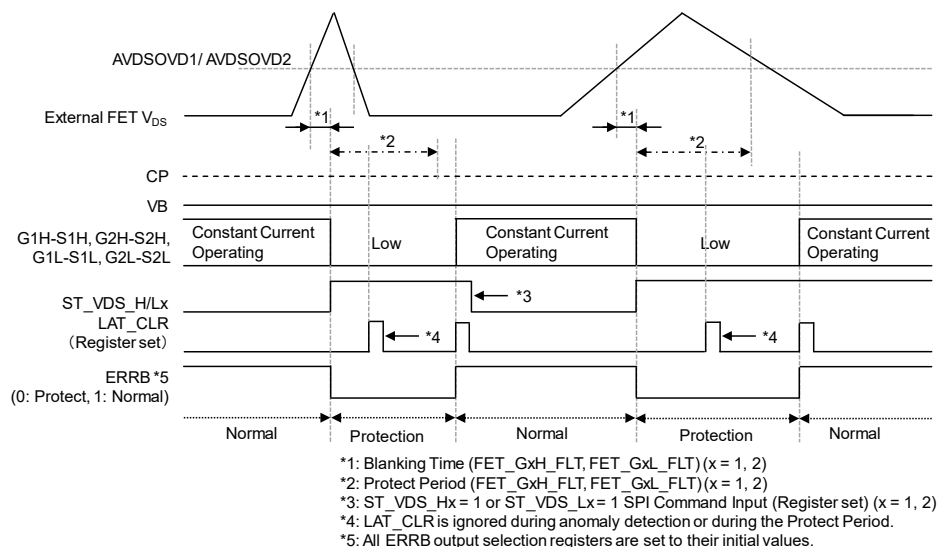


Figure 35. Drain-Source Overvoltage Protection Timing Chart (LAT_VDS_Hx = 1, LAT_VDS_Lx = 1)

Shunt Resistor Overvoltage Protection (RDET)

This protect function monitors the external shunt resistor for fault overvoltage (overcurrent) behavior and performs RDET protection operation should it detect it. The RDET detection and protection operations are independent for the gate driver outputs G1L and G2L, and each operates separately. When an overcurrent flows through the shunt resistor and the voltage between the AINxP-AINxN pins exceeds the detection voltage V_{RDET_x} (set by the register $RDET_x$), an RDET fault is detected, and when it becomes smaller than V_{RDET_x} , it is released. In addition, a blanking time (set by the registers FET_G1L_FLT and FET_G2L_FLT) is provided to prevent noise and false detection during gate driver output transition.

When this fault behavior is detected between the AIN1P-AIN1N pins, the gate driver output G1L is set to low, and when fault is detected between the AIN2P-AIN2N pins, the gate driver output G2L is set to low. At this time, the protect function sets the status register ST_VRDET_x to '1' corresponding to the AINxP-AINxN pins where the RDET fault was detected. After the fault overvoltage (overcurrent) behavior is detected, the gate driver output continues the protection operation for the time set in the Protect Period (protection operation period. Set using the registers FET_G1L_FLT and FET_G2L_FLT). The operation when RDET is released depends on the setting value of the register LAT_VRDET_x .

When the register $LAT_VRDET_x = 0$, if RDET fault is no longer detected after the Protect Period, the gate driver output will self-recover, and if the fault behavior continues, the protection operation will continue.

When the register $LAT_VRDET_x = 1$, the gate driver output will continue the protection operation even if the RDET fault is released after the Protect Period. To release the protection operation state, set the register $LAT_CLR = 1$ via SPI write. However, during the Protect Period or while RDET fault is still detected, the protection operation will not be released even if $LAT_CLR = 1$ is set. The value of the status register can be reset by setting $ST_VRDET_x = 1$. The register LAT_CLR is automatically initialized to $LAT_CLR = 0$ after setting $LAT_CLR = 1$. ($x = 1, 2$)

As with the drain-source overvoltage protection, if an overcurrent state continues, the IC may heat up or deteriorate, so if an overcurrent state continues, take measures such as putting the IC into standby mode.

Global Status: OCD

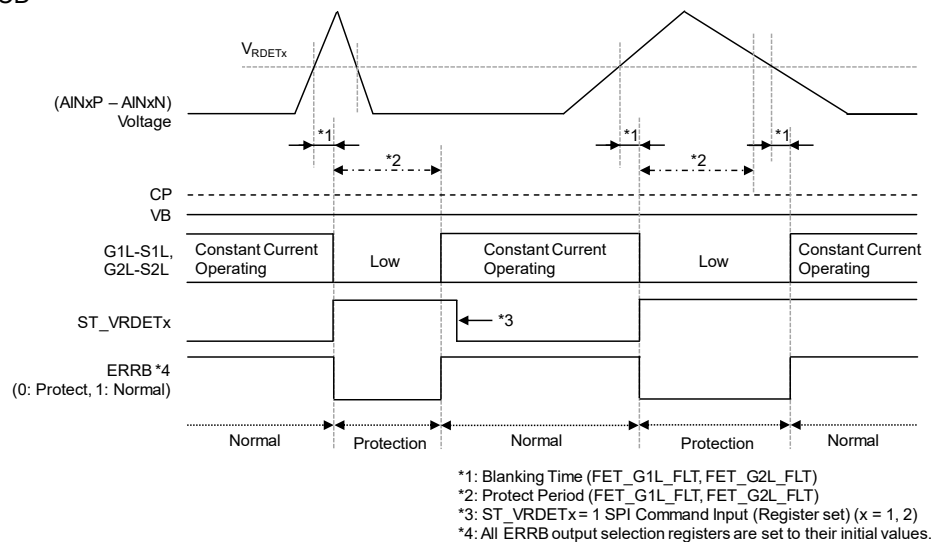


Figure 36. Shunt Resistor Overvoltage Protection Timing Chart ($LAT_VRDET_x = 0$)

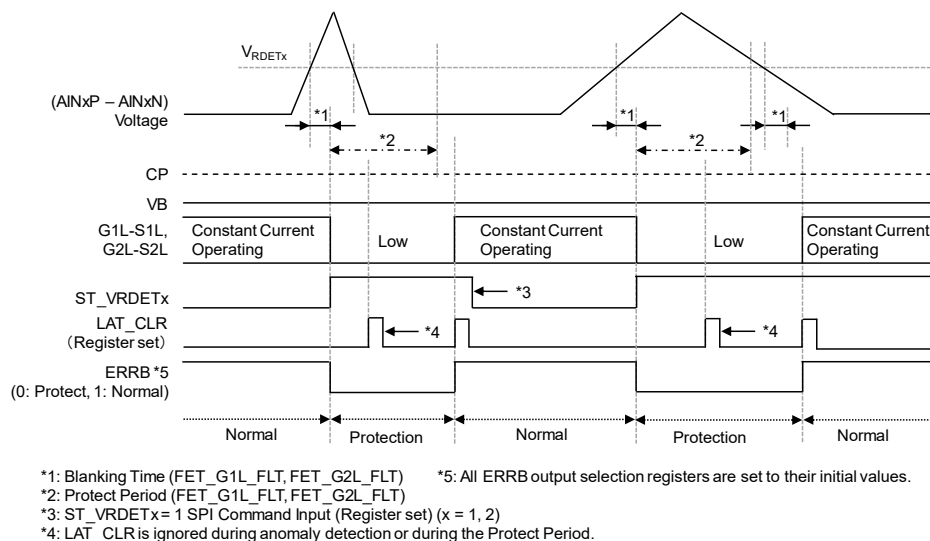


Figure 37. Shunt Resistor Overvoltage Protection Timing Chart ($LAT_VRDET_x = 1$)

Thermal Shutdown (TSD)

This protect function monitors for fault high IC temperature and performs TSD protective operation if the fault high IC temperature is detected. If the junction temperature rises and exceeds ($T_{TSD} = 175\text{ °C}$ (Typ)), a TSD fault is detected, and it is released when the junction temperature falls below ($T_{TSD} - T_{TSD_hys} = 160\text{ °C}$ (Typ)). If this fault behavior is detected, the gate driver output is pulled down to 160 k Ω (Typ) and the charge pump output is also stopped. At this time, the protect function sets the status register ST_TSD to '1'. How the protection operation is released depends on the setting value of the register LAT_TSD.

When the register LAT_TSD = 0, if the charge pump circuit has not detected a reduced voltage when the TSD fault detection is released, the gate driver output will recover automatically. If the charge pump circuit has detected a reduced voltage, the gate driver output will recover by starting the charge pump circuit. To start the charge pump circuit, the register LAT_CLR = 1 must be set.

When the register LAT_TSD = 1, the gate driver output will continue the protection operation even if the TSD fault detection is released. To release the protection operation state, set the register LAT_CLR = 1 via SPI write, which will release the protection operation, start the charge pump circuit, and restore the gate driver output. However, while the TSD fault is still detected, the protection operation will not be released even if LAT_CLR = 1 is set. The value of the status register ST_TSD can be reset by setting ST_TSD = 1.

After setting LAT_CLR = 1, the register LAT_CLR is automatically initialized to LAT_CLR = 0.

Global Status: OT

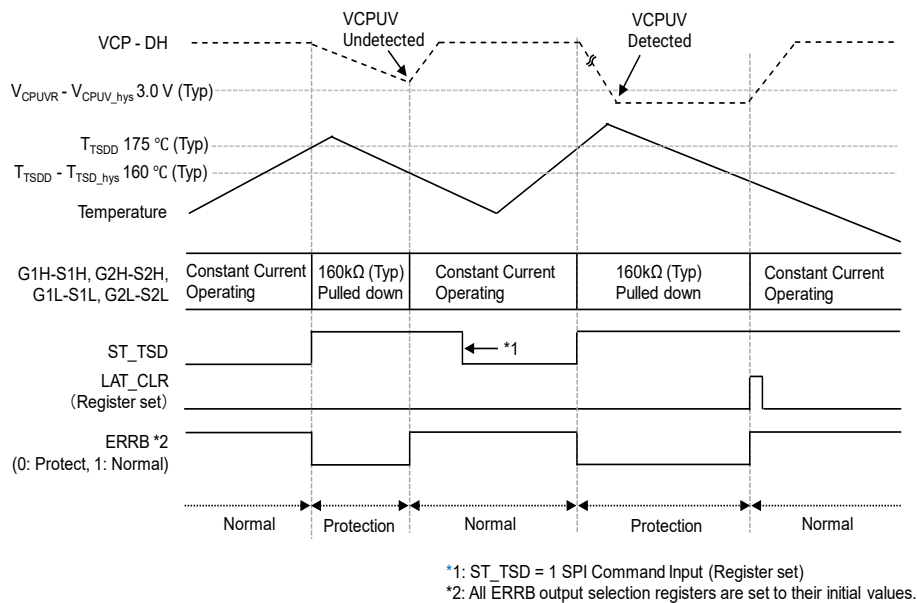


Figure 38. Thermal Shutdown Timing Chart (LAT_TSD = 0)

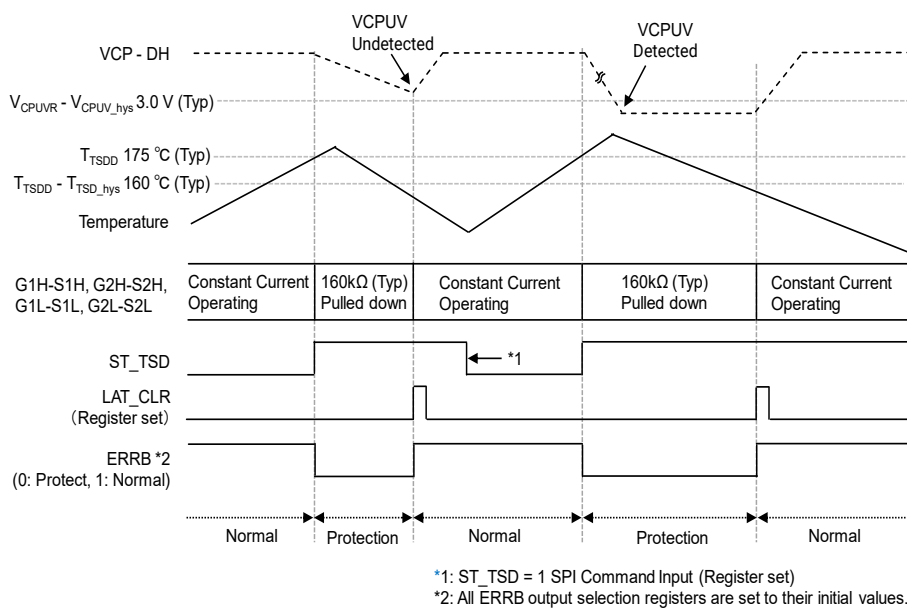


Figure 39. Thermal Shutdown Timing Chart (LAT_TSD = 1)

Thermal Warning (TW)

This protect function monitors the IC temperature and notifies if the temperature has reached a certain level. If the junction temperature rises and exceeds (T_{TWD}) = 132.5 °C (Typ), a TW fault detected, and if it falls below ($T_{TWD} - T_{TW_hys}$) = 122.5 °C (Typ), it is cleared. If a TW fault is detected, the IC is notified and it sets the status register ST_TW to '1'. The status register ST_TW can be reset by writing ST_TW = 1. Even if this fault or fault behavior is detected, the gate driver output and charge pump continues to operate.

The operation of the error notification signal (ERRB) depends on the setting value of the register LAT_TW.

When the register LAT_TW = 0, the signal goes low when a TW fault is detected, and the ERRB signal automatically returns to normal when it is cleared.

When the register LAT_TW = 1, the signal goes low when a TW fault is detected, and the signal continues to go low even after it has been cleared. The fault notification (low output) can be released when no thermal warning is detected by setting the register LAT_CLR = 1. After setting LAT_CLR = 1, the register LAT_CLR is automatically initialized to LAT_CLR = 0.

Global Status: OT

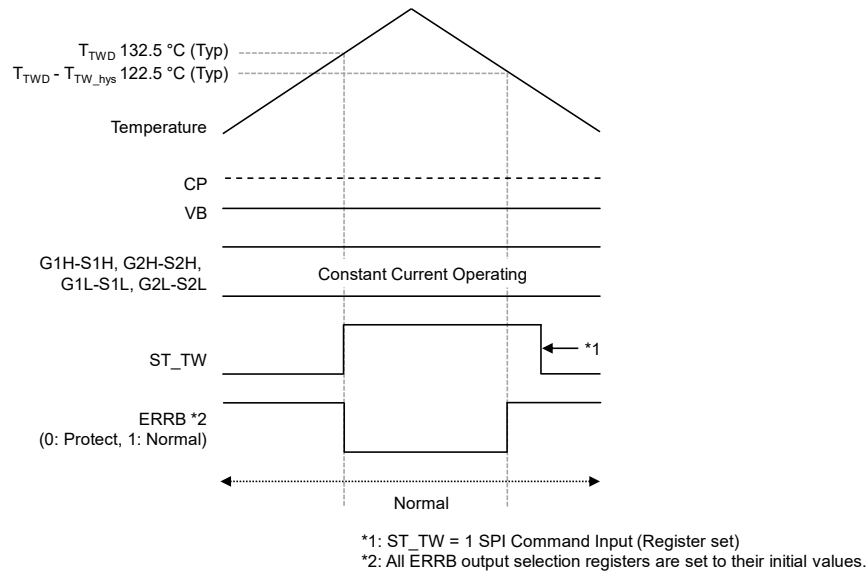


Figure 40. Thermal Warning Timing Chart (LAT_TW = 0)

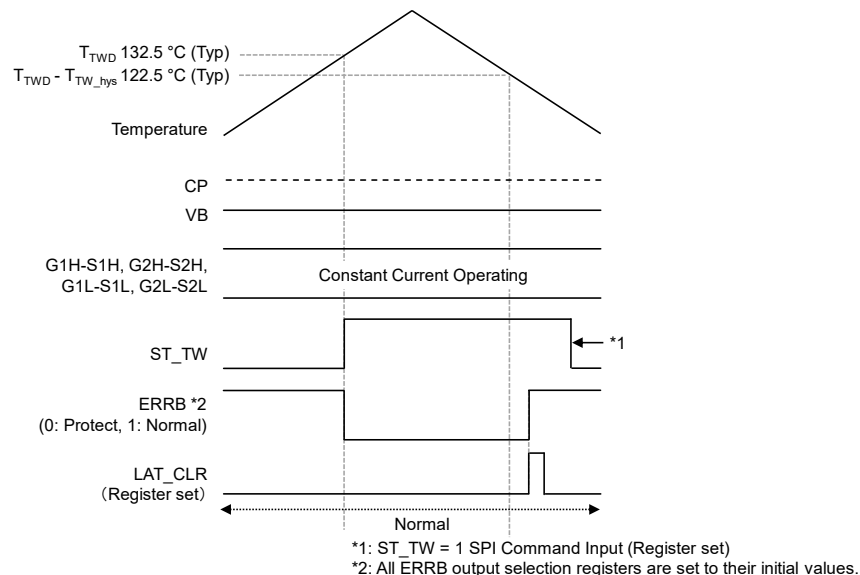


Figure 41. Thermal Warning Timing Chart (LAT_TW = 1)

Gate-Source Undervoltage Fault Detection (VGSUV)

When the gate driver output is set to High, this protect function monitors the reduced voltage between the gate and source of the external MOS FET and performs VGSUV protection operation if it is detected. The VGSUV detection and protection operations are independent for each gate driver output G1H, G1L, G2H, G2L, and each one operates separately. When the upper and lower gate driver output High voltages (V_{GxHHx} , V_{GxLHx}) are being output, if the gate-source voltage of the external MOS FET falls below (V_{GSUVd}) = 3.0 V (Typ), a VGSUV fault is detected, and when it exceeds (V_{GSUVd}) = 3.0 V (Typ), the VGSUV fault detection is released. In addition, a blanking time (set by registers FET_GxH_FLT, FET_GxL_FLT) is provided to prevent noise and false detection during gate driver output transitions. When a VGSUV fault is detected, only the gate driver output where the fault or fault behavior was detected goes Low. At this time, the status register ST_VGS_Hx_UV (or ST_VGS_Lx_UV) corresponding to the gate driver output where the VGSUV fault was detected is set to '1'. After it has been detected, the gate driver output continues the protection operation for the time set in the Protect Period (protection operation period. Set using the registers FET_GxH_FLT and FET_GxL_FLT).

How this protect operation is released depends on the setting values of the registers LAT_VGS_Hx and LAT_VGS_Lx. When register LAT_VGS_Hx (or LAT_VGS_Lx) = 0, if VGSUV fault is released after the Protect Period, the gate driver output will recover automatically, and if the detection of the VGSUV fault continues, protection operation will continue. (The timing of self-recovery depends on the time set in the Protect Period). When the register LAT_VGS_Hx (or LAT_VGS_Lx) = 1, the gate driver output continues the protection operation even if the VGSUV fault is released after the Protect Period. To release the protection operation state, set the register LAT_CLR = 1 via SPI write to release the protection operation. However, during the Protect Period or while VGSUV fault is still being detected, the protection operation will not be released even if LAT_CLR = 1 is set.

The value of the status register can be reset by writing ST_VGS_Hx_UV = 1 (or ST_VGS_Lx_UV = 1). The value of the register LAT_CLR is automatically initialized to LAT_CLR = 0 after LAT_CLR = 1 is set.

(x = 1, 2)

Global Status: VGS

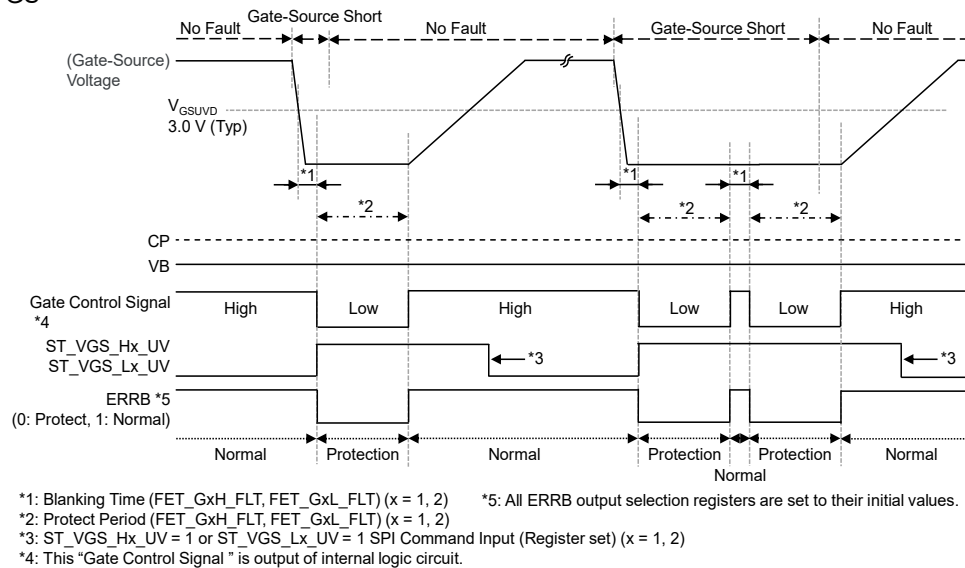


Figure 42. Gate-Source Undervoltage Fault Detection Timing Chart (LAT_VGS_Hx = 0, LAT_VGS_Lx = 0)

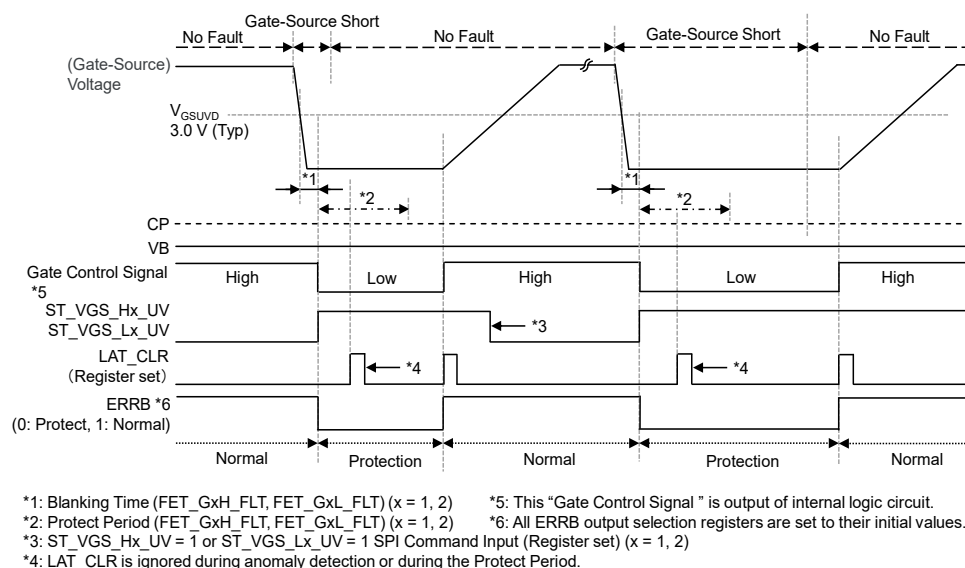


Figure 43. Gate-Source Undervoltage Fault Detection Timing Chart (LAT_VGS_Hx = 1, LAT_VGS_Lx = 1)

Gate-Source Overvoltage Fault Detection (VGSOV)

When the gate output is set to low, this protect function of the device monitors the overvoltage between the gate and source of the external MOS FET and performs VGSOV protection operation if it is detected. The VGSOV detection and protection operations are independent for each gate driver output G1H, G1L, G2H, G2L, and each one operates separately. When the upper and lower gate driver output low voltages (V_{GxHLx} , V_{GxLLx}) are being output, if the gate-source voltage of the external MOS FET exceeds (V_{GSOVD}) = 1.2 V (Typ), a VGSOV fault is detected. When it falls below (V_{GSOVD}) = 1.2 V (Typ), the VGSOV fault detection is released. In addition, a blanking time (set by registers FET_GxH_FLT, FET_GxL_FLT) is provided to prevent noise and false detection during gate driver output transitions. When a VGSOV fault is detected, only the gate driver output where the fault or fault behavior was detected is pulled down to 160 k Ω (Typ). At this time, the status register ST_VGS_Hx_OV (or ST_VGS_Lx_OV) corresponding to the gate driver output where the VGSOV fault was detected is set to '1'. After it has been detected, the gate driver output continues the protection operation for the time set in the Protect Period (protection operation period). Set using the registers FET_GxH_FLT and FET_GxL_FLT).

How this protection operation is released depends on the setting values of the registers LAT_VGS_Hx and LAT_VGS_Lx. When register LAT_VGS_Hx (or LAT_VGS_Lx) = 0, if VGSOV fault is released after the Protect Period, the gate driver output will recover automatically, and if the detection of the VGSOV fault continues, protection operation will continue. (The timing of self-recovery depends on the time and timing set in the Protect Period.) When the register LAT_VGS_Hx (or LAT_VGS_Lx) = 1, the gate driver output continues the protection operation even if the VGSOV fault is released after the Protect Period. To release the protection operation state, set the register LAT_CLR = 1 via SPI write to release the protection operation. However, during the Protect Period or while VGSOV fault is still being detected, the protection operation will not be released even if LAT_CLR = 1 is set.

The value of the status register can be reset by writing the register ST_VGS_Hx_OV = 1 (or ST_VGS_Lx_OV = 1). The value of the register LAT_CLR is automatically initialized to LAT_CLR = 0 after setting LAT_CLR = 1.

(x = 1, 2)

Global Status: VGS

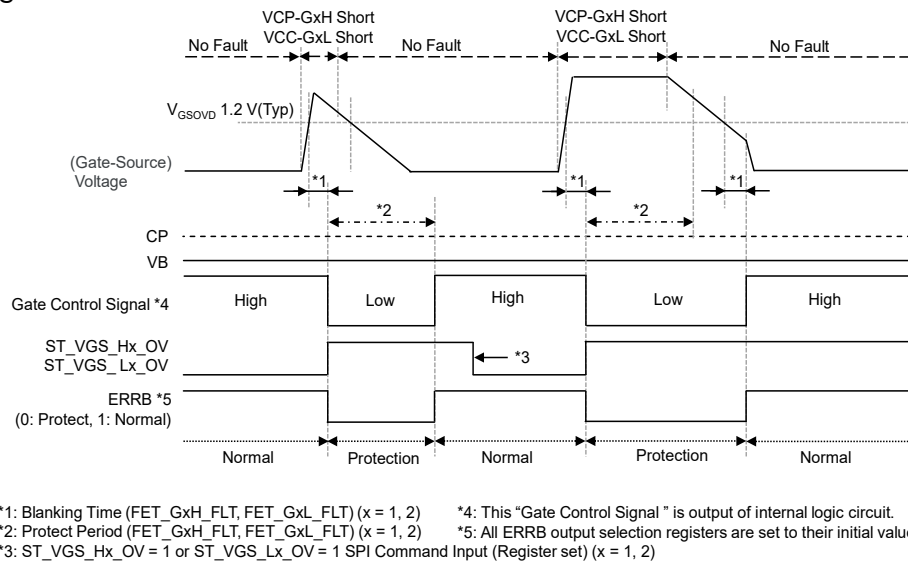


Figure 44. Gate-Source Overvoltage Fault Detection Timing Chart (LAT_VGS_Hx = 0, LAT_VGS_Lx = 0)

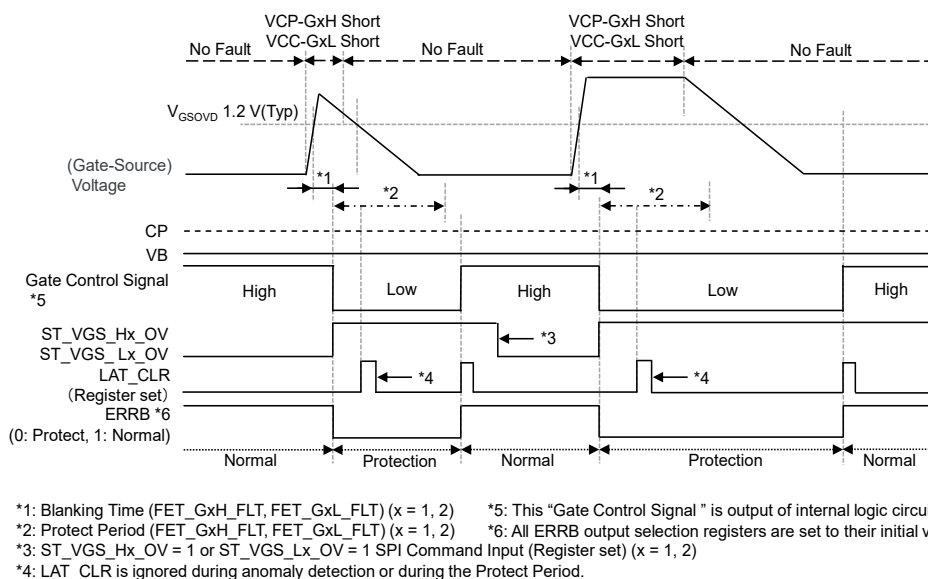


Figure 45. Gate-Source Overvoltage Fault Detection Timing Chart (LAT_VGS_Hx = 1, LAT_VGS_Lx = 1)

Dead Time Protection

The gate-source voltage of the external MOS FET is monitored to prevent the upper and lower MOS FET from being turned on at the same time. In H-bridge control mode, the gate driver control signals GxH and GxL are controlled while monitoring the gate-source voltage. When turning on the upper MOS FET, the upper MOS FET is turned on after it has confirmed that the lower MOS FET is turned off. Conversely, when turning on the lower MOS FET, the lower MOS FET is turned on after it has confirmed that the upper MOS FET is turned off. The monitoring circuit for this gate-source voltage has a comparator delay t_{propa2} , and since the gate-source voltage cannot be monitored accurately during this t_{propa2} time, a dead time of 2 μs (Typ) is forcibly inserted to prevent shoot-through current in the MOS FET, preventing the generation of shoot-through current due to incorrect recognition of the gate driver-source voltage (See [Figure 46. Dead Time Protection Timing Chart \(No VGS Response\)](#)). As a result, there may be a difference in the PWM Duty of the PWM input signal and the motor drive output signal. Note that the signal input to the PWMx pin is synchronized with the internal clock, so a synchronization delay time (t_{syn}) also occurs.

The minimum pulse width of the PWM Low output is the total time t_{pwm1} , which is the time it takes for the gate driver circuit to respond after the control logic circuit turns on the gate driver output control signal (t_{propa1}), the rise and fall times of the gate driver signal, the VGS comparator response time t_{propa2} , the time it takes for the opposite side gate driver circuit to respond (t_{propa1}), the Dead Time protection time $t_{propa2mask}$ 2 μs (Typ), the time it takes for the gate driver circuit to respond (t_{propa1}), and the internal clock synchronization delay time (t_{syn}) of the PWMx pin input signal. (See [Figure 47. Dead Time Protection Timing Chart \(with VGS response\)](#)).

The rise and fall times of the gate driver signals vary depending on the gate driver output current settings (set in registers CUR_SO_HxSEL, CUR_SO_Hx, CUR_SI_HxSEL, CUR_SI_Hx, CUR_SO_LxSEL, CUR_SO_Lx, CUR_SI_LxSEL, CUR_SI_Lx) and the capacitance value of the MOS FET, so please verify these values in your system and determine the PWM frequency and duty before performing PWM control.

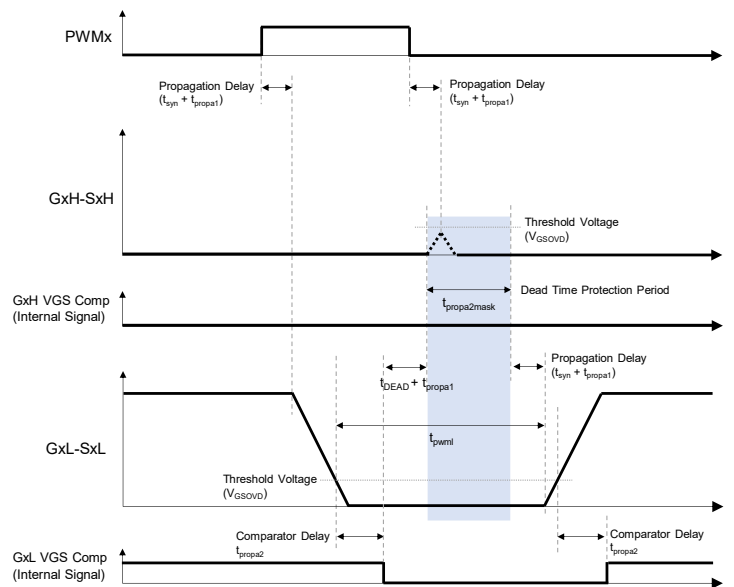


Figure 46. Dead Time Protection Timing Chart (No VGS Response)

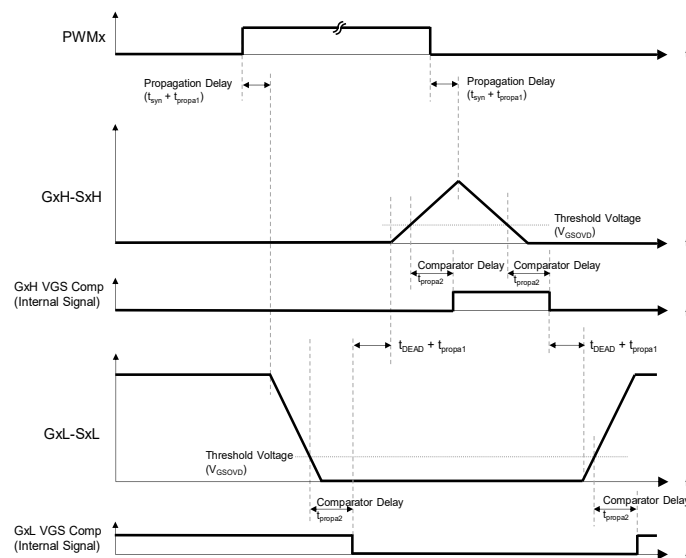


Figure 47. Dead Time Protection Timing Chart (with VGS response)

SPI Transfer Error (SPI_FAIL)

This protect function monitors SPI transfer and protective action is taken. An SPI fail fault is detected if there are other than 16 SCK clock pulses while CSB is low. At this time, the status register ST_SPI = 1 is set. The status register ST_SPI is updated every time CSB rises. The status register ST_SPI can be reset by writing ST_SPI = 1. Note that the gate driver output will not be turned off even if fault is detected.

Global Status: SPI_FL

Register Map

The table below lists the register map. The registers can be set by SPI.

Description	R/W	Address	DATA bit								Initial Value
	15	14-8	7	6	5	4	3	2	1	0	
Software Reset	W	00h	Software Reset								00h
Fault Protection State Reset	W	01h	-	-	-	-	-	-	LAT_CLR	-	00h
Enable Settings	R/W	02h	-	-	-	-	-	CP_EN	DRV_GHI $\bar{Z}$	CS_EN	02h
Mode Settings	R/W	03h	G2H_SEL	G2H_FIX	G2L_SEL	G2L_FIX	G1H_SEL	G1H_FIX	G1L_SEL	G1L_FIX	00h
Fault Status1	R/W	04h	ST_VCPUV	ST_DHUV	ST_VBOV	ST_VBUV	ST_VCOV	ST_VCUV	ST_TW	ST_TSD	04h
Fault Status2	R/W	05h	ST_VDS_H2	ST_VDS_L2	ST_VDS_H1	ST_VDS_L1	ST_SPI	-	ST_VRDET2	ST_VRDET1	00h
Fault Status3	R/W	06h	ST_VGS_H2_OV	ST_VGS_L2_OV	ST_VGS_H2_UV	ST_VGS_L2_UV	ST_VGS_H1_OV	ST_VGS_L1_OV	ST_VGS_H1_UV	ST_VGS_L1_UV	00h
Latch Settings1	R/W	07h	-	LAT_DHUV	LAT_VBOV	LAT_VBUV	LAT_VCOV	-	LAT_TW	LAT_TSD	00h
Latch Settings2	R/W	08h	LAT_VDS_H2	LAT_VDS_L2	LAT_VDS_H1	LAT_VDS_L1	-	-	LAT_VRDET2	LAT_VRDET1	00h
Latch Settings3	R/W	09h	-	-	LAT_VGS_H2	LAT_VGS_L2	-	-	LAT_VGS_H1	LAT_VGS_L1	00h
Mask Settings1	R/W	0Ah	MASK_VCPUV	MASK_DHUV	MASK_VBOV	MASK_VBUV	MASK_VCOV	-	-	-	00h
Mask Settings2	R/W	0Bh	MASK_VDS_H2	MASK_VDS_L2	MASK_VDS_H1	MASK_VDS_L1	-	-	MASK_VRDET2	MASK_VRDET1	00h
Mask Settings3	R/W	0Ch	-	-	MASK_VGS_H2	MASK_VGS_L2	-	-	MASK_VGS_H1	MASK_VGS_L1	00h
Flag Settings1	R/W	0Dh	FLG_VCPUV	FLG_DHUV	FLG_VBOV	FLG_VBUV	FLG_VCOV	-	FLG_TW	FLG_TSD	FBh
Flag Settings2	R/W	0Eh	FLG_VDS_H2	FLG_VDS_L2	FLG_VDS_H1	FLG_VDS_L1	FLG_SPI	-	FLG_VRDET2	FLG_VRDET1	FBh
Flag Settings3	R/W	0Fh	-	-	FLG_VGS_H2	FLG_VGS_L2	-	-	FLG_VGS_H1	FLG_VGS_L1	33h

Register Map - continued

Description	R/W	Address	DATA bit								Initial Value
	15	14-8	7	6	5	4	3	2	1	0	
Output Current Settings1	R/W	10h	CUR_SO_H1SEL	CUR_SO_H1 [2]	CUR_SO_H1 [1]	CUR_SO_H1 [0]	CUR_SI_H1SEL	CUR_SI_H1 [2]	CUR_SI_H1 [1]	CUR_SI_H1 [0]	FFh
Output Current Settings2	R/W	11h	CUR_SO_L1SEL	CUR_SO_L1 [2]	CUR_SO_L1 [1]	CUR_SO_L1 [0]	CUR_SI_L1SEL	CUR_SI_L1 [2]	CUR_SI_L1 [1]	CUR_SI_L1 [0]	FFh
Output Current Settings3	R/W	12h	CUR_SO_H2SEL	CUR_SO_H2 [2]	CUR_SO_H2 [1]	CUR_SO_H2 [0]	CUR_SI_H2SEL	CUR_SI_H2 [2]	CUR_SI_H2 [1]	CUR_SI_H2 [0]	FFh
Output Current Settings4	R/W	13h	CUR_SO_L2SEL	CUR_SO_L2 [2]	CUR_SO_L2 [1]	CUR_SO_L2 [0]	CUR_SI_L2SEL	CUR_SI_L2 [2]	CUR_SI_L2 [1]	CUR_SI_L2 [0]	FFh
Analog Settings1	R/W	14h	MODE_SEL	VBOV_SEL	-	CHP_FREQ_DFUE	-	CSAMP_REF	CSAMP_GAIN [1]	CSAMP_GAIN [0]	01h
Dead Time Setting	R/W	16h	-	-	-	-	TDEAD [3]	TDEAD [2]	TDEAD [1]	TDEAD [0]	00h
VDS Settings1	R/W	17h	-	VDS_H1 [2]	VDS_H1 [1]	VDS_H1 [0]	-	VDS_L1 [2]	VDS_L1 [1]	VDS_L1 [0]	44h
VDS Settings2	R/W	18h	-	VDS_H2 [2]	VDS_H2 [1]	VDS_H2 [0]	-	VDS_L2 [2]	VDS_L2 [1]	VDS_L2 [0]	44h
RDET Settings	R/W	19h	-	RDET2 [2]	RDET2 [1]	RDET2 [0]	-	RDET1 [2]	RDET1 [1]	RDET1 [0]	44h
VDS, VGS, RDET Blanking Settings1	R/W	1Ah	FET_G1H_FLT [3]	FET_G1H_FLT [2]	FET_G1H_FLT [1]	FET_G1H_FLT [0]	FET_G1L_FLT [3]	FET_G1L_FLT [2]	FET_G1L_FLT [1]	FET_G1L_FLT [0]	33h
VDS, VGS, RDET Blanking Settings2	R/W	1Bh	FET_G2H_FLT [3]	FET_G2H_FLT [2]	FET_G2H_FLT [1]	FET_G2H_FLT [0]	FET_G2L_FLT [3]	FET_G2L_FLT [2]	FET_G2L_FLT [1]	FET_G2L_FLT [0]	33h
DHUV Blanking Setting	R/W	1Ch	-	-	-	-	DHUV_FLT [3]	DHUV_FLT [2]	DHUV_FLT [1]	DHUV_FLT [0]	00h
Static OPEN/SHORT Check	W	1Eh	-	-	-	-	OS_EN	AUTO_OS_START	SET_OS2	SET_OS1	00h
Static OPEN/SHORT Status	R	1Fh	-	ST_OSCHK_STEP [2]	ST_OSCHK_STEP [1]	ST_OSCHK_STEP [0]	ST_OSCHK_END	ST_OSCHK_FAIL	ST_OSCHK2	ST_OSCHK1	00h

Address = 00h <Software Reset>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
00h	W	Software Reset							
Initial Value	00h	0	0	0	0	0	0	0	0

Software reset command. Initialization of the digital block is performed. All registers are initialized. 5Ah of data is sent to perform a software reset. When EN = H, the software reset command can be used.

Address = 01h <Fault Protection State Reset>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
01h	W	-	-	-	-	-	-	LAT_CLR	-
Initial Value	00h	0	0	0	0	0	0	0	0

LAT_CLR: Set LAT_CLR = 1 if you want to return from protection state after fault is detected.

The value of LAT_CLR is automatically initialized to '0' after being set to '1'. Note that while fault is being detected or during protection operation due to the Protect Period, the protection state will not be released even if LAT_CLR = 1 is set. Protection operation will continue.

Address = 02h <Enable Settings>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
02h	R/W	-	-	-	-	-	CP_EN	DRV_GHIZ	CS_EN
Initial Value	02h	0	0	0	0	0	0	1	0

CP_EN: Charge Pump enable

0: Boost operation is stopped and G1H and G2H are pulled down by 160 kΩ (Typ).

G1L and G2L operate according to the setting.

1: Starts boost operation, and G1H and G2H can also output.

DRV_GHIZ: Gate driver output enable

0: G1H, G2H, G1L, and G2L outputs operate according to the setting.

1: G1H, G2H, G1L, and G2L are pulled down by 160 kΩ (Typ).

CS_EN: Current detection amplifier enable

0: AOUT1 and AOUT2 are Hi-Z.

1: AOUT1 and AOUT2 amplify and output the input difference between AIN1P, AIN1N, AIN2P and AIN2N.

Address = 03h <Mode Settings>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
03h	R/W	G2H_SEL	G2H_FIX	G2L_SEL	G2L_FIX	G1H_SEL	G1H_FIX	G1L_SEL	G1L_FIX
Initial Value	00h	0	0	0	0	0	0	0	0

Each gate driver output can be driven High or Low by PWM input signal or SPI register setting value.

G2H_SEL, G2L_SEL, G1H_SEL, G1L_SEL

Changes the control mode of each gate driver output.

0: Each gate driver output is output according to the value set by the following register G1H_FIX, G1L_FIX, G2H_FIX, G2L_FIX.

1: Each gate driver output is output according to the input value of the PWM1 and PWM2 pins.

G2H_FIX, G2L_FIX, G1H_FIX, G1L_FIX

When G2H_SEL, G2L_SEL, G1H_SEL, G1L_SEL = 0, controls the logic of the gate driver outputs.

When G2H_SEL, G2L_SEL, G1H_SEL, G1L_SEL = 1, the set value has no effect on the gate driver outputs.

0: Gate driver output is Low.

1: Gate driver output is High.

For details about the control modes, refer to Table 6 below. For information about PWM control, refer to the chapter on PWM control. Note that combinations not listed in Table 6 below are prohibited from use. When set to prohibited conditions, all gate driver outputs will be set to low.

Table 6. Gate Driver Output Control Mode

Gate Driver Output Control Mode Configuration														
No.	MODE_SEL	G1H_SEL	G1H_FIX	G1L_SEL	G1L_FIX	G1H	G1L	G2H_SEL	G2H_FIX	G2L_SEL	G2L_FIX	G2H	G2L	Channel Control
1	0	0	0	0	0	Low	Low	0	0	0	0	Low	Low	Independent Control
2		0	0	1	x	Low	PWM1	0	0	1	x	Low	PWM2	
3		0	0	0	1	Low	High	0	0	0	1	Low	High	
4		1	x	0	0	PWM1	Low	1	x	0	0	PWM2	Low	
5		1	x	0	1	PWM1	High	1	x	0	1	PWM2	High	
6		0	1	0	0	High	Low	0	1	0	0	High	Low	
7		0	1	1	x	High	PWM1	0	1	1	x	High	PWM2	
8		0	1	0	1	High	High	0	1	0	1	High	High	
9		1	x	1	x	PWM1	PWM1	1	x	1	x	PWM2	PWM2	
10	1	0	0	0	0	Low	Low	0	0	0	0	Low	Low	H-bridge Control
11		0	1	0	0	High	Low	0	1	0	0	High	Low	
12		0	0	0	1	Low	High	0	0	0	1	Low	High	
13		0	1	0	0	High	Low	0	0	0	1	Low	High	
14		0	0	0	1	Low	High	0	1	0	0	High	Low	
15		1	x	0	0	PWM1	Low	0	0	0	1	Low	High	
16		0	0	0	1	Low	High	1	x	0	0	PWM2	Low	
17		1	x	1	x	PWM1	PWM1	1	x	1	x	PWM2	PWM2	

Address = 04h <Fault Status1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
04h	R/W	ST_VCPUV	ST_DHUV	ST_VBOV	ST_VBUV	ST_VCOV	ST_VCUV	ST_TW	ST_TSD
Initial Value	04h	0	0	0	0	0	1	0	0

This is a status register that indicates the results of each detected fault.

0: No fault detected

1: Fault detected

ST_VCPUV : VCP Undervoltage Detection results

ST_DHUV : DH Undervoltage Detection results

ST_VBOV : VB Overvoltage Detection results

ST_VBUV : VB Undervoltage Detection results

ST_VCOV : VCC Overvoltage Detection results

ST_VCUV : VCC Undervoltage Detection results

ST_TW : Thermal Warning Detection results

ST_TSD : Thermal Shutdown Detection results

Writing 1 to each register ST_XXX (status register) resets the fault detection result to 0. The corresponding global status register is also reset. Note that while fault is being detected or during a protection period set by the Protect Period, the status register cannot be reset to 0 even if ST_XXX = 1 is set. It will still continue to be detected.

Only the register ST_VCUV has a different initial value than the other status registers. The initial value is ST_VCUV = 1 (fault detected), so it is necessary to set the value to ST_VCUV = 0 once. If a VCUV fault is detected after that, it will be reset to ST_VCUV = 1. Note that if a VCC undervoltage fault behavior is detected, the entire LOGIC circuit is reset, and so the values of other fault status registers and settings are also reset.

Address = 05h <Fault Status2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
05h	R/W	ST_VDS_H2	ST_VDS_L2	ST_VDS_H1	ST_VDS_L1	ST_SPI	-	ST_VRDET2	ST_VRDET1
Initial Value	00h	0	0	0	0	0	0	0	0

This is a status register that indicates the results of each detected fault.

0: No fault detected

1: Fault detected

ST_VDS_H2 : External MOS FET (DH-S2H) Overcurrent (Overvoltage) detection result

ST_VDS_L2 : External MOS FET (S2H-S2L) Overcurrent (Overvoltage) detection result

ST_VDS_H1 : External MOS FET (DH-S1H) Overcurrent (Overvoltage) detection result

ST_VDS_L1 : External MOS FET (S1H-S1L) Overcurrent (Overvoltage) detection result

ST_SPI : SPI transfer error detection result

ST_VRDET2 : Shunt Resistor (AIN2P-AIN2N) Overcurrent (Overvoltage) detection result

ST_VRDET1 : Shunt Resistor (AIN1P-AIN1N) Overcurrent (Overvoltage) detection result

Writing 1 to each register ST_XXX (status register) resets the fault detection result to 0. The corresponding global status register is also reset. Note that while fault is being detected or during a protection period set by the Protect Period, the status register cannot be reset to 0 even if ST_XXX = 1 is set. It will still continue to be detected.

Address = 06h <Fault Status3>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
06h	R/W	ST_VGS_H2_OV	ST_VGS_L2_OV	ST_VGS_H2_UV	ST_VGS_L2_UV	ST_VGS_H1_OV	ST_VGS_L1_OV	ST_VGS_H1_UV	ST_VGS_L1_UV
Initial Value	00h	0	0	0	0	0	0	0	0

This is a status register that indicates the results of each detected fault.

0: No fault detected

1: Fault detected

ST_VGS_H2_OV : G2H VGS Overvoltage Detection result

ST_VGS_L2_OV : G2L VGS Overvoltage Detection result

ST_VGS_H2_UV : G2H VGS Undervoltage Detection result

ST_VGS_L2_UV : G2L VGS Undervoltage Detection result

ST_VGS_H1_OV : G1H VGS Overvoltage Detection result

ST_VGS_L1_OV : G1L VGS Overvoltage Detection result

ST_VGS_H1_UV : G1H VGS Undervoltage Detection result

ST_VGS_L1_UV : G1L VGS Undervoltage Detection result

Writing 1 to each register ST_XXX (status register) resets the fault detection result to 0. The corresponding global status register is also reset. Note that while fault is being detected or during a protection period set by the Protect Period, the status register cannot be reset to 0 even if ST_XXX = 1 is set. It will still continue to be detected.

Address = 07h <Latch Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
07h	R/W	-	LAT_DHUV	LAT_VBOV	LAT_VBUV	LAT_VCOV	-	LAT_TW	LAT_TSD
Initial Value	00h	0	0	0	0	0	0	0	0

It is possible to select the protective action to be taken when fault is detected and the mode of the error notification signal (ERRB).

0: Automatic recovery mode. Output operation is automatically restored when the fault or fault condition is resolved.

1: Latch Mode. Even if the abnormal condition is resolved, the protection operation continues until the SPI command (LAT_CLR) is set.

LAT_DHUV : Protection operation after DH undervoltage detection and error notification signal mode selection.

LAT_VBOV : Protection operation after VB overvoltage detection and error notification signal mode selection.

LAT_VBUV : Protection operation after VB undervoltage detection and error notification signal mode selection.

LAT_VCOV : Protection operation after VCC overvoltage detection and error notification signal mode selection.

LAT_TW : After thermal warning detection, error notification signal mode selection.

LAT_TSD : Protection operation after Thermal Shutdown detection and error notification signal mode selection.

Address = 08h <Latch Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
08h	R/W	LAT_VDS_H2	LAT_VDS_L2	LAT_VDS_H1	LAT_VDS_L1	-	-	LAT_VRDE_T2	LAT_VRDE_T1
Initial Value	00h	0	0	0	0	0	0	0	0

It is possible to select the protective action to be taken when fault is detected and the mode of the error notification signal (ERRB).

0: Automatic recovery mode. Output operation is automatically restored when the fault or fault condition is resolved.

1: Latch Mode. Even if the abnormal condition is resolved, the protection operation continues until the SPI command (LAT_CLR) is set.

LAT_VDS_H2: Protection operation after External MOS FET (DH-S2H) Overcurrent (Overvoltage) detection and error notification signal mode selection.

LAT_VDS_L2 : Protection operation after External MOS FET (S2H-S2L) Overcurrent (Overvoltage) detection and error notification signal mode selection.

LAT_VDS_H1: Protection operation after External MOS FET (DH-S1H) Overcurrent (Overvoltage) detection and error notification signal mode selection.

LAT_VDS_L1 : Protection operation after External MOS FET (S1H-S1L) Overcurrent (Overvoltage) detection and error notification signal mode selection.

LAT_VRDET2: Protection operation after Shunt Resistor (AIN2P-AIN2N) Overcurrent (Overvoltage) detection and error notification signal mode selection.

LAT_VRDET1: Protection operation after Shunt Resistor (AIN1P-AIN1N) Overcurrent (Overvoltage) detection and error notification signal mode selection.

Address = 09h <Latch Settings3>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
09h	R/W	-	-	LAT_VGS_ H2	LAT_VGS_ L2	-	-	LAT_VGS_ H1	LAT_VGS_ L1
Initial Value	00h	0	0	0	0	0	0	0	0

It is possible to select the protective action to be taken when fault is detected and the mode of the error notification signal (ERRB).

0: Automatic recovery mode. Output operation is automatically restored when the fault or fault condition is resolved.

1: Latch Mode. Even if the abnormal condition is resolved, the protection operation continues until the SPI command (LAT_CLR) is set.

LAT_VGS_H2: Protection operation after External MOS FET (G2H-S2H) voltage detection and error notification signal mode selection.

LAT_VGS_L2 : Protection operation after External MOS FET (G2L-S2L) voltage detection and error notification signal mode selection.

LAT_VGS_H1: Protection operation after External MOS FET (G1H-S1H) voltage detection and error notification signal mode selection.

LAT_VGS_L1 : Protection operation after External MOS FET (G1L-S1L) voltage detection and error notification signal mode selection.

Address = 0Ah <Mask Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Ah	R/W	MASK_VCPUV	MASK_DHUV	MASK_VBOV	MASK_VBUV	MASK_VCOV	-	-	-
Initial Value	00h	0	0	0	0	0	0	0	0

The detection operation of each protection can be selected.

0: Fault Detection Enable. If the specified fault or fault condition occurs, it is detected, and protective action is taken.

1: Fault Detection Disable. Even if the specified fault or fault condition occurs, it is not detected.

MASK_VCPUV : VCP Undervoltage Detection Mask Select

MASK_DHUV : DH Undervoltage Detection Mask Select

MASK_VBOV : VB Overvoltage Detection Mask Select

MASK_VBUV : VB Undervoltage Detection Mask Select

MASK_VCOV : VCC Overvoltage Detection Mask Select

Address = 0Bh <Mask Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Bh	R/W	MASK_VDS_H2	MASK_VDS_L2	MASK_VDS_H1	MASK_VDS_L1	-	-	MASK_VRDET2	MASK_VRDET1
Initial Value	00h	0	0	0	0	0	0	0	0

The detection operation of each protection can be selected.

0: Fault Detection Enable. If the specified fault or fault condition occurs, it is detected, and protective action is taken.

1: Fault Detection Disable. Even if the specified fault or fault condition occurs, it is not detected.

MASK_VDS_H2 : External MOS FET (DH-S2H) Overcurrent (Overvoltage) Detection Mask Select

MASK_VDS_L2 : External MOS FET (S2H-S2L) Overcurrent (Overvoltage) Detection Mask Select

MASK_VDS_H1 : External MOS FET (DH-S1H) Overcurrent (Overvoltage) Detection Mask Select

MASK_VDS_L1 : External MOS FET (S1H-S1L) Overcurrent (Overvoltage) Detection Mask Select

MASK_VRDET2 : Shunt Resistor (AIN2P-AIN2N) Overcurrent (Overvoltage) Detection Mask Select

MASK_VRDET1 : Shunt Resistor (AIN1P-AIN1N) Overcurrent (Overvoltage) Detection Mask Select

Address = 0Ch <Mask Settings3>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Ch	R/W	-	-	MASK_VGS_H2	MASK_VGS_L2	-	-	MASK_VGS_H1	MASK_VGS_L1
Initial Value	00h	0	0	0	0	0	0	0	0

The detection operation of each protection can be selected.

0: Fault Detection Enable. If the specified fault or fault condition occurs, it is detected, and protective action is taken.

1: Fault Detection Disable. Even if the specified fault or fault condition occurs, it is not detected.

MASK_VGS_H2 : External MOS FET (G2H-S2H) Voltage Detection Mask Select

MASK_VGS_L2 : External MOS FET (G2L-S2L) Voltage Detection Mask Select

MASK_VGS_H1 : External MOS FET (G1H-S1H) Voltage Detection Mask Select

MASK_VGS_L1 : External MOS FET (G1L-S1L) Voltage Detection Mask Select

Address = 0Dh <Flag Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Dh	R/W	FLG_VCPUV	FLG_DHUV	FLG_VBOV	FLG_VBUV	FLG_VCOV	-	FLG_TW	FLG_TSD
Initial Value	FBh	1	1	1	1	1	0	1	1

ERRB pin output operation can be selected.

0: Fault detection does not output to ERRB pin.

1: Fault detection outputs to ERRB pin.

FLG_VCPUV : VCP Undervoltage Detection ERRB output select
 FLG_DHUV : DH Undervoltage Detection ERRB output select
 FLG_VBOV : VB Overvoltage Detection ERRB output select
 FLG_VBUV : VB Undervoltage Detection ERRB output select
 FLG_VCOV : VCC Overvoltage Detection ERRB output select
 FLG_TW : Thermal Warning Detection ERRB output select
 FLG_TSD : Thermal Shutdown Detection ERRB output select

Address = 0Eh <Flag Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Eh	R/W	FLG_VDS_H2	FLG_VDS_L2	FLG_VDS_H1	FLG_VDS_L1	FLG_SPI	-	FLG_VRDET2	FLG_VRDET1
Initial Value	FBh	1	1	1	1	1	0	1	1

ERRB pin output operation can be selected.

0: Fault detection does not output to ERRB pin.

1: Fault detection outputs to ERRB pin.

FLG_VDS_H2 : External MOS FET (DH-S2H) Overcurrent (Overvoltage) Detection ERRB output select
 FLG_VDS_L2 : External MOS FET (S2H-S2L) Overcurrent (Overvoltage) Detection ERRB output select
 FLG_VDS_H1 : External MOS FET (DH-S1H) Overcurrent (Overvoltage) Detection ERRB output select
 FLG_VDS_L1 : External MOS FET (S1H-S1L) Overcurrent (Overvoltage) Detection ERRB output select
 FLG_SPI : SPI transfer error Detection ERRB output select
 FLG_VRDET2 : Shunt resistance (AIN2P-AIN2N) Overcurrent (Overvoltage) Detection ERRB output select
 FLG_VRDET1 : Shunt resistance (AIN1P-AIN1N) Overcurrent (Overvoltage) Detection ERRB output select

Address = 0Fh <Flag Settings3>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
0Fh	R/W	-	-	FLG_VGS_H2	FLG_VGS_L2	-	-	FLG_VGS_H1	FLG_VGS_L1
Initial Value	33h	0	0	1	1	0	0	1	1

ERRB pin output operation can be selected.

0: Fault detection does not output to ERRB pin.

1: Fault detection outputs to ERRB pin.

FLG_VGS_H2 : External MOS FET (G2H-S2H) Voltage Detection ERRB output select
 FLG_VGS_L2 : External MOS FET (G2L-S2L) Voltage Detection ERRB output select
 FLG_VGS_H1 : External MOS FET (G1H-S1H) Voltage Detection ERRB output select
 FLG_VGS_L1 : External MOS FET (G1L-S1L) Voltage Detection ERRB output select

Address = 10h <Output Current Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
10h	R/W	CUR_SO_H1SEL	CUR_SO_H1[2]	CUR_SO_H1[1]	CUR_SO_H1[0]	CUR_SI_H1SEL	CUR_SI_H1[2]	CUR_SI_H1[1]	CUR_SI_H1[0]
Initial Value	FFh	1	1	1	1	1	1	1	1

CUR_SO_H1SEL : Gate Driver Output G1H Source Current Range Setting

CUR_SO_H1[2:0] : Gate Driver Output G1H Source Current Setting

CUR_SI_H1SEL : Gate Driver Output G1H Sink Current Range Setting

CUR_SI_H1[2:0] : Gate Driver Output G1H Sink Current Setting

Table 7. Gate Driver Output Source/Sink Current Settings

CUR_SO_HxSEL CUR_SI_HxSEL CUR_SO_LxSEL CUR_SI_LxSEL (X = 1, 2)	CUR_SO_Hx[2:0] CUR_SI_Hx[2:0] CUR_SO_Lx[2:0] CUR_SI_Lx[2:0] (X = 1, 2)	Source Current Sink Current
0	0h	1.50 mA
	1h	1.75 mA
	2h	2.00 mA
	3h	2.50 mA
	4h	3.00 mA
	5h	4.00 mA
	6h	6.00 mA
	7h	10.00 mA
1	0h	4.50 mA
	1h	5.25 mA
	2h	6.00 mA
	3h	7.50 mA
	4h	9.00 mA
	5h	12.00 mA
	6h	18.00 mA
	7h	30.00 mA

The source/sink current value does not include the pull-down current due to the 160 kΩ (Typ) resistor.

Address = 11h <Output Current Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
11h	R/W	CUR_SO_L1SEL	CUR_SO_L1 [2]	CUR_SO_L1 [1]	CUR_SO_L1 [0]	CUR_SI_L1SEL	CUR_SI_L1 [2]	CUR_SI_L1 [1]	CUR_SI_L1 [0]
Initial Value	FFh	1	1	1	1	1	1	1	1

CUR_SO_L1SEL : Gate Driver Output G1L Source Current Range Setting

CUR_SO_L1 [2:0] : Gate Driver Output G1L Source Current Setting

CUR_SI_L1SEL : Gate Driver Output G1L Sink Current Range Setting

CUR_SI_L1 [2:0] : Gate Driver Output G1L Sink Current Setting

For details on register settings, see [Table 7. Gate Driver Output Source/Sink Current Settings](#)**Address = 12h <Output Current Settings3>**

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
12h	R/W	CUR_SO_H2SEL	CUR_SO_H2 [2]	CUR_SO_H2 [1]	CUR_SO_H2 [0]	CUR_SI_H2SEL	CUR_SI_H2 [2]	CUR_SI_H2 [1]	CUR_SI_H2 [0]
Initial Value	FFh	1	1	1	1	1	1	1	1

CUR_SO_H2SEL : Gate Driver Output G2H Source Current Range Setting

CUR_SO_H2 [2:0] : Gate Driver Output G2H Source Current Setting

CUR_SI_H2SEL : Gate Driver Output G2H Sink Current Range Setting

CUR_SI_H2 [2:0] : Gate Driver Output G2H Sink Current Setting

For details on register settings, see [Table 7. Gate Driver Output Source/Sink Current Settings](#)**Address = 13h <Output Current Settings4>**

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
13h	R/W	CUR_SO_L2SEL	CUR_SO_L2 [2]	CUR_SO_L2 [1]	CUR_SO_L2 [0]	CUR_SI_L2SEL	CUR_SI_L2 [2]	CUR_SI_L2 [1]	CUR_SI_L2 [0]
Initial Value	FFh	1	1	1	1	1	1	1	1

CUR_SO_L2SEL : Gate Driver Output G2L Source Current Range Setting

CUR_SO_L2 [2:0] : Gate Driver Output G2L Source Current Setting

CUR_SI_L2SEL : Gate Driver Output G2L Sink Current Range Setting

CUR_SI_L2 [2:0] : Gate Driver Output G2L Sink Current Setting

For details on register settings, see [Table 7. Gate Driver Output Source/Sink Current Settings](#)

Address = 14h <Analog Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
14h	R/W	MODE_SEL	VBOV_SEL	-	CHP_FREQ_DFUEEN	-	CSAMP_REF	CSAMP_GAIN [1]	CSAMP_GAIN [0]
Initial Value	01h	0	0	0	0	0	0	0	1

MODE_SEL: Select H-bridge control mode or independent control mode.

0: Independent Control Mode

1: H-bridge Control

VBOV_SEL: Thresholds for Detecting VB Overvoltage

Table 8. VB Overvoltage Detection Threshold Voltage Setting

VBOV_SEL	Threshold Voltage [V]
0	Detect: 22.0 V/Release: 21.0 V (Typ)
1	Detect: 32.5 V/Release: 31.5 V (Typ)

CHP_FREQ_DFUEEN: Frequency Diffusion Setting

Table 9. Frequency Diffusion Setting

CHP_FREQ_DFUEEN	Frequency Diffusion Setting
0	Frequency Diffusion is Disabled
1	Frequency Diffusion is Enabled

This device is equipped with a frequency diffusion function that varies the frequency over a given range. Using the frequency diffusion function makes it possible to suppress EMI radiation noise. The diffusion frequency band is 333 kHz (Typ) to 455 kHz (Typ) $\pm 10\%$, and frequency diffusion is performed in 8 steps.

CSAMP_REF: REF Voltage Setting of Current Detection Amplifier

Table 10. Current Detection Amplifier REF Voltage Setting

CSAMP_REF	REF Voltage Setting [V]
0	REF/2
1	REF/8

CSAMP_GAIN [1:0] : Gain Setting of Current Detection Amplifier

Table 11. Gain Setting of Current Detection Amplifier

CSAMP_GAIN [1:0]	Gain Setting Multiplier
0h	8 times
1h	16 times
2h	32 times
3h	48 times

Address = 16h <Dead Time Settings>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
16h	R/W	-	-	-	-	TDEAD [3]	TDEAD [2]	TDEAD [1]	TDEAD [0]
Initial Value	00h	0	0	0	0	0	0	0	0

TDEAD [3:0] : Dead time Setting for preventing shoot-through current

Table 12. Dead Time Setting

TDEAD [3:0]	Dead Time
0h	0 μ s (Note 1)
1h	1 μ s
2h	2 μ s
3h	3 μ s
4h	4 μ s
5h	5 μ s
6h	6 μ s
7h	7 μ s
8h	8 μ s
9h	12 μ s
Ah	16 μ s
Bh	24 μ s
Ch	32 μ s
Dh	48 μ s
Eh	64 μ s
Fh	96 μ s

(Note 1) To prevent shoot-through current, do not set TDEAD [3:0] = 0h.

Address = 17h <VDS Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
17h	R/W	-	VDS_H1 [2]	VDS_H1 [1]	VDS_H1 [0]	-	VDS_L1 [2]	VDS_L1 [1]	VDS_L1 [0]
Initial Value	44h	0	1	0	0	0	1	0	0

VDS_H1 [2:0] : External MOS FET (DH-S1H) Overvoltage (Overcurrent) detection threshold voltage setting

VDS_L1 [2:0] : External MOS FET (S1H-S1L) Overvoltage (Overcurrent) detection threshold voltage setting

Table 13. VDS Overvoltage (Overcurrent) Detection Threshold Voltage Setting

VDS_Hx [2:0] VDS_Lx [2:0] (X = 1, 2)	VDS Overvoltage (Overcurrent) detection threshold voltage setting (V_{VDSx})
0h	200 mV
1h	300 mV
2h	400 mV
3h	500 mV
4h	750 mV
5h	1000 mV
6h	1250 mV
7h	1500 mV

Address = 18h <VDS Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
18h	R/W	-	VDS_H2 [2]	VDS_H2 [1]	VDS_H2 [0]	-	VDS_L2 [2]	VDS_L2 [1]	VDS_L2 [0]
Initial Value	44h	0	1	0	0	0	1	0	0

VDS_H2 [2:0] : External MOS FET (DH-S2H) Overvoltage (Overcurrent) detection threshold voltage setting

VDS_L2 [2:0] : External MOS FET (S2H-S2L) Overvoltage (Overcurrent) detection threshold voltage setting

For details on register settings, see [Table 13. VDS Overvoltage \(Overcurrent\) Detection Threshold Voltage Setting](#)

Address = 19h <RDET Settings>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
19h	R/W	-	RDET2 [2]	RDET2 [1]	RDET2 [0]	-	RDET1 [2]	RDET1 [1]	RDET1 [0]
Initial Value	44h	0	1	0	0	0	1	0	0

RDET2 [2:0] : Shunt Resistor (AIN2P-AIN2N) Overvoltage detection threshold voltage setting

RDET1 [2:0] : Shunt Resistor (AIN1P-AIN1N) Overvoltage detection threshold voltage setting

Table 14. Shunt Resistor Overvoltage Detection Threshold Voltage Setting

RDET2 [2:0] RDET1 [2:0]	Shunt Resistor Overvoltage detection threshold voltage setting ($V_{RDET\text{x}}$)
0h	200 mV
1h	300 mV
2h	400 mV
3h	500 mV
4h	750 mV
5h	1000 mV
6h	1250 mV
7h	1500 mV

Address = 1Ah <VDS, VGS RDET Blanking Settings1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
1Ah	R/W	FET_G1H_FLT [3]	FET_G1H_FLT [2]	FET_G1H_FLT [1]	FET_G1H_FLT [0]	FET_G1L_FLT [3]	FET_G1L_FLT [2]	FET_G1L_FLT [1]	FET_G1L_FLT [0]
Initial Value	33h	0	0	1	1	0	0	1	1

FET_G1H_FLT [3:0] : Fault detection blanking time and protection hold time settings for VDS fault detection of external MOS FET (DH-S1H) and VGS fault detection of external MOS FET (G1H-S1H).

FET_G1L_FLT [3:0] : Fault detection blanking time and protection hold time settings for VDS fault detection of external MOS FET (DH-S1L), VGS fault detection of external MOS FET (G1L-S1L), and Overcurrent (overvoltage) fault detection of shunt resistor (AIN1P-AIN1N).

The blanking time includes the Blanking Time Setting time set in the register plus an internal circuit delay of 2.4 μs (Max)
(Note).

Therefore, the actual blanking time is calculated using the following formula.

$$\text{Blanking Time} = \text{Internal Delay (2.4 } \mu\text{s} < \text{Max} >)^{(\text{Note})} + \text{Blanking Time Setting}$$

Table 15. Blanking Time/Protection Period Setting 1

FET_G1H_FLT [3:0] FET_G1L_FLT [3:0]	Blanking Time Setting	Protect Period
0h	1 μs	10 μs
1h	2 μs	20 μs
2h	3 μs	30 μs
3h	4 μs	40 μs
4h	6 μs	60 μs
5h	8 μs	80 μs
6h	10 μs	100 μs
7h	12 μs	120 μs
8h	16 μs	160 μs
9h	24 μs	240 μs
Ah	28 μs	280 μs
Bh	32 μs	320 μs
Ch	40 μs	400 μs
Dh	48 μs	480 μs
Eh	56 μs	560 μs
Fh	64 μs	640 μs

(Note) This is a design guarantee item and is not inspected at the time of shipment.

Address = 1Bh <VDS, VGS RDET Blanking Settings2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
1Bh	R/W	FET_G2H_FLT [3]	FET_G2H_FLT [2]	FET_G2H_FLT [1]	FET_G2H_FLT [0]	FET_G2L_FLT [3]	FET_G2L_FLT [2]	FET_G2L_FLT [1]	FET_G2L_FLT [0]
Initial Value	33h	0	0	1	1	0	0	1	1

FET_G2H_FLT [3:0] : Fault detection blanking time and protection hold time settings for VDS fault detection of external MOS FET (DH-S2H) and VGS fault detection of external MOS FET (G2H-S2H).

FET_G2L_FLT [3:0] : Fault detection blanking time and protection hold time settings for VDS fault detection of external MOS FET (DH-S2L), VGS fault detection of external MOS FET (G2L-S2L), and Overcurrent (overvoltage) fault detection of shunt resistor (AIN2P-AIN2N).

The blanking time includes the Blanking Time Setting time set in the register plus an internal circuit delay of 2.4 μs (Max)
(Note).

Therefore, the actual blanking time is calculated using the following formula.

$$\text{Blanking Time} = \text{Internal Delay (2.4 } \mu\text{s} < \text{Max} >)^{(\text{Note})} + \text{Blanking Time Setting}$$

Table 16. Blanking Time/Protection Period Setting 2

FET_G2H_FLT [3:0] FET_G2L_FLT [3:0]	Blanking Time Setting	Protect Period
0h	1 μs	10 μs
1h	2 μs	20 μs
2h	3 μs	30 μs
3h	4 μs	40 μs
4h	6 μs	60 μs
5h	8 μs	80 μs
6h	10 μs	100 μs
7h	12 μs	120 μs
8h	16 μs	160 μs
9h	24 μs	240 μs
Ah	28 μs	280 μs
Bh	32 μs	320 μs
Ch	40 μs	400 μs
Dh	48 μs	480 μs
Eh	56 μs	560 μs
Fh	64 μs	640 μs

(Note) This is a design guarantee item and is not inspected at the time of shipment.

Address = 1Ch <DHUV Blanking Setting>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
1Ch	R/W	-	-	-	-	DHUV_FLT [3]	DHUV_FLT [2]	DHUV_FLT [1]	DHUV_FLT [0]
Initial Value	00h	0	0	0	0	0	0	0	0

DHUV_FLT [3:0] : DH Undervoltage Detection Fault detection blanking time and protection hold time setting.

The blanking time includes the Blanking Time Setting time set in the register plus an internal circuit delay of 2.4 μs (Max)
(Note).

Therefore, the actual blanking time is calculated using the following formula.

$$\text{Blanking Time} = \text{Internal Delay (2.4 } \mu\text{s} < \text{Max} >)^{(Note)} + \text{Blanking Time Setting}$$

Table 17. DH Undervoltage Detection, Fault Detection Blanking Time and Protection Hold Time Setting

DHUV_FLT [3:0]	Blanking Time Setting	Protect Period
0h	1 μs	10 μs
1h	2 μs	20 μs
2h	3 μs	30 μs
3h	4 μs	40 μs
4h	6 μs	60 μs
5h	8 μs	80 μs
6h	10 μs	100 μs
7h	12 μs	120 μs
8h	16 μs	160 μs
9h	24 μs	240 μs
Ah	28 μs	280 μs
Bh	32 μs	320 μs
Ch	40 μs	400 μs
Dh	48 μs	480 μs
Eh	56 μs	560 μs
Fh	64 μs	640 μs

(Note) This is a design guarantee item and is not inspected at the time of shipment.

Address = 1Eh <Static OPEN/SHORT Check>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
1Eh	W	-	-	-	-	OS_EN	AUTO_OS START	SET_OS2	SET_OS1
Initial Value	00h	0	0	0	0	0	0	0	0

OS_EN : Static OPEN/SHORT Check Enable
AUTO_OS_START : Static OPEN/SHORT Check Automatic Enable Start
SET_OS2 : Static OPEN/SHORT Check Setting 2
SET_OS1 : Static OPEN/SHORT Check Setting 1

Address = 1Fh <Static OPEN/SHORT Status>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
1Fh	R	-	ST_OSCHK K_STEP [2]	ST_OSCHK K_STEP [1]	ST_OSCHK K_STEP [0]	ST_OSCHK K_END	ST_OSCHK K_FAIL	ST_OSCHK K2	ST_OSCHK K1
Initial Value	00h	0	0	0	0	0	0	0	0

ST_OSCHK_STEP[2:0] : Static OPEN/SHORT Check result (Detection step) See detection mode table

See [Table 18. Static OPEN/SHORT Check Detection Step](#)

ST_OSCHK_END : Static OPEN/SHORT Check Completion Flag

ST_OSCHK_FAIL : Static OPEN/SHORT Check Fail Flag

ST_OSCHK2 : Static OPEN/SHORT Result

ST_OSCHK1 : Static OPEN/SHORT Result

Table 18. Static OPEN/SHORT Check Detection Step

ST_OSCHK_STEP [2:0]	Detection Part
1h	Drain-Source short circuit failure of M2 or M4 MOS FET
2h	Drain-Source short circuit failure of M1 or M3 MOS FET / Open circuit failure of Motor
3h	Drain-Source short circuit failure of M1 or M3 MOS FET / Open circuit failure of Motor
4h	Open circuit failure of G1H connected MOS FET
5h	Open circuit failure of G2H connected MOS FET
6h	Open circuit failure of G1L connected MOS FET
7h	Open circuit failure of G2L connected MOS FET

Table 19. Static OPEN/SHORT Check Results

Table 19: State Of EN/SHORT Check Results			
Detection Results (Status Register)			
ST_OSCHK2	ST_OSCHK1	ST_OSCHK_STEP [2:0]	Check Result
0	0	1h	Pass
1	0		Fail: Drain-Source Short circuit failure of M2 or M4 connected MOS FET
Other			Fail: Illegal (Fail)
0	0	2h	Pass
0	1		Fail: Drain-Source Short circuit failure of M1 or M3 connected MOS FET
1	0		Fail: Open circuit failure of Motor
Other			Fail: Illegal (Fail)
0	0	3h	Pass
0	1		Fail: Drain-Source Short circuit failure of M1 or M3 connected MOS FET / Open circuit failure of Motor
Other			Fail: Illegal (Fail)
0	0	4h	Pass
1	0		Fail: Open circuit failure of M1 (G1H) connected MOS FET
Other			Fail: Illegal (Fail)
0	0	5h	Pass
1	1		Fail: Open circuit failure of M3 (G2H) connected MOS FET
Other			Fail: Illegal (Fail)
0	0	6h	Pass
1	1		Fail: Open circuit failure of M3 (G2H) connected MOS FET
Other			Fail: Illegal (Fail)
0	0	7h	Pass
0	1		Fail: Open circuit failure of M4 (G2L) connected MOS FET
Other			Fail: Illegal (Fail)

I/O Equivalence Circuit

Pin No.	Pin name	Equivalence circuit	Pin No.	Pin name	Equivalence circuit
1 2 6 7	PWM1 PWM2 SCK SDI		3 32	VCC EN	
4	ERRB		5	CSB	
8	SDO		9 10	AOUT1 AOUT2	
11	REF		12 28	GND PGND	
13 14 15 16	AIN1N AIN1P AIN2N AIN2P		17 24 18 23	G1H G2H S1H S2H	
19 22 20 21	G1L G2L S1L S2L		25	DH	

I/O Equivalence Circuit - continued

Pin No.	Pin name	Equivalence circuit	Pin No.	Pin name	Equivalence circuit
26 30	VCP VB		27	CPH	
29	CPL		31	DBRKB	

Typical Performance Curves

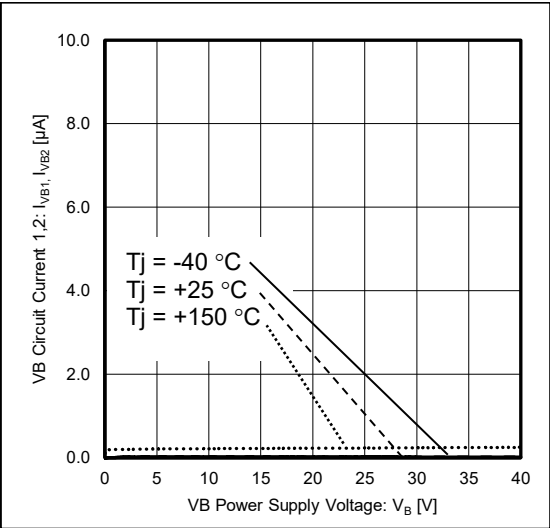


Figure 48. VB Circuit Current 1,2 vs VB Power Supply Voltage

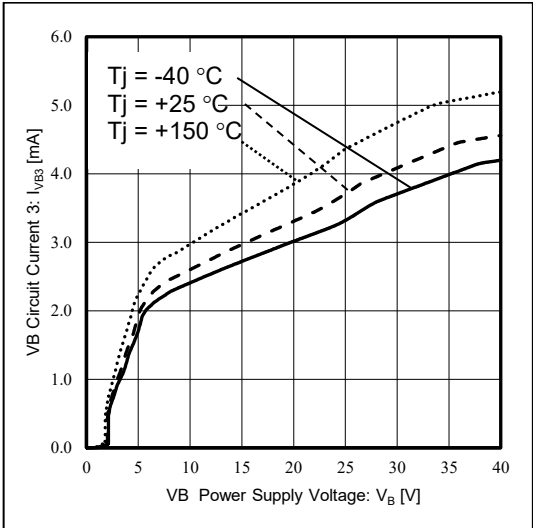


Figure 49. VB Circuit Current 3 vs VB Power Supply Voltage

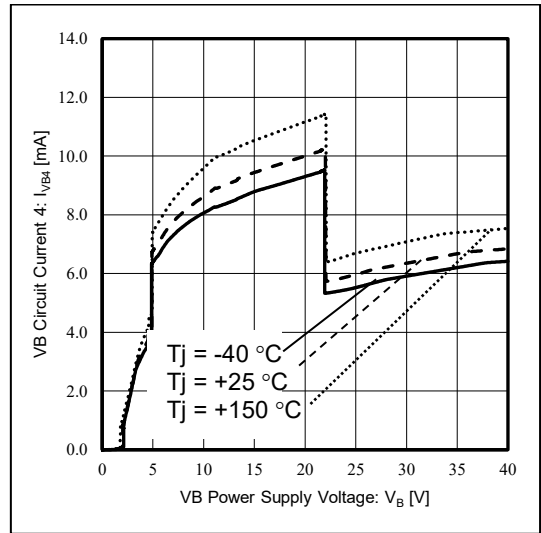


Figure 50. VB Circuit Current 4 vs VB Power Supply Voltage
(VBOV_SEL = 0)

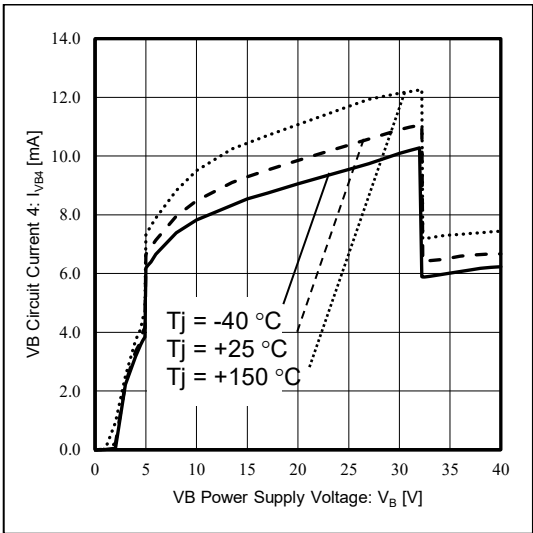


Figure 51. VB Circuit Current 4 vs VB Power Supply Voltage
(VBOV_SEL = 1)

Typical Performance Curves - continued

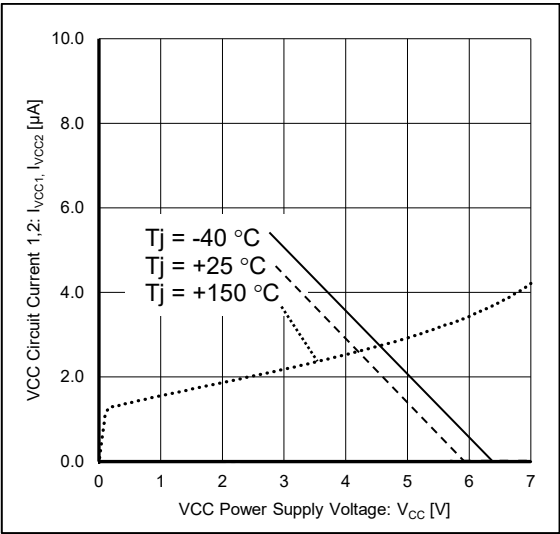


Figure 52. VCC Circuit Current 1,2 vs VCC Power Supply Voltage

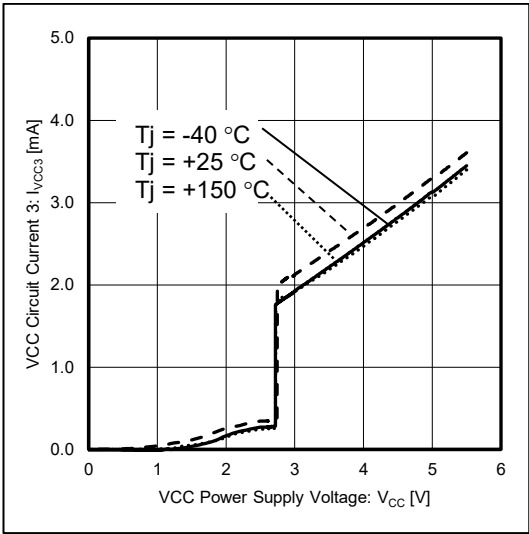


Figure 53. VCC Circuit Current 3 vs VCC Power Supply Voltage

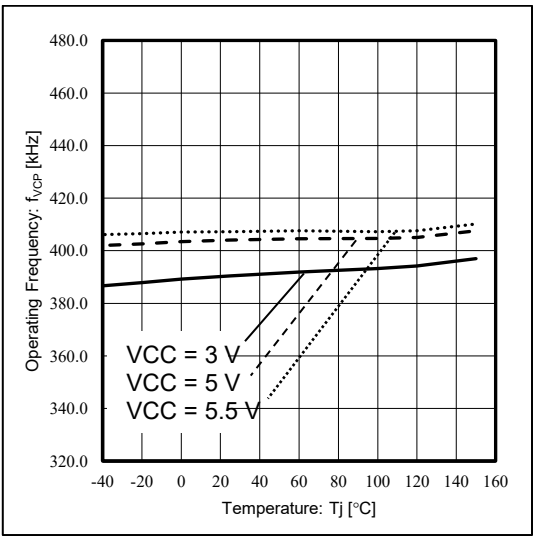


Figure 54. Operating Frequency vs Temperature

Typical Performance Curves - continued

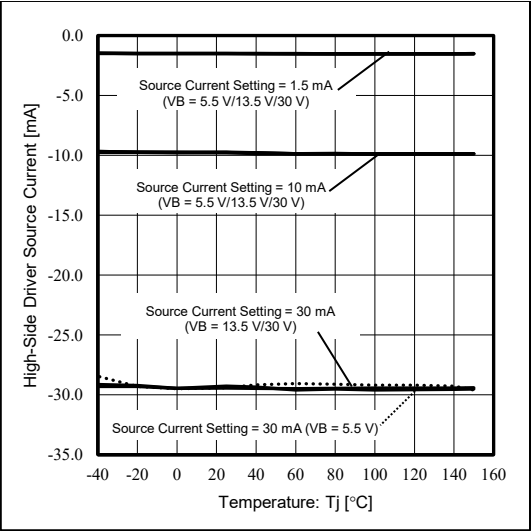


Figure 55. High-Side Driver Source Current vs Temperature

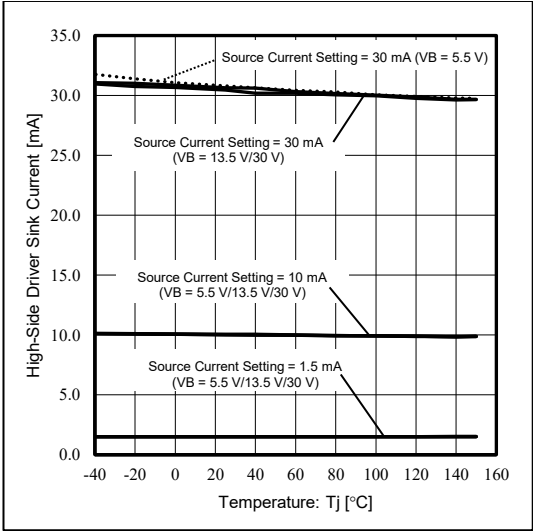


Figure 56. High-Side Driver Sink Current vs Temperature

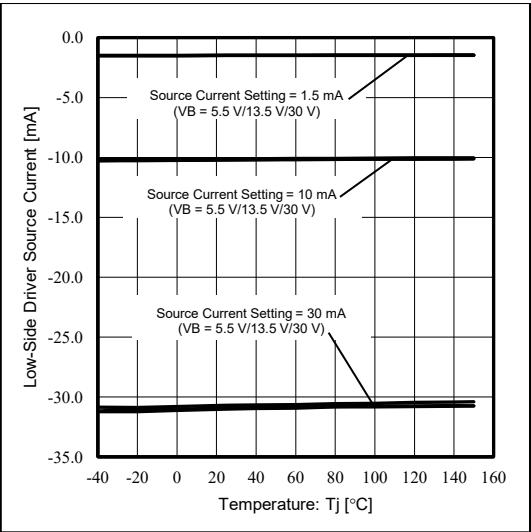


Figure 57. Low-Side Driver Source Current vs Temperature

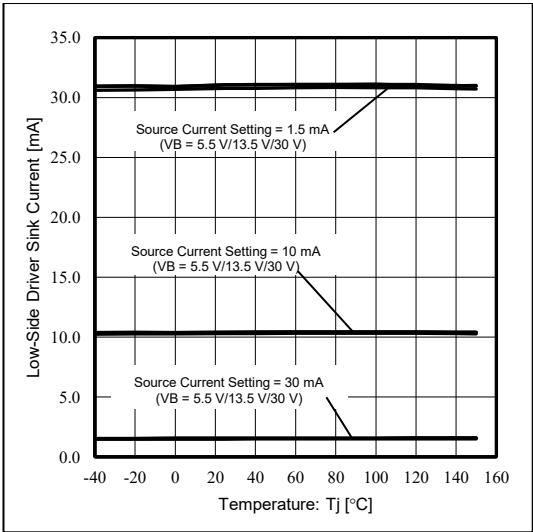


Figure 58. Low-Side Driver Sink Current vs Temperature

Typical Performance Curves - continued

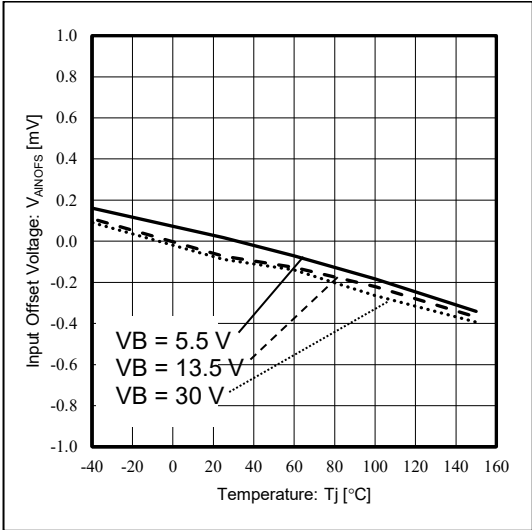


Figure 59. Input Offset Voltage vs Temperature
(CSAMP_GAIN [1:0] = 0h)

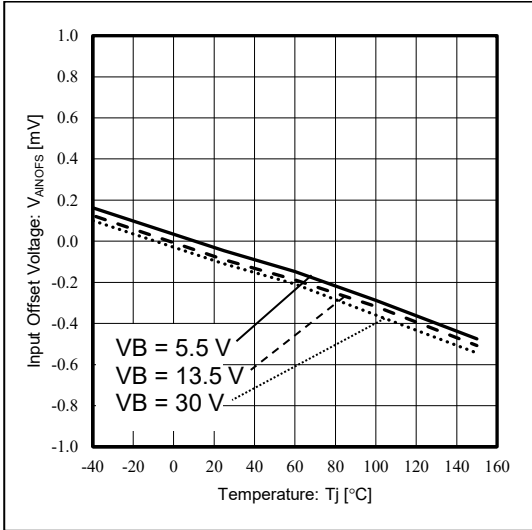


Figure 60. Input Offset Voltage vs Temperature
(CSAMP_GAIN [1:0] = 1h)

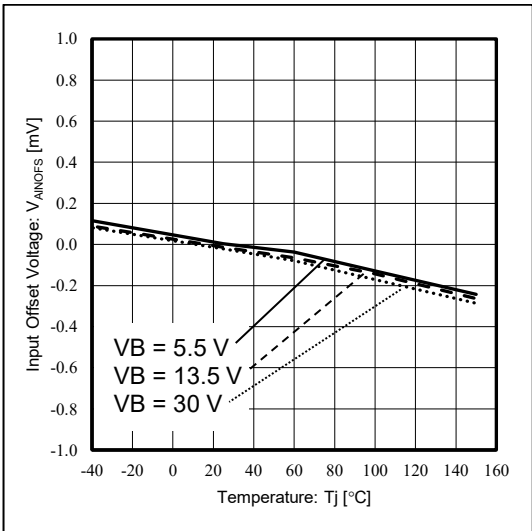


Figure 61. Input Offset Voltage vs Temperature
(CSAMP_GAIN [1:0] = 2h)

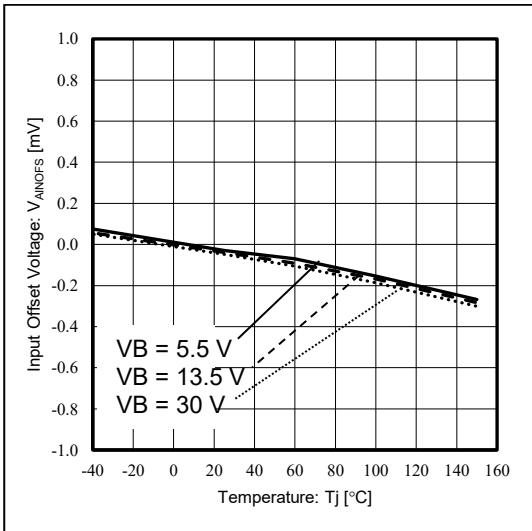


Figure 62. Input Offset Voltage vs Temperature
(CSAMP_GAIN [1:0] = 3h)

Typical Performance Curves - continued

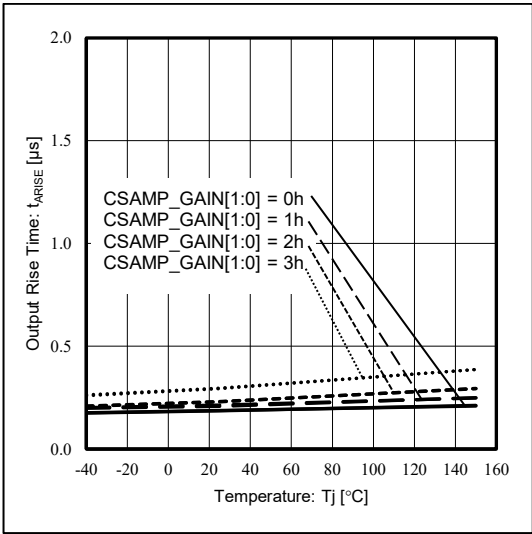


Figure 63. Output Rise Time vs Temperature
(VB = 13.5 V, VCC = 5 V)

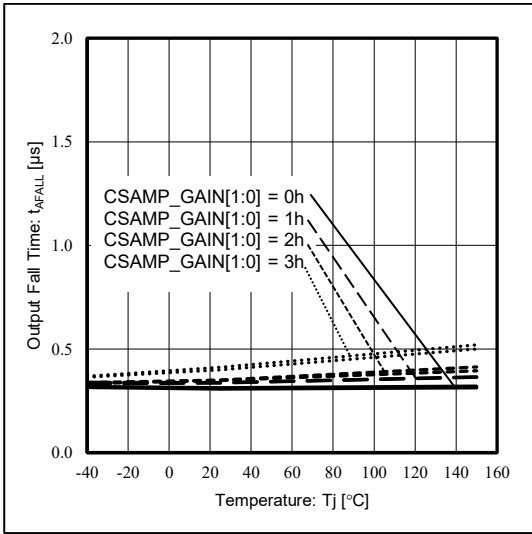


Figure 64. Output Fall Time vs Temperature
(VB = 13.5 V, VCC = 5 V)

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

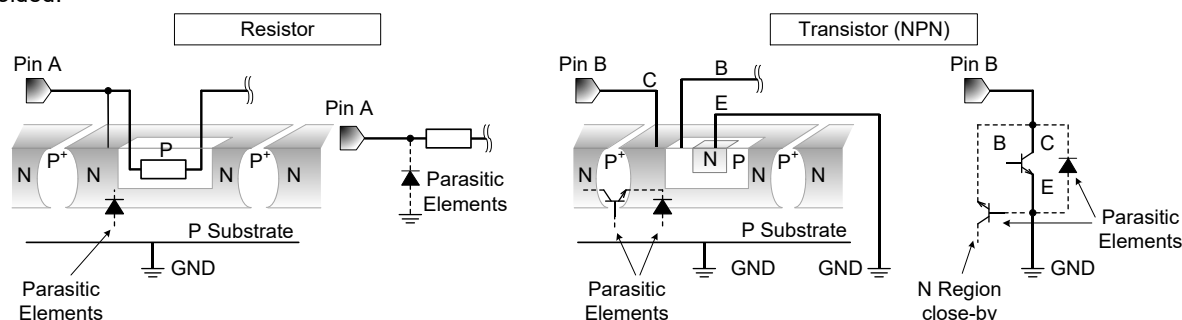


Figure 65. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins.

This IC supports two configurations, Retry Mode and Latch Mode.

When configured in Retry Mode, when the T_j falls below the TSD threshold, the outputs are automatically restored to normal operation.

When configured in Latch Mode, the TSD circuit keeps the outputs in the OFF state even if the T_j falls below the TSD threshold. The IC should be powered down and turned ON again to resume normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

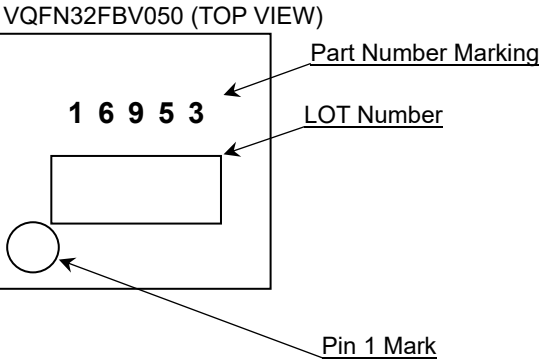
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

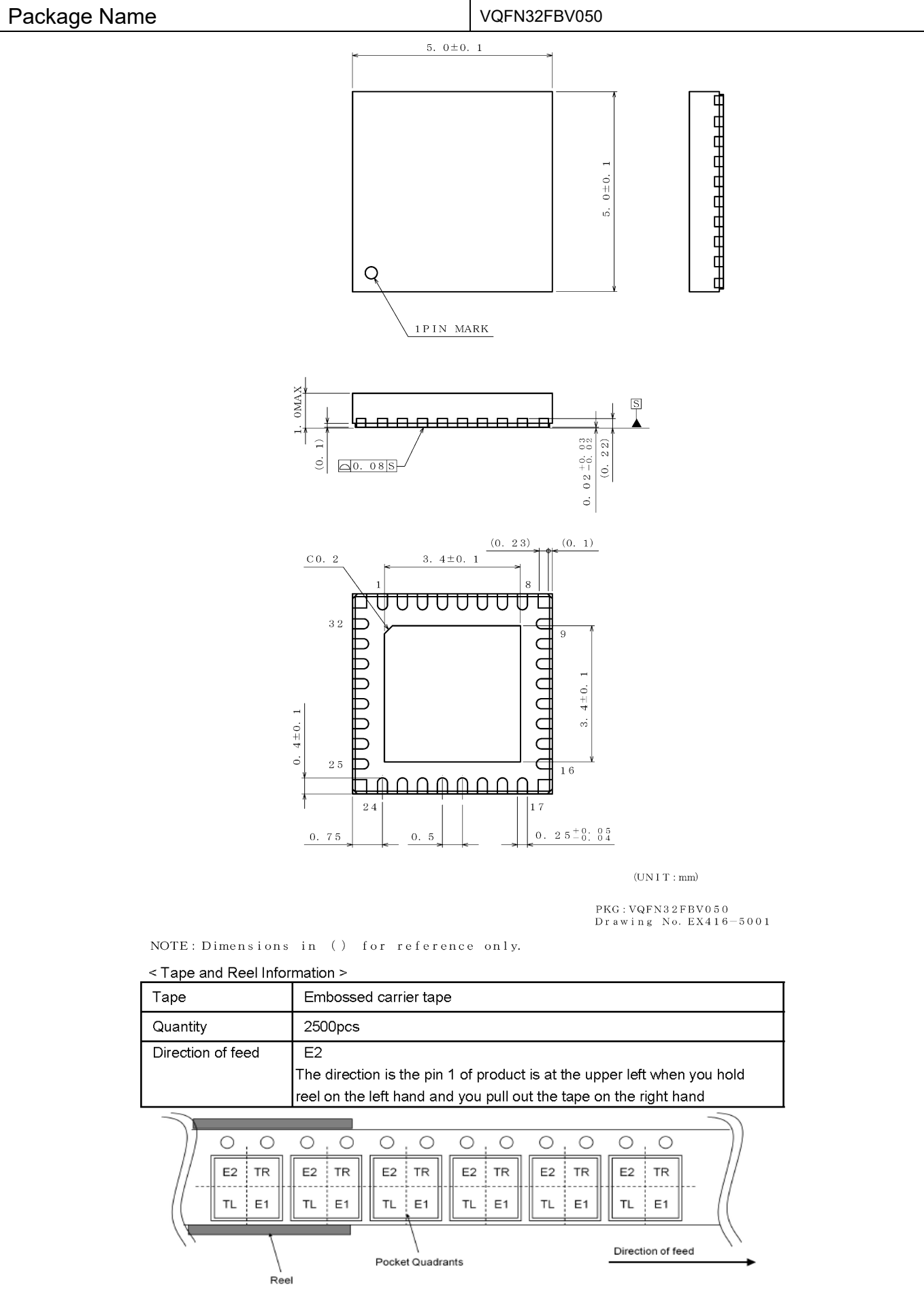
Ordering Information

B D 1 6 9 5 3 M U F										-	C E 2		
										Package	Product rank		
										MUF: VQFN32FBV050	C: Automotive ranked products		
											Packaging and forming		
											specifications		
											E2: Embossed tape and reel		

Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Edition	Changes
16.Mar.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - [a] Installation of protection circuits or other protective devices to improve system safety
 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application examples, their constants, software, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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