Stepping Motor Driver for Automotive

BD68960EKV-C

General Description

BD68960EKV-C is a low-consumption bipolar driver driven by PWM current. Rated power supply voltage of the device is 35 V, and rated output current is 1.8 A. PARA-IN driving mode is adopted for input interface and current decay mode is the SLOW DECAY.

Key Specifications

- Input Voltage: 35 V
- Output Current: ±1.8 A/Phase
- Operating Temperature Range: -40 °C to +125 °C
- Output ON Resistance: 0.35 Ω (Typ)
  (total of upper and lower resistors)

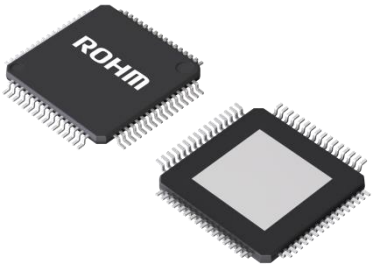
Features

- AEC-Q100 Qualified*(Note 1)*
- Rated Output Current (DC) 1.8 A
- Low ON Resistance H Bridge Output
- PARA-IN Drive Mode
- Built-in Noise-masking Function
  (External Noise Filter is Unnecessary)
- Full-, Half (Two Kinds)-, Quarter-Step Functionality
- Open Detection Mask Time Selection Function
- Current Limit Mask Time Function
- Built-in Logic Input Pull-down Resistor
- Power ON Reset Circuit (POR)
- Thermal Shutdown Circuit (TSD)
- Over-Current Protection Circuit (OCP)
- Open Error Detection Circuit
- Diagnostics Output Circuit (Open Drain Output)
- Ultra-thin and High Heat-radiation
  (exposed metal type) Package

(Note 1) Grade 1

Package

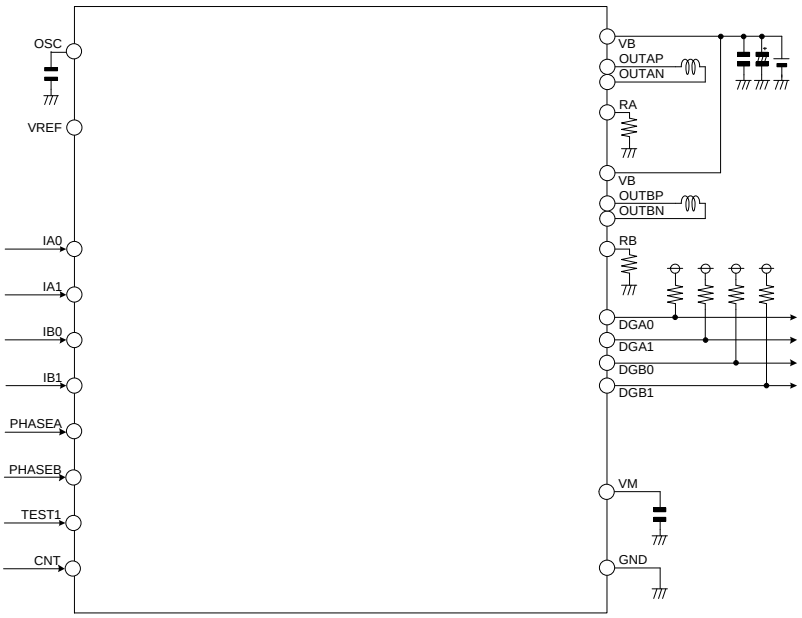
Package	W (Typ) x D (Typ) x H (Max)
HTQFP64BV	12.0 mm x 12.0 mm x 1.0 mm



Applications

- EGR Valve
- Printer, PPC, Scanner, Monitoring Camera, Sewing Machine and Robot.

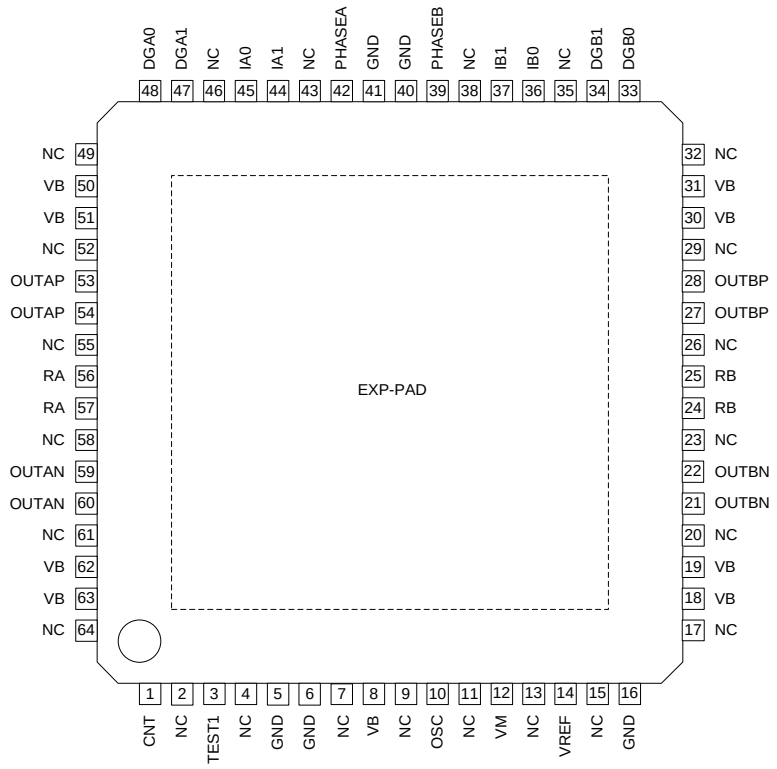
Typical Application Circuit



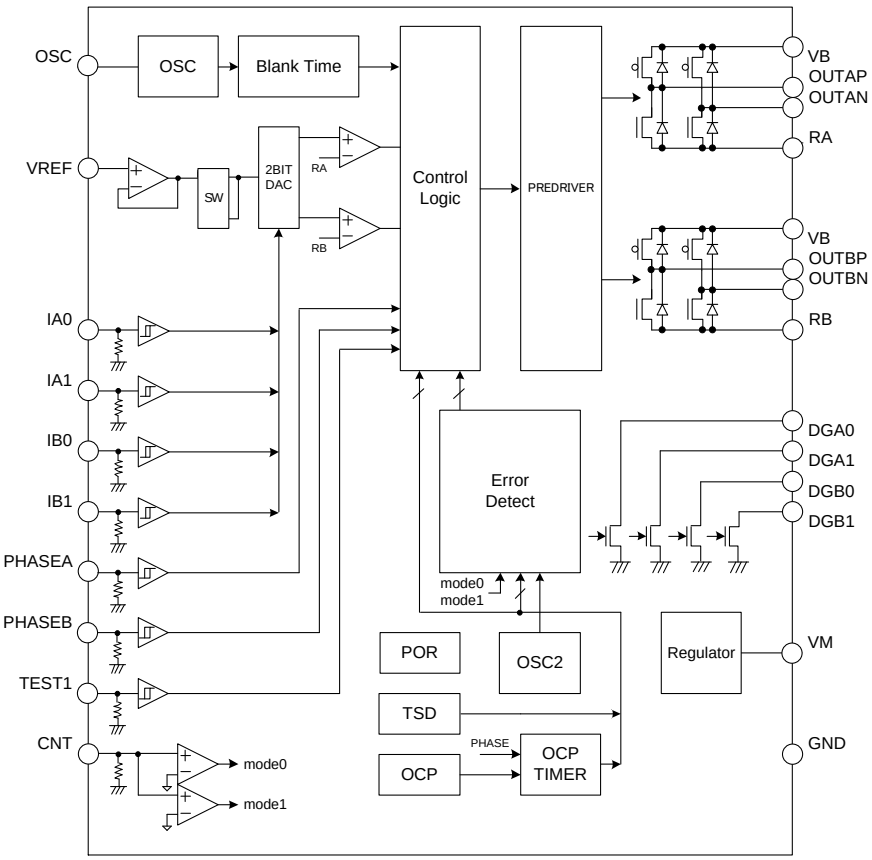
Contents

Pin Configuration

(TOP VIEW)



Block Diagram



Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	CNT	Open detection mask time selection	33	DGB0	PHASEB error detection output
2	NC	Non connection	34	DGB1	PHASEB error detection output
3	TEST1	Test pin (connect to GND for use)	35	NC	Non connection
4	NC	Non connection	36	IB0	PHASEB DAC division ratio setting
5	GND	Ground pin	37	IB1	PHASEB DAC division ratio setting
6	GND	Ground pin	38	NC	Non connection
7	NC	Non connection	39	PHASEB	PHASEB selection pin
8	VB	Power supply pin	40	GND	Ground pin
9	NC	Non connection	41	GND	Ground pin
10	OSC	Chopping frequency setting pin	42	PHASEA	PHASEA selection pin
11	NC	Non connection	43	NC	Non connection
12	VM	Regulator output pin	44	IA1	PHASEA DAC division ratio setting
13	NC	Non connection	45	IA0	PHASEA DAC division ratio setting
14	VREF	Output current value setting pin	46	NC	Non connection
15	NC	Non connection	47	DGA1	PHASEA error detection output
16	GND	Ground pin	48	DGA0	PHASEA error detection output
17	NC	Non connection	49	NC	Non connection
18	VB	Power supply pin	50	VB	Power supply pin
19	VB	Power supply pin	51	VB	Power supply pin
20	NC	Non connection	52	NC	Non connection
21	OUTBN	PHASEB H bridge output pin	53	OUTAP	PHASEA H bridge output pin
22	OUTBN	PHASEB H bridge output pin	54	OUTAP	PHASEA H bridge output pin
23	NC	Non connection	55	NC	Non connection
24	RB	Connection pin of resistor for PHASEB output current detection	56	RA	Connection pin of resistor for PHASEA output current detection
25	RB	Connection pin of resistor for PHASEB output current detection	57	RA	Connection pin of resistor for PHASEA output current detection
26	NC	Non connection	58	NC	Non connection
27	OUTBP	PHASEB H bridge output pin	59	OUTAN	PHASEA H bridge output pin
28	OUTBP	PHASEB H bridge output pin	60	OUTAN	PHASEA H bridge output pin
29	NC	Non connection	61	NC	Non connection
30	VB	Power supply pin	62	VB	Power supply pin
31	VB	Power supply pin	63	VB	Power supply pin
32	NC	Non connection	64	NC	Non connection
-	EXP-PAD	Connect EXP-PAD to GND	-	-	-

Function Description

1 PHASEA, PHASEB/Phase selection pin

These pins control the energization of H bridge output.

PHASEA	PHASEB	PHASEA energization status	PHASEB energization status
L	L	OUTAN→OUTAP	OUTBN→OUTBP
H	L	OUTAP→OUTAN	OUTBN→OUTBP
L	H	OUTAN→OUTAP	OUTBP→OUTBN
H	H	OUTAP→OUTAN	OUTBP→OUTBN

2 IA0, IA1, IB0, IB1/DAC division ratio setting pin

These pins control the divide ratio of internal 2bit DAC.

IA0 IB0	IA1 IB1	Output current level (%)
L	L	0
L	H	41.12
H	L	74.03
H	H	100

Each H bridge output pin is OFF when (Ix0, Ix1) is set to (L, L).

3 VB/Power supply pin

Design a thick and short wire with low impedance because the motor drive current flows in this pin. Always arrange the bypass capacitors (47 µF to 470 µF) close to the pin as much as possible, and adjust the stability of VB voltage because VB voltage may have large fluctuations due to counter electromotive force of the motor, PWM switching noise and etc.

Increase the capacitor load as needed especially when using large current, and motors with high counter electromotive force. Further, we recommend placing 0.01 µF to 0.1 µF multilayer ceramic capacitor in parallel to lower the impedance of power supply in a wide frequency band. Always make sure that the VB voltage does not exceed the rating even for a short period of time. Although VB is shorted inside the IC, it must also be shorted externally. Otherwise, malfunction or destruction may occur because of current route convergence if it is used without shorting.

In addition, clamp element for preventing electrostatic damage is embedded in the power supply pin. This clamp element will function when a steep pulse signal is applied or there is a surge of voltage that exceeds the absolute maximum rating, and that may lead into destruction. Therefore, avoid exceeding the absolute maximum rating. It is also effective to attach a Zener diode of the absolute maximum rating. Also, take note that IC may breakdown when inverse voltage is applied to VB pins and GND pins.

4 GND/Ground pin

In order to reduce the noise caused by switching current and the stabilization of internal reference voltage of IC, minimize the wiring impedance from this pin as much as possible to achieve the lowest electrical potential in any operating conditions. Also, design a pattern that does not have common impedance with other GND patterns.

Function Description - continued

5 OUTAP, OUTAN, OUTBP, OUTBN/H bridge output pin

Design a thick and short wire with low impedance because the motor drive current flows in this pin. It is also useful to add a Schottky diode if output has high positive or negative fluctuation when large current is used. For example, a counter electromotive voltage is high. When a steep pulse signal is applied or there is a surge of voltage that exceeds the absolute maximum rating, and that may lead into destruction. Therefore, avoid exceeding the absolute maximum rating. Further, when a capacitor is inserted between output and GND, set the capacitance load (Max 6700 pF) so that output current will not go over the regulated value.

6 VREF/Output current value setting pin

This is the pin to set the output current value. The output current setting mode can be set by the voltage of VREF pin. Below formula shows the output current when VREF voltage is within input range (Max 3.0 V).

$$I_{OUT} = \frac{V_{VREF}}{3} \times \frac{1}{Rx} \quad [A]$$

Where:

I_{OUT}	is the Output current
V_{VREF}	is the VREF Input Voltage.
R_X	is the Current-sensing resistor

When VREF is supplied by resistor divider, decide the resistance value in consideration of output current (Max 10 µA).
When using open VREF pin, the voltage pin becomes V_{REFLIN}: 3.4 V (Typ) or more due to internal pull-up resistor. Therefore, the setting mode changes and the output current value becomes the internal setting value (refer to Electrical Characteristics).
The minimum current that can be controlled by VREF voltage is decided by the L and R components of the motor coil and the minimum ON time in PWM drive.

7 RA, RB/Connection pin of resistor for detecting of output current

This is the pin to connect the resistor for detecting output current. When using open the VREF pin, insert resistor for detecting current to GND. To select resistor, RA and RB voltage should not exceed 1.2 V maximum applied voltage under the usage condition. Also, determine the resistor value in such a way that W = I_{OUT}^2 x R[W] will not exceed the power consumption of the resistor. Further, the pattern of the RA pin, the RB pin – resistor for current detection – GND should be wired with low impedance because drive current flows. Ensure that there is no common impedance with other GND patterns. When RA, RB pins are shorted to GND, normal PWM current could not be controlled, thus large current will flow. Be careful because OCP or TSD may function.
When 0.125 V (Typ) or less the RA pin or the RB pin is detected to be t_{OPND} (2.5 ms (Typ)) or more, output load can be judged as open, and the open error diagnostics signal is outputted.
Current flows in H bridge low side output, and when 2.5 V (Typ) or more the RA pin or the RB pin is detected to be t_{OCPMSK} (2 µs (Typ)) or more, it is in over current status. H bridge output is turned OFF at a certain time and short error diagnostics signal is outputted.
When RA pin or RB pin is open, the input pin voltage increases due to internal pull-up resistor. The IC judges RA resistor or RB resistor is open when the IC detects that the RA and RB pin voltage is 3.4 V (Typ) or more with t_{OPND} (2.5 ms (Typ)) or more. The upper side output of H bridge is turned ON, and open error diagnostics signal is outputted.
When RA pin and RB pin voltage are over the rating (6.5 V), there is a possibility of circuit malfunction. Therefore, avoid exceeding the ratings.

8 OSC/Connection pin for setting chopping frequency

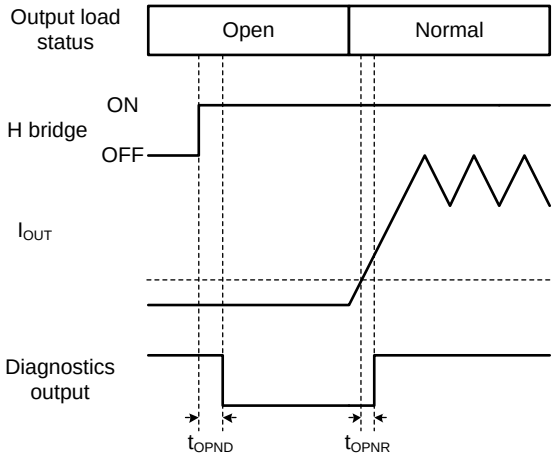
This is the pin to set the chopping frequency of output. Connect the external capacitor (330 pF to 6800 pF) between this pin and GND. Refer to Page 12 for the details of frequency setting method. The variable frequency range is 20 kHz to 175 kHz.
For the connection of external capacitor to GND, ensure that there will be no common impedance with other GND patterns. In addition, avoid getting close to connections of steep pulses such as square wave. Make a pattern design that there will be little noise plunging. When the OSC pin is open or it is biased externally, normal PWM constant current cannot be controlled. Therefore always mount a capacitor if to be used to control PWM constant current.

Function Description - continued

9 DGA0, DGA1, DGB0, DGB1/Error detection output pin

This is the error status output for Open, Short (over current) and overheating of output load and RA and RB resistor.
This pin structure is open drain output so use the external resistor (1 kΩ to 100 kΩ) connected to 7 V or less power supply.

DGA0 DGB0	DGA1 DGB1	Status	Control prioritize of H bridge and Diagnostics output
H	H	No Error	-
H	L	Open Error Not energization mode	3
L	H	Short Error	2
L	L	Thermal Error	1



10 CNT/Open detection mask time selection pin

This pin control the open detection mask time.

CNT	Open Detection Mask Time
L	2.5 ms (Typ)
M	10.0 ms (Typ)
H	5.0 ms (Typ)

The CNT pin is connected to 100 kΩ (Typ) internal pull-down resistor.
Open or connect to GND in order to control L. Connect external resistor (95 kΩ to 105 kΩ) between CNT and VM in order to control M and connect to VM in order to control H.

11 VM/Regulator output pin

This pin is 5 V (Typ) output. Connect the external Capacitor (0.01 μF to 1 μF) between this pin and GND.

12 TEST1 pin

This is the pin to use during IC shipment test. Connect to GND and use.

13 Non connection

This pin is not electrically connected to IC internal circuit.
Since NC terminals are placed in consideration of adjacent pin shorts, use as open as possible.

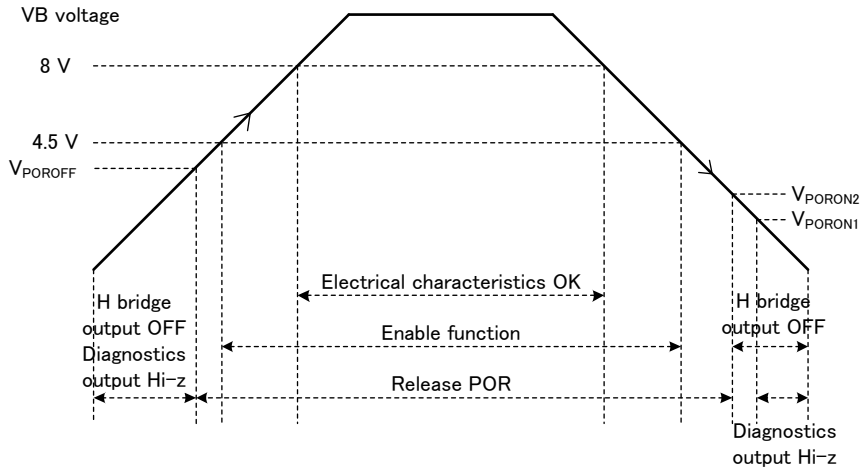
14 IC Back Metal

The HTQFP64BV package has a metal for heat dissipation at the back of the IC. Since it is assumed to be used by applying heat dissipation treatment to this metal, always connect with GND plane on the board with solder. Use with wide GND pattern to ensure sufficient heat dissipation area. Further, the backside metal is shorted with the IC's backside, which makes it a GND potential. Never pass the wiring pattern other than GND at the back of IC because there is a possibility of malfunction and destruction when it is shorted to other potential than GND.

Protection Circuits

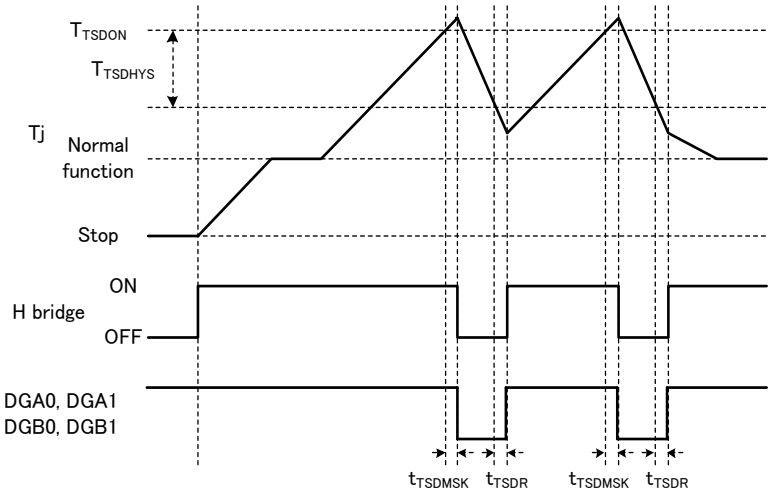
1 Power ON reset circuit (POR)

This IC has a built-in Power On reset circuit to prevent H bridge output malfunction caused by low level power supply.
When VB input voltage is V_{PORON2} (3.85 V(Typ)) or less during decreasing VB input voltage, H bridge output is set to OFF and the diagnostics output is hold V_{PORON2} state. When VB input voltage is V_{PORON1} (2.8 V(Typ)) or less, the diagnostics output is set to Hi-z. And When VB input voltage is V_{POROFF} (4.1 V(Typ)) or more, the diagnostics output is recovered to normal function automatically.
During VB input voltage is between 4.0 V and 8.0 V, Motor, Diagnostics and Error protection functions enable. But Electrical Characteristics are not guaranteed.



2 Thermal Shutdown circuit (TSD)

This IC has a built-in thermal shutdown circuit for protection against overheating. If the chip temperature of the IC is 175 °C (Typ) or above with t_{TSDMSK} (2 µs (Typ)) or more, the H bridge output detected overheating will become open and overheating error signal is output from the diagnostics pin. H bridge output and diagnostics output will automatically return to normal operation when the temperature goes 160 °C (Typ) or below with t_{TSDR} (2 µs (Typ)) or more. However, even when TSD is in operation, if heat is continuously applied externally, it will result in thermal runaway and can lead to destruction of the IC.



Protection Circuits - continued

3 Over Current Protection circuit (OCP)

This IC has a built-in over current protection circuit as a provision against destruction when the H bridge outputs are shorted each other or VM-motor output or motor output-GND is shorted. This circuit control the H bridge output to OFF condition for t_{OCPOFF} (400 µs(Typ)) and output short (Over Current) error signal from the diagnostics pin when the regulated threshold current flows for t_{OCPMSK} (2 µs (Typ)).

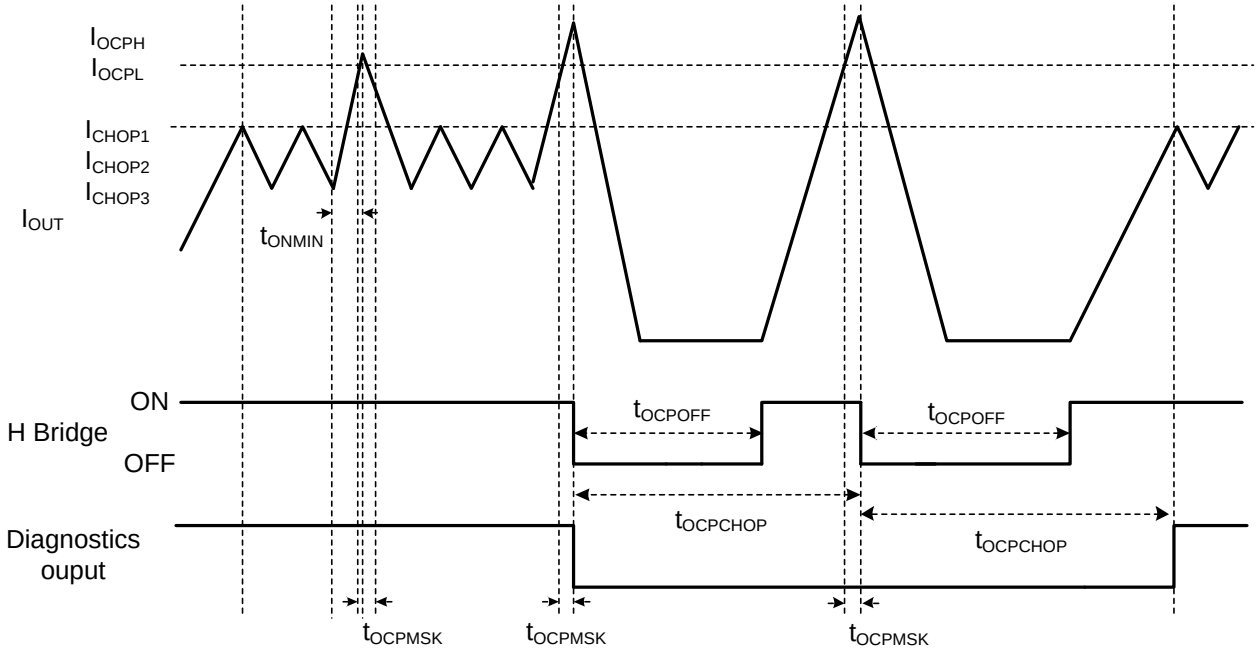
And then when over current is detected again within $t_{OCPCHOP}$ (800 µs(Typ)), the diagnostics pin status is hold. And PHASE signal is changed during over current status, the diagnostics pin is reset and H bridge output is recovered from OFF state.

The overcurrent protection circuit is designed to prevent the breakdown of IC caused by overcurrent in abnormal conditions such as shorted motor outputs. This protection is not intended to guarantee the protection of application circuit. Therefore, do not design the protection of the system using this circuit function.

After detecting over current, then power-on again or by reset while IC is still in abnormal state, the OCP operates repeatedly ("latch → recover → latch"). Note that the IC may generate heat and may lead to deterioration of the IC.

When the L value is large due to long wires, there is a possibility of destruction of the IC after the over current has flowed and the output pin voltage suddenly jumps to a value that is over the absolute maximum ratings.

If the current is the OCP detection current level or below and the output current rating level or above, the IC can heat up, exceed Tjmax = 150 °C and then deteriorate, so current which exceeds the output rating should not be applied.

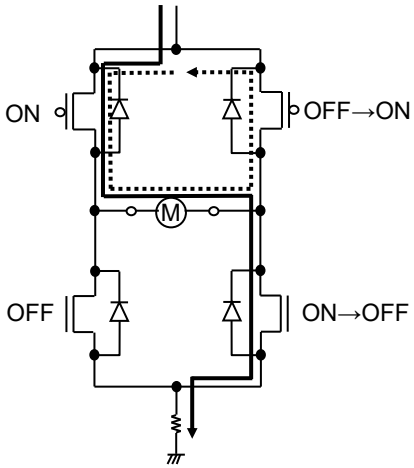


4 Operation Under Strong Electromagnetic Field

The IC is not designed for using in the presence of strong electromagnetic field. Be sure to confirm that no malfunction is found when using the IC in a strong electromagnetic field.

Current Decay Mode

The following diagrams show the state of H bridge output and the regenerative current path during the in SLOW DECAY mode.



Output ON Time

Current Decay Time

SLOW DECAY

During current attenuation, the voltage between motor coils is low, and the current ripple is few because the regeneration current decreases slowly. This is favorable for keeping motor torque. However, in the lower operating current condition, the output current increases because of lower controllability of current. And in using HALF STEP and QUATER STEP with high-pulse-rate driving, the current waveform cannot follow the change of the current target due to the influence of motor back electromotive voltage. As the result, the distortion and motor vibration are increased. Thus, this decay mode is most suited to FULL STEP modes, or low-pulse-rate HALF STEP or QUARTER STEP modes.

PWM Constant Current Control

1 Current control operation

The output current increases when the H bridge output is turned on. When the RA and RB voltage that is converted the output current by detection resistance reaches the level set by internal setting value or VREF input voltage and 2bit DAC in IC, the current limit comparator operates, then the IC enters current decay mode. After decay time set by timer, the output transistor turns on again. This sequence repeats continuously.

2 Noise-masking function

In order to avoid misdetection of H bridge output current due to RA and RB spike noise that may occur when the output turns ON, the IC has the minimum ON time t_{ONMIN} (Blank time). The current detection is invalid from the output transistor turned on to t_{ONMIN}. This allows for constant-current drive without the need for an external filter.
The minimum ON time shows the time after dead time from current decay mode to ON again during current limit function.
In addition, take note that IC enters current decay mode when RA and RB pin voltage reach the setting voltage or more and minimum on time or more by discharge from the capacitor inserted between output and GND.

3 Timer

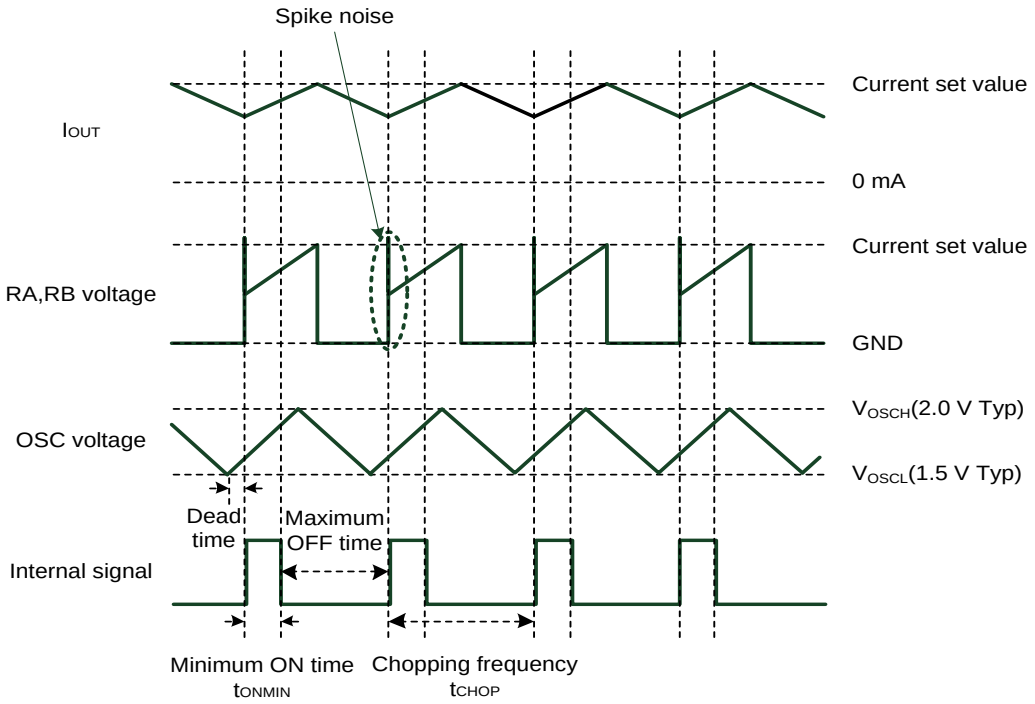
The OSC pin is repeatedly charged and discharged between the V_{OSCH} and V_{OSCL} levels through the external capacitor.The detection of the current-sense comparator is disabled while charging from V_{OSCL} level through dead time to constant time (0.75 µs (Typ)). This period is the minimum ON time: t_{ONMIN}. When the output current reach the target current during from t_{ONMIN} to next V_{OSCL} level, the IC enters current decay mode. When OSC is discharged to V_{OSCL} level, IC recovers to output ON mode from current decay mode. At the same time, IC starts charging again. The chopping period is defined by external capacitance value. The calculation formula is as follows.

$$t_{CHOP} = 2 \times C \times \frac{V_{OSCH} - V_{OSCL}}{90 \times 10^{-6}} \text{ [s]}$$

Where:

t_{CHOP}	is the Chopping period
C	is the External capacitance
V_{OSCH}	is the 2.0 V (Typ)
V_{OSCL}	is the 1.5 V (Typ)

When the phase is changed during decay mode, H bridge output recovers ON mode and there is phase change minimum on time: $t_{ONMINPH}$ (5 µs (Typ)).



There is a risk that the output current may exceed the setting value due to the internal L and R components of the output motor coil (recommended value is 330 pF to 6800 pF). Also, ensure that the chopping period (t_{CHOP}) is not set longer than necessary, as doing so will increase the output ripple, thereby decreasing the average output current and yielding lower output rotation efficiency. Select optimal value so that motor drive sound, and distortion of output current waveform can be minimized.

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V_{VB}	-0.3 to +35.0	V
Input Voltage Range for Control Pin (PHASEA, PHASEB, IA0, IA1, IB0, IB1, CNT, VREF, TEST1)	V_{IN}	-0.5 to +6.5	V
Diagnostics Pin Voltage Range (DGA0,DGA1,DGB0,DGB1)	V_{DG}	-0.5 to +6.5	V
Diagnostics Pin Current (DGA0,DGA1,DGB0,DGB1)	I_{DG}	+2	mA
RA,RB Maximum Input Voltage	V_R	+6.5	V
Output Current	I_{OUT}	±1.8*(Note 1)*	A/Phase
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Do not exceed Tjmax = 150 °C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
HTQFP64BV				
Junction to Ambient	θ_{JA}	63.4	14.9	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	2	1	°C/W

(Note 2) Based on JESD51-2A(Still-Air)

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5,7

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connects with the copper pattern of all layers.

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{VB}	4.5	14.0	18.0	V
Maximum Output Current *(Note 1)*	I_{OUT}	-	-	1.3	A/Phase
RA, RB Maximum Voltage	V_R	-	-	1.2	V
Operating Temperature	Topr	-40	+25	+125	°C

(Note 1) Do not exceed Tjmax = 150 °C.

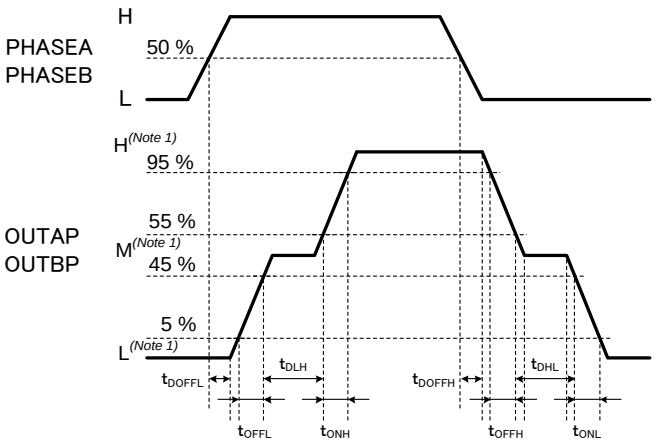
Electrical Characteristic (Unless otherwise specified V_{VB} = 8 V to 18 V, Tj = -40 °C to +125 °C)

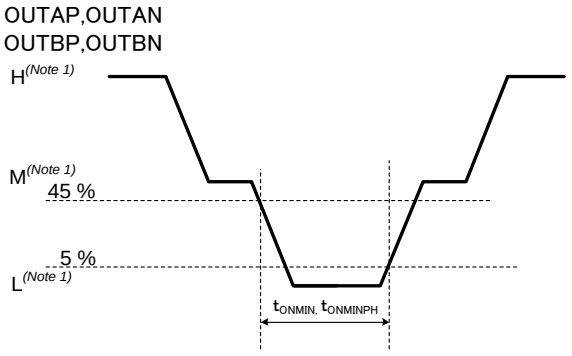
Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
[Whole]						
Circuit Current	I_B	-	4	10	mA	
Power ON Reset Voltage 1	V_{PORON1}	2.5	2.8	3.1	V	
Power ON Reset Voltage 2	V_{PORON2}	3.50	3.85	4.20	V	
Power ON Reset Release Voltage	V_{POROFF}	3.7	4.1	4.5	V	
POR2 Hysteresis Voltage	$V_{POR2HYS}$	0.05	0.30	0.50	V	V_{POROFF} - V_{PORON2}
VM Voltage	V_{VM}	4.7	5.0	5.3	V	I_{VM} = 1 mA
[Control input] (PHASEA, PHASEB, IA0, IA1, IB0, IB1)						
H-level Input Voltage	V_{INH}	3.1	-	-	V	
L-level Input Voltage	V_{INL}	-	-	1.5	V	
Input Hysteresis Voltage	V_{INHYS}	-	0.1	-	V	
H-level Input Current	I_{INH}	10	50	100	µA	V_{IN} = 5 V
L-level Input Current	I_{INL}	-10	0	+10	µA	V_{IN} = 0 V
[Control input] (CNT)						
H-level Input Voltage	V_{CNTH}	V_{VM} x 0.8	-	-	V	
M-level Input Voltage	V_{CNTM}	V_{VM} x 0.4	-	V_{VM} x 0.6	V	
L-level Input Voltage	V_{CNTL}	-	-	V_{VM} x 0.2	V	
H-level Input Current	I_{CNTH}	10	50	100	µA	V_{CNT} = 5 V
L-level Input Current	I_{CNTL}	-10	0	+10	µA	V_{CNT} = 0 V
[H bridge output] (OUTAP, OUTAN, OUTBP, OUTBN)						
Output ON Resistance (total of upper and lower resistors)	R_{ON}	-	0.35	1.00	Ω	I_{OUT} = ±1 A
Output Leak Current	I_{LEAK}	-	-	10	µA	
[Current control]						
RA, RB Input Current	I_R	-100	-50	-10	µA	V_{RA} = V_{RB} = 0 V V_{IA0} = V_{IA1} = V_{IB0} = V_{IB1} = 0 V
VREF Input Current	I_{VREF}	-10	-5	-1	µA	V_{VREF} = 0 V
VREF Input Voltage	V_{VREF}	0	-	3.0	V	
VREF Mode Change Voltage *(Note 2)*	V_{REFLIN}	3.1	3.4	3.9	V	
Comparator Threshold	V_{CTH}	843	878	917	mV	V_{IA0} = V_{IA1} = V_{IB0} = V_{IB1} = 5 V
Current Limit Mask Time	t_{CLMASK}	0.10	0.20	0.35	µs	
[Diagnostics output] (DGA0, DGA1, DGB0, DGB1)						
Output L Voltage	V_{DG}	-	0.15	0.50	V	I_{DG} = 1 mA
Output Leak Current	I_{DG}	-10	0	+10	µA	V_{DG} = 5 V

(Note 2) The Voltage to change Output Current Value setting to IC Internal Setting Value Mode.

Electrical Characteristic (Unless otherwise specified V_{VB} = 8 V to 18 V, Tj = -40 °C to +125 °C) - continued

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Chopping Frequency Accuracy	$f_{CHOPACC}$	-25	0	+25	%	IC standalone, C = 2200 pF
Chopping Current 1	I_{CHOP1}	288	361	422	mA	IC standalone, RA = RB = 1 Ω, (IA0, IA1) = (IB0, IB1) = (L, H)
Chopping Current 2	I_{CHOP2}	583	650	717	mA	IC standalone, RA = RB = 1 Ω, (IA0, IA1) = (IB0, IB1) = (H, L)
Chopping Current 3	I_{CHOP3}	843	878	917	mA	IC standalone, RA = RB = 1 Ω, (IA0, IA1) = (IB0, IB1) = (H, H)
TSD On Temperature	T_{TSDON}	150	175	200	°C	Not 100% tested.
TSD Hysteresis Temperature	T_{TSDHYS}	5	15	25	°C	Not 100% tested.
OCP Detection Current (Source)	I_{OCPH}	2.0	3.0	5.0	A	
OCP Detection Current (Sink)	I_{OCPL}	2.0	2.5	3.0	A	RA = RB = 1 Ω
Minimum On Time (brank time)	t_{ONMIN}	0.35	0.75	1.10	µs	VREF = OPEN, V_{RA} = V_{RB} = 1 V, Pull-up = Pull-down = 100 Ω
Output Upper Rise Time	t_{ONH}	20	60	200	ns	V_{VB} = 14 V
Output Upper Fall Time	t_{OFFH}	-	60	200	ns	V_{VB} = 14 V
Output Upper Off Delay Time	t_{DOFFH}	-	150	300	ns	V_{VB} = 14 V
Output Lower Rise Time	t_{ONL}	20	60	200	ns	V_{VB} = 14 V
Output Lower Fall Time	t_{OFFL}	-	60	200	ns	V_{VB} = 14 V
Output Lower Off Delay Time	t_{DOFFL}	-	150	300	ns	V_{VB} = 14 V
Dead Time (L to H)	t_{DLH}	100	350	800	ns	
Dead Time (H to L)	t_{DHL}	100	350	800	ns	
Diagnostics Output Delay Time	t_{DDG}	-	2	20	µs	Pull-up = 10 kΩ, C = 50 pF
Thermal Detection Mask Time	t_{TSDMSK}	-	2	6	µs	
Thermal Detection Release Time	t_{TSDR}	-	2	6	µs	
Over Current Detection Mask Time	t_{OCPMSK}	-	2	6	µs	
OCP Off Time	t_{OCPOFF}	-	400	-	µs	
OCP Chopping Judgement Period	$t_{OCPCHOP}$	-	800	-	µs	
Open Detection Mask Time	t_{OPND}	0.8	2.5	7.0	ms	CNT = L
Open Detection Release Time	t_{OPNR}	1.0	2.5	6.0	µs	CNT = L
Output Load Open Detection Voltage	V_{OPNOUT}	40	125	200	mV	
RX Open Detection Voltage	V_{OPNRX}	-	3.4	-	V	
PHASE Change Minimum on Time	$t_{ONMINPH}$	1	5	10	µs	VREF = OPEN, V_{RA} = V_{RB} = 1 V, Pull-up = Pull-down = 100 Ω





(Note 1) H: VB±1 V, M: VB/2±1 V, L: ±1 V

Typical Performance Curve (reference data)

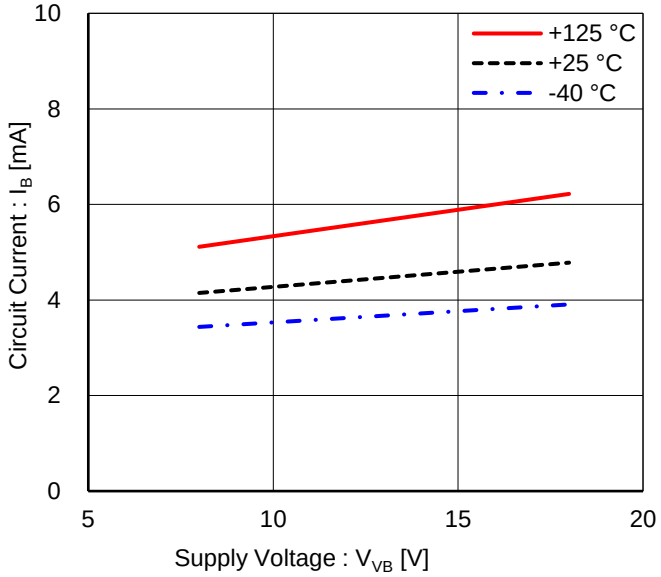


Figure 1. Circuit Current vs Supply Voltage

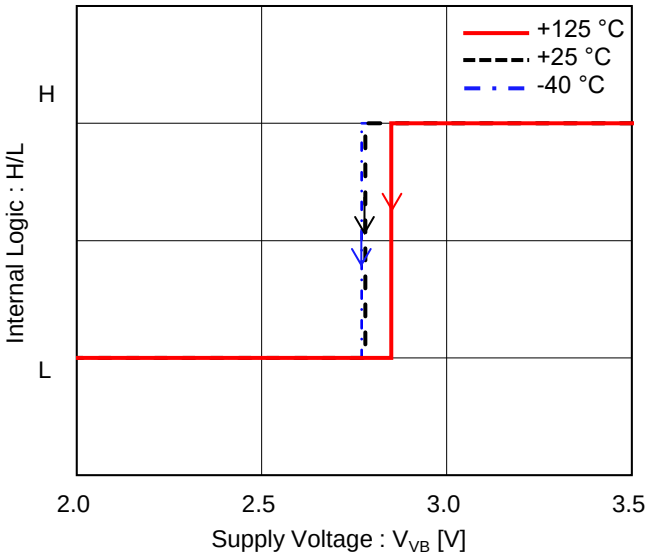


Figure 2. Internal Logic vs Supply Voltage
(Power On Reset Voltage 1)

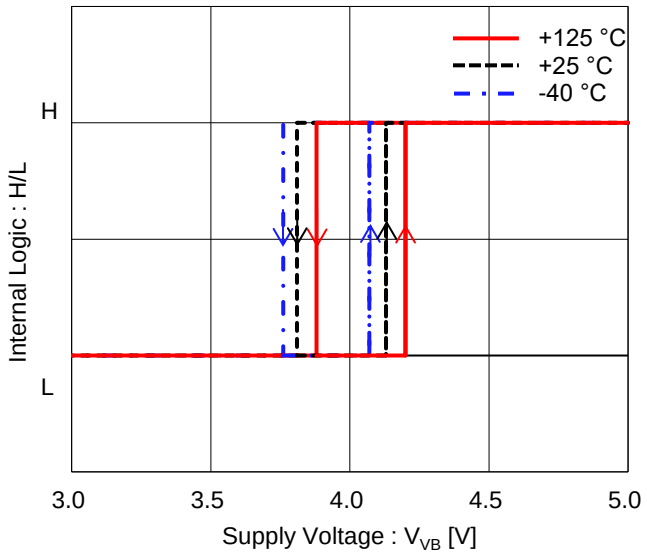


Figure 3. Internal Logic vs Supply Voltage
(Power On Reset Voltage 2, Reset Release Voltage)

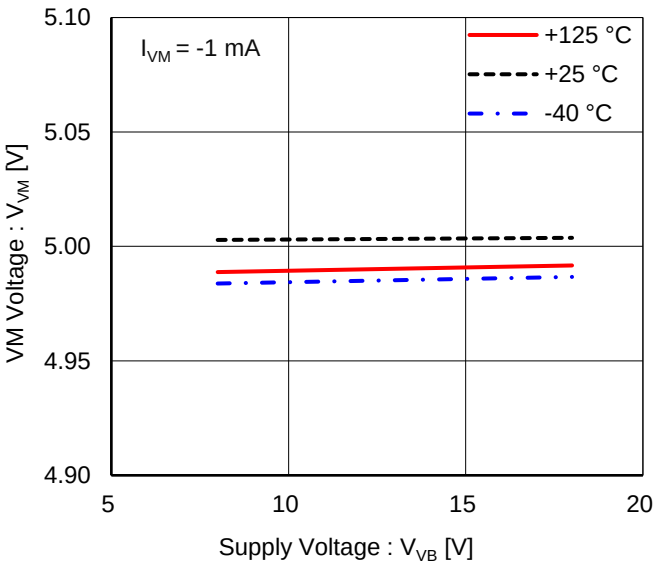


Figure 4. VM Voltage vs Supply Voltage

Typical Performance Curve (reference data) - continued

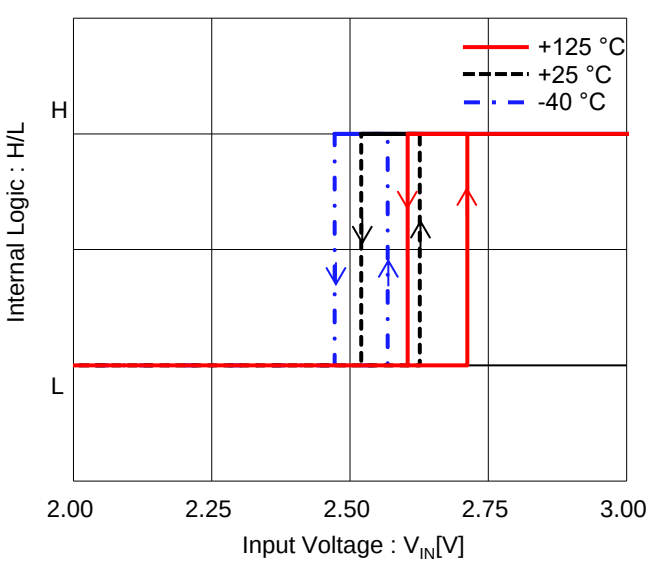


Figure 5. Internal Logic vs Input Voltage
(Control Pin Input Voltage)

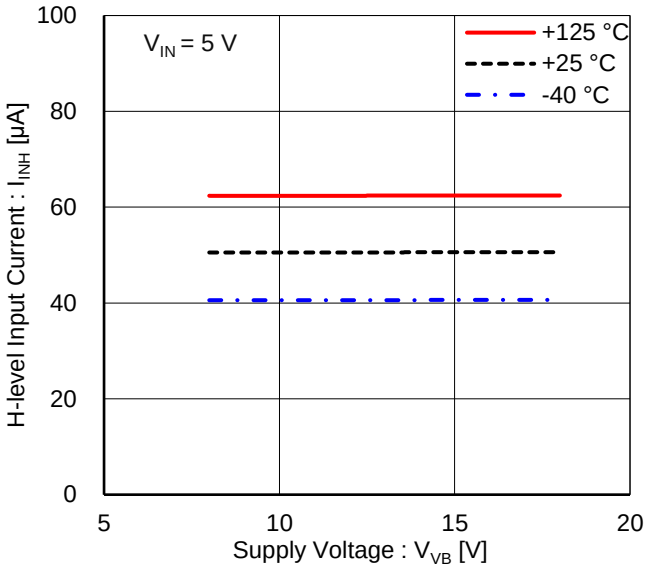


Figure 6. H-level Input Current vs Supply Voltage
(Control Pin H Level Input Current)

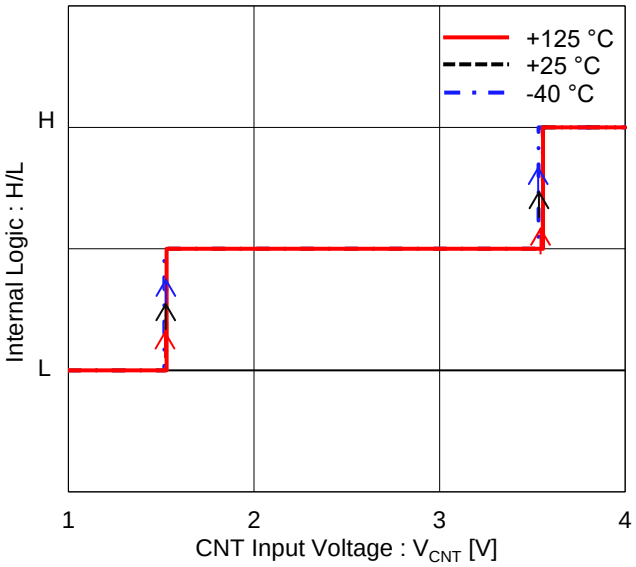


Figure 7. Internal Logic vs CNT Input Voltage
(CNT Pin Input Voltage)

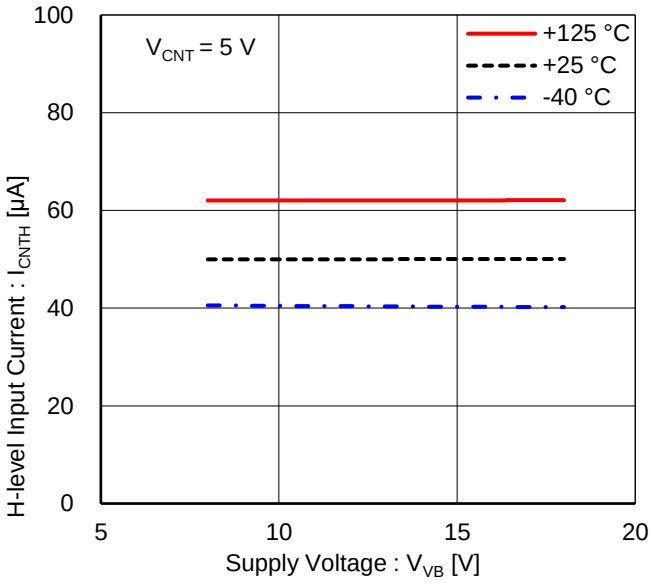


Figure 8. H-level Input Current vs Supply Voltage
(CNT Pin H Level Input Current)

Typical Performance Curve (reference data) - continued

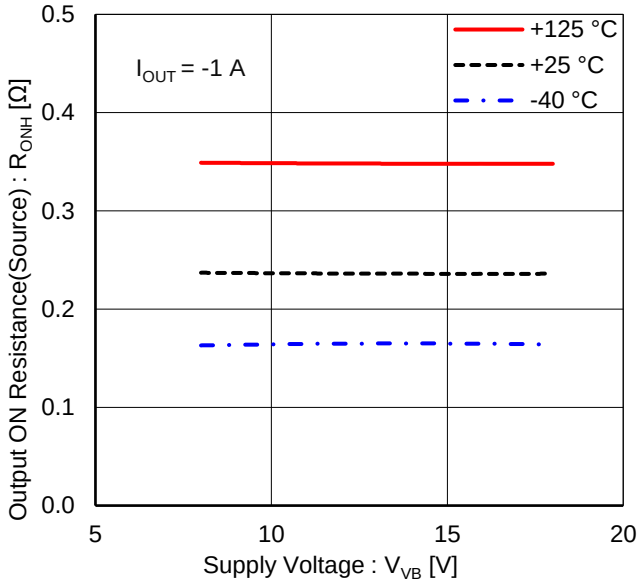


Figure 9. Output ON Resistance (Source) vs Supply Voltage

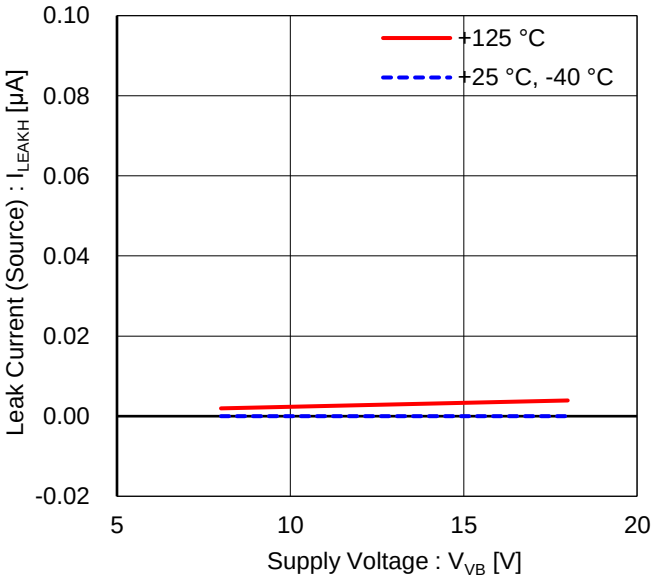


Figure 10. Leak Current (Source) vs Supply Voltage

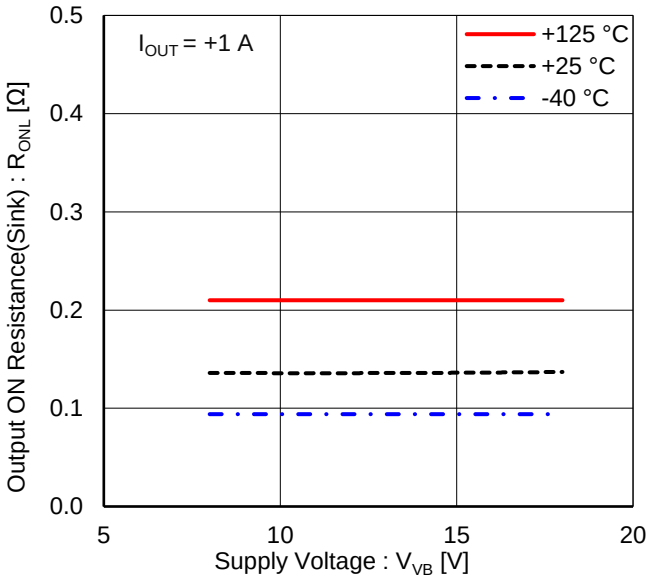


Figure 11. Output ON Resistance (Sink) vs Supply Voltage

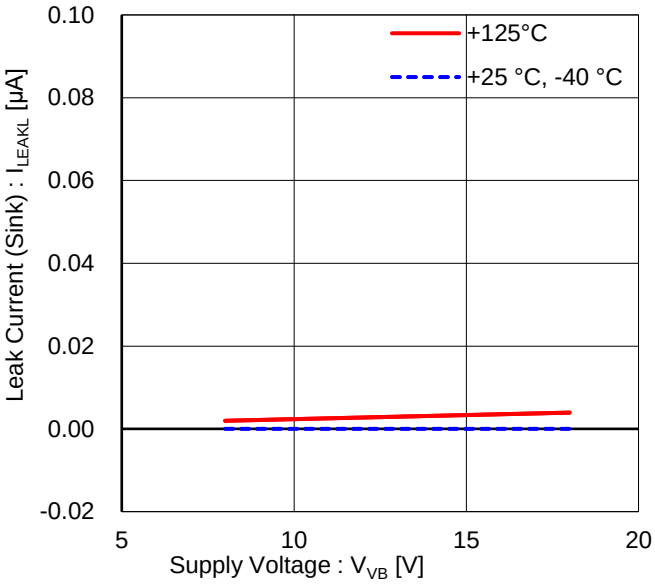


Figure 12. Leak Current (Sink) vs Supply Voltage

Typical Performance Curve (reference data) - continued

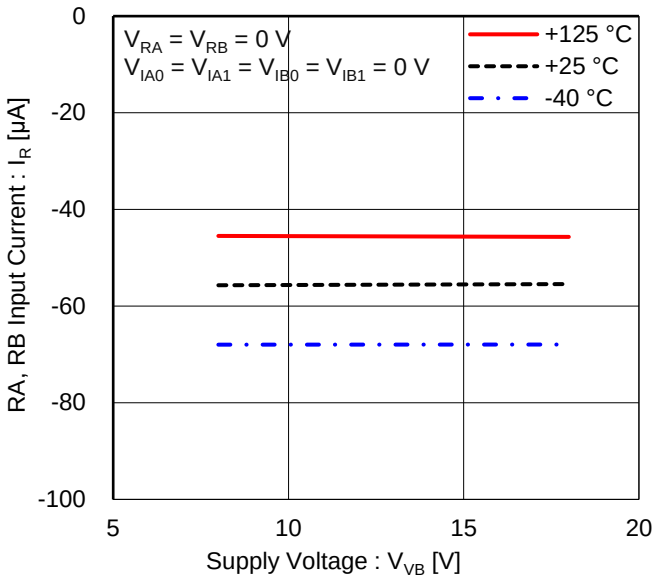


Figure 13. RA, RB Input Current vs Supply Voltage

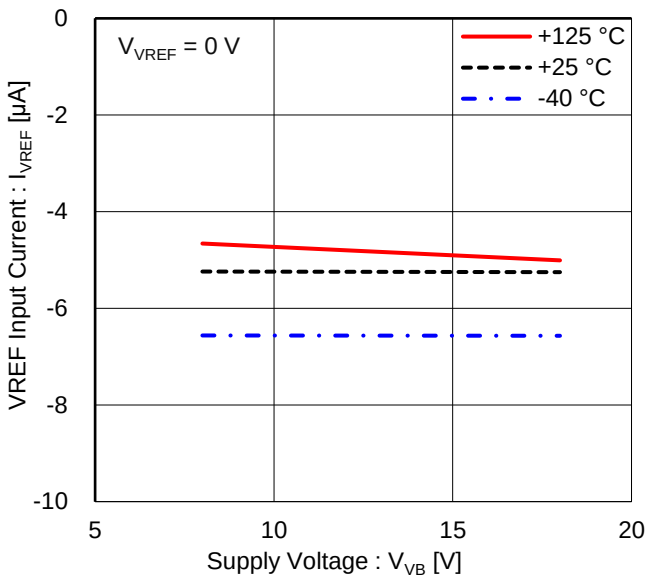


Figure 14. VREF Input Current vs Supply Voltage

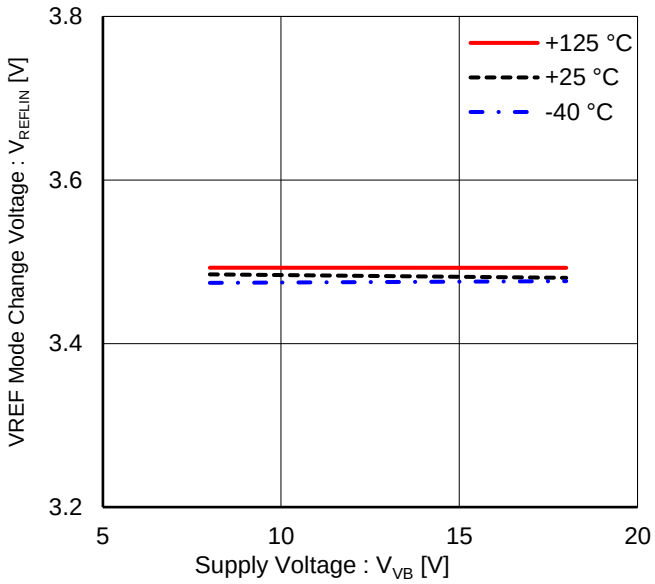


Figure 15. VREF Mode Change Voltage vs Supply Voltage

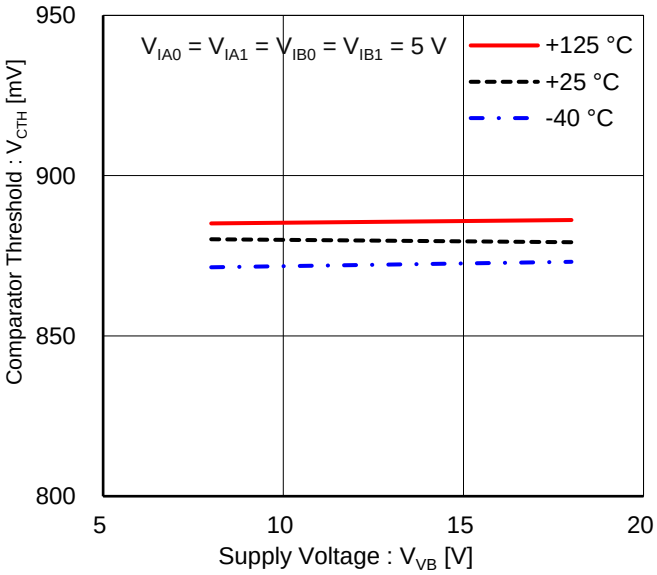


Figure 16. Comparator Threshold vs Supply Voltage

Typical Performance Curve (reference data) - continued

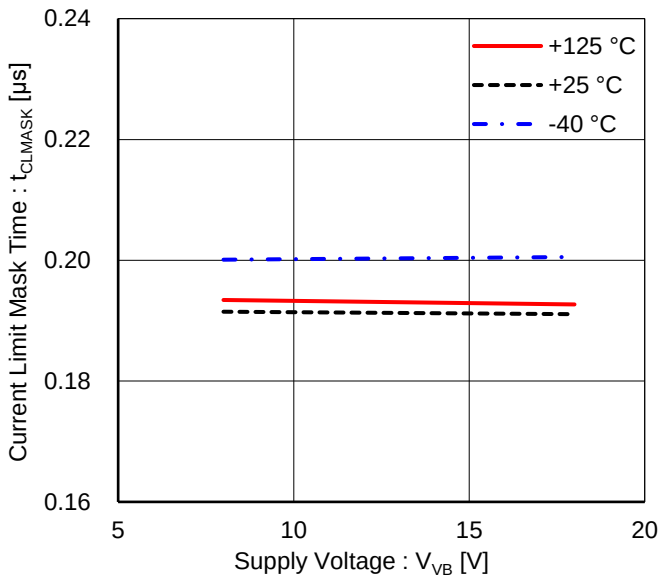


Figure 17. Current Limit Mask Time vs Supply Voltage

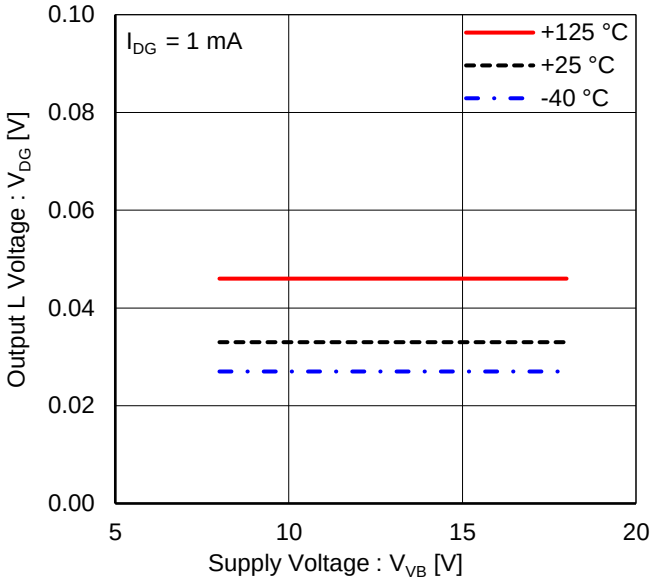


Figure 18. Output L Voltage vs Supply Voltage
(Diagnostics Output L Voltage)

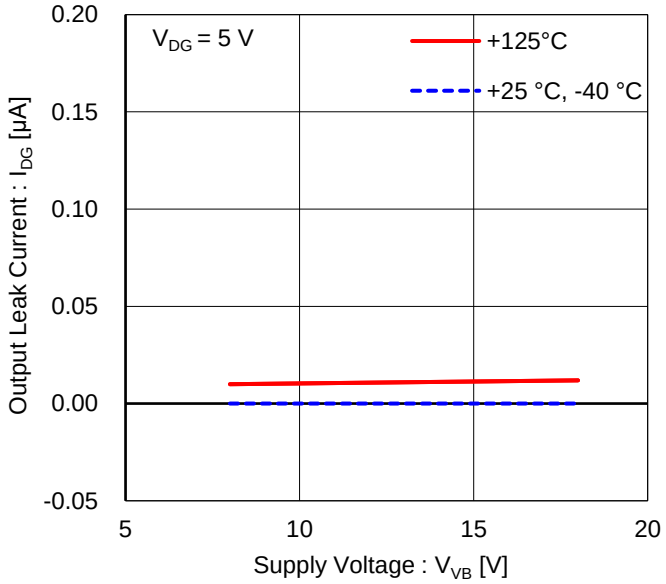


Figure 19. Output Leak Current vs Supply Voltage
(Diagnostics Output Leak Current)

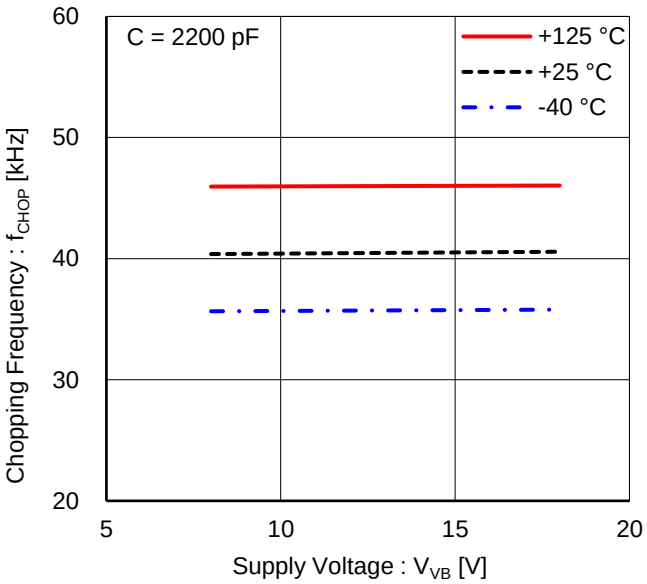


Figure 20. Chopping Frequency vs Supply Voltage

Typical Performance Curve (reference data) - continued

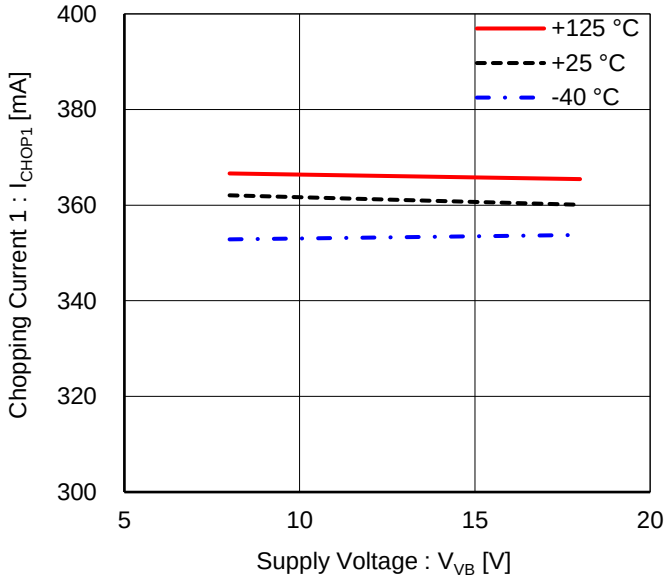


Figure 21. Chopping Current 1 vs Supply Voltage

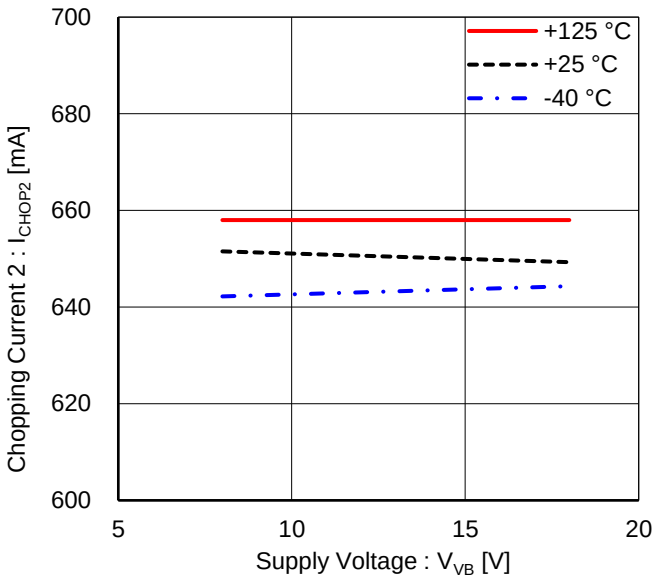


Figure 22. Chopping Current 2 vs Supply Voltage

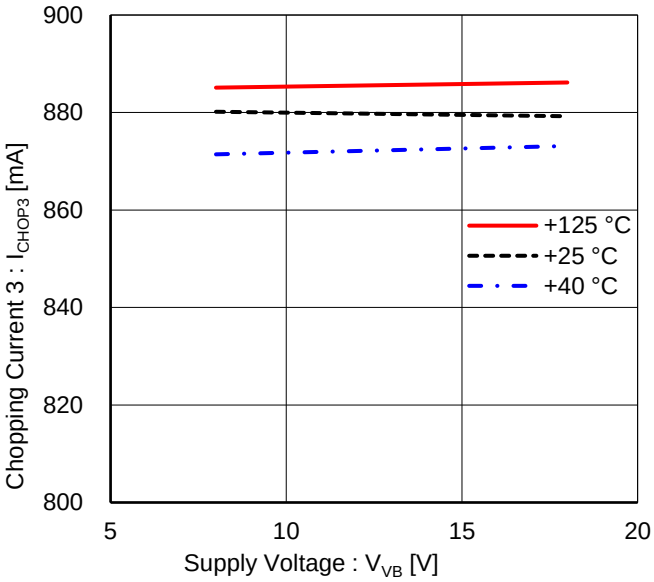


Figure 23. Chopping Current 3 vs Supply Voltage

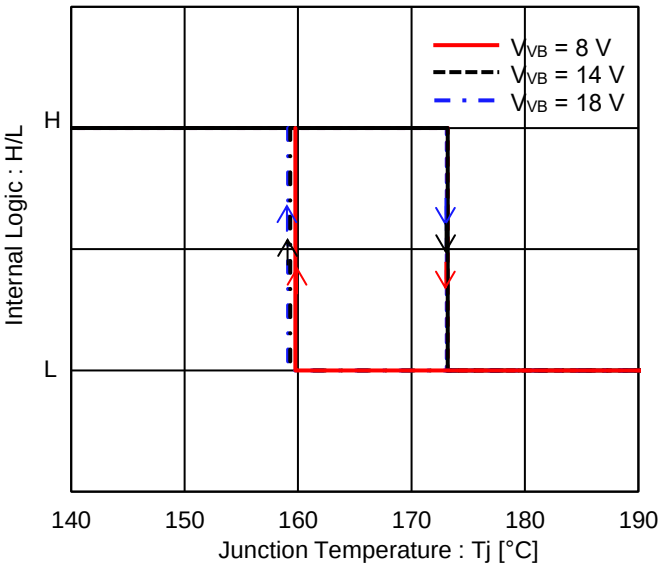


Figure 24. Internal Logic vs Junction Temperature (Thermal Shutdown)

Typical Performance Curve (reference data) - continued

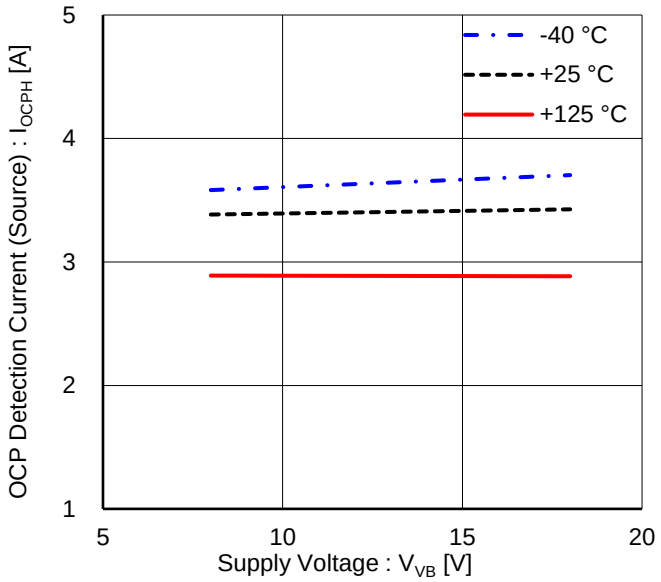


Figure 25. OCP Detection Current (Source) vs Supply Voltage

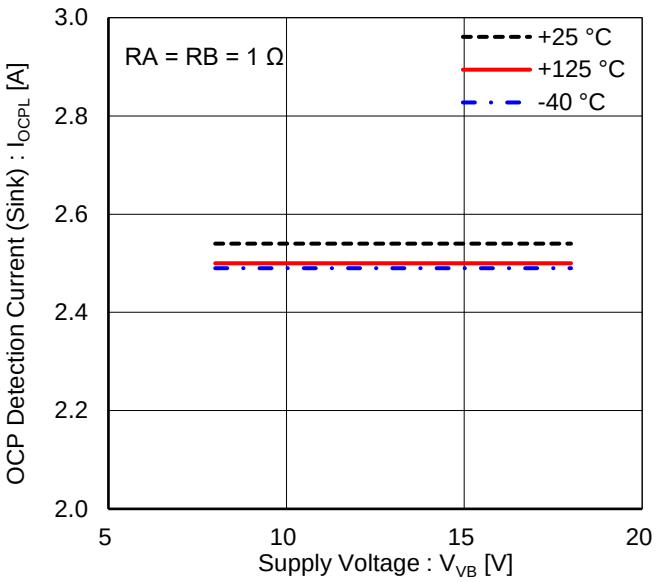


Figure 26. OCP Detection Current (Sink) vs Supply Voltage

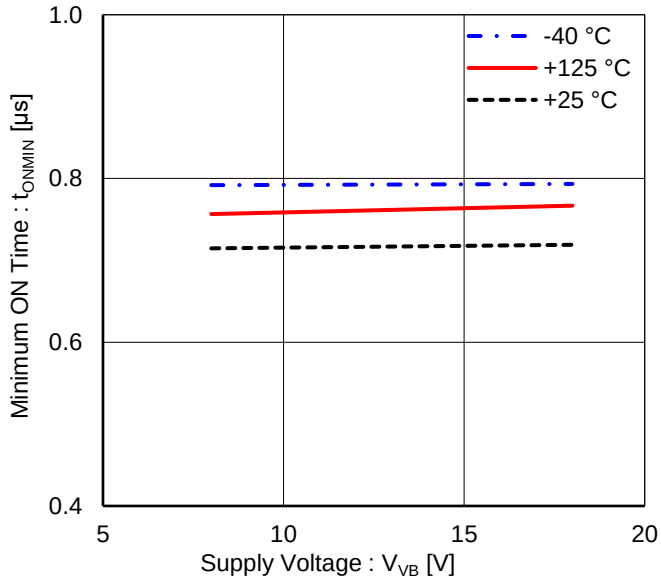


Figure 27. Minimum ON Time vs Supply Voltage

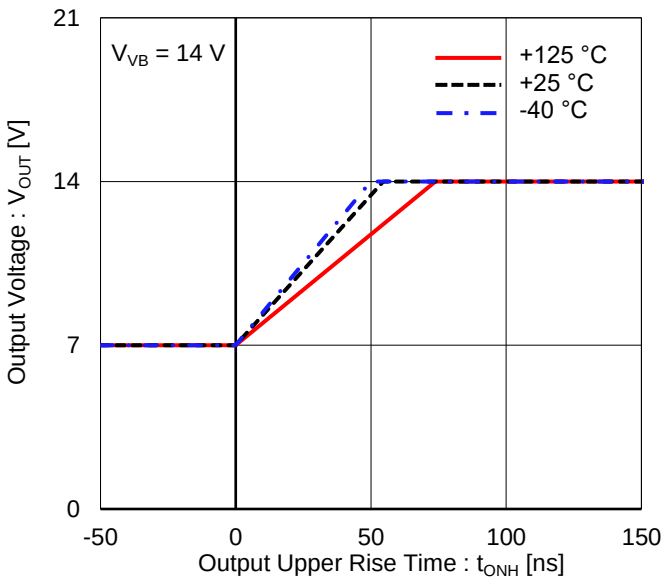


Figure 28. Output Voltage vs Output Upper Rise Time

Typical Performance Curve (reference data) - continued

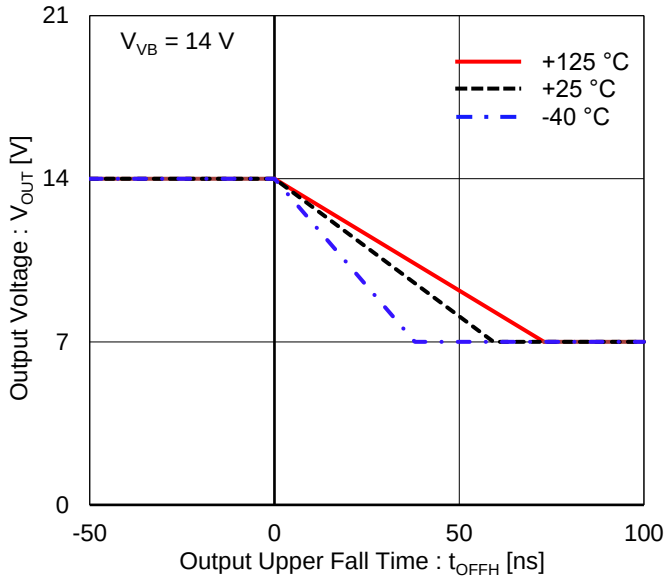


Figure 29. Output Voltage vs Output Upper Fall Time

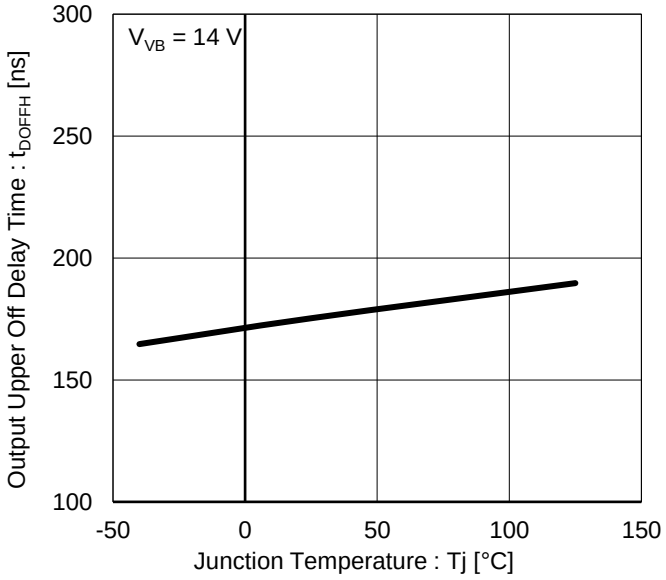


Figure 30. Output Upper Off Delay Time vs Junction Temperature

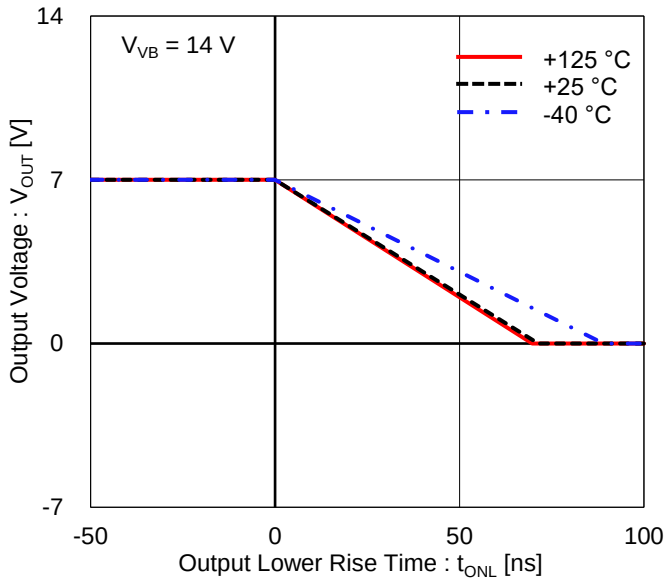


Figure 31. Output Voltage vs Output Lower Rise Time

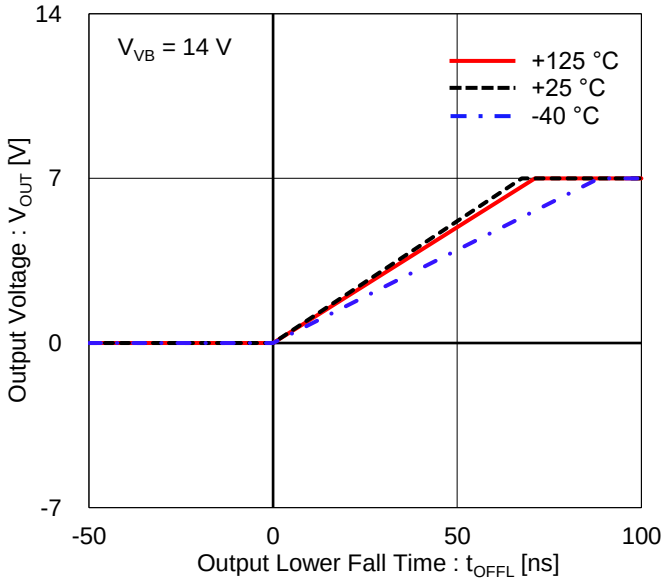


Figure 32. Output Voltage vs Output Lower Fall Time

Typical Performance Curve (reference data) - continued

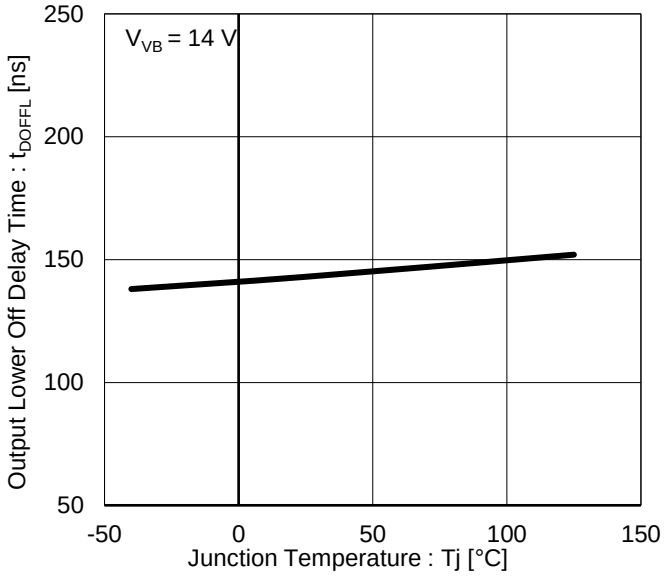


Figure 33. Output Lower Off Delay Time vs Junction Temperature

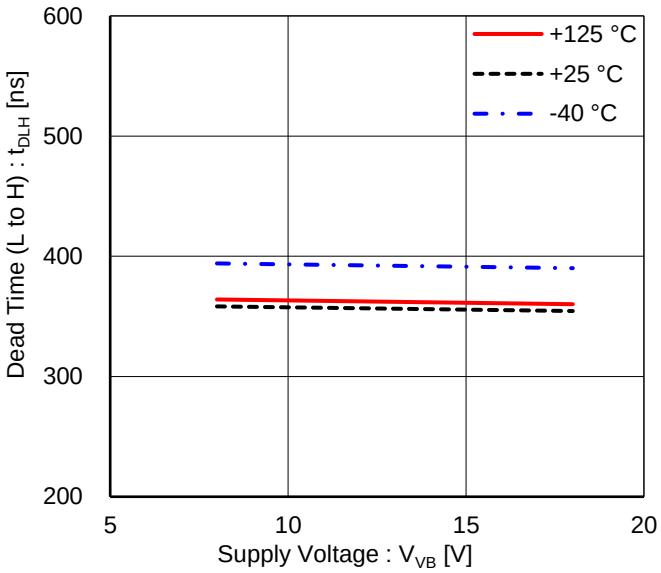


Figure 34. Dead Time (L to H) vs Supply Voltage

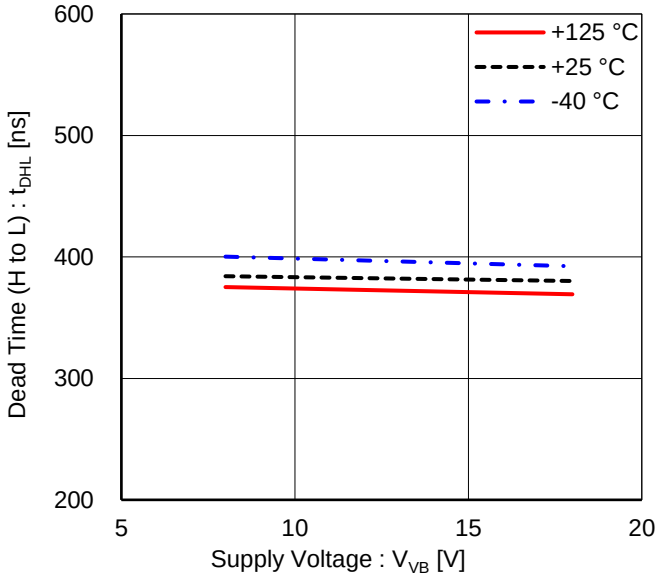


Figure 35. Dead Time (H to L) vs Supply Voltage

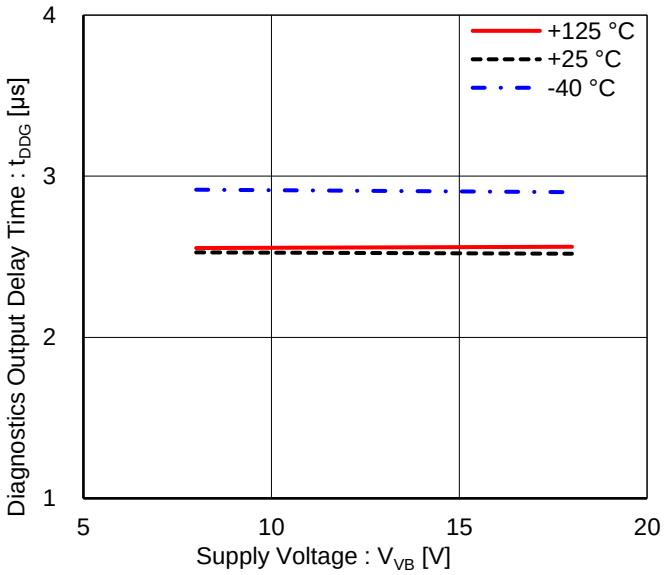


Figure 36. Diagnostics Output Delay Time vs Supply Voltage

Typical Performance Curve (reference data) - continued

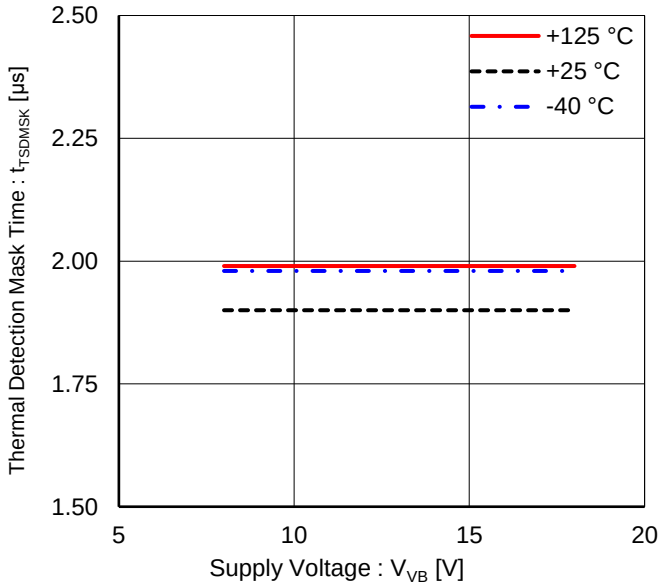


Figure 37. Thermal Detection Mask Time vs Supply Voltage

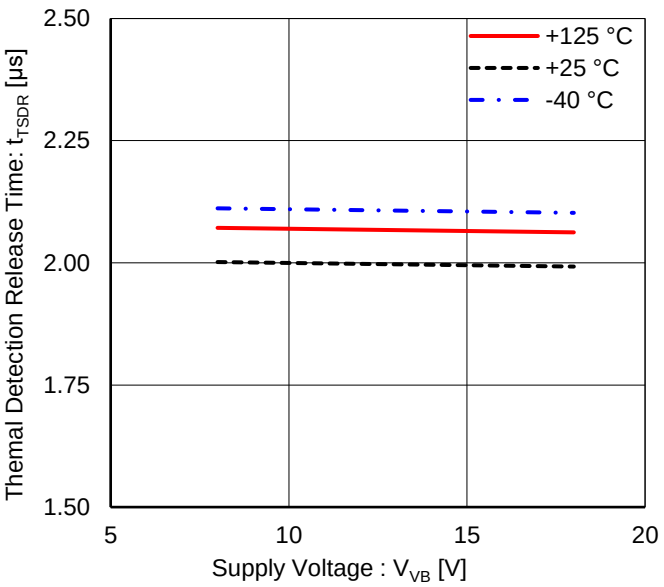


Figure 38. Thermal Detection Release Time vs Supply Voltage

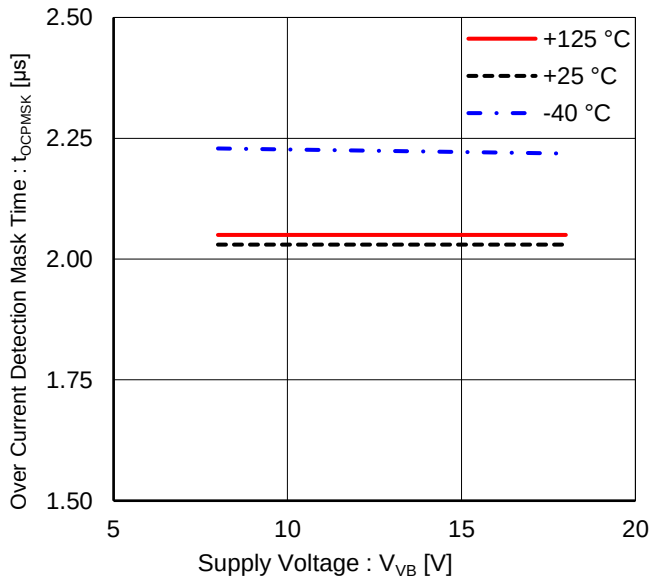


Figure 39. Over Current Detection Mask Time vs Supply Voltage

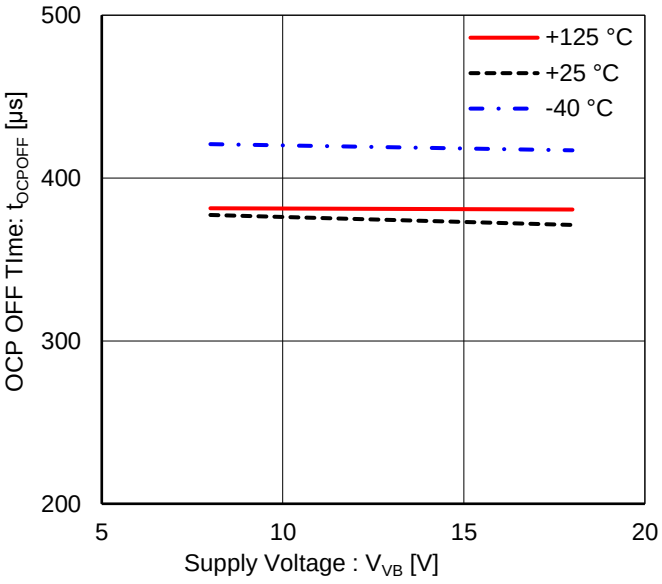


Figure 40. OCP Off Time vs Supply Voltage

Typical Performance Curve (reference data) - continued

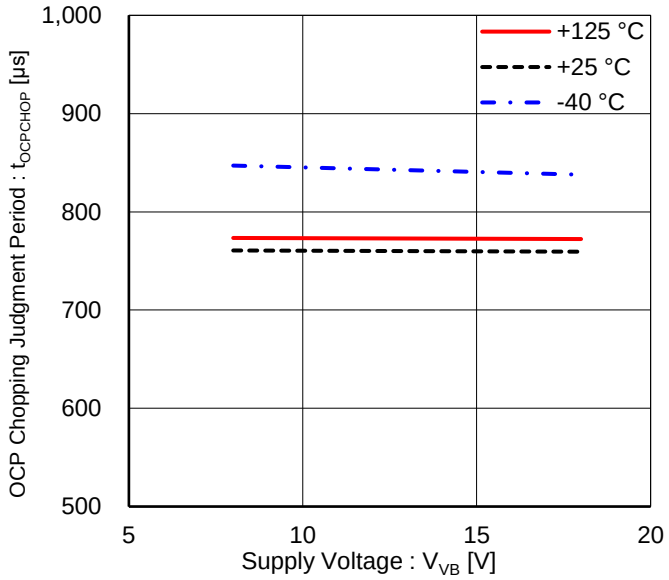


Figure 41. OCP Chopping Judgement Period vs Supply Voltage

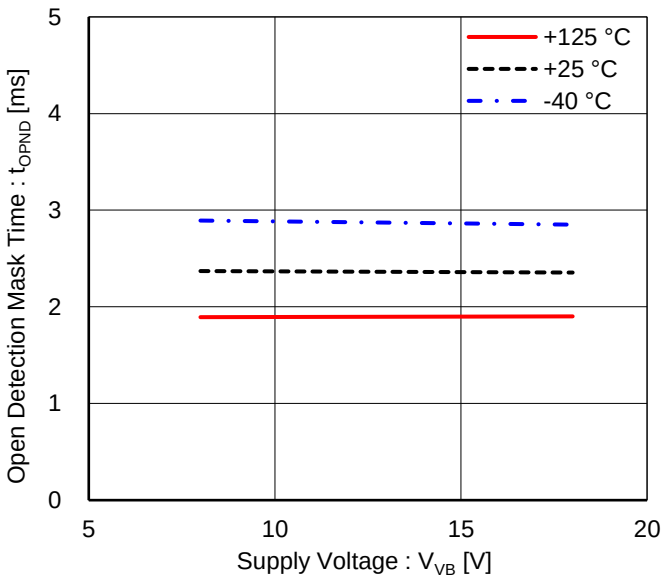


Figure 42. Open Detection Mask Time vs Supply Voltage

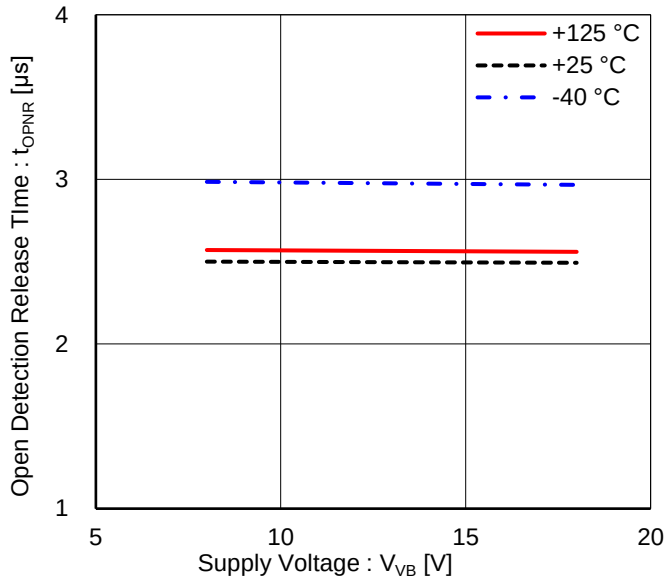


Figure 43. Open Detection Release Time vs Supply Voltage

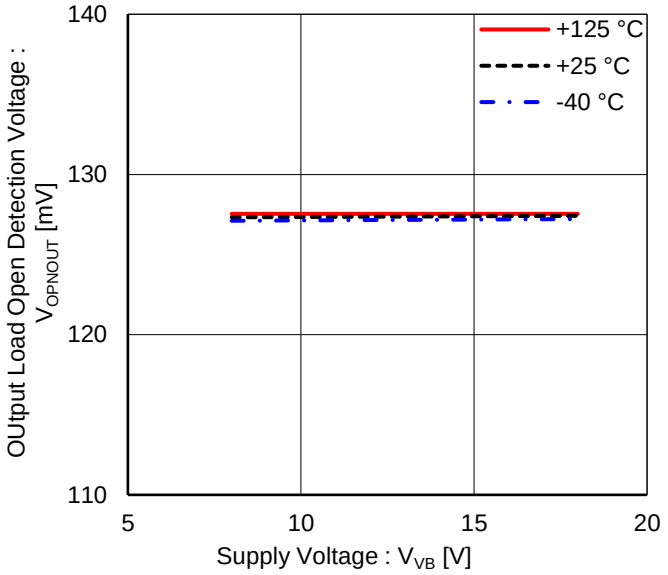


Figure 44. Output Load Open Detection Voltage vs Supply Voltage

Typical Performance Curve (reference data) - continued

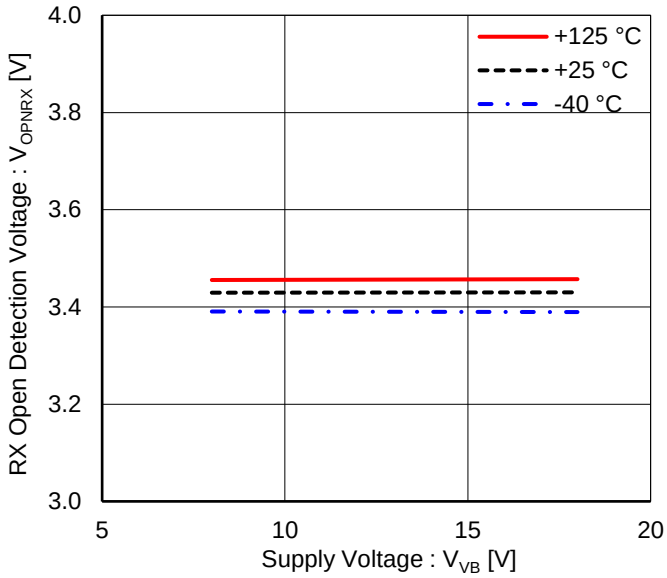


Figure 45. RX Open Detection Voltage vs Supply Voltage

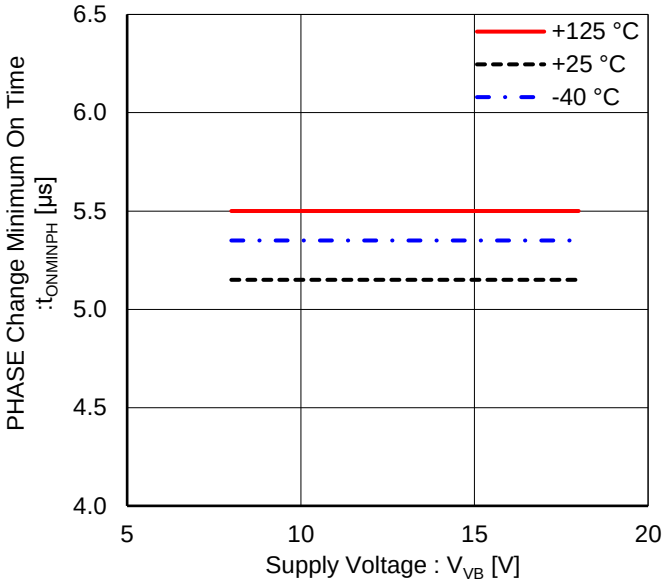


Figure 46. PHASE Change Minimum On Time vs Supply Voltage

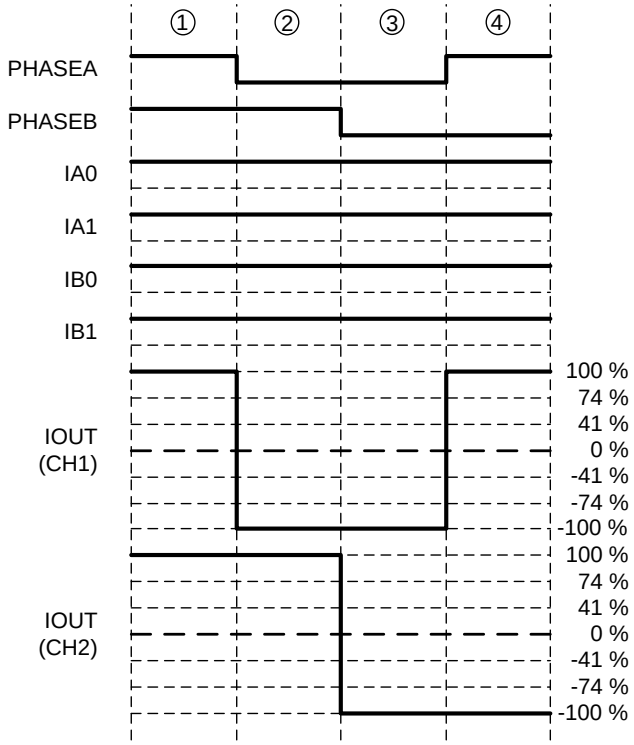
Timing Chart

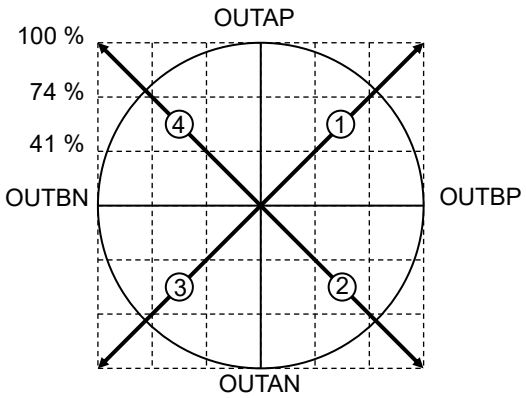
It is possible to drive stepping motor with FULL STEP, HALF STEP, and QUARTER STEP by inputting the following motor control signals using PARALLEL-IN drive mode.

Examples of control sequence and torque vector

1 FULL STEP

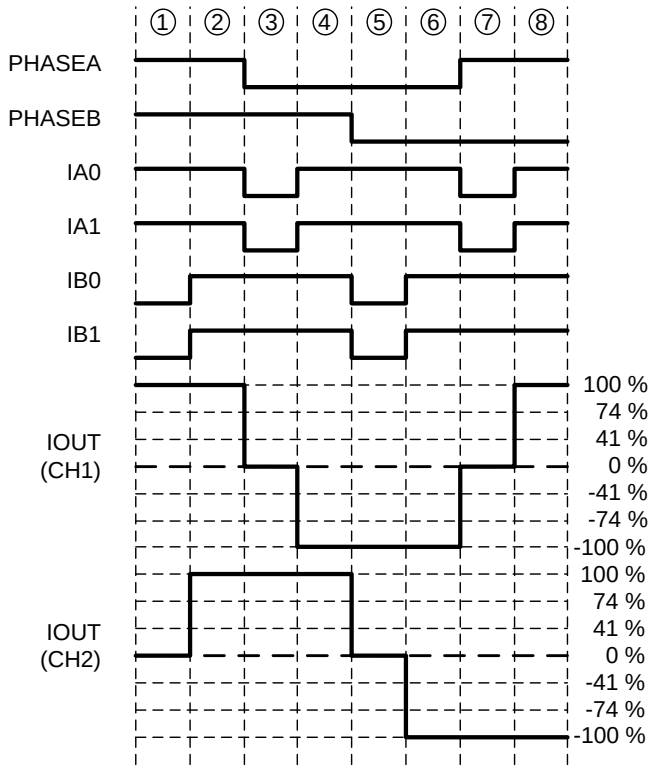
Controlled by 2 logic signals of PHASEA and PHASEB

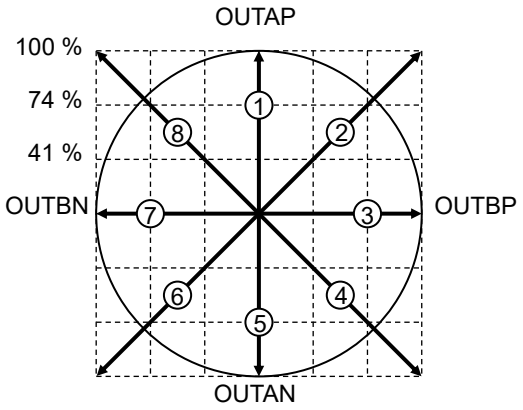




2 HALF STEP A

Controlled by 4 logic signals of PHASEA, PHASEB, IA0 (IA1), and IB0 (IB1)

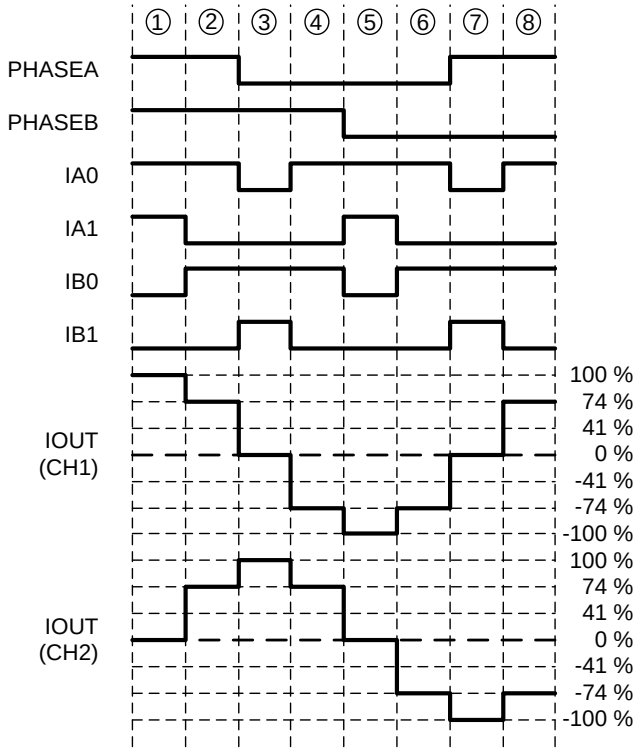


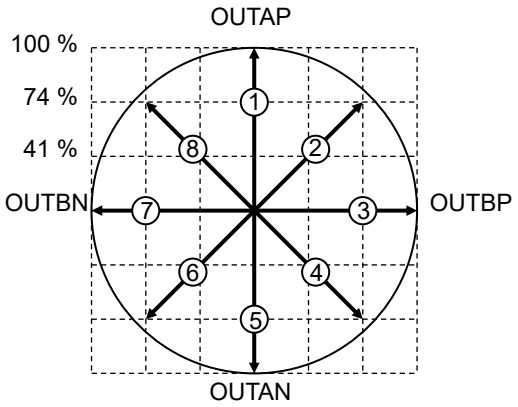


Timing Chart - continued

3 HALF STEP B

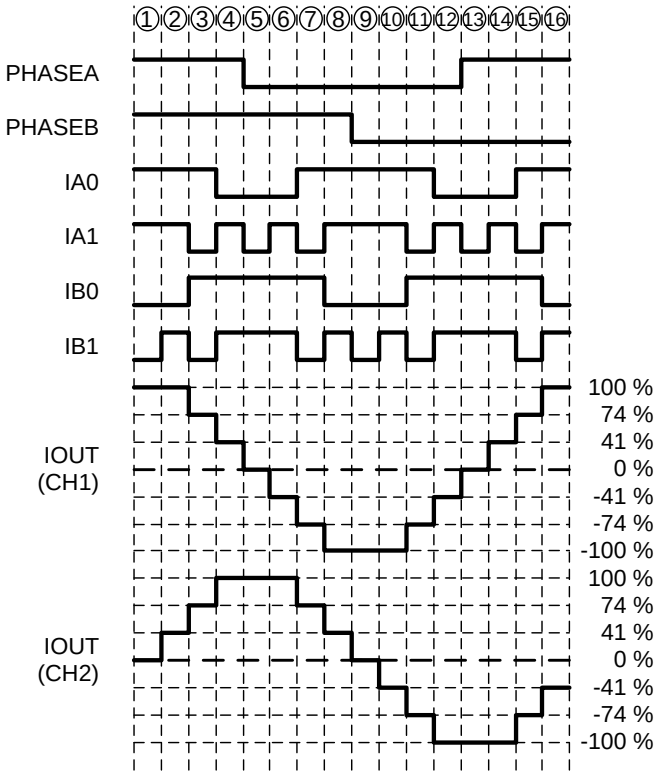
Controlled by 6 logic signals of PHASEA, PHASEB, IA0, IA1, IB0, and IB1

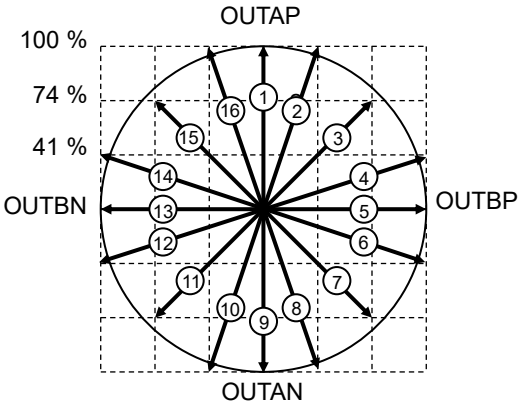




4 QUATER STEP

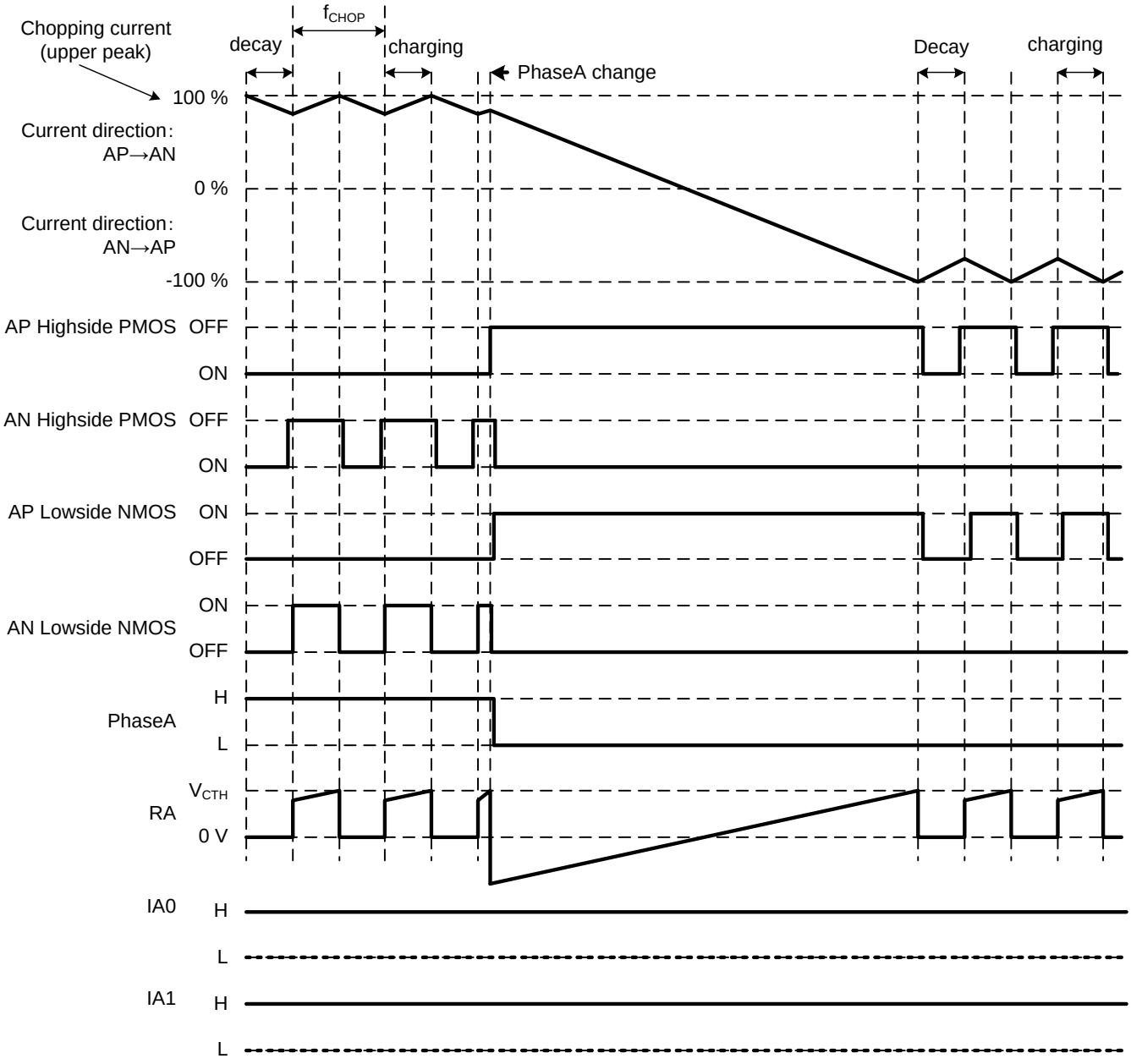
Controlled by 6 logic signals of PHASEA, PHASEB, IA0, IA1, IB0, and IB1



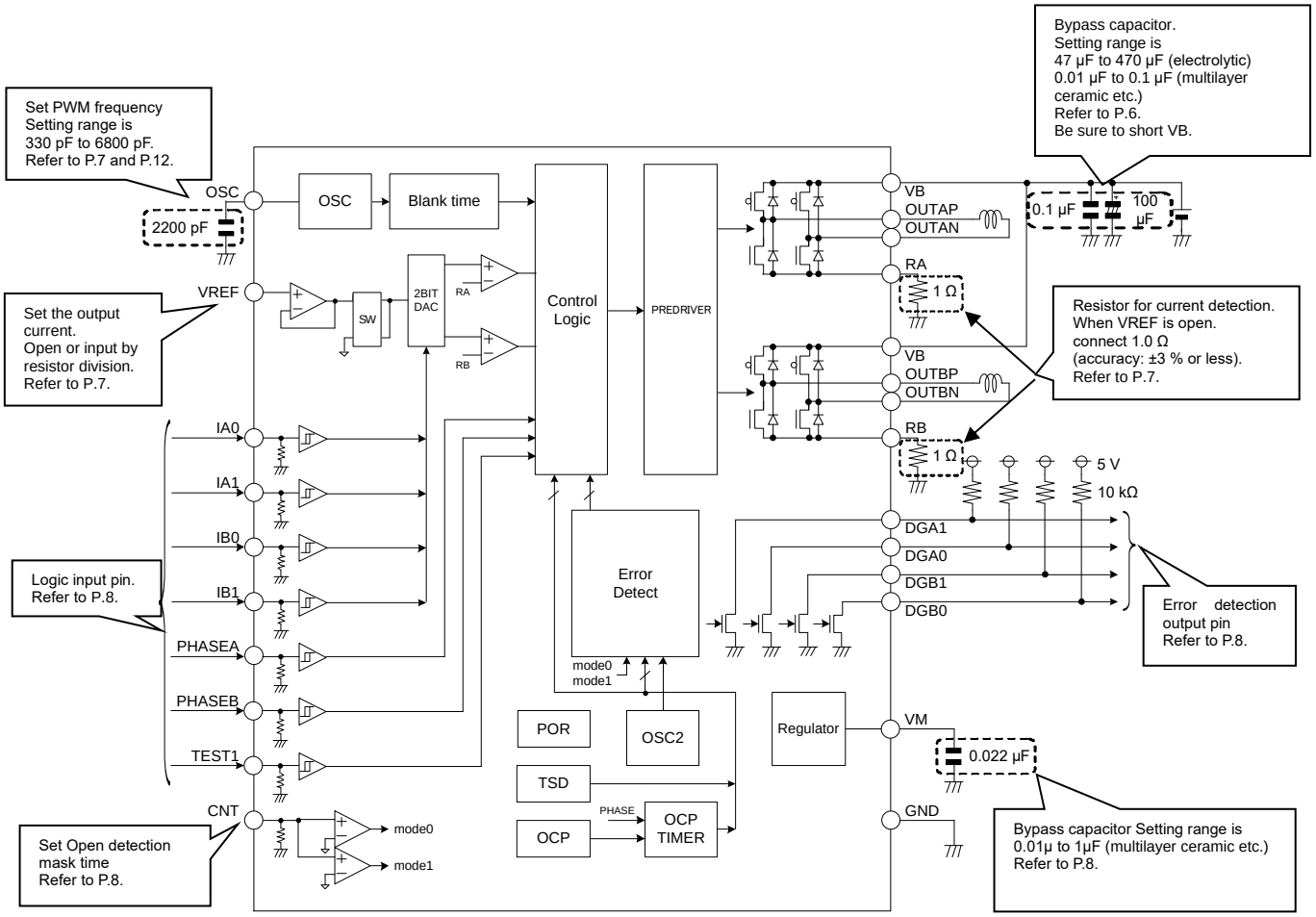


Timing Chart - continued

5 Normal Operation Timing Chart



Application Example



Power Dissipation

In consideration of the IC's power consumption (W), thermal resistance (θja), and ambient temperature (Ta), confirm that the IC's chip temperature Tj is not over 150 °C. When Tj = 150 °C is exceeded, the functions as a semiconductor do not operate and problems such as parasitism and leaks occur. Constant use under these circumstances leads to deterioration and eventually destruction of the IC. Tjmax = 150 °C must be strictly obeyed under all circumstances.

1 Thermal Calculation

The IC's consumed power can be estimated roughly with the power supply voltage (VB), circuit current (I_B), upper side output ON resistance (R_{ONH}), lower side ON resistance (R_{ONL}) and motor output current value (I_{OUT}).
The calculation method during FULL STEP drive, SLOW DECAY mode is shown here:

$$W_{VB} = VB \times I_B \quad [W]$$

Where:

W_{VB}	is the consumed power of the VB.
VB	is the power supply voltage.
I_B	is the circuit current.

$$W_{DMOS} = W_{ON} + W_{DECAY} \quad [W]$$

$$W_{ON} = (R_{ONH} + R_{ONL}) \times {I_{OUT}}^2 \times 2 \times on\_duty \quad [W]$$

$$W_{DECAY} = (2 \times R_{ONL}) \times {I_{OUT}}^2 \times 2 \times (1 - on\_duty) \quad [W]$$

Where:

W_{DMOS}	is the consumed power of the output DMOS.
W_{ON}	is the consumed power during output ON.
W_{DECAY}	is the consumed power during current decay.
R_{ONH}	is the upper P-channel DMOS ON-resistance.
R_{ONL}	is the lower N-channel DMOS ON-resistance.
I_{OUT}	is the motor output current value.
on_duty	PWM on duty= t_{ON}/t_{CHOP}

t_{ON} varies depending on the L and R values of the motor coil and the current set value. Confirm by actual measurement, or make an approximate calculation.
t_{CHOP} is the chopping period, which depends on the external capacitor. Refer to P.12

IC number	Upper Pch DMOS ON Resistance R_{ONH}[Ω] (Typ)	Lower Nch DMOS ON Resistance R_{ONL}[Ω] (Typ)
BD68960EKV-C	0.20	0.15

$$W\_total = W_{VB} + W_{DMOS} \quad [W]$$

$$Tj = Ta + \theta ja \times W\_total \quad [°C]$$

Where:

W_total	is the consumed total power of IC.
Tj	is the junction temperature.
Ta	is the ambient temperature.
θja	is the thermal resistance value.

However, the thermal resistance value θja [°C/W] differs greatly depending on circuit board conditions. The calculated values above are only theoretical. For actual thermal design, perform sufficient thermal evaluation for the application board used, and create the thermal design with enough margin not to exceed Tjmax = 150 °C. Although unnecessary with normal use, if the IC is used under especially strict heat conditions, consider externally attaching a Schottky diode between the motor output pin and GND to abate heat from the IC.

Power Dissipation - continued

2 Temperature Monitoring

In respect of BD68960EKV-C, there is a way to directly measure the approximate chip temperature by using the TEST1 pin of the low level with a protection diode for prevention from electrostatic discharge. However, temperature monitor way is used only for evaluation and experimenting, and must not be used in actual usage conditions.

(1) Measure the pin voltage when a current of I_{DIODE} = 50 µA flows from the low level Input pin to the GND, without supplying VB to the IC. This measurement is for measuring the V_F voltage of the internal diode.

(2) Measure the temperature characteristics of this pin voltage. (Vf has a linear negative temperature factor against the temperature.) With the results of these temperature characteristics, chip temperature can be calibrated from the TEST1 pin voltage.

(3) Supply V_{VB}, confirm the TEST1 pin voltage while running the motor, and the chip temperature can be approximated from the results of (2).

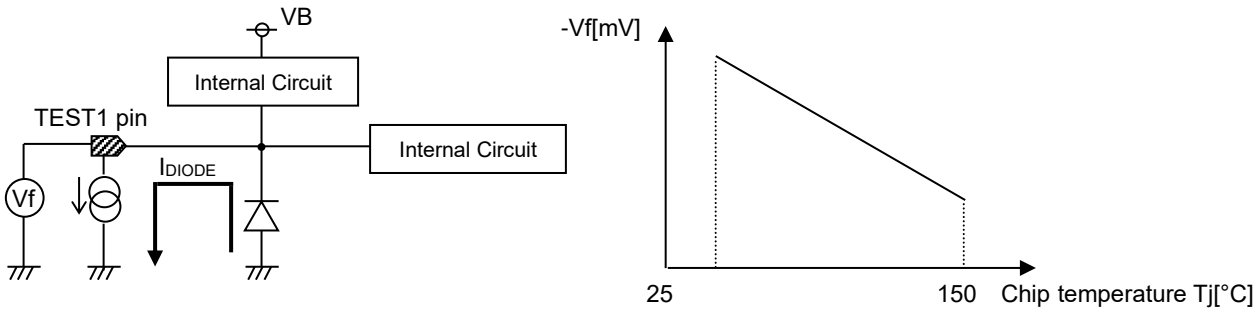
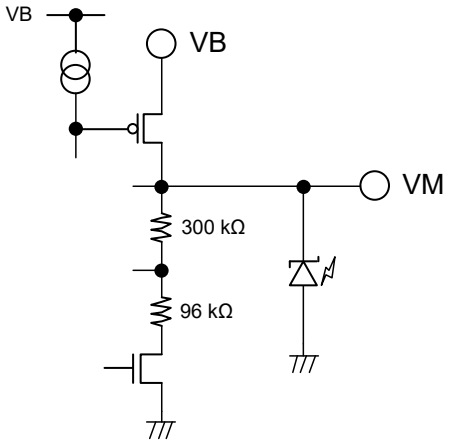
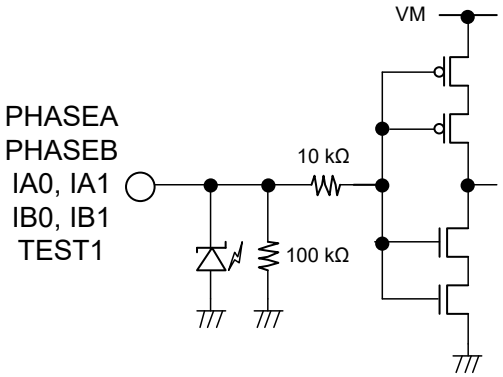
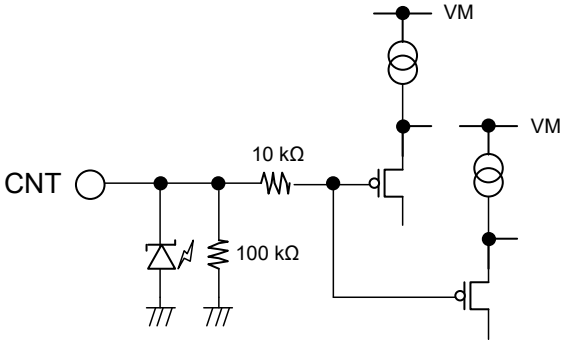


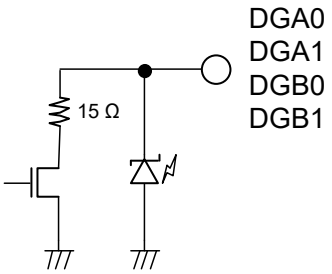
Figure 47. Model diagram for measuring chip temperature

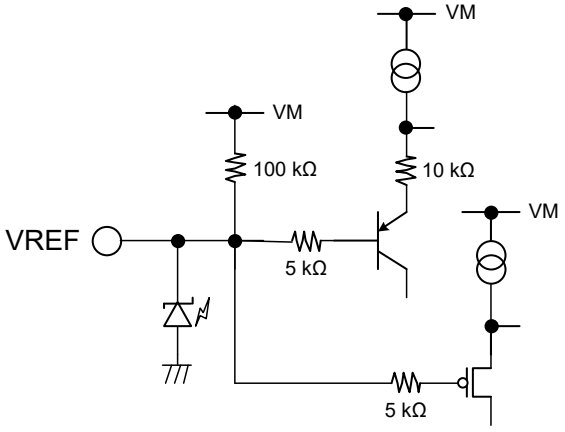
I/O Equivalence Circuit

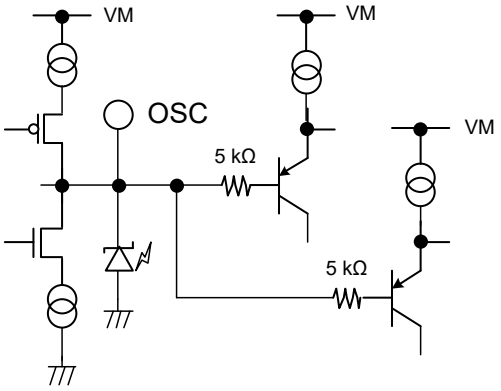


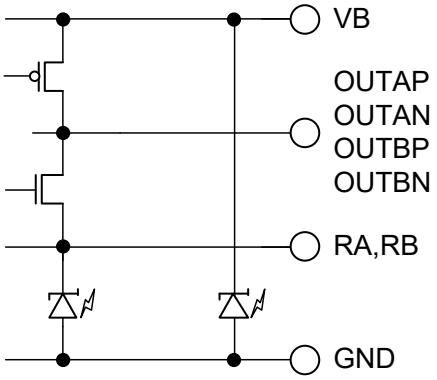


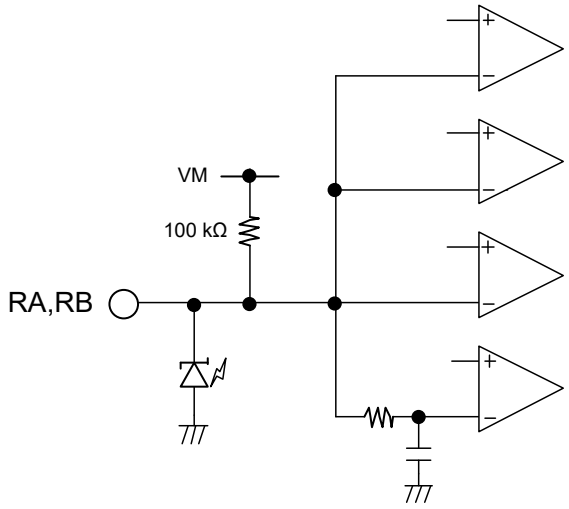












Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

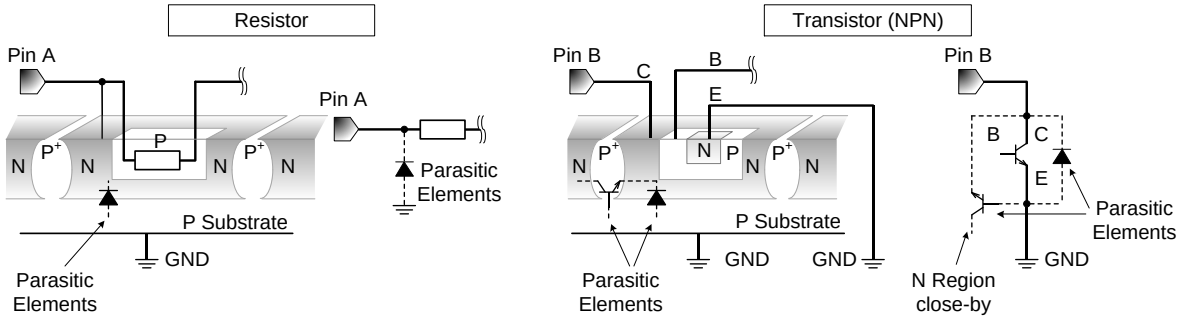


Figure 48. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

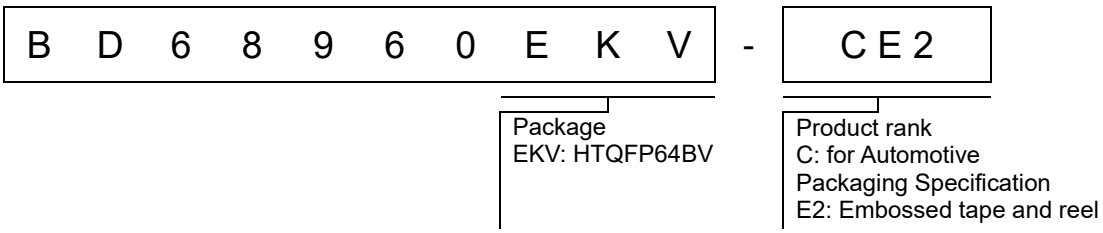
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

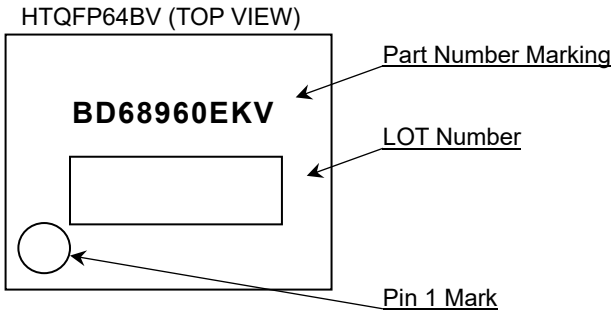
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

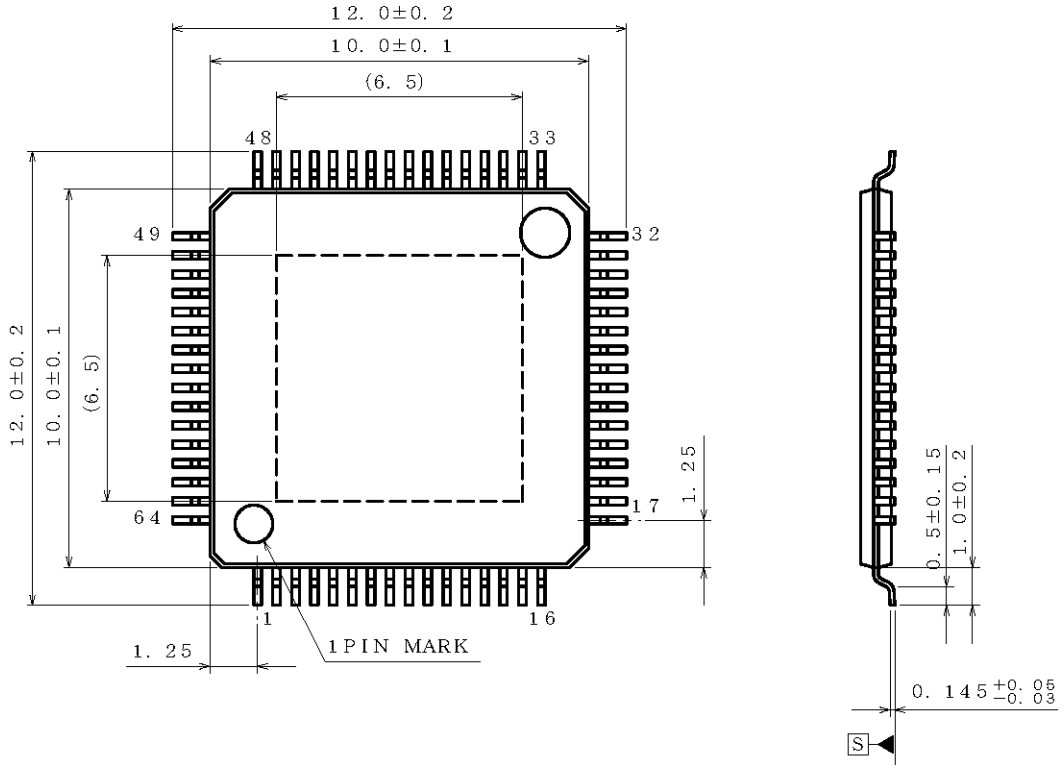


Marking Diagram



Physical Dimension and Packing Information

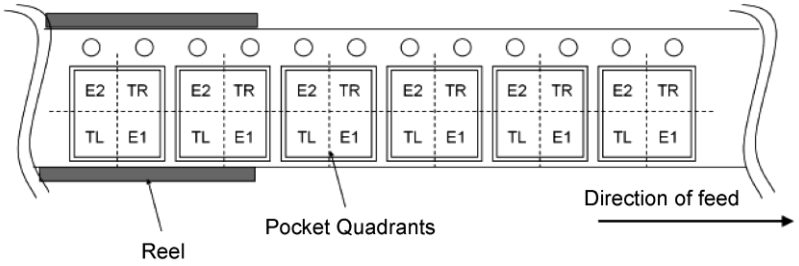
Package Name	HTQFP64BV



(UNIT:mm)
PKG:HTQFP64BV
Drawing No. EX282-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
10.Dec.2019	001	New Release
28.Feb.2022	002	P.14 Recommended Operating Condition - Supply Voltage - Typ value P.35 Operational Notes – 3.Ground Voltage

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

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