

4 A/6 A 1ch High-speed Gate Driver with Built-in LDO for GaN HEMT

BD3GD02NVX-LB BD3GD03NVX-LB

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

The BD3GD02NVX-LB and BD3GD03NVX-LB are 1-channel gate drivers for driving GaN HEMTs at high speed. The high-speed gate driver circuit for GaN HEMTs and the LDO that generates the gate drive voltage are enclosed in a 6-pin SON compact package, which is especially optimized for driving E-mode GaN HEMT devices.

Since the input is compatible with the gate drive voltage for Si FETs, it can be connected to the gate drive line for Si FETs in an existing system to drive GaN HEMTs without any system modifications.

The output pins are divided into source and sink drive pins, and the slew rates of the source and sink sides can be adjusted separately with external resistors.

As protection functions, a low input malfunction prevention circuit (UVLO) between VDD and GND and a low output voltage protection circuit (UVP) between VREG and GND are provided.

Key Specifications

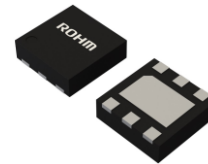
- Power Supply Voltage Range (VDD Pin)
 - BD3GD02NVX-LB: 4.5 V to 18 V
 - BD3GD03NVX-LB: 5.25 V to 18 V
- Input Voltage Range (IN+ Pin, EN Pin): 0 V to 18 V
- LDO Output Voltage (Gate Drive Voltage)
 - BD3GD02NVX-LB: 5.0 V (Typ)
 - BD3GD03NVX-LB: 5.75 V (Typ)
- Output Current I_{OMAXH} / I_{OMAXL} : 4 A / 6 A (Typ)
- Turn-on Propagation Delay Time: 14 ns (Typ)
- Turn-off Propagation Delay Time: 14 ns (Typ)
- Input High Pulse Width: 10 ns (Min)
- Operating Temperature Range: -40 °C to +125 °C

Package

SSON06RX2020

W (Typ) x D (Typ) x H (Max)

2.0 mm x 2.0 mm x 0.6 mm



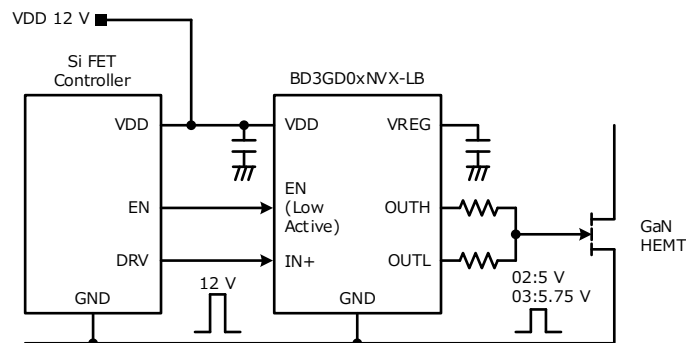
Features

- Built-in LDO for Drive Voltage Control.
- Wide Operating Input Voltage Range.
- Supports Non-invert Operating Input and Invert Operating Input.
- Low Propagation Delay.
- Built-in VDD UVLO Protection.
- Built-in VREG UVP Protection.

Applications

- Industrial Equipment.
- GaN Applications.
- PFC or LLC Topology Power Supply.
- Power Supplies with Bridge Topology Configuration.

Typical Application Circuit



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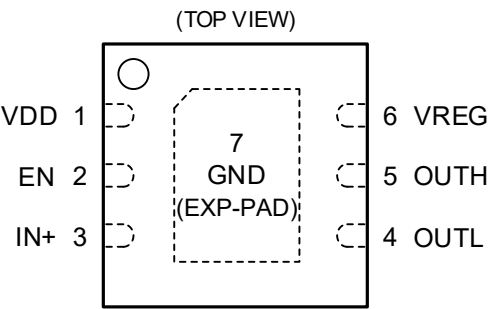
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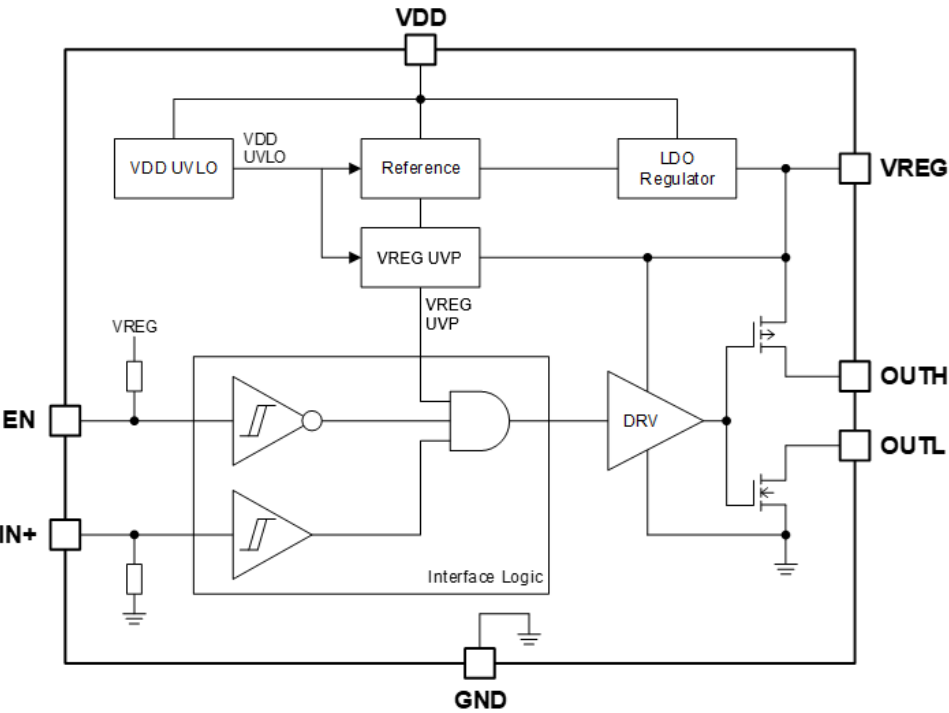
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	VDD	Power supply pin
2	EN	Enable pin (Low active)
3	IN+	Non-inverting gate drive input pin
4	OUTL	Sink side output pin for gate driving
5	OUTH	Source side output pin for gate driving
6	VREG	Capacitor connection pin for gate drive voltage generation circuit
7	GND (EXP-PAD)	GND pin This pin also serves as a backside heat dissipation pad. Excellent heat dissipation characteristics can be obtained by connecting to the internal PCB ground plane using vias.

Block Diagram



Description of Blocks

1 Outline

This product, which incorporates a gate driver circuit, a LDO regulator for generating gate drive voltage, and a protection function, has the function of converting the input gate driver drive voltage from Si-FETs to the gate drive voltage of GaN HEMTs, so that GaN HEMTs can be used in existing applications with gate drive outputs for Si-FETs. Therefore, GaN HEMTs can be used without system modifications by connecting to existing applications with gate drive outputs for Si-FETs.

In addition, a UVLO (Under Voltage Lock Out) function to monitor VDD and a UVP (Under Voltage Protection) function to monitor the LDO regulator's output are integrated to protect the product from damage.

2 Description of Each Block

2.1 Gate Driver (DRV) Block

This is a gate driver for the GaN HEMT and drives the gate of the GaN HEMT device to the High level of VREG output and Low level of GND. Until VREG output is determined to be normal (no UVP protection detected on VREG), the driver remains in off state (OUTH = Open, OUTL = Low).

2.2 LDO Regulator Block

The voltage used to drive the GaN HEMT is regulated from VDD supply, ensuring the specified gate drive voltage over a wide VDD input voltage range.

2.2 μF (Typ) ceramic capacitor C_{VREG} is required between the VREG and GND pins.

This LDO provides only the gate charge current to the GaN HEMT. It cannot be used for external power supply.

2.3 Interface Block

The input interface circuit allows direct connection and use of voltage signals up to 18 V, such as the output of a general MCU or ACDC controller, as input signals for the IN+ and EN pins.

Table 1 shows the driver operation with the combination of the EN and IN+ pins.

2.4 VREG UVP Block

A low output voltage protection circuit that monitors the built-in LDO output and turns off the driver function (OUTH = Open, OUTL = Low) when the VREG pin becomes 80 % (Typ) or lower than the output voltage. The threshold voltage has a hysteresis of 5 % (Typ) with respect to the output voltage.

The delay time is 10 μs (Typ) for detection.

2.5 VDD UVLO Block

This is a low input voltage malfunction prevention circuit that monitors VDD voltage and turns off the driver function when VDD falls below 3.55 V (Typ). The threshold voltage has a hysteresis of 0.25 V (Typ).

2.6 Reference Block

Generates a reference voltage from the VDD input voltage to generate the VREG voltage and the protection circuit detection voltage.

Table 1. Function Table of Driver.

VDD	VREG	IN+	EN	OUTH	OUTL
$< V_{\text{UVLO}}$	OFF	X	X	Open	Low
$\geq V_{\text{UVLO}}$	$< V_{\text{UVP}}$	X	X	Open	Low
$\geq V_{\text{UVLO}}$	$\geq V_{\text{UVP}}$	L	L	Open	Low
$\geq V_{\text{UVLO}}$	$\geq V_{\text{UVP}}$	H	L	High	Open
$\geq V_{\text{UVLO}}$	$\geq V_{\text{UVP}}$	L	H	Open	Low
$\geq V_{\text{UVLO}}$	$\geq V_{\text{UVP}}$	H	H	Open	Low

(Note) X: Don't care.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Maximum Input Voltage 1	V _{MAX1}	-0.3 to +20	V	VDD pin voltage
Maximum Input Voltage 2	V _{MAX2}	-0.6 to +20	V	IN+ pin voltage
Maximum Input Voltage 3	V _{MAX3}	-0.6 to +20	V	EN pin voltage
Maximum Input Voltage 4	V _{MAX4}	-0.3 to +7.0	V	VREG pin voltage
Maximum Junction Temperature	T _{jmax}	150	°C	
Storage Temperature Range	T _{stg}	-55 to +150	°C	

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
SSON06RX2020				
Junction to Ambient	θ _{JA}	284.5	83.2	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ _{JT}	35.0	22.0	°C/W

(Note 2) Based on JESD51-2A (Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range	V _{DD}	4.50	12.00	18.00	V	BD3GD02NVX-LB VDD pin voltage
		5.25	12.00	18.00	V	BD3GD03NVX-LB VDD pin voltage
Input Voltage Range 1	V _{IN+}	0	-	18	V	IN+ pin voltage
Input Voltage Range 2	V _{EN}	0	-	18	V	EN pin voltage
Input High Pulse Width	t _{IN_MIN}	10	-	-	ns	
VREG Pin Output Capacitor Range	C _{VREG}	0.47	2.20	10.00	μF	Ceramic capacitor is recommended ^(Note 1)
Operating Temperature	T _{opr}	-40	-	+125	°C	Ambient temperature

(Note 1) The capacitance of the capacitor should be set so that it does not fall below the minimum value in consideration of temperature characteristics and DC bias characteristics.

Electrical Characteristics

(Unless otherwise specified V_{DD} = 12 V, T_j = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
VDD Current Consumption 1	I _{VDD1}	-	50	90	μA	V _{IN+} = V _{DD} , V _{EN} = 0 V VDD = 3 V
VDD Current Consumption 2	I _{VDD2}	-	50	90	μA	V _{IN+} = 0 V, V _{EN} = V _{DD} VDD = 3 V
VDD Pin						
VDD UVLO Release Voltage	V _{UVLO1}	3.55	3.80	4.15	V	VDD pin voltage sweep up
VDD UVLO Detection Voltage	V _{UVLO2}	3.30	3.55	3.90	V	VDD pin voltage sweep down
VDD UVLO Hysteresis Voltage	V _{UVLO3}	-	0.25	-	V	V _{UVLO3} = V _{UVLO1} - V _{UVLO2}
VREG Pin						
LDO Voltage (Gate Drive Voltage)	V _{VREG}	4.85	5.00	5.15	V	BD3GD02NVX-LB, at no load
		5.58	5.75	5.92	V	BD3GD03NVX-LB, at no load
VREG UVP Release Voltage	V _{UVP1}	80	85	90	%	Percentage of V _{VREG} voltage
VREG UVP Detection Voltage	V _{UVP2}	75	80	85	%	Percentage of V _{VREG} voltage
VREG UVP Hysteresis Voltage	V _{UVP3}	-	5	-	%	V _{UVP3} = V _{UVP1} - V _{UVP2}
IN+ Pin, EN Pin						
Input Threshold Voltage 1	V _{INPOS}	1.85	2.05	2.25	V	Input voltage Sweep up
Input Threshold Voltage 2	V _{INNEG}	0.90	1.10	1.30	V	Input voltage Sweep down
Input Hysteresis Voltage	V _{INHYS}	-	0.95	-	V	V _{INHYS} = V _{INPOS} - V _{INNEG}
Input Leakage Current	I _{INLEAK}	50	150	250	μA	V _{IN+} = V _{EN} = 5 V
OUTH Pin, OUTL Pin						
OUTH Pull Up Resistance	R _{OUTH}	-	0.6	1.0	Ω	I _{OUTH} = -50 mA
OUTL Pull Down Resistance	R _{OUTL}	-	0.20	0.50	Ω	I _{OUTL} = 50 mA
Startup Time						
VREG Startup Time	t _{VREG}	80	160	340	μs	C _{VREG} = 2.2 μF (nominal value)

Electrical Characteristics – continued
(Unless otherwise specified $V_{DD} = 12\text{ V}$, $T_j = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Switching Specifications						
Output Source Side Maximum Current	I_{OMAXH}	-	4.0	-	A	(Note 1)
Output Sink Side Maximum Current	I_{OMAXL}	-	6.0	-	A	(Note 1)
Turn-on Propagation Delay Time	t_{DON}	-	14	25	ns	$C_{LOAD} = 1\text{ nF}$ $IN = 0\text{ V} \rightarrow 5\text{ V}$ (Note 2)
Turn-off Propagation Delay Time	t_{DOFF}	-	14	25	ns	$C_{LOAD} = 1\text{ nF}$ $IN = 5\text{ V} \rightarrow 0\text{ V}$ (Note 2)
Rise Time	t_{RISE}	-	3.5	-	ns	$C_{LOAD} = 1\text{ nF}$ (Note 2)
Fall Time	t_{FALL}	-	3.5	-	ns	$C_{LOAD} = 1\text{ nF}$ (Note 2)

(Note 1) No shipping inspection.
(Note 2) Refer to 'Switching Parameter Measurement Information'.

Switching Parameter Measurement Information

Figure 1 shows a circuit for measuring switching parameters.
Figure 2 shows the measurement information for the switching parameters.

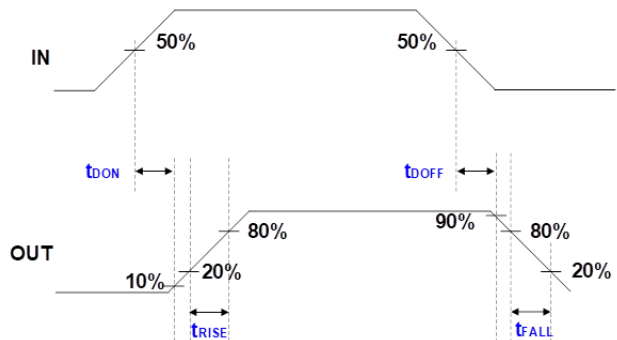
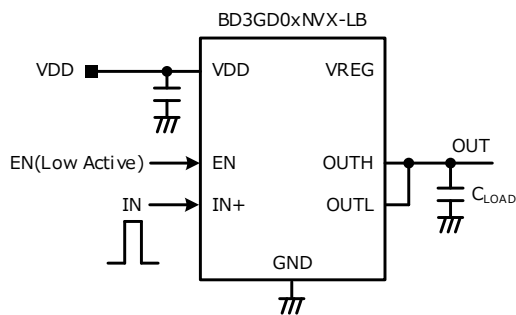


Figure 1. Switching Parameter Measurement Circuit Diagram Figure 2. Switching Parameter Measurement Information

- 1 Turn-on Propagation Delay Time: t_{DON}**
The turn-on propagation delay time is the time from the rising edge of the IN voltage (at 50 % of the IN's high voltage level) until the OUT begins to turn-on (when OUT rises to 10 % of V_{OUTH}).
- 2 Output Rise Time: t_{RISE}**
The output rise time is the time it takes for OUT to rise from 20 % to 80 % of V_{OUTH} .
- 3 Turn-off Propagation Delay Time: t_{DOFF}**
The turn-off propagation delay time is the time from the falling edge of the IN voltage (at 50 % of the IN's high voltage level) until the OUT begins to turn-off (when OUT falls to 90 % of V_{OUTH}).
- 4 Output Fall Time: t_{FALL}**
The output fall time is the time it takes for OUT to fall from 80 % to 20 % of V_{OUTH} .

Typical Performance Curves

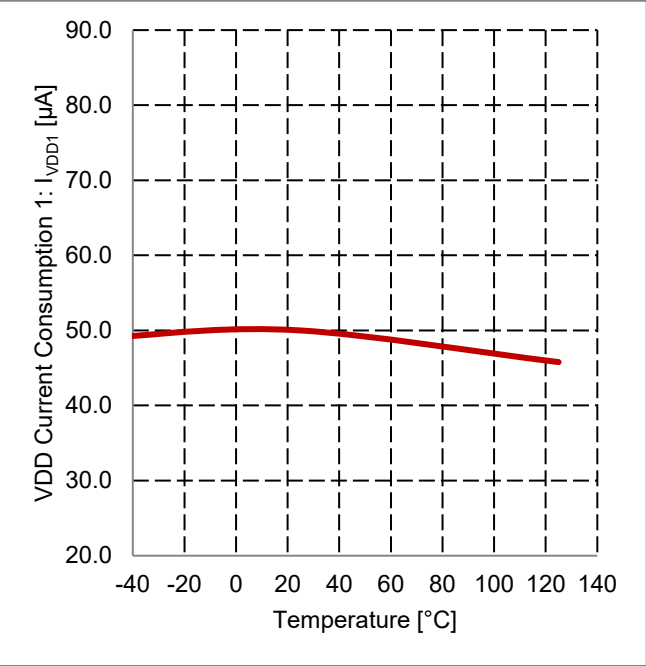


Figure 3. VDD Current Consumption 1 vs Temperature

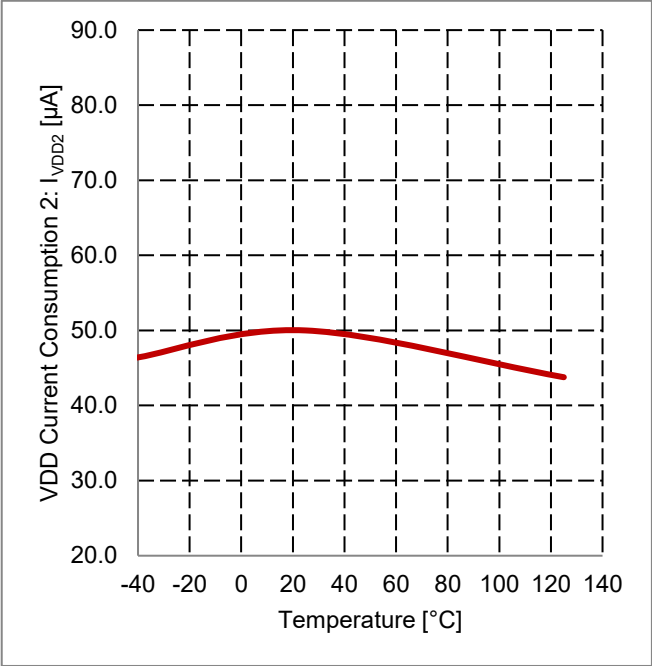


Figure 4. VDD Current Consumption 2 vs Temperature

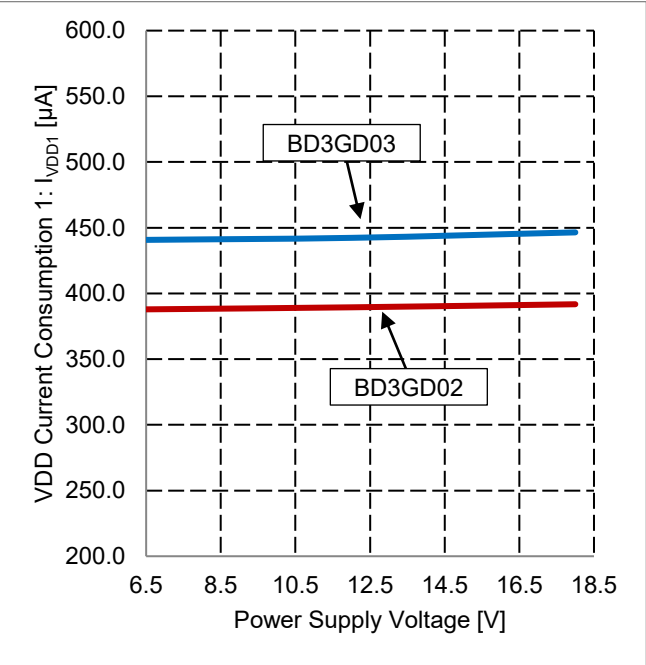


Figure 5. VDD Current Consumption 1 vs Power Supply Voltage

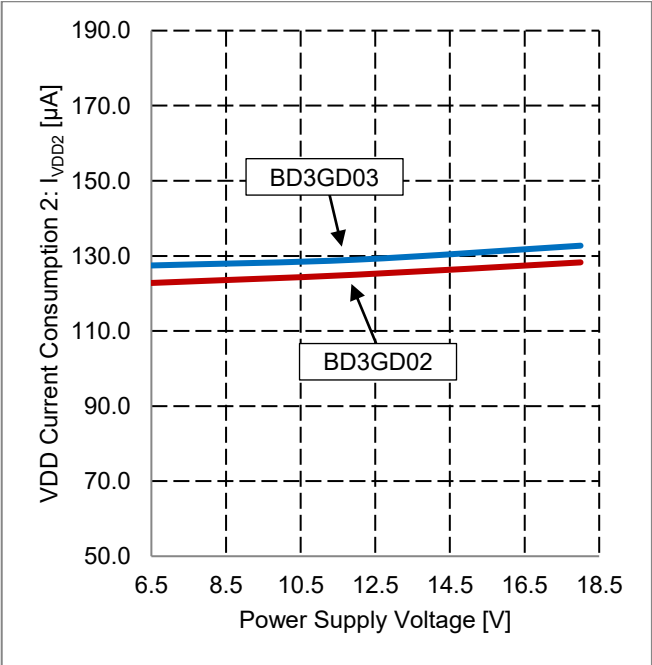


Figure 6. VDD Current Consumption 2 vs Power Supply Voltage

Typical Performance Curves – continued

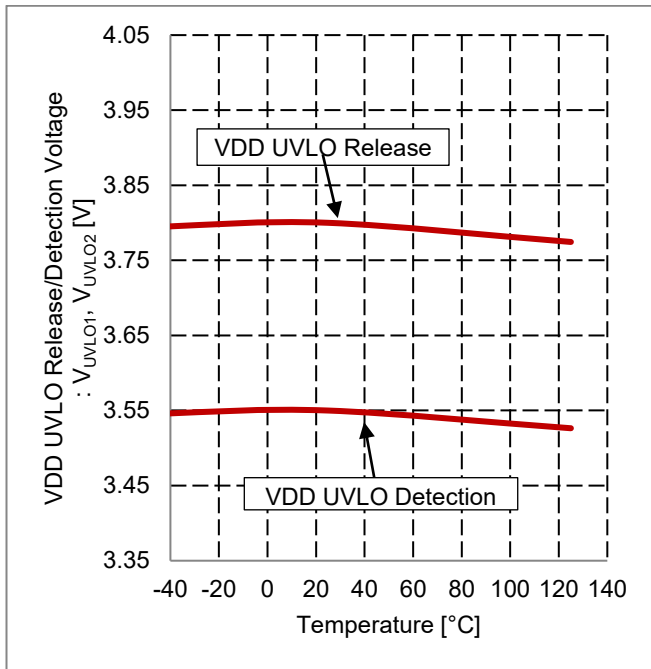


Figure 7. VDD UVLO Release/Detection Voltage vs Temperature

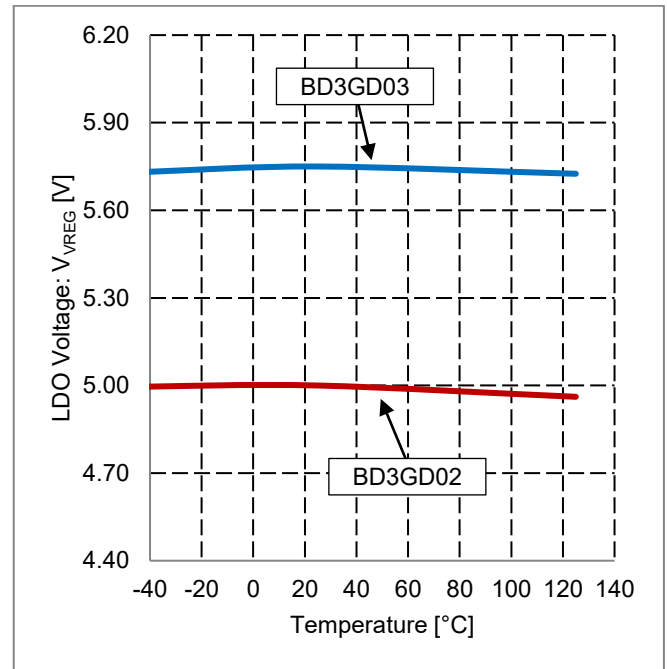


Figure 8. LDO Voltage vs Temperature

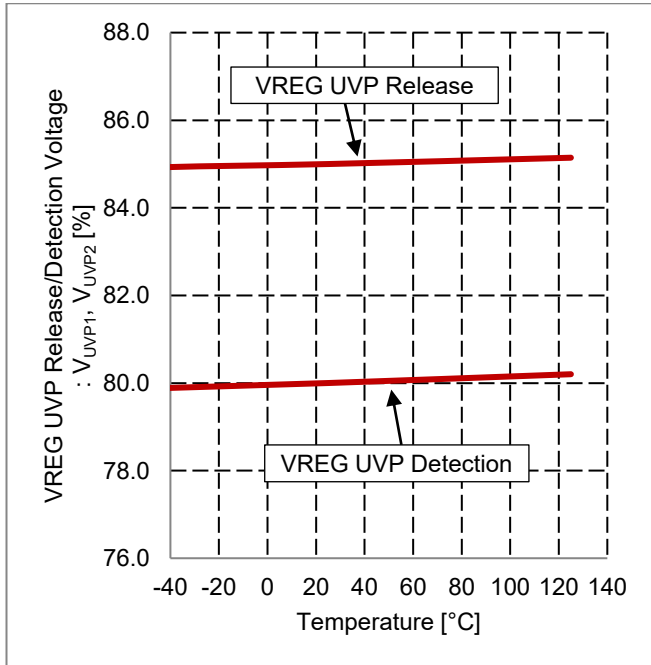


Figure 9. VREG UVP Release/Detection Voltage vs Temperature

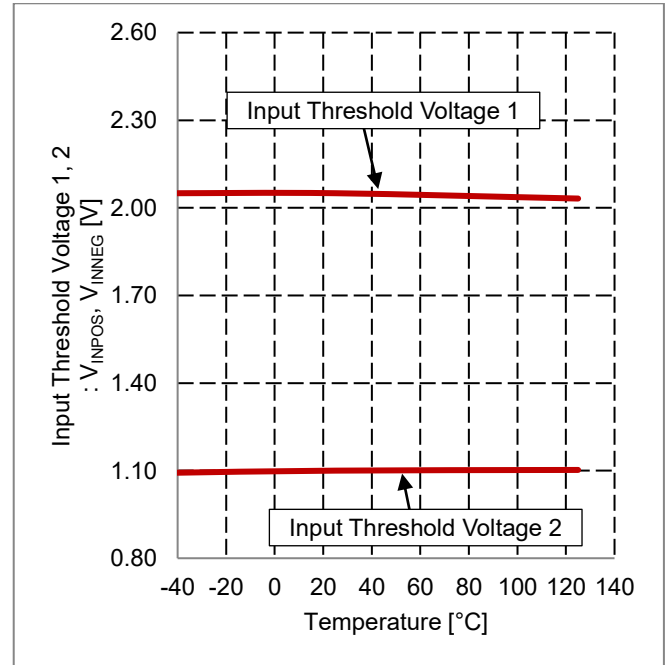


Figure 10. Input Threshold Voltage 1, 2 vs Temperature

Typical Performance Curves – continued

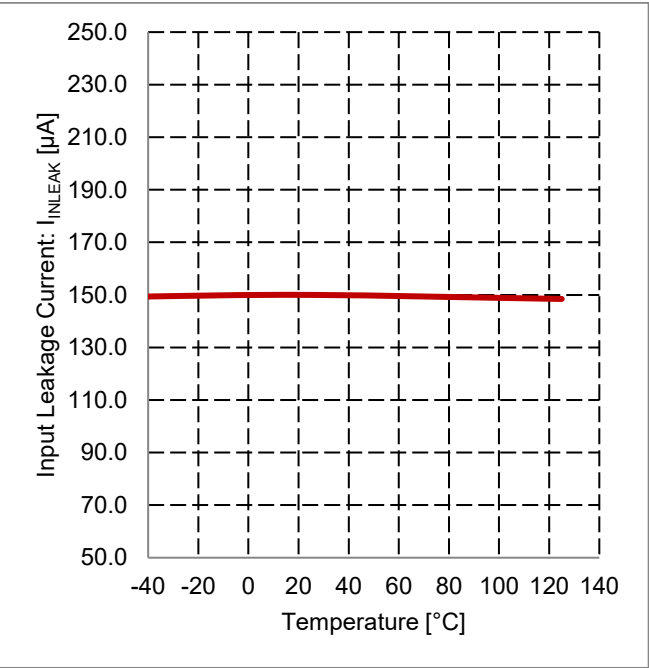


Figure 11. Input Leakage Current vs Temperature

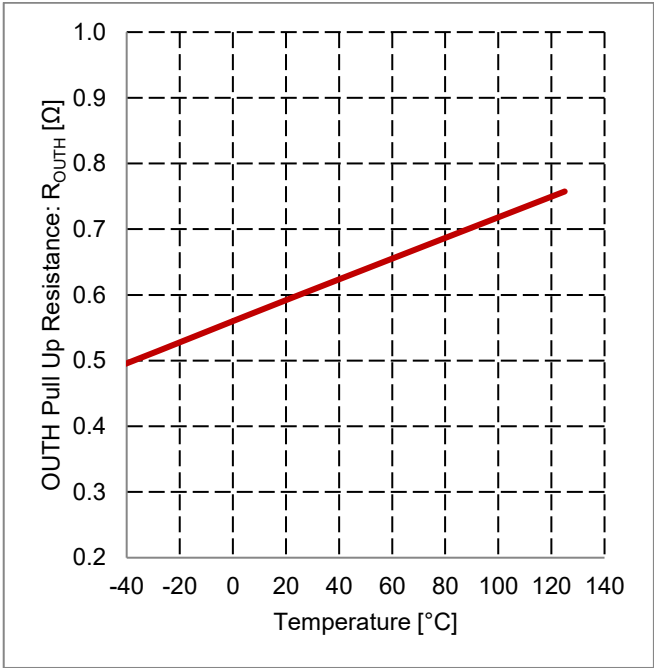


Figure 12. OUTH Pull Up Resistance vs Temperature

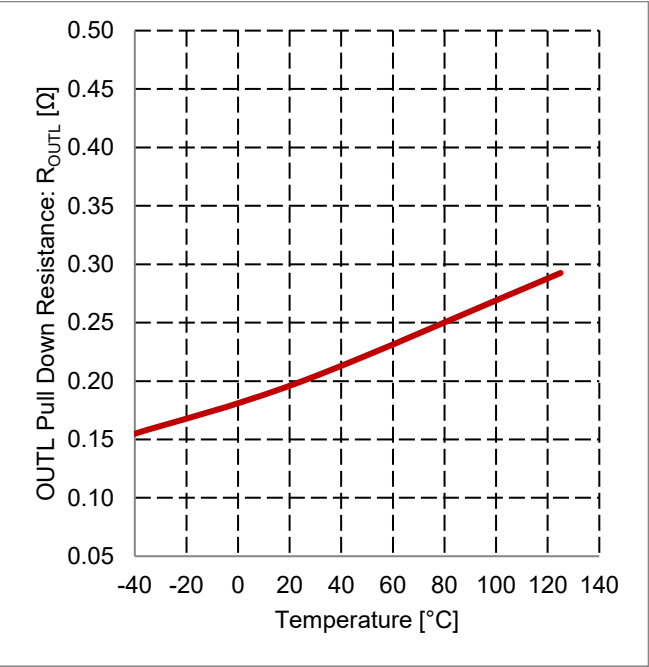


Figure 13. OUTL Pull Down Resistance vs Temperature

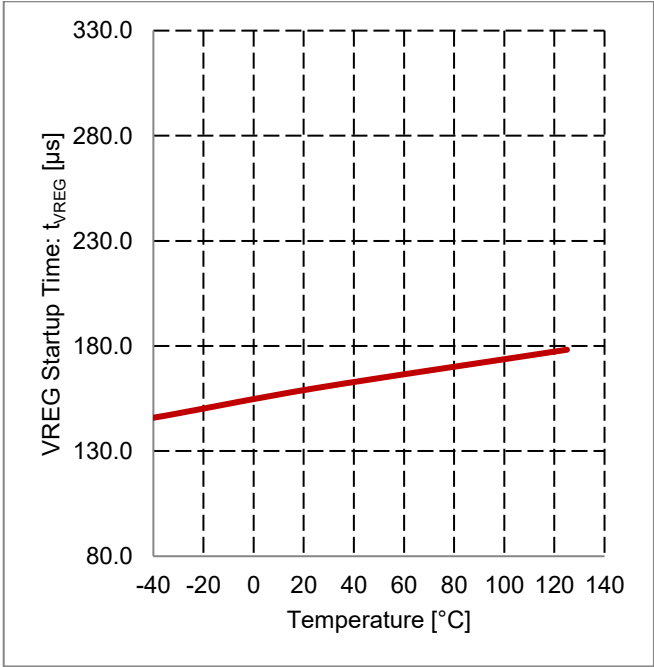


Figure 14. VREG Startup Time vs Temperature

Typical Performance Curves – continued

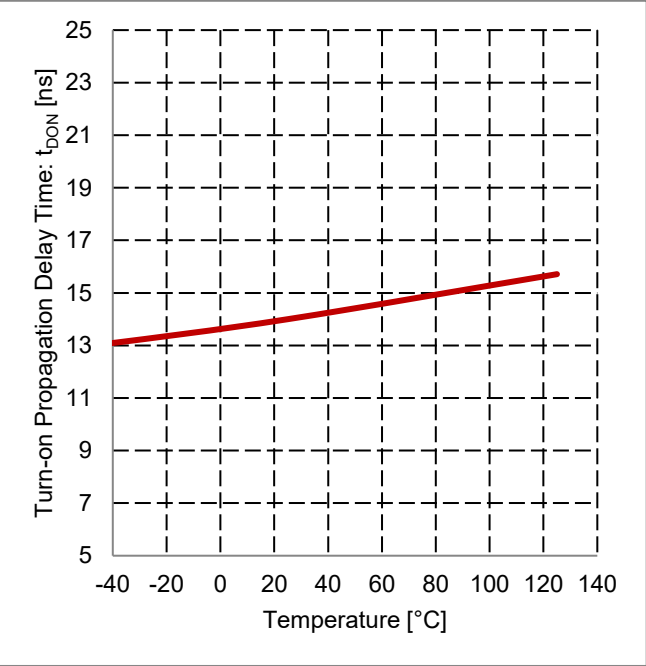


Figure 15. Turn-on Propagation Delay Time vs Temperature

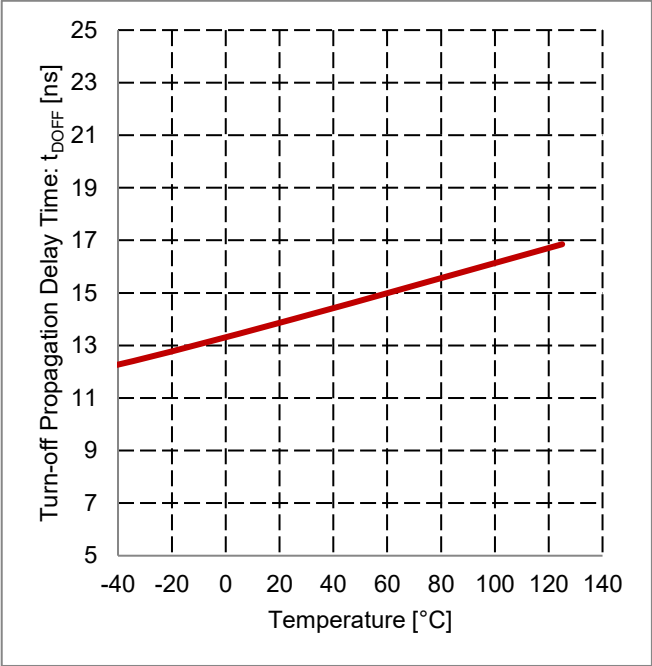


Figure 16. Turn-off Propagation Delay Time vs Temperature

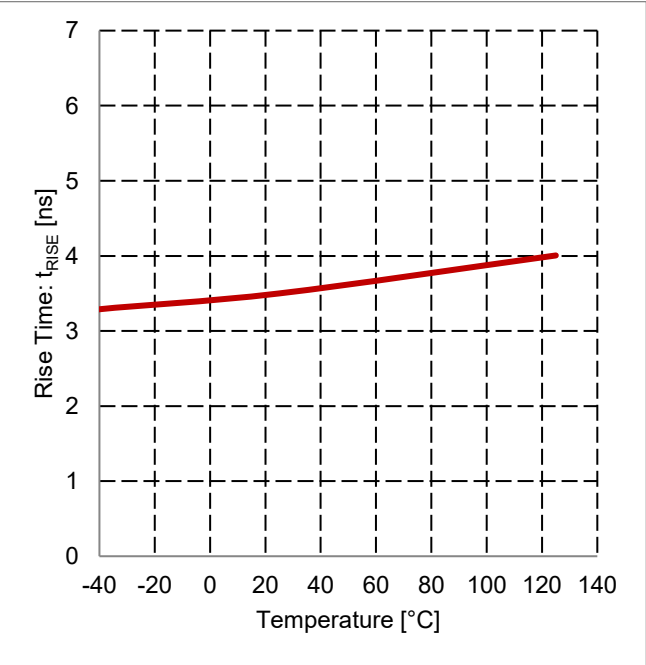


Figure 17. Rise Time vs Temperature

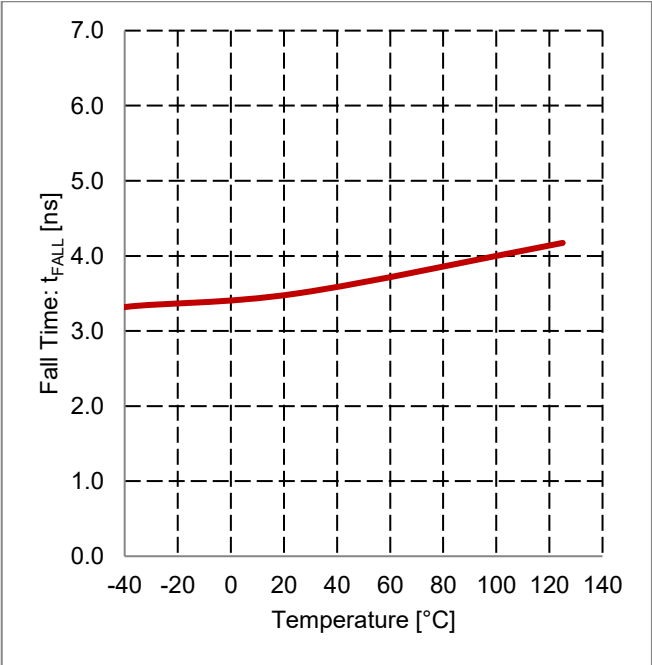


Figure 18. Fall Time vs Temperature

Timing Chart

See the following sections for detailed descriptions.

1 Startup / Shutdown Sequence

The Startup sequence and the shutdown sequence are shown in Figure 19.

Avoid using the power supply line for the supply voltage VDD that changes voltage during operation and be sure to connect a bypass capacitor with an effective capacitance value of 1 μ F or more between the VDD pin and the GND pin as close to IC as possible to prevent a steep slew rate drop in the power supply line.

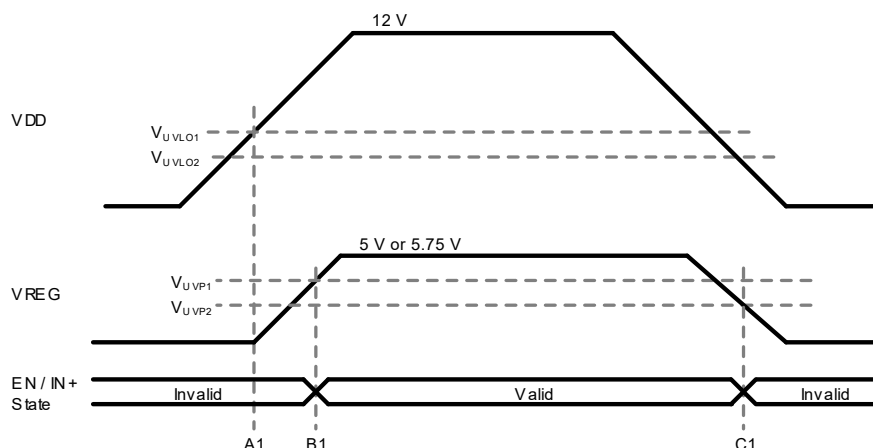


Figure 19. Startup and Shutdown Sequence Timing Chart

- A1: When the VDD pin voltage exceeds V_{UVLO1} , the IC starts operating and the VREG pin voltage begins to rise.
- B1: When the VREG pin voltage exceeds V_{UVP1} , the input signal logic becomes valid. The state of the input becomes effective with the next change after VREG voltage above V_{UVP1} .
- C1: If the VDD pin voltage drops and the VREG pin voltage falls below V_{UVP2} , the logic of the input is invalidated and OUTH = Open and OUTL = Low state is fixed.

2 VREG UVP Detection

The VREG voltage supplies the gate drive voltage of the GaN HEMT, and when the voltage drops below 80 % (Typ) of the output voltage, the driver function is turned off (OUTH = Open, OUTL = Low). The detection function has a delay time of 10 μ s (Typ).

When the VREG voltage returns again to 85 % (Typ) or more of the output voltage, the state of the input pins becomes valid. The state of the input becomes valid at the timing of the next change after the VREG voltage next exceeds V_{UVP1} . The VREG output has an internal overcurrent protection function to prevent IC destruction in the event of a load short. However, this protection function is effective in preventing destruction due to a sudden accident and is not designed for continuous protection operation or use during transient conditions.

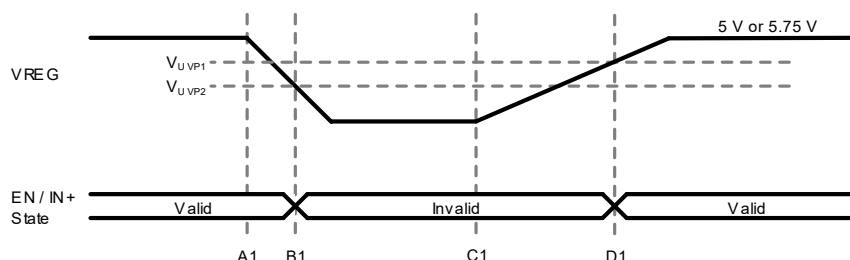


Figure 20. LDO ground-short and return Timing Chart

- A1: The VREG pin voltage becomes lower or shorted to ground for some reason.
- B1: If the VREG pin voltage falls below V_{UVP2} , the input signal logic is invalidated and fixed in the OUTH = Open and OUTL = Low states.
- C1: When VREG is released from the ground-short states, it restarts in the time specified by t_{VREG} .
- D1: When the VREG pin voltage exceeds V_{UVP1} , the logic of the input is valid. The state of the input becomes effective with the next change in VREG voltage above V_{UVP1} .

Application Example

By using this IC, Enhanced-mode GaN HEMTs can be directly applied to systems using Si FETs. Since the IN+ and EN input ranges are allowed up to the supply voltage range of the controller, an additional level shifter is not required.

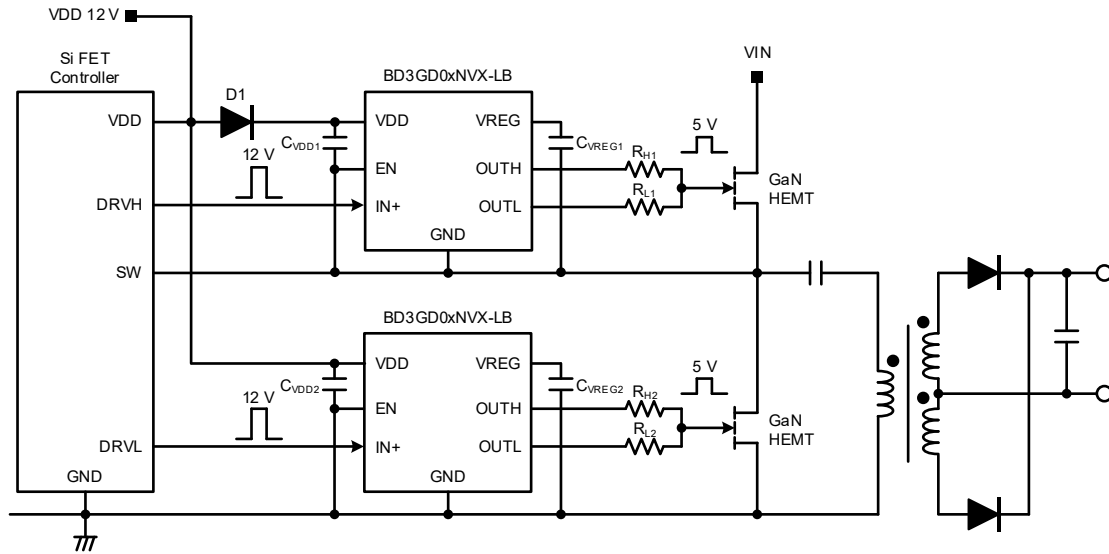


Figure 21. Application Circuit Example

Selection of Components Externally Connected

This gate driver has separate output driver pins for the source and sink sides, and the slew rate of the rising and falling edge of the drive waveform can be individually adjusted by inserting resistors between the gate pins of the GaN HEMT.

The gate resistors R_{GH}/R_{GL} should be selected according to the switching speed of the power device.

Since the switching time (t_{SW}) is taken as the time it takes for the plateau voltage to finish, the turn-on gate resistance R_{GH} is calculated by the following equation.

$$I_G = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \quad [A] \quad [1]$$

$$R_{TOTAL(ON)} = R_{PON} + R_{GH} = \frac{V_{REG} - V_{GS(TH)}}{I_G} \quad [\Omega] \quad [2]$$

$$t_{SW} = \frac{Q_{gs} + Q_{gd}}{I_G} = \frac{(Q_{gs} + Q_{gd})(R_{PON} + R_{GH})}{(V_{REG} - V_{GS(TH)})} \quad [s] \quad [3]$$

Where:

I_G is the Current through the gate of a power device.

Q_{gs} is the Gate-Source charge of power devices.

Q_{gd} is the Gate-to-drain charge of power devices.

$V_{GS(TH)}$ is the Threshold voltage of power devices.

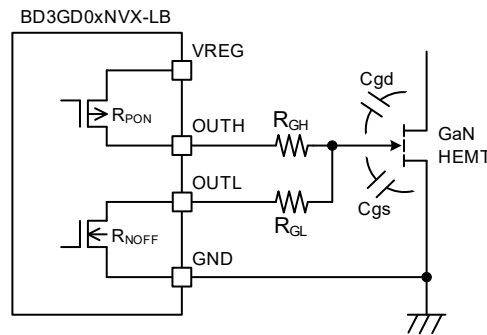


Figure 22. Gate Drive Equivalent Circuit

The slew rate (dV/dt) at the output can be determined by the turn-on gate resistance value. The slew rate of a power device uses the following equation.

$$\frac{dV_D}{dt} = \frac{I_G}{C_{rSS}} \quad [V/s] \quad [4]$$

Where:

C_{rSS} is the Feedback capacitance of power devices.

Substituting equation [4] into equation [2], the gate resistance becomes

$$R_{TOTAL(ON)} = R_{PON} + R_{GH} = \frac{V_{REG} - V_{GS(TH)}}{C_{rSS} \times \frac{dV_D}{dt}} \quad [\Omega] \quad [5]$$

$$R_{GH} = \frac{V_{REG} - V_{GS(TH)}}{C_{rSS} \times \frac{dV_D}{dt}} - R_{PON} \quad [\Omega] \quad [6]$$

Selection of Components Externally Connected – continued

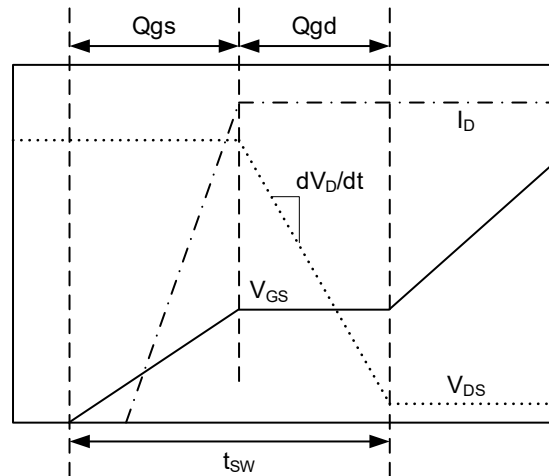


Figure 23. Gate Charging Characteristics of Power Devices

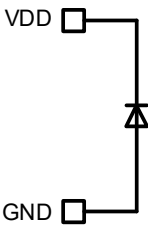
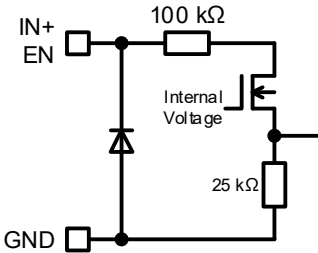
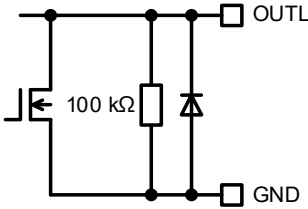
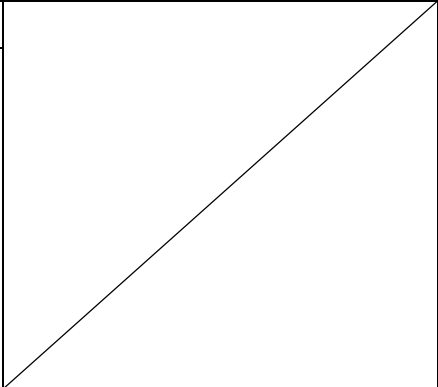
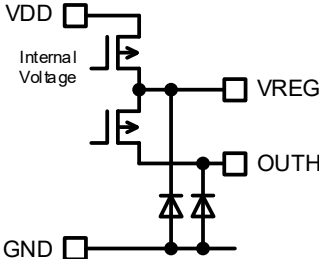
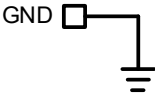
When a power device is off, current flows through C_{gd} when another power device turns on. At this time, the gate resistance value (R_{GL}) should be set so that the gate voltage does not exceed the threshold (and cause self turn-on).

$$V_{GS(TH)} \geq (R_{NOFF} + R_{GL}) \times I_G = (R_{NOFF} + R_{GL}) \times C_{gd} \times \frac{dV_D}{dt} \quad [V] \quad [7]$$

$$R_{GL} \leq \frac{V_{GS(TH)}}{C_{gd} \times \frac{dV_D}{dt}} - R_{NOFF} \quad [\Omega] \quad [8]$$

Each set value obtained from the above formulas should be determined after a thorough evaluation with consideration to the design margin.

I/O Equivalence Circuits

1	VDD	2, 3	EN, IN+	4	OUTL
					
5,6	OUTH, VREG	7	GND		
					

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

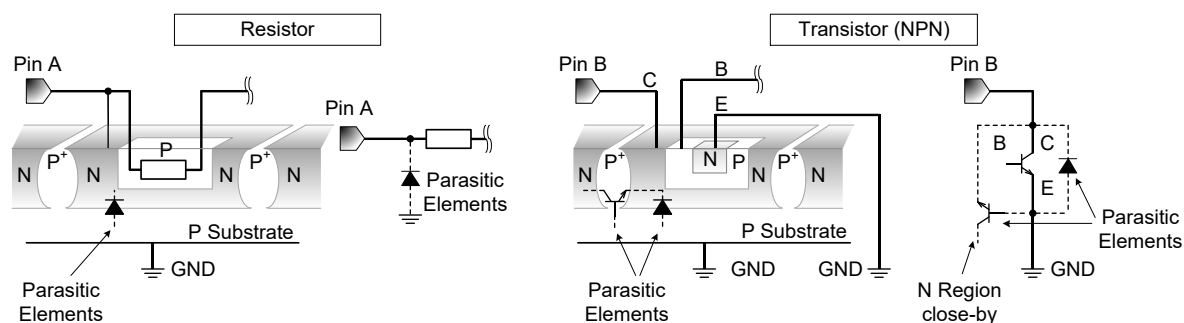
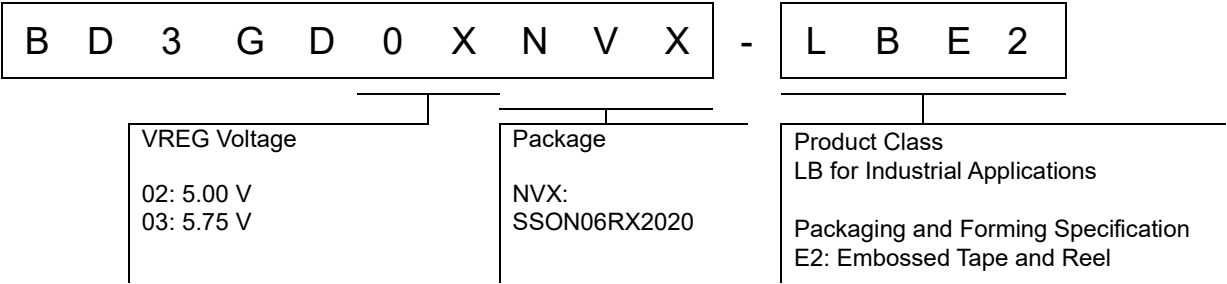


Figure 24. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

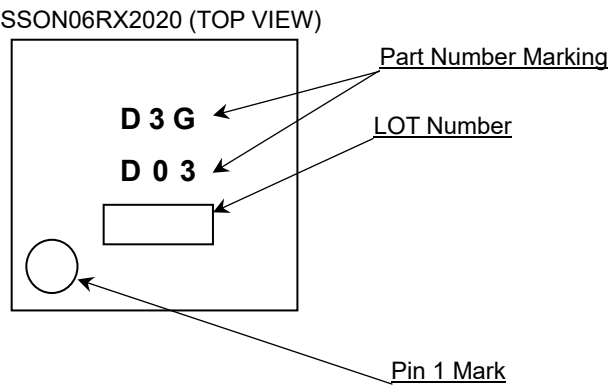
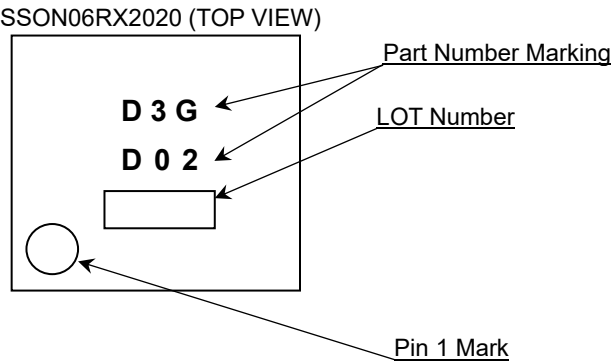
Ordering Information



Lineup

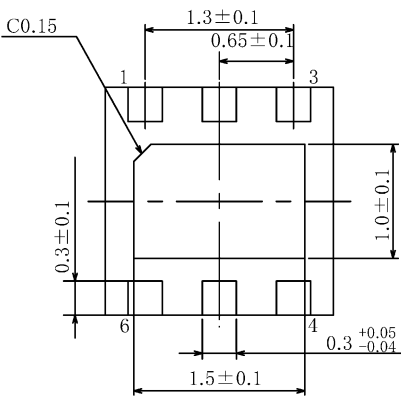
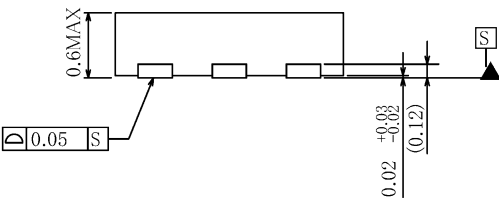
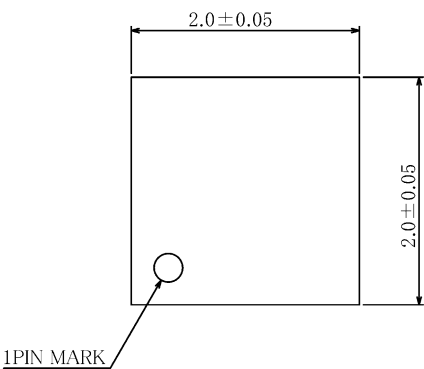
Product Name	Part Number Marking	Orderable Part Number	Package
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BD3GD03NVX-LB	D3GD03	BD3GD03NVX-LBE2	SSON06RX2020

Marking Diagram



Physical Dimension and Packing Information

Package Name	SSON06RX2020
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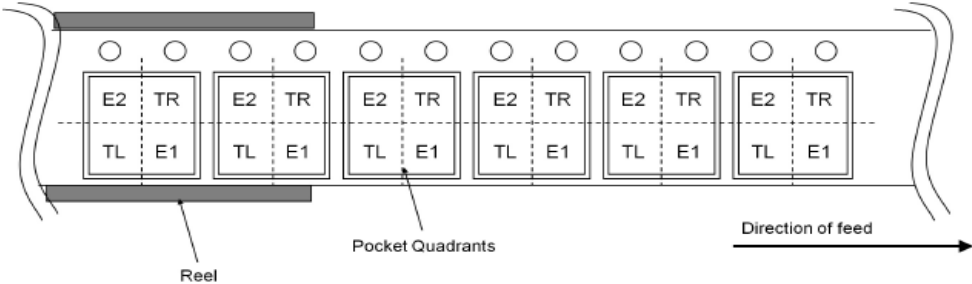


(UNIT:mm)

PKG:SSON06RX2020
Drawing No.EX068-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
06.Feb.2026	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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