4A/6A 1ch high-speed gate driver with built-in LDO for Enhancement mode GaN HEMT

BD3GD02NVX-LB BD3GD03NVX-LB

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

The BD3GD02NVX-LB and BD3GD03NVX-LB are 1-channel gate drivers for driving GaN HEMTs at high speed. The high-speed gate driver circuit for GaN HEMTs and the LDO that generates the gate drive voltage are enclosed in a 6-pin SON compact package, which is especially optimized for driving E-mode GaN HEMT devices.

Since the input is compatible with the gate drive voltage for Si FETs, it can be connected to the gate drive line for Si FETs in an existing system to drive GaN HEMTs without any system modification.

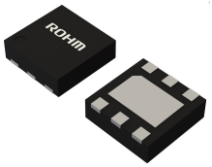
The output pins are divided into source and sink drive pins, and the slew rates of the source and sink sides can be adjusted separately with external resistors.

As protection functions, a low input malfunction prevention circuit (UVLO) between VDD and GND and a low output voltage protection circuit (UVP) between VREG and GND are provided.

Key Specifications

- Power Supply Voltage Range (VDD): V_{VREG}+1.5V to 18 V
- Input Voltage Range (IN+, EN): 0 V to 18 V
- LDO Output Voltage (Gate Drive Voltage)
  - BD3GD02NVX-LB: 5.0 V (Typ)
  - BD3GD03NVX-LB: 5.75 V (Typ)
- Output Current I_{O+} / I_{O-} : 4 A / 6 A (Typ)
- Turn On Propagation Delay: 14 ns (Typ)
- Turn Off Propagation Delay: 14 ns (Typ)
- Minimum Input Pulse Width: 24 ns (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
SSON06RX2020	2.0 mm x 2.0 mm x 0.6 mm



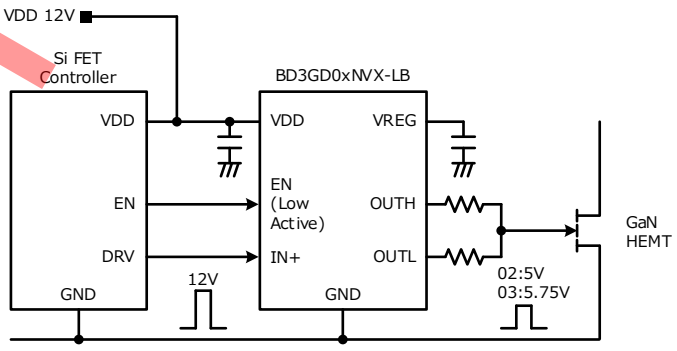
Features

- Built-in LDO for drive voltage control.
- Wide operating input voltage range.
- Supports non-invert operating input and invert operating input.
- Low propagation delay.
- Built-in VDD UVLO Protection.
- Built-in VREG UVP Protection.

Applications

- Industrial Equipment.
- GaN Applications.
- PFC or LLC topology power supply.
- Power supplies with bridge topology configuration.

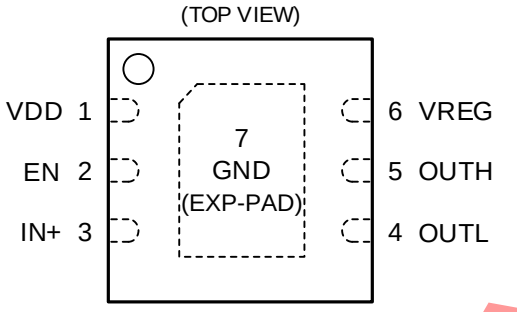
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

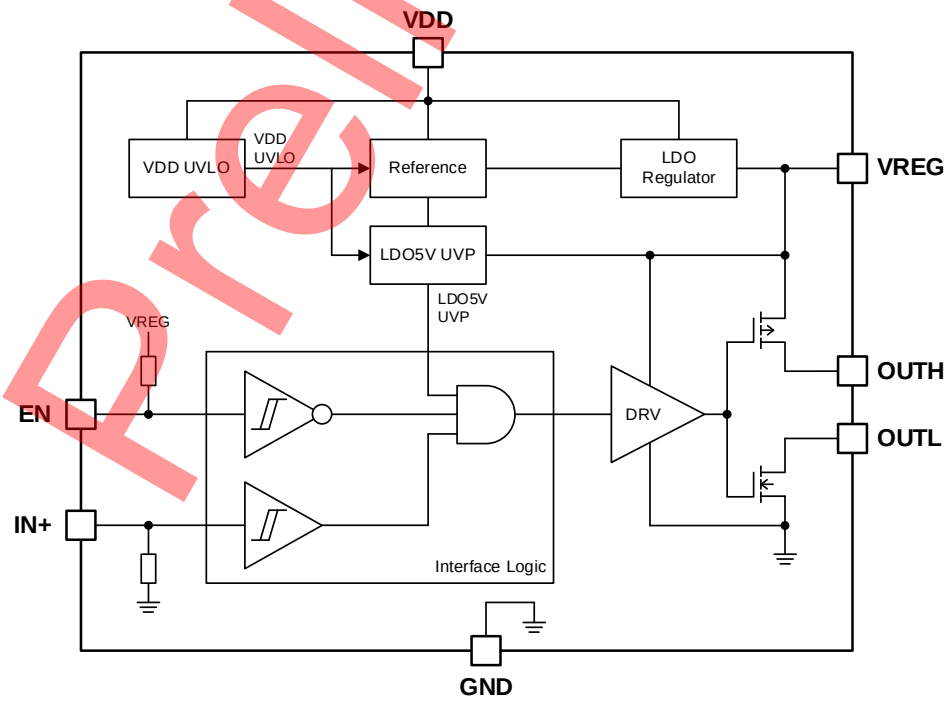
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	VDD	Power supply pin.
2	EN	Enable pin. (Low active)
3	IN+	Non-inverting gate drive input pin.
4	OUTL	Sink side output pin for gate driving.
5	OUTH	Source side output pin for gate driving.
6	VREG	Capacitor connection pin for gate drive voltage generation circuit.
7	GND (EXP-PAD)	GND pin. This terminal also serves as a backside heat dissipation pad. Excellent heat dissipation characteristics can be obtained by connecting to the internal PCB ground plane using vias.

Block Diagram



Description of Blocks

Outline

This product, which incorporates a gate driver circuit, an LDO regulator for generating gate drive voltage, and a protection function, has the function of converting the input gate driver drive voltage for Si-FETs to the gate drive voltage of GaN HEMTs, so that GaN HEMTs can be used in existing applications with gate drive outputs for Si-FETs. Therefore, GaN HEMTs can be used without system modifications by connecting to existing applications with gate drive outputs for Si-FETs.
In addition, an UVLO (Under Voltage Lock Out) function to monitor VDD and an UVP (Under Voltage Protection) function to monitor the LDO regulator's output are integrated to protect the product from damage.

Description of each block

1. Gate Driver (DRV) block
   This is a gate driver for GaN HEMT and drives the gate of GaN HEMT device to the High level of VREG output and Low level of GND. Until VREG output is determined to be normal (no UVP protection detected on VREG), the driver remains in off state (OUTH=Open, OUTL =Low).

2. LDO Regulator block
   A 2.2 µF ceramic capacitor C_{VREG} is required between the VREG and GND pins.
   This LDO provides only the gate charge current to the GaN HEMT. It cannot be used for external power supply.

3. Interface block
   The input interface circuit allows direct connection and use of voltage signals up to 18 V, such as the output of a general MCU or ACDC controller, as input signals for the IN+ and EN pins.
   Table 1 shows the driver operation with the combination of the EN and IN+ pins.

4. VREG UVP block
   A low output voltage protection circuit that monitors the built-in LDO output and turns off the driver function (OUTH=Open, OUTL=Low) when the VREG pin becomes 85 % (Typ) or lower than the output voltage. The threshold voltage has a hysteresis of 5 % (Typ) with respect to the output voltage.
   The delay time is 10 µs (Typ) for detection.

5. VDD UVLO block
   This is a low input voltage malfunction prevention circuit that monitors VDD voltage and turns off the driver function when VDD falls below 3.55 V (Typ). The threshold voltage has a hysteresis of 0.25 V (Typ).

6. Reference block
   Generates a reference voltage from the VDD input voltage to generate the VREG voltage and the protection circuit detection voltage.

Table 1. Function table of driver.

VDD	VREG	IN+	EN	OUTH	OUTL
$< V_{UVLO}$	OFF	X	X	Open	Low
$\geqq V_{UVLO}$	$< V_{UVP}$	X	X	Open	Low
$\geqq V_{UVLO}$	$\geqq V_{UVP}$	L	L	Open	Low
$\geqq V_{UVLO}$	$\geqq V_{UVP}$	H	L	High	Open
$\geqq V_{UVLO}$	$\geqq V_{UVP}$	L	H	Open	Low
$\geqq V_{UVLO}$	$\geqq V_{UVP}$	H	H	Open	Low

X: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Maximum Input Voltage 1	V_{MAX1}	-0.3 to +20	V	VDD pin
Maximum Input Voltage 2	V_{MAX2}	-0.6 to +20	V	IN+ pin
Maximum Input Voltage 3	V_{MAX3}	-0.6 to +20	V	EN pin
Maximum Input Voltage 4	V_{MAX4}	-0.3 to +7.0	V	VREG pin
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
SSON06RX2020				
Junction to Ambient	θ_{JA}	284.5	83.2	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	35.0	22.0	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range	V_{DD}	V_{VREG} + 1.5	12	18	V	VDD pin VREG Load Current = 10 mA
Input Voltage Range 1	V_{IN+}	0	-	18	V	IN+ pin
Input Voltage Range 2	V_{EN}	0	-	18	V	EN pin
Input High Pulse Width	t_{IN_MIN}	10	-	-	ns	
VREG Output Capacitor Range	C_{VREG}	0.47	2.2	-	µF	Ceramic capacitors are recommended.*(Note 1)*
Operating Temperature	Topr	-40	-	+125	°C	Ambient temperature

(Note 1) The capacitance of the capacitor should be set so that it does not fall below the minimum value in consideration of temperature characteristics, DC bias characteristics.

Electrical Characteristics
(Unless otherwise specified V_{DD} = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
VDD Current Consumption 1	I_{VDD1}	-	70	120	µA	V_{IN+} = VDD、V_{EN} = 0 V VDD = 3 V
VDD Current Consumption 2	I_{VDD2}	-	70	120	µA	V_{IN+} = 0 V、V_{EN} = VDD VDD = 3 V
VDD Terminal						
VDD UVLO Release Voltage	V_{UVLO1}	3.55	3.80	4.15	V	VDD Sweep Up
VDD UVLO Detection Voltage	V_{UVLO2}	3.30	3.55	3.90	V	VDD Sweep Down
VDD UVLO Hysteresis Voltage	V_{UVLO3}	-	0.25	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2}
VREG Terminal						
VREG Voltage （Gate Drive Voltage）	V_{VREG}	4.75	5.00	5.15	V	BD3GD02NVX, No Load
		5.58	5.75	5.92	V	BD3GD03NVX, No Load
VREG UVP Release Voltage	V_{UVP1}	80	85	90	%	Percentage of V_{VREG} voltage
VREG UVP Detection Voltage	V_{UVP2}	75	80	85	%	Percentage of V_{VREG} voltage
VREG UVP Hysteresis Voltage	V_{UVP3}	-	5	-	%	V_{UVP3} = V_{UVP1} - V_{UVP2}
IN+ Terminal, EN Terminal						
Threshold Voltage 1	V_{INPOS}	1.85	2.05	2.25	V	Sweep Up
Threshold Voltage 2	V_{INNEG}	0.90	1.10	1.30	V	Sweep Down
Hysteresis Voltage	V_{INHYS}	-	0.95	-	V	V_{INHYS} = V_{INPOS} – V_{INNEG}
Input Current	I_{INLEAK}	80	165	-	µA	V_{IN+} = V_{EN} = 5 V
OUTH Terminal, OUTL Terminal						
OUTH Pull Up Resistance	R_{OUTH}	-	1.0	2.0	Ω	I_{OUTH} = -50 mA
OUTL Pull Down Resistance	R_{OUTL}	-	0.35	1.50	Ω	I_{OUTL} = 50 mA
Start Up Time						
Start Up Delay Time	t_{D_IN}	-	15	30	µs	
VREG Start Up Time	t_{VREG}	50	100	200	µs	C_{VREG} = 2.2 µF (nominal value)

Electrical Characteristics– continued
(Unless otherwise specified V_{DD} = 12 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Switching Specifications						
Output source side maximum current	$I_{OUTMAXH}$	-	4.0	-	A	*(Note 1)*
Output sink side maximum current	$I_{OUTMAXL}$	-	6.0	-	A	*(Note 1)*
Turn ON Propagation Delay	t_{DON}	-	14	25	ns	C_{LOAD} = 1 nF IN = 0 V → 5 V *(Note 2)*
Turn OFF Propagation Delay	t_{DOFF}	-	14	25	ns	C_{LOAD} = 1 nF IN = 5 V → 0 V *(Note 2)*
Rise Time	t_{RISE}	-	5	-	ns	C_{LOAD} = 1 nF *(Note 2)*
Fall Time	t_{FALL}	-	5	-	ns	C_{LOAD} = 1 nF *(Note 2)*

(Note 1) Not tested.
(Note 2) See "Switching Parameter Measurement Information.

Switching parameter measurement information

Figure 1 shows a circuit for measuring switching parameters.
Figure 2 shows the measurement information for the switching parameters.

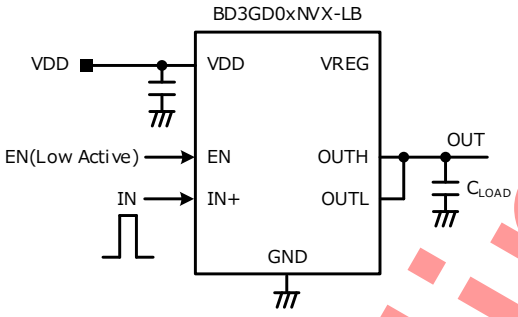


Figure 1 Measurement circuit diagram

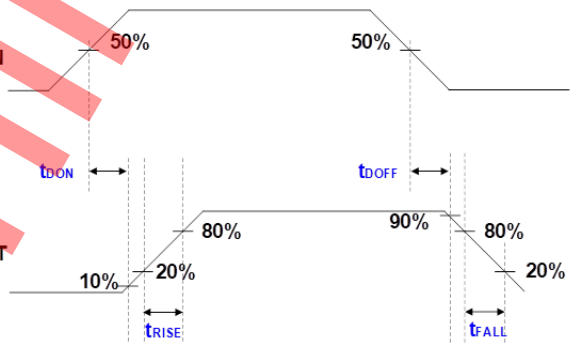


Figure 2 Switching parameter measurement information

1. **Turn On Delay TIme: t_{DON}**
   The turn-on delay time is the time from the rising edge of the IN voltage (at 50 % of the IN's high voltage level) until the OUT begins to turn on (when OUT rises to 10 % of V_{OUTH}).

2. **Output Rise Time: t_{RISE}**
   The output rise time is the time it takes for OUT to rise from 20 % to 80 % of V_{OUTH}.

3. **Turn Off Delay Time: t_{DOFF}**
   The turn-off delay time is the time from the falling edge of the IN voltage (at 50 % of the IN's high voltage level) until the OUT begins to turn off (when OUT falls to 90 % of V_{OUTH}).

4. **Output Fall Time: t_{FALL}**
   The output fall time is the time it takes for OUT to fall from 80 % to 20 % of V_{OUTH}.

Typical Performance Curves

Timing Chart

Startup / Shutdown Sequence

The startup sequence is shown in Figure 3. See the following sections for detailed descriptions.

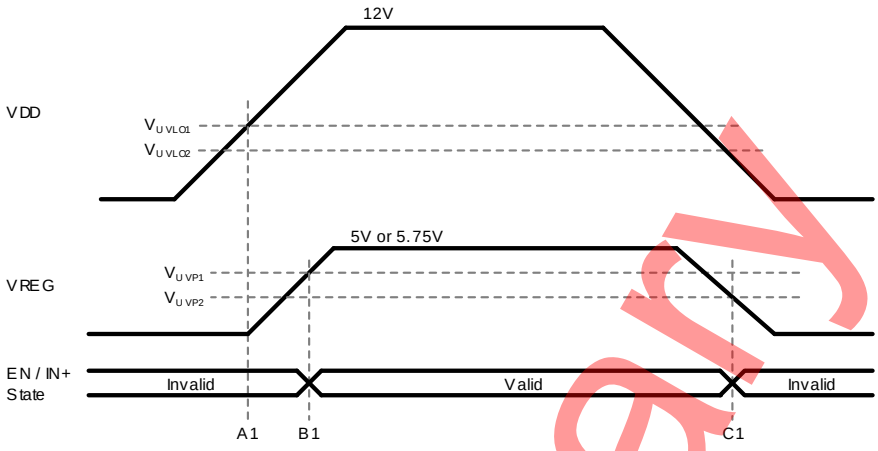


Figure 3. Startup and shutdown sequence Timing chart

A1: When the VDD pin voltage exceeds V_{UVLO1}, the IC starts operating and the VREG pin voltage begins to rise.
B1: When the VREG pin voltage exceeds V_{UVP1}, the input signal logic becomes valid.
C1: If the VDD pin voltage drops and the VREG pin voltage falls below V_{UVP2}, the logic of the input is disabled and OUTH = Open and OUTL = Low state is fixed.

Application Example

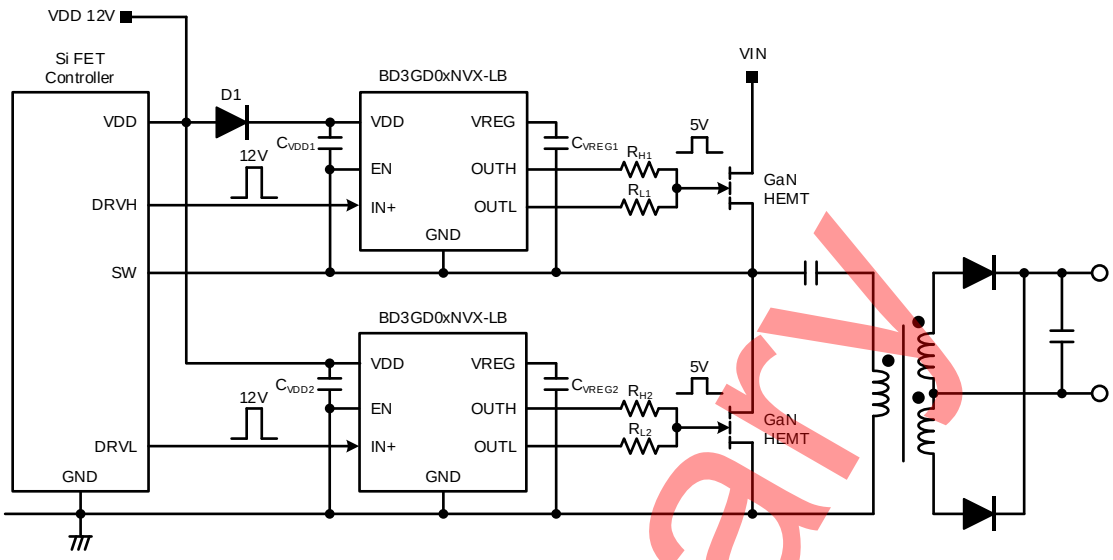
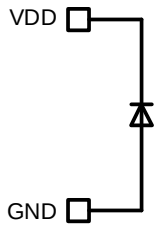
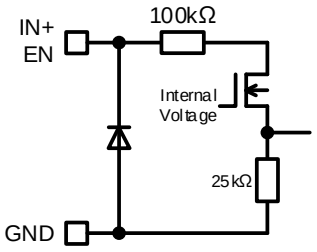
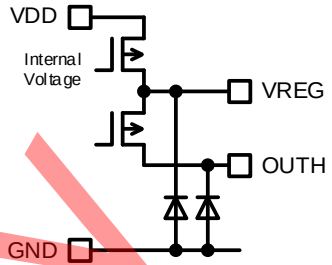
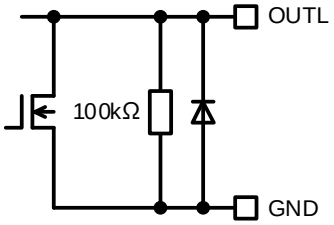
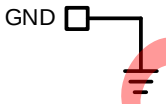


Figure 4. Application Circuit Example

I/O Equivalence Circuits

1. VDD	2. EN, 3. IN+	4. OUTH, 6. VREG
		
5. OUTL	**7. GND**	
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

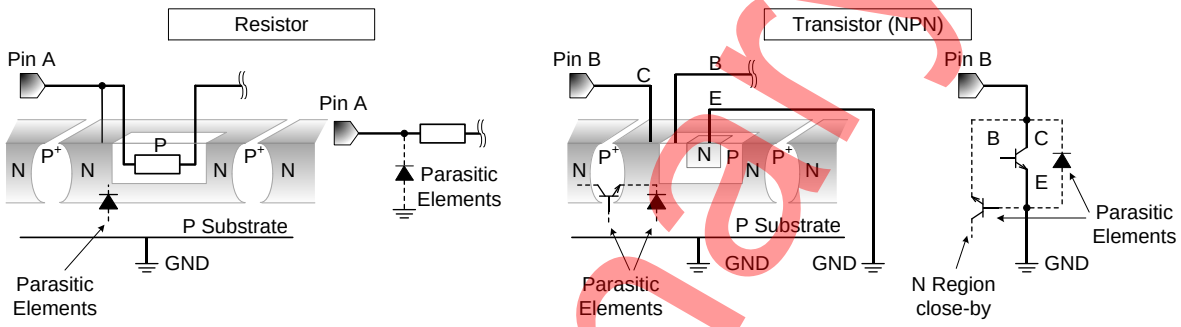


Figure 5. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

B	D	3	G	D	0	X	N	V	X	-	L	B	E	2

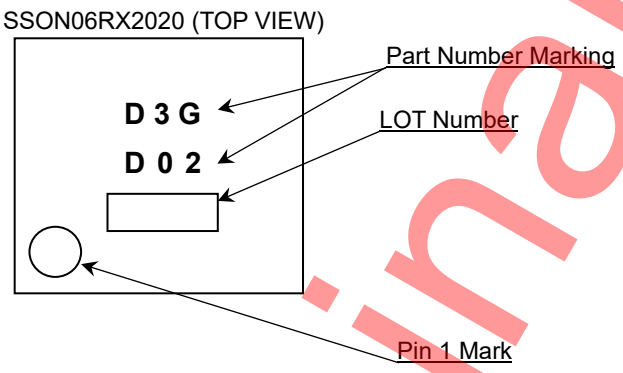
VREG Voltage
02: 5.0V
03: 5.75V

Package
NVX:
SSON06RX2020

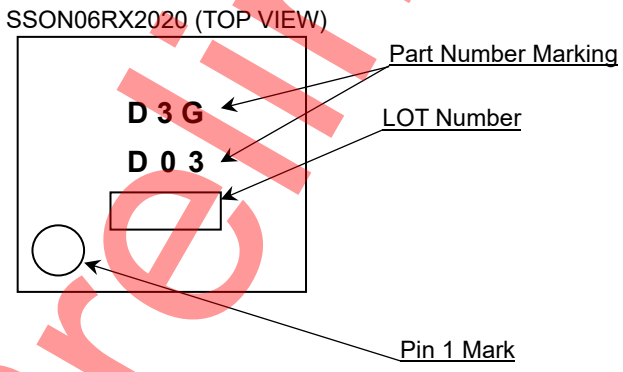
Rank
LB for Industrial Applications

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram（BD3GD02NVX-LB）

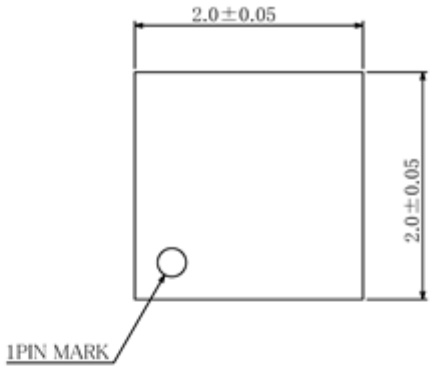


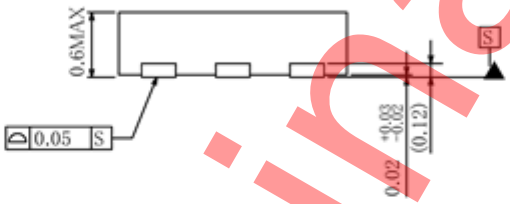
Marking Diagram（BD3GD03NVX-LB）

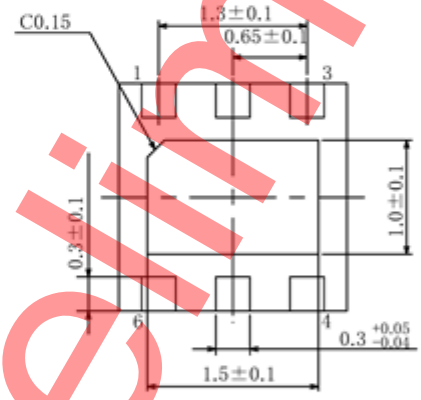


Physical Dimension and Packing Information

Package Name	SSON06RX2020





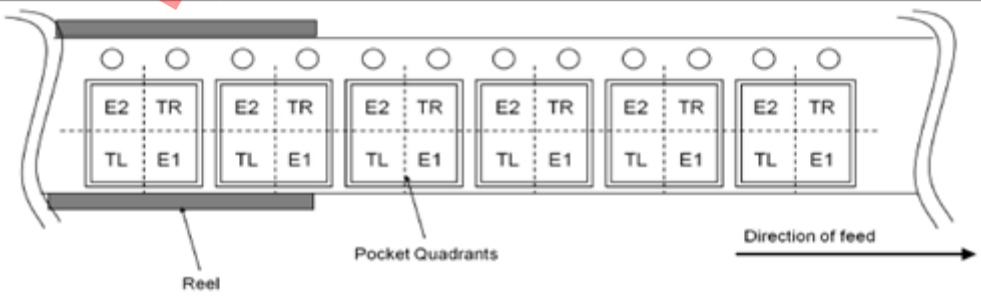


(UNIT:mm)

PKG:SSON06RX2020
Drawing No.EX068-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
30.Aug.2024	000	New Release for Target Specification. After the specification fix, it will be changed to the 001 version.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

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