650V Half Bridge Driver IC for GaN HEMT

BD4HB00FV-LB

Preliminary

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

BM4HB00FV-LB is 650V half bridge driver for Enhancement mode GaN HEMT. This IC provides an optimum solution for all Half Bridge Topology that requires high switching applications.
The driver includes High-Side and Low-Side Nano Cap LDO^{TM} supply for driver.
In addition, the built-in Active Miller Clamping function provides robust driver's bias rales.
Owing to this, this IC provides stable dV/dt operation rated up to 150 V/ns for both driver output stages.

Key Specifications

- Power Supply Voltage Range
  - VCC pin: 9.3 V to 25 V
  - BST pin referred to SW: 8.0 V to 25 V
  - BST pin: 683 V(Max)
  - SW pin: -5.0 V to +650 V (Max)
  - HIN / LIN pin: -0.3 V to +33 V (Max)
- Output Current Io+/Io-: 2A / 2A (Typ)
- VCC Quiescent Current: 210 µA (Typ)
- BST Quiescent Current: 120 µA (Typ)
- Propagation Delay Time: 50 ns (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
SSOP-B20	6.5 mm x 6.4 mm x 1.45 mm pitch 0.65 mm

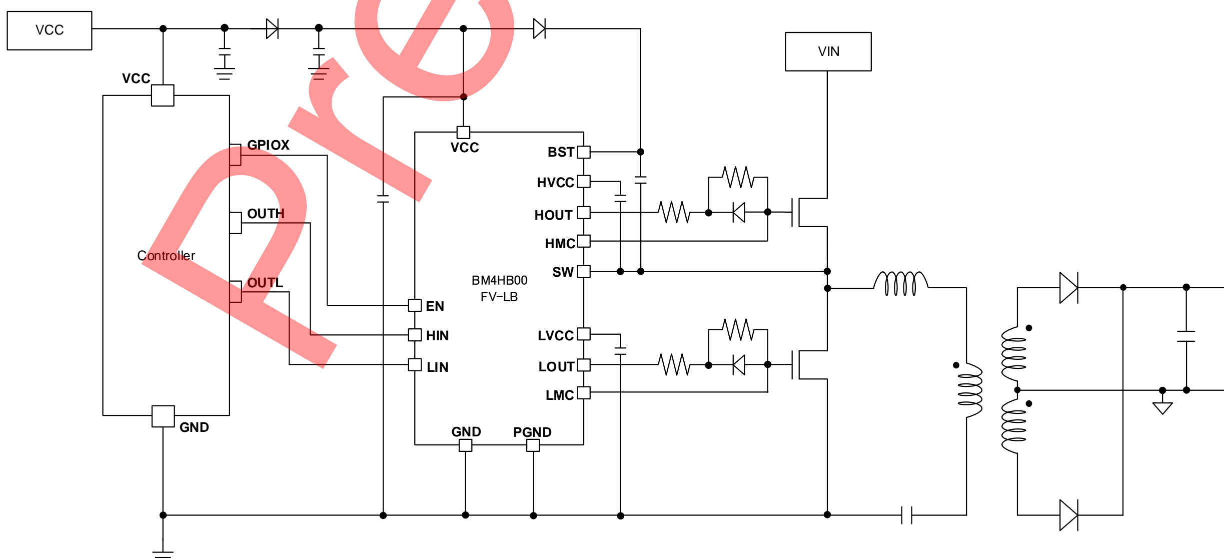
Features

- Active Miller Clamping
- Wide Operating Range for VCC Pin Voltage
- Wide Operating Range for IN Pin Voltage
- Low VCC Quiescent and Operating Current
- Low BST Quiescent and Operating Current
- Low Propagation Delay
- High dv/dt Immunity
- Integrated High Precision LDO for Gate Drive
- Enable Signal Input
- VCC UVLO Protection
- LVCC and HVCC UVLO Protection
- Thermal Shutdown Protection
- SSOP-B20 Package

Applications

- Industrial Equipment, Power Supply by Bridge Topology such as Totem-pole PFC, LLC, Active Clamp Flyback, etc.

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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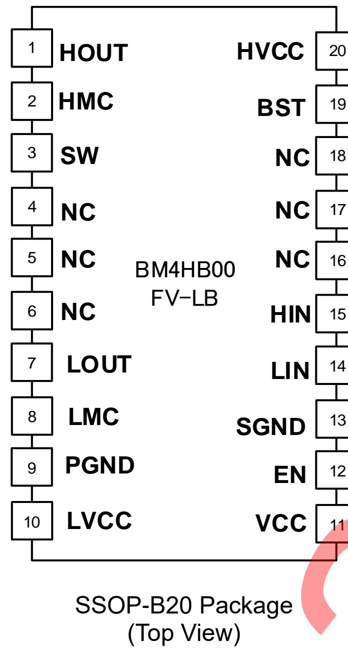
Pin Configuration



SSOP-B20 Package
(Top View)

Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	HOUT	I/O	High side driver output pin
2	HMC	I	High side mirror clamp input pin
3	SW	I/O	Half bridge output pin
4, 5, 6, 15, 16, 17	N.C.	-	Non connection (Note 1)
7	LOUT	I/O	Low side driver output pin
8	LMC	I	Low side mirror clamp input pin
9	PGND	O	Low side power GND pin
10	LVCC	O	Low side driver power supply pin
11	VCC	I	Logic side power supply pin
12	EN	I	Enable signal input pin
13	GND	O	Logic side GND pin
14	LIN	I	Low side driver logic input pin
15	HIN	I	High side driver logic input pin
19	BST	O	Bootstrap diode anode connection pin
20	HVCC	O	High side driver power supply pin

(Note 1) Do not connect to other pins.

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Block Diagram

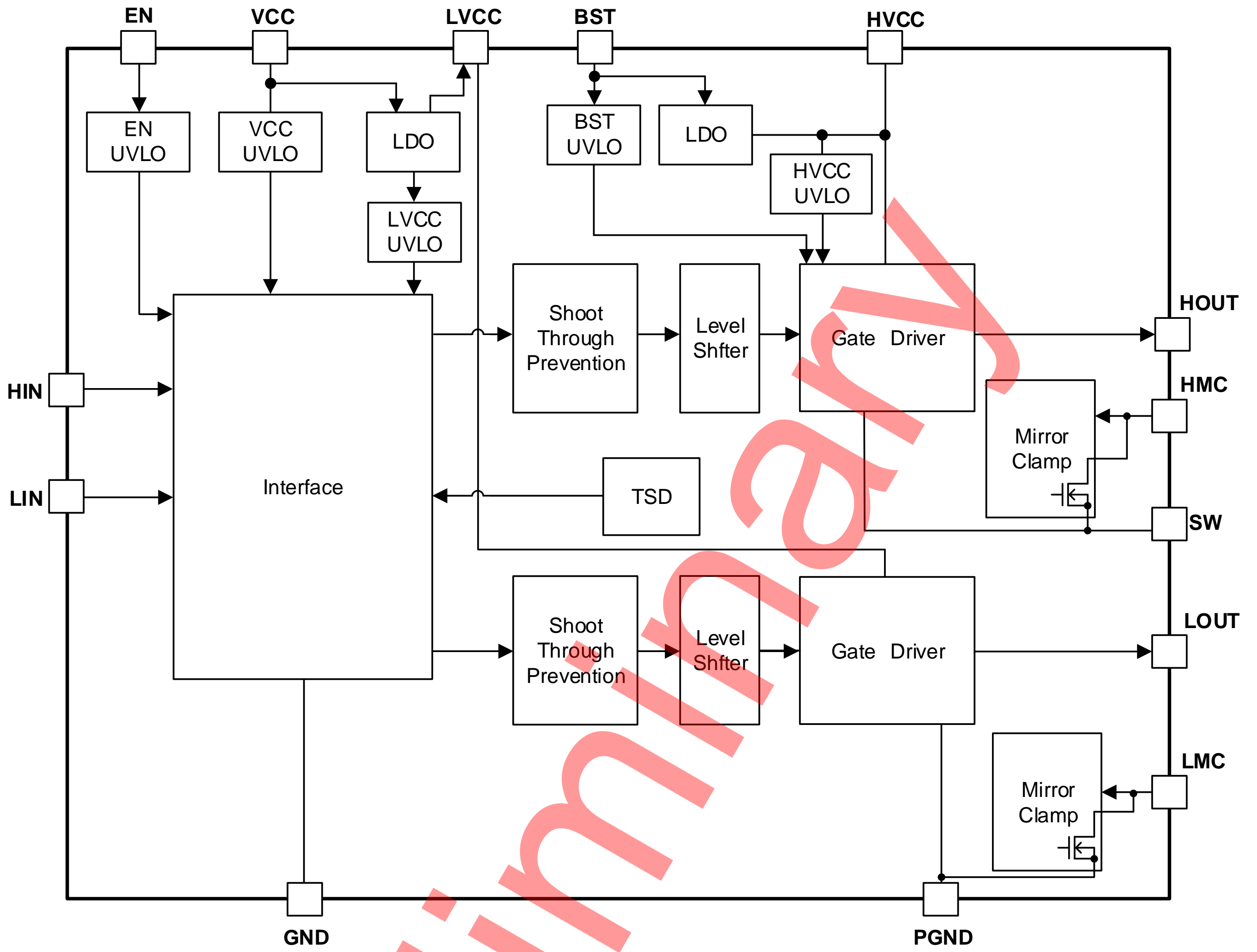

Figure 1. Block Diagram

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Description of Blocks

1 Overview

The IC, which gate drivers for high and low side, additional functions such as protections, offers an optimum solution for making high power density design much easier and more efficient.
Furthermore, various protections such as VCC UVLO, EN UVLO, LVCC UVLO, BST UVLO, HVCC UVLO and thermal shutdown (TSD) are also integrated to protect this IC from damages.

2 Feature Descriptions

The IC is designed to be efficient, robust, and easy using.

2.1 Gate Driver

This IC integrates the original high and low side gate driver for the enhancement-mode GaN devices.

2.2 Level Shifter

This IC integrates level shifter circuit which has low propagation delay and high dv/dt immunity.

2.3 VCC UVLO, EN UVLO, LVCC UVLO, BST UVLO, HVCC UVLO, TSD

This IC has some protection circuits.

2.4 LDO

This IC integrates a LDO regulator with 5.75 V output voltage which is outputted from LVCC pin and HVCC pin.
The low side LDO output (LVCC pin voltage) is disabled when VCC UVLO is detected.
It is recommended to use an output capacitor C_{LVCC} of at least 0.22 µF between the LVCC pin and the PGND pin.
Also, the high side LDO output (HVCC pin voltage) is disabled when BST UVLO is detected.
It is recommended to use an output capacitor C_{HVCC} of at least 0.22 µF between the HVCC pin and the SW pin.
The ceramic capacitor which has low ESR should be used for an output capacitor C_{LVCC} and C_{HVCC}.

2.5 Interface

It is possible to use the output of most of general MCUs or ACDC controllers as the HIN pin's input signal or LIN pin's input signal directly, due to the original interface circuit.
The relationship between HIN or LIN pin's logic signal level and high or low side driver outputs state are shown in Table 1.
However, both side driver output (HOUT and LOUT) are forced to be OFF state if either VCC UVLO, EN UVLO, LVCC UVLO, or TSD is detected.
Also, High side deriver output (HOUT) is forced to be OFF state if BST UVLO or HVCC UVLO is detected.

Table 1. Relationship between HIN or LIN pin's logic signal level and high or low side driver outputs state

Input		Output	
HIN	LIN	LOUT	HOUT
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF

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Feature Descriptions – continued

2.6 Shoot Through Prevention

This IC integrates shoot through prevention function.
This function prevents logic input signal on one side from propagating to the driver output (HOUT or LOUT) and turning it on for turn-on mask time t_{MASK} after the logic input signal on the other side is turned off.
This function does not affect the delay time from input to gate driver outputs when the dead time between LIN and HIN.
For the example, the timing chart when the Shoot Through Prevention function operates in Figure 2.

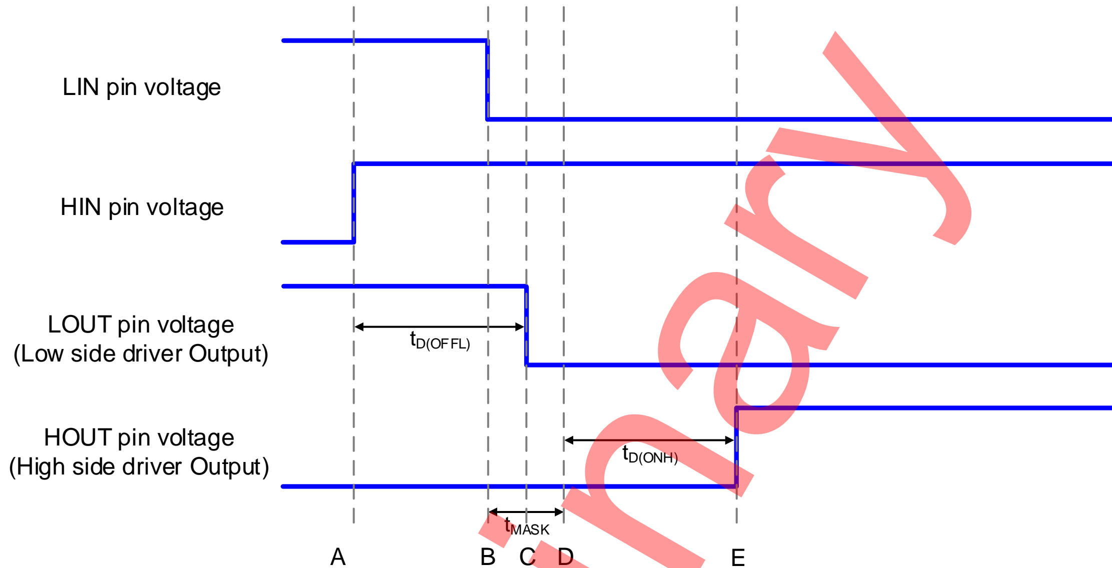

Figure 2. Shoot Through Prevention function

A: HIN logic input signal is turned on while LIN Logic input singal is ON.
B: LIN logic input signal is turned off and t_{MASK} starts to be counted.
C: Low side gate driver output (LOUT) is turned off after the low side turn-off delay time $t_{D(OFFL)}$ from A due to interface logic.
D: The period of t_{MASK} ends and HIN logic input signal starts to be propagated to high side gate driver output (HOUT).
E: High side gate driver output is turned on after the high side turn-on delay time $t_{D(ONH)}$ from D.

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Description of Blocks – continued

2.7 Mirror Clamp

This IC integrates high side and low side Mirror Clamp function.

Table 2. Low side Mirror Clamp state

LIN	LMC	Internal MOSFET of the LMC pin
0	Over than V_{MC}	OFF
0	Less than V_{MC}	ON
1	Over than V_{MC}	OFF
1	Less than V_{MC}	OFF

Table 3. High side Mirror Clamp state

HIN	LMC	Internal MOSFET of the HMC pin
0	Over than V_{MC}	OFF
0	Less than V_{MC}	ON
1	Over than V_{MC}	OFF
1	Less than V_{MC}	OFF

For the example, the timing chart when the low side Mirror Clamp function operates in Figure 3.

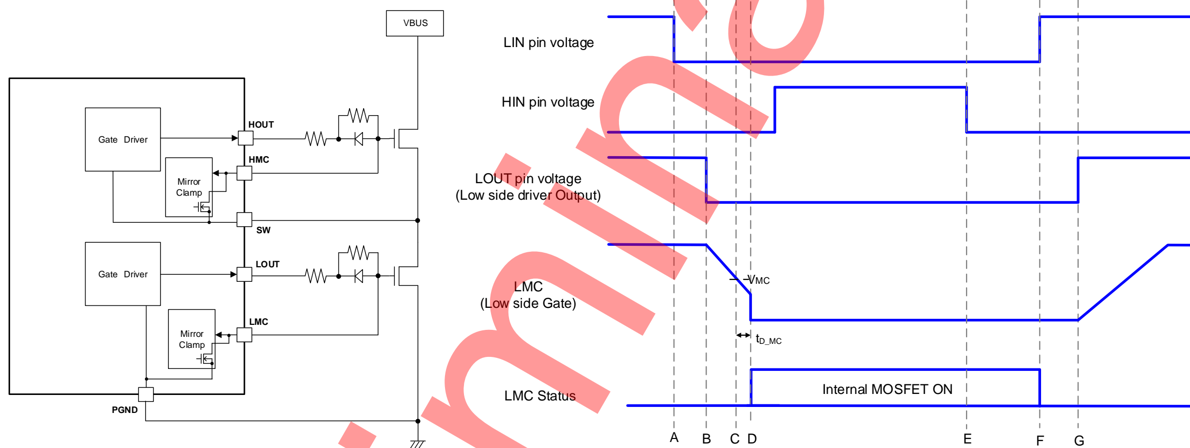

Figure 3. Mirror Clamp Function (Low Side)

A: LIN logic input signal is turned off.
B: Low side gate driver output (LOUT) is turned off and LMC pin voltage (Low side Gate) is falling.
C: LMC pin voltage fall under V_{MC}, Mirror Clamp function is detected.
D: The internal MOSFET is turned on after t_{D_MC} from C.
E: LIN logic input signal is turned on and the internal MOSFET is turned off.
F: LOUT pin voltage is turned on and Low side Gate is rising.

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Description of Blocks – continued

3 Start Sequence

Start sequence is shown in Figure 4.

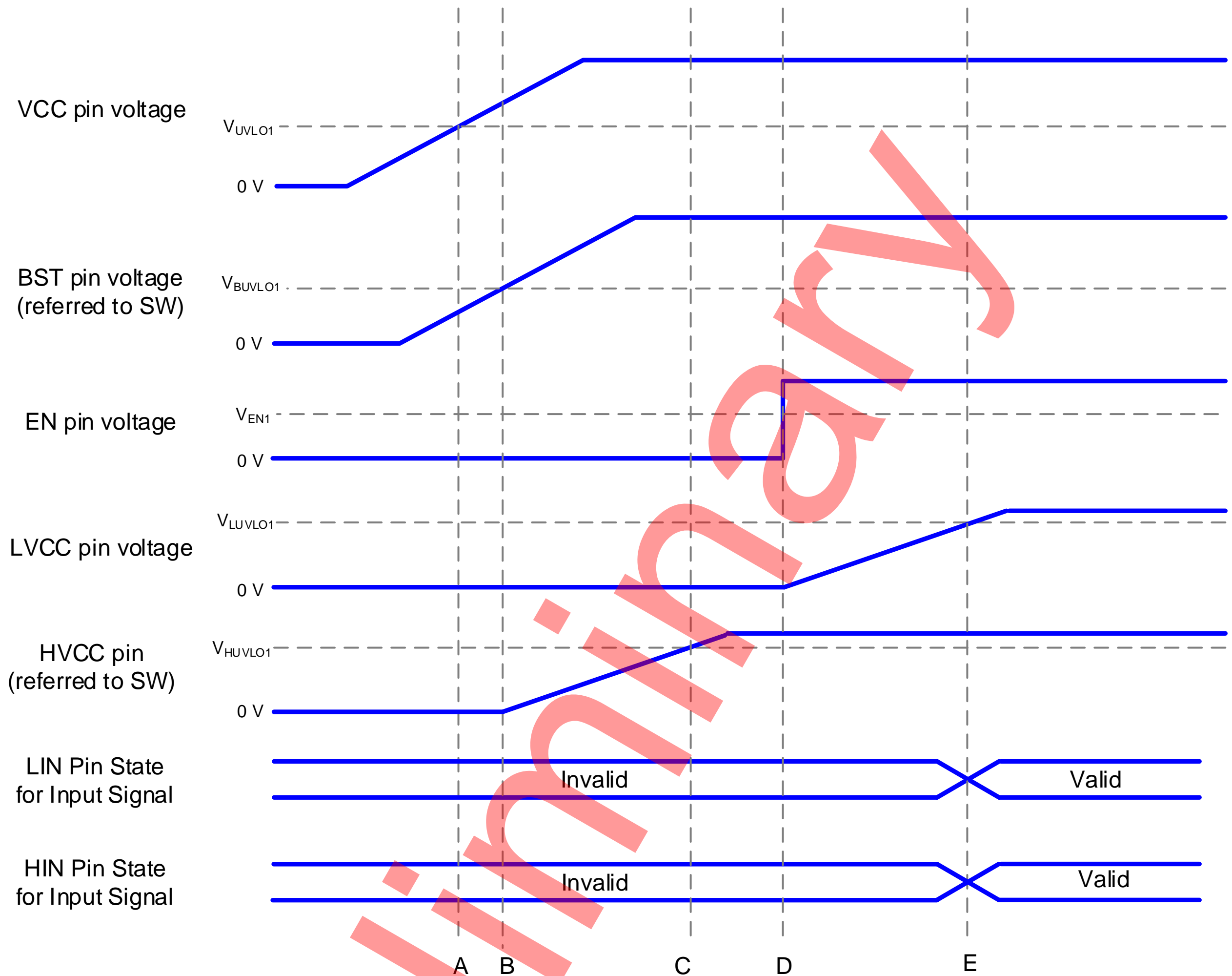

Figure 4. Start Sequences

A: When the VCC pin voltage exceeds V_{UVLO1}, VCC UVLO is released.

B: When the BST pin voltage exceeds V_{BUVLO1}, BST UVLO is released, the LDO regulator for high side drive starts, and HVCC pin voltage starts to rise.

C: When the HVCC pin voltage exceeds V_{HUVLO1}, HVCC UVLO is released.

D: When the EN pin voltage exceeds V_{EN1}, EN UVLO is released.
VCC ULVO and EN UVLO released, the LDO regulator for low side drive starts, and LVCC pin voltage starts to rise.

E: When the LVCC pin voltage exceeds V_{LUVLO1}, LVCC UVLO is released and the input signal to LIN pin becomes enabled.
Here, HVCC UVLO released, the condition that the input signal to HIN pin becomes enabled.

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Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +683	V	BST, HVCC, HMC pin voltage
Maximum Applied Voltage 2	V_{MAX2}	-5 to +650	V	SW pin voltage
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +33	V	VCC, EN, HIN, LIN pin voltage
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +33	V	BST pin voltage referred to SW
Maximum Applied Voltage 5	V_{MAX5}	-0.3 to +7	V	LVCC, LMC pin voltage
Maximum Applied Voltage 6	V_{MAX6}	-0.3 to +7	V	HVCC, HOUT, HMC pin voltage referred to SW
Maximum Applied Voltage 7	V_{MAX7}	-2.5 to +2.5	V	PGND pin voltage referred to GND
SW dv/dt	dv/dt	150	V/ns	V_{SW} = 0V to 400V
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %.

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 4)	2s2p (Note 5)	
SSOP-B20				
Junction to Ambient	θ_{JA}	115.4	57.3	°C/W
Junction to Top Characterization Parameter (Note 3)	Ψ_{JT}	10	8	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via (Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range 1	V_{CC}	9.3	15	25	V	VCC pin voltage
Power Supply Voltage Range 2	V_{BST}	8.0	15	25	V	BST pin voltage referred to SW
Input Voltage Range 1	V_{IN_H}	3.0	5	V_{CC}	V	HIN, LIN pin high voltage
Input Voltage Range 2	V_{IN_L}	-0.3	0	+0.3	V	HIN, LIN pin low voltage
SW Voltage Range	V_{SW}	-3.5	0	600	V	SW pin voltage
PGND Voltage Range	V_{PGND}	-1.5	0	+1.5	V	PGND pin voltage referred to GND
LVCC Load Current Range	I_{LVCC}	-	-	10	mA	
LVCC pin Output Capacitor Range	C_{LVCC}	0.22	-	1	μF	
HVCC Load Current Range	I_{HVCC}	-	-	10	mA	
HVCC pin Output Capacitor Range	C_{HVCC}	0.22	-	1	μF	
BST pin Output Capacitor Range	C_{BST}	TBD	-	-	μF	
Operating Temperature	Topr	-40	-	+125	°C	Surrounding temperature

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Electrical Characteristics

(Unless noted otherwise, V_{CC}=15V, V_{BST} = 15 V, Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VCC Blocks						
VCC Operating Current	I_{ON1}		1.0	1.5	mA	Operating at 500 kHz, duty = 50 %
VCC Quiescent Current	I_{ON2}	-	210	330	µA	V_{LIN} = V_{HIN} = 0 V
VCC Standby Current	I_{STB}	-	120	180	µA	V_{CC} = 9.3 V
VCC UVLO Release Voltage	V_{UVLO1}	8.0	8.6	9.2	V	At VCC pin voltage rising
VCC UVLO Detection Voltage	V_{UVLO2}	7.5	8.1	8.7	V	At VCC pin voltage dropping
VCC UVLO Hysteresis	V_{UVLO3}	-	0.5	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2}
EN Blocks						
EN UVLO Release Voltage	V_{EN1}	1.8	2.0	2.2	V	At EN pin voltage rising
EN UVLO Detection Voltage	V_{UVLO2}	1.3	1.5	1.7	V	At EN pin voltage dropping
EN UVLO Hysteresis	V_{UVLO3}	-	0.5	-	V	V_{EN3} = V_{EN1} - V_{EN2}
EN Leakage Current	I_{EN_LEAK}	-	2	4	µA	V_{EN} = 5 V
Input Blocks						
LIN, HIN pin ON Threshold Voltage	V_{IN_ON}	-	(2.2)	2.6	V	
LIN, HIN pin OFF Threshold Voltage	V_{IN_OFF}	0.9	(1.2)	-	V	
LIN, HIN pin Threshold Hysteresis	V_{IN_HYS}	-	1.0	-	V	
LIN, HIN pin Leakage Current	I_{IN_LEAK}	-	3.5	-	µA	V_{LIN}, V_{HIN} = 5 V
TSD Blocks						
TSD Temperature 1	T_{SD1}	(150)	(175)	(200)	°C	At temperature rising (Note 1)
TSD Temperature 2	T_{SD2}	-	(100)	-	°C	At temperature falling (Note 1)
TSD Hysteresis	T_{SD3}	-	(75)	-	°C	T_{SD3} = T_{SD1} - T_{SD2}
TSD Timer	t_{TSD}	50	100	150	µs	
LVCC Blocks						
LVCC Output Voltage	V_{LVCC}	5.50	5.75	6.00	V	
LVCC Maximum Output Current	I_{LVCC}	10	-	-	mA	
LVCC UVLO Release Voltage	V_{LUVLO1}	4.20	4.60	5.00	V	At LVCC pin voltage rising
LVCC UVLO Detection Voltage	V_{LUVLO2}	3.90	4.30	4.70	V	At LVCC pin voltage falling
LVCC UVLO Hysteresis	V_{LUVLO3}	-	0.30	-	V	V_{LUVLO3} = V_{LUVLO1} - V_{LUVLO2}
LVCC Internal Pull-down Resistance	R_{LVCC}	2.6	5.2	7.8	MΩ	EN = 0 V
HVCC Blocks						
HVCC Output Voltage	V_{HVCC}	5.50	5.75	6.00	V	
HVCC Maximum Output Current	I_{HVCC}	10	-	-	mA	
HVCC UVLO Release Voltage	V_{HUVLO1}	4.20	4.60	5.00	V	At HVCC pin voltage rising
HVCC UVLO Detection Voltage	V_{HUVLO2}	3.90	4.30	4.70	V	At HVCC pin voltage falling
HVCC UVLO Hysteresis	V_{HUVLO3}	-	0.30	-	V	V_{HUVLO3} = V_{HUVLO1} - V_{HUVLO2}
HVCC Internal Pull-down Resistance	R_{HVCC}	0.6	1.3	2.0	MΩ	EN = 0 V

(Note 1) No shipping inspection.

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Electrical Characteristics - continued

(Unless noted otherwise, V_{CC} = 15 V, V_{BST} = 15 V, Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BST Blocks						
BST Operating Current	I_{BSTON1}	-	0.8	1.2	mA	Operating at 500 kHz, duty = 50 %
BST Quiescent Current	I_{BSTON2}	-	120	180	μA	V_{HIN} = 0 V
BST UVLO Release Voltage	V_{BUVLO1}	6.70	7.30	7.90	V	At BST pin voltage rising
BST UVLO Detection Voltage	V_{BUVLO2}	6.40	7.00	7.60	V	At BST pin voltage falling
BST UVLO Hysteresis	V_{BUVLO2}	-	0.30	-	V	V_{BUVLO3} = V_{BUVLO1} – V_{BUVLO2}
Output Items						
LOUT, HOUT Source ON Resistance	R_{ONH}	-	1	2	Ω	I_{LOUT}, I_{HOUT} = 10mA
LOUT, HOUT Sink ON Resistance	R_{ONL}	-	0.65	1.30	Ω	I_{LOUT}, I_{HOUT} = 10mA
LOUT, HOUT Source Current	I_{SOURCE}	-	(2)	-	A	V_{LOUT}, V_{HOUT} = 0 V *(Note 1)*
LOUT, HOUT Sink Current	I_{SINK}	-	(2)	-	A	V_{LOUT}, V_{HOUT} = 5 V *(Note 1)*
Switching Items						
LOUT Turn-on Propagation Delay Time	t_{D_ONL}	-	50	75	ns	V_{CC}, V_{BST} = 12V to 25 V *(Note 2)*
		-	50	100	ns	V_{CC}, V_{BST} = 9.3V to 11V *(Note 2)*
LOUT Turn-off Propagation Delay Time	t_{D_OFFL}	-	50	75	ns	V_{CC}, V_{BST} = 12V to 25 V *(Note 2)*
		-	50	100	ns	V_{CC}, V_{BST} = 9.3V to 11V *(Note 2)*
HOUT Turn-on Propagation Delay Time	t_{D_ONH}	-	50	75	ns	V_{CC}, V_{BST} = 12V to 25 V *(Note 2)*
		-	50	100	ns	V_{CC}, V_{BST} = 9.3V to 11V *(Note 2)*
HOUT Turn-off Propagation Delay Time	t_{D_OFFH}	-	50	75	ns	V_{CC}, V_{BST} = 12V to 25 V *(Note 2)*
		-	50	100	ns	V_{CC}, V_{BST} = 9.3V to 11V *(Note 2)*
Low and High Side Delay Matching	t_{DMATCH}	-15	0	15	ns	V_{CC}, V_{BST} = 12V to 25 V *(Note 1)*
		-30	0	30	ns	V_{CC}, V_{BST} = 9.3V to 11 V *(Note 1)*
Turn-on Mask Time	t_{MASK}	35	65	100	ns	
LOUT Fall Time	t_{FL}	-	2.5	5 (TBD)	ns	C_{LOUT} = 1nF *(Note 1) (Note 2) (Note 3)*
LOUT Rise Time	t_{RL}	-	4.0	8 (TBD)	ns	C_{LOUT} = 1nF *(Note 1) (Note 2) (Note 3)*
High Side Fall Time	t_{FH}	-	2.5	5 (TBD)	ns	C_{LOUT} = 1nF, SW=PGND *(Note 1) (Note 2) (Note 3)*
High Side Rise Time	t_{RH}	-	4.0	8 (TBD)	ns	C_{LOUT} = 1nF, SW=PGND *(Note 1) (Note 2) (Note 3)*
Minimum Input Pulse width	t_{PW_MIN}	-	-	30	ns	V_{CC}, V_{BST} = 15 V *(Note 1)*
		-	-	40	ns	V_{CC}, V_{BST} = 9.3V to 25 V *(Note 1)*
Mirror Clamping Blocks						
Mirror Clamp Sink ON Resistance	R_{MC}	-	0.6	1.2	Ω	I_{LMC}, I_{HMC} = 10mA
Mirror Clamp Detect Voltage	V_{MC}	0.7	1.0	1.3	V	At LMC, HMC pin voltage falling
Mirror Clamp Delay Time	t_{D_MC}	-	-	30	ns	C_{LMC}, C_{HMC} = 1nF *(Note 1) (Note 3)*

(Note 1) No shipping inspection.
(Note 2) Refer to ‘Switching Parameter Measurement Information’.
(Note 3) Varies greatly depending on the conditions of the application.

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Switching Parameter Measurement Information

Figure 5 shows the circuit for measurements of switching parameters.
Figure 6 shows instruction of them.

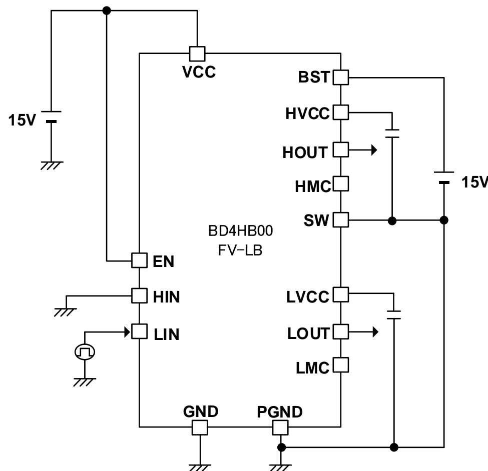

Figure 5. Switching Parameters Measurement Circuit

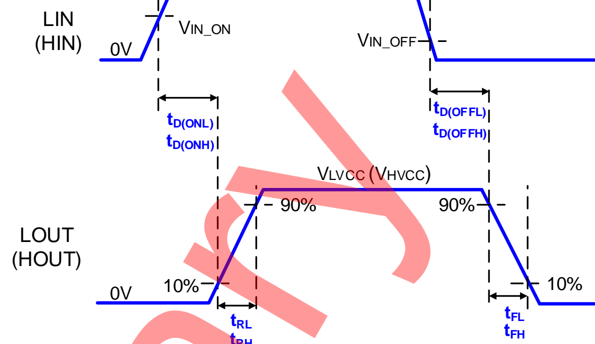

Figure 6. Instruction of Switching Parameters

1 LOUT / HOUT Turn-on Propagation Delay Time: $t_{D(ONL)}$ / $t_{D(ONH)}$

The turn-on delay time is the time from rising edge of the LIN/HIN pin voltage (LIN / HIN pin voltage is rising to V_{IN_ON}) to when the driver output starts turning on (LOUT / HOUT pin voltage is rising to 10%).

2 LOUT / HOUT Rise Time: t_{RL} / t_{RH}

The rise time is the time it takes for LOOUT / HOUT pin voltage rises from V_{LVCC}/V_{HVCC} x 10% to V_{LVCC}/V_{HVCC} x 90%.

3 LOUT / HOUT Turn-off Propagation Delay: $t_{D(OFFL)}$ / $t_{D(OFFH)}$

The turn-off delay time is the time from falling edge of the LIN / HIN pin voltage (LIN / HIN pin voltage is falling to V_{IN_OFF}) to when the driver starts turning off (LOUT / HOUT pin voltage is falling to V_{LVCC} / V_{HVCC} x 90%).

4 LOUT / HOUT Fall Time: t_{FL} / t_{FH}

The fall time is the time it takes for LOUT / HOUT pin voltage falls from V_{LVCC} / V_{HVCC} x 90% to V_{LVCC} / V_{HVCC} x 10%.

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Typical Performance Curves
(Reference Data)

T.B.D.

I/O Equivalence Circuit

T.B.D.

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Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

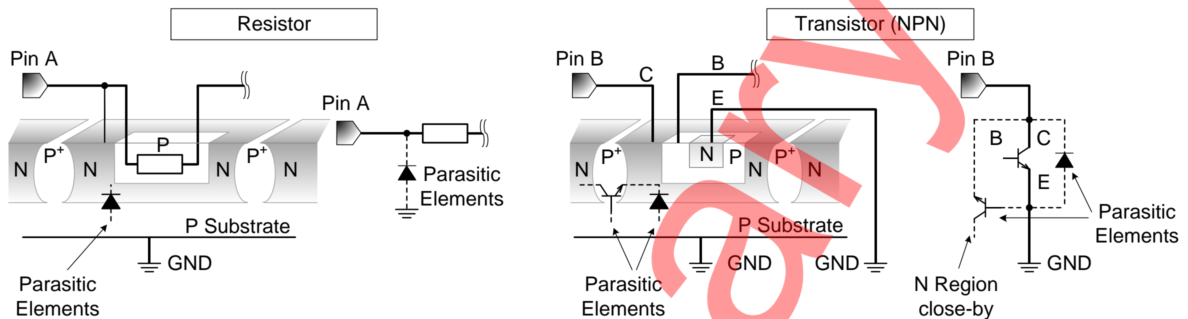

Figure 7 Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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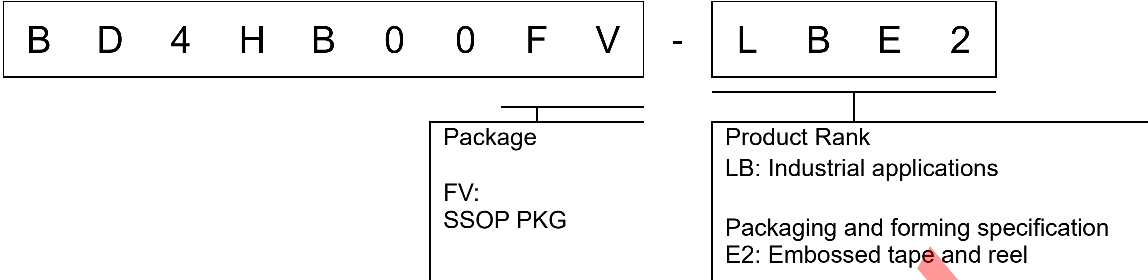
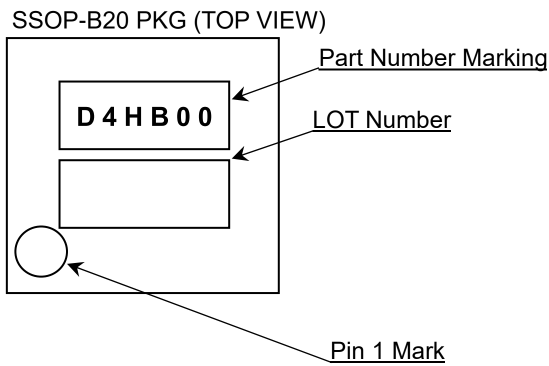
Ordering Information



Marking Diagram



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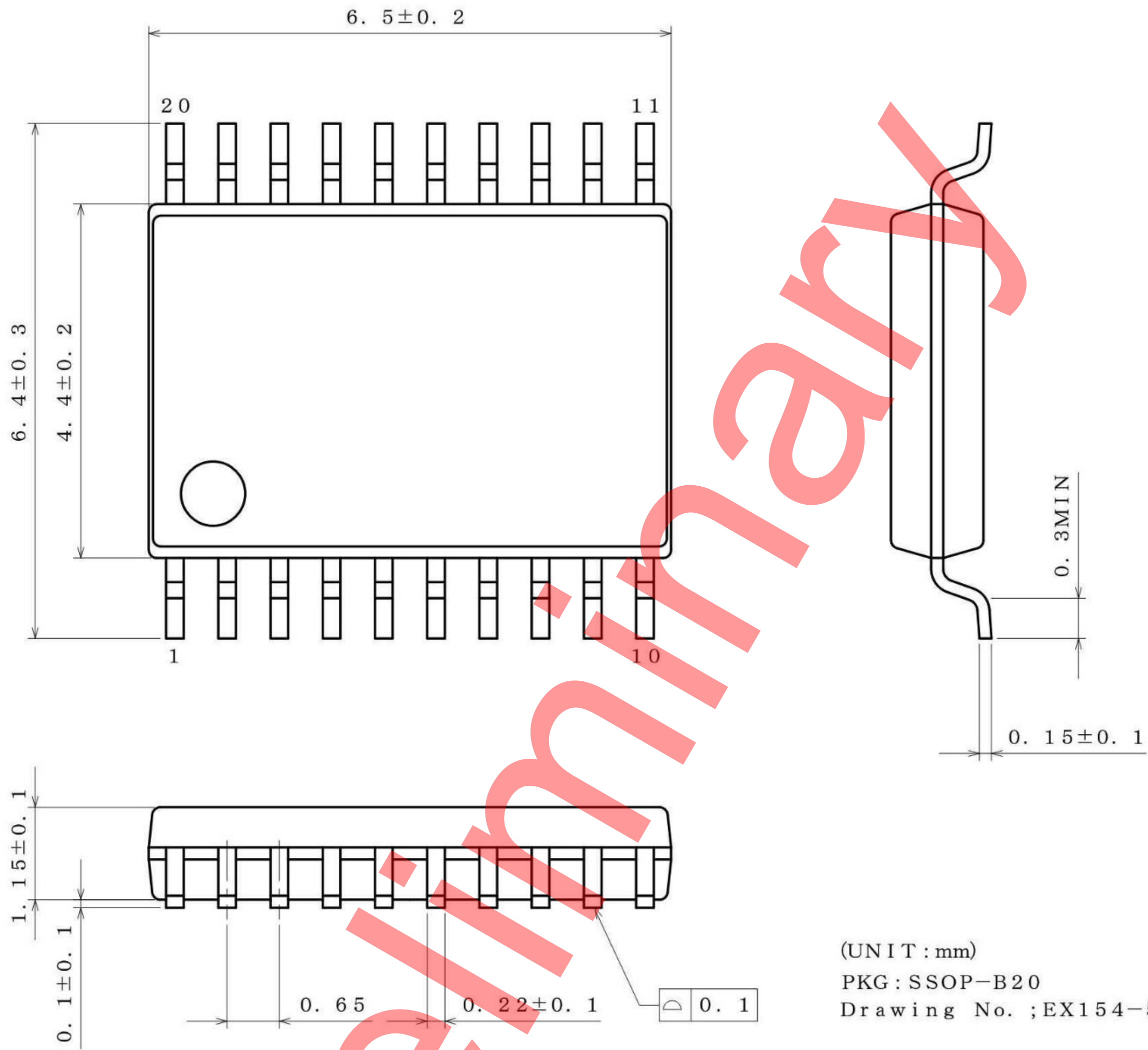
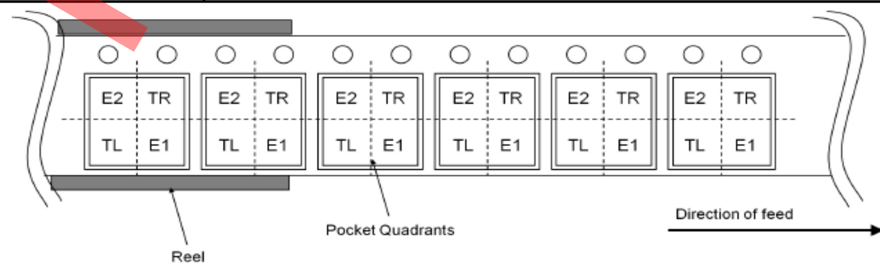
Physical Dimension and Packing Information

Package Name	SSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
28.May.2024	000	New Release (Temporary version)

Preliminary

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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