Datasheet

Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 2500 Vrms
1ch Gate Driver Providing Galvanic Isolation

BM6117FU-C

General Description

The BM6117FU-C is a gate driver with an isolation voltage of 2500 Vrms. It has an I/O delay time of 450 ns, minimum input pulse width of 400 ns, and incorporates the fault signal output function, under voltage lockout (UVLO) function, short circuit protection (SCP) function, active miller clamping function, temperature monitoring function, gate constant current driving function and output state feedback function.

Key Specifications

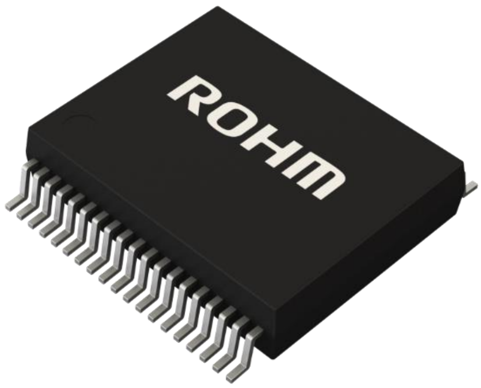
■ Isolation Voltage:	2500 Vrms
■ Maximum Gate Drive Voltage:	24 V
■ I/O Delay Time:	450 ns (Max)
■ Minimum Input Pulse Width:	400 ns

Package	W (Typ) x D (Typ) x H (Max)
SSOP-C38W	10.0 mm x 10.4 mm x 2.4 mm

Features

- AEC-Q100 Qualified(Note 1)
- Fault Signal Output Function
- Under Voltage Lockout Function
- Short Circuit Protection Function
- Fast Turn Off Function for Short Circuit Protection
- Soft Turn Off Function for Short Circuit Protection (Adjustable turn off time)
- Active Miller Clamping Function
- Temperature Monitoring Function
- Gate Constant Current Driving Function
- Output State Feedback Function

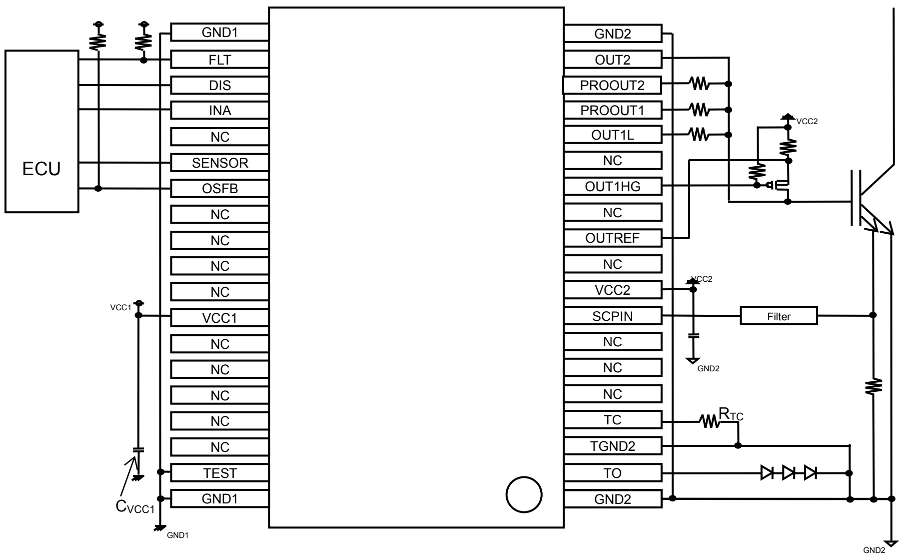
(Note 1) Grade1



Applications

- Automotive Inverter System
- Automotive DCDC Converter
- Industrial Inverter System
- UPS System

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

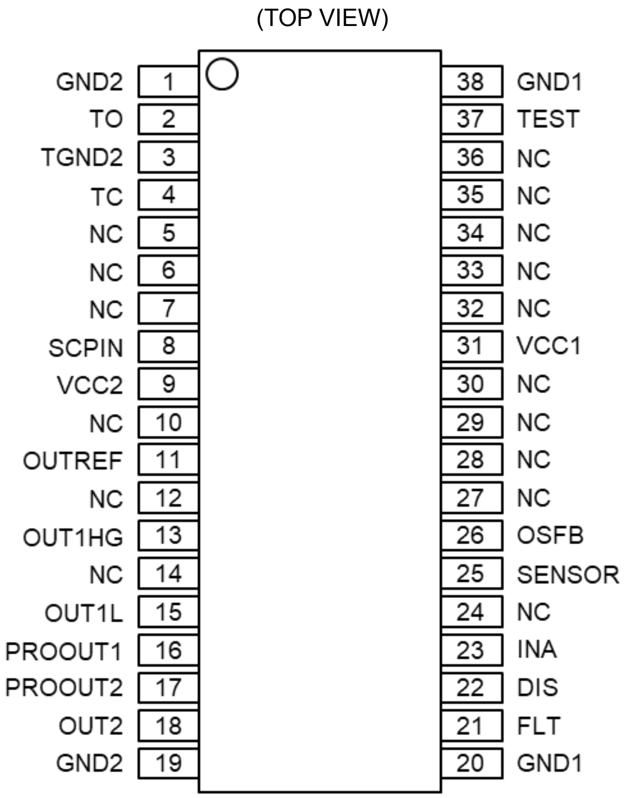
Contents

Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
TC (As Temperature Monitor)	R_{TC}	1.25	-	50	kΩ
TC (No Temperature Monitor)	R_{TC}	0.1	1	10	MΩ
VCC1	C_{VCC1}	0.3	-	-	μF
VCC2	C_{VCC2}	0.4	-	-	μF

C_{VCC1} : For supplying driving internal transformer.
C_{VCC2} : For supplying gate charge current of MOS FET/IGBT and driving internal transformer.

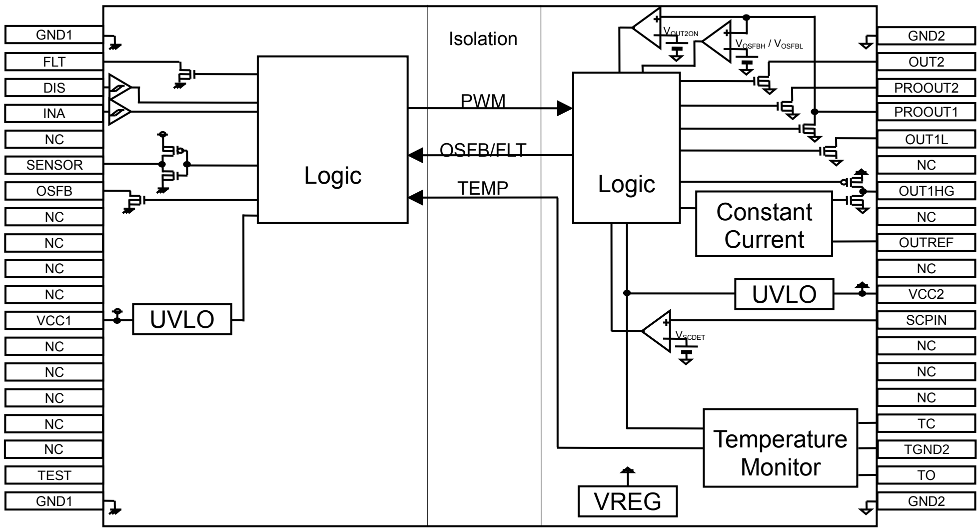
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	GND2	Output side ground pin
2	TO	Constant current output pin / Sensor voltage input pin
3	TGND2	Ground pin for temperature sensor
4	TC	Resistor connection pin for setting constant current source output
5	NC	Non connection
6	NC	Non connection
7	NC	Non connection
8	SCPIN	Short circuit detection pin
9	VCC2	Output side power supply pin
10	NC	Non connection
11	OUTREF	Reference voltage pin for constant current driving
12	NC	Non connection
13	OUT1HG	Source side MOS buffer driving pin
14	NC	Non connection
15	OUT1L	Sink side output pin
16	PROOUT1	Soft turn off pin for short circuit protection / Gate voltage input pin
17	PROOUT2	Fast turn off pin for short circuit protection
18	OUT2	Output pin for Miller Clamp
19	GND2	Output side ground pin
20	GND1	Input side ground pin
21	FLT	Fault output pin
22	DIS	Input enabling signal input pin
23	INA	Control input pin
24	NC	Non connection
25	SENSOR	Temperature information output pin
26	OSFB	Output state feedback output pin
27	NC	Non connection
28	NC	Non connection
29	NC	Non connection
30	NC	Non connection
31	VCC1	Input side power supply pin
32	NC	Non connection
33	NC	Non connection
34	NC	Non connection
35	NC	Non connection
36	NC	Non connection
37	TEST	Test mode setting pin
38	GND1	Input side ground pin

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input side Supply Voltage	V_{CC1MAX}	-0.3 to +7.0 (Note 2)	V
Output side Supply Voltage	V_{CC2MAX}	-0.3 to +30.0 (Note 3)	V
TGND2 Pin Input Voltage	V_{TGND2}	-0.3 to +0.3 (Note 3)	V
INA, DIS Pin Input Voltage	V_{INMAX}	-0.3 to +7.0 (Note 2)	V
FLT, OSFB Pin Input Voltage	V_{FLTMAX}	-0.3 to +7.0 (Note 2)	V
FLT, OSFB Pin Output Current	I_{FLT}	10	mA
SENSOR Pin Output Current	I_{SENSOR}	10	mA
SCPIN Pin Input Voltage	$V_{SCPINMAX}$	-0.3 to +VCC2 + 0.3 (Note 3)	V
TO Pin Input Voltage	V_{TOMAX}	-0.3 to +VCC2 + 0.3 (Note 3)	V
TO Pin Output Current	I_{TOMAX}	8	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 2) Relative to GND1
(Note 3) Relative to GND2

Thermal Resistance (Note 4)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 6)	2s2p (Note 7)	
SSOP-C38W				
Junction to Ambient	θ_{JA}	84.5	50.1	°C/W
Junction to Top Characterization Parameter (Note 5)	Ψ_{JT}	28	22	°C/W

(Note 4) Based on JESD51-2A (Still-Air).
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.
(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input side Supply Voltage	V_{CC1} (Note 8)	4.5	5.5	V
Output side Supply Voltage	V_{CC2} (Note 9)	V_{UVLO2L}	24	V
TO Pin Input Voltage	V_{TO} (Note 10)	1.35	3.84	V
Operating Temperature	Topr	-40	+125	°C

(Note 8) Relative to GND1
(Note 9) Relative to GND2
(Note 10) Relative to TGND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO} = 500 V)	R_S	> 10^9	Ω
Insulation Withstand Voltage (1 min)	V_{ISO}	2500	Vrms
Insulation Test Voltage (1 s)	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = V_{UVLO2L} to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input side Supply Circuit Current 1	I_{CC11}	0.2	0.6	1.1	mA	INA, DIS not switching
Input side Supply Circuit Current 2	I_{CC12}	0.3	0.7	1.2	mA	INA = 10 kHz, Duty 50 % DIS = L
Input side Supply Circuit Current 3	I_{CC13}	0.3	0.8	1.4	mA	INA = 20 kHz, Duty 50 % DIS = L
Output side Supply Circuit Current	I_{CC2}	1.5	3.1	4.8	mA	R_{TC} = 10 kΩ
Logic Block						
Logic High Level Input Voltage	V_{INH}	0.7 x V_{CC1}	-	5.5	V	INA, DIS
Logic Low Level Input Voltage	V_{INL}	0	-	0.3 x V_{CC1}	V	INA, DIS
Logic Pull-Down Resistance	R_{IND}	25	50	100	kΩ	INA
Logic Pull-Up Resistance	R_{INU}	25	50	100	kΩ	DIS
Logic Input Filtering Time	t_{INFIL}	80	130	180	ns	INA, DIS

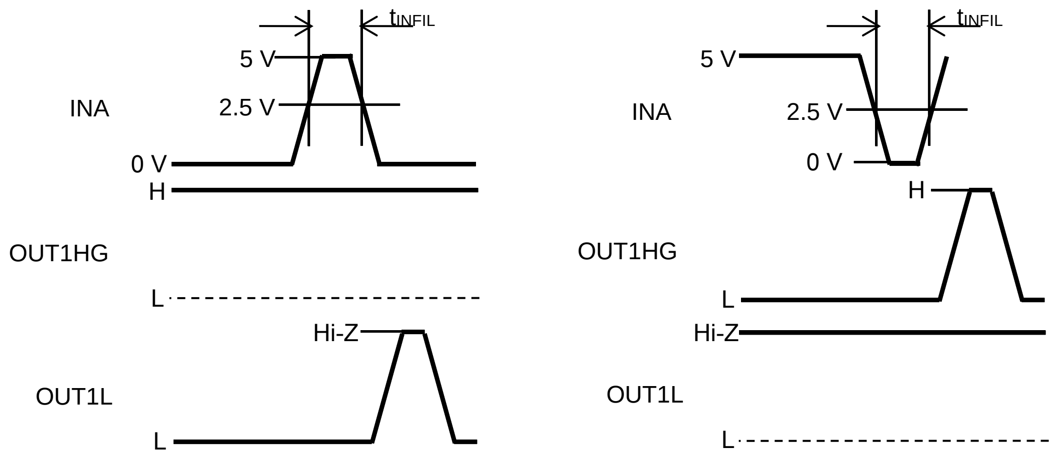
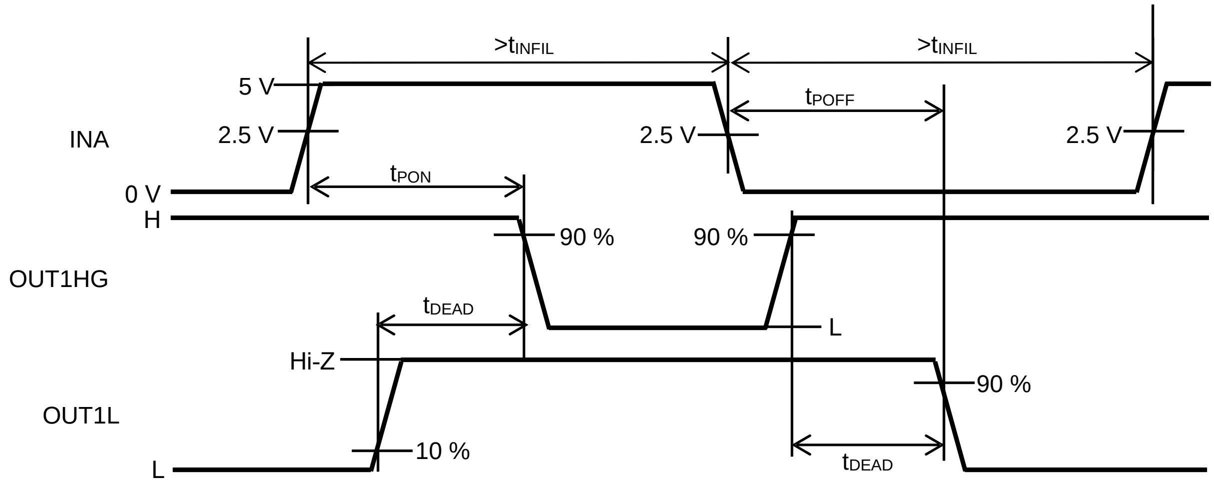


Figure 1. Logic Input Timing Chart

Electrical Characteristics - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output						
OUT1HG H Level Output Voltage	$V_{OUT1HGH}$	-	-	0.8	V	I_{OUT1HG} = -40 mA Relative to VCC2 (Absolute Value)
OUT1HG L Level Output Voltage	$V_{OUT1HGL}$	-	-	0.6	V	I_{OUT1HG} = +40 mA
OUTREF Reference Voltage	V_{OUTREF}	1.96	2.00	2.04	V	Relative to VCC2 (Absolute Value)
OUT1L On Resistance	R_{OUT1L}	-	0.26	0.52	Ω	I_{OUT1L} = 40 mA
OUT1L Maximum Current	$I_{OUTMAX1}$	10	-	-	A	V_{CC2} = 15 V, Guaranteed by design
OUT1 Turn On Time	t_{PON}	210	330	450	ns	INA, DIS
OUT1 Turn Off Time	t_{POFF}	210	330	450	ns	INA, DIS
OUT1HG - OUT1L Dead Time	t_{DEAD}	90	160	230	ns	
OUT1HG L to H Transition Time	$t_{OUT1HGLH}$	-	25	50	ns	Between OUT1HG and VCC2 = 1000 pF Guaranteed by design
PROOUT1 On Resistance	R_{ONPRO1}	-	0.8	1.8	Ω	$I_{PROOUT1}$ = 40 mA
PROOUT2 On Resistance	R_{ONPRO2}	-	0.4	0.9	Ω	$I_{PROOUT2}$ = 40 mA
OUT2 On Resistance	R_{ON2}	-	0.4	0.9	Ω	I_{OUT2} = 40 mA
OUT2 On Threshold Voltage	V_{OUT2ON}	1.8	2.0	2.2	V	
OUT2 On Delay Time	t_{OUT2ON}	-	50	80	ns	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design



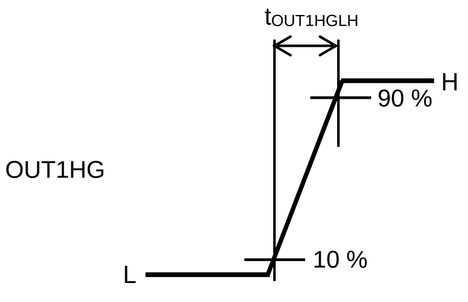


Figure 2. OUT1HG, OUT1L Output Timing Chart

Electrical Characteristics - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Temperature Monitor						
TC Voltage	V_{TC}	0.980	1.000	1.020	V	
TO Output Current	I_{TO}	0.975	1.000	1.025	mA	R_{TC} = 10 kΩ
SENSOR Output Frequency	f_{OSC_TO}	8	10	14	kHz	
SENSOR Output Duty1	$D_{SENSOR1}$	87.5	90.0	92.5	%	V_{TO} = 1.35 V
SENSOR Output Duty2	$D_{SENSOR2}$	47.0	50.0	53.0	%	V_{TO} = 2.59 V
SENSOR Output Duty3	$D_{SENSOR3}$	5.6	10.0	14.4	%	V_{TO} = 3.84 V
SENSOR On Resistance (Source side)	$R_{SENSORH}$	-	60	160	Ω	I_{SENSOR} = -5 mA
SENSOR On Resistance (Sink side)	$R_{SENSORL}$	-	60	160	Ω	I_{SENSOR} = +5 mA
Protection Functions						
Input side UVLO Off Threshold Voltage	V_{UVLO1H}	4.05	4.25	4.45	V	
Input side UVLO On Threshold Voltage	V_{UVLO1L}	3.95	4.15	4.35	V	
Input side UVLO Filtering Time	$t_{UVLO1FIL}$	2	10	30	μs	
Input side UVLO Delay Time (OUT1HG)	$t_{DUVLO1OUT1HG}$	2	10	30	μs	
Input side UVLO Delay Time (FLT)	$t_{DUVLO1FLT}$	2	10	30	μs	
Output side UVLO Off Threshold Voltage	V_{UVLO2H}	10.7	11.7	12.7	V	
Output side UVLO On Threshold Voltage	V_{UVLO2L}	9.7	10.7	11.7	V	
Output side UVLO Filtering Time	$t_{UVLO2FIL}$	2	10	30	μs	
Output side UVLO Delay Time (OUT1HG)	$t_{DUVLO2OUT1HG}$	2	10	30	μs	
Output side UVLO Delay Time (FLT)	$t_{DUVLO2FLT}$	3	-	65	μs	
Short Current Detection Voltage	V_{SCDET}	0.67	0.70	0.73	V	
Short Current Detection Delay Time (OUT1HG)	$t_{DSCPOUT1HG}$	0.02	0.07	0.11	μs	OUT1HG = 1 kΩ Pull up
Short Current Detection Delay Time (PROOUT1)	$t_{DSCPPRO1}$	0.02	0.05	0.08	μs	PROOUT1 = 30 kΩ Pull up
Short Current Detection Delay Time (PROOUT2)	$t_{DSCPPRO2}$	0.02	0.05	0.08	μs	PROOUT2 = 30 kΩ Pull up
Short Current Detection Delay Time (FLT)	$t_{DSCPFLT}$	1	-	35	μs	
PROOUT2 On Time	t_{PRO2ON}	90	160	230	ns	
Soft Turn Off Release Time	t_{SCPOFF}	30	-	110	μs	OUT1L = 30 kΩ Pull up
FLT Output On Resistance	R_{FLTL}	-	30	80	Ω	I_{FLT} = 5 mA
Fault Output Holding Time	t_{FLTRLS}	20	35	50	ms	
Gate State H Detection Threshold Voltage	V_{OSFBH}	4.5	5.0	5.5	V	
Gate State L Detection Threshold Voltage	V_{OSFBL}	4.0	4.5	5.0	V	
OSFB Output Filtering Time	$t_{OSFBFIL}$	5.0	7.4	9.8	μs	
OSFB Output On Resistance	R_{OSFBL}	-	30	80	Ω	I_{OSFB} = 5 mA
OSFB Output Holding Time	$t_{OSFBRLS}$	20	35	50	ms	

Typical Performance Curves
(Reference data)

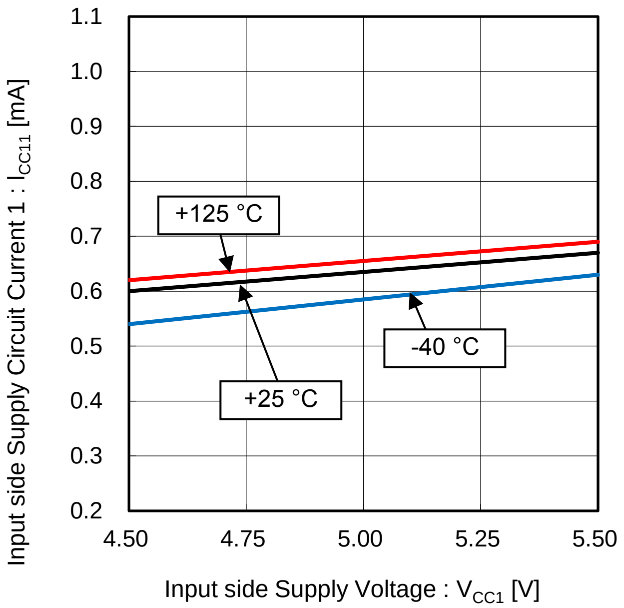


Figure 3. Input side Supply Circuit Current 1 vs Input side Supply Voltage
(INA not switching)

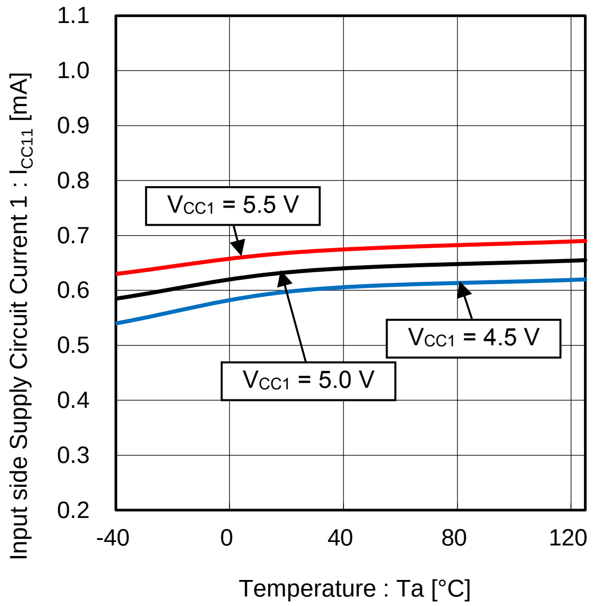


Figure 4. Input side Supply Circuit Current 1 vs Temperature
(INA not switching)

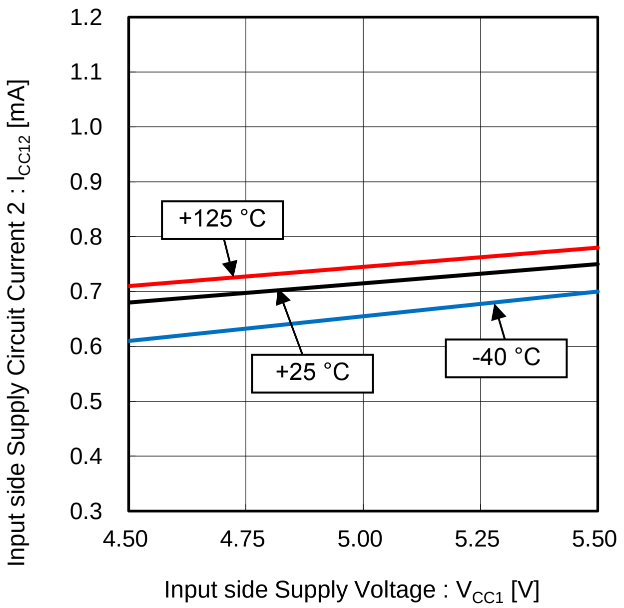


Figure 5. Input side Supply Circuit Current 2 vs Input side Supply Voltage
(INA = 10 kHz, Duty = 50 %)

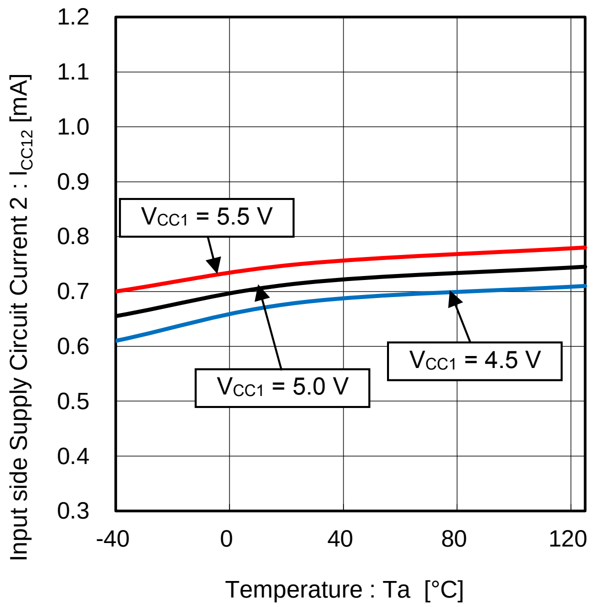


Figure 6. Input side Supply Circuit Current 2 vs Temperature
(INA = 10 kHz, Duty = 50 %)

Typical Performance Curves - continued

(Reference data)

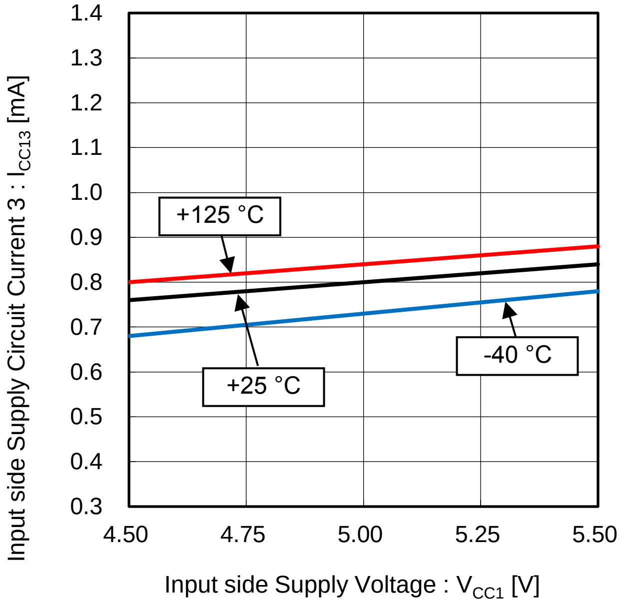


Figure 7. Input side Supply Circuit Current 3 vs Input side Supply Voltage (INA = 20 kHz, Duty = 50 %)

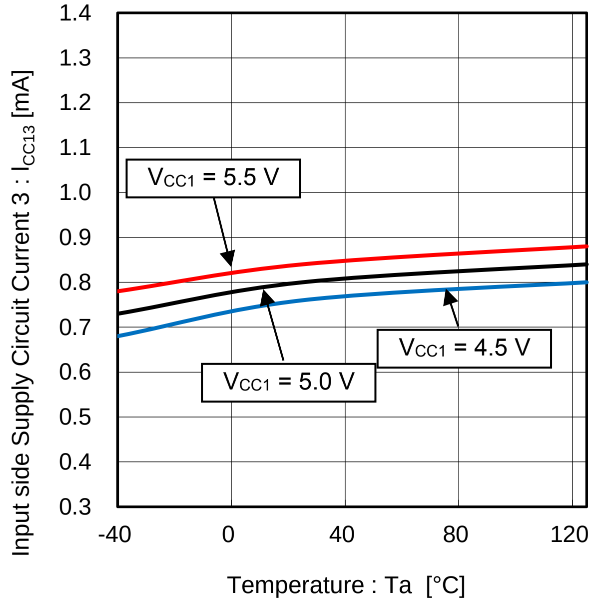


Figure 8. Input side Supply Circuit Current 3 vs Temperature (INA = 20 kHz, Duty = 50 %)

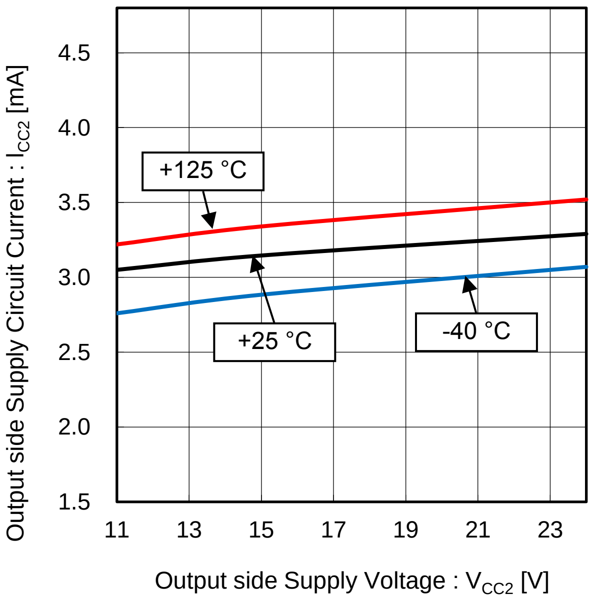


Figure 9. Output side Supply Circuit Current vs Output side Supply Voltage (R_{TC} = 10 kΩ)

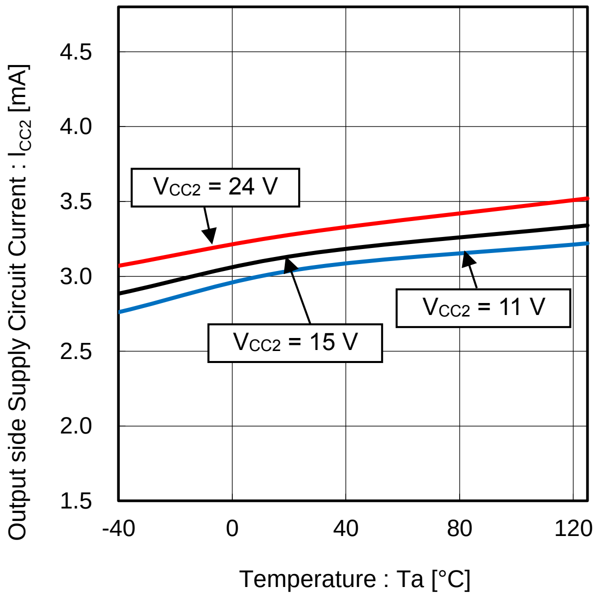


Figure 10. Output side Supply Circuit Current vs Temperature (R_{TC} = 10 kΩ)

Typical Performance Curves - continued
(Reference data)

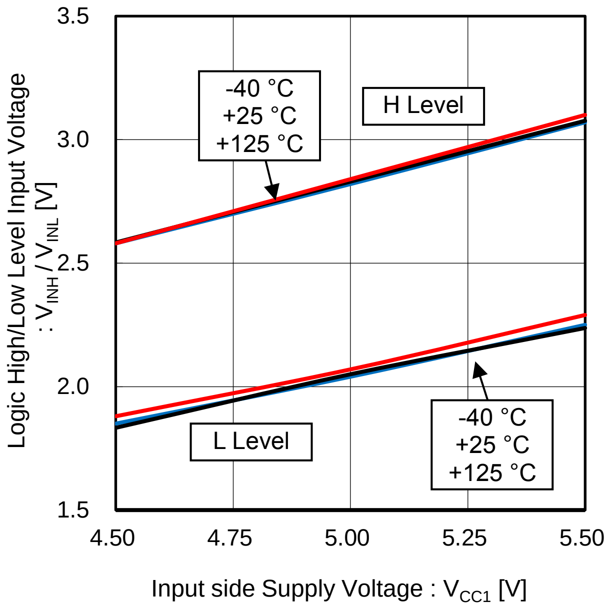


Figure 11. Logic High/Low Level Input Voltage vs Input side Supply Voltage

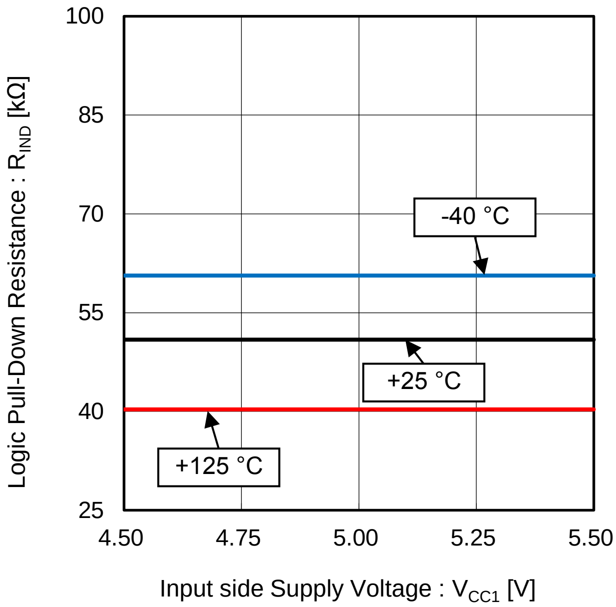


Figure 12. Logic Pull-Down Resistance vs Input side Supply Voltage

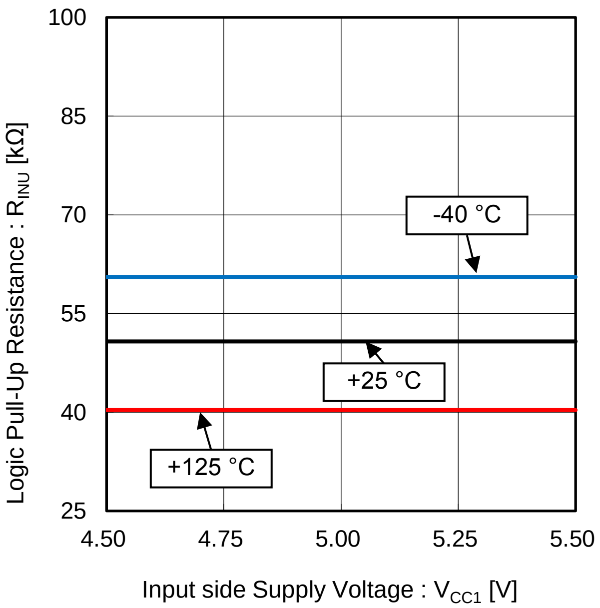


Figure 13. Logic Pull-Up Resistance vs Input side Supply Voltage

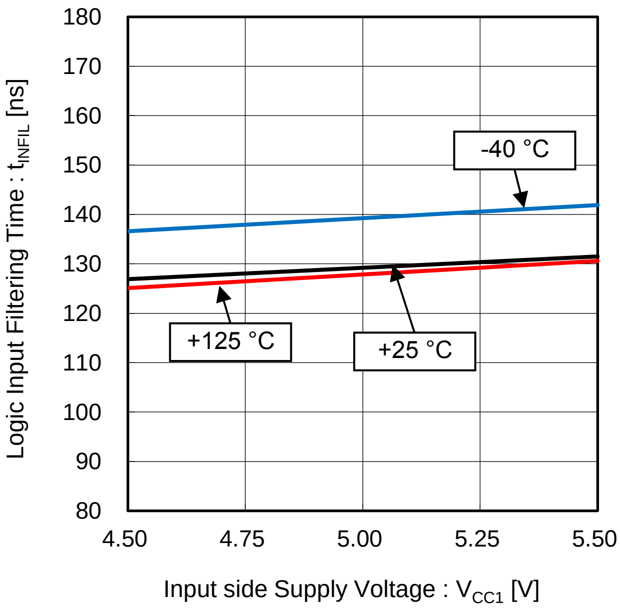


Figure 14. Logic Input Filtering Time vs Input side Supply Voltage

Typical Performance Curves - continued
(Reference data)

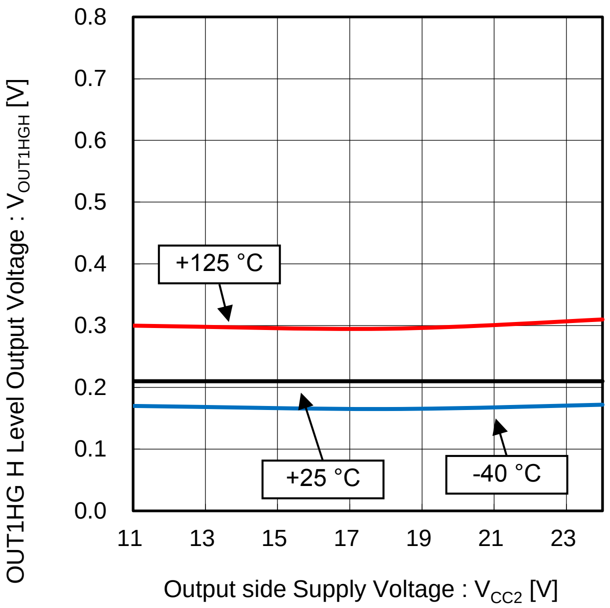


Figure 15. OUT1HG H Level Output Voltage vs Output side Supply Voltage (I_{OUT1HG} = -40 mA)

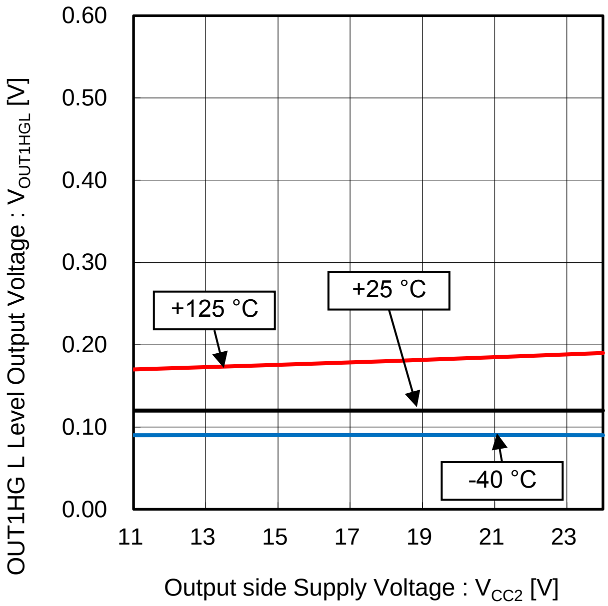


Figure 16. OUT1HG L Level Output Voltage vs Output side Supply Voltage (I_{OUT1HG} = +40 mA)

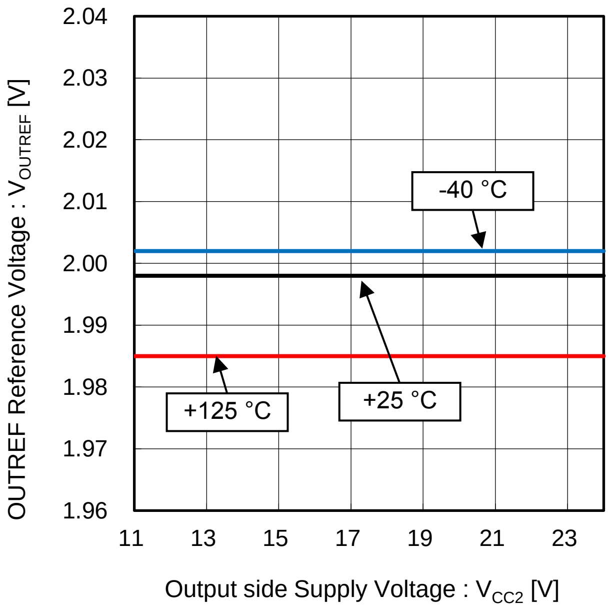


Figure 17. OUTREF Reference Voltage vs Output side Supply Voltage (Relative to VCC2)

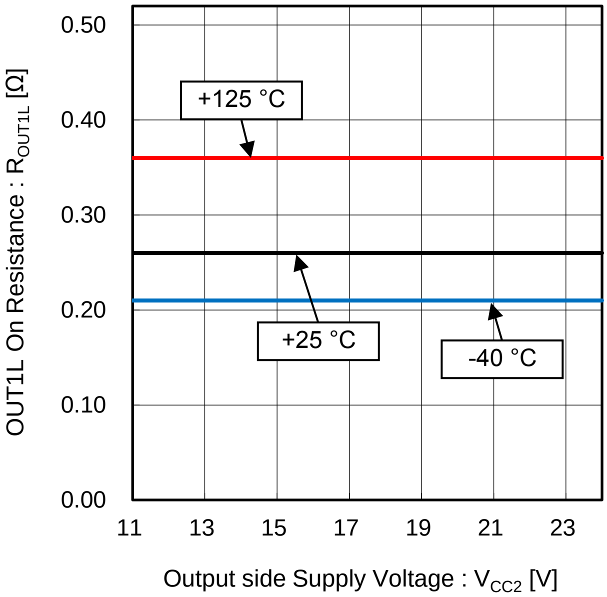


Figure 18. OUT1L On Resistance vs Output side Supply Voltage (I_{OUT1L} = 40 mA)

Typical Performance Curves - continued
(Reference data)

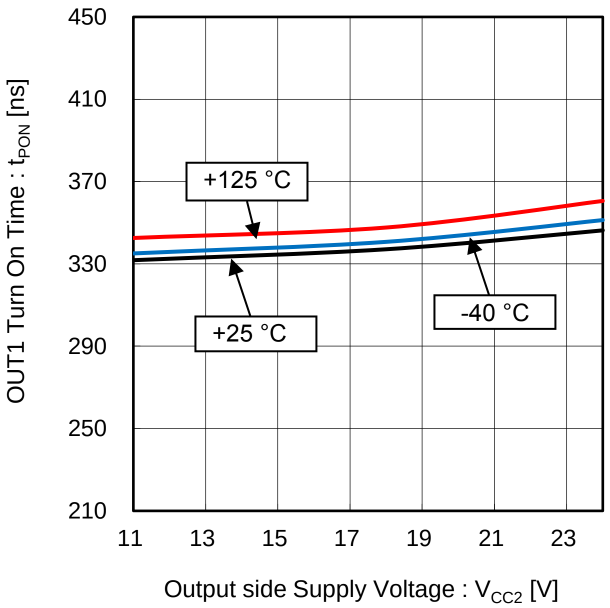


Figure 19. OUT1 Turn On Time vs Output side Supply Voltage

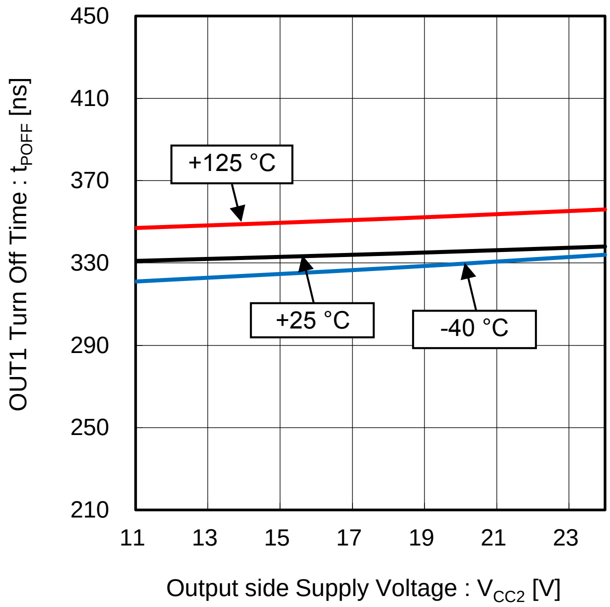


Figure 20. OUT1 Turn Off Time vs Output side Supply Voltage

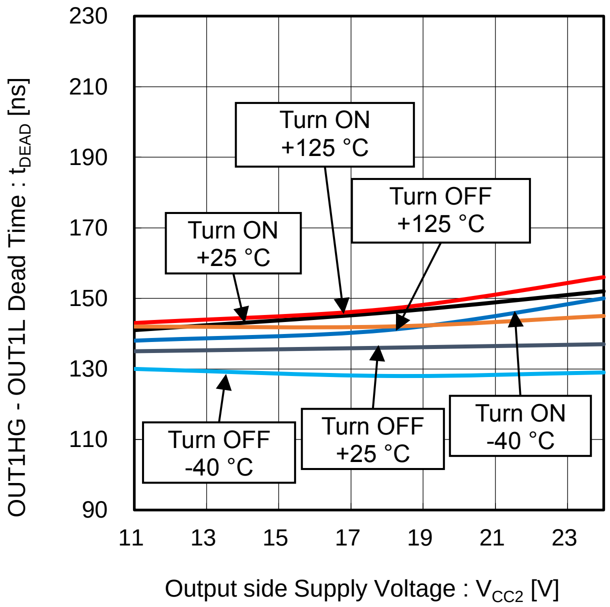


Figure 21. OUT1HG - OUT1L Dead Time vs Output side Supply Voltage

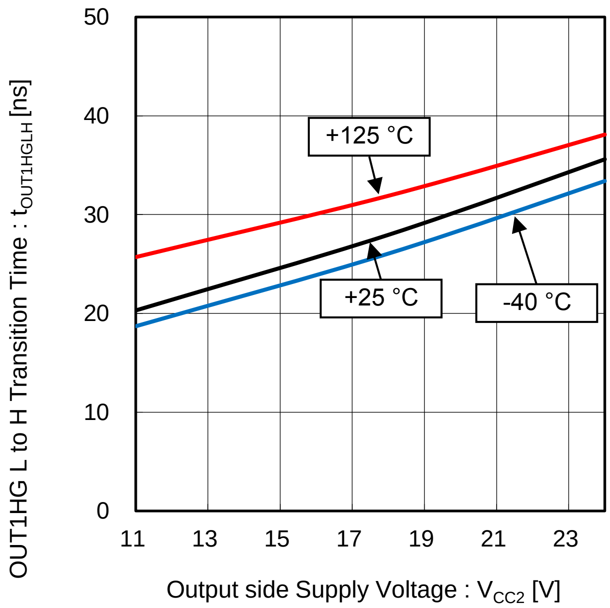


Figure 22. OUT1HG L to H Transition Time vs Output side Supply Voltage (OUT1HG-VCC2 1000 pF)

Typical Performance Curves - continued
(Reference data)

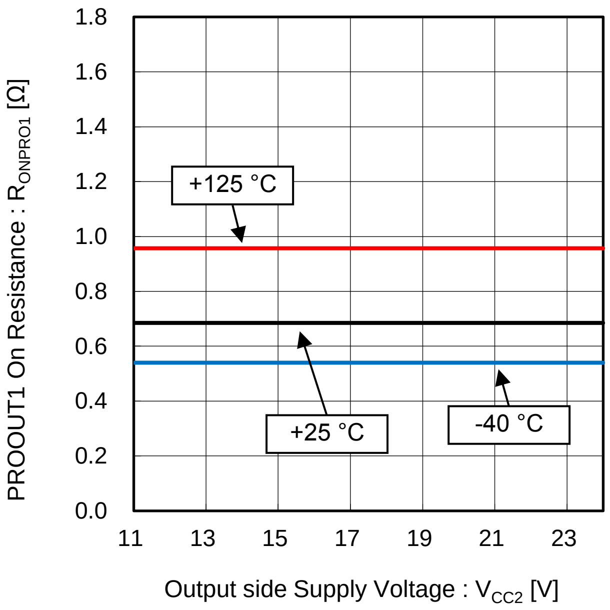


Figure 23. PROOUT1 On Resistance vs Output side Supply Voltage
($I_{PROOUT1}$ = 40 mA)

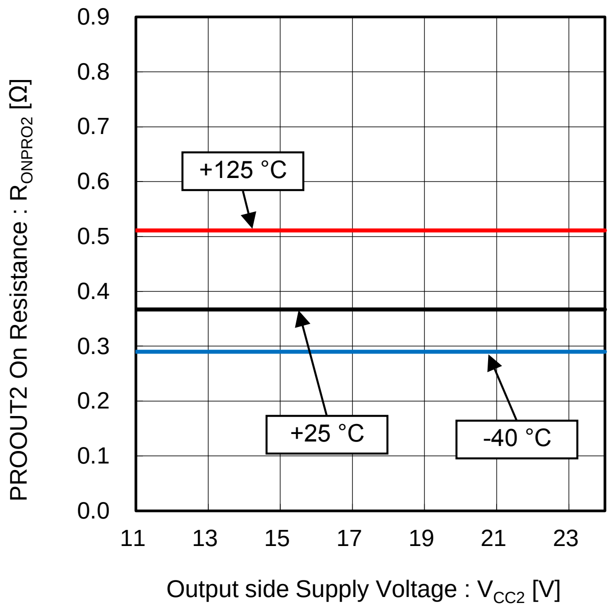


Figure 24. PROOUT2 On Resistance vs Output side Supply Voltage
($I_{PROOUT2}$ = 40 mA)

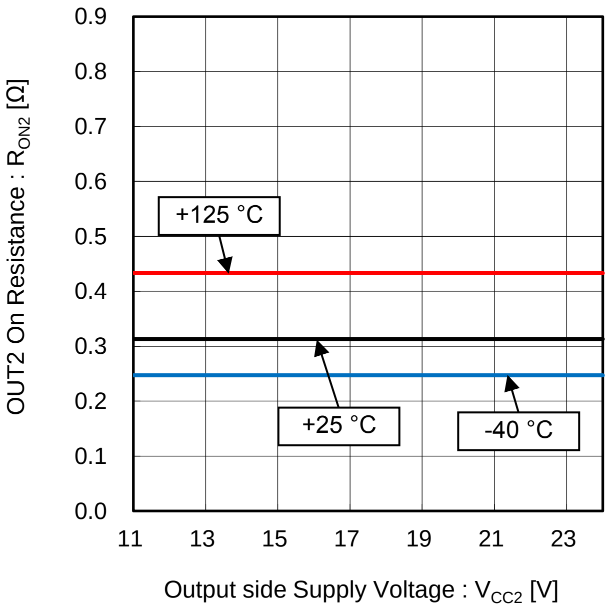


Figure 25. OUT2 On Resistance vs Output side Supply Voltage
(I_{OUT2} = 40 mA)

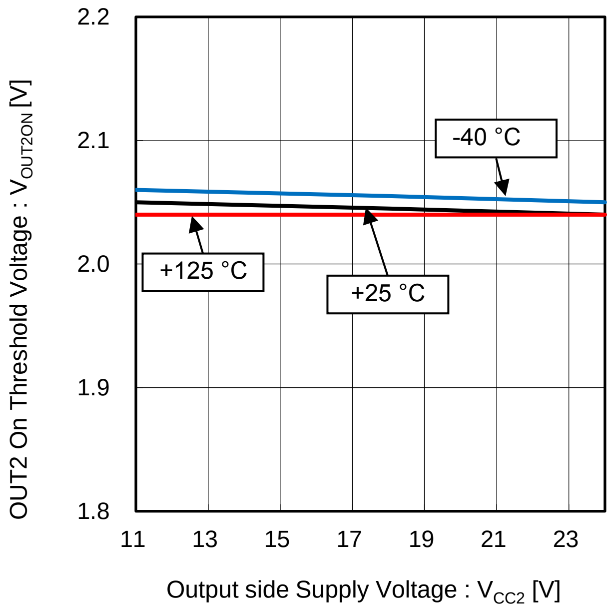


Figure 26. OUT2 On Threshold Voltage vs Output side Supply Voltage

Typical Performance Curves - continued
(Reference data)

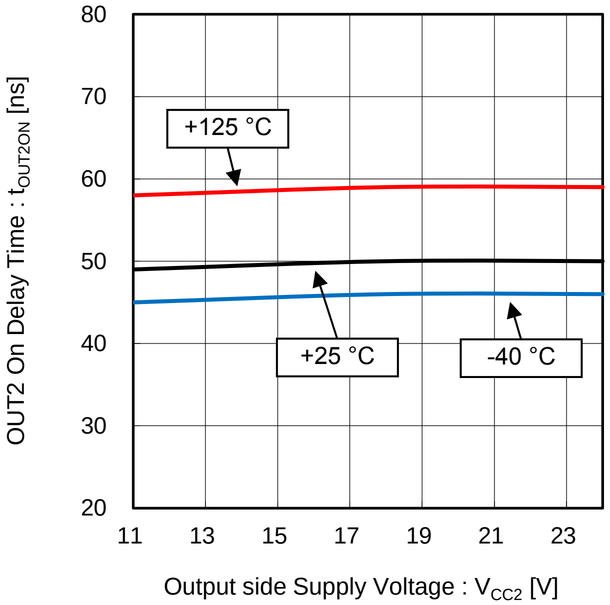


Figure 27. OUT2 On Delay Time vs Output side Supply Voltage

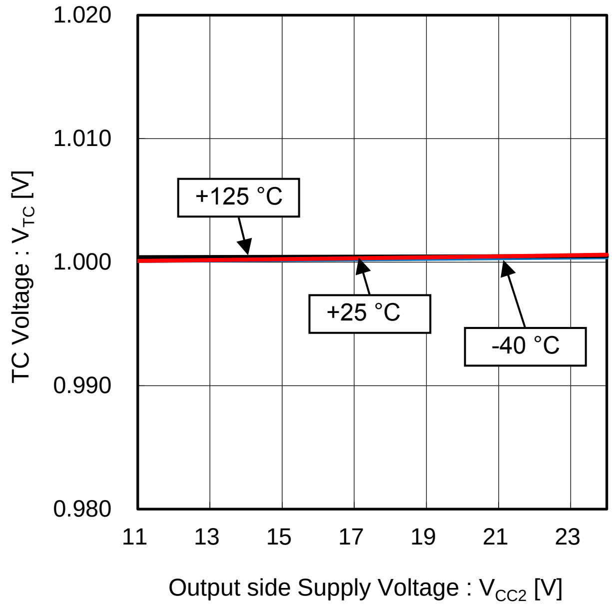


Figure 28. TC Voltage vs Output side Supply Voltage

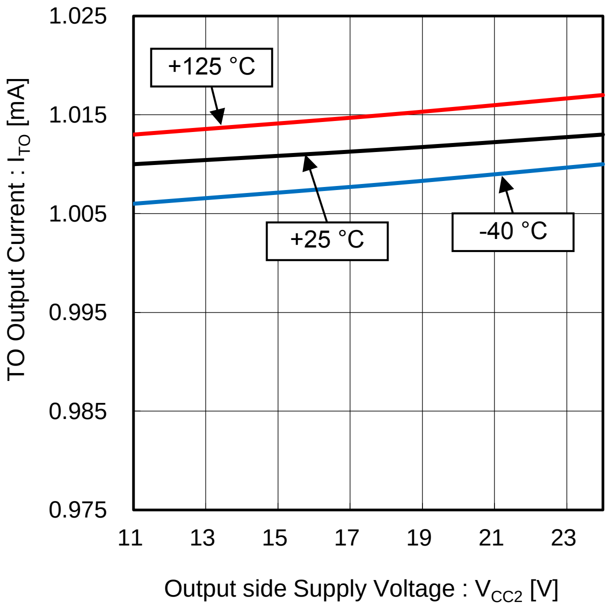


Figure 29. TO Output Current vs Output side Supply Voltage
(R_{TC} = 10 kΩ)

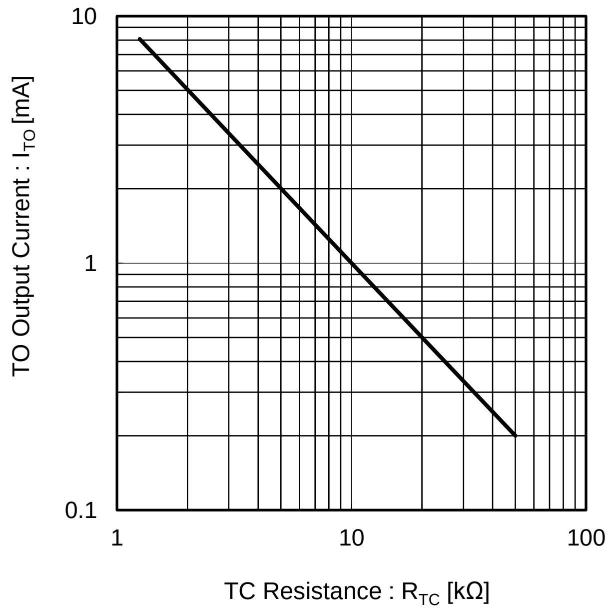


Figure 30. TO Output Current vs TC Resistance

Typical Performance Curves - continued

(Reference data)

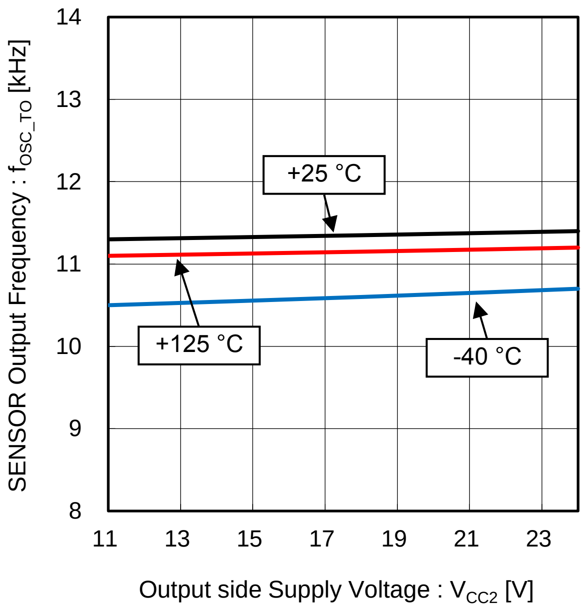


Figure 31. SENSOR Output Frequency vs Output side Supply Voltage

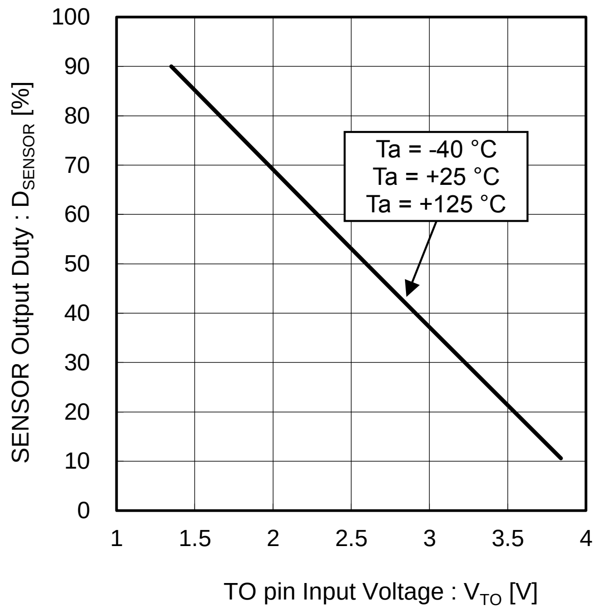


Figure 32. SENSOR Output Duty vs TO pin Input Voltage

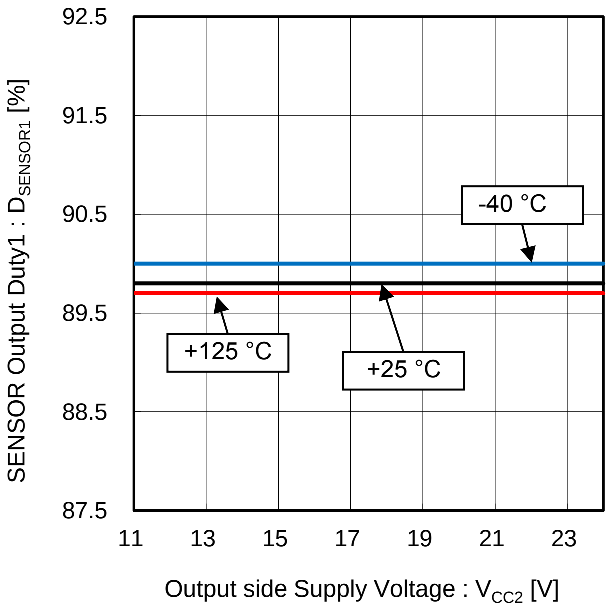


Figure 33. SENSOR Output Duty1 vs Output side Supply Voltage (V_{TO} = 1.35 V)

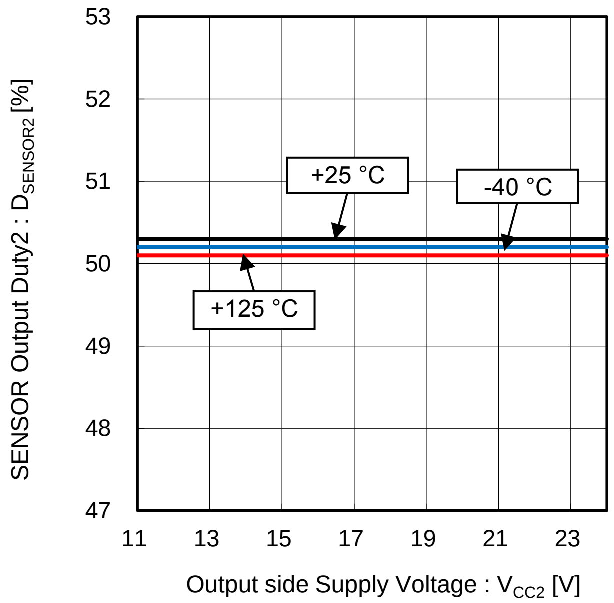


Figure 34. SENSOR Output Duty2 vs Output side Supply Voltage (V_{TO} = 2.59 V)

Typical Performance Curves - continued

(Reference data)

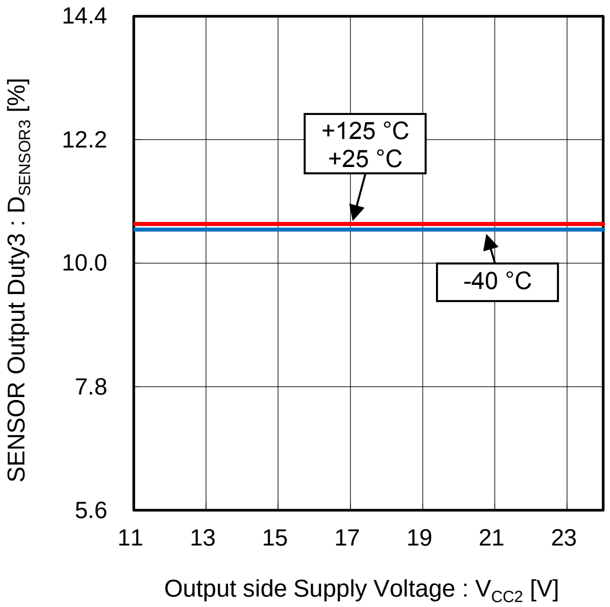


Figure 35. SENSOR Output Duty3 vs Output side Supply Voltage
(V_{TO} = 3.84 V)

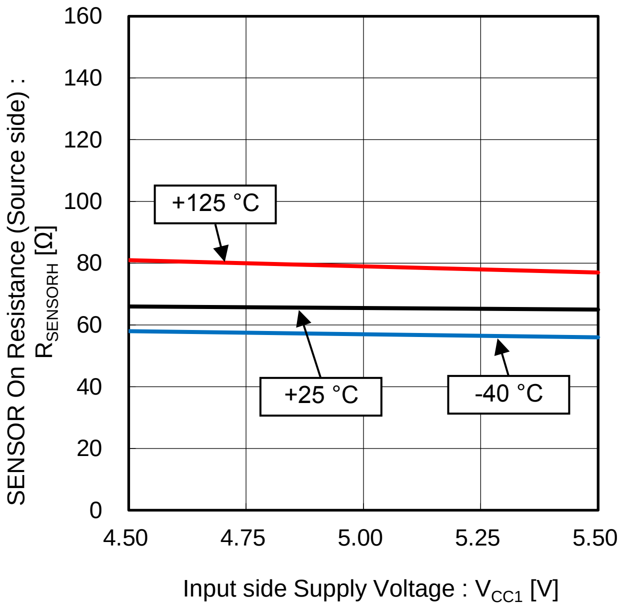


Figure 36. SENSOR On Resistance (Source side) vs Input side Supply Voltage
(I_{SENSOR} = -5 mA)

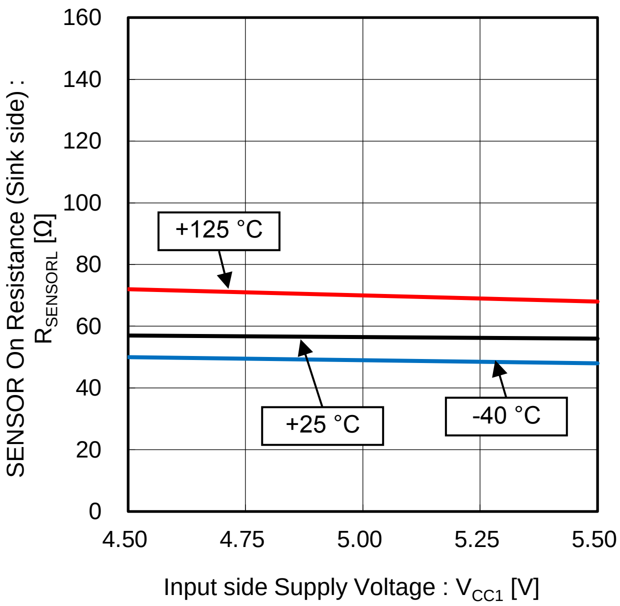


Figure 37. SENSOR On Resistance (Sink side) vs Input side Supply Voltage
(I_{SENSOR} = +5 mA)

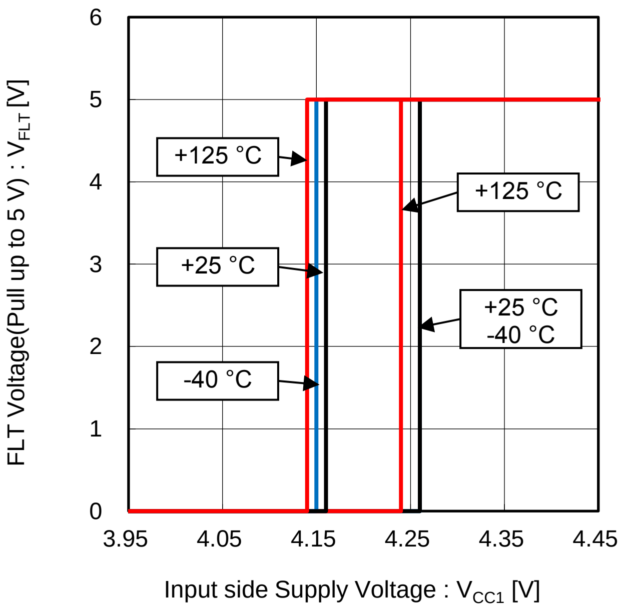


Figure 38. FLT Voltage vs Input side Supply Voltage
(V_{CC1} UVLO On / Off Voltage)

Typical Performance Curves - continued

(Reference data)

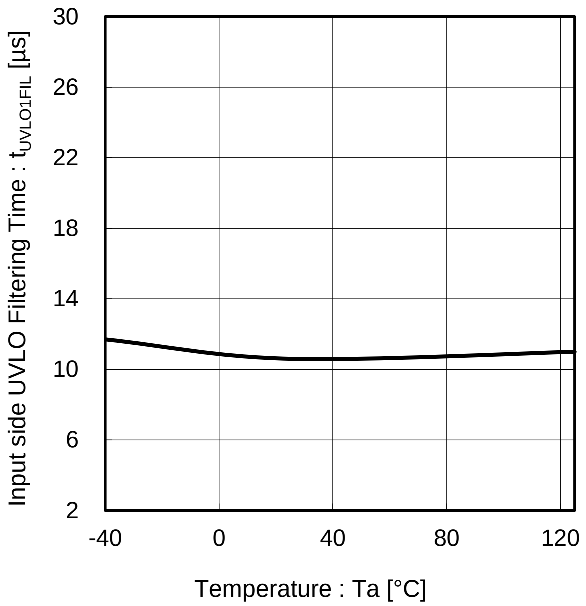


Figure 39. Input side UVLO Filtering Time vs Temperature

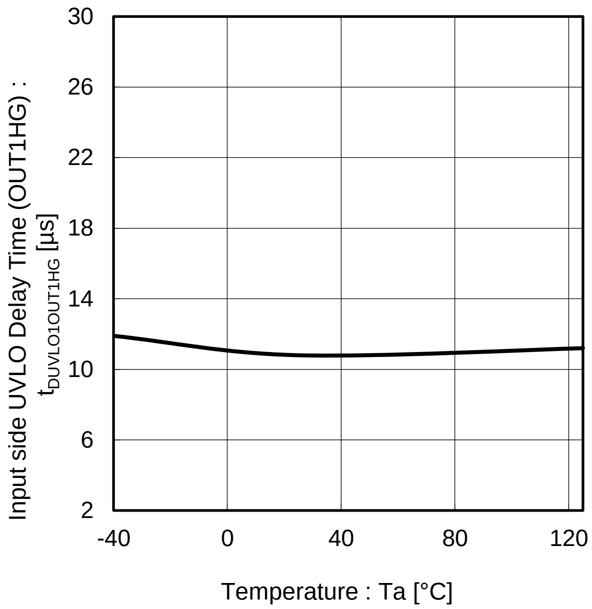


Figure 40. Input side UVLO Delay Time (OUT1HG) vs Temperature

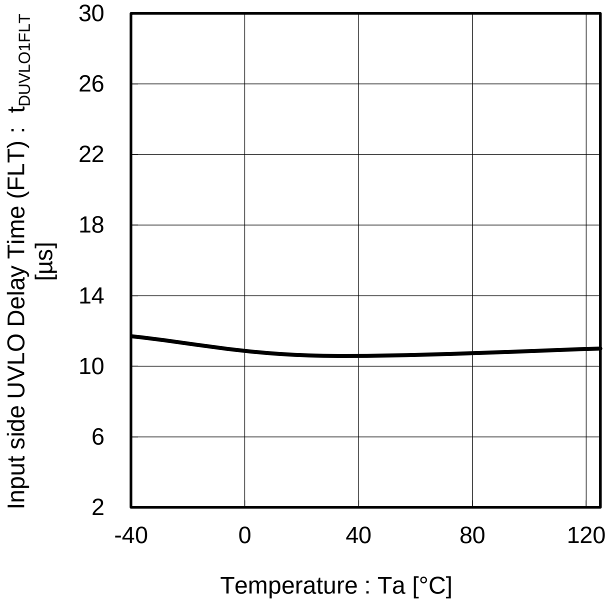


Figure 41. Input side UVLO Delay Time (FLT) vs Temperature

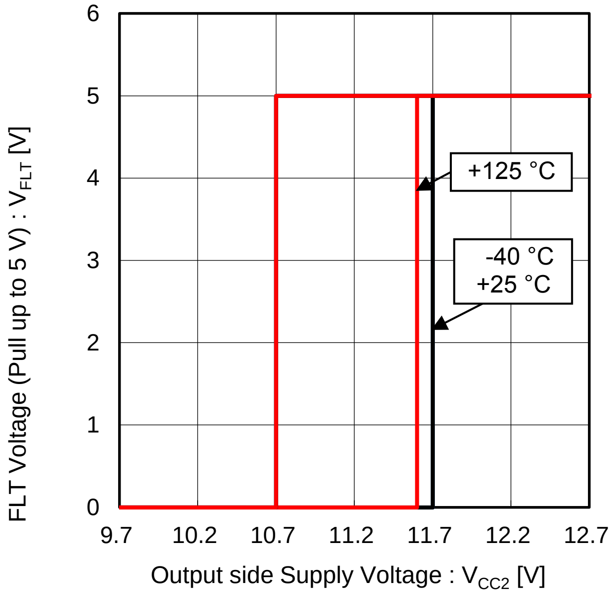


Figure 42. FLT Voltage vs Output side Supply Voltage
(V_{CC2} UVLO On / Off Voltage)

Typical Performance Curves - continued

(Reference data)

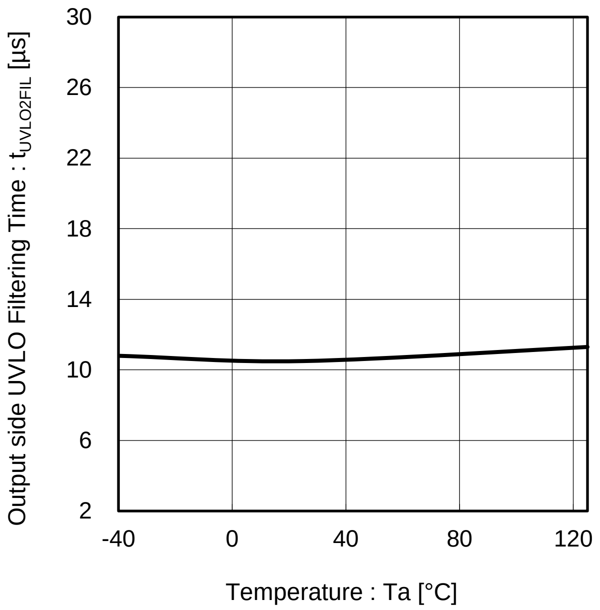


Figure 43. Output side UVLO Filtering Time vs Temperature

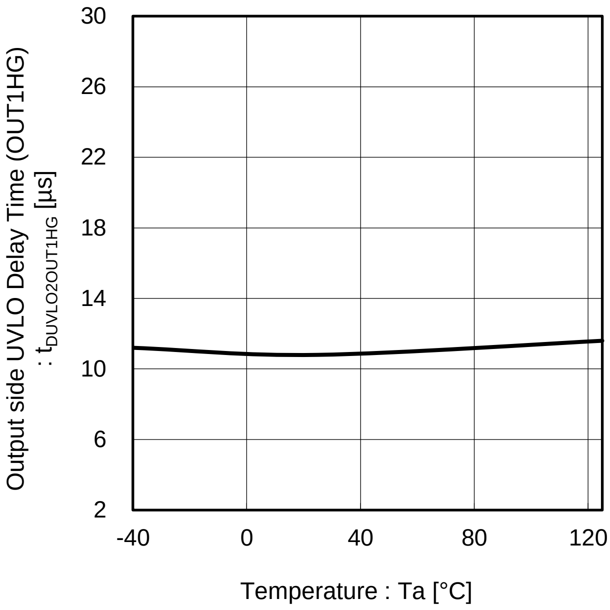


Figure 44. Output side UVLO Delay Time (OUT1HG) vs Temperature

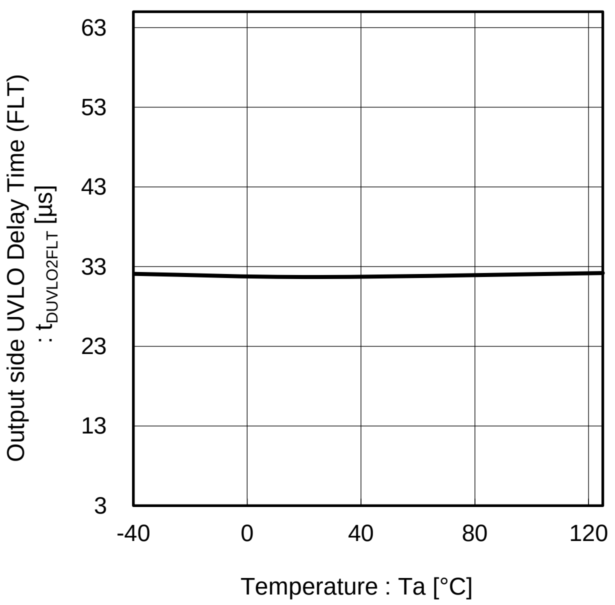


Figure 45. Output side UVLO Delay Time (FLT) vs Temperature

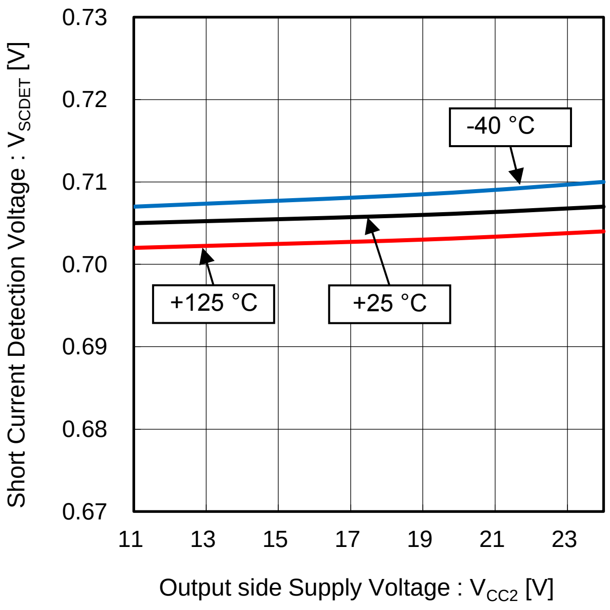


Figure 46. Short Current Detection Voltage vs Output side Supply Voltage

Typical Performance Curves - continued
(Reference data)

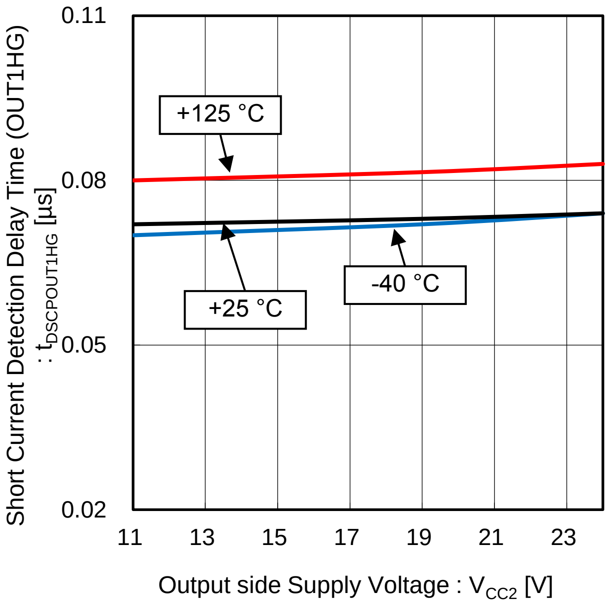


Figure 47. Short Current Detection Delay Time (OUT1HG) vs Output side Supply Voltage (OUT1HG = 1 kΩ Pull Up)

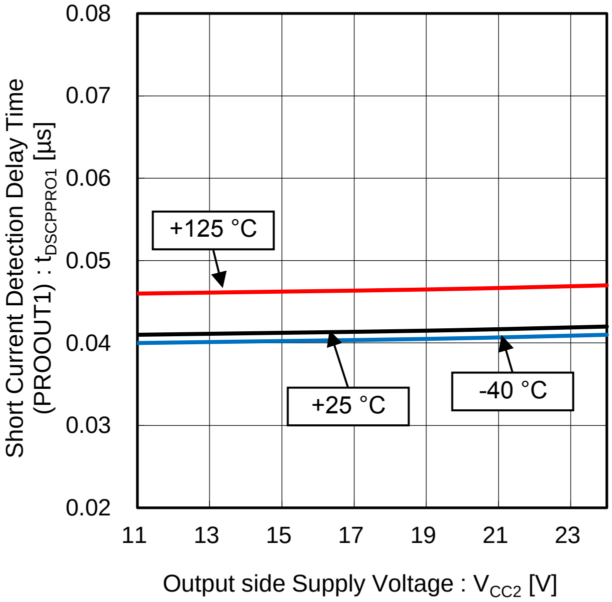


Figure 48. Short Current Detection Delay Time (PROOUT1) vs Output side Supply Voltage

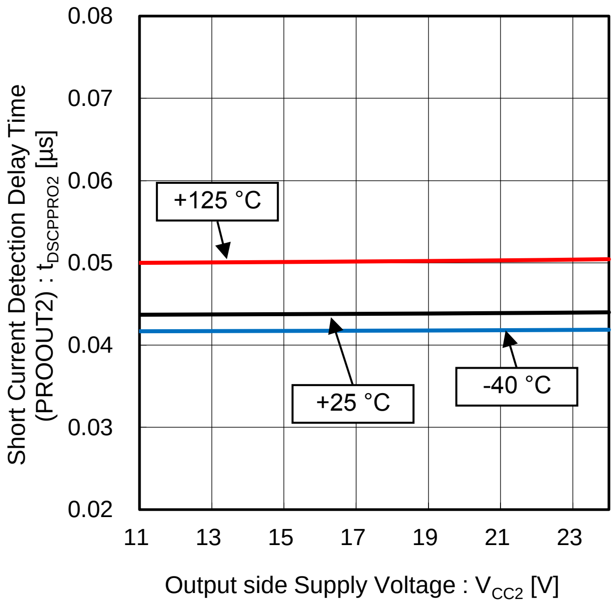


Figure 49. Short Current Detection Delay Time (PROOUT2) vs Output side Supply Voltage

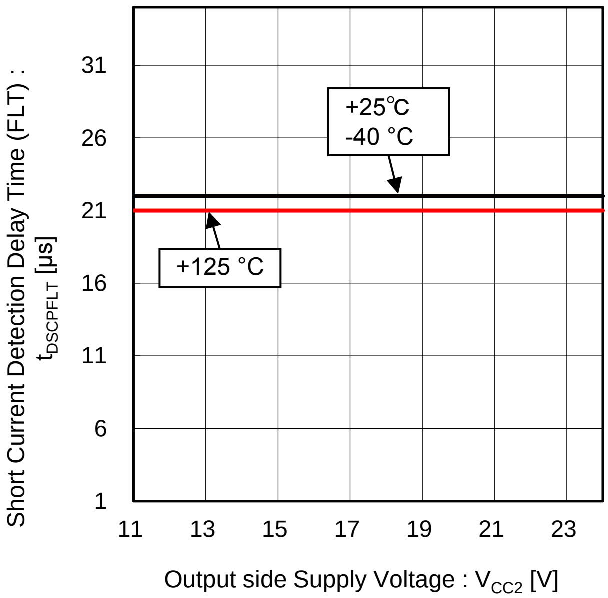


Figure 50. Short Current Detection Delay Time (FLT) vs Output side Supply Voltage

Typical Performance Curves - continued

(Reference data)

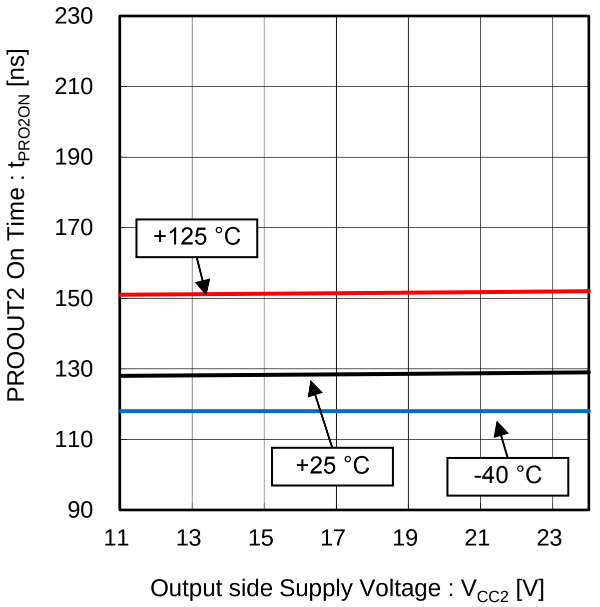


Figure 51. PROOUT2 On Time vs Output side Supply Voltage

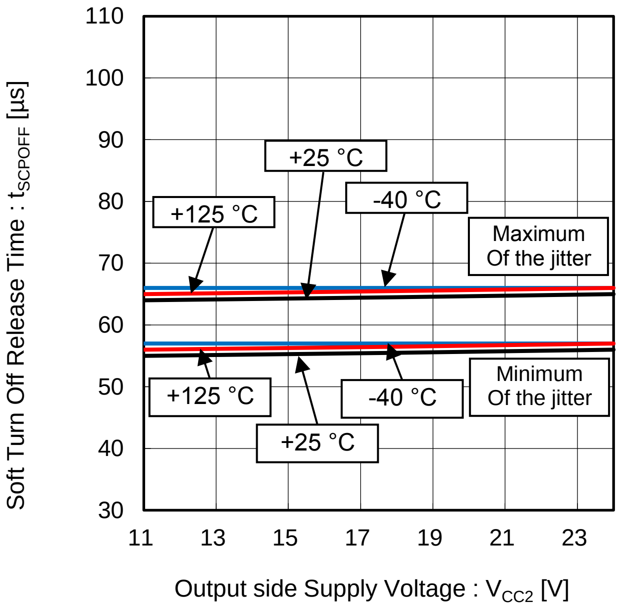


Figure 52. Soft Turn Off Release Time vs Output side Supply Voltage

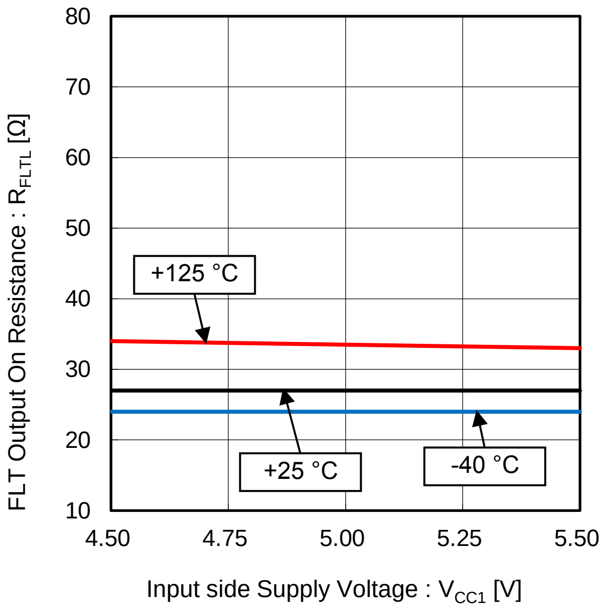


Figure 53. FLT Output On Resistance vs Input side Supply Voltage (I_{FLT} = 5 mA)

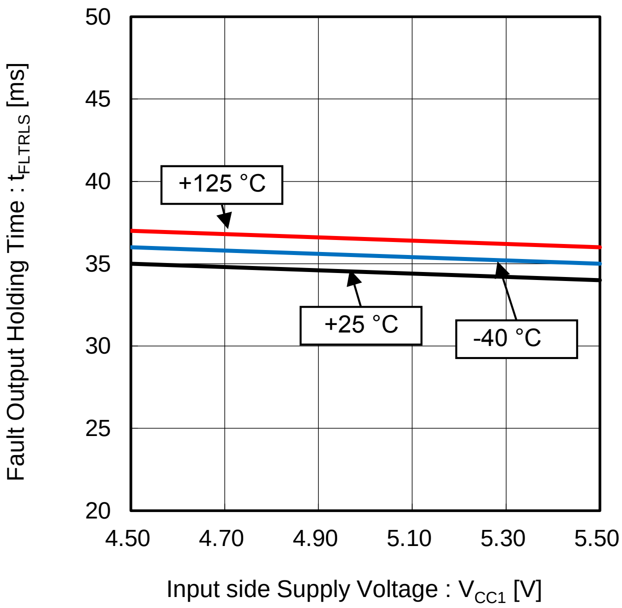


Figure 54. Fault Output Holding Time vs Input side Supply Voltage

Typical Performance Curves - continued

(Reference data)

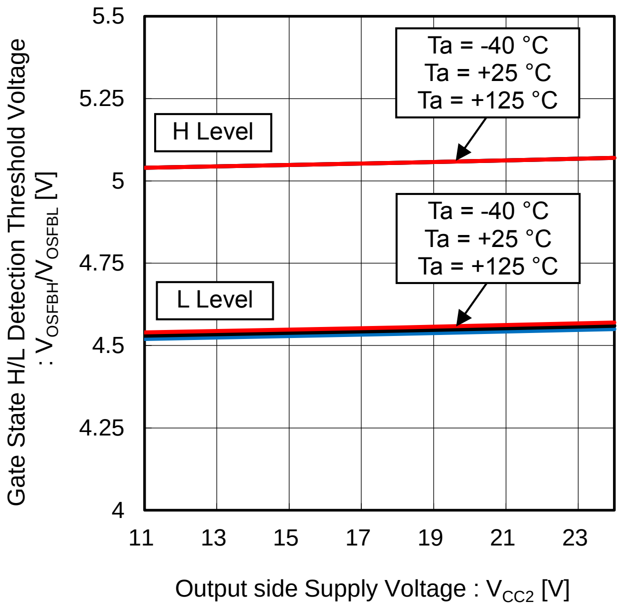


Figure 55. Gate State H/L Detection Threshold Voltage vs Output side Supply Voltage

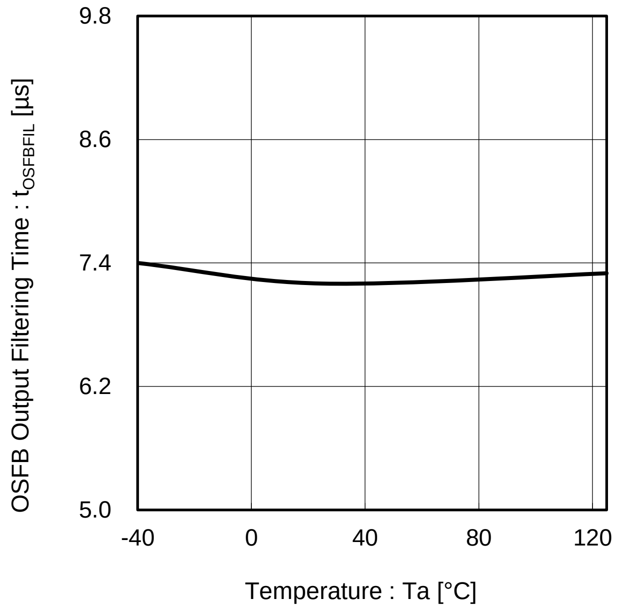


Figure 56. OSFB Output Filtering Time vs Temperature

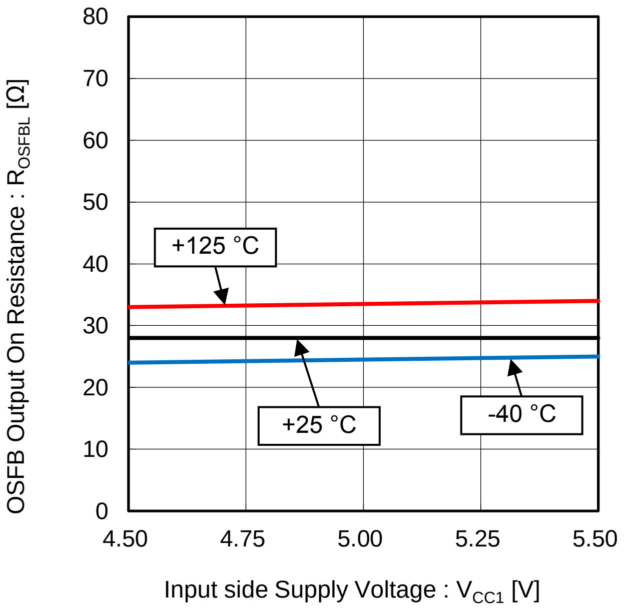


Figure 57. OSFB Output On Resistance vs Input side Supply Voltage (I_{OSFB} = 5 mA)

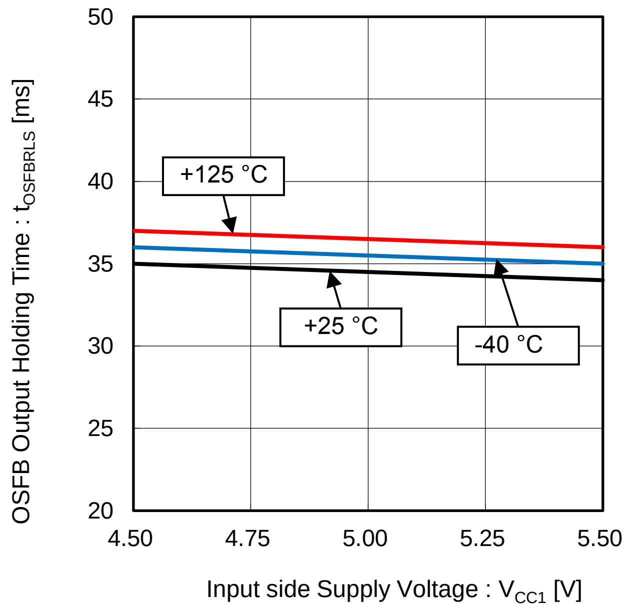


Figure 58. OSFB Output Holding Time vs Input side Supply Voltage

Description of Pins and Cautions on Layout of Board

1. VCC1 (Input side power supply pin)
   This is a power supply pin on the input side. To reduce voltage fluctuations due to the driving current of the internal transformer current. Connect a bypass capacitor between the VCC1 pin and the GND1 pin.

2. GND1 (Input side ground pin)
   This is the ground pin on the input side.

3. VCC2 (Output side power supply pin)
   This is a power supply pin on the output side. To reduce voltage fluctuations due to the driving current of the internal transformer and output current. Connect a bypass capacitor between the VCC2 pin and the GND2 pin.

4. GND2 (Output side ground pin)
   This is the ground pin on the output side. Connect the GND2 pin to the emitter/source of output device.

5. INA (Control input pin) , DIS (Input enabling signal input pin)
   They are the pins for determining the output logic.

DIS	INA	OUT1HG	OUT1L
H	X	H	L
L	L	H	L
L	H	L	Hi-Z

X: Don't care

6. FLT (Fault output pin)
   This is an open drain pin that sends a fault signal when a fault occurs (i.e., Input side / Output side under voltage lockout (UVLO) function or short circuit protection (SCP) function is activated).

Status	FLT
Normal operation	Hi-Z
Fault (Input side UVLO, Output side UVLO, SCP)	L

7. OSFB (Output state feedback output pin)
   This is an open drain pin which compares gate logic of the output device monitored with the PROOUT1 pin and the DIS or INA pin input logic. And this pin outputs Low when they disaccord.

Status	DIS	INA	PROOUT1 input	OSFB
Normal operation	H	X	H	L
	H	X	L	Hi-Z
	L	L	H	L
	L	L	L	Hi-Z
	L	H	H	Hi-Z
	L	H	L	L
Fault	X	X	X	Hi-Z

X: Don't care

8. SENSOR (Temperature information output pin)
   This is a pin that output voltage of the TO pin converted to Duty cycle.

9. OUT1HG (Source side MOS buffer driving pin)
   This is the buffer driving pin for gate on side. Connect it to the gate pin of the buffer (Pch MOS FET). Also, connect a resistor R_{OUT1HG} between the OUT1HG pin and the VCC2 pin to control the gate voltage of the buffer.

10. OUTREF (Reference voltage pin for constant current driving)
    This is the reference pin for gate constant current drive. Connect a resistor R_{OUTREF} between the VCC2 pin and the source pin of the buffer (Pch MOS FET). Also, connect the source pin of the buffer to the OUTREF pin.

11. OUT1L (Sink side output pin)
    This is the driving pin for gate off side.

Description of Pins and Cautions on Layout of Board - continued

12. OUT2 (Output pin for Miller Clamp)
    This is the miller clamp pin for preventing a rise of gate voltage with output miller current. Leave it open when the miller clamping function is not used.

13. PROOUT1 (Soft turn off pin for short circuit protection / Gate voltage input pin), PROOUT2 (Fast turn off pin for short circuit protection)
    They are pins for turn off of output device when short circuit protection is activated. Both the PROOUT1 pin and the PROOUT2 pin are turned on for t_{PRO2ON} from short circuit detection. After t_{PRO2ON} has passed, only the PROOUT1 pin is turned on. The PROOUT1 pin functions as monitoring gate voltage pin for miller clamping function and output state feedback function.

14. SCPIN (Short circuit detection pin)
    This is a pin used to detect current for short circuit protection. When the SCPIN pin voltage is more than V_{SCDET}, the short circuit protection function is activated. There is a possibility of the IC malfunction in an open state. To avoid such trouble, short the SCPIN pin to the GND2 when the short circuit protection function is not used.

15. TC (Resistor connection pin for setting constant current source output)
    This is the resistor connection pin for setting the constant current output. If an arbitrary resistor is connected between the TC pin and the GND2 pin, it is possible to set the constant current value output from the TO pin.

16. TO (Constant current output / Sensor voltage input pin)
    This is the constant current output voltage input pins. It can be used as a sensor input by connecting a device with arbitrary impedance between the TO pin and the GND2 pin.

17. TGND2 (Ground pin for temperature sensor)
    This is the ground pin for temperature monitoring function. Connect it to ground side of temperature sensor.

18. TEST (Test mode setting pin)
    This is the setting pin for test mode. Connect it to the GND1 pin.

Description of Functions and Examples of Constant Setting

1. Fault Signal Output Function

This function is used to output a fault signal from the FLT pin when a fault occurs (i.e., when the under voltage lockout (UVLO) function or short circuit protection (SCP) function is activated), after fault state cancellation, the FLT pin holds a fault signal until fault output holding time (t_{FLTRLS}).

Status	FLT pin
Normal operation	Hi-Z
Fault	L

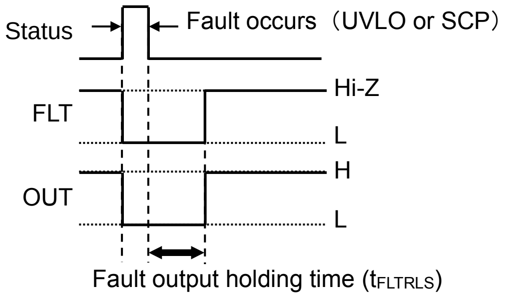


Figure 59. Fault Status Output Timing Chart

2. Under Voltage Lockout (UVLO) Function

This IC incorporates the under voltage lockout function on input side power supply pin (VCC1) and output side power supply pin (VCC2). When the power supply voltage drops to the UVLO ON voltage, the OUT1HG pin outputs the "H" signal and the OUT1L pin and the FLT pin both output the "L" signal. When the power supply voltage rises to the UVLO OFF voltage, these pins are reset. However, during the fault output holding time, the OUT1HG pin holds the "H" signal and the OUT1L pin and the FLT pin hold the "L" signal. In addition, to prevent miss-triggering due to noise, filtering time $t_{UVLO1FIL}$ and $t_{UVLO2FIL}$ are set on input side and output side power supply pins.

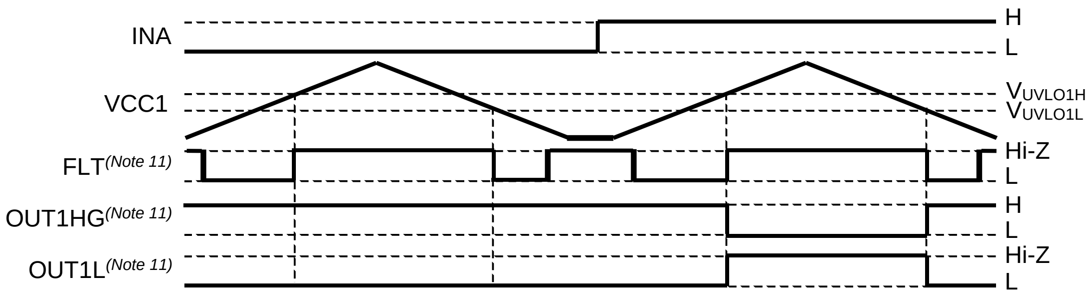


Figure 60. Input side power supply pin (VCC1) UVLO Operation Timing Chart

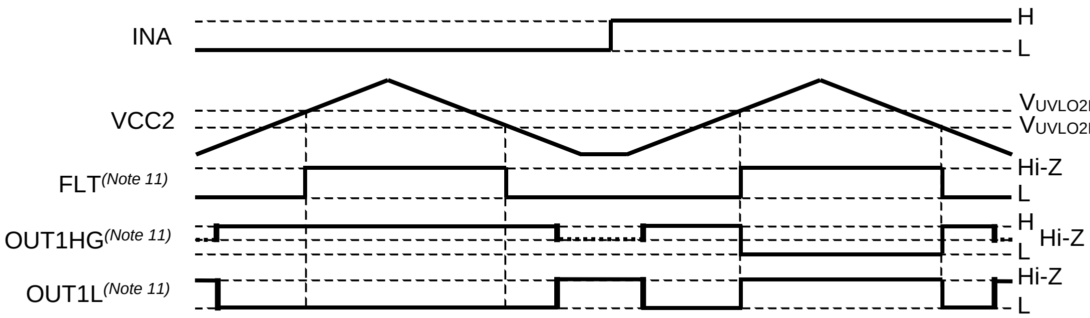


Figure 61. Output side power supply pin (VCC2) UVLO Operation Timing Chart

(Note 11) The FLT pin, the OUT1HG pin and the OUT1L pin start operation after fault output holding time.

Description of Functions and Examples of Constant Setting - continued

3. Short Circuit Protection (SCP) Function

When the SCPIN pin voltage exceeds the V_{SCDET}, the short circuit protection function is activated. When the short circuit protection function is activated, the OUT1HG pin voltage is set to the "H" level, the OUT1L pin voltage is set to the "Hi-Z" level and the PROOUT1 pin, the PROOUT2 pin and the FLT pin voltage go to the "L" level first (Fast Turn Off). Next, after t_{PRO2ON} has passed from the Short Current Detection, the PROOUT2 pin is set to the "Hi-Z" level (Soft Turn Off). And then, after t_{SCPOFF} has passed from short circuit current to be under threshold, the OUT1L pin becomes the "L" level. Finally, when the fault output holding time has passed, the SCP function is released and the FLT pin becomes the "Hi-Z" level. The PROOUT1 pin holds the "L" state until the OUT1HG pin becomes the "L" level with the INA pin is inputted "H" level and the DIS pin is inputted "L" level.

As a side note, when the OUT1L pin is the "L" level, the short circuit is not detected.

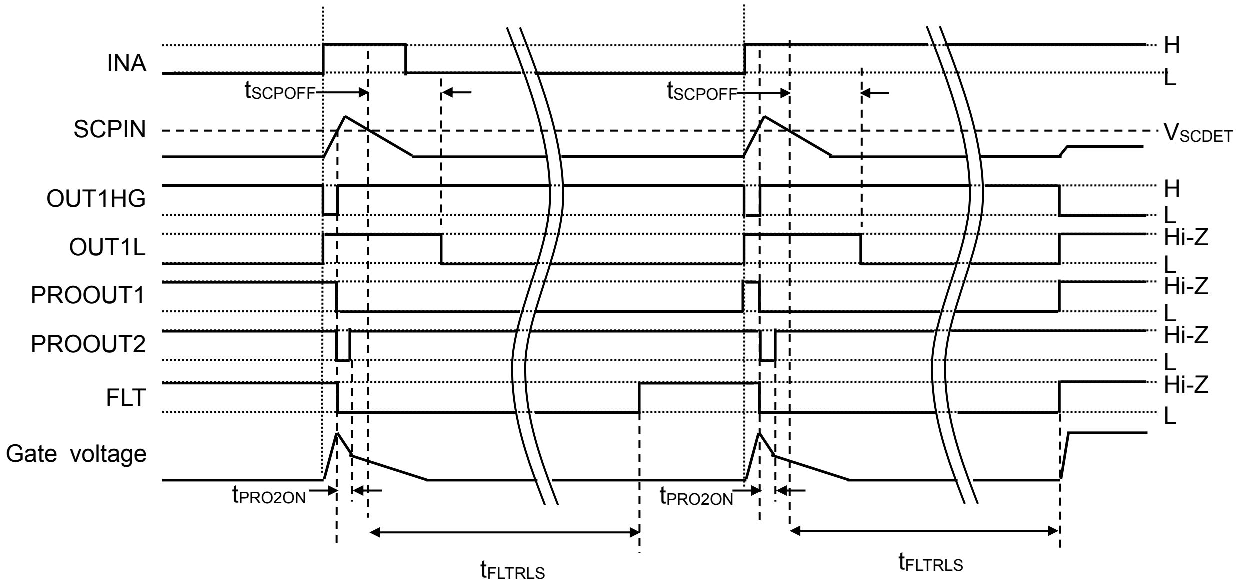


Figure 62. SCP Operation Timing Chart

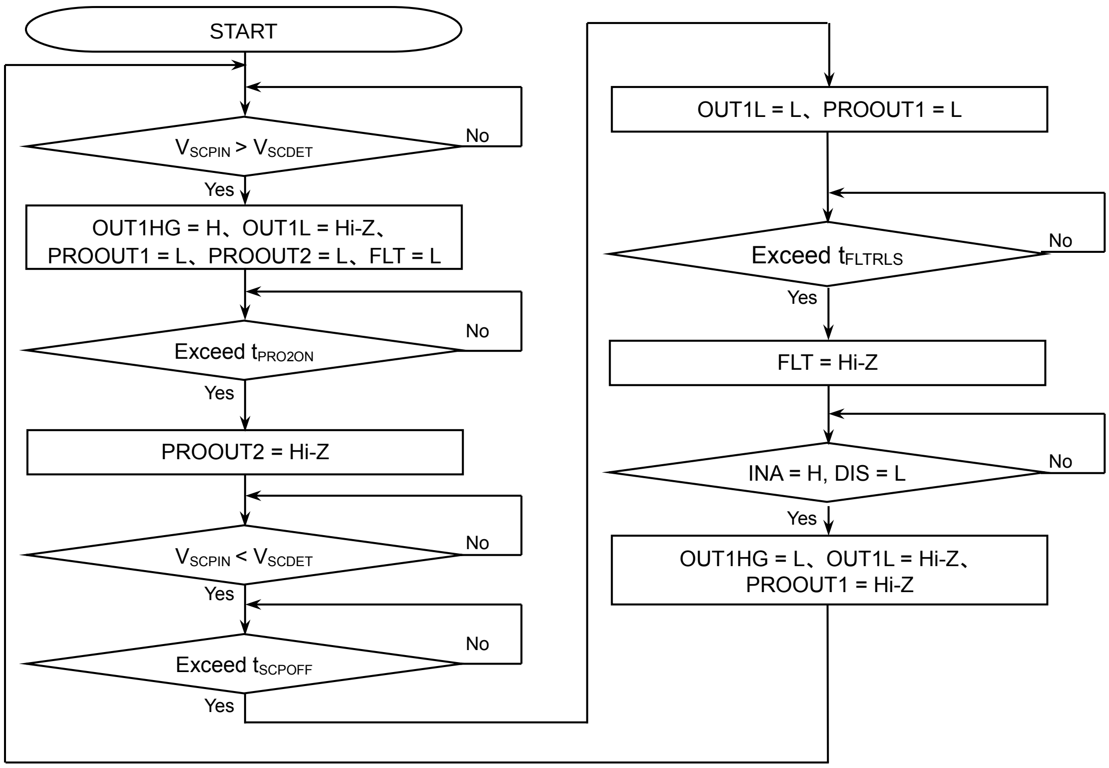


Figure 63. SCP Operation Status Transition Diagram

Description of Functions and Examples of Constant Setting - continued

4. Active Miller Clamping Function

When the OUT1HG pin = “H” level, the OUT1L pin = “L” level and the PROOUT1 pin voltage < V_{OUT2ON}, the internal MOS of the OUT2 pin is turned ON and the active miller clamping function operates. The OUT2 pin is kept the “L” level until the OUT1L pin becomes the “Hi-Z” level. While the short circuit protection function is activated, active miller clamping function operates after soft turn off release time t_{SCPOFF} has passed.

Short current protection	SCPIN	INA	PROOUT1	OUT2
Operated	≥ V_{SCDET}	X	X	Hi-Z
Not operated	X	L	≥ V_{OUT2ON}	Hi-Z
	X	L	< V_{OUT2ON}	L
	X	H	X	Hi-Z

X: Don't care

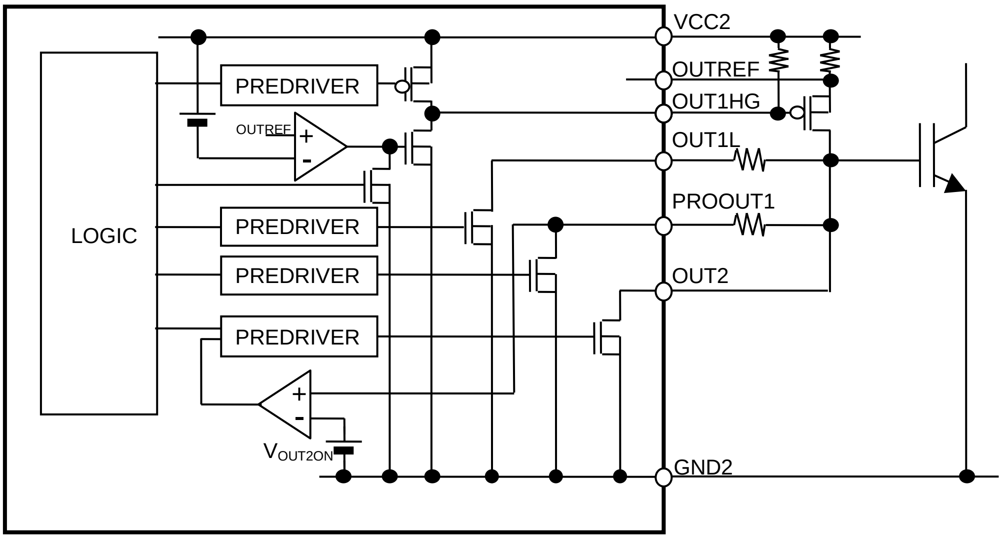


Figure 64. Block Diagram of Miller Clamping Function

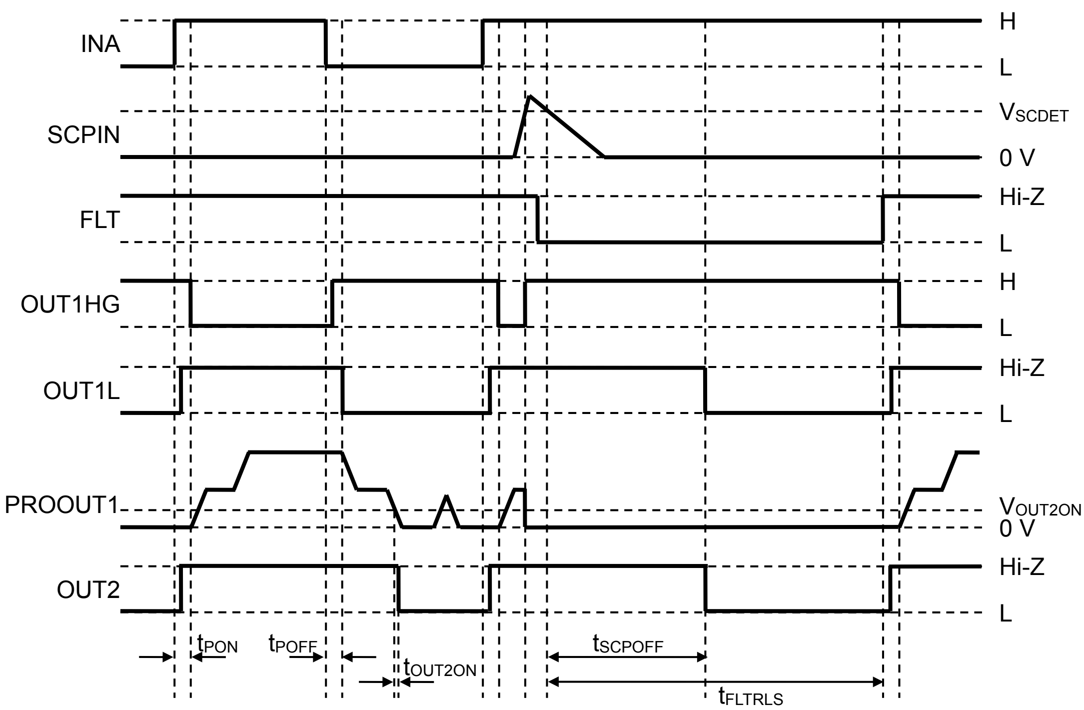


Figure 65. Timing Chart of Miller Clamping Function

Description of Functions and Examples of Constant Setting - continued

5. Gate Constant Current Driving Function

This IC has a gate constant current driving function. Charge the gate of the output element with a constant current by connecting buffer (Pch MOS FET M_{OUT1H}) and resistors (R_{OUTREF}, R_{OUT1HG}) as shown in Figure 66. Constant current I_{GATE} can be set using the following formula:

$$I_{GATE}\,[\mathrm{A}] = V_{OUTREF}\,[\mathrm{V}]\,/R_{OUTREF}\,[\Omega]$$

The table below shows the recommended components for the external parts (M_{OUT1H}, R_{OUTREF}, and R_{OUT1HG}). If using other component for M_{OUT1H} or using resistors outside the recommended range, please make sure that there is no overshoot or oscillation of the current in the operating temperature condition and current setting.

Symbol	Manufacturer	Recommended Components	Recommended Value		Unit
			Min	Max	
M_{OUT1H}	ROHM	RSR015P06HZGTL	-	-	-
R_{OUTREF}	ROHM	MCR Series LTR Series	0.34	-	Ω
R_{OUT1HG}	ROHM		0.5	2.5	kΩ

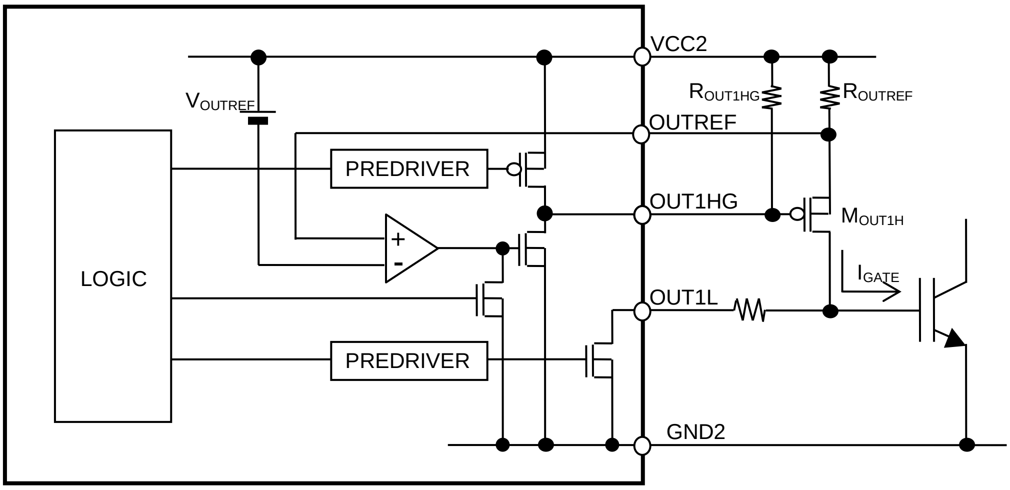


Figure 66. Block Diagram of Gate Constant Current Driving Function

6. Output State Feedback Function

When the gate logic of output device monitored with the PROOUT1 pin and input logic are compared, and they are different, the OSFB pin outputs the "L" signal. In order to prevent the detection error due to delay of input and output, OSFB filter time t_{OSFBON} is provided. After resolving the mismatch state, hold the OSFB to the "L" level during OSFB output holding time ($t_{OSFBRLS}$).

Description of Functions and Examples of Constant Setting - continued

7. Temperature Monitoring Function

This IC has a built-in constant current output circuit that supplies a constant current output from the TO pin. The current can be adjusted depending on the resistance value connected between the TC pin and the TGND2 pin. Furthermore, the TO pin has voltage input function. The SENSOR pin outputs the signal of the TO pin voltage converted to Duty. When the temperature monitoring function is not used, connect the TO pin to GND2.

$$\text{Constant Current: } I_{TO}[\text{mA}] = 10 \times V_{TC}[\text{V}] \;/\; R_{TC}[\text{k}\Omega]$$

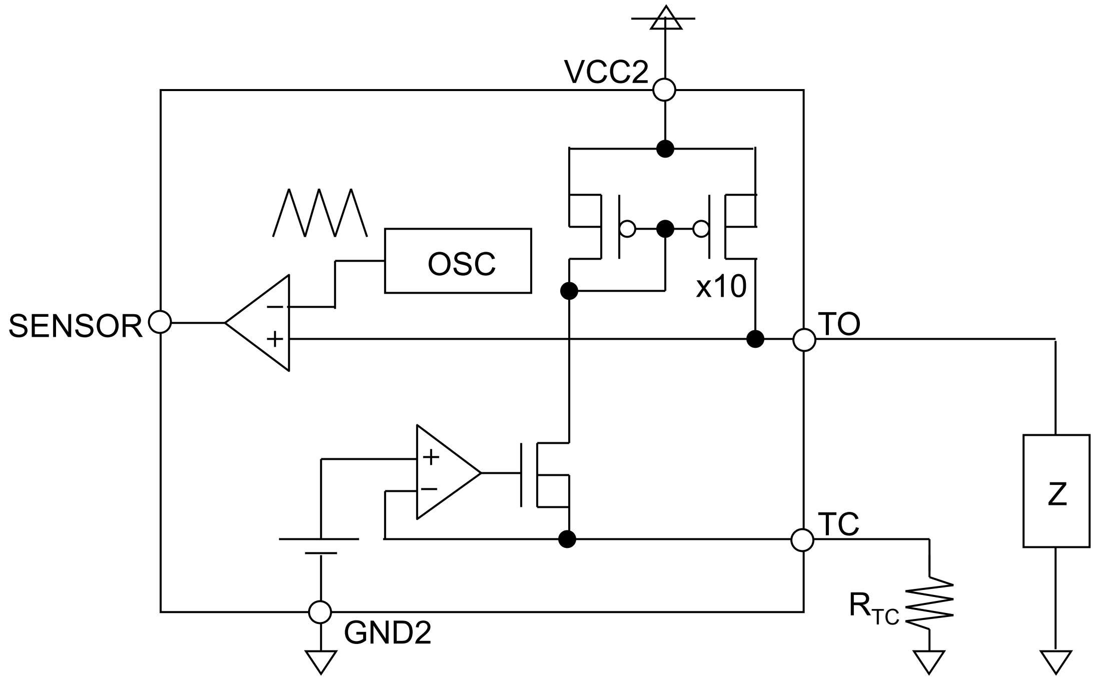


Figure 67. Block Diagram of Temperature Monitoring Function

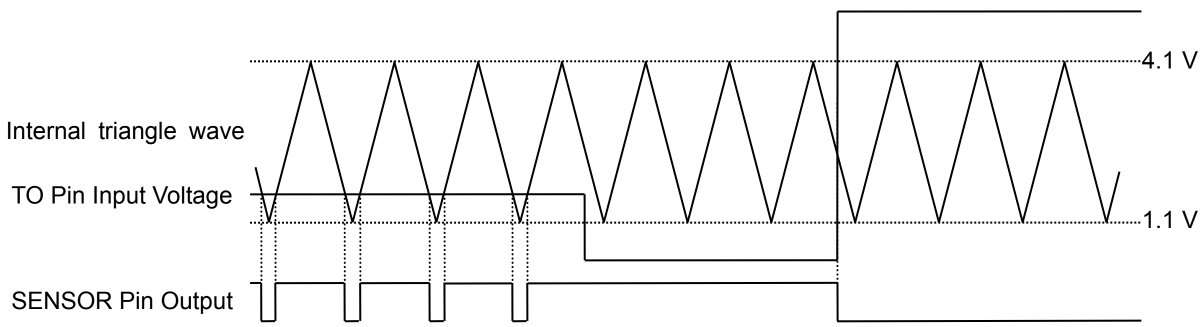


Figure 68. Timing Chart of Temperature Monitoring Function

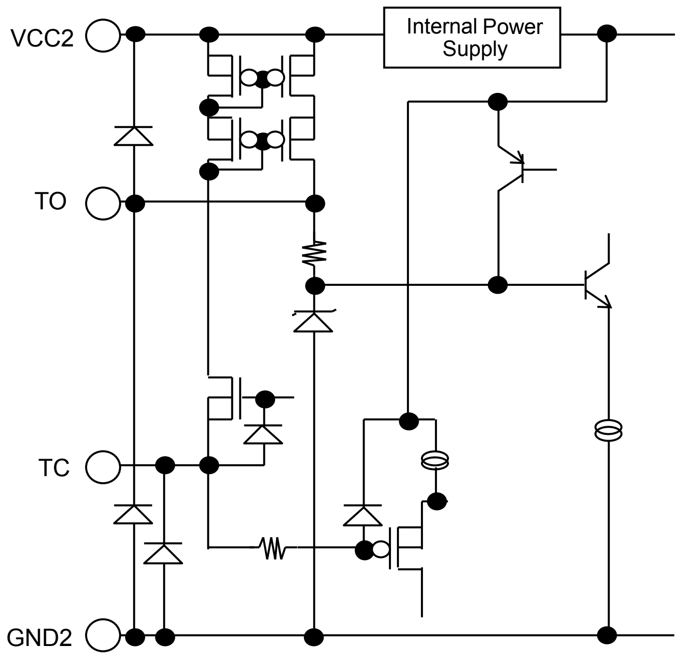
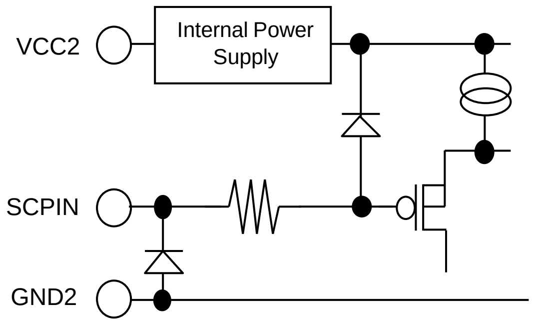
Description of Functions and Examples of Constant Setting - continued

8. I/O Condition Table

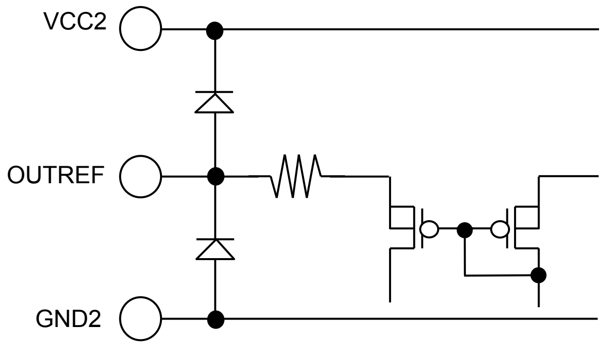
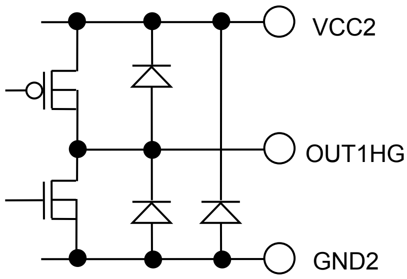
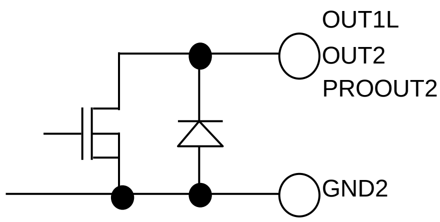
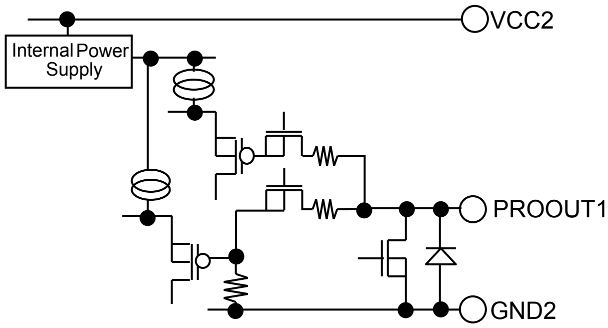
No	Status	Input						Output						
		VCC1	VCC2	SCPIN	DIS	INA	PROOUT1 Input	OUT1HG	OUT1L	OUT2	PROOUT1	PROOUT2	FLT	OSFB
1	SCP	○	○	H	L	H	X	H	Z	Z	L	L→Z	L	Z
2	VCC1 UVLO	UVLO	X	L	X	X	H	H	L	Z	Z	Z	L	Z
3		UVLO	X	L	X	X	L	H	L	L	Z	Z	L	Z
4	VCC2 UVLO	X	UVLO	L	X	X	H	H	L	Z	Z	Z	L	Z
5		X	UVLO	L	X	X	L	H	L	L	Z	Z	L	Z
6	Disable	○	○	L	H	X	H	H	L	Z	Z	Z	Z	L
7		○	○	L	H	X	L	H	L	L	Z	Z	Z	Z
8	Normal Operation L Input	○	○	L	L	L	H	H	L	Z	Z	Z	Z	L
9		○	○	L	L	L	L	H	L	L	Z	Z	Z	Z
10	Normal Operation H Input	○	○	L	L	H	H	L	Z	Z	Z	Z	Z	Z
11		○	○	L	L	H	L	L	Z	Z	Z	Z	Z	L

○: Power supply voltage > UVLO, X: Don't care, Z: Hi-Z

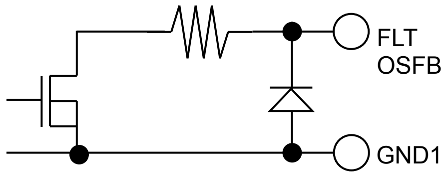
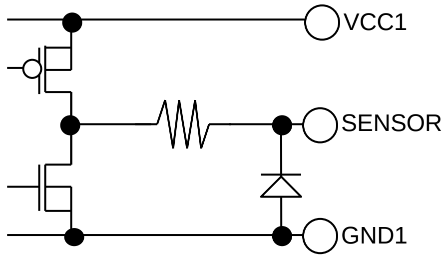
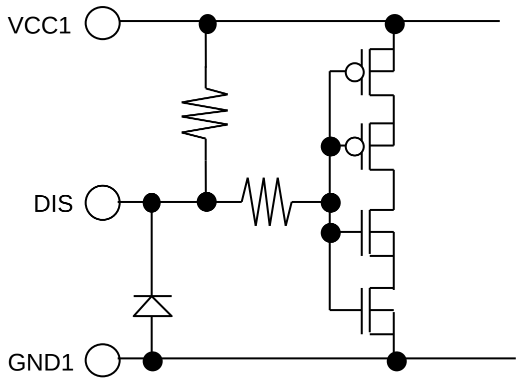
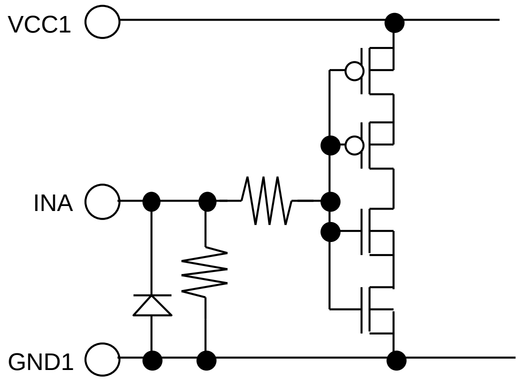
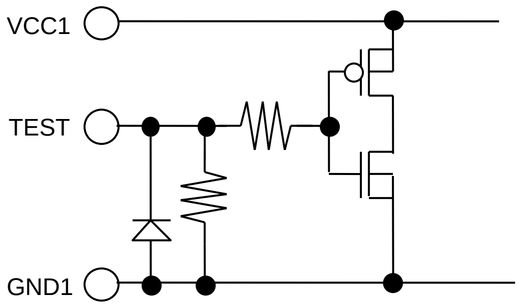
I/O Equivalence Circuits

Pin No.	Pin Name	Input Output Equivalence Circuit Diagram
	Pin Function	
2	TO	
	Constant current output pin / Sensor voltage input pin	
4	TC	
	Resistor connection pin for setting constant current source output	
8	SCPIN	
	Short circuit detection pin	

I/O Equivalence Circuits - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
11	OUTREF Reference voltage pin for constant current driving	
13	OUT1HG Source side MOS buffer driving pin	
15	OUT1L Sink side output pin	
18	OUT2 Output pin for Miller Clamp	
17	PROOUT2 Fast turn off pin for short circuit protection	
16	PROOUT1 Soft turn off pin for short circuit protection / Gate voltage input pin	

I/O Equivalence Circuits - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
21	FLT Fault output pin	
26	OSFB Output state feedback output pin	
25	SENSOR Temperature information output pin	
22	DIS Input enabling signal input pin	
23	INA Control input pin	
37	TEST Test mode setting pin	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

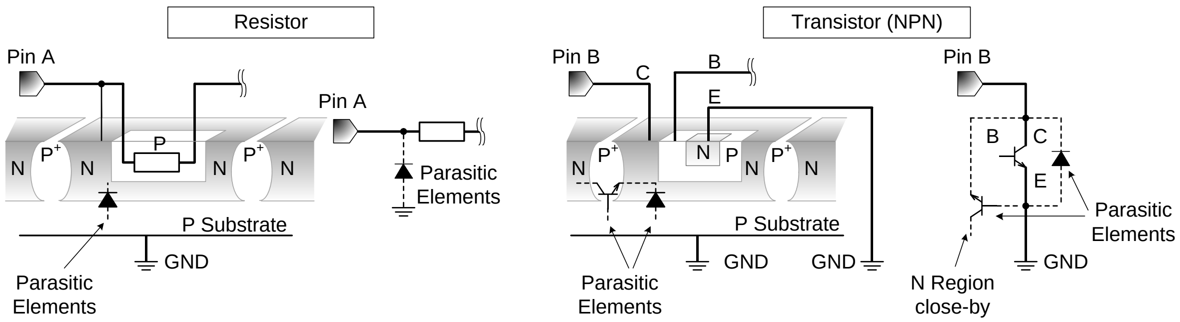


Figure 69. Example of IC Structure

11. **Ceramic Capacitor**
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others

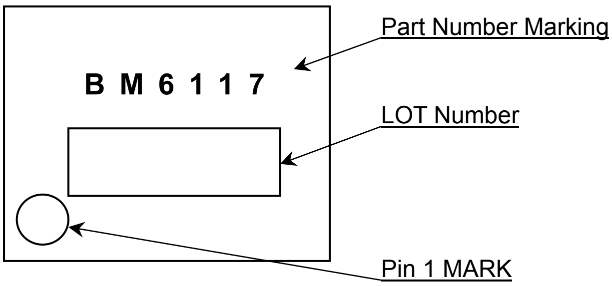
Ordering Information

B M 6 1 1 7 F U - C E 2

- Part Number
- Package
  FU : SSOP-C38W
- Product class
  C: for Automotive applications
  Packaging and forming specification
  E2: Embossed tape and reel

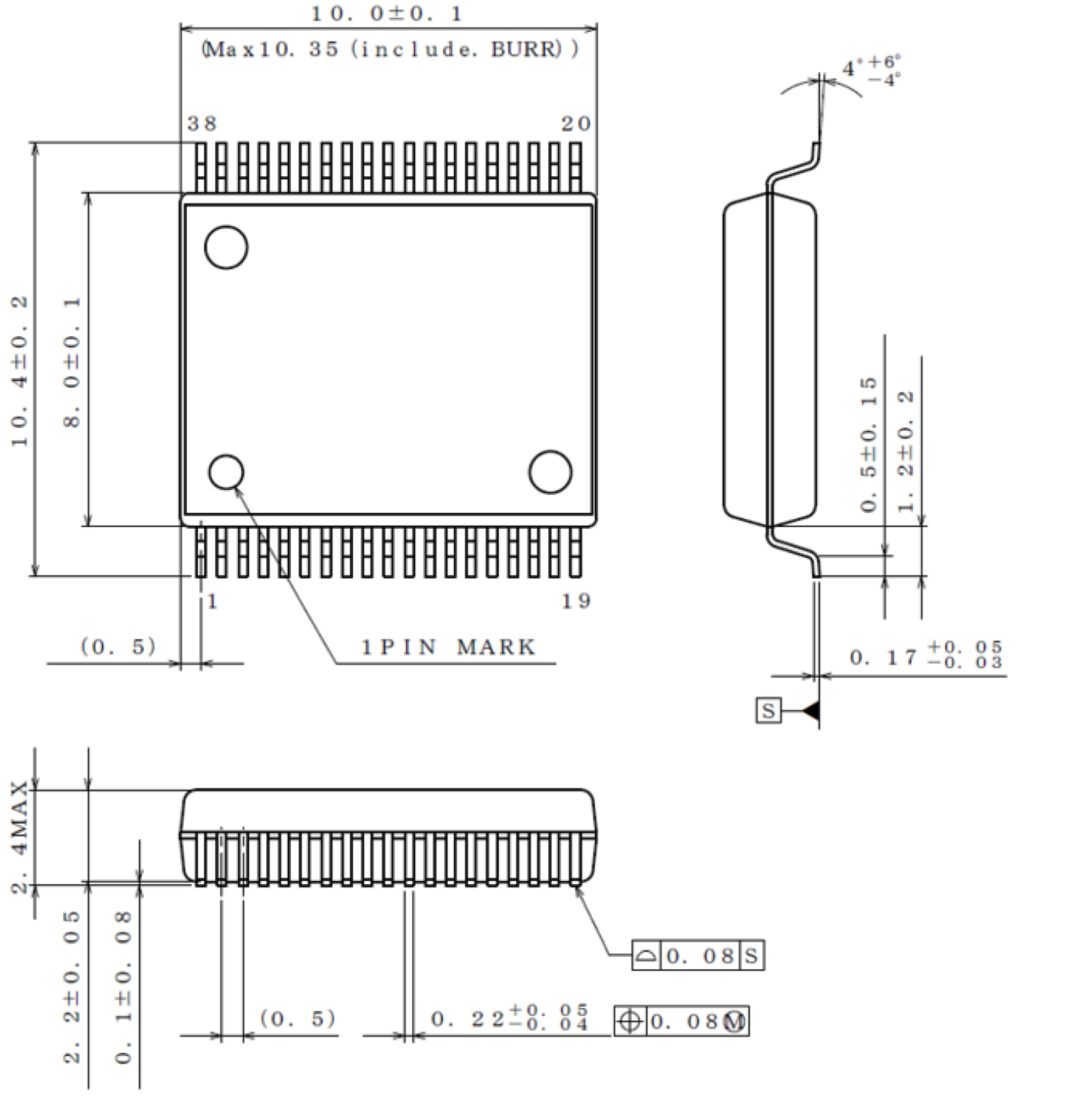
Marking Diagram

SSOP-C38W (TOP VIEW)



Physical Dimension and Packing Information

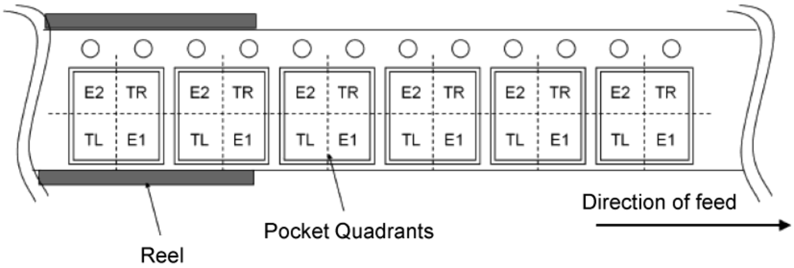
Package Name	SSOP-C38W



(UNIT : mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
04.Oct.2024	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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