Datasheet

Automotive IPD Series

5ch Low Side Switch with Built-in LDO

BD5LL20AEFV-C

General Description

BD5LL20AEFV-C is 5-channel SPI-input low side switch developed as engine control. It has built-in open load detection function, over current protection function, thermal shutdown function, and active clamp function. It also has a 5 V output LDO as a power supply for the microcontroller and a built-in K-LINE communication circuit, making it suitable for motorcycle engine control.

Features

- AEC-Q100 Qualified(Note 1)
- Monolithic Power Management IC with Control Block (CMOS) and a Power MOSFET mounted on a Single Chip
- Each Channel Control/Error can be detected by 16 bit SPI Commands
- Built-in Open Load Detection Function (OLD)
- Built-in Over Current Protection Function (OCP)
- Built-in Thermal Shutdown Function (TSD)
- Built-in Active Clamp Function
- Built-in 5 V Output LDO
- Built-in K-LINE Communication Circuit
- Surface-mount HTSSOP-B20 Packaging

(Note 1) Grade 1

Application

- Driving Resistive and Inductive Load

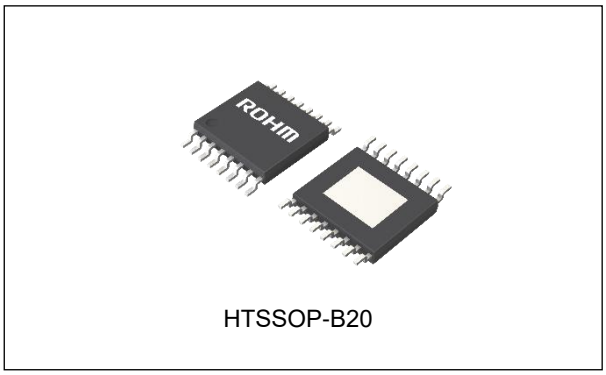
Key Specifications

- Power Supply Operating Range VX: 6 V to 18 V
- Power Supply Operating Range VS: 6 V to 8 V
- LDO Output Voltage: 5.0 V (Typ)
- LDO Over Current Threshold Value: 250 mA (Min)
- On Resistance(Note 1): 200 mΩ / 540 mΩ (Typ)
- Over Current Threshold Value: 2.0 A / 0.5 A (Min)
- Active Clamp Energy(Note 1): 300 mJ / 250 mJ
- Operating Temperature Range: -40 °C to +150 °C

(Note 1) (OUT1 ,OUT2, OUT3) / (OUT4, OUT5) value

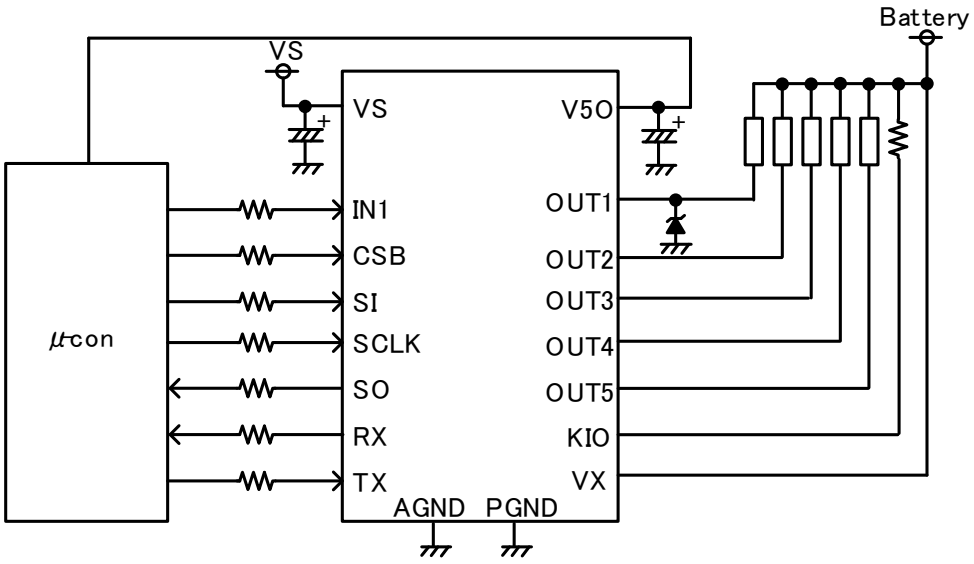
Package

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B20	6.5 mm x 6.4 mm x 1.0 mm



HTSSOP-B20

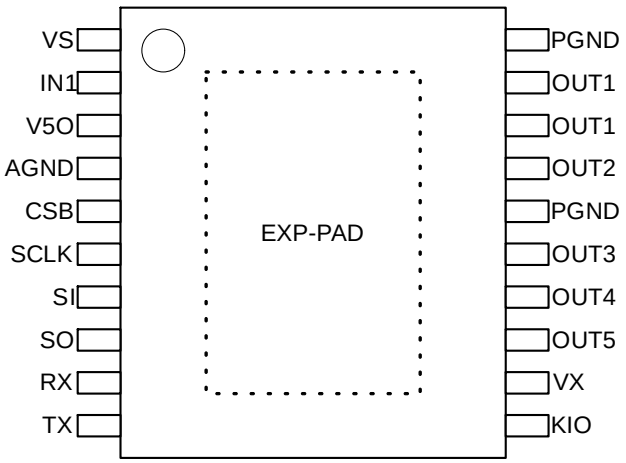
Typical Application Circuit



Contents

Pin Configuration

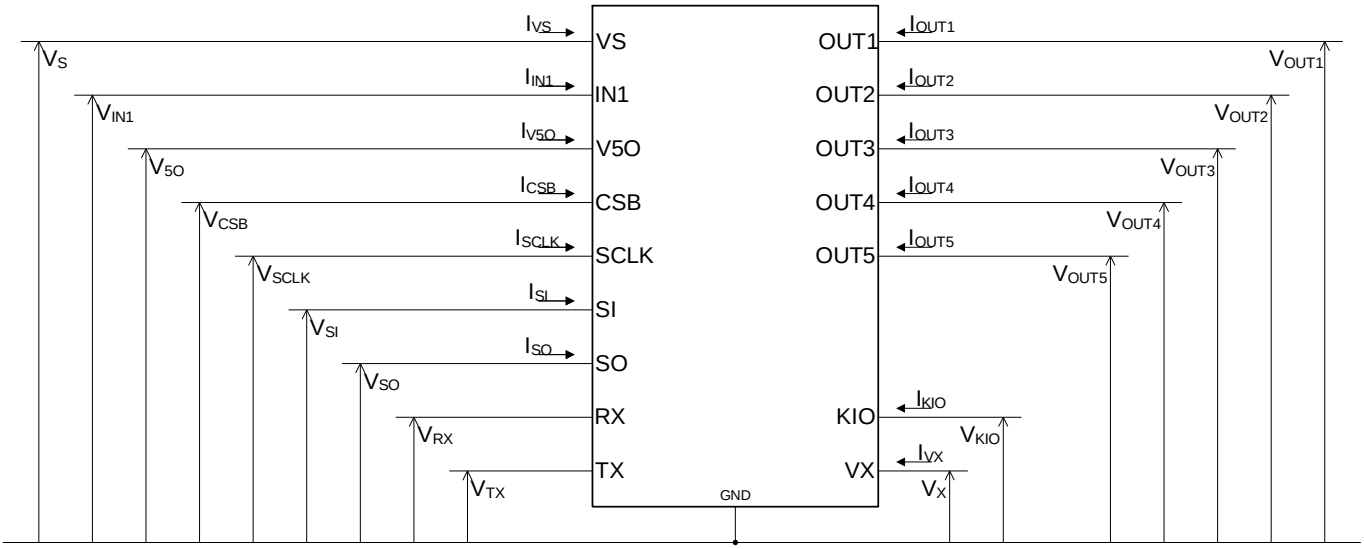
(TOP VIEW)



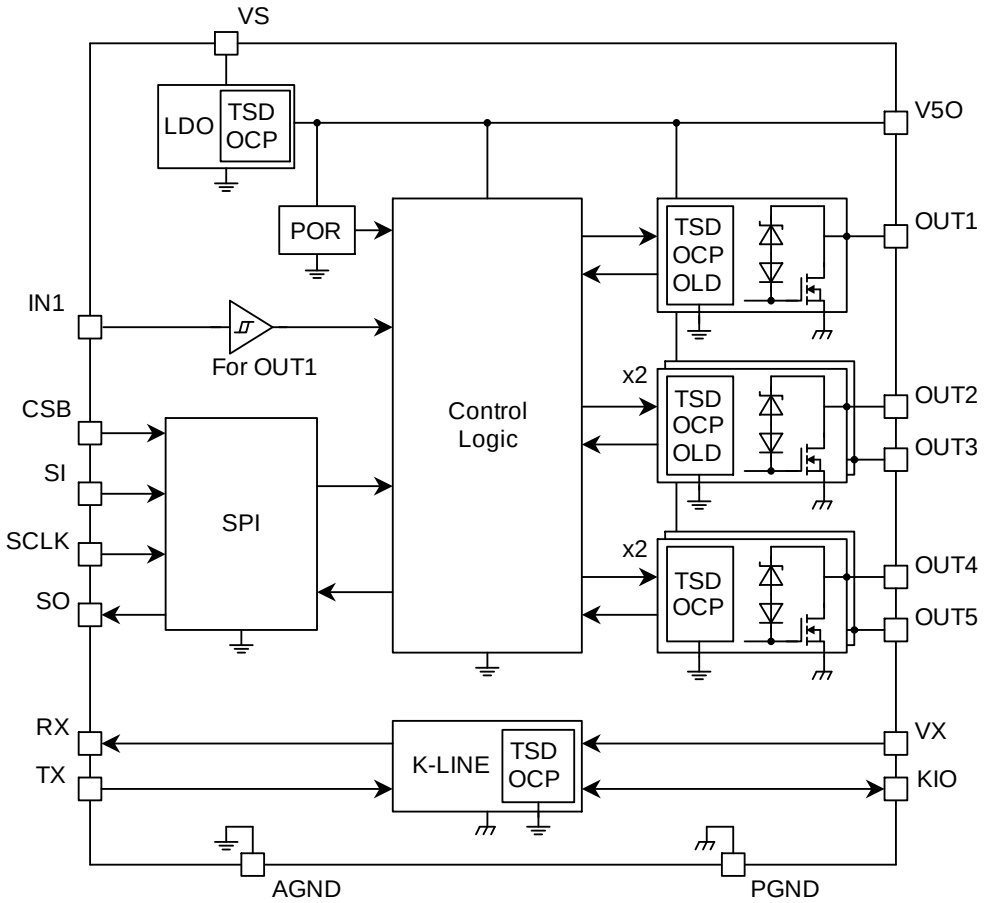
Pin Descriptions

Pin No.	Pin Name	Function
1	VS	LDO power supply
2	IN1	OUT1 control input Connected to GND via an internal pull-down resistor.
3	V5O	5 V output
4	AGND	Analog GND
5	CSB	SPI enable Connected to V5O via an internal pull-up resistor.
6	SCLK	Serial clock input Connected to GND via an internal pull-down resistor.
7	SI	Serial data input Connected to GND via an internal pull-down resistor.
8	SO	Serial data output
9	RX	K-LINE output
10	TX	K-LINE input Connected to V5O via an internal pull-up resistor.
11	KIO	K-LINE bus connection
12	VX	K-LINE power supply
13	OUT5	ch5 output
14	OUT4	ch4 output
15	OUT3	ch3 output
16	PGND	Power GND
17	OUT2	ch2 output
18	OUT1	ch1 output
19	OUT1	ch1 output
20	PGND	Power GND
-	EXP-PAD	The EXP-PAD is connected to GND.

Definition



Block Diagram



Absolute Maximum Ratings (Tj = 25 °C)

Parameter	Symbol	Rating	Unit
VX Power Supply Voltage	V_X	-0.3 to +30	V
VS Power Supply Voltage	V_S	-0.3 to +10	V
Output Voltage OUT1, OUT2, OUT3, OUT4, OUT5	V_{OUT1-5}	-0.3 to +30 (Internal Limit)*(Note 1)*	V
Output Current OUT1, OUT2, OUT3	I_{OUT123}	2.0 (Internal Limit)*(Note 2)*	A
Output Current OUT4, OUT5	I_{OUT45}	0.5 (Internal Limit)*(Note 2)*	A
Output Voltage SO	V_{SO}	-0.3 to +7	V
Output Voltage RX	V_{RX}	-0.3 to +7	V
Input Voltage CSB,SI,SCLK	V_{CSB}, V_{SCLK}, V_{SI}	-0.3 to +7	V
Input Voltage IN1,TX	V_{IN1}, V_{TX}	-0.3 to +7	V
Input Voltage KIO	V_{KIO}	-0.3 to +30	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Active Clamp Energy (Single Pulse) OUT1, OUT2, OUT3, $Tj_{(START)}$ = 25 °C, $I_{OUT1(START)}$ = 1.0 A	$E_{AS123(25\ °C)}$	300	mJ
Active Clamp Energy (Single Pulse) OUT1, OUT2, OUT3, $Tj_{(START)}$ = 150 °C, $I_{OUT1(START)}$ = 1.0 A	$E_{AS123(150\ °C)}$	75	mJ
Active Clamp Energy (Single Pulse) OUT4, OUT5 $Tj_{(START)}$ = 25 °C, $I_{OUT2(START)}$ = 0.5 A	$E_{AS45(25\ °C)}$	250	mJ
Active Clamp Energy (Single Pulse) OUT4, OUT5 $Tj_{(START)}$ = 150 °C, $I_{OUT2(START)}$ = 0.5 A	$E_{AS45(150\ °C)}$	50	mJ

(Note 1) Limited by the active clamp function.
(Note 2) Limited by the over current protection function.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Caution 3: *When IC is turned off with an inductive load, reverse energy has to be dissipated in the IC. This energy can be calculated by the following equation:*

$$E_L = \frac{1}{2} L I_{OUT(START)}{}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}}\right)$$

Where:
L is the inductance of the inductive load.
$I_{OUT(START)}$ is the output current at the time of turning off.
$V_{OUT(CL)}$ is the output clamp voltage.

The IC integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp energy E_{AS123} (Figure 1.), E_{AS45} (Figure 2.) or under when inductive load is used.

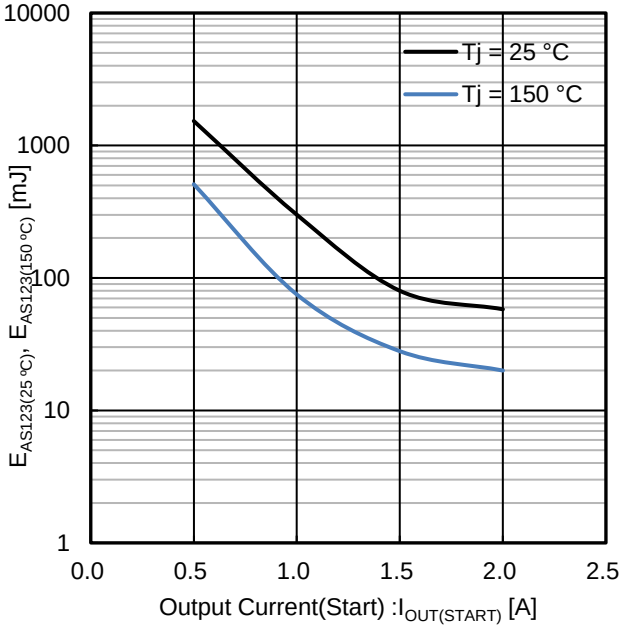


Figure 1. Active Clamp Energy (Single Pulse) vs Output Current(Start) (OUT1, OUT2, OUT3)

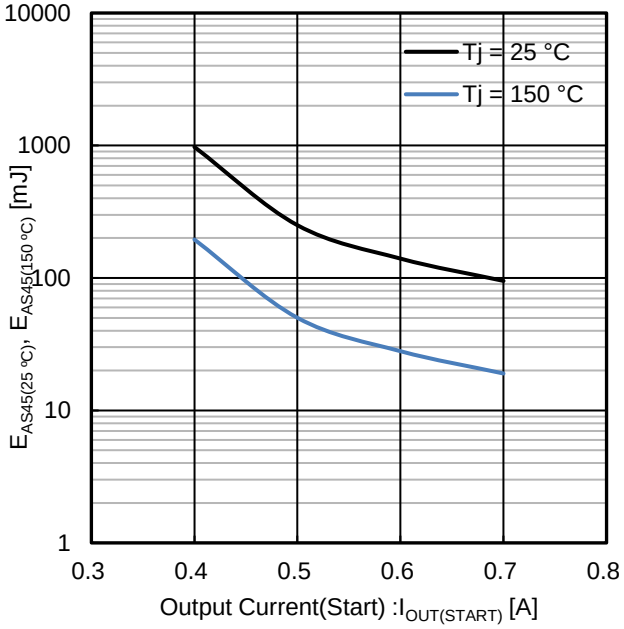


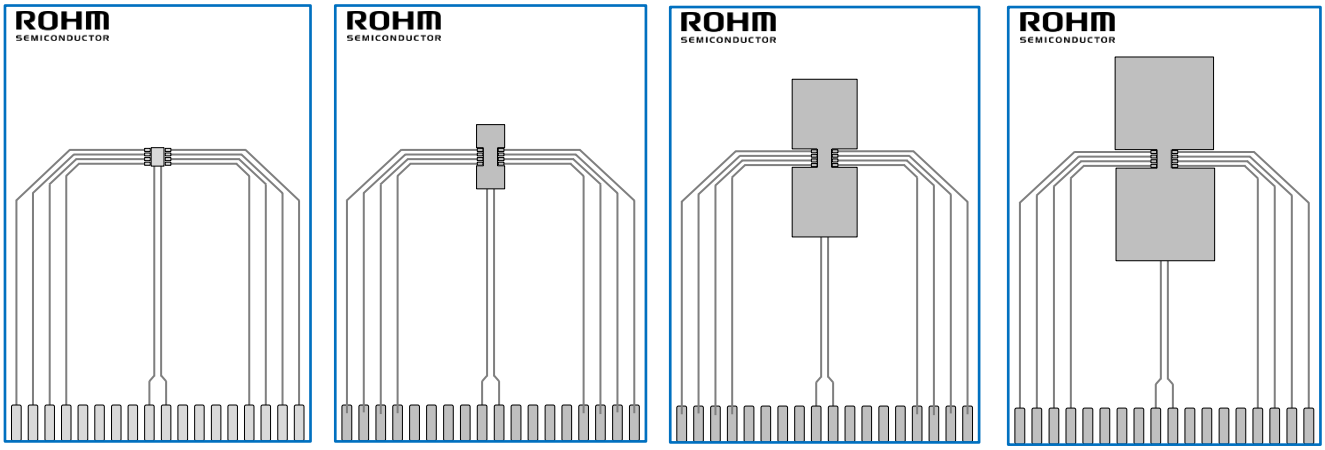
Figure 2. Active Clamp Energy (Single Pulse) vs Output Current(Start) (OUT4, OUT5)

Thermal Resistance *(Note 1)*

Parameter	Symbol	Typ	Unit	Condition
HTSSOP-B20				
Between Junction and Surroundings Temperature Thermal Resistance	θ_{JA}	95.6	°C/W	1s *(Note 2)*
		33.8	°C/W	2s *(Note 3)*
		24.4	°C/W	2s2p *(Note 4)*

(Note 1) The thermal impedance is based on JESD51-2A(Still-Air) standard.
(Note 2) JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)
(Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper.)
(Note 3) JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s).
(Top copper foil: ROHM recommended Footprint + wiring to measure/
Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm, copper (top & reverse side) 2 oz.)
(Note 4) JESD51-5/-7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, copper (top & reverse side/inner layers) 2 oz./1 oz.)

■ PCB Layout 1 layer (1s)



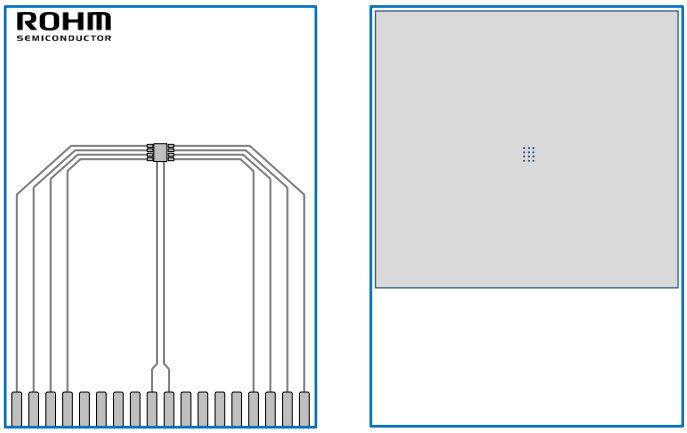
Footprint 100 mm^2 600 mm^2 1200 mm^2

Figure 3. PCB Layout 1 Layer (1s)

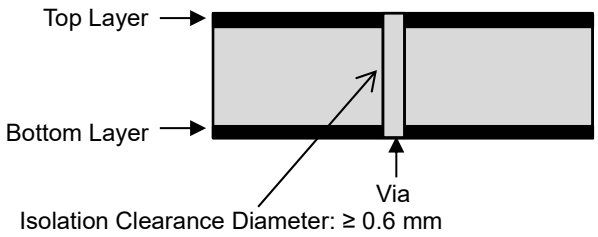
Dimension	Value
Board Finish Thickness	1.57 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top Layer)	0.070 mm (Cu: 2 oz)
Copper Foil Area Dimension	Footprint/100 mm^2/600 mm^2/1200 mm^2

Thermal Resistance – continued

■ PCB Layout 2 layers (2s)



Top Layer Bottom Layer



Cross Section

Figure 4. PCB-layout 2-layer (2s)

Dimension	Value
Board Finish Thickness	1.60 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu +Plating)
Thermal Vias Separation/Diameter	1.2 mm/0.3 mm

Thermal Resistance – continued

■ PCB Layout 4 layers (2s2p)

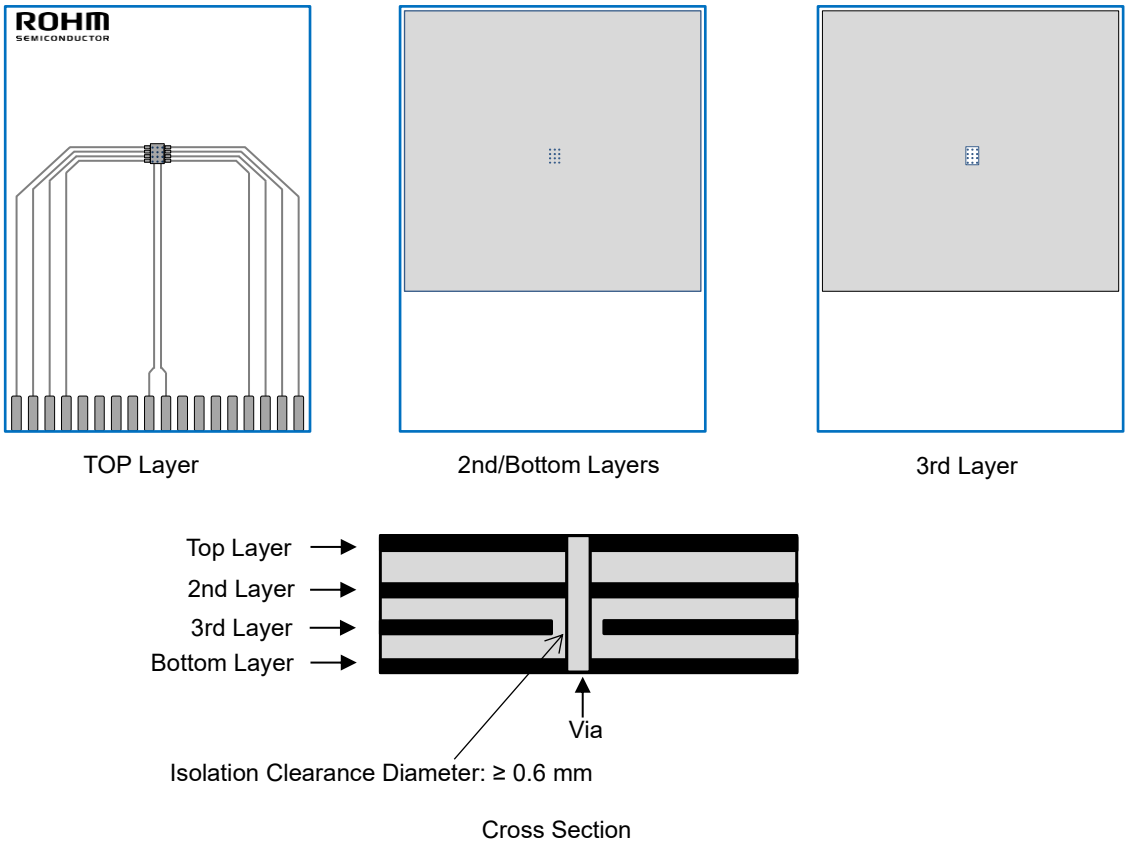


Figure 5. PCB-layout 4-layer (2s2p)

Dimension	Value
Board Finish Thickness	1.60 mm ± 10 %
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top/Bottom Layers)	0.070 mm (Cu +Plating)
Copper Thickness (Inner Layers)	0.035 mm
Thermal Vias Separation/Diameter	1.2 mm/0.3 mm

Thermal Resistance – continued

■ Transient Thermal Resistance (Single Pulse)

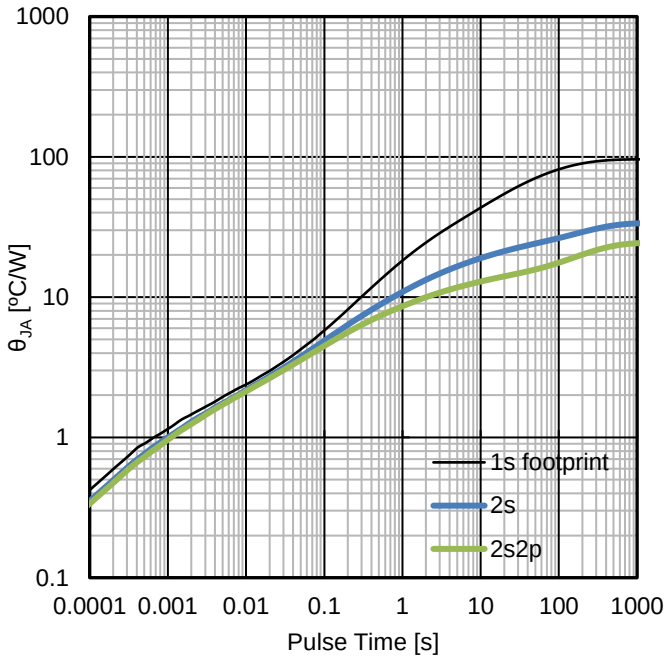


Figure 6. Transient Thermal Resistance

■ Thermal Resistance (θ_{JA} vs Copper Foil area 1s)

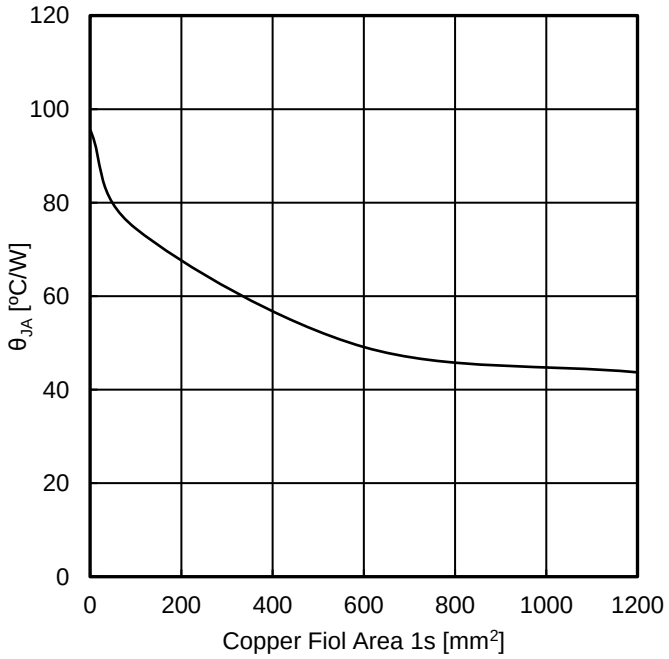


Figure 7. Thermal Resistance

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VX Power Supply Voltage	V_X	6.0	12.0	18.0	V
VS Power Supply Voltage	V_S	6.0	7.0	8.0	V
Operating Temperature	Tj	-40	+25	+150	°C
LDO Output Capacitance	C_{V5O}	68	-	270	µF

Electrical Characteristics (Unless otherwise specified V_X = 6 V to 18 V, V_S = 6V to 8V, Tj = -40 °C to 150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VS Circuit Current	I_{VS}	-	3.0	6.0	mA	V_{IN1} = 0 V
LDO						
V5O Output Voltage	V_{5O}	4.9	5.0	5.1	V	1 mA < I_{V5O} < 250 mA
V5O Over Current Threshold Value	$I_{OCP(V5O)}$	250	500	-	mA	V_{5O} = 4.5 V
Load Regulation	$\Delta V_{5O\text{-}Load}$	-	-	50	mV	1 mA < I_{V5O} < 250 mA
Line Regulation	$\Delta V_{5O\text{-}Line}$	-	-	10	mV	I_{V5O} = 1 mA, 6 V < V_S < 8 V
Low Dropout Voltage	$\Delta V_{5O\text{-}Drop}$	-	200	500	mV	I_{V5O} = 250 mA
Power Supply Ripple Rejection Ratio	PSRR	-	60	-	dB	C_{V5O} = 220 µF, f = 1 kHz
Input (CSB, SCLK, SI, IN1)						
Low Level Input Voltage	V_{IL}	0	-	V_{5O} x 0.2	V	
High Level Input Voltage	V_{IH}	V_{5O} x 0.7	-	V_{5O}	V	
Input Hysteresis Voltage	V_{HYS}	0.2	0.45	0.7	V	
Low Level Input Current 1 (except CSB)	I_{IL1}	-10	0	+10	µA	V_{SCLK}, V_{SI}, V_{IN1} = 0 V
Low Level Input Current 2 (CSB)	I_{IL2}	-100	-50	-25	µA	V_{CSB} = 0 V
High Level Input Current 1 (except CSB)	I_{IH1}	25	50	100	µA	V_{SCLK}, V_{SI}, V_{IN1} = 5 V
High Level Input Current 2 (CSB)	I_{IH2}	-10	0	+10	µA	V_{CSB} = V_{5O}
Serial Out Output						
SO Low Level Output Voltage	V_{SOL}	-	0.15	0.6	V	I_{SO} = 1 mA
SO High Level Output Voltage	V_{SOH}	V_{5O} - 0.6	V_{5O} - 0.3	-	V	I_{SO} = -1 mA
Serial Out Output Leakage Current	$I_{SO(OFF)}$	-5	0	+5	µA	V_{SO} = 0 V / 5 V
Power MOS Output OUT1, OUT2, OUT3						
Output On Resistance	$R_{DS(ON)123}$	-	200	250	mΩ	I_{OUT} = 1 A, Tj = 25 °C
		-	300	375	mΩ	I_{OUT} = 1 A, Tj = 150 °C
Output Sink Current During OLD	I_{OLD}	15	40	90	µA	V_{OUT} = 24 V
Turn-On Time	t_{ON123}	-	6	12	µs	R_L = 24 Ω, V_{BAT} = 12 V
Turn-Off Time	t_{OFF123}	-	6	12	µs	R_L = 24 Ω, V_{BAT} = 12 V
Slew Rate (On)	SR_{ON123}	1.3	2.5	4.0	V/µs	R_L = 24 Ω, V_{BAT} = 12 V
Slew Rate (Off)	SR_{OFF123}	2.0	3.5	6.0	V/µs	R_L = 24 Ω, V_{BAT} = 12 V
Output Clamp Voltage	V_{CL123}	30	35	40	V	I_{OUT} = 1 mA (Output Off)
Power MOS Output OUT1, OUT2, OUT3 Protection Circuit						
Over Current Threshold Value	I_{OCP123}	2	3.5	5.5	A	
Over Current Detection Time	t_{OCP123}	22	45	90	µs	
Open Load Detection Release Voltage	$V_{OLD(OFF)}$	1.2	2.5	3.5	V	Output Off Setting
Open Load Detection Detect Voltage	$V_{OLD(ON)}$	1.0	2.0	3.1	V	Output Off Setting
Output Overhead Detection Detect Voltage	$V_{OFD(ON)}$	1.2	2.5	3.5	V	Output On Setting
Output Overhead Detection Release Voltage	$V_{OFD(OFF)}$	1.0	2.0	3.1	V	Output On Setting

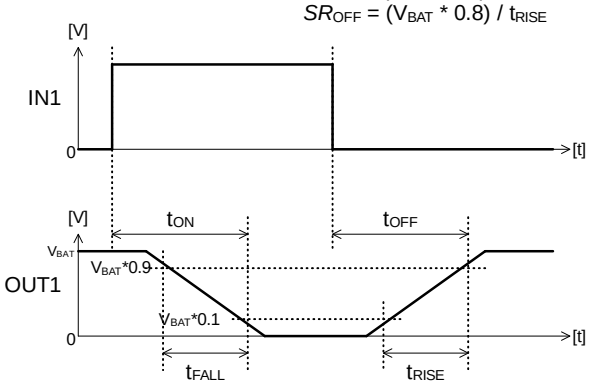
Electrical Characteristics – continued (Unless otherwise specified V_X = 6 V to 18 V, V_S = 6V to 8V, Tj = -40 °C to 150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power MOS Output OUT4, OUT5						
Output On Resistance	$R_{DS(ON)45}$	-	540	675	mΩ	I_{OUT} = 0.2 A, Tj = 25 °C
		-	880	1100	mΩ	I_{OUT} = 0.2 A, Tj = 150 °C
Output Leakage Current	$I_{OUT(L)45}$	-	0	1	µA	V_{OUT} = 24 V, Tj = 25 °C
		-	0.5	3	µA	V_{OUT} = 24 V, Tj = 150 °C
Turn-On Time	t_{ON45}	-	15	25	µs	R_L = 60 Ω, V_{BAT} = 12 V
Turn-Off Time	t_{OFF45}	-	30	50	µs	R_L = 60 Ω, V_{BAT} = 12 V
Slew Rate (On)	SR_{ON45}	0.4	1.0	2.2	V/µs	R_L = 60 Ω, V_{BAT} = 12 V
Slew Rate (Off)	SR_{OFF45}	0.4	1.0	2.2	V/µs	R_L = 60 Ω, V_{BAT} = 12 V
Output Clamp Voltage	V_{CL45}	30	35	40	V	I_{OUT} = 1 mA (Output Off)
Power MOS Output OUT4, OUT5 Protection Circuit						
Over Current Threshold Value	I_{OCP45}	0.5	0.9	1.4	A	
Over Current Detection Time	t_{OCP45}	22	45	90	µs	
K-LINE						
VX Circuit Current	I_{VX}	-	0.03	0.10	mA	V_{TX} = 0 V
RX Low Level Output Voltage	V_{RXL}	-	-	0.4	V	I_{RX} = 1 mA
RX High Level Output Voltage	V_{RXH}	V_{5O} - 0.4	-	-	V	I_{RX} = -1 mA
RX Output Delay Time	t_{RXD}	-	-	2	µs	
TX Low Level Input Voltage	$V_{IL(TX)}$	0	-	V_{5O} x 0.2	V	
TX High Level Input Voltage	$V_{IH(TX)}$	V_{5O} x 0.7	-	V_{5O}	V	
TX Input Hysteresis Voltage	$V_{HYS(TX)}$	0.1	0.3	0.5	V	
TX Pull-up Resistor	R_{TX}	5	10	20	kΩ	
KIO Low Level Output Voltage	V_{KIOL}	-	-	1.4	V	R_{KIO} = 480 Ω
KIO Output Leakage Current	$I_{KIO(L)}$	-	0	3	µA	V_{KIO} = 18 V
KIO Over Current Threshold Value	$I_{OCP(KIO)}$	40	-	140	mA	
KIO Output Delay Time	t_{KIOD}	-	-	2	µs	R_{KIO} = 480 Ω

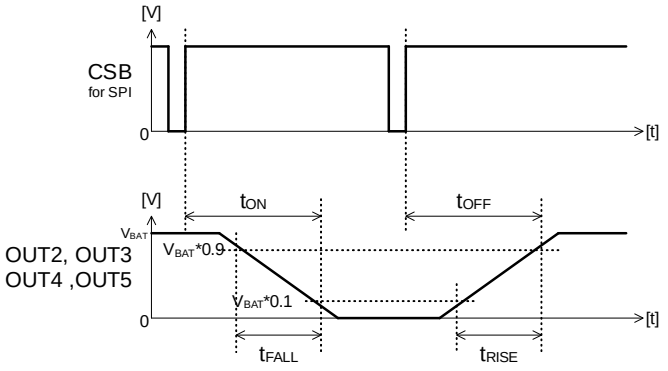
Switching Time Measurement Waveform

OUT1 (Control by IN1)

SR_{ON} = (V_{BAT} * 0.8) / t_{FALL}
SR_{OFF} = (V_{BAT} * 0.8) / t_{RISE}



OUT2, OUT3, OUT4, OUT5 (Control by SPI)



Typical Performance Curves

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

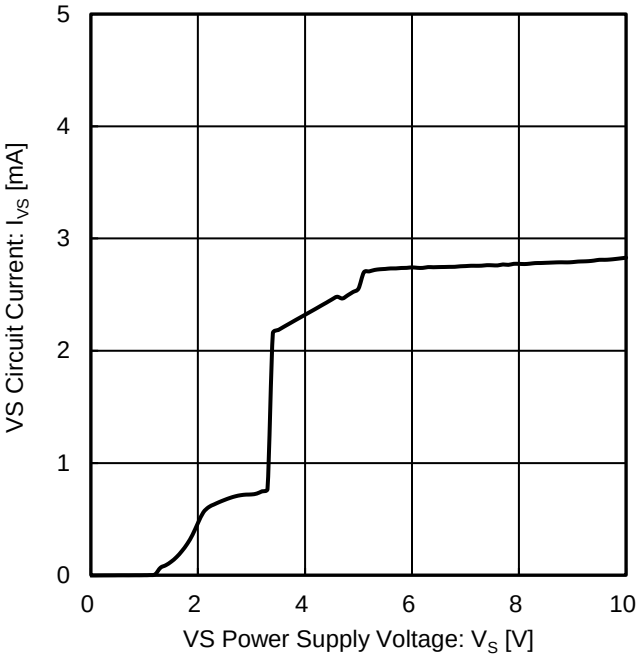


Figure 8. VS Circuit Current vs VS Power Supply Voltage

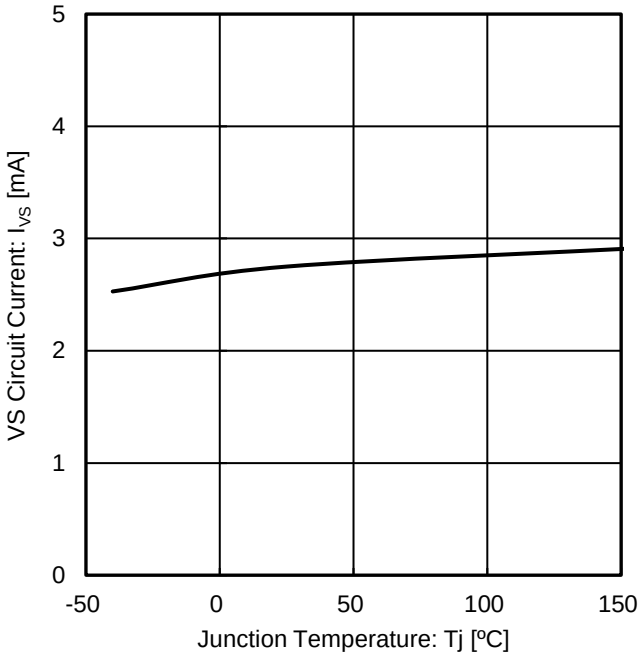


Figure 9. VS Circuit Current vs Junction Temperature

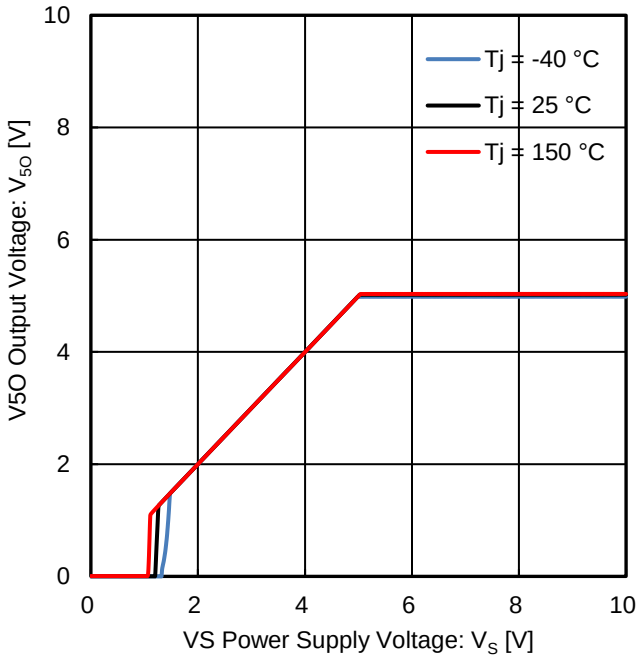


Figure 10. V5O Output voltage vs VS Power Supply Voltage

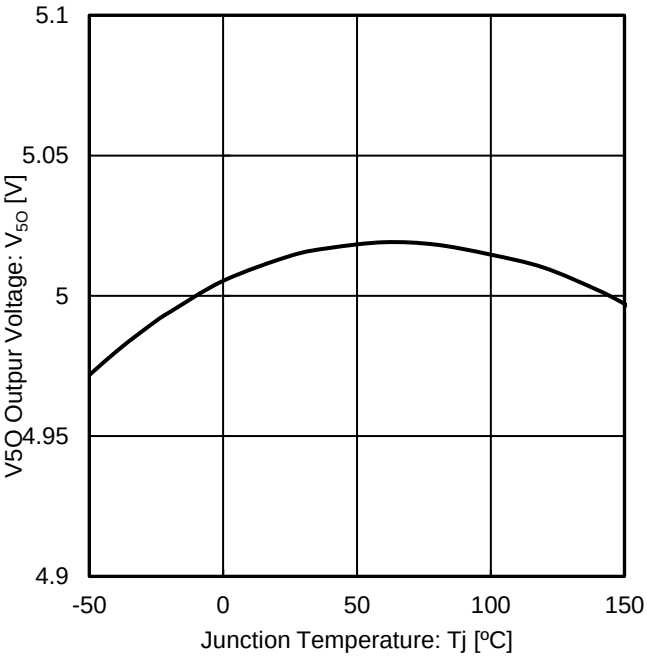


Figure 11. V5O Output voltage vs Junction Temperature

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

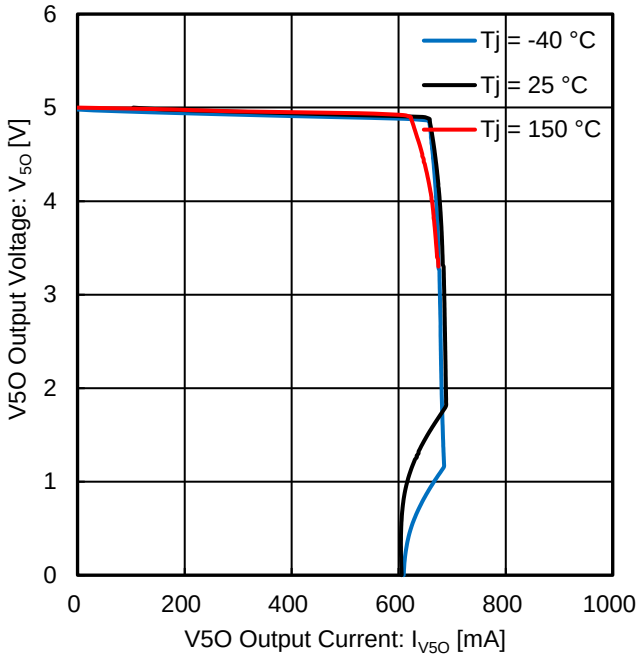


Figure 12. V5O Output voltage vs V5O Output Current

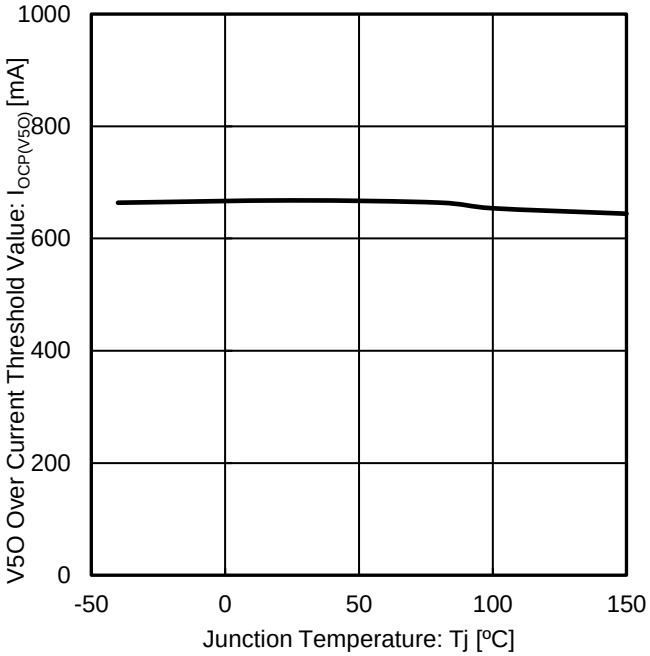


Figure 13. V5O Over Current Threshold Value vs Junction Temperature

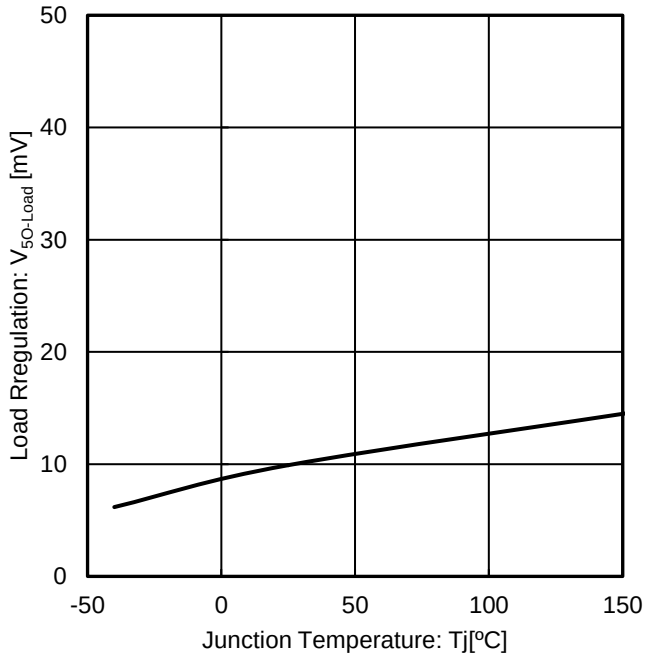


Figure 14. Load Regulation vs Junction Temperature

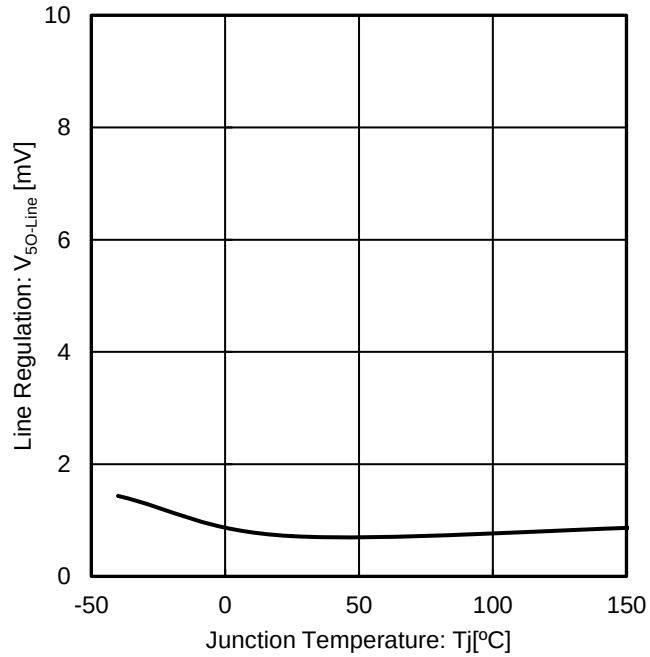


Figure 15. Line Regulation vs Junction Temperature

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

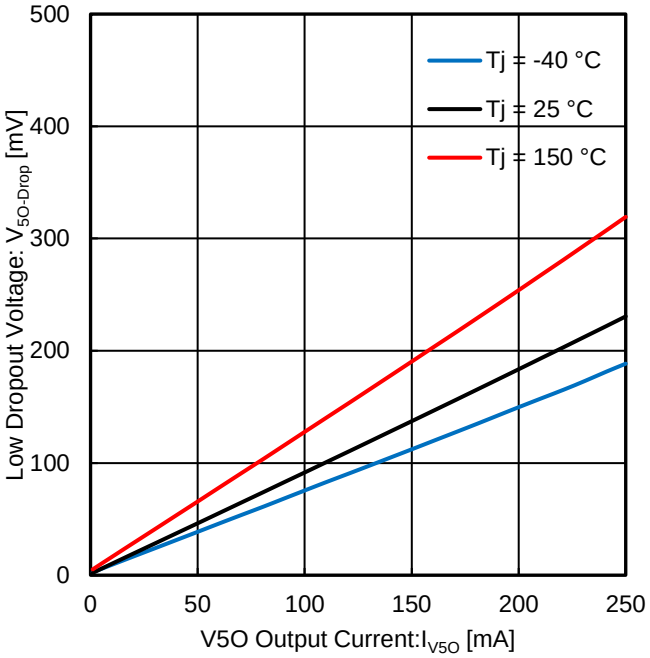


Figure 16. Low Dropout Voltage vs V5O Output Current

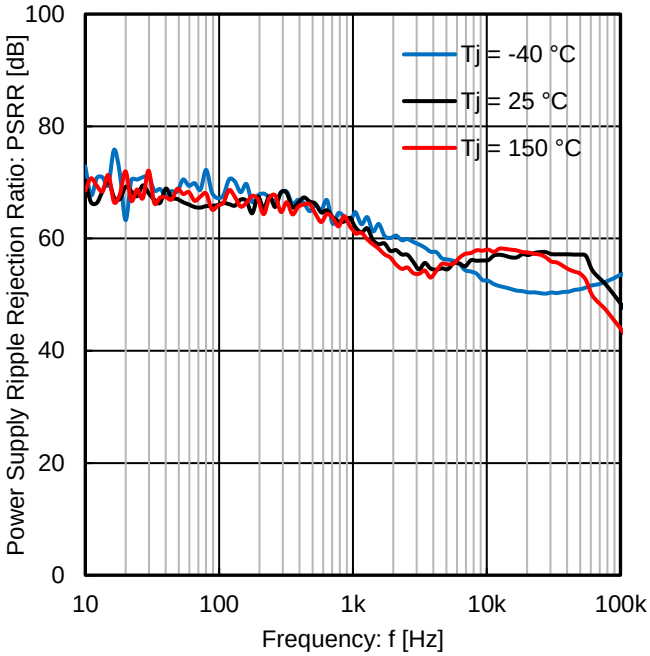


Figure 17. Power Supply Ripple Rejection Ratio vs Frequency

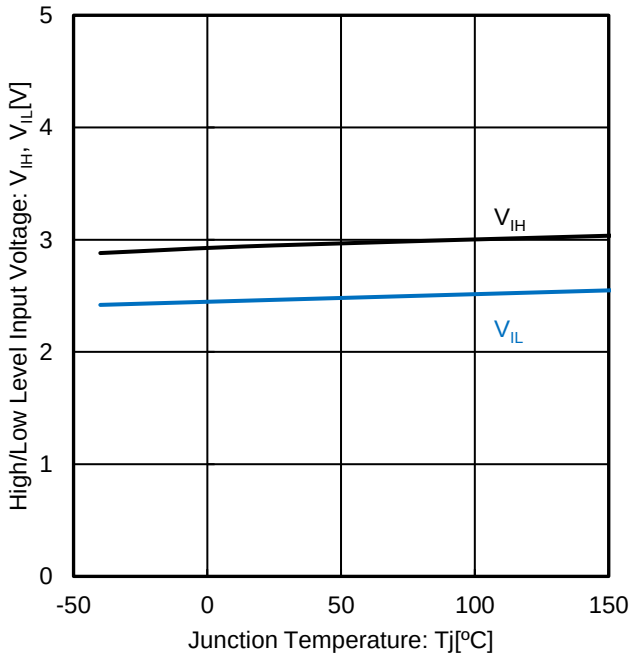


Figure 18. High Level Input Voltage / Low Level Input Voltage vs Junction Temperature

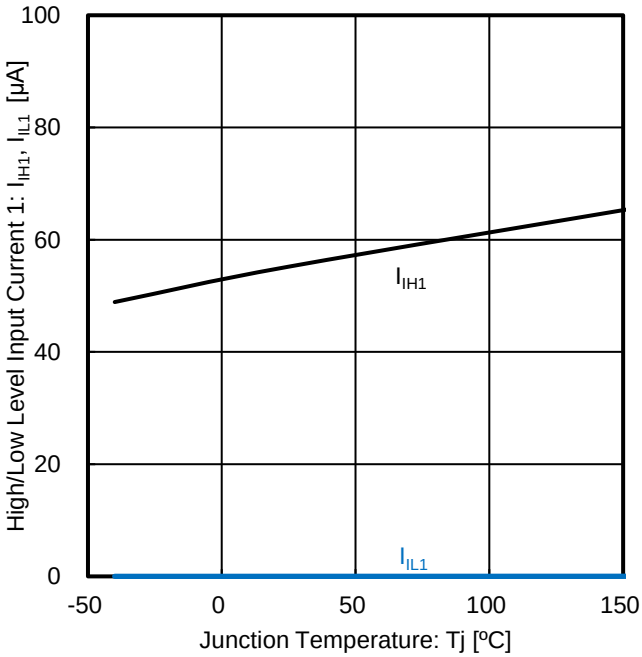


Figure 19. High Level Input Current 1 / Low Level Input Current 1 vs Junction Temperature

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

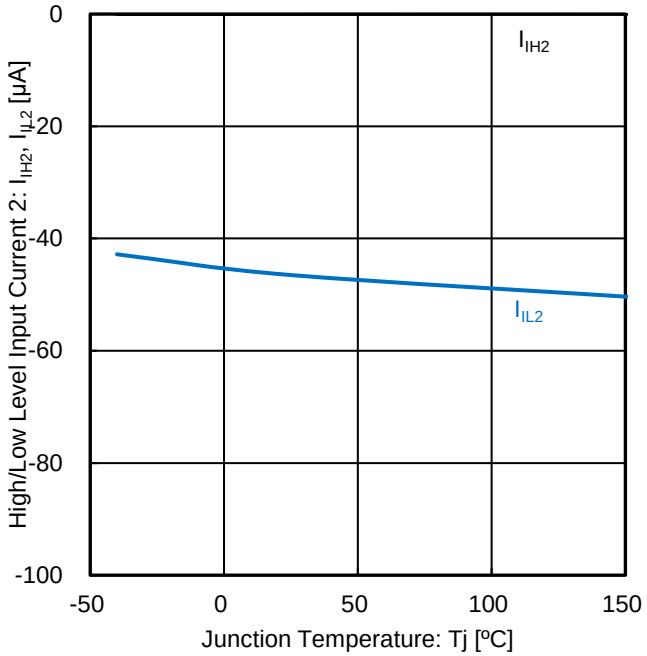


Figure 20. High Level Input Current 2 / Low Level Input Current 2 vs Junction Temperature

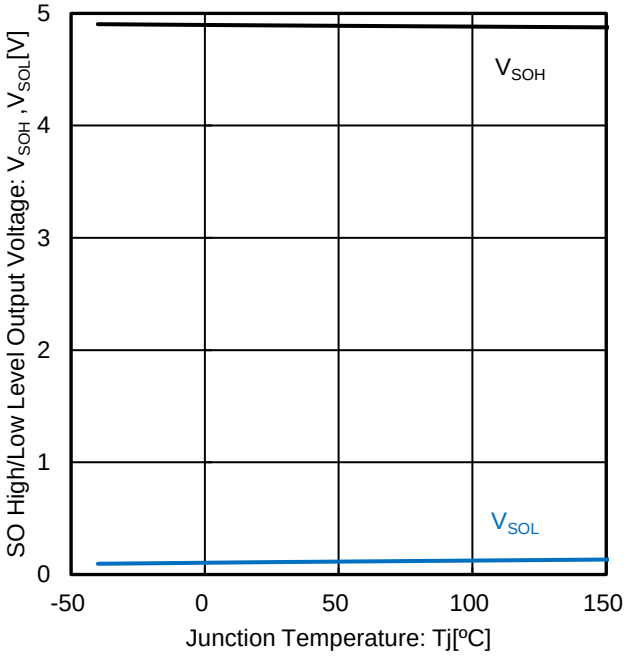


Figure 21. SO High Level Output Voltage / SO Low Level Output Voltage vs Junction Temperature

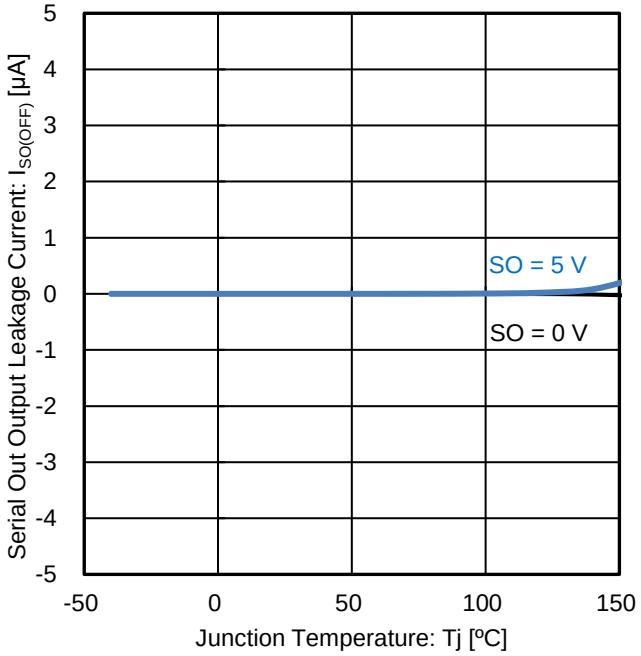


Figure 22. Serial Out Output Leakage Current vs Junction Temperature

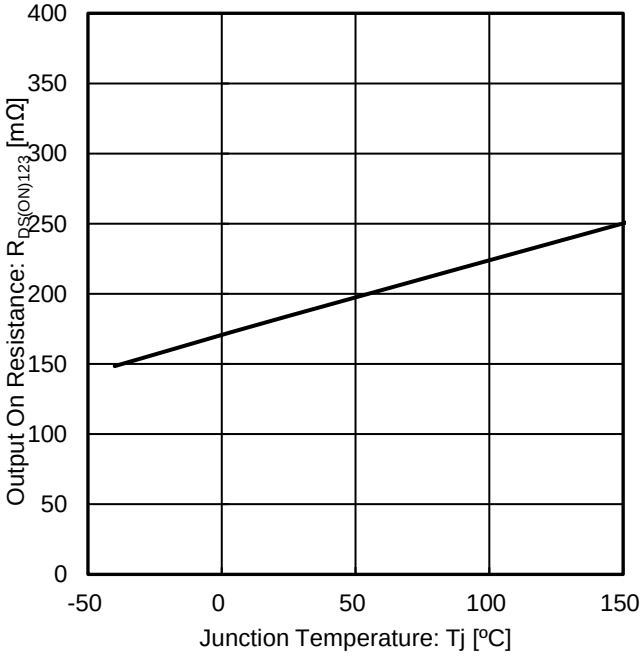


Figure 23. Output On Resistance vs Junction Temperature (OUT1, OUT2, OUT3)

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

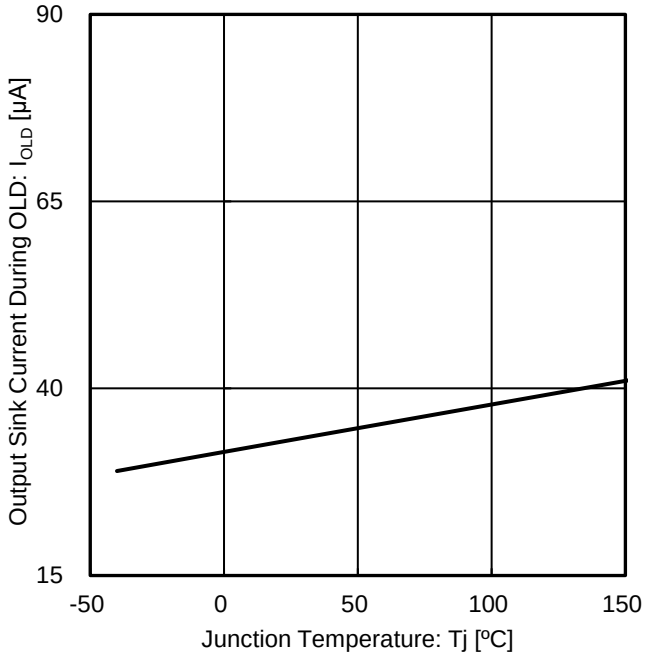


Figure 24. Output Sink Current During OLD vs Junction Temperature

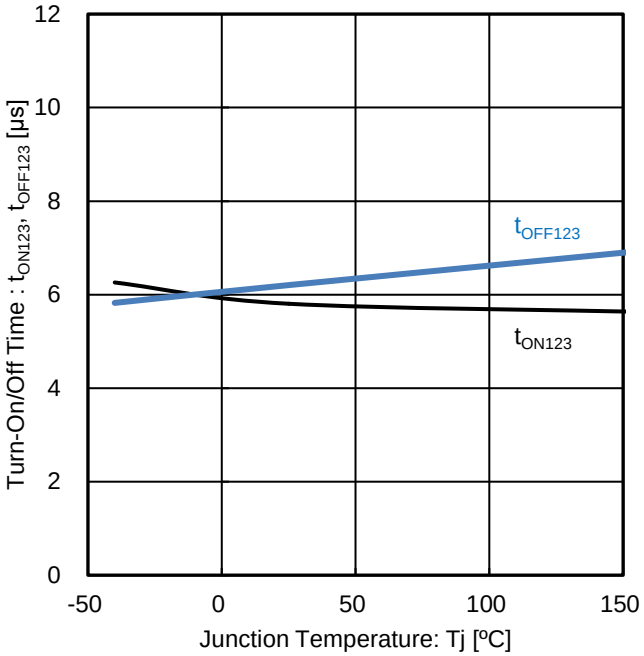


Figure 25. Turn-On Time / Turn-Off Time vs Junction Temperature (OUT1, OUT2, OUT3)

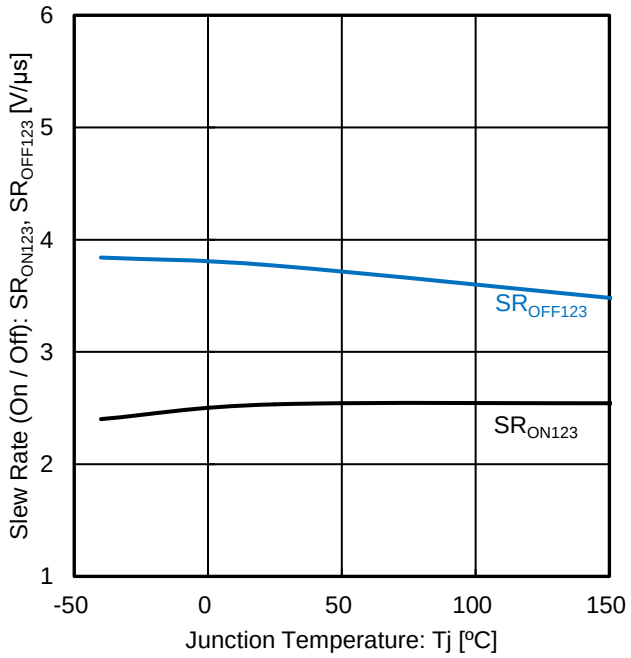


Figure 26. Slew Rate (On) / Slew Rate (Off) vs Junction Temperature (OUT1, OUT2, OUT3)

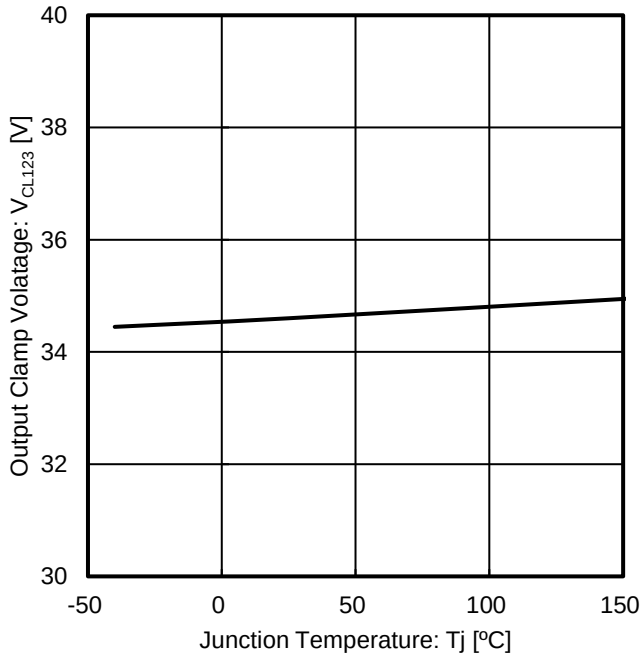


Figure 27. Output Clamp Voltage vs Junction Temperature (OUT1, OUT2, OUT3)

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

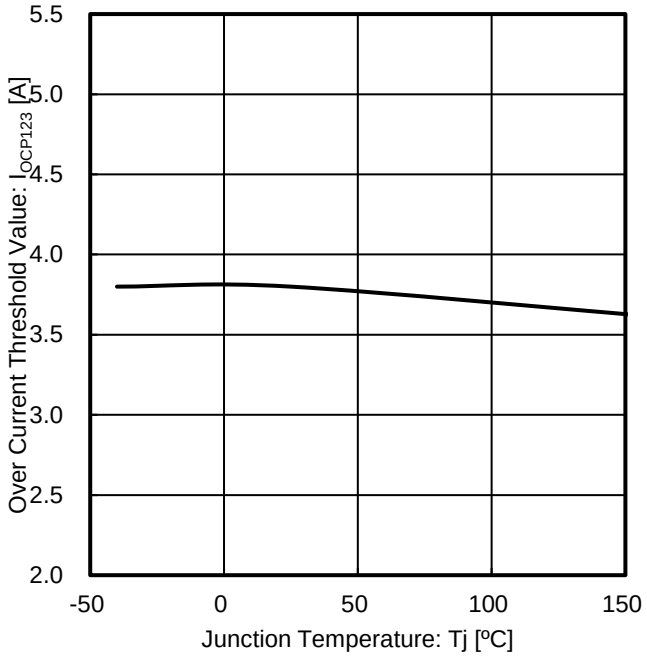


Figure 28. Over Current Threshold Value vs Junction Temperature
(OUT1, OUT2, OUT3)

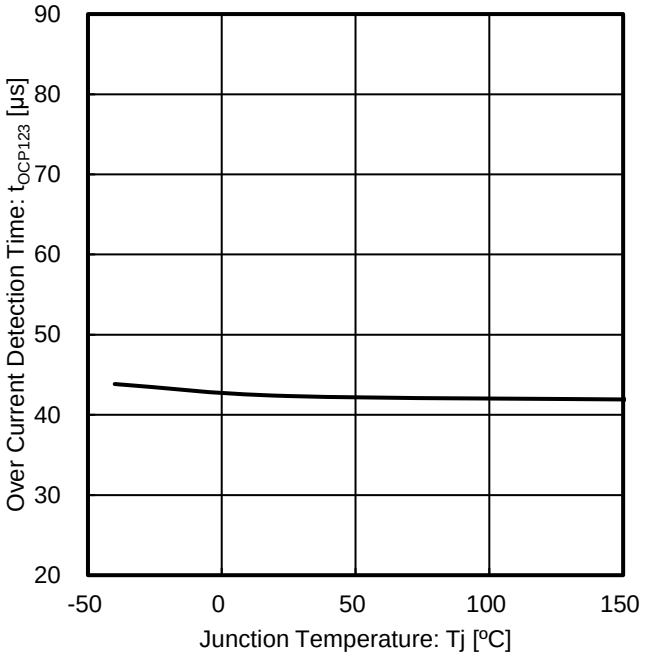


Figure 29. Over Current Detection Time vs Junction Temperature
(OUT1, OUT2, OUT3)

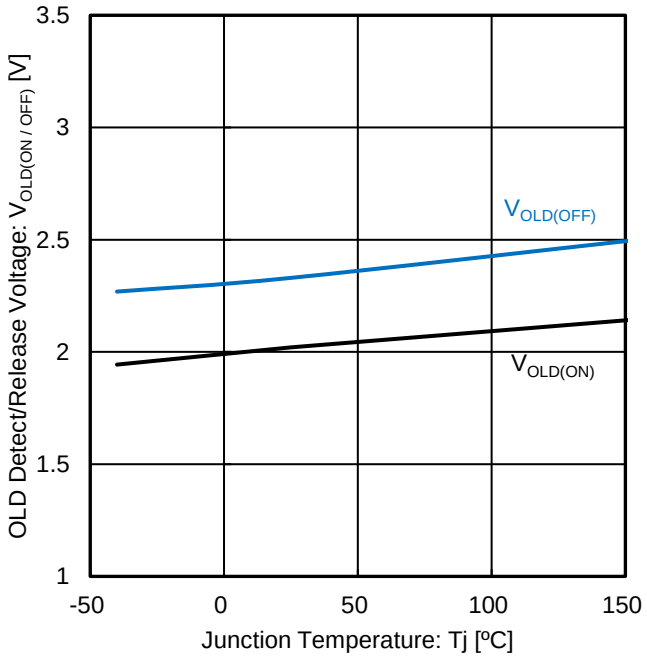


Figure 30. Open Load Detection Detect Voltage / Open Load Detection Release Voltage
vs Junction Temperature

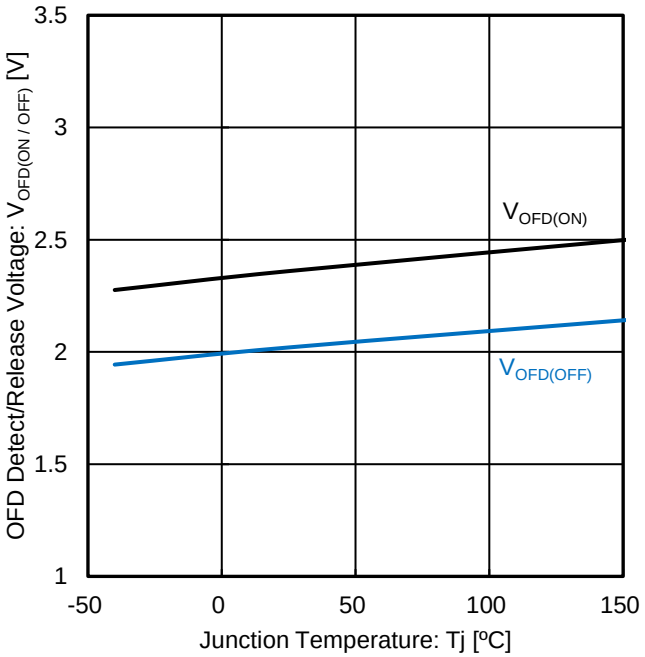


Figure 31. Output Overhead Detection Detect Voltage / Output Overhead Detection Release Voltage
vs Junction Temperature

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

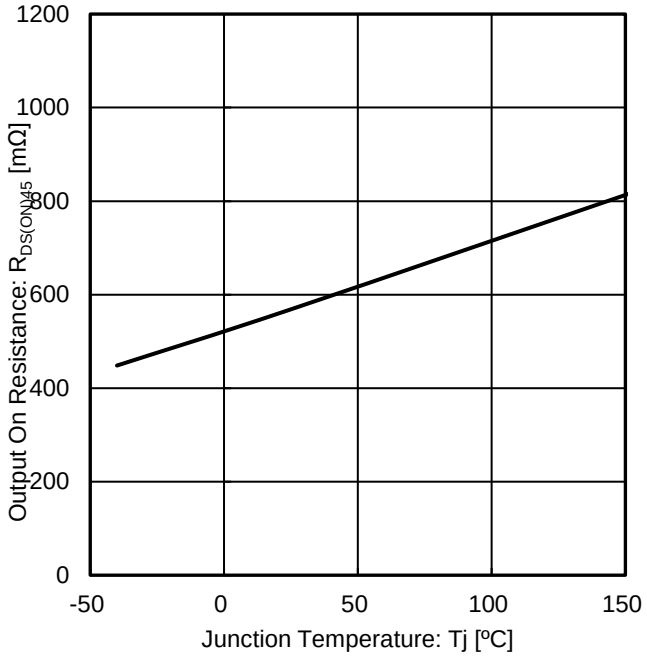


Figure 32. Output On Resistance vs Junction Temperature (OUT4, OUT5)

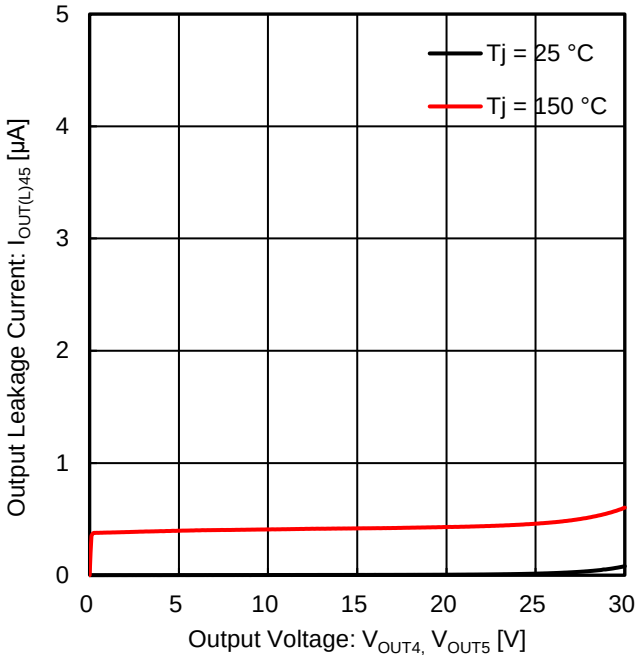


Figure 33. Output Leakage Current vs Output Voltage (OUT4, OUT5)

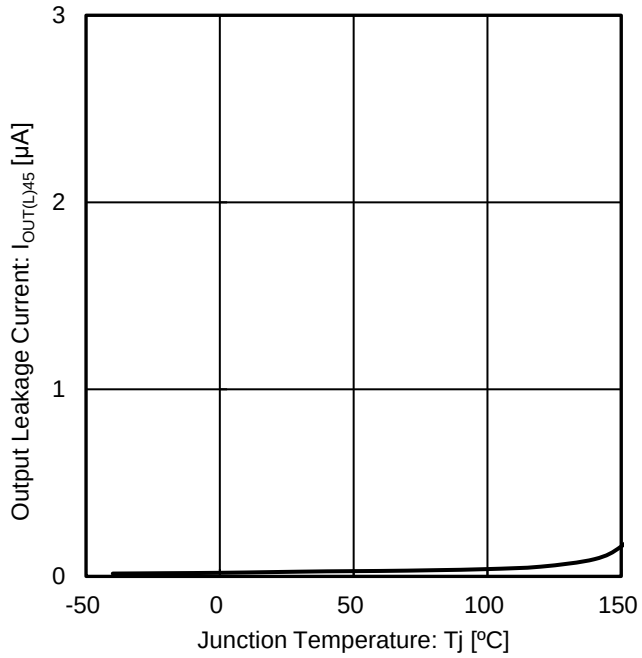


Figure 34. Output Leakage Current vs Junction Temperature (OUT4, OUT5)

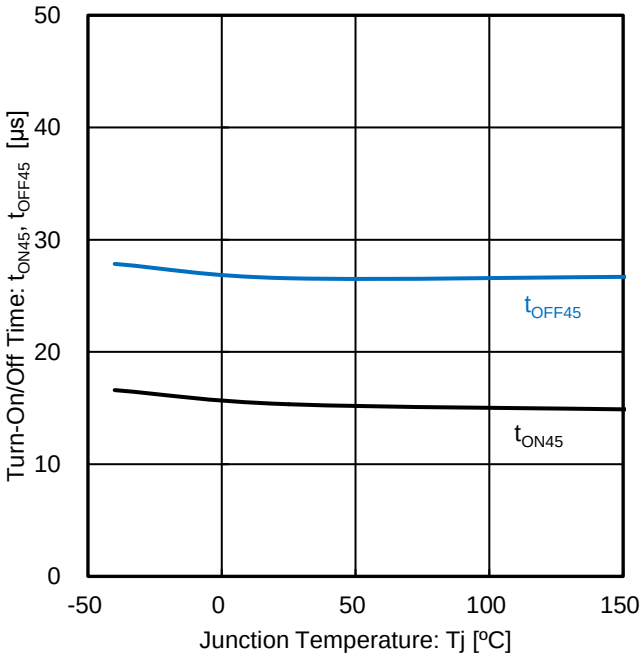


Figure 35. Turn-On Time / Turn-Off Time vs Junction Temperature (OUT4, OUT5)

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

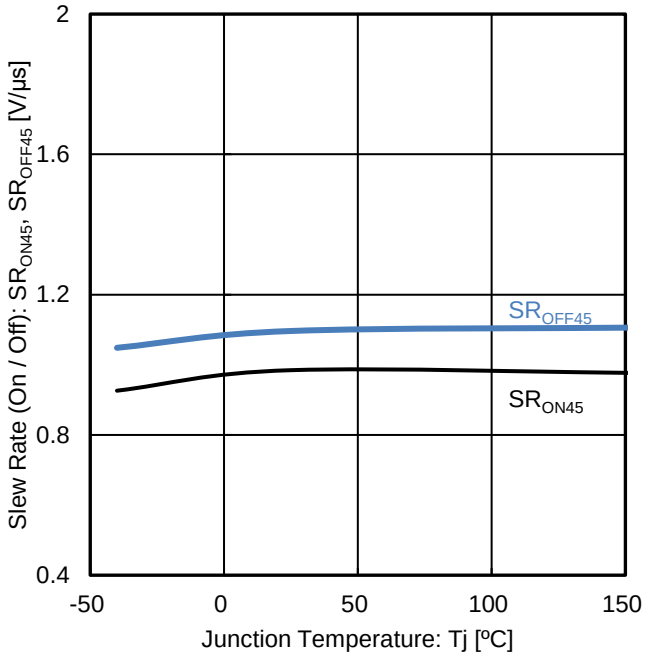


Figure 36. Slew Rate (On) / Slew Rate (Off) vs Junction Temperature (OUT4, OUT5)

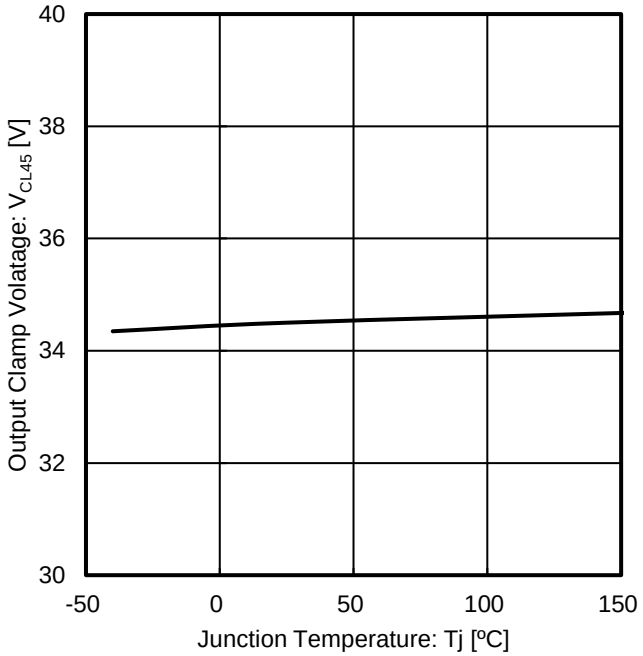


Figure 37. Output Clamp Voltage vs Junction Temperature (OUT4, OUT5)

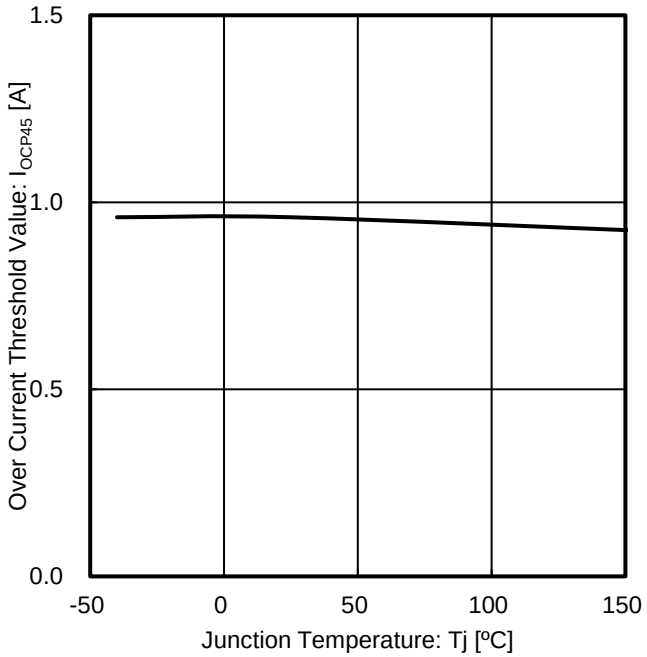


Figure 38. Over Current Threshold Value vs Junction Temperature (OUT4, OUT5)

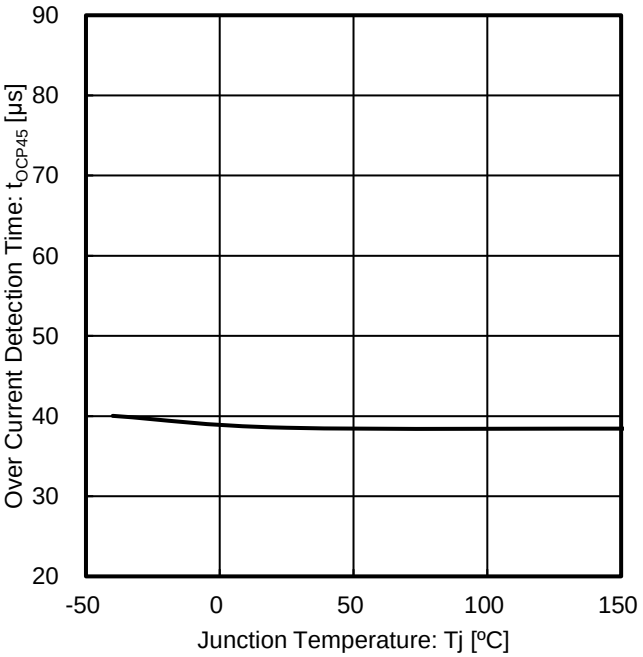


Figure 39. Over Current Detection Time vs Junction Temperature (OUT4, OUT5)

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

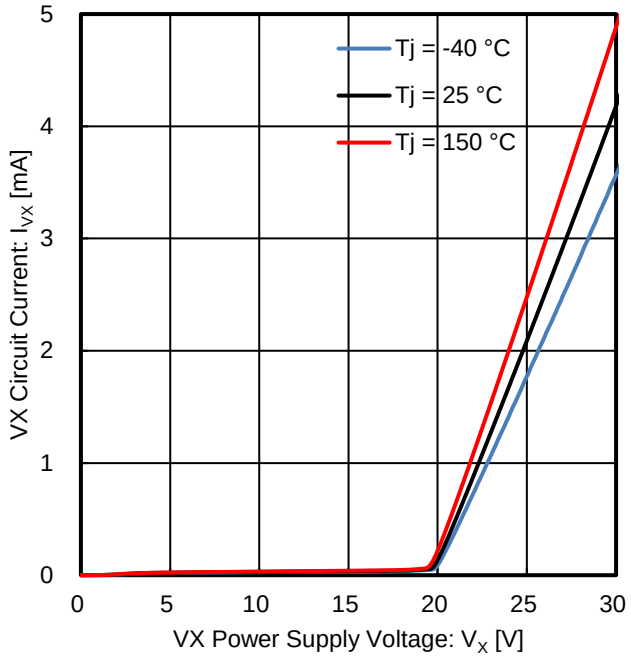


Figure 40. VX Circuit Current vs VX Power Supply Voltage

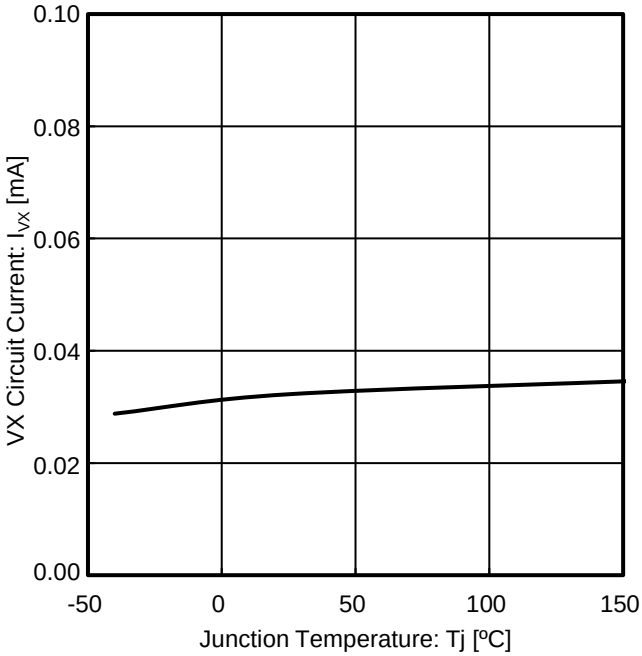


Figure 41. VX Circuit Current vs Junction Temperature

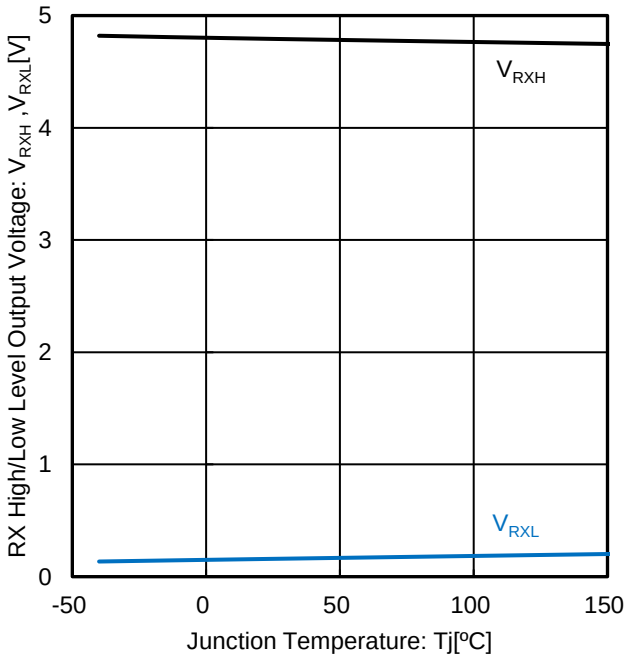


Figure 42. RX High Level Output Voltage / RX Low Level Output Voltage vs Junction Temperature

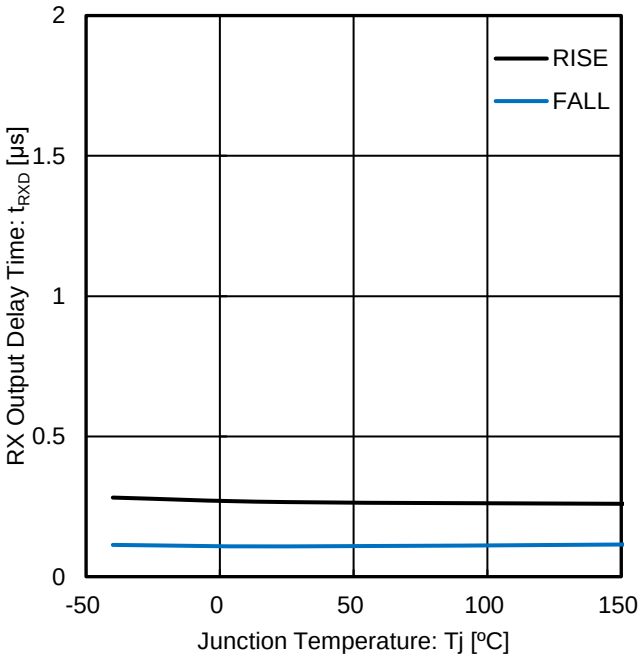


Figure 43. RX Output Delay Time vs Junction Temperature

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

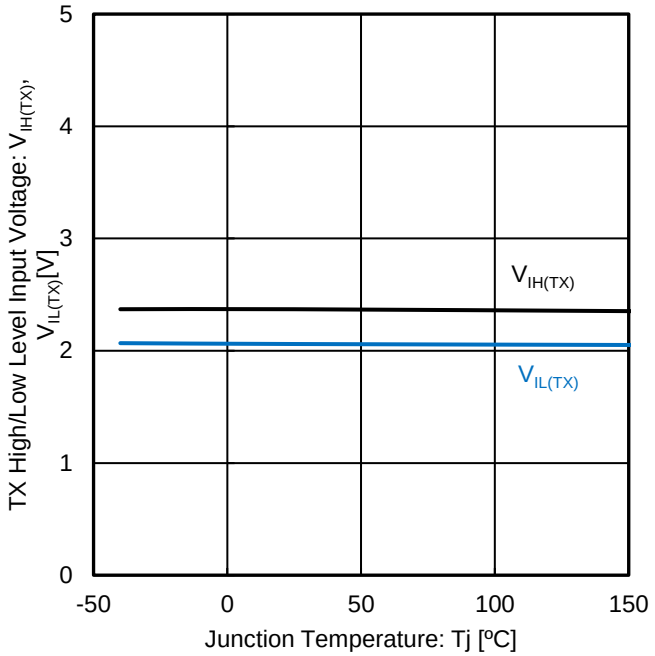


Figure 44. TX High Level Input Voltage / TX Low Level Input Voltage vs Junction Temperature

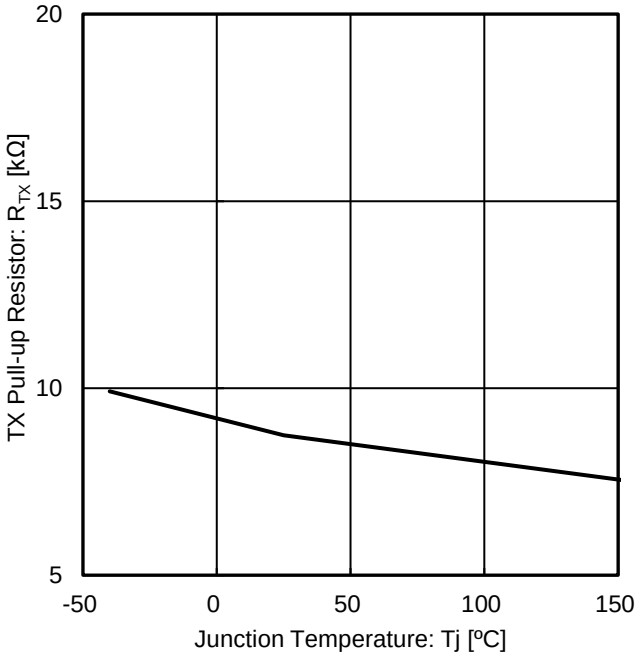


Figure 45. TX Pull-up Resistor vs Junction Temperature

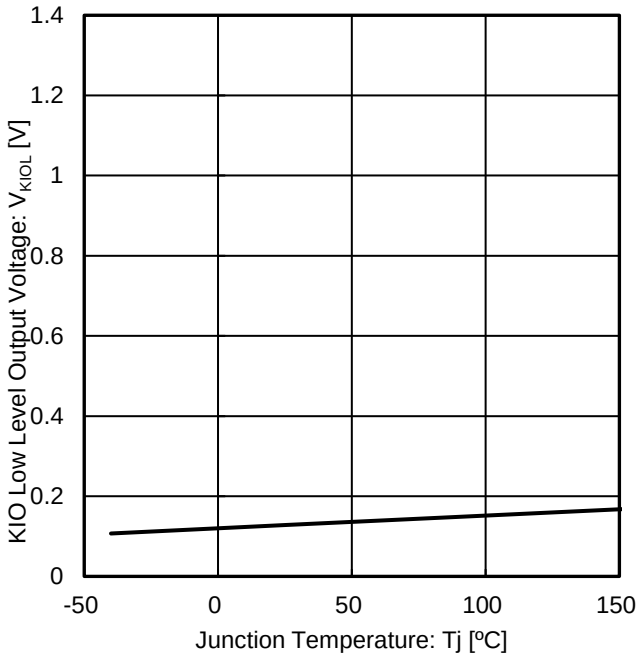


Figure 46. KIO Low Level Output Voltage vs Junction Temperature

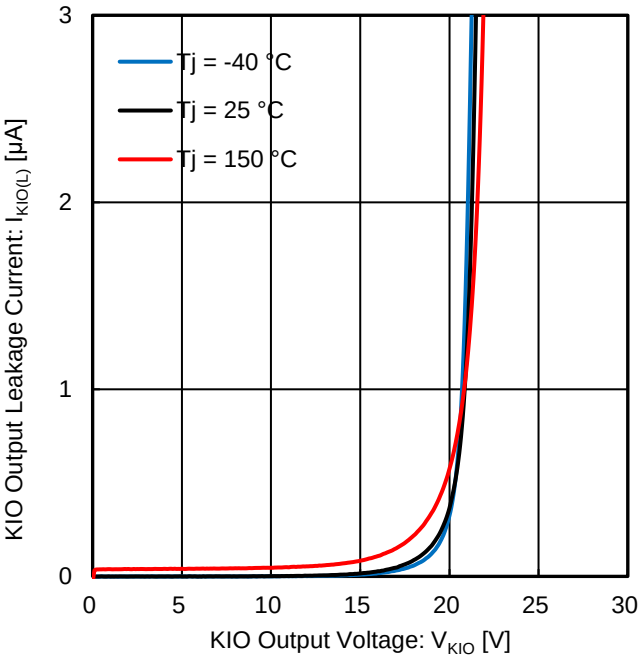


Figure 47. KIO Output Leakage Current vs KIO Output Voltage

Typical Performance Curves – continued

(Reference data) (Unless otherwise specified, V_X = 12 V, V_S = 7 V, Tj = 25 °C)

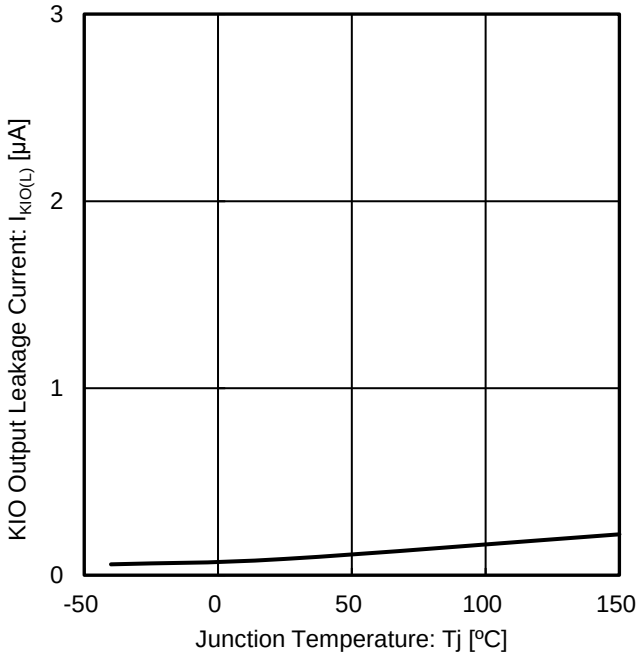


Figure 48. KIO Output Leakage Current vs Junction Temperature

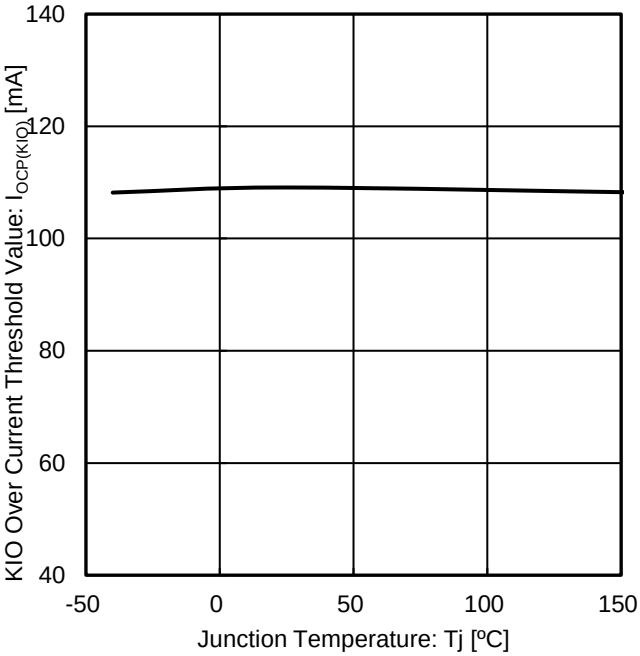


Figure 49. KIO Over Current Threshold Value vs Junction Temperature

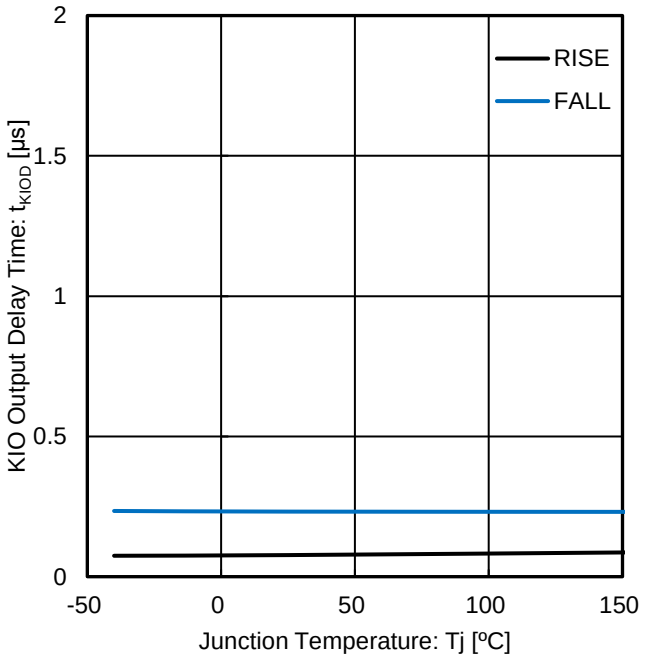


Figure 50. KIO Output Delay Time vs Junction Temperature

Measurement Circuits

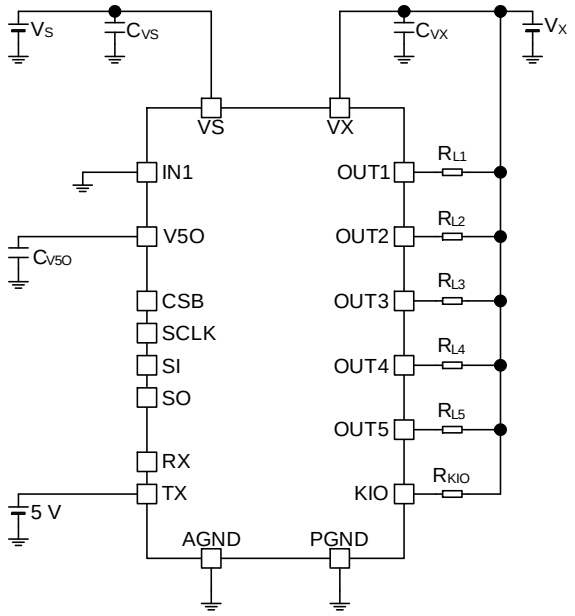


Figure 51.
VS Circuit Current
VX Circuit Current

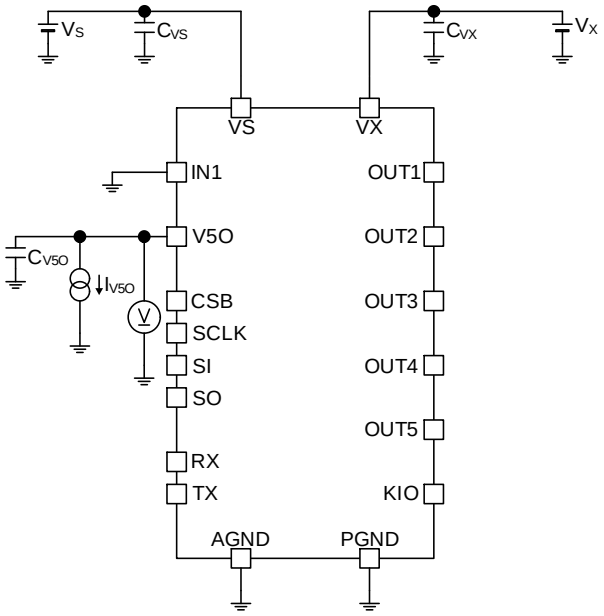


Figure 52.
V5O Output voltage
Load Regulation
Line Regulation
Low Dropout Voltage

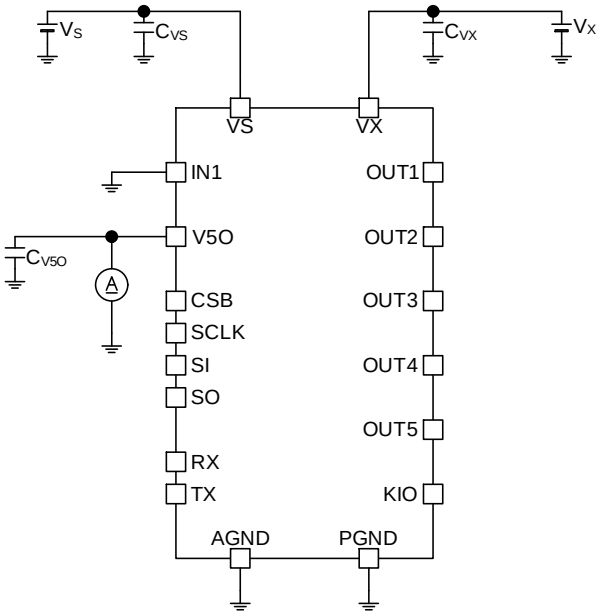


Figure 53.
V5O Over Current Threshold Value

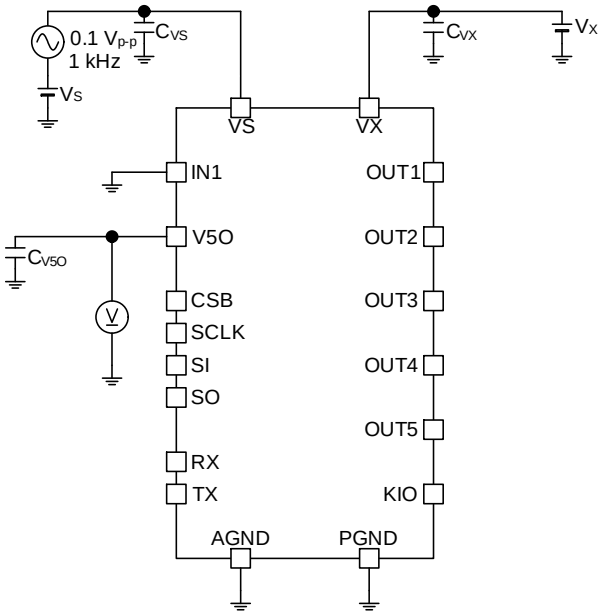


Figure 54.
Power Supply Ripple Rejection Ratio

Measurement Circuits – continued

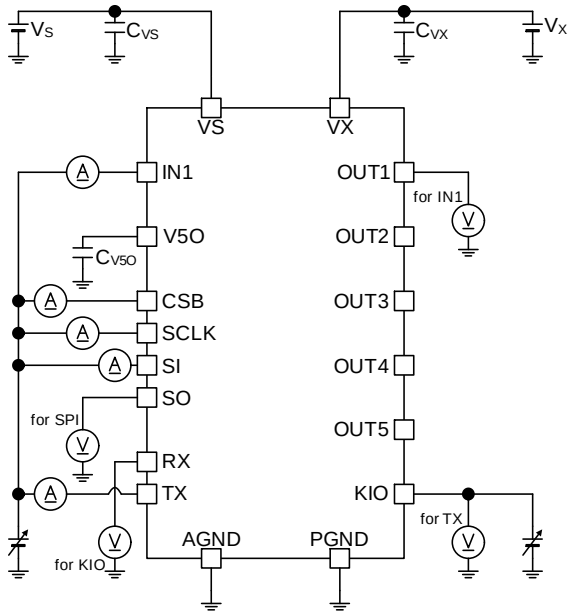


Figure 55.
High Level Input Voltage
Low Level Input Voltage
Input Hysteresis Voltage
High Level Input Current 1
Low Level Input Current 1
High Level Input Current 2
Low Level Input Current 2
TX Pull-up Resistor

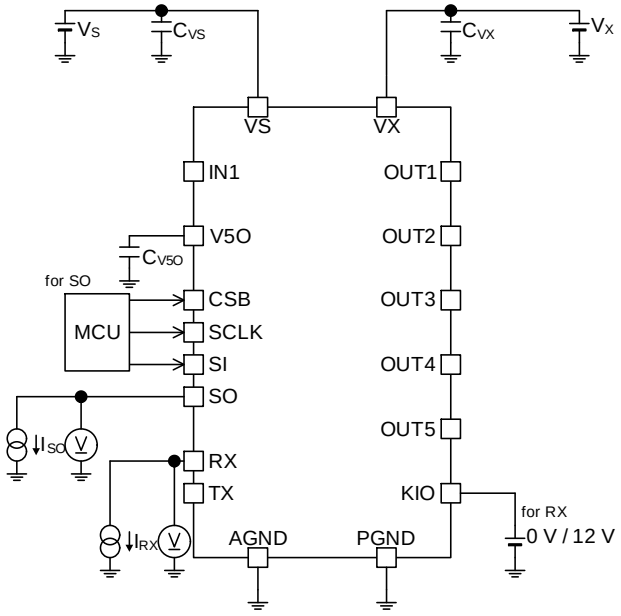


Figure 56.
SO High Level Output Voltage
SO Low Level Output Voltage
RX High Level Output Voltage
RX Low Level Output Voltage

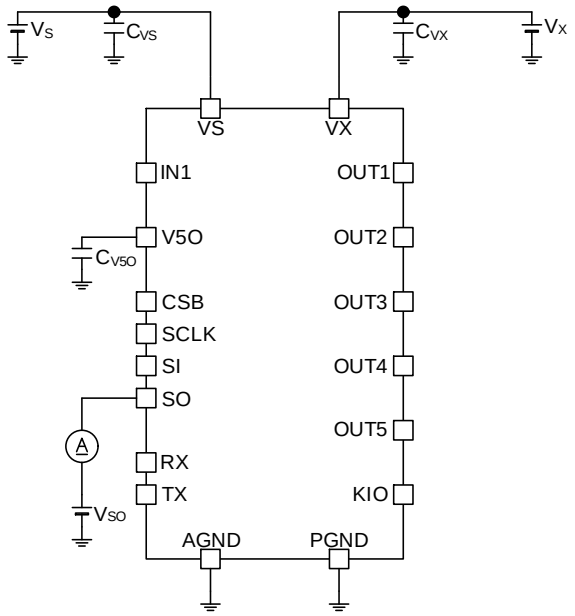


Figure 57.
Serial Out Output Leakage Current

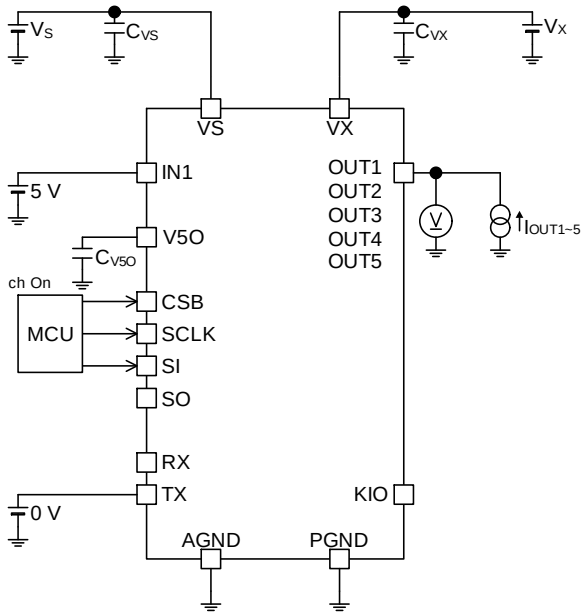


Figure 58.
Output On Resistance

Measurement Circuits – continued

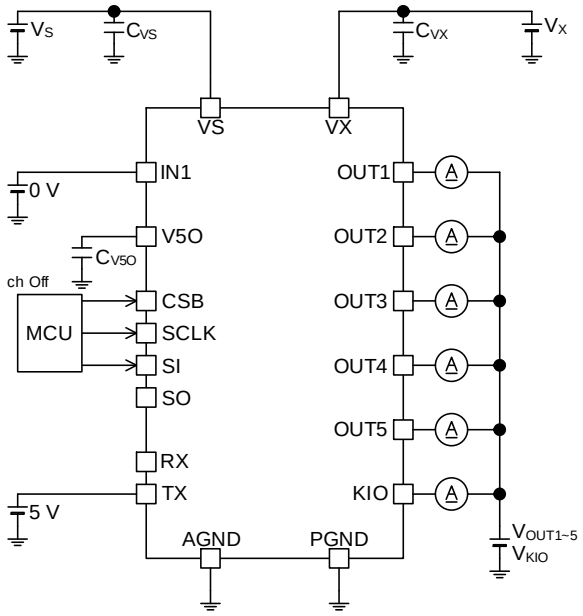


Figure 59.
Output Sink Current During OLD
Output Leakage Current
KIO Output Leakage Current

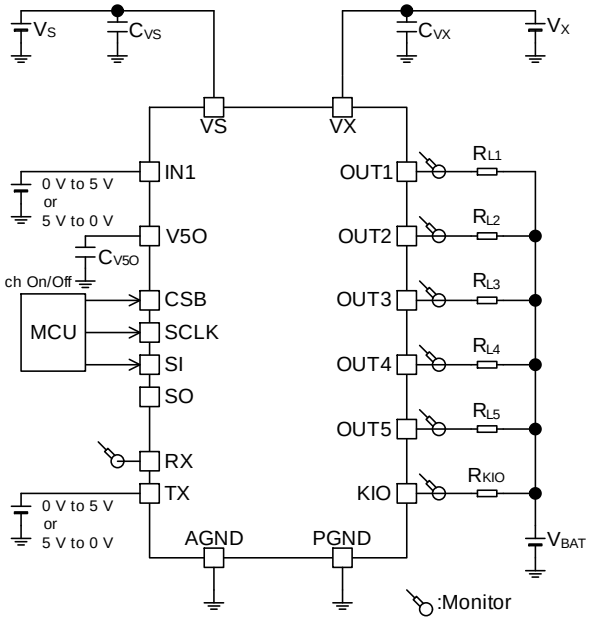


Figure 60.
Turn-On Time
Turn-Off Time
Slew Rate (On)
Slew Rate (Off)
RX Output Delay Time
KIO Output Delay Time

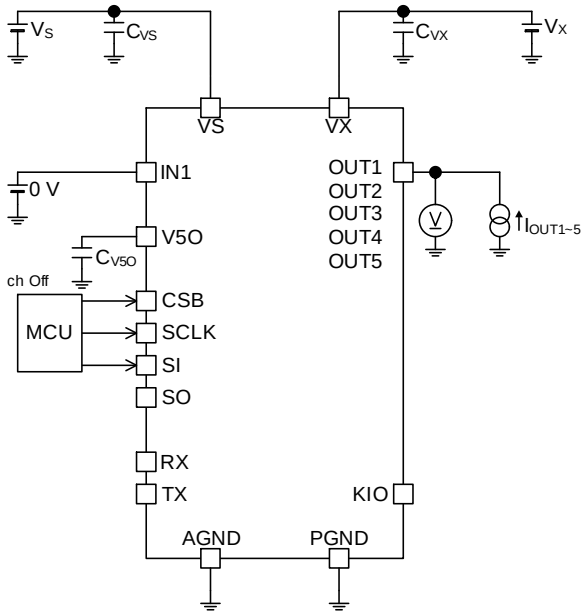


Figure 61.
Output Clamp Voltage

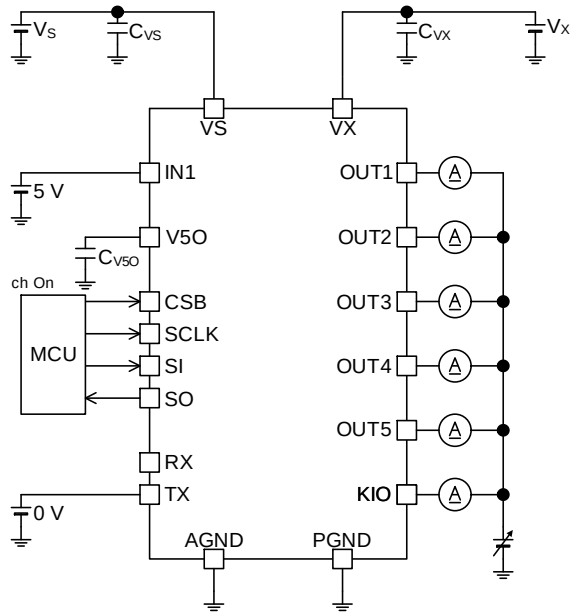


Figure 62.
Over Current Threshold Value
Over Current Detection Time
KIO Over Current Threshold Value

Measurement Circuits – continued

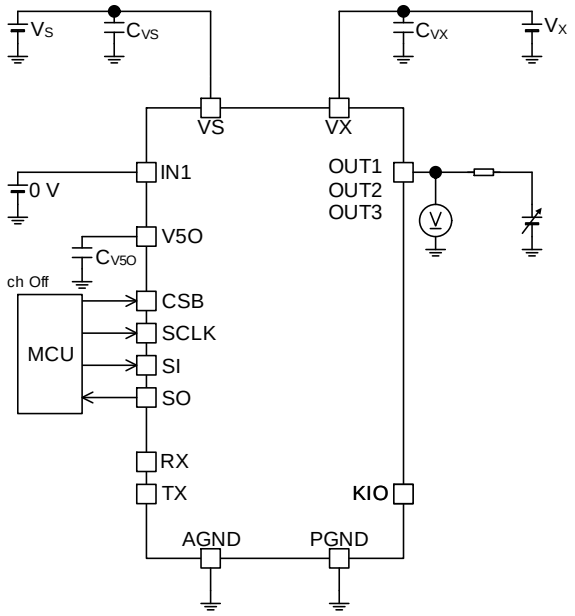


Figure 63.
Open Load Detection Detect Voltage
Open Load Detection Release Voltage

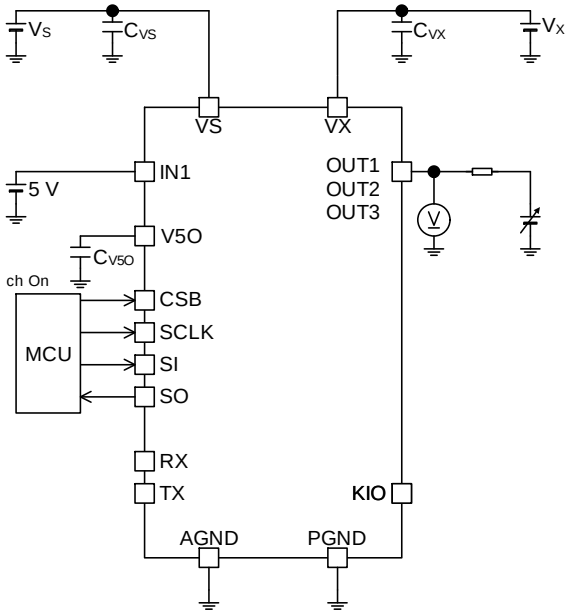


Figure 64.
Output Overhead Detection Detect Voltage
Output Overhead Detection Release Voltage

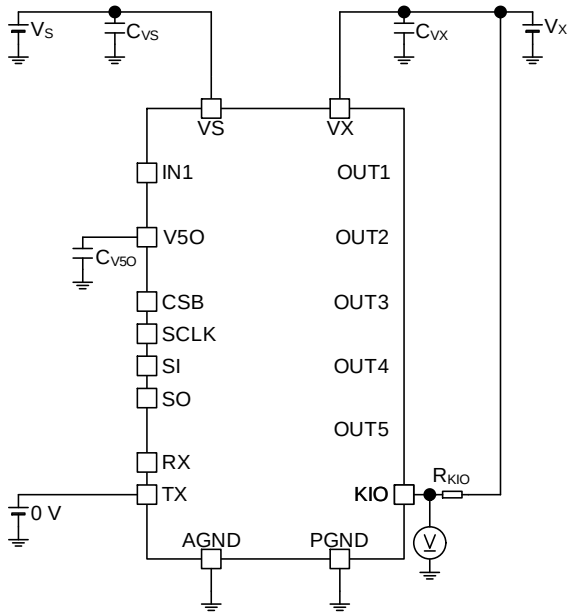
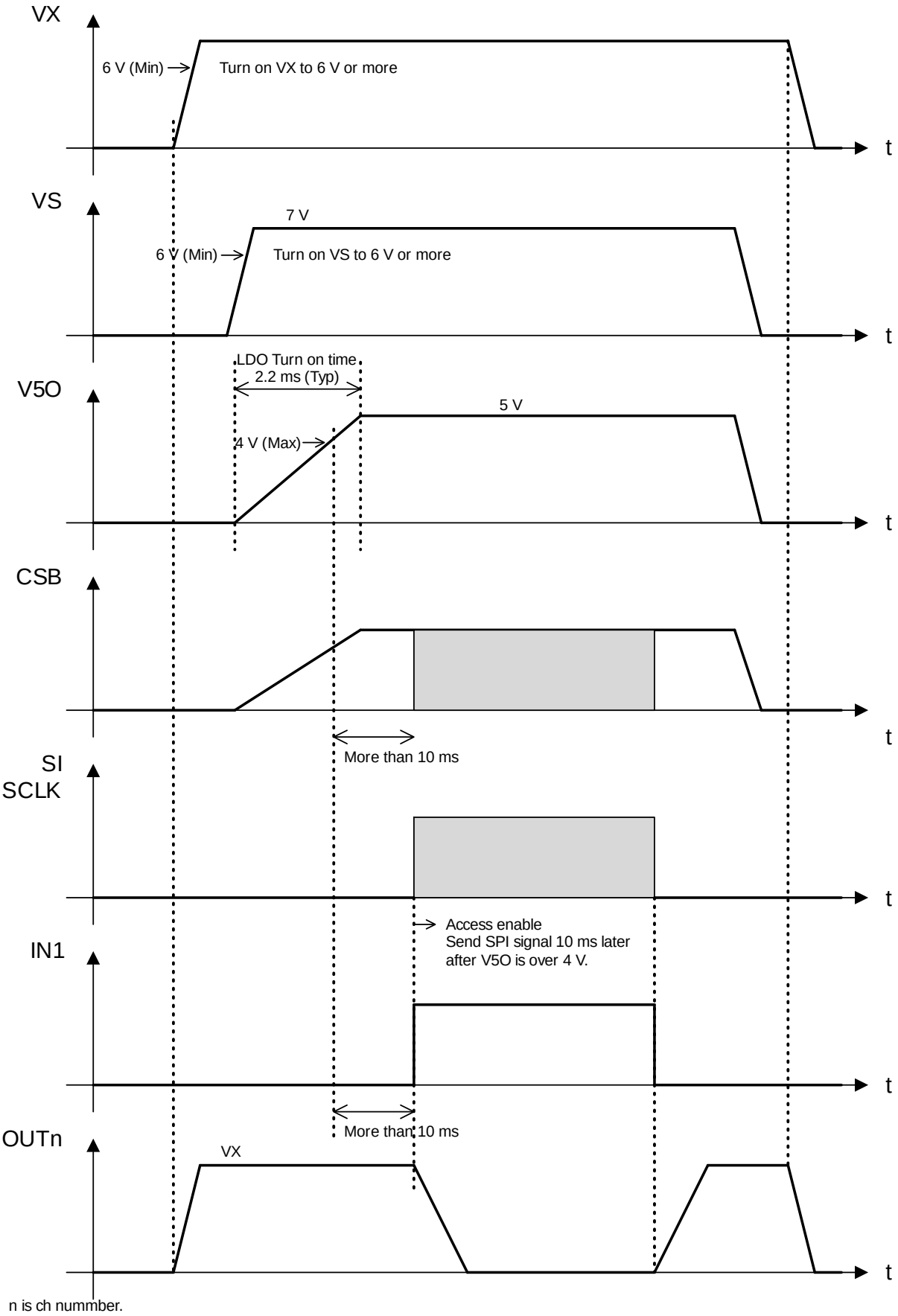
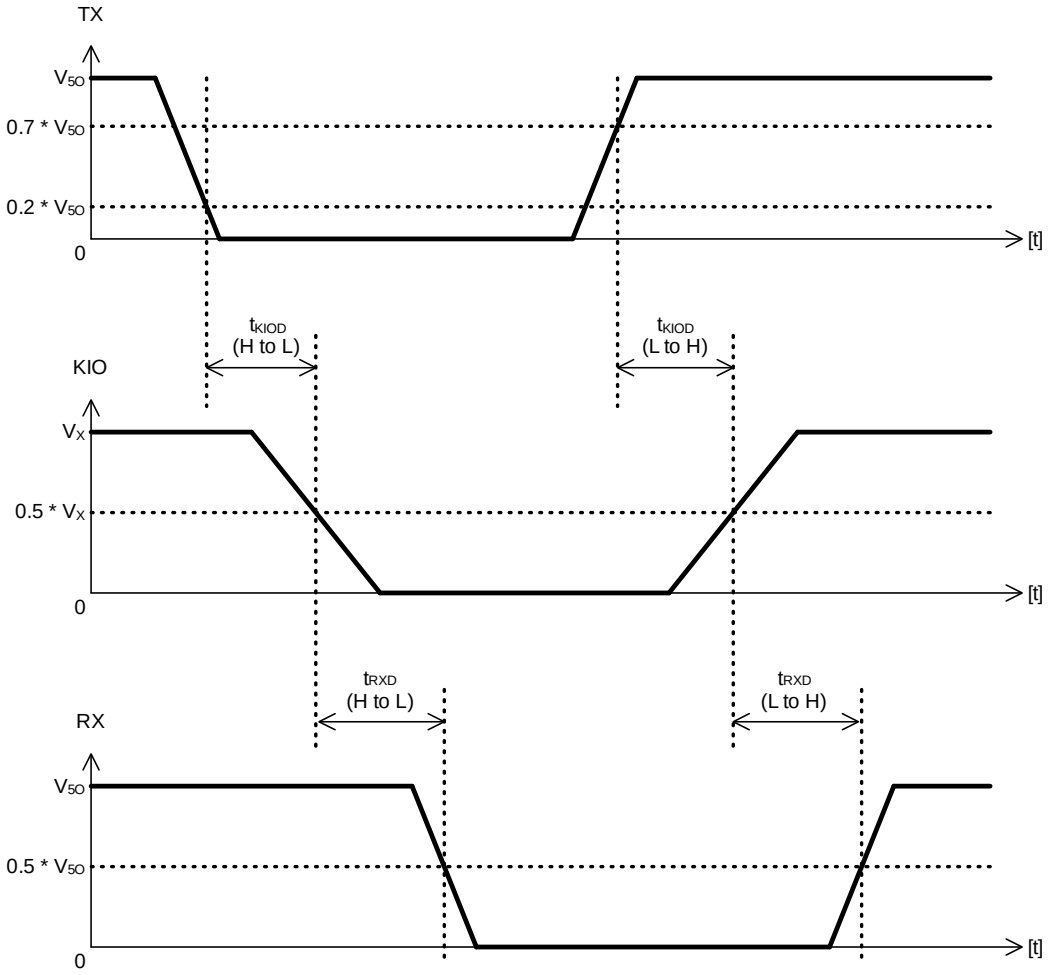


Figure 65.
KIO Low Level Output Voltage

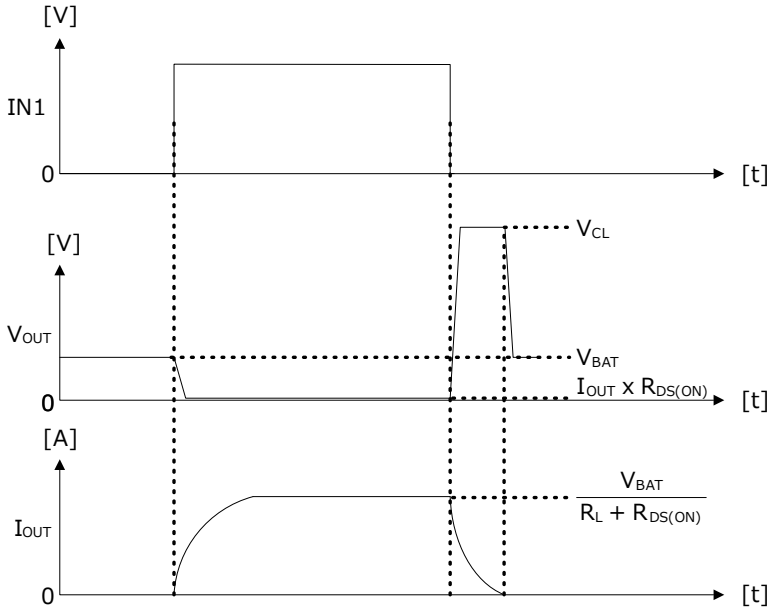
Timing Chart



K-LINE Timing Chart

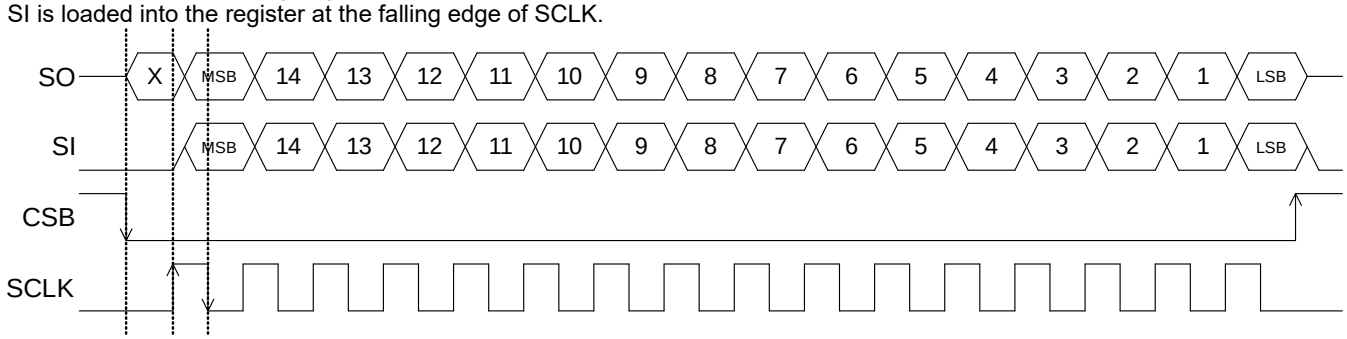


Output waveform During Inductive Load Operation

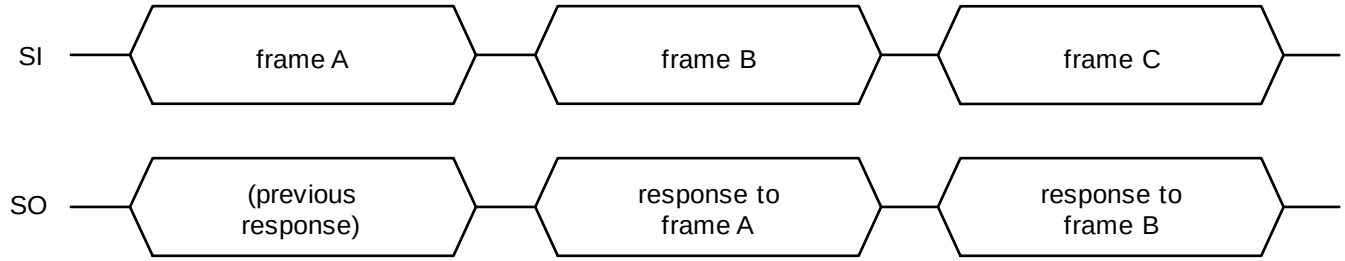


SPI Specification

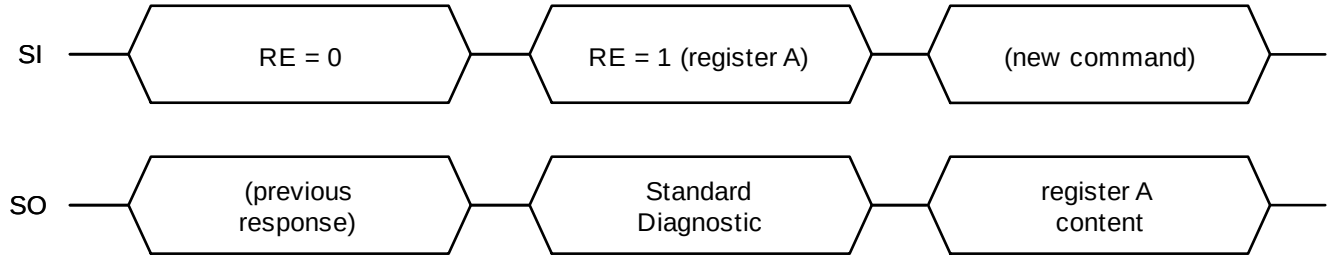
·SPI Overview
When CSB = H
The SO pin is High-Z.
When CSB = L
Outputs to SO at the rising edge of SCLK.
SI is loaded into the register at the falling edge of SCLK.



·SPI Protocol
The SO response to SPI access is returned at the next SPI access as shown in the following figure.

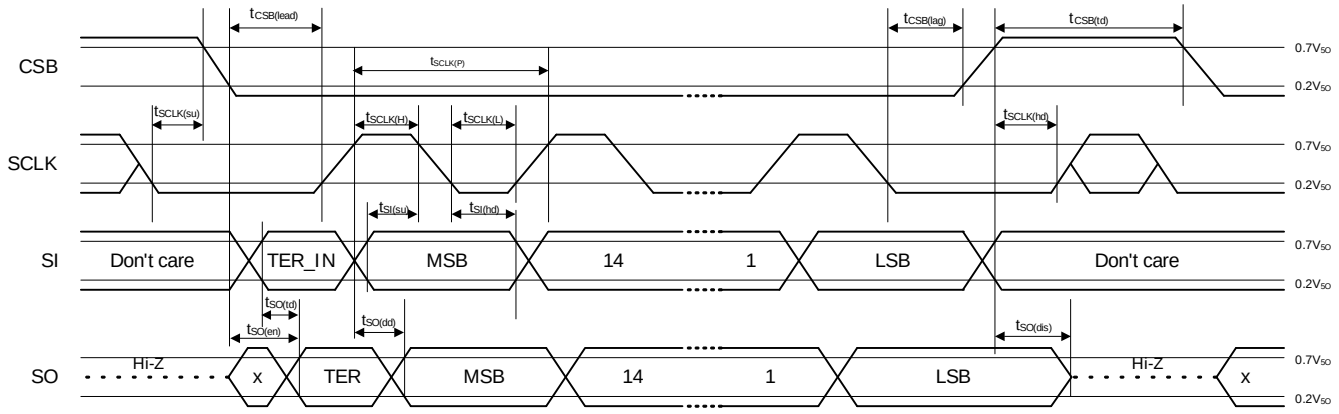


·Response when accessing with RE = 0 and with RE = 1
When accessing with RE = 0, respond “Standard Diagnostic”.
When accessing with RE = 1, respond the value of the specified register.



SPI Specification – continued

·SPI Timing Chart



Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	0	-	5	MHz
SCLK Period	$t_{SCLK(P)}$	200	-	-	ns
SCLK High Time	$t_{SCLK(H)}$	50	-	-	ns
SCLK Low Time	$t_{SCLK(L)}$	50	-	-	ns
SCLK Setup Time	$t_{SCLK(su)}$	50	-	-	ns
SCLK Hold Time	$t_{SCLK(hd)}$	50	-	-	ns
CSB Lead Time	$t_{CSB(lead)}$	250	-	-	ns
CSB Lag Time	$t_{CSB(lag)}$	250	-	-	ns
Transfer Delay Time	$t_{CSB(td)}$	250	-	-	ns
Data Setup Time	$t_{SI(su)}$	20	-	-	ns
Data Hold Time	$t_{SI(hd)}$	20	-	-	ns
SPI Output Enable Time*(Note 1)*	$t_{SO(en)}$	-	-	200	ns
SPI Output Disable Time*(Note 1)*	$t_{SO(dis)}$	-	-	250	ns
SPI Output Data Delay Time*(Note 1)(Note 2)*	$t_{SO(dd)}$	-	-	100	ns
ERR Output Through Delay Time*(Note 1)*	$t_{SO(td)}$	-	-	200	ns

(Note 1) Not 100 % tested.
(Note 2) SO pin capacitance = 20 pF

SPI Specification – continued

·SI Data Structure

Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
RE	WE	Address					TEST	Data							

RE
0: The SO pin outputs "Standard Diagnostic" at the next SPI access.
1: The SO pin outputs the register value specified by Address at the next SPI access.

WE
0: Not Write.
1: Write.

TEST
Be sure to set 0.

Data
When WE = 1, various settings are enabled by writing '0' or '1' to Data.
For details, refer to "Register Map".

·"Standard Diagnostic" (when RE = 0 setting in the previous SPI access)

Initial Value 0x4000

Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0	INIT	0	0	0	TER	0	TSD KLINE	OLD3	OLD2	OLD1	ERR5	ERR4	ERR3	ERR2	ERR1

INIT
0: Normal (after power on, from the second time SPI access).
1: After power on, first time SPI access.

TER
0: Normal
1: SPI communication error
When High pulse input of SCLK is other than (16 times + 8 x m, m is an integer 0 or above) in the low level section of CSB, a communication error is judged.

TSDKLINE
0: Normal
1: Thermal shutdown of K-LINE section
Once detected, it latches." Standard Diagnostic" is cleared by read access.

DIAG_OLDn (n shows ch number)
0: Normal
1: Open load detection of OUT1, OUT2, OUT3
Once detected, it latches." Standard Diagnostic" is cleared by read access.

ERRn (n shows ch number)
0: Normal
1: Over current protection, thermal shutdown, or output overhead detection (OUT1, OUT2, OUT3 only) for OUTn
(Logical OR of DIAG_OCPn, DIAG_TSDn, and DIAG_OFDn)

·SO Output Data Structure (when RE = 1 setting in the previous SPI access)

Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
1	WE	Address					ERR_{ALL}	Data							

WE, Address
Outputs WE and Address values that were set during the previous SPI access.

ERR_{ALL}
Outputs 1 when either open load detection, output overhead detection, over current protection or thermal shutdown is detected on at least one channel.
(Logical OR of DIAG_OLDn, DIAG_OFDn, DIAG_OCPn, DIAG_TSDn and DIAG_TSD_KLINE for all channels)

Data
Outputs the register value of Address that were set during the previous SPI access.

Register Map

Register Name	Register Access	Address	TEST	Data								Initial
		Bit[13:9]	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	
OUTCTRL	R/W	0x00	0	0	0	0	OUTCTRL5	OUTCTRL4	OUTCTRL3	OUTCTRL2	0	0x00
STATUS_IN	RO	0x06	0	0	0	0	0	0	0	0	STATUS_IN1	0x00
DIAG_OUT32	RO	0x0A	0	0	DIAG_OFD3	DIAG_OCP3	DIAG_TSD3	0	DIAG_OFD2	DIAG_OCP2	DIAG_TSD2	0x00
DIAG_OUT541	RO	0x0B	0	DIAG_OCP5	DIAG_TSD5	DIAG_OCP4	DIAG_TSD4	0	DIAG_OFD1	DIAG_OCP1	DIAG_TSD1	0x00
HWCR	WO	0x0C	0	0	RST	0	0	0	0	0	0	0x00
T_TESTMODE	WO	0x1E	1	0	0	0	0	0	0	0	TESTMODE	0x00

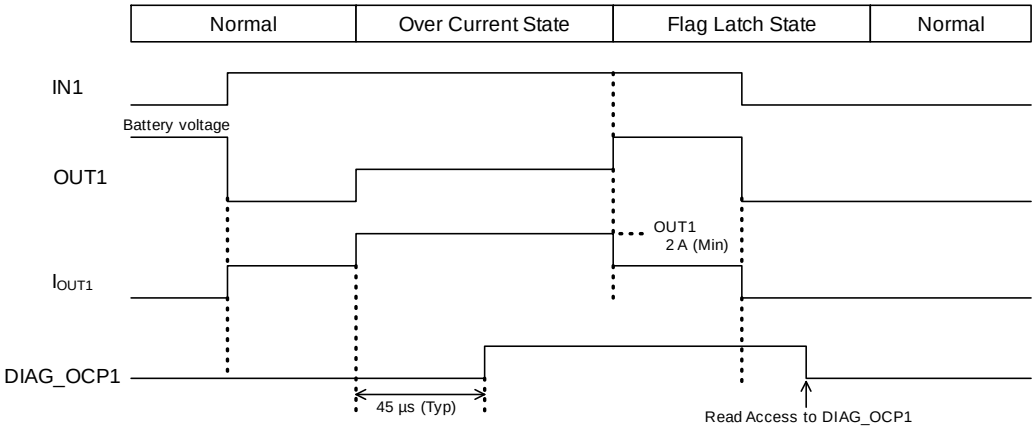
Register Name	Register Access	Address	Explanation of Data
OUTCTRL	Read / Write	0x00h	OUTCTRLn bit (n represents the channel number) '0': OUTn off setting '1': OUTn on setting
STATUS_IN	Read Only	0x06h	STATUS_IN1 bit '0': IN1 L input, OUT1 Off Setting '1': IN1 H input, OUT1 On Setting
DIAG_OUT32 DIAG_OUT541	Read Only	0x0Ah 0x0Bh	Reads the error flags of OUT1 to OUT5. DIAG_OFDn bit '0': Normal '1': Output overhead detection Once detected, it latches. Cleared by read access to DIAG_OFDn. DIAG_OCPn bit '0': Normal '1': Over current protection detection It latches, if over current protection is detected at the same time as thermal shutdown or if continue detecting over current protection for a certain period of time. Cleared by read access to DIAG_OCPn. If over current protection is detected on OUT2 to OUT5, the OUTCTRLn bit of the corresponding channel is cleared to '0' and the output is turned off. After clearing DIAG_OCPn, OUTn is turned on by setting OUTCTRLn to '1' again. DIAG_TSDn bit '0': Normal '1': Thermal shutdown detection Once detected, it latches. Cleared by read access to DIAG_TSDn.
HWCR	Write Only	0x0Ch	RST '0': Normal '1': Hardware reset (auto clear)
T_TESTMODE	Write Only	0x1Eh	TESTMODE '0': Normal '1': Test Mode If IN pin is 5.6 V (Min) or more and "1" is written to this register, IC enters test mode. For this reason, do not access to this register.

Protection Function

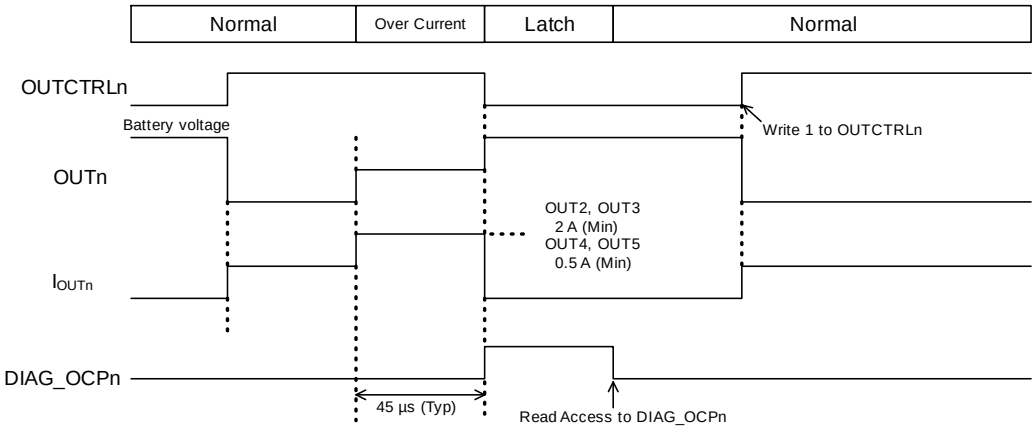
Protection Function		Detection and Release Conditions			Output Behavior
Low Side Switch	Over Current Protection	Detection Conditions	OUT1	2 A (Min)	Current limitation
			OUT2 OUT3	2 A (Min)	Output latch after 45 µs (Typ) of current-limit state has elapsed
			OUT4 OUT5	0.5 A (Min)	Output latch after 45 µs (Typ) of current-limit state has elapsed
		Release Conditions	OUT1	2 A (Min) or less (automatic recovery)	Normal operation
			OUT2 OUT3	Write '1' to OUTCTRL2 or OUTCTRL3 after read access to DIAG_OUT32	Output latch is released
			OUT4 OUT5	Write '1' to OUTCTRL4 or OUTCTRL5 after read access to DIAG_OUT541	Output latch is released
	Thermal Shutdown	Detection Condition	Tj ≥ 150 °C (Min)		Output stop
		Release Condition	Tj ≤ 125 °C (Min)		Normal operation
	Open Load Detection (Only OUT1, OUT2 and OUT3 are supported)	Detection Condition	Output off state and Output voltage 2.0 V (Typ) or less		Normal operation
		Release Condition	Output off state and Output voltage 2.5 V (Typ) or more		Normal operation
	Output Overhead Detection (Only OUT1, OUT2 and OUT3 are supported)	Detection Condition	Output on and Output voltage 2.5 V (Typ) or more		Normal operation
		Release Condition	Output on and Output voltage 2.0 V (Typ) or less		Normal operation
LDO	Over Current Protection	Detection Condition	I_{V5O} ≥ 250 mA (Min)		-
		Release Condition	I_{V5O} < 250 mA (Min)		-
	Thermal Shutdown	Detection Condition	Tj ≥ 150 °C (Min)		LDO output stopped
		Release Condition	Tj ≤ 125 °C (Min)		Normal operation
	Power-on Reset	Detection Condition	V_{5O} ≤ 3.0 V (Min)		Low side output stopped KIO output stopped
		Release Condition	V_{5O} ≥ 4.0 V (Min)		Normal operation
K-LINE	KIO Over Current Protection	Detection Condition	Output current 40 mA (Min)		Current limitation
		Release Condition	Output current 40 mA (Min) or less		Normal operation
	Thermal Shutdown	Detection Condition	Tj ≥ 150 °C (Min)		KIO output stopped
		Release Condition	Tj ≤ 125 °C (Min)		Normal operation

Over Current Protection

If a current exceeding the over current detection value flows to the low side output, over current protection is applied and an error flag (DIAG_OCPn) is output.
For OUT1, the current flowing to the output is limited when over current protection is applied.

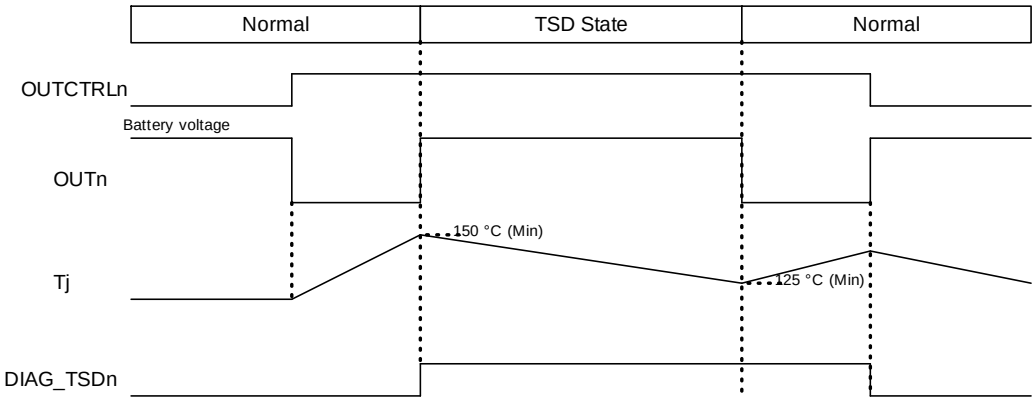


For OUT2 to OUT5, the output is turned off when over current protection is applied. In this case, OUTCTRLn is set to '0'; read access to DIAG_OCPn clears the error flag and setting OUTCTRLn to '1' turns on the output.

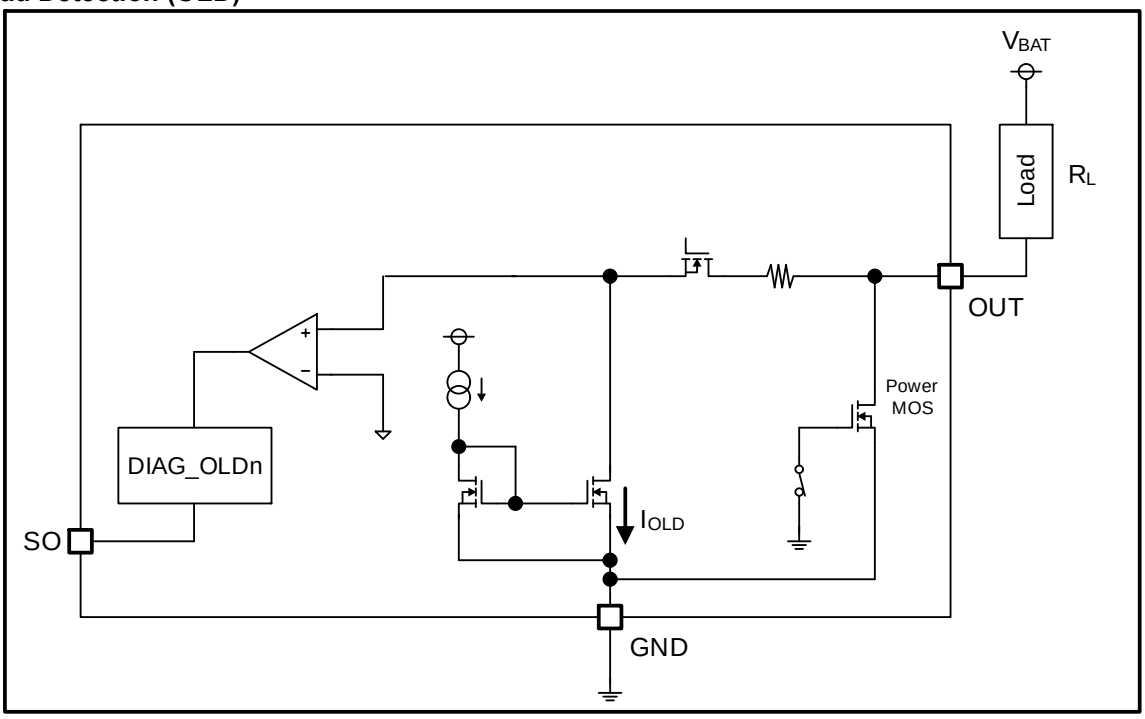


Thermal Shutdown

Turns off the low side output, LDO output, and KIO output when Tj rises 150 °C (Min) or above. Turns back on when Tj falls 125 °C (Min) or below.



Open Load Detection (OLD)

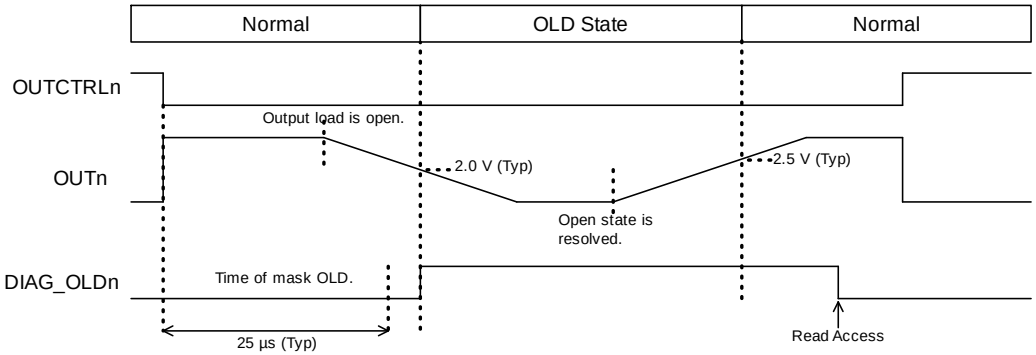


OUT1, OUT2, and OUT3 have an open load detection (OLD) function: output inflow current I_{OLD} is applied to OUT, and as load R_L increases, output voltage V_{OUT} decreases, and when it falls below $V_{OLD(ON)}$, an open load detection state occurs and an error flag is output.

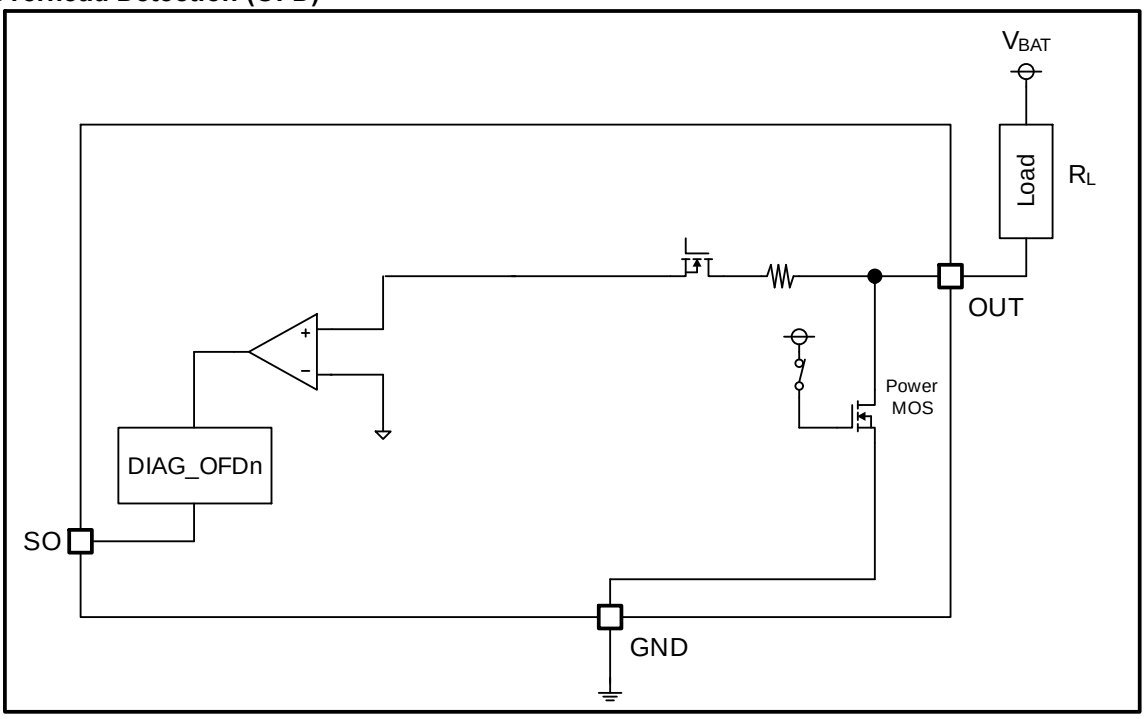
The value of R_L that detects OLD is obtained from the following formula.

$$R_L \geq \frac{V_{BAT} - V_{OLD(ON)}}{I_{OLD}}$$

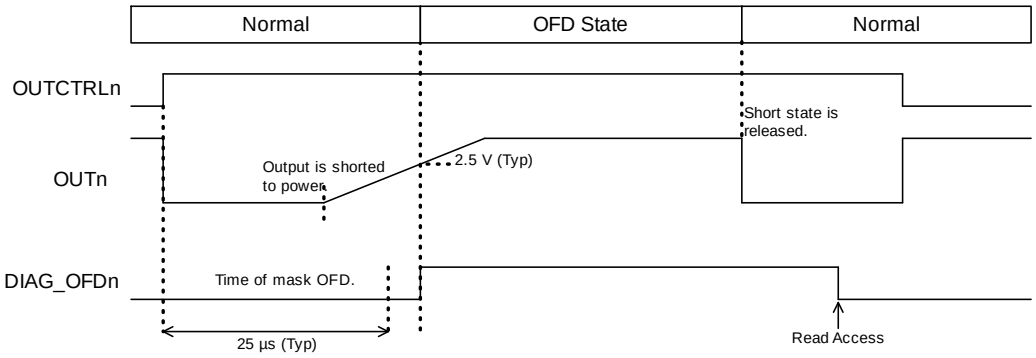
V_{BAT} : Battery voltage
$V_{OLD(ON)}$: Open load detection voltage 3.1 V (Max)
I_{OLD} : Output inflow current during open detection operation 90 µA (Max)



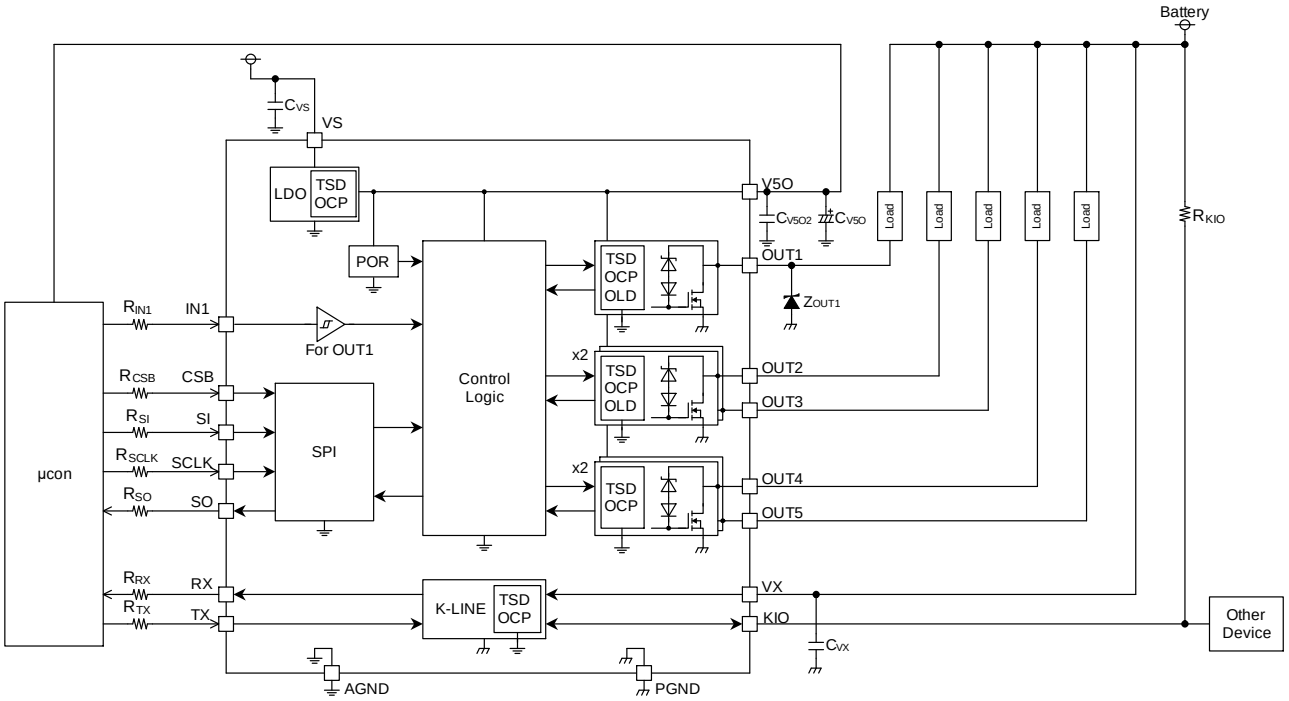
Output Overhead Detection (OFD)



OUT1, OUT2, and OUT3 have an output overhead detection (OFD) function.
When the output transistor is on, if the output voltage of OUT1 to OUT3 exceeds $V_{OFD(ON)}$, a state of top fault detection occurs, and an error flag is output.



Application Example

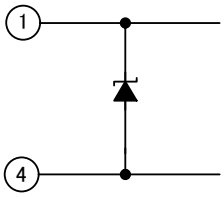
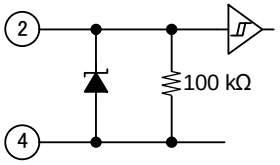
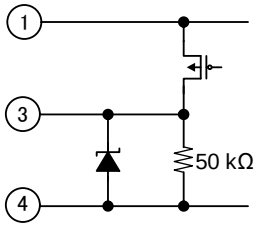
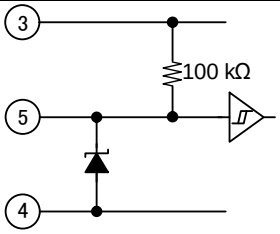
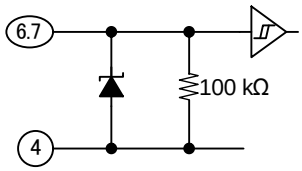
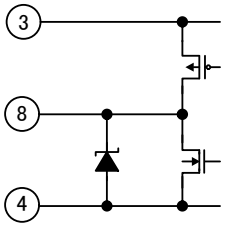


Selection of Components Externally Connected

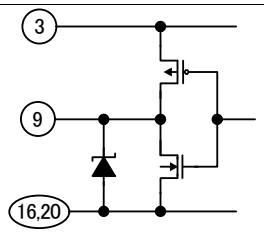
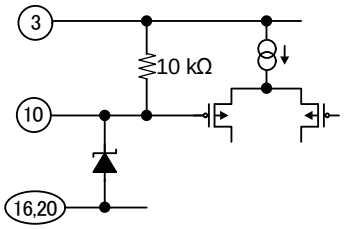
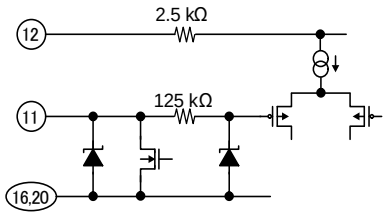
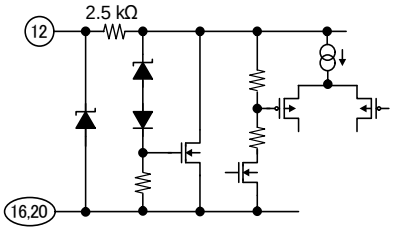
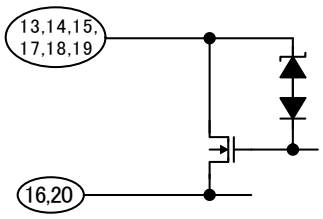
Symbol	Value	Purpose
R_{IN1}, R_{CSB}, R_{SI}, R_{SCLK}, R_{SO}	1 kΩ	Register for microcontroller protection against negative voltage surge.
R_{RX}, R_{TX}	1 kΩ	Register for microcontroller protection against negative voltage surge.
R_{KIO}	480 Ω	KIO Pull-up Resistor
C_{VX}	0.1 µF	Capacitor for noise rejection on power supply lines *(Note 1)*
C_{VS}	0.1 µF	Capacitor for noise rejection on power supply lines *(Note 1)*
C_{V5O}	220 µF	LDO Output Capacitor *(Note 1)(Note 2)*
C_{V5O2}	0.1 µF	LDO Output Capacitor *(Note 1)(Note 3)*
Z_{OUT1}	-	Zener diode for the reverse energy absorption when inductive load is turned off *(Note 4)*

(Note 1) It is recommended to insert capacitors as close as possible between VX and PGND, between VS and AGND, and between V5O and AGND.
(Note 2) Connect large capacitor to stabilize the output.
(Note 3) When using a capacitor with ESR of 1 Ω or more in C_{V5O}, insert a ceramic capacitor (C_{V5O2}) in parallel.
(Note 4) Connect it when driving an inductive load that exceeds active clamp energy of this product. The same is true for OUT2 to OUT5.

I/O Equivalence Circuits

Pin No.	Pin Name	I/O Equivalence Circuit
1	VS	
2	IN1	
3	V5O	
4	AGND	-
5	CSB	
6	SCLK	
7	SI	
8	SO	

I/O Equivalence Circuits – continued

Pin No.	Pin Name	I/O Equivalence Circuit
9	RX	
10	TX	
11	KIO	
12	VX	
13	OUT5	
14	OUT4	
15	OUT3	
16	PGND	
17	OUT2	
18 19	OUT1	
20	PGND	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input and Output Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

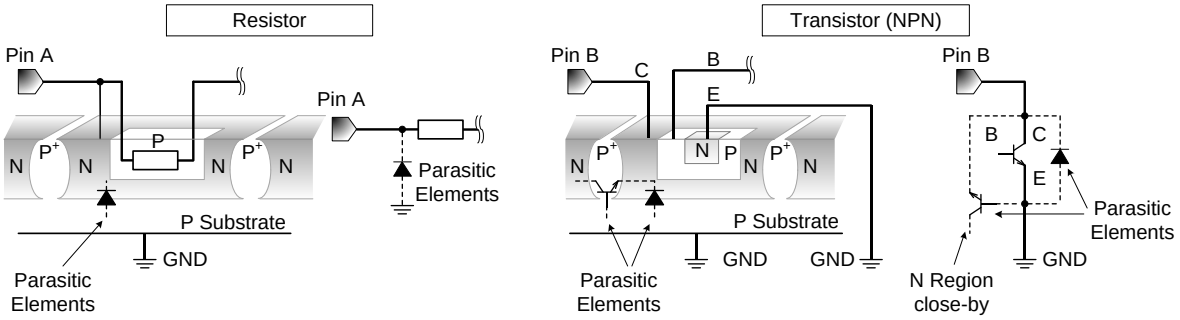


Figure 66. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Function (TSD)

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Function (OCP)

This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

14. Active Clamp Operation

The IC integrates the active clamp function to internally absorb the reverse energy E_L which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy E_L is active clamp tolerance E_{AS} (refer to Figure 1.2.) or under when inductive load is used.

Operational Notes – continued

15. Power Supply Steep Fluctuation

If the voltage of the power supply pin (VS) falls sharply, the output pin (OUT) may temporarily turn off as shown in Figure 67. If the power supply pin is expected to fall sharply, take measures such as inserting a capacitor between the power supply pin and the ground pin so that it falls within the recommended usage range shown in Figure 68.

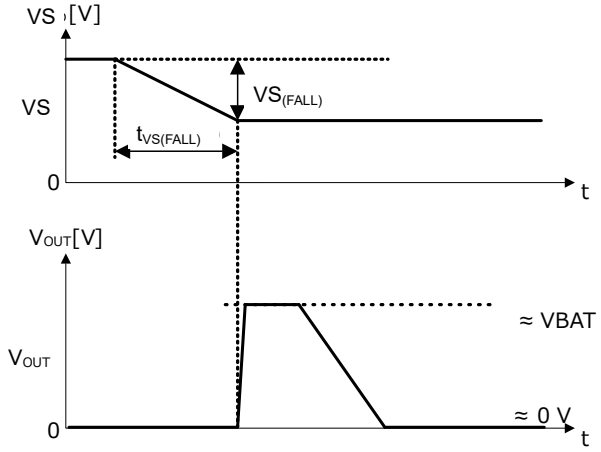


Figure 67. Output OFF operation when power supply fluctuates sharply

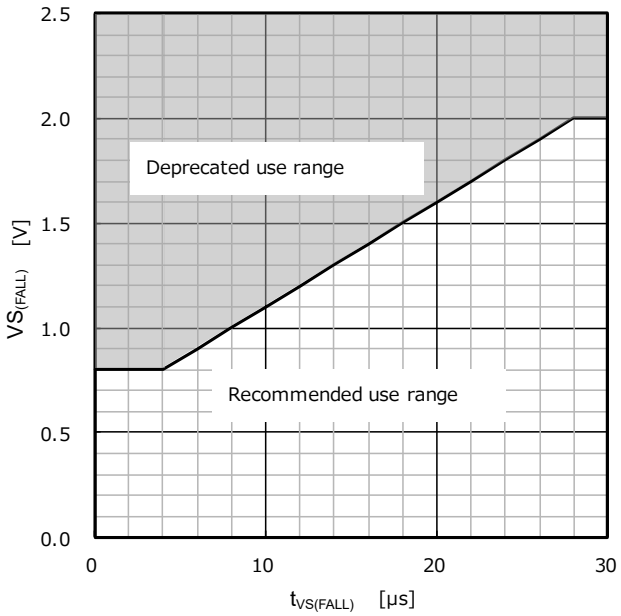


Figure 68. Recommended use range

16. GND Pin Connection

Connect all ground pins to ground.

17. Same Pin Connection

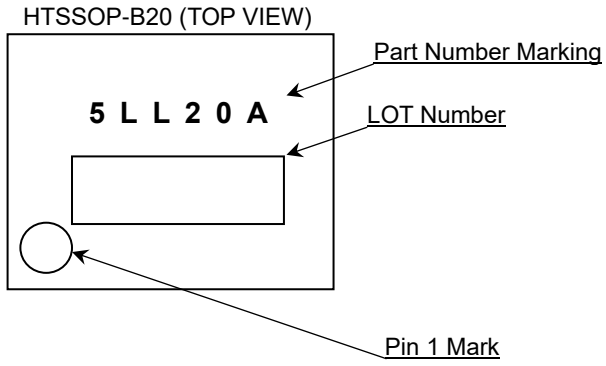
Connect all OUT1 pins to same line.

Ordering Information

B	D	5	L	L	2	0	A	E	F	V	-	CE 2

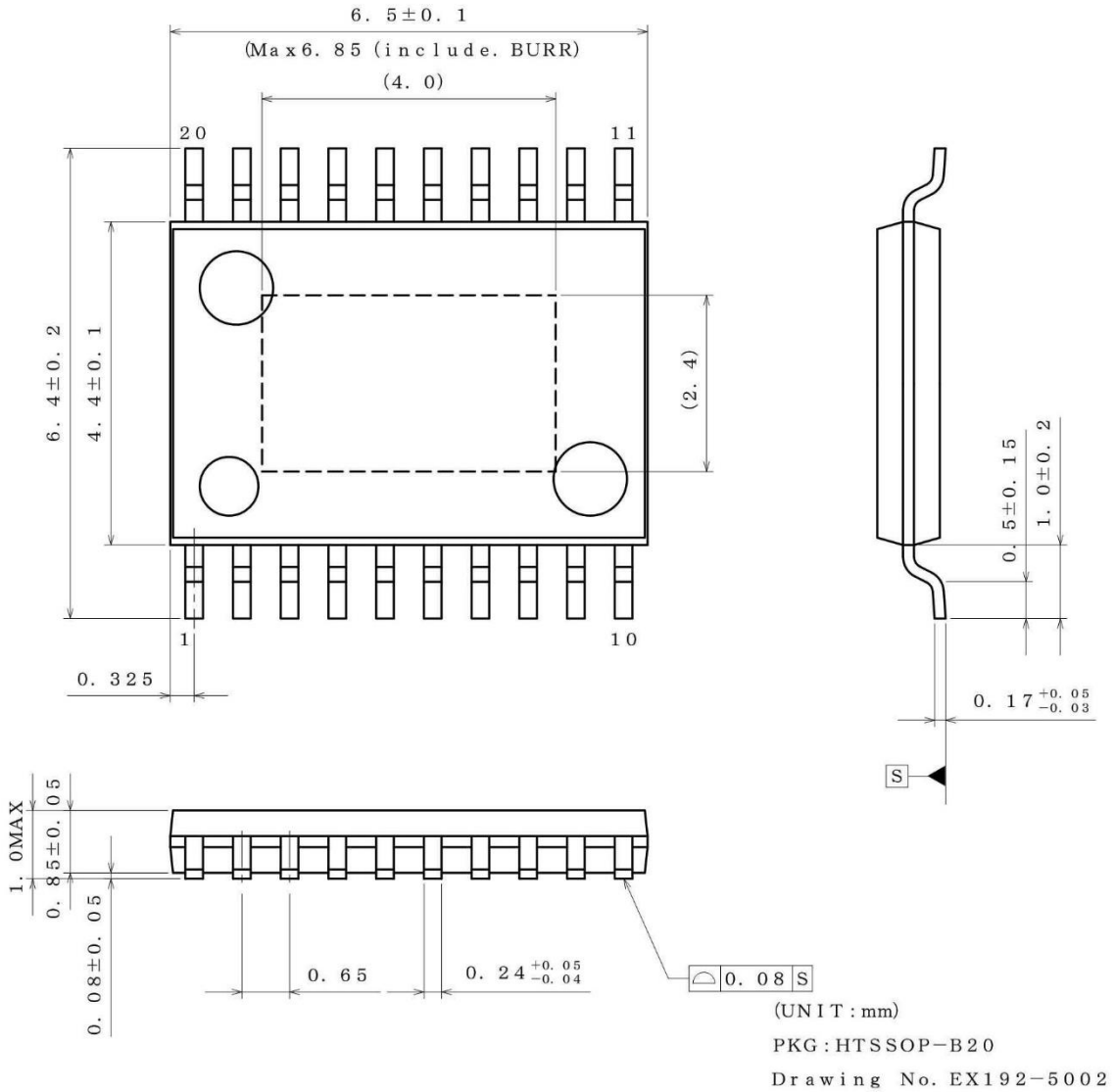
- 5: 5ch
  L: low side switch
- Package
  EFV: HTSSOP-B20
- Product Rank
  C: For Automotive
  Packaging Specification
  E2: Embossed tape and reel

Marking Diagram



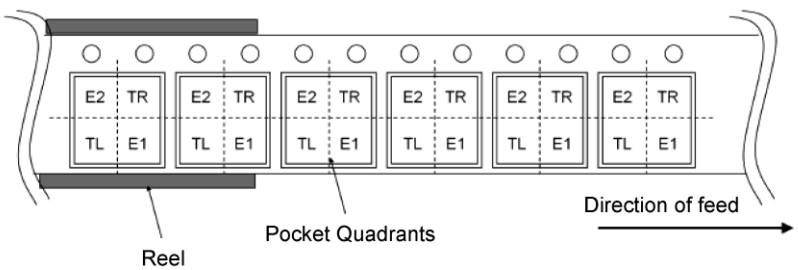
Physical Dimension and Packing Information

Package Name	HTSSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
13.Jan.2023	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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