## Automotive IPD Series

# 8ch Low Side Switch

## BD8LD650EFV-C

### General Description

BD8LD650EFV-C is an 8-channel SPI-input low side switch for automotive and industrial application. It has built-in open load detection function, short ground detection function, over current protection function, thermal shutdown function, and active clamp function.

### Features

- AEC-Q100 Qualified*(Note 1)*
- Monolithic Power Management IC with Control Block (CMOS) and a Power MOSFET Mounted on a Single Chip
- Channel Control/error can be Detected by 16 bit SPI Commands.
- Built-in Open Load Detection Function (OLD)
- Built-in Short Ground Detection Function (SGD)
- Built-in Over Current Protection Function (OCP)
- Built-in Thermal Shutdown Function(TSD)
- Built-in Active Clamp Function
- Built-in Synchro Mode
- Built-in Limp Home Mode
- Surface-mount HTSSOP-B20 Packaging

*(Note 1)* Grade1

### Application

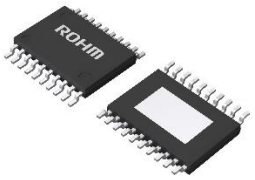
- Driving Resistive and Inductive Load

### Key Specifications

- Input Voltage Range VDD: 4.0 V to 5.5 V
- Input Voltage Range VDDIO: 3.0 V to 5.5 V
- On State Resistance: 650 mΩ (Typ)
- Over Current Threshold Value: 0.5 A/1.0 A (Min)
- Active Clamp Energy: 125 mJ
- Operating Temperature Range Tj:-40 °C to +150 °C

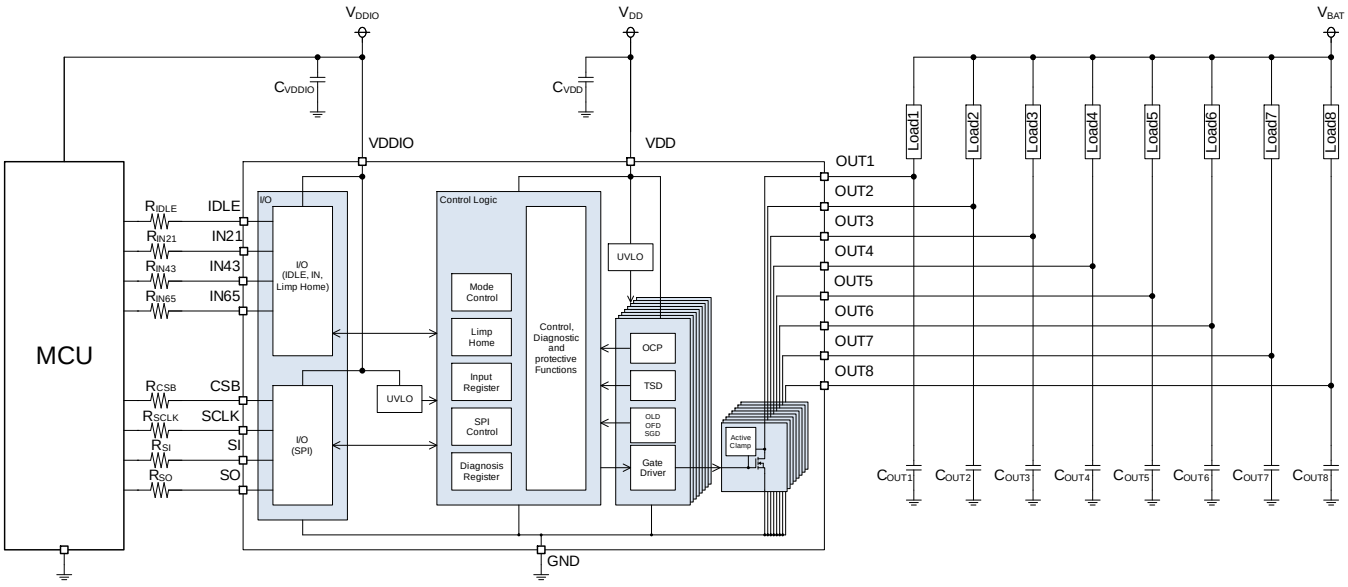
### Package

| | W (Typ) x D (Typ) x H (Max) |
|---|---|
| HTSSOP-B20 | 6.5 mm x 6.4 mm x 1.0 mm |



HTSSOP-B20

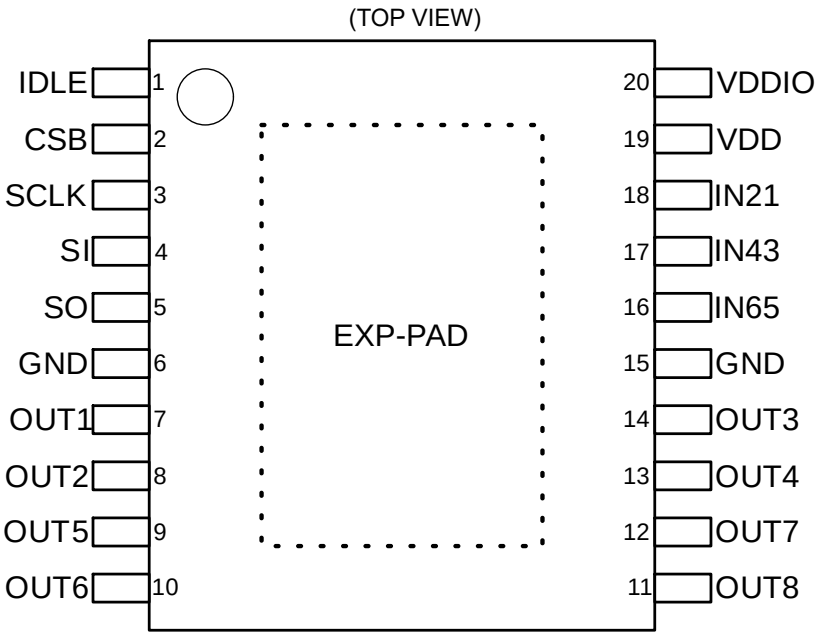
### Typical Application Circuit




○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

# Contents

### Pin Configuration

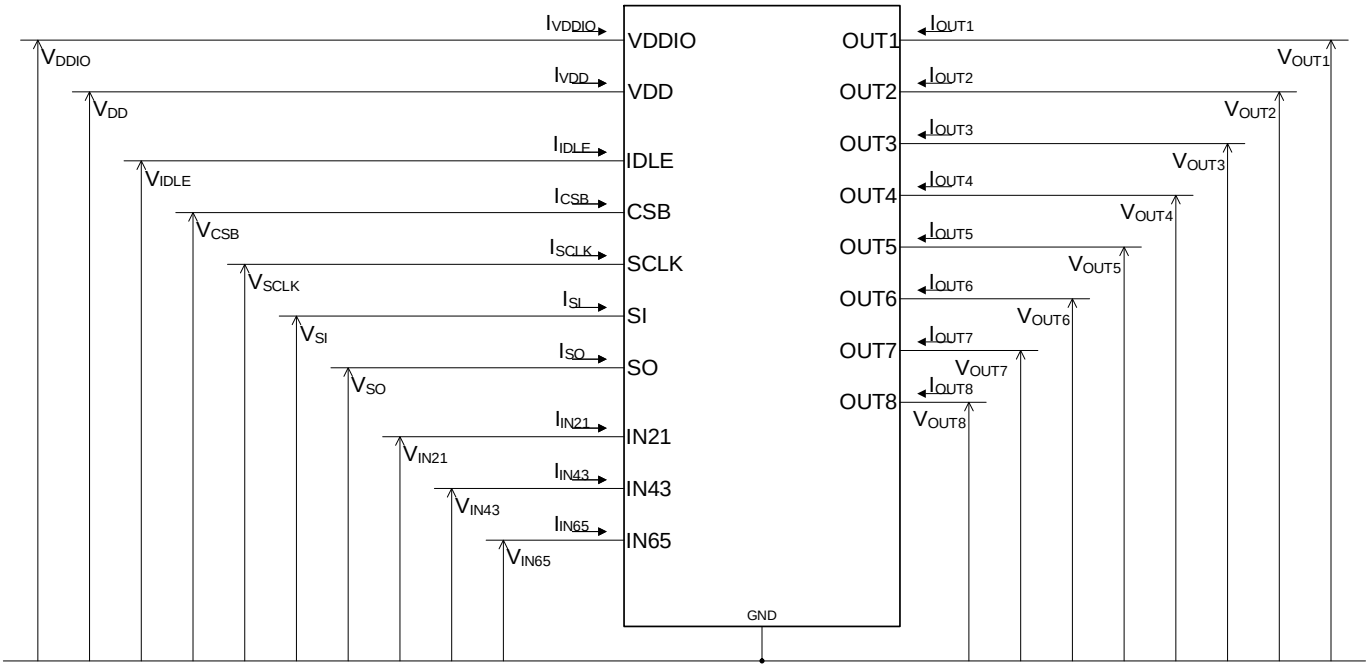



### Pin Descriptions

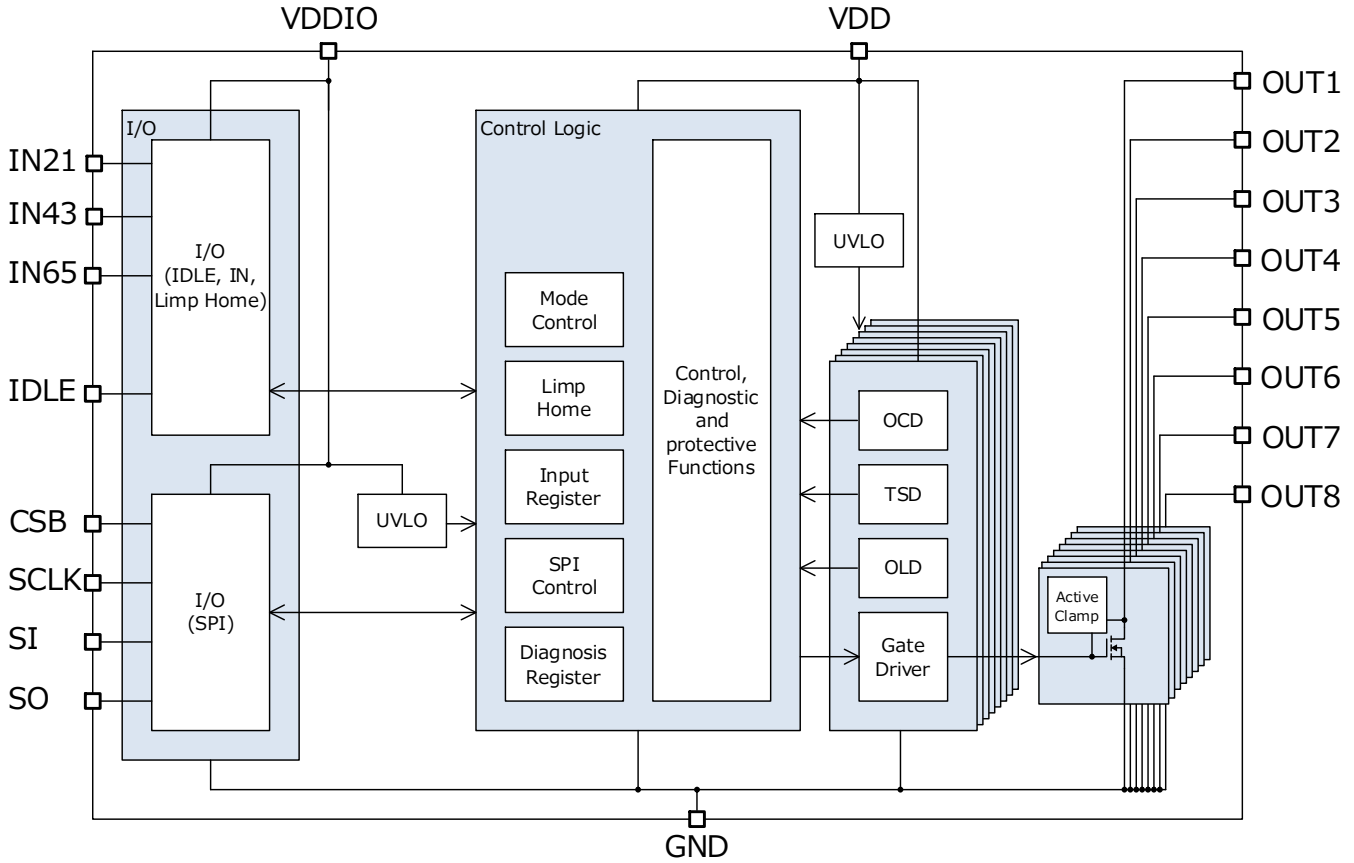
| Pin No. | Pin Name | Function |
|---|---|---|
| 1 | IDLE | Limp home mode control<br>This pin is connected to GND via an internal pull-down resistor. |
| 2 | CSB | SPI enable<br>This pin is connected to VDDIO via an internal pull-up resistor. |
| 3 | SCLK | Serial clock input<br>This pin is connected to GND via an internal pull-down resistor. |
| 4 | SI | Serial data input<br>This pin is connected to GND via an internal pull-down resistor. |
| 5 | SO | Serial data output |
| 6 | GND | GND |
| 7 | OUT1 | ch1 output |
| 8 | OUT2 | ch2 output |
| 9 | OUT5 | ch5 output |
| 10 | OUT6 | ch6 output |
| 11 | OUT8 | ch8 output |
| 12 | OUT7 | ch7 output |
| 13 | OUT4 | ch4 output |
| 14 | OUT3 | ch3 output |
| 15 | GND | GND |
| 16 | IN65 | ch5, ch6 control*(Note 1)*<br>This pin is connected to GND via an internal pull-down resistor. |
| 17 | IN43 | ch3, ch4 control*(Note 1)*<br>This pin is connected to GND via an internal pull-down resistor. |
| 18 | IN21 | ch1, ch2 control*(Note 1)*<br>This pin is connected to GND via an internal pull-down resistor. |
| 19 | VDD | Analog power supply |
| 20 | VDDIO | Digital power supply |
| - | EXP-PAD | Be sure to connect EXP-PAD to GND. |

*(Note 1)* Controlled channels can be changed by accessing DIRCTRL register from the SPI.

### Definition




### Block Diagram



## Absolute Maximum Ratings (Tj = 25 °C)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| VDDIO, VDD Power Supply Voltage | $V_{DDIO}$, $V_{DD}$ | -0.3 to +7 | V |
| Output Voltage (Power MOS Output) | $V_{OUT1-8}$ | -0.3 to (Internal Limit)*(Note 1)* | V |
| Output Current (Power MOS Output) | $I_{OUT1-8}$ | (Internal Limit)*(Note 2)* | A |
| Output Voltage (SPI) | $V_{SO}$ | -0.3 to +7 | V |
| Input Voltage (IDLE) | $V_{IDLE}$ | -0.3 to +7 | V |
| Input Voltage (SPI) | $V_{CSB}$, $V_{SCLK}$, $V_{SI}$ | -0.3 to +7 | V |
| Input Voltage (IN65, IN43, IN21) | $V_{IN65}$, $V_{IN43}$, $V_{IN21}$ | -0.3 to +7 | V |
| Storage Temperature Range | Tstg | -55 to +150 | °C |
| Maximum Junction Temperature | Tjmax | 150 | °C |
| Active Clamp Energy (Single Pulse)<br>$T_{j(START)}$ = 25 °C, $I_{OUT1-8(START)}$ = 0.4 A | $E_{AS1-8(25\ °C)}$ | 125 | mJ |
| Active Clamp Energy (Single Pulse)*(Note 3)*<br>$T_{j(START)}$ = 150 °C, $I_{OUT1-8(START)}$ = 0.4 A | $E_{AS1-8(150\ °C)}$ | 25 | mJ |
| Active Clamp Energy (Single Pulse)<br>$T_{j(START)}$ = 25 °C, $I_{OUT1-8(START)}$ = 0.8 A, Synchro Mode | $E_{S,\ AS1-8(25\ °C)}$ | 57 | mJ |
| Active Clamp Energy (Single Pulse)*(Note 3)*<br>$T_{j(START)}$ = 150 °C, $I_{OUT1-8(START)}$ = 0.8 A, Synchro Mode | $E_{S,\ AS1-8(150\ °C)}$ | 19 | mJ |
| Active Clamp Energy (Repetitive)*(Note 3)(Note 4)*<br>$T_{j(START)}$ = 125 °C, $I_{OUT(START)}$ = 0.2 A | $E_{AR(125\ °C)}$ | 12 | mJ |
| Active Clamp Energy (Repetitive)*(Note 3)(Note 4)*<br>$T_{j(START)}$ = 125 °C, $I_{OUT(START)}$ = 0.4 A, Synchro Mode | $E_{S,\ AR(125\ °C)}$ | 9 | mJ |

*(Note 1)* Limited by the active clamp function.
*(Note 2)* Limited by the over current protection function. The over current detection value can be adjusted in two levels.
*(Note 3)* Not 100 % are tested.
*(Note 4)* 2M cycles, All channel input.

***Caution 1:*** *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

***Caution 2:*** *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

***Caution 3:*** *When IC is turned off with an inductive load, reverse energy has to be dissipated in the IC. This energy can be calculated by the following equation:*

$$E_L = \frac{1}{2} L I_{OUT(START)}{}^2 \times \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CL)}}\right)$$

*Where:*
*L is the inductance of the inductive load.*
*$I_{OUT(START)}$ is the output current at the time of turning off.*
*$V_{OUT(CL)}$ is the output clamp voltage.*

*The IC integrates the active clamp function to internally absorb the reverse energy $E_L$ which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy $E_L$ is active clamp energy $E_{AS}$ (Figure 1.), $E_{S,AS}$ (Figure 2.) or under when inductive load is used.*

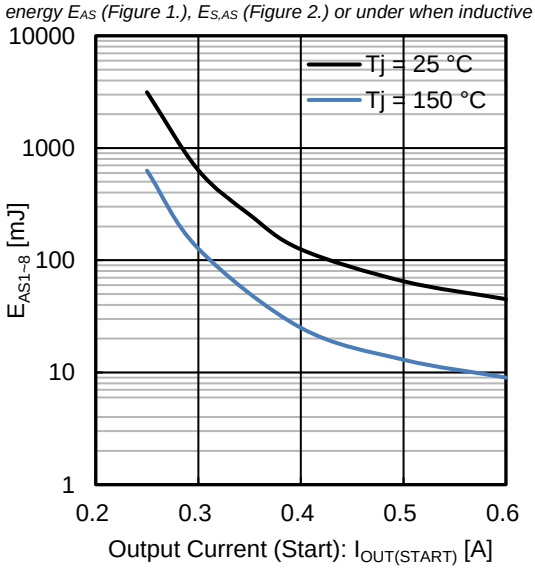



Figure 1. Active Clamp Energy (Single Pulse) vs Output Current

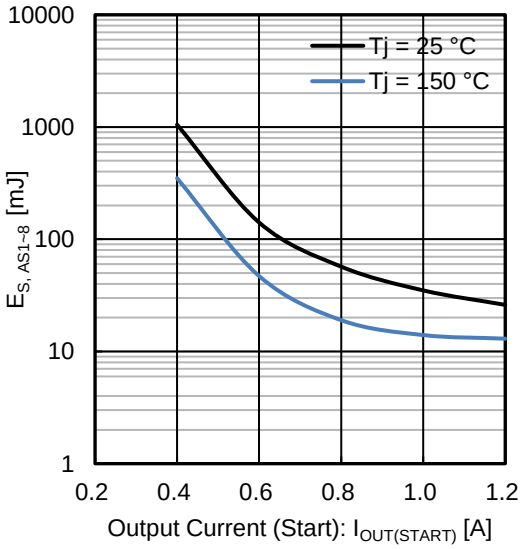


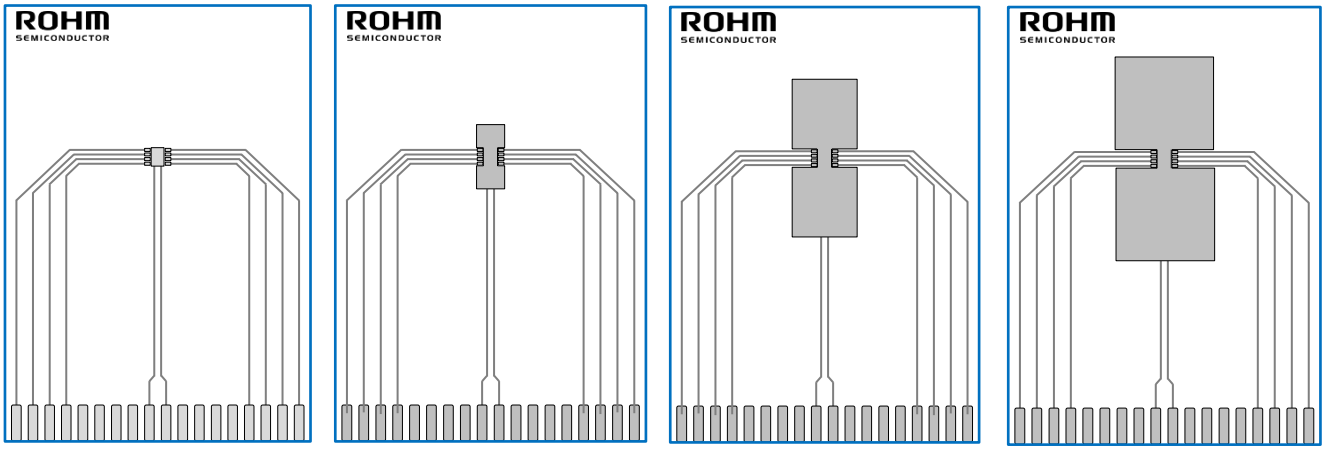

Figure 2. Active Clamp Energy (Single Pulse) Synchro Mode vs Output Current

### Thermal Resistance *(Note 1)*

| Parameter | Symbol | Typ | Unit | Condition |
|---|---|---|---|---|
| HTSSOP-B20 | | | | |
| Between Junction and Surroundings Temperature Thermal Resistance | $\theta_{JA}$ | 96.6 | °C/W | 1s *(Note 2)* |
| | | 35.1 | °C/W | 2s *(Note 3)* |
| | | 24.5 | °C/W | 2s2p *(Note 4)* |

*(Note 1)* The thermal impedance is based on JESD51-2A(Still-Air) standard.
*(Note 2)* JESD51-3 standard FR4 114.3 mm x 76.2 mm x 1.57 mm 1-layer (1s)
(Top copper foil: ROHM recommended Footprint + wiring to measure, 2 oz. copper. )
*(Note 3)* JESD51-5 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 2-layers (2s).
(Top copper foil: ROHM recommended Footprint + wiring to measure/
Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, copper (top & reverse side) 2 oz )
*(Note 4)* JESD51-5/-7 standard FR4 114.3 mm x 76.2 mm x 1.60 mm 4-layers (2s2p)
(Top copper foil: ROHM recommended Footprint + wiring to measure/
2 inner layers and copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, copper (top & reverse side/inner layers) 2 oz./1 oz.)

■ PCB Layout 1 layer (1s)



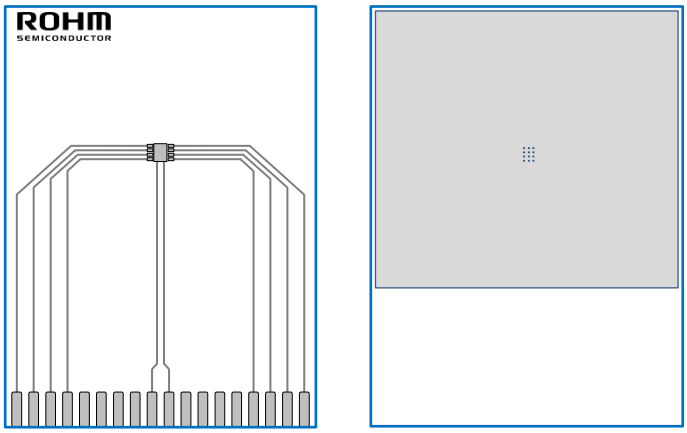

Footprint 100 mm$^2$ 600 mm$^2$ 1200 mm$^2$

Figure 3. PCB Layout 1 Layer (1s)

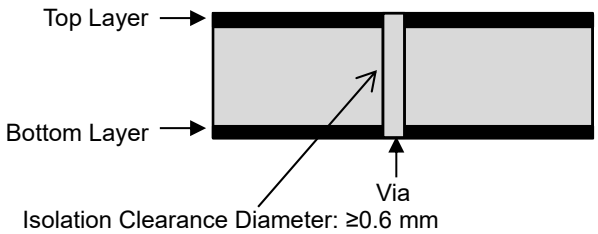
| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.57 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top Layer) | 0.070 mm (Cu: 2 oz) |
| Copper Foil Area Dimension | Footprint/100 mm$^2$/600 mm$^2$/1200 mm$^2$ |

### Thermal Resistance – continued

■ PCB Layout 2 layers (2s)




Top Layer Bottom Layer




Cross Section

Figure 4. PCB-layout 2-layer (2s)

| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top/Bottom Layers) | 0.070 mm (Cu +Plating) |
| Thermal Vias Separation/Diameter | 1.2 mm/0.3 mm |

### Thermal Resistance – continued

■ PCB Layout 4 layers (2s2p)

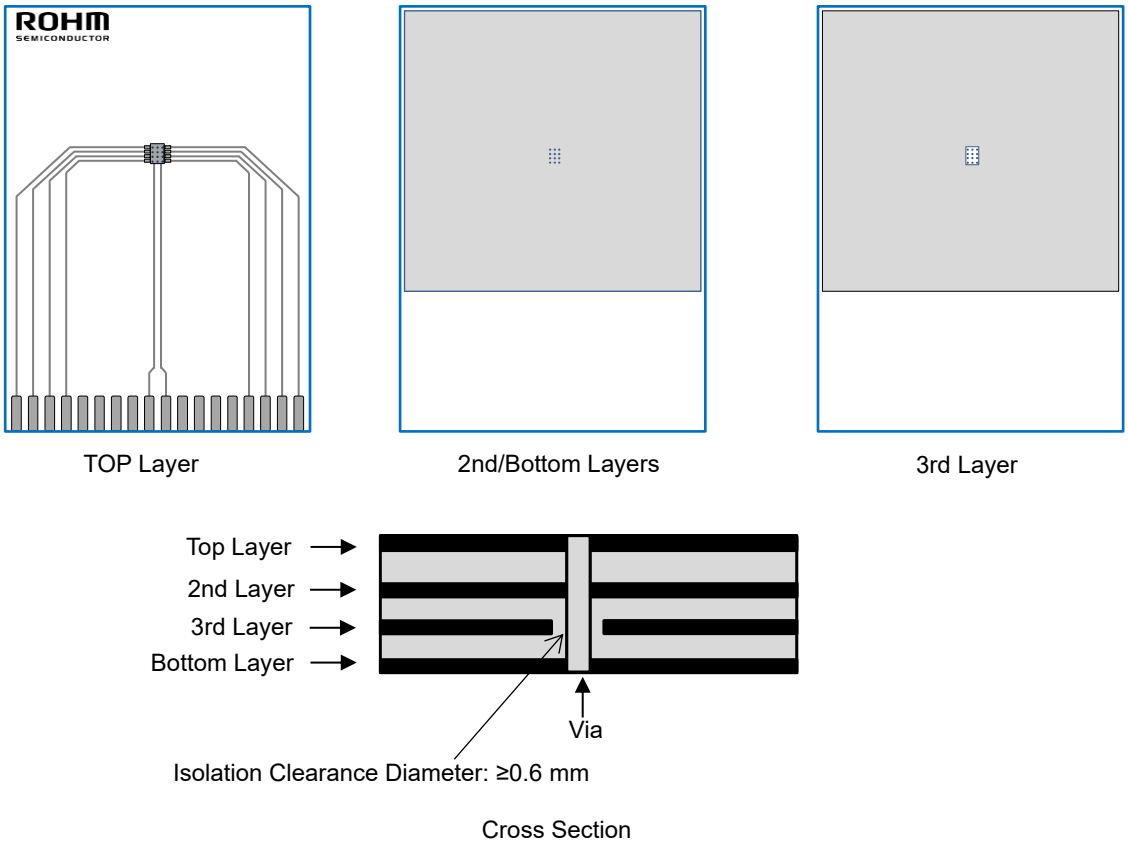



Figure 5. PCB-layout 4-layer (2s2p)

| Dimension | Value |
|---|---|
| Board Finish Thickness | 1.60 mm ± 10 % |
| Board Dimension | 76.2 mm x 114.3 mm |
| Board Material | FR4 |
| Copper Thickness (Top/Bottom Layers) | 0.070 mm (Cu +Plating) |
| Copper Thickness (Inner Layers) | 0.035 mm |
| Thermal Vias Separation/Diameter | 1.2 mm/0.3 mm |

## Thermal Resistance – continued

■ Transient Thermal Resistance (Single Pulse)

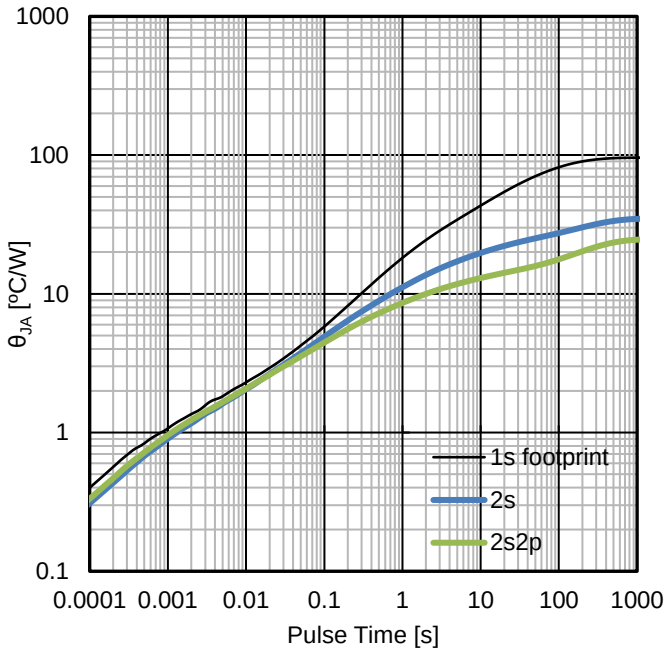



Figure 6. Transient Thermal Resistance

■ Thermal Resistance ($\theta_{JA}$ vs Copper Foil area 1s)

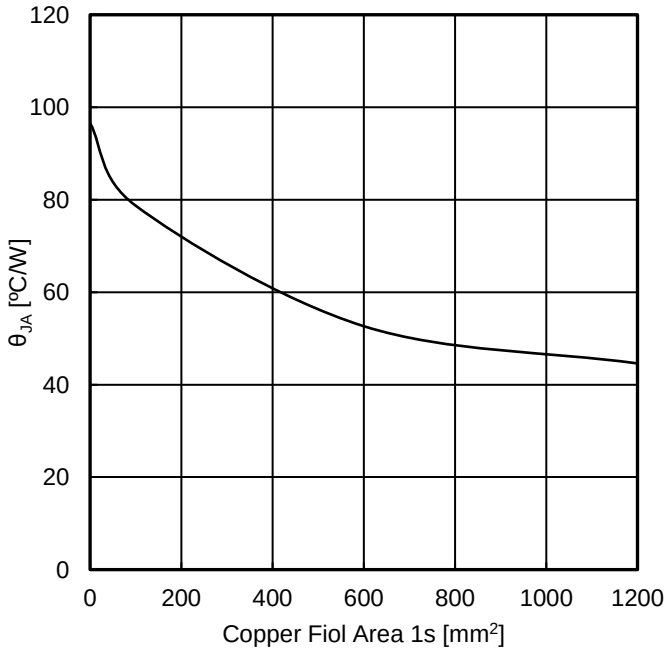



Figure 7. Thermal Resistance

### Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| VDD Power Supply Voltage | $V_{DD}$ | 4.0 | 5.0 | 5.5 | V |
| VDDIO Power Supply Voltage | $V_{DDIO}$ | 3.0 | 5.0 | 5.5 | V |
| Operating Temperature | Topr | -40 | +25 | +150 | °C |

### Electrical Characteristics
**(Unless otherwise specified $V_{DD}$ = 4.0 V to 5.5 V, $V_{DDIO}$ = 3.0 V to 5.5 V, Tj = -40 °C to +150 °C)**

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| [Power Supply] | | | | | | |
| VDD Standby Current | $I_{VDDS}$ | - | 0 | 20 | µA | $V_{IDLE}$ = 0 V<br>$V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 0 V |
| VDDIO Standby Current | $I_{VDDIOS}$ | - | 0 | 20 | µA | $V_{IDLE}$ = 0 V<br>$V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 0 V |
| VDD Operating Current | $I_{VDD}$ | - | 1.2 | 2.4 | mA | $V_{IDLE}$ = 5 V<br>$V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 5 V<br>OUTCTRLn[7:0] = FF *(Note 1)* |
| VDDIO Operating Current | $I_{VDDIO}$ | - | 30 | 150 | µA | $V_{IDLE}$ = 5 V<br>$V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 5 V<br>OUTCTRLn[7:0] = FF *(Note 1)* |
| VDD Power On Reset Voltage | $V_{PORA}$ | - | - | 4.0 | V | |
| VDDIO Power On Reset Voltage | $V_{PORD}$ | - | - | 2.7 | V | |
| [Input (IDLE, CSB, SCLK, SI, IN21, IN43, IN65)] | | | | | | |
| Low Level Input Voltage | $V_{IL}$ | 0 | - | $V_{DDIO}$ × 0.2 | V | |
| High Level Input Voltage | $V_{IH}$ | $V_{DDIO}$ × 0.7 | - | $V_{DDIO}$ | V | |
| Input Hysteresis Voltage | $V_{HYS}$ | 0.25 | 0.45 | 0.65 | V | |
| Low Level Input Current 1 (except CSB) | $I_{IL1}$ | -10 | 0 | +10 | µA | $V_{IDLE}$, $V_{SCLK}$, $V_{SI}$, $V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 0 V |
| Low Level Input Current 2 (CSB) | $I_{IL2}$ | -100 | -50 | -25 | µA | $V_{CSB}$ = 0 V |
| High Level Input Current 1 (except CSB) | $I_{IH1}$ | 25 | 50 | 100 | µA | $V_{IDLE}$, $V_{SCLK}$, $V_{SI}$, $V_{IN21}$, $V_{IN43}$, $V_{IN65}$ = 5 V |
| High Level Input Current 2 (CSB) | $I_{IH2}$ | -10 | 0 | +10 | µA | $V_{CSB}$ = 5 V |
| [Output (SO)] | | | | | | |
| Low Level Output Voltage | $V_{OL}$ | 0 | 0.15 | 0.45 | V | $I_{SO}$ = 1 mA |
| High Level Output Voltage | $V_{OH}$ | $V_{DDIO}$ – 0.45 | $V_{DDIO}$ – 0.15 | - | V | $I_{SO}$ = -1 mA |
| Serial Out Output Leakage Current | $I_{SO}$ | -5 | 0 | +5 | µA | $V_{SO}$ = 0 V / 5.5 V |
| [Power MOS Output] | | | | | | |
| Output On Resistance | $R_{DS(ON)}$ | - | 650 | 800 | mΩ | $V_{DD}$ = 5 V<br>$I_{OUT}$ = 0.2 A, Tj = 25 °C |
| | | - | 1200 | 1500 | mΩ | $V_{DD}$ = 5 V<br>$I_{OUT}$ = 0.2 A, Tj = 150 °C |
| Output Leakage Current | $I_{OUT(L)}$ | - | 0 | 1 | µA | $V_{OUT}$ = 30 V, Tj = 25 °C |
| | | - | 0.15 | 2.00 | µA | $V_{OUT}$ = 30 V, Tj = 150 °C |
| Output Clamp Voltage | $V_{CL}$ | 37 | 41 | 45 | V | $I_{OUT}$ = 1 mA, Output Off |

*(Note 1)* Set by SPI control. Details are given in "Register Map". n represents the channel number.

**Electrical Characteristics – continued**
**(Unless otherwise specified, $V_{DD}$ = 4.0 V to 5.5 V, $V_{DDIO}$ = 3.0 V to 5.5 V, Tj = -40 °C to +150 °C)**

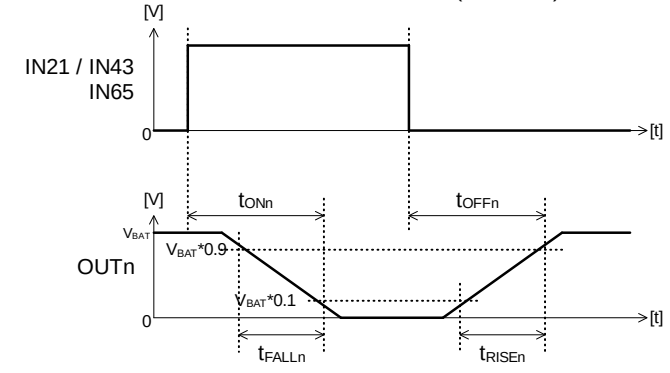
| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| [Power MOS Output] | | | | | | |
| Turn-On Time 1 | $t_{ON1}$ | - | - | 50 | µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 00 *(Note 1)* |
| Turn-Off Time 1 | $t_{OFF1}$ | - | - | 50 | µs | |
| Turn-On Time 2 | $t_{ON2}$ | - | - | 200 | µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 10 *(Note 1)* |
| Turn-Off Time 2 | $t_{OFF2}$ | - | - | 200 | µs | |
| Turn-On Time 3 | $t_{ON3}$ | - | - | 25 | µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 01 *(Note 1)* |
| Turn-Off Time 3 | $t_{OFF3}$ | - | - | 25 | µs | |
| Slew Rate (On) 1 | $SR_{ON1}$ | 0.50 | 1.00 | 1.50 | V/µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 00 *(Note 1)* |
| Slew Rate (Off) 1 | $SR_{OFF1}$ | 0.50 | 1.00 | 1.50 | V/µs | |
| Slew Rate (On) 2 | $SR_{ON2}$ | 0.10 | 0.30 | 0.50 | V/µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 10 *(Note 1)* |
| Slew Rate (Off) 2 | $SR_{OFF2}$ | 0.10 | 0.30 | 0.50 | V/µs | |
| Slew Rate (On) 3 | $SR_{ON3}$ | 1.35 | 2.25 | 3.15 | V/µs | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 01 *(Note 1)* |
| Slew Rate (Off) 3 | $SR_{OFF3}$ | 1.35 | 2.25 | 3.15 | V/µs | |
| PWM Output Range | $f_{PWM}$ | - | - | 5 | kHz | $R_L$ = 60 Ω, $V_{IDLE}$ = 5 V, $V_{BAT}$ = 12 V, SRCTRLn[1:0] = 00 *(Note 1)* |
| [Over Current Protection Function] | | | | | | |
| Over Current Threshold Value 1 | $I_{OCP1}$ | 0.50 | 0.85 | 1.30 | A | OCPCTRLn = '0' *(Note 1)* |
| Over Current Threshold Value 2 | $I_{OCP2}$ | 1.00 | 1.70 | 2.40 | A | OCPCTRLn = '1' *(Note 1)* |
| Output Stop Time at OCP Detection | $t_{OCP\_OFF}$ | 0.4 | 1.0 | 1.9 | ms | OCPCTRLn = '0' / '1' *(Note 1)* |
| Over Current Detection Time | $t_{OCP\_DET}$ | 2.3 | - | - | µs | OCPCTRLn = '0' / '1' *(Note 1)* |
| [Open Load Detection Function] | | | | | | |
| Open Load Detect Voltage | $V_{OLD\_DET}$ | 1.2 | 2.2 | 3.2 | V | DIAG_OLD/OFDn = '1' *(Note 1)* Output Off |
| Open Load Release Voltage | $V_{OLD\_REL}$ | 1.6 | 2.6 | 3.6 | V | |
| Output Sink Current | $I_{OLD}$ | 15 | 40 | 90 | µA | $V_{OUT}$ = 12 V |
| [Output Overhead Fault Detection Function] | | | | | | |
| Output Overhead Detect Voltage | $V_{OFD\_DET}$ | 1.6 | 2.6 | 3.6 | V | DIAG_OLD/OFDn = '1' *(Note 1)* Output On |
| Output Overhead Release Voltage | $V_{OFD\_REL}$ | 1.2 | 2.2 | 3.2 | V | |
| [Short Ground Detection Function] | | | | | | |
| Short Ground Detect Voltage | $V_{SGD\_DET}$ | 0.3 | 1.0 | 1.5 | V | DIAG_SGDn = '1' *(Note 1)* Output Off |
| Short Ground Release Voltage | $V_{SGD\_REL}$ | 0.5 | 1.4 | 1.9 | V | |
| Output Source Current | $I_{SGD}$ | -40 | -25 | -10 | µA | $V_{OUT}$ = 0 V |
| [Thermal Shutdown Function] | | | | | | |
| Detect Temperature *(Note 2)* | $T_{TSD\_DET}$ | 150 | 175 | 200 | °C | |
| Hysteresis Temperature *(Note 2)* | $T_{TSD\_HYS}$ | - | 15 | - | °C | |

*(Note 1)* Set by SPI control. Details are given in "Register Map". n represents the channel number.
*(Note 2)* Not 100 % are tested.

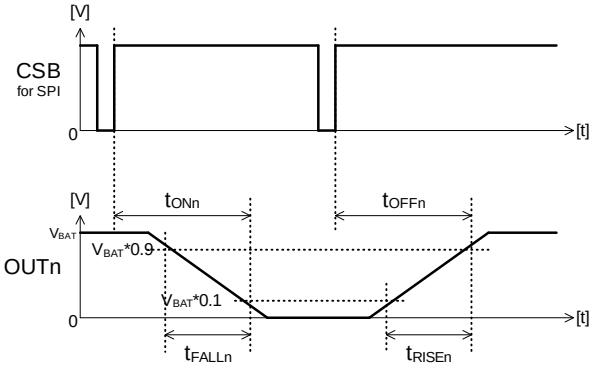
Switching Time Measurement Waveform

Control by IN21 / IN43/ IN65

$SR_{ON}$ = ($V_{BAT}$ * 0.8) / $T_{FALL}$
$SR_{OFF}$ = ($V_{BAT}$ * 0.8) / $T_{RISE}$




Control by SPI



**Typical Performance Curves**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

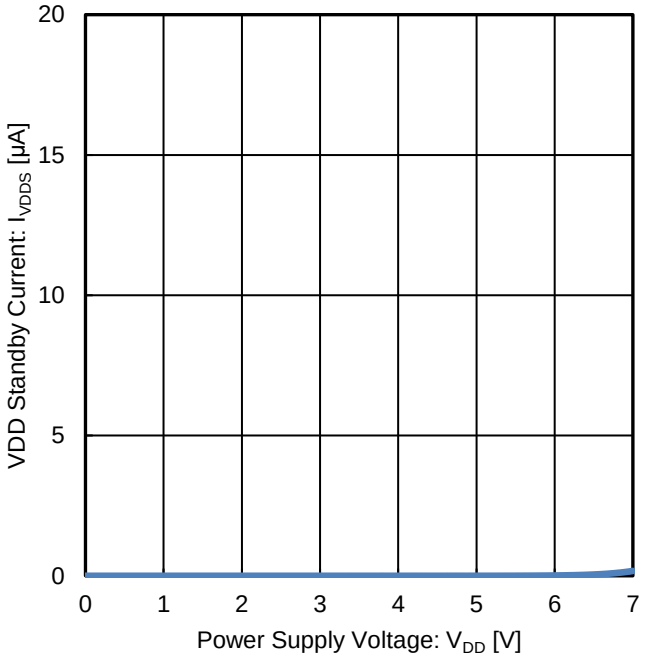



Figure 8. VDD Standby Current vs Power Supply Voltage

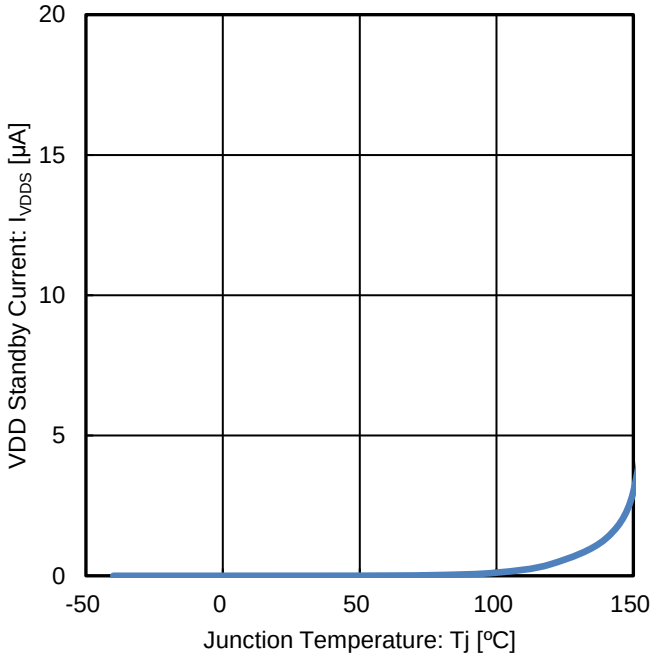



Figure 9. VDD Standby Current vs Junction Temperature

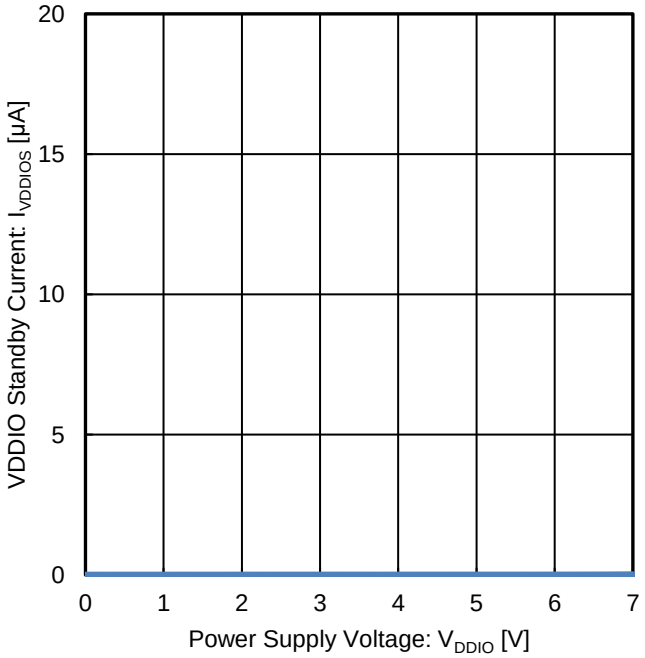



Figure 10. VDDIO Standby Current vs Power Supply Voltage

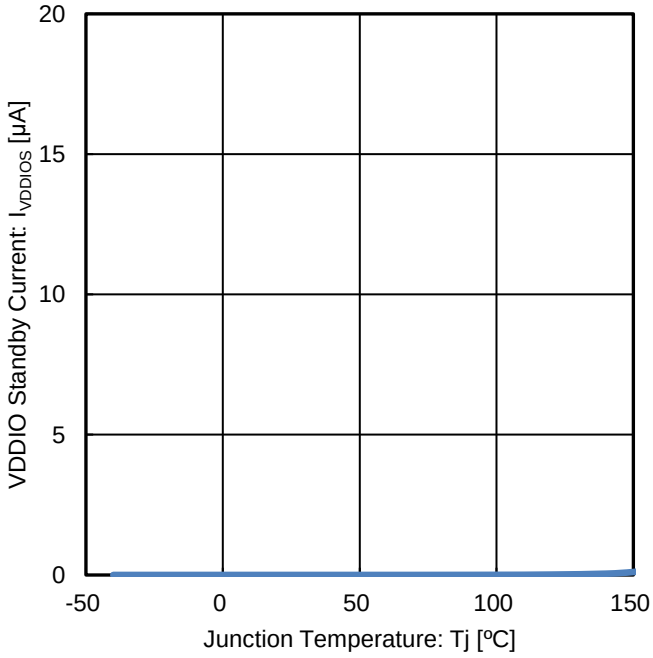



Figure 11. VDDIO Standby Current vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

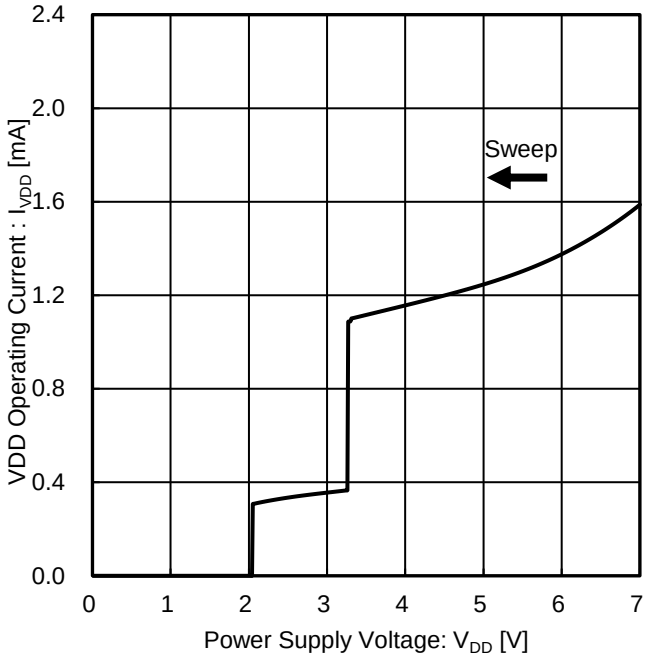



Figure 12. VDD Operating Current vs Power Supply Voltage

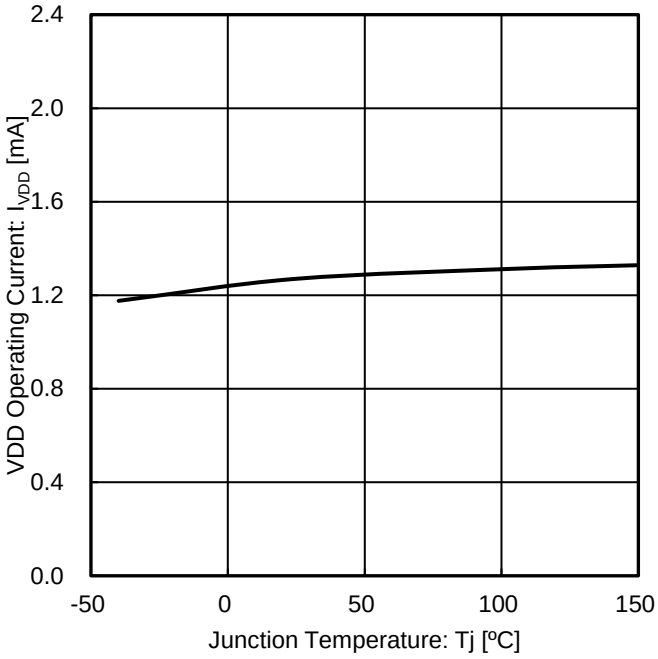



Figure 13. VDD Operating Current vs Junction Temperature

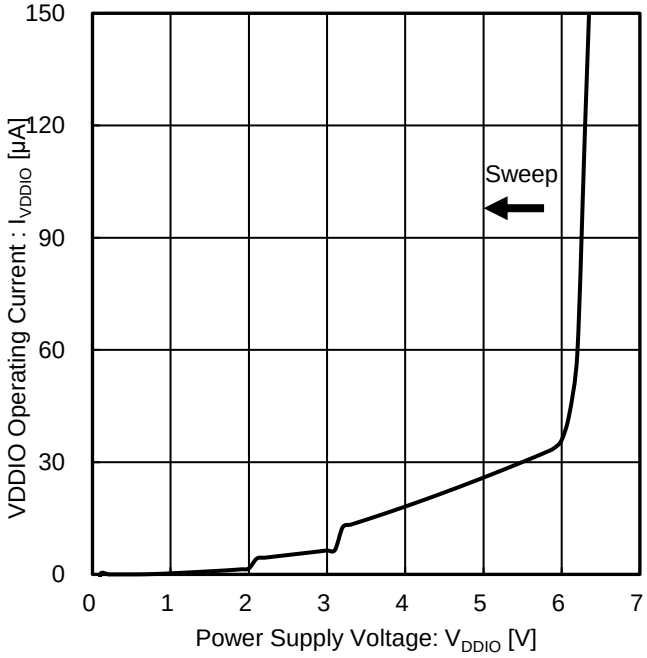



Figure 14. VDDIO Operating Current vs Power Supply Voltage

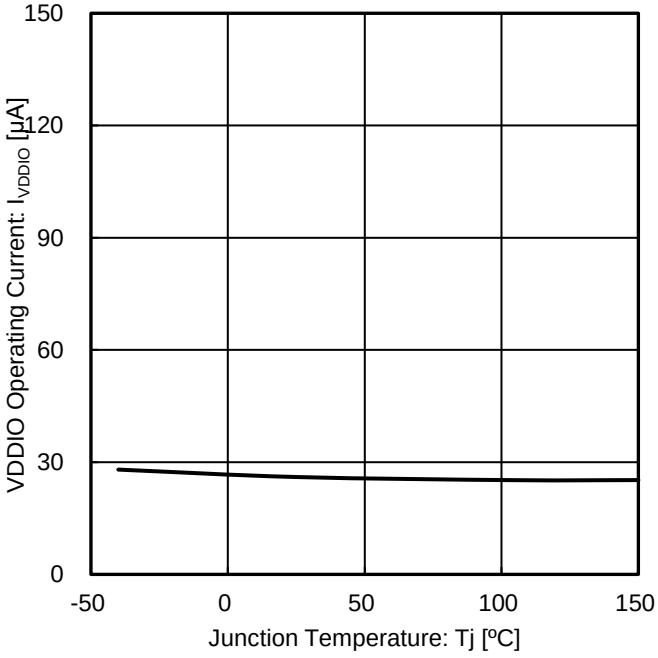



Figure 15. VDDIO Operating Current vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

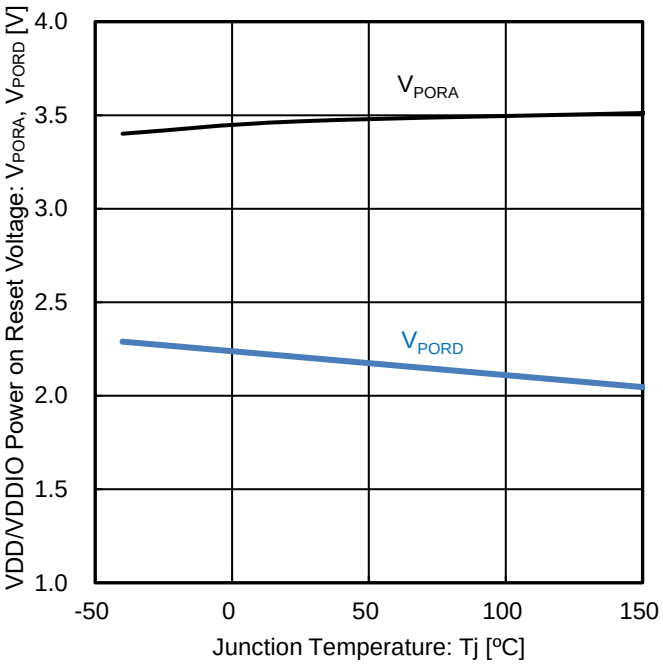



Figure 16. VDD/VDDIO Power On Reset Voltage vs Junction Temperature

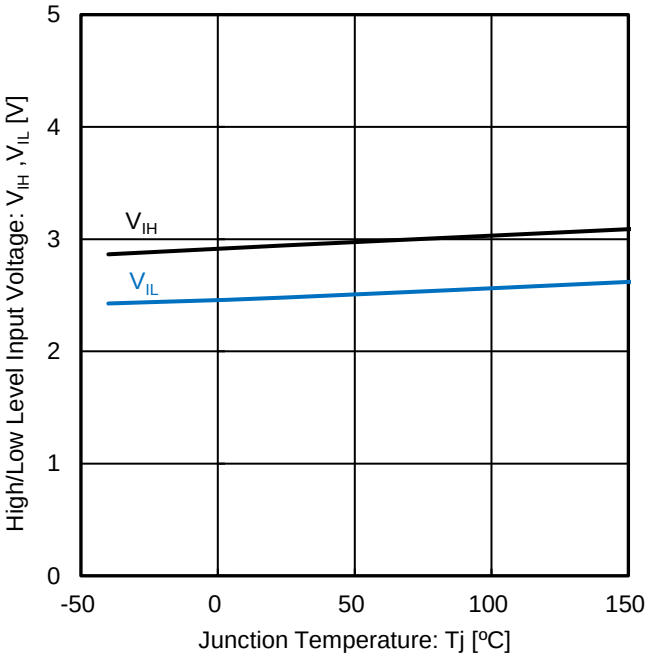



Figure 17. High/Low Level Input Voltage vs Junction Temperature

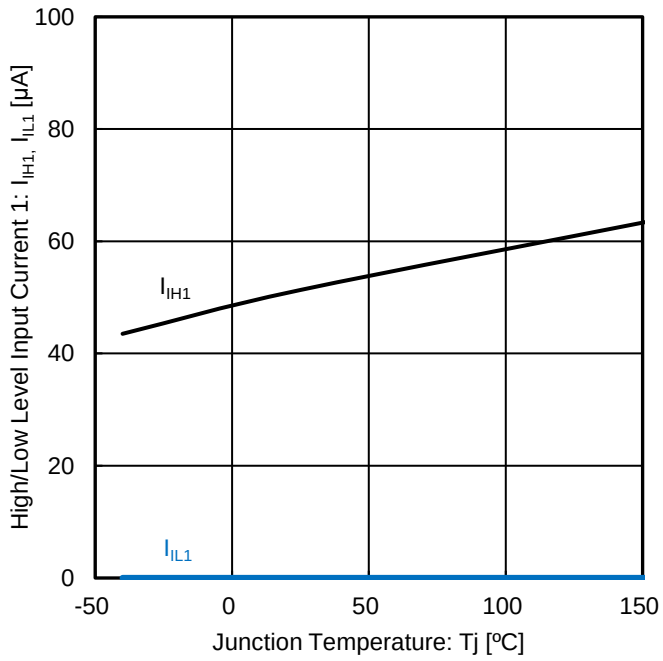



Figure 18. High/Low Level Input Current 1 vs Junction Temperature

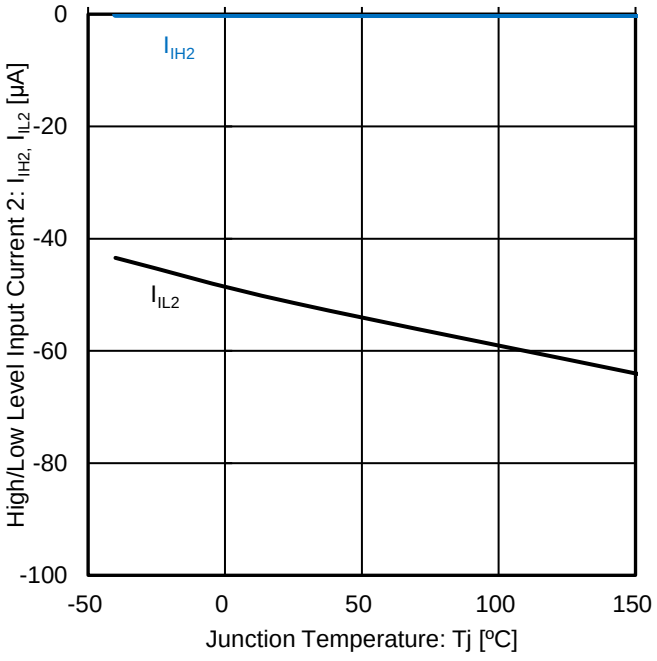



Figure 19. High/Low Level Input Current 2 vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

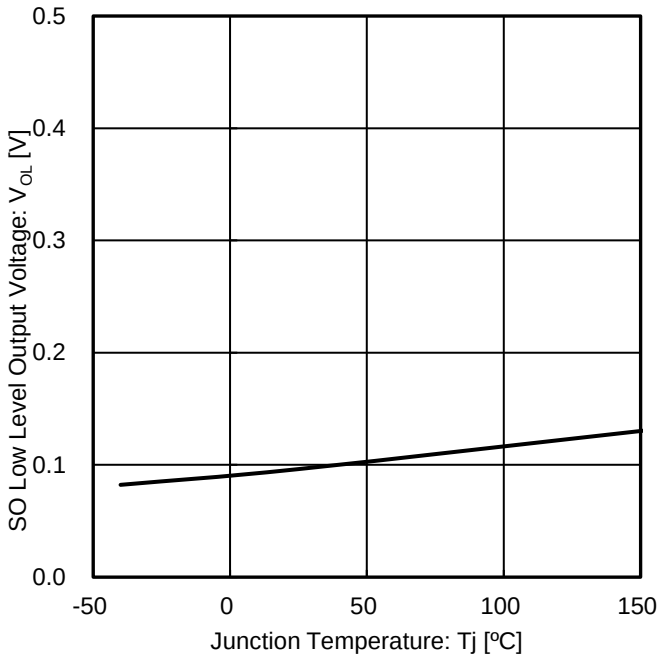



Figure 20. SO Low Level Output Voltage vs Junction Temperature

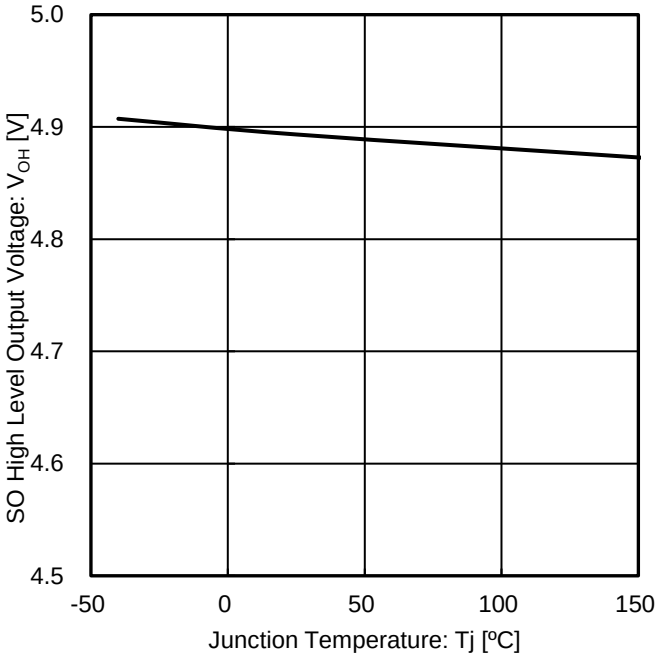



Figure 21. SO High Level Output Voltage vs Junction Temperature

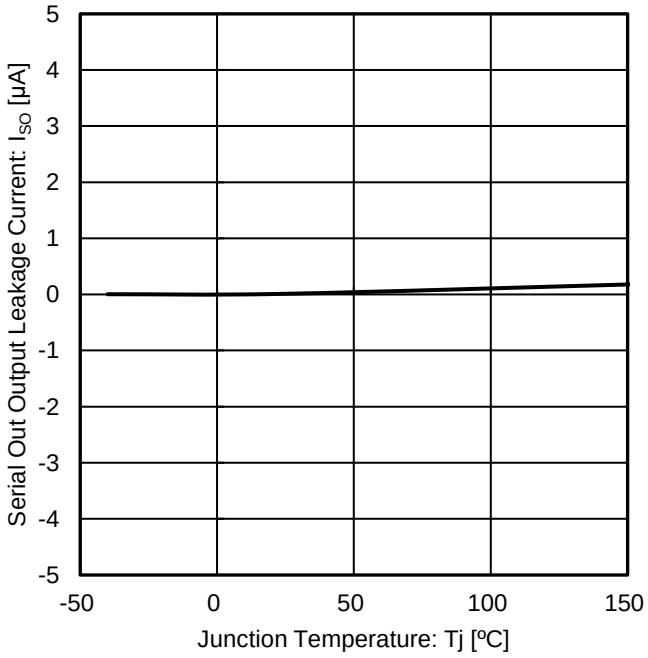



Figure 22. Serial Out Output Leakage Current vs Junction Temperature

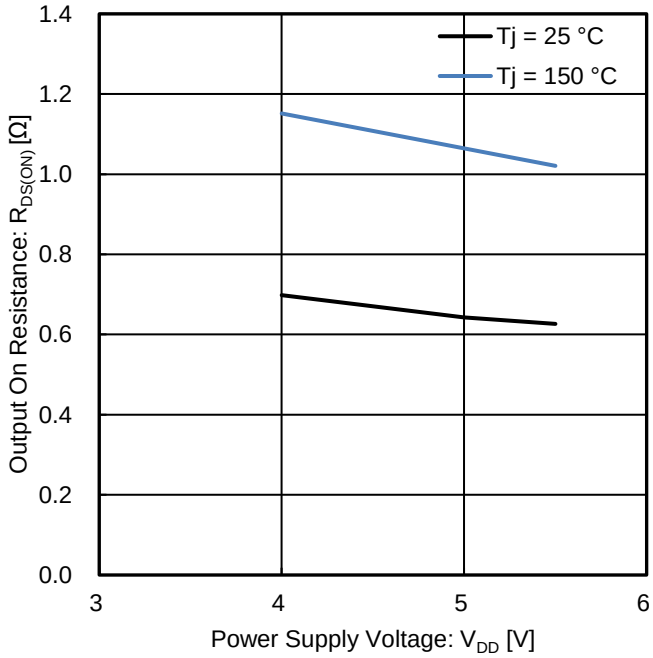



Figure 23. Output On Resistance vs Power Supply Voltage

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

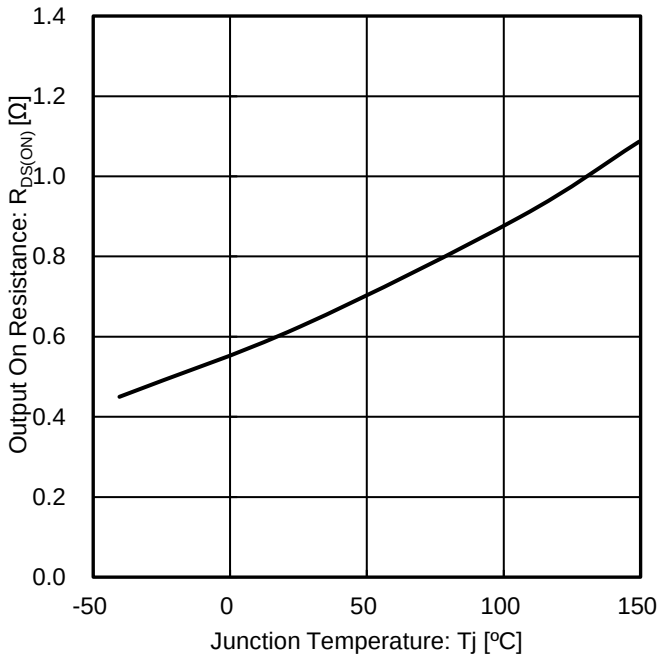



Figure 24. Output On Resistance vs Junction Temperature

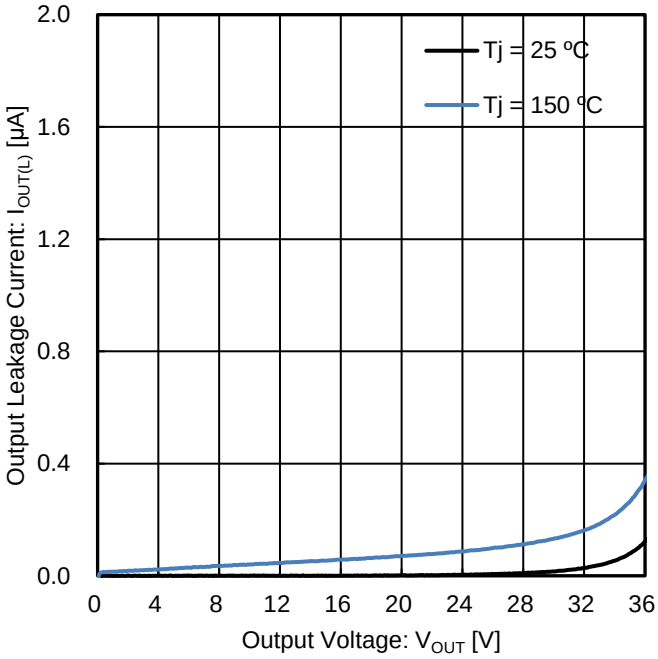



Figure 25. Output Leakage Current vs Output Voltage

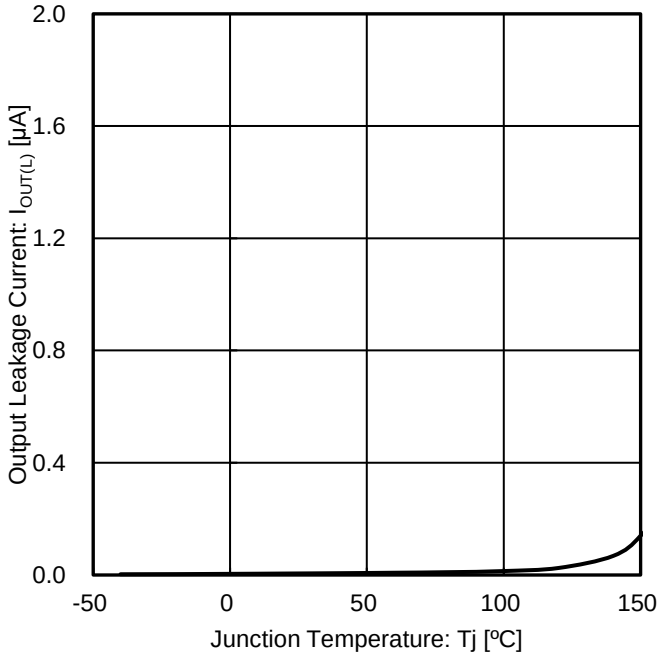



Figure 26. Output Leakage Current vs Junction Temperature

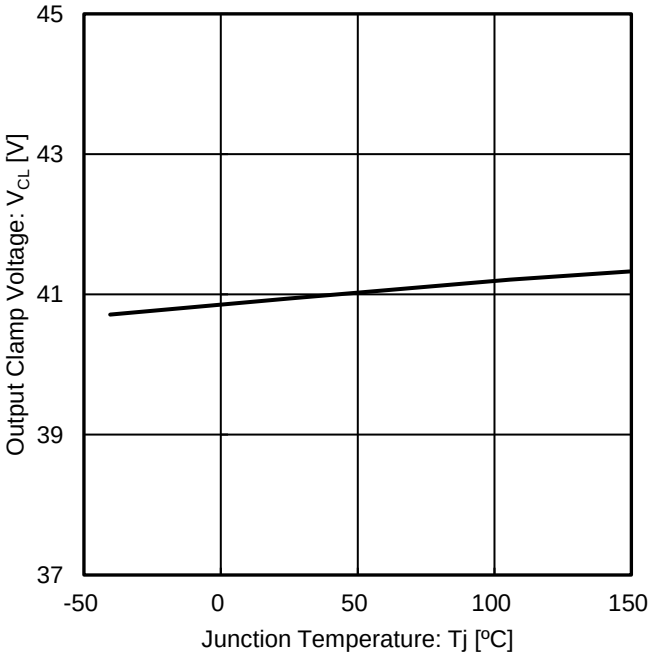



Figure 27. Output Clamp Voltage vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

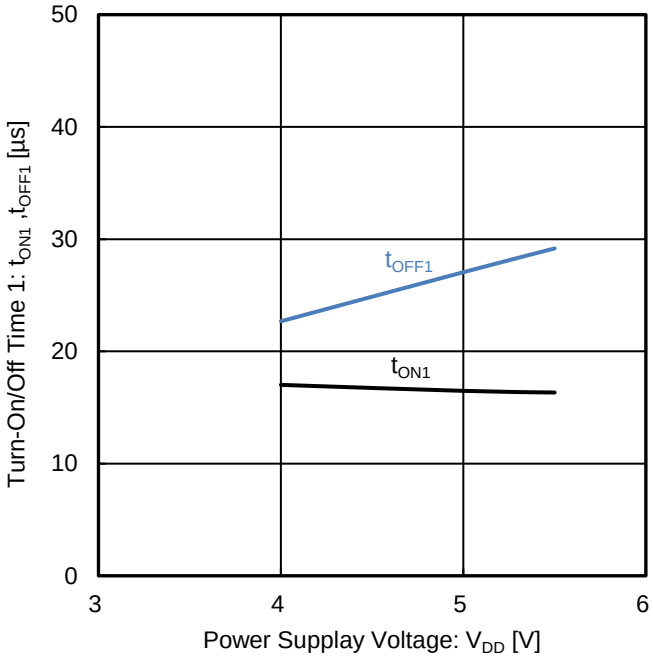



Figure 28. Turn-On/Off Time 1 vs Power Supply Voltage

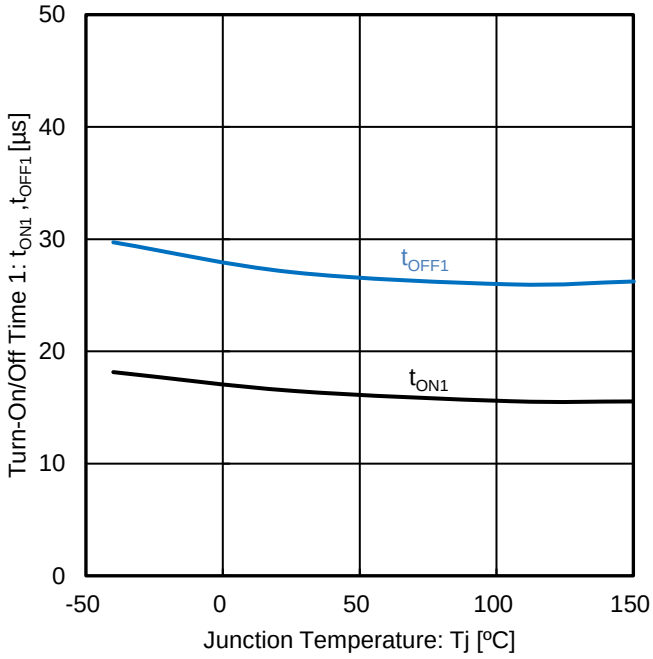



Figure 29. Turn-On/Off Time 1 vs Junction Temperature

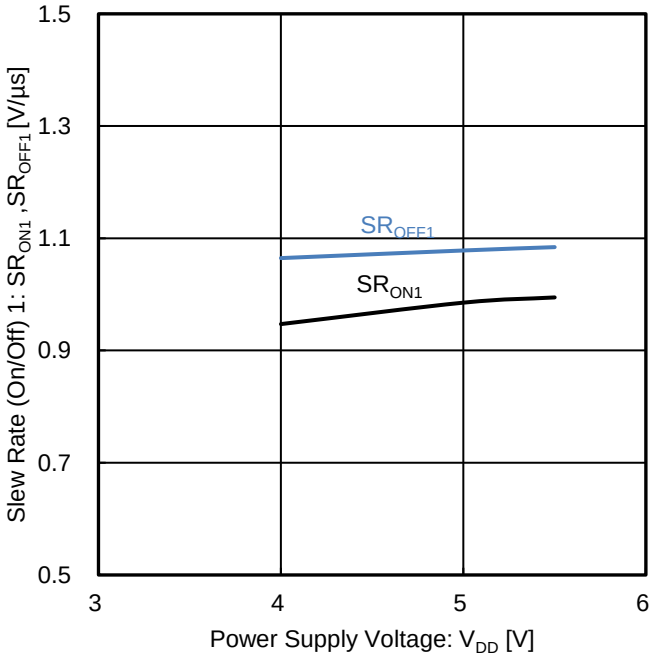



Figure 30. Slew Rate (On/Off) 1 vs Power Supply Voltage

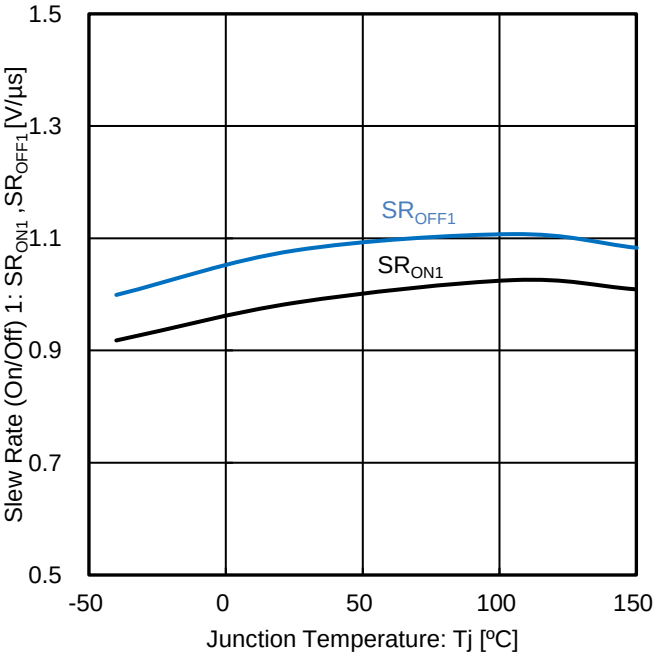



Figure 31. Slew Rate (On/Off) 1 vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

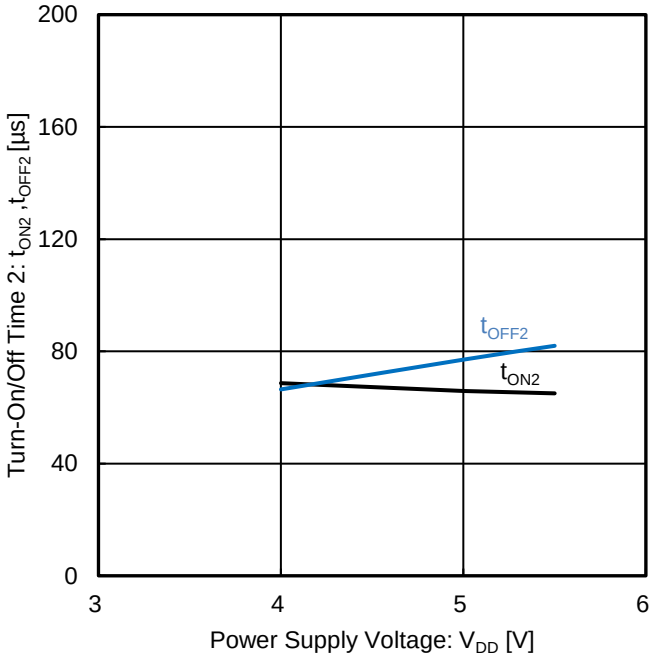



Figure 32. Turn-On/Off Time 2 vs Power Supply Voltage

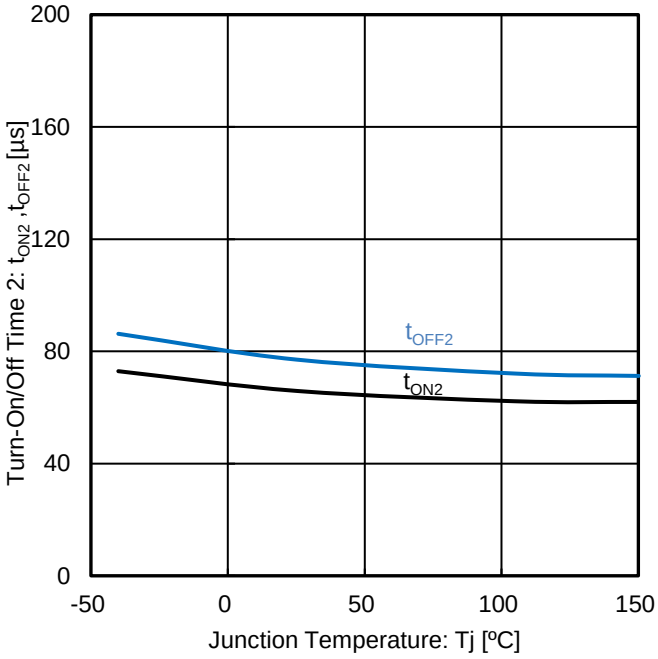



Figure 33. Turn-On/Off Time 2 vs Junction Temperature

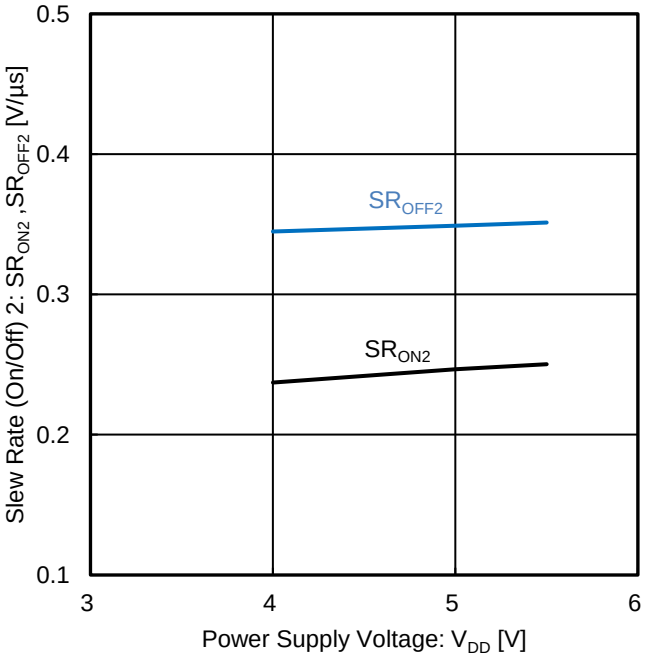



Figure 34. Slew Rate (On/Off) 2 vs Power Supply Voltage

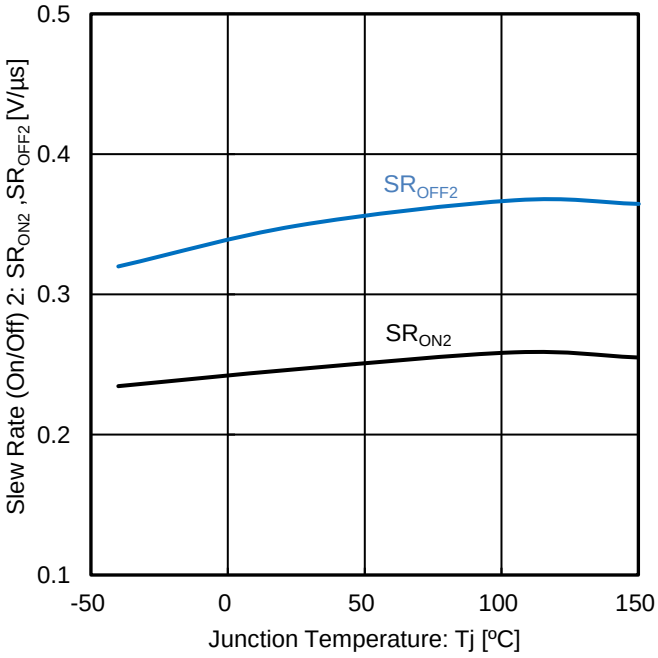



Figure 35. Slew Rate (On/Off) 2 vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

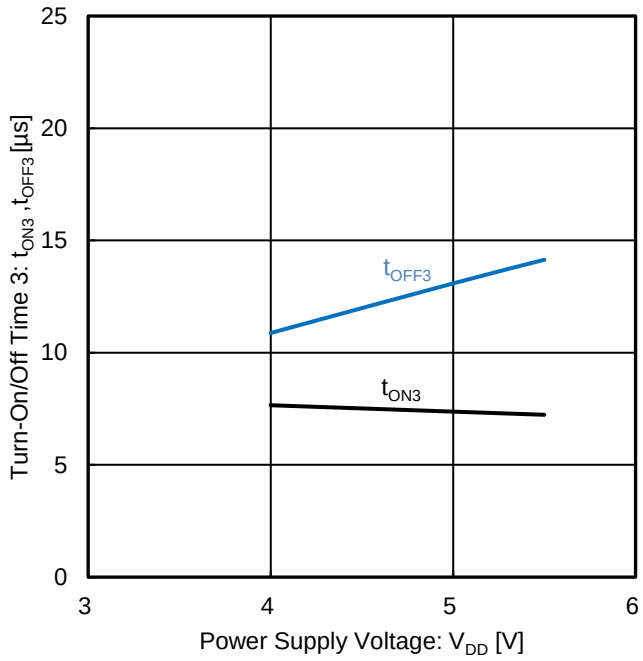



Figure 36. Turn-On/Off Time 3 vs Power Supply Voltage

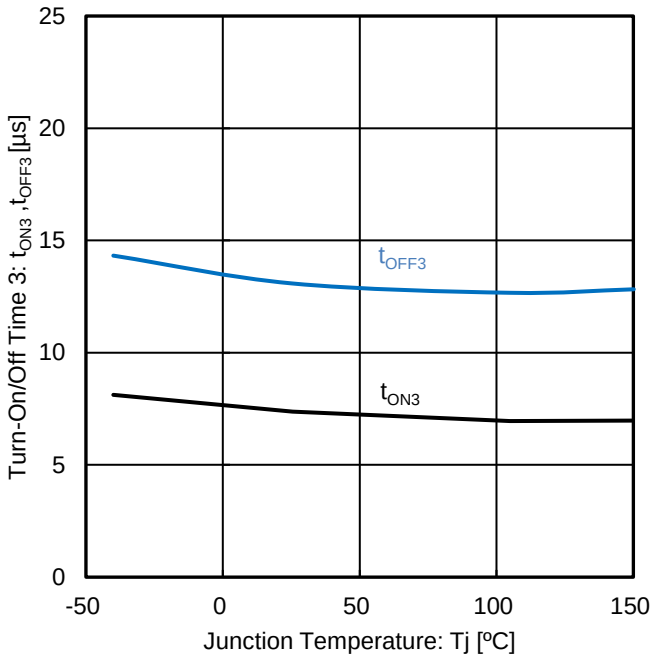



Figure 37. Turn-On/Off Time 3 vs Junction Temperature

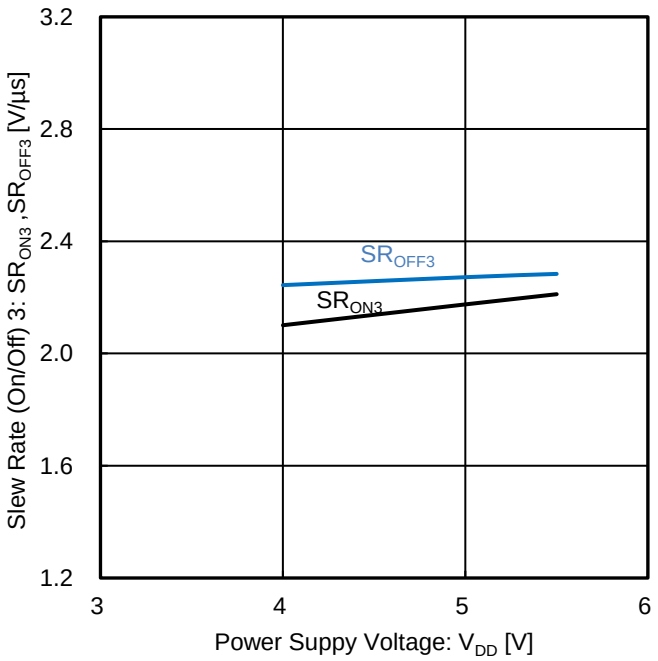



Figure 38. Slew Rate (On/Off) 3 vs Power Supply Voltage

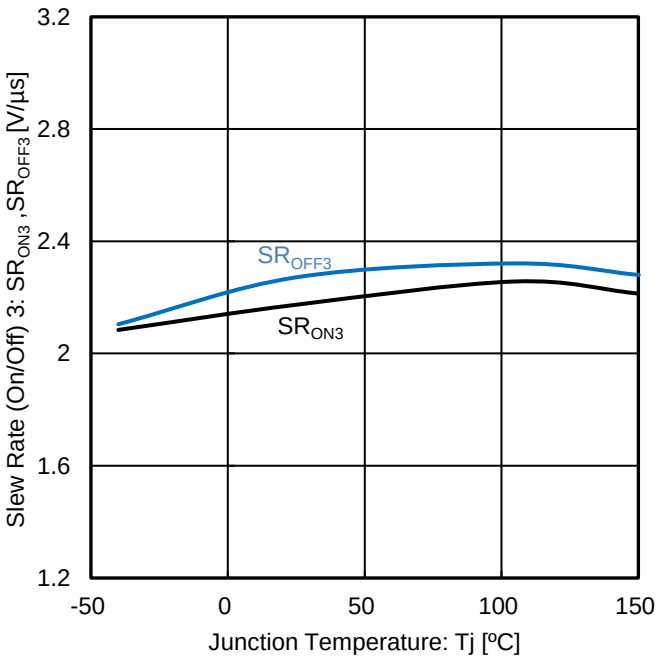



Figure 39. Slew Rate (On/Off) 3 vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

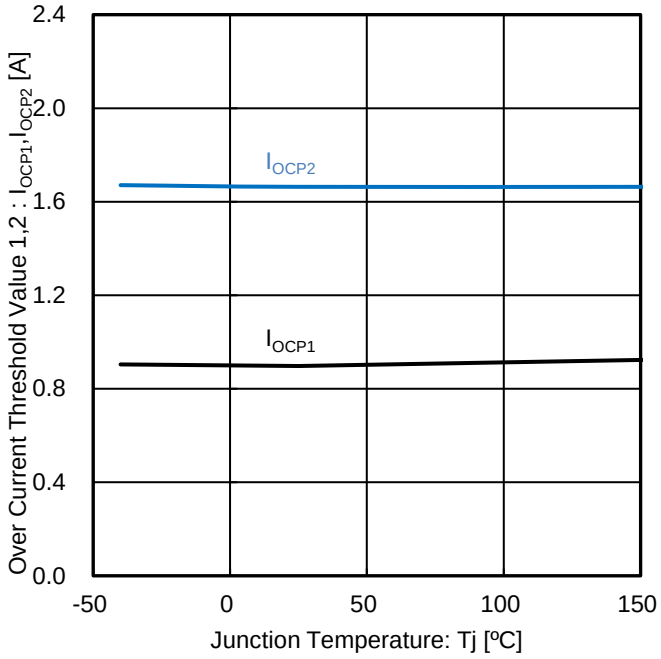



Figure 40. Over Current Threshold Value 1,2 vs Junction Temperature

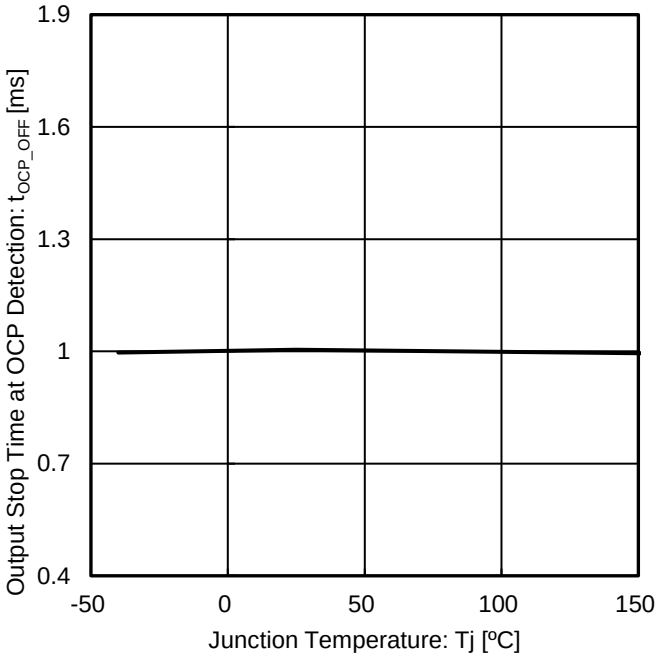



Figure 41. Output Stop Time at OCP Detection vs Junction Temperature

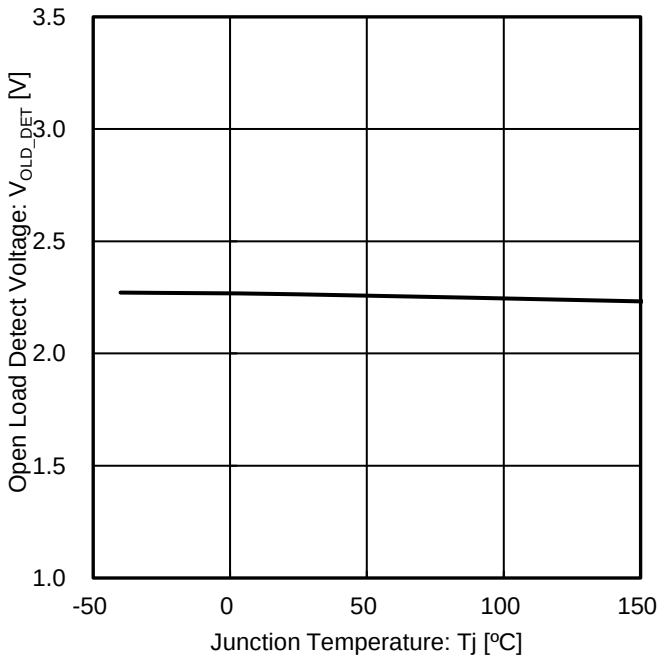



Figure 42. Open Load Detect Voltage vs Junction Temperature

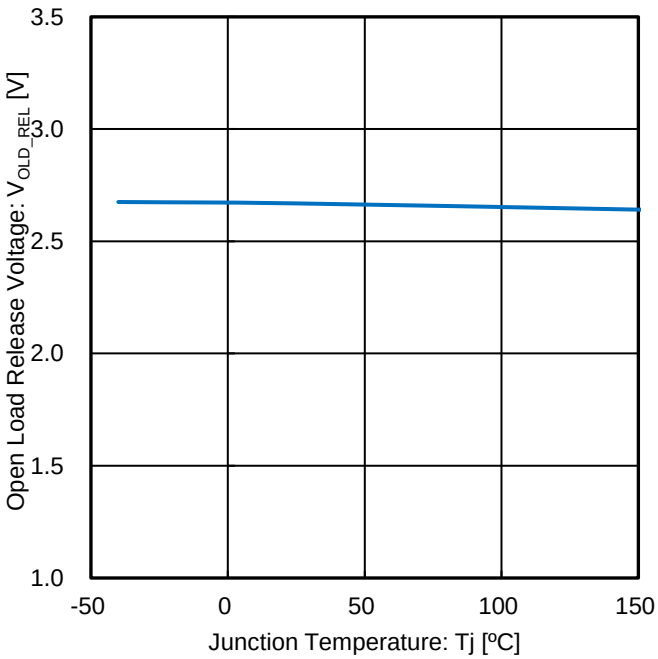



Figure 43. Open Load Release Voltage vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

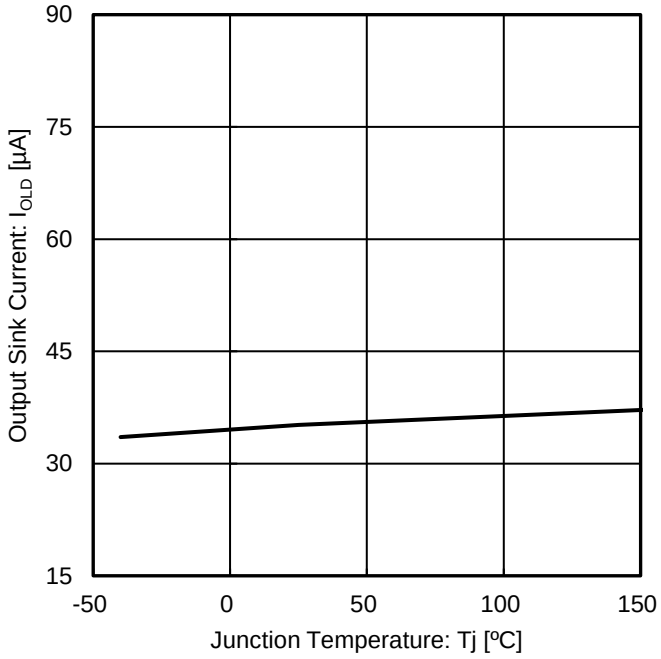



Figure 44. Output Sink Current vs Junction Temperature

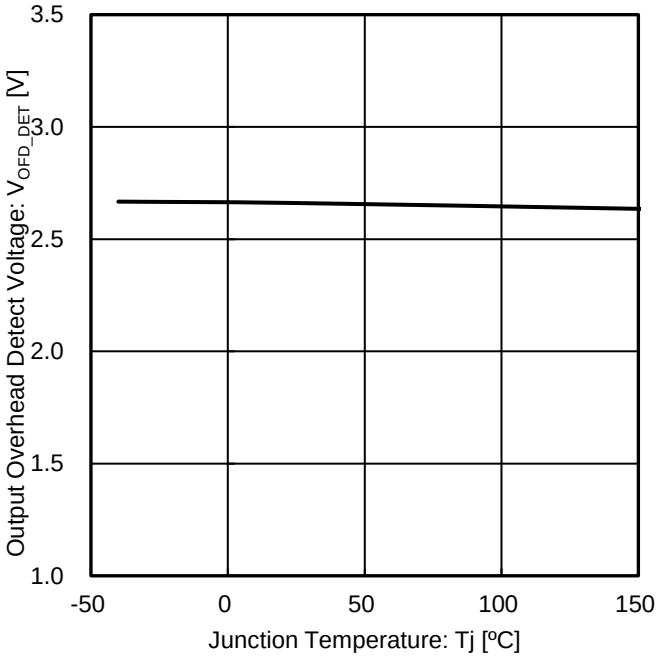



Figure 45. Output Overhead Detect Voltage vs Junction Temperature

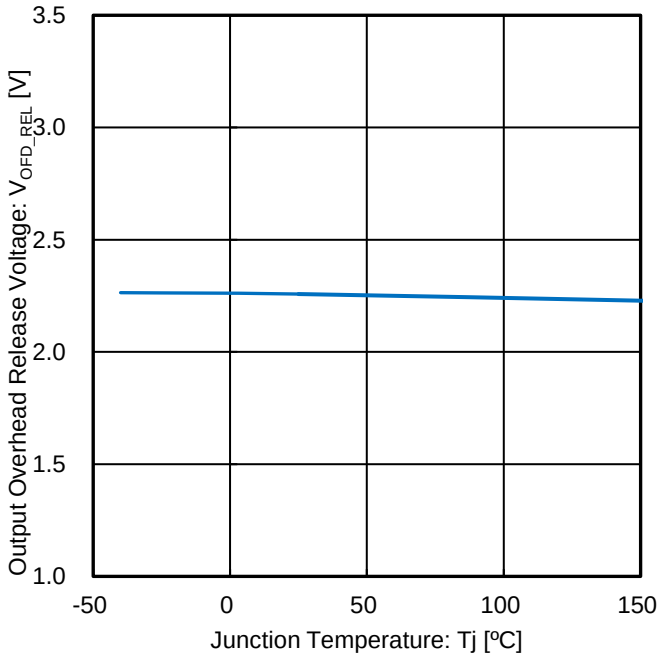



Figure 46. Output Overhead Release Voltage vs Junction Temperature

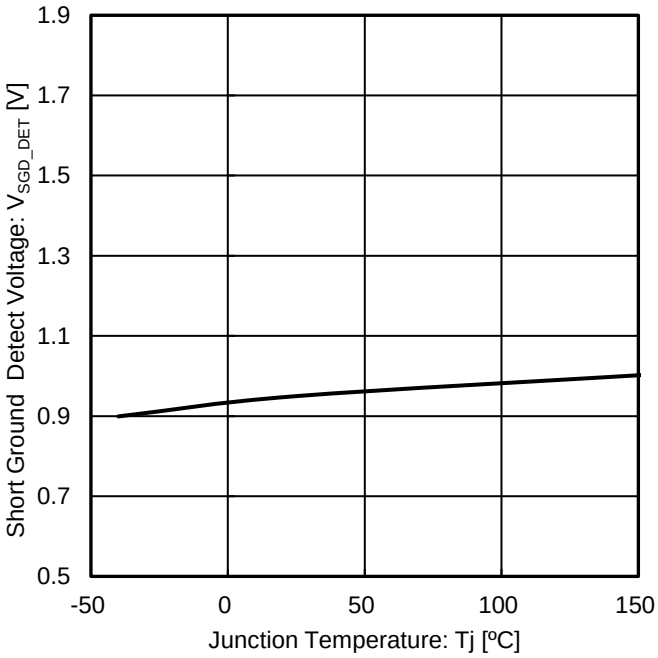



Figure 47. Short Ground Detect Voltage vs Junction Temperature

**Typical Performance Curves – continued**
(Reference data) (Unless otherwise specified, $V_{DD}$ = 5 V, $V_{DDIO}$ = 5 V, Tj = 25 °C)

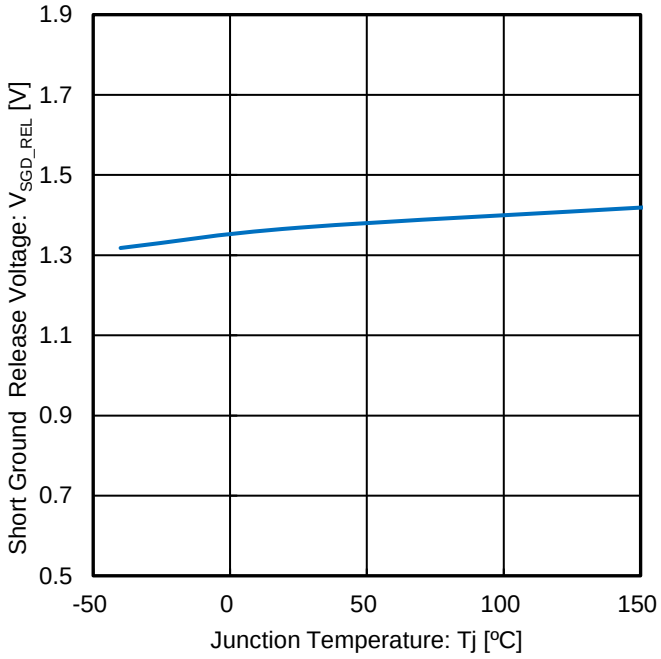



Figure 48. Short Ground Release Voltage vs Junction Temperature

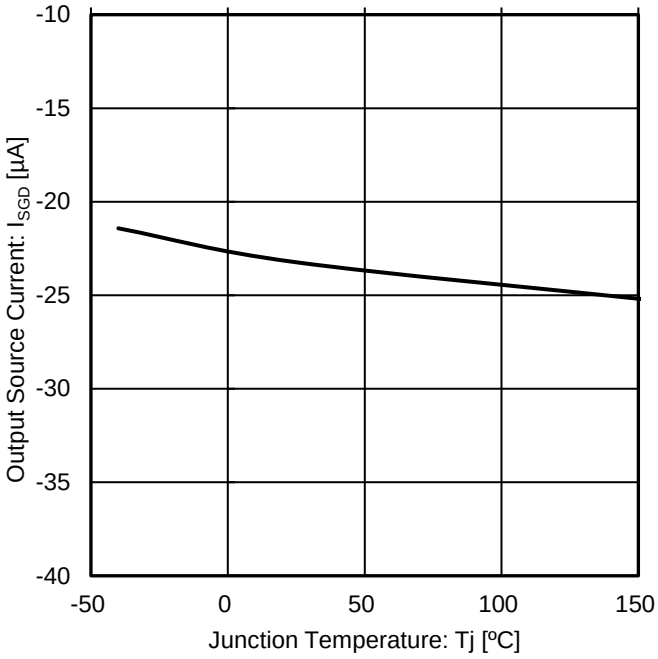



Figure 49. Output Source Current vs Junction Temperature

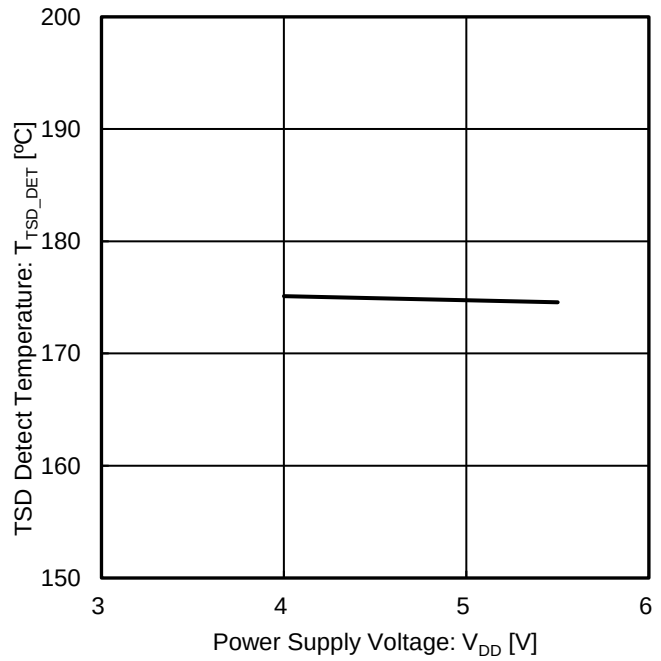



Figure 50. Thermal Shutdown Detect Temperature vs Power Supply Voltage

**Measurement Circuit**

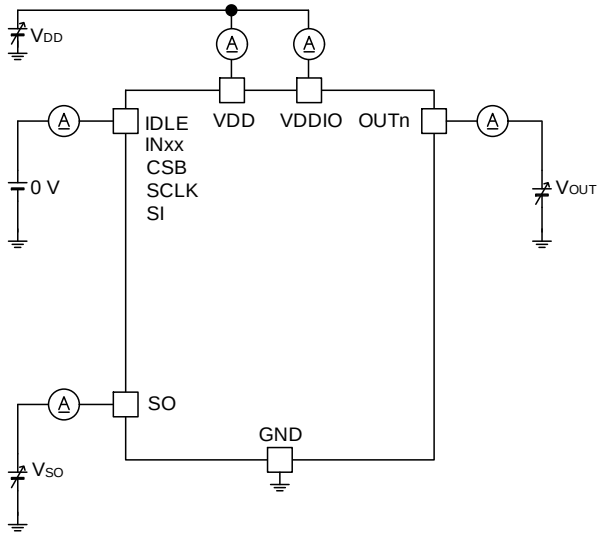



Figure 51. VDD Standby Current
VDDIO Standby Current
Low Level Input Current 1, 2
Output Leakage Current
Serial Out Output Leakage Current

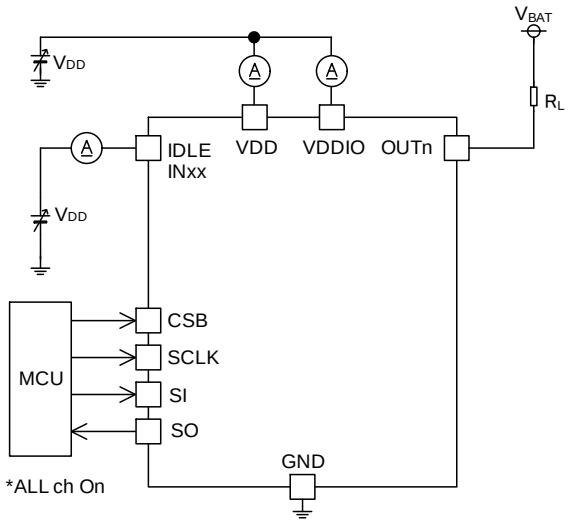



Figure 52. VDD Operating Current
VDDIO Operating Current
VDD Power On Reset Voltage
VDDIO Power On Reset Voltage
Thermal Shutdown Detect Temperature
Thermal Shutdown Hysteresis Temperature

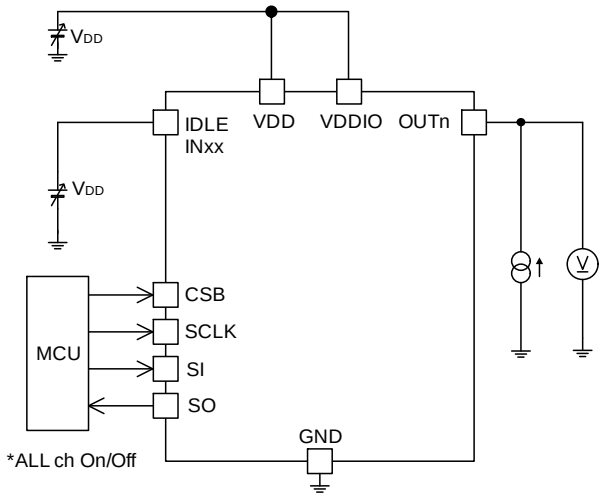



Figure 53. Output On Resistance
Output Clamp Voltage

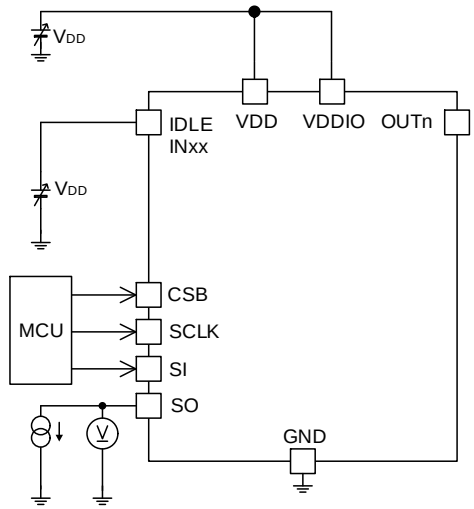



Figure 54. SO High/Low Level Output Voltage

**Measurement Circuit – continued**

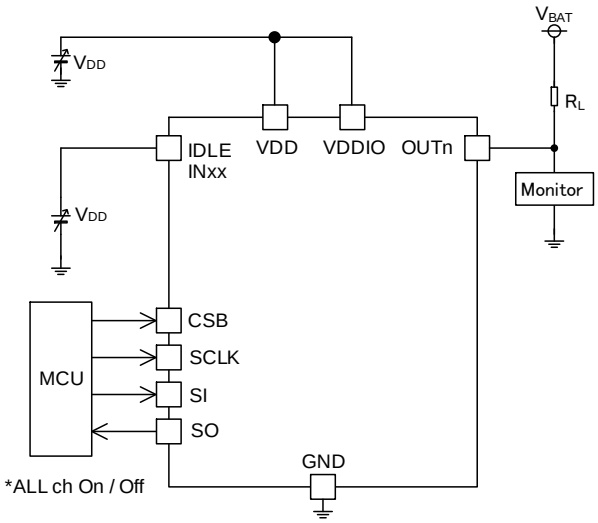



Figure 55. Slew Rate (On/Off) 1, 2, 3
Turn-On/Off Time 1, 2, 3

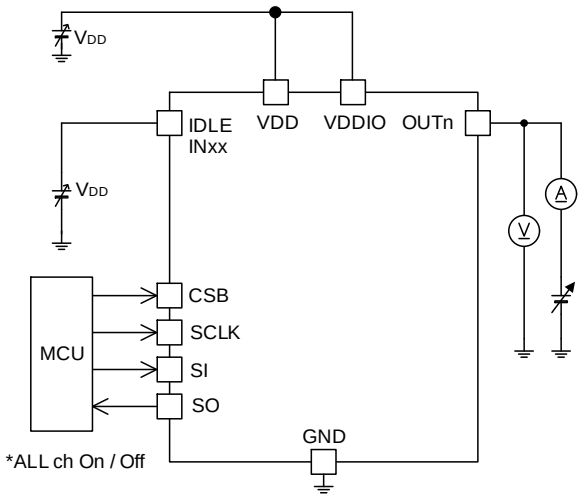



Figure 56. Open Load Detect/Release Voltage
Output Sink Current
Output Overhead Detect/Release Voltage
Short Ground Detect/Release Voltage
Output Source Current
Over Current Threshold Value 1, 2
Output Stop Time at OCP Detection

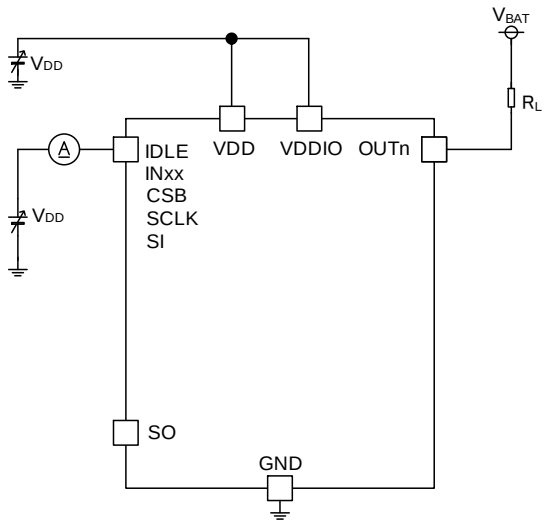
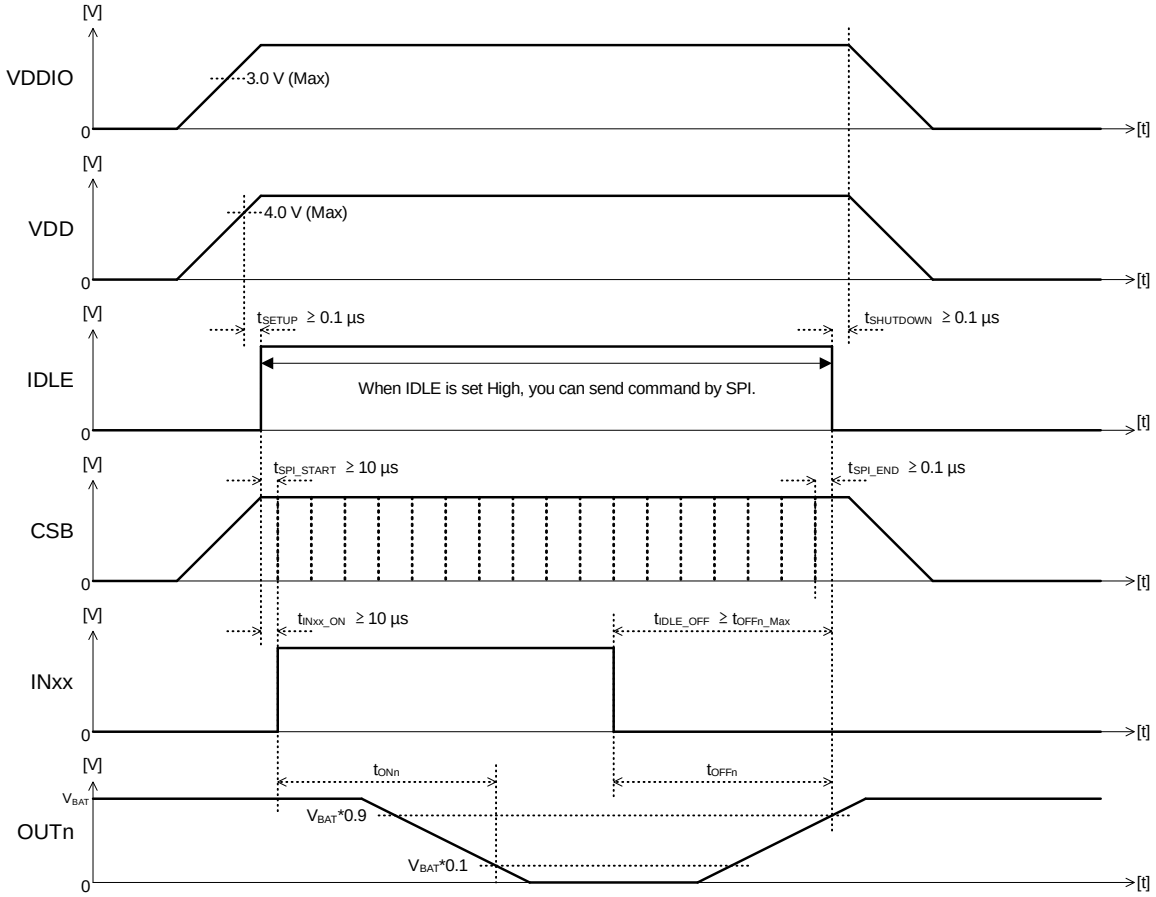



Figure 57. Low Level Input Voltage
High Level Input Voltage
Input Hysteresis Voltage
High Level Input Current 1, 2

### Timing Chart

The following shows the sequence when H is input to the IDLE pin after the power is supplied.
"xx" denotes each input (21, 43, 65), and n denotes the channel number.




(Supplement) About Each Symbol
$t_{SETUP}$: Time from VDDIO and VDD reaches operating voltage until H can be input to IDLE.

$t_{SPI\_START}$: Time from H is input to IDLE until SPI communication is available.
$t_{INxx\_ON}$: Time from H is input to IDLE until control by INxx is available.

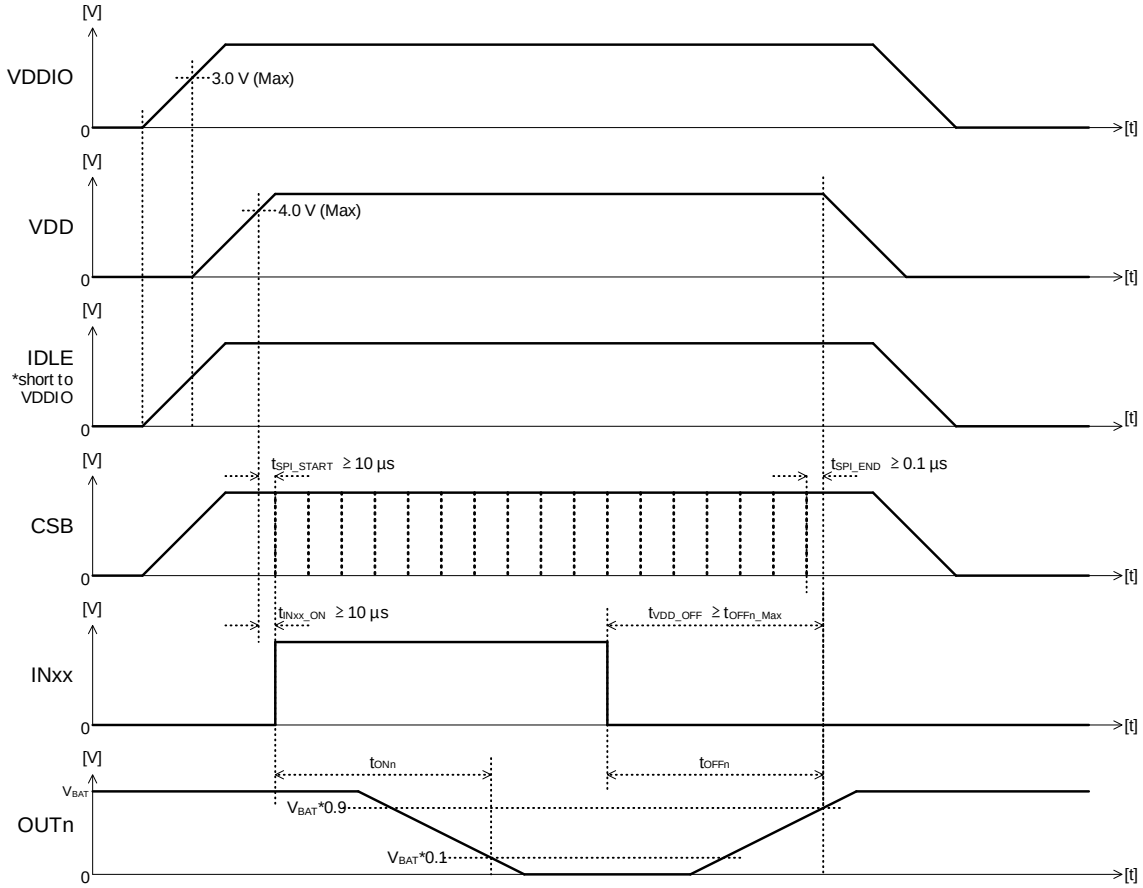
$t_{SPI\_END}$: Time from completion of SPI communication until L is input L to IDLE *(Note 1)*.
$t_{IDLE\_OFF}$: Time from end of control by INxx until input L to IDLE.

$t_{ONn}$: Turn-On time
$t_{OFFn}$: Turn-Off time
$t_{OFFn\_Max}$: Turn-Off Time (Max)

$t_{SHUTDOWN}$: Time from input L to IDLE until VDDIO and VDD are turned off.
*(Note 1)* If using SPI control to turn off low side SW, wait $t_{IDLE\_OFF}$ before inputting L to IDLE.

### Timing Chart – continued

The following shows the sequence when the VDDIO and IDLE pins are simultaneously turned on/off.
"xx" denotes each input (21, 43, 65), and n denotes the channel number.

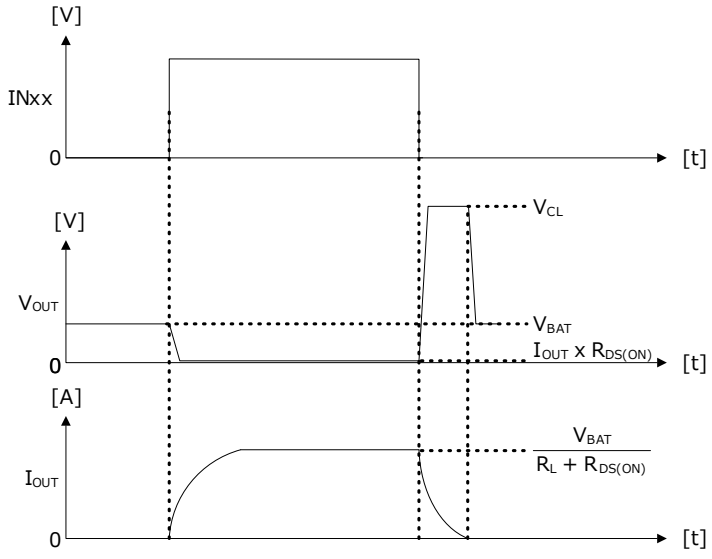



(Supplement) About Each Symbol
$t_{SPI\_START}$: Time from H is input to IDLE until SPI communication is available.
$t_{INxx\_ON}$: Time from VDD reaches operating voltage until control by INxx is available.

$t_{SPI\_END}$: Time from completion of SPI communication until lowering VDD*(Note 1)*.
$t_{VDD\_OFF}$: Time from end of control by INxx until lowering VDD.

$t_{ONn}$: Turn-On time
$t_{OFFn}$: Turn-Off time
$t_{OFFn\_Max}$: Turn-Off time (Max)
*(Note 1)* If using SPI control to turn off low side SW, wait $t_{VDD\_OFF}$ before lowering VDD.

Inductive Load Operation

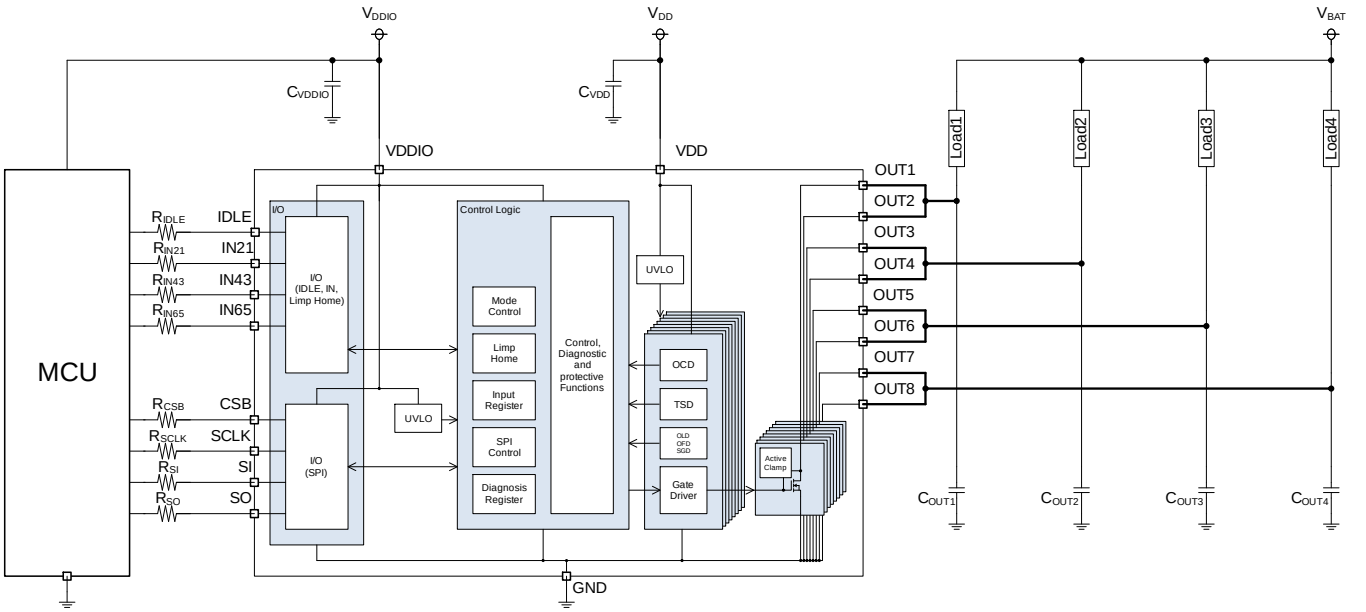


### Synchro Mode

Two adjacent output pins can be connected in parallel. Parallel connection is available by combining OUT1/OUT2, OUT3/OUT4, OUT5/OUT6, OUT7/OUT8. The synchro mode can be set by SPI. For details, refer to "Register Map".

When controlling by IN21/IN43/IN65, channels connected in parallel are driven simultaneously.
All control by SPI is set from the odd number channel, and the even number channel setting is ignored. For example, to turn on OUT1/OUT2, write "1" to OUTCTRL1 bit of OUTCTRL register. Writing to OUTCTRL2 bit is ignored.

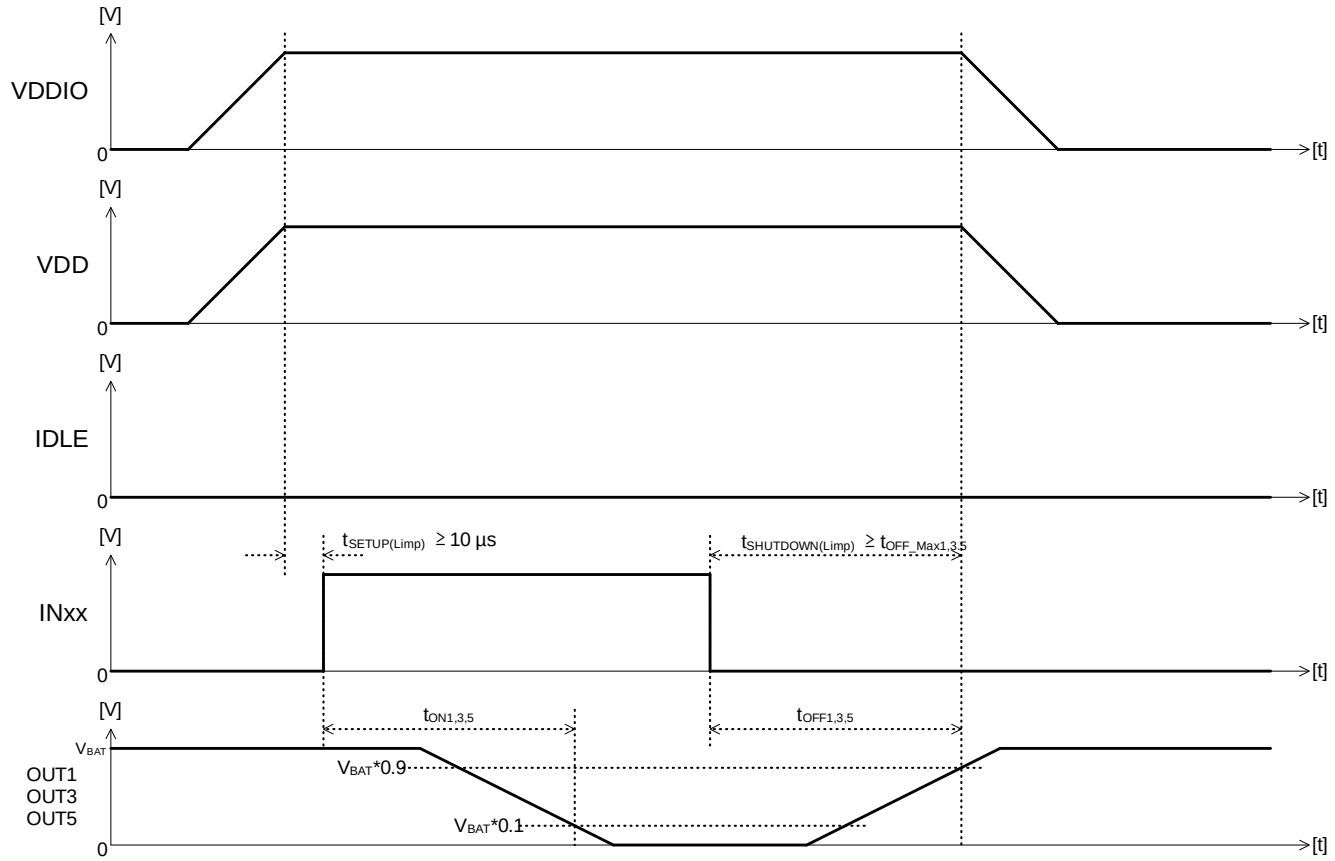
Over current protection and thermal shutdown is active on each channel connected in parallel, and both channels are turned off when protection is detected in either channel.
The detection of protection can be read from SPI by accessing DIAG_OUT4321 or DIAG_OUT8765 registers.
The error flag is output from the odd number channel and the error flag of the even number channel is fixed to "0". For example, if over current protection is detected in OUT1/OUT2, "1" is output from DIAG_OCP1 bit of DIAG_OUT4321 register, and DIAG_OCP2 bit outputs "0".




Caution: Differences in wire impedance between two neighboring outputs may affect characteristics such as turn-On/Off, slew rate, over current threshold value, and active clamp energy. To avoid this, it is recommended to short output pin with near the IC as possible.

### Limp Home Mode

When IDLE is set to L, the IC enters Limp Home mode. This mode enables operation with low current consumption. Control by SPI is not possible in this mode, but on/off control by IN21/IN43/IN65 is available. Controllable channels are limited to odd number channels (1ch, 3ch, 5ch). When IDLE becomes L, the register is cleared and returns to the default setting.
The timing chart in Limp Home mode is shown below.



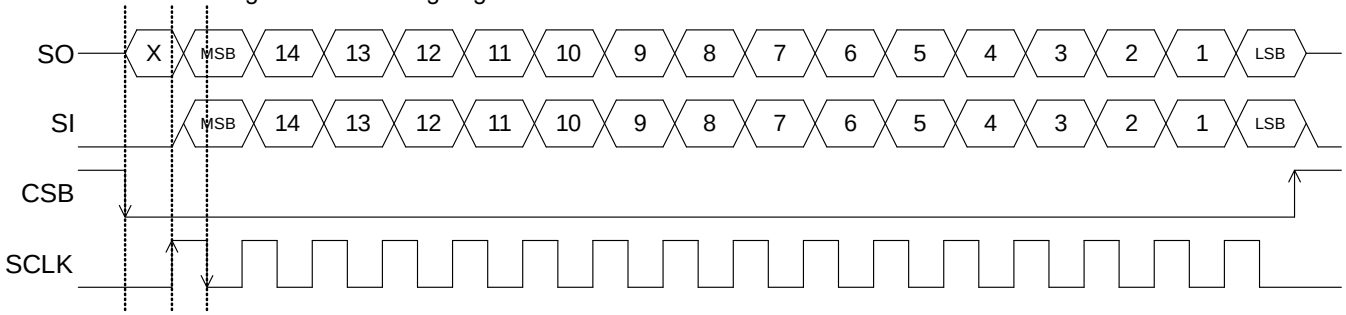

(Supplement) About Each Symbol
$t_{SETUP(Limp)}$: Time from VDDIO and VDD reaches operating voltage until control by INxx is available.

$t_{ON1,3,5}$: Turn-On time
$t_{OFF1,3,5}$: Turn-Off time
$t_{OFF\_Max1,3,5}$: Turn-Off time (Max)

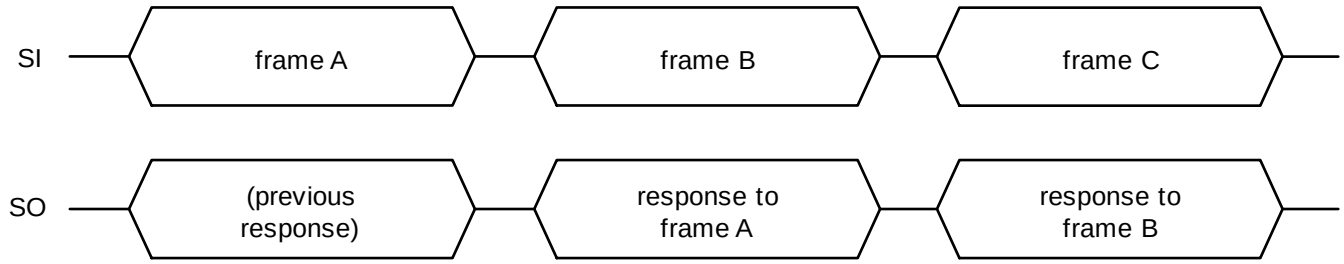
$t_{SHUTDOWN(Limp)}$: Time from all INxx is set to L until VDDIO and VDD are turned off.

### SPI Specification

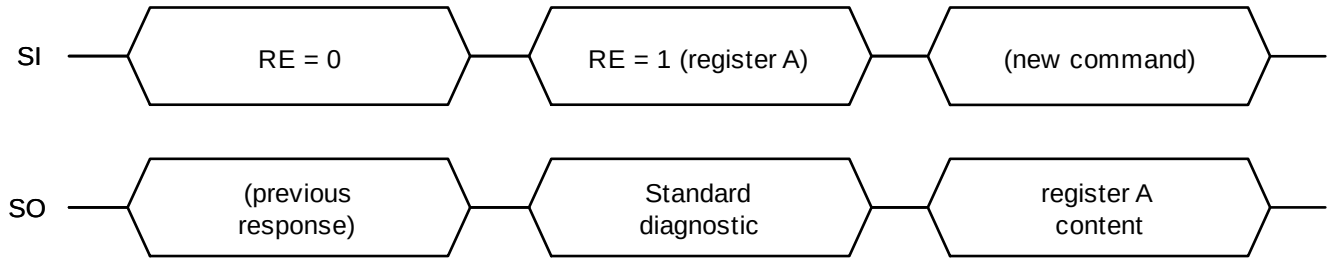
SPI overview
When CSB = H
SO is High-Z.
When CSB = L
Outputs to SO at the rising edge of SCLK.
SI is loaded into the register at the falling edge of SCLK.




SPI protocol
The SO response to SPI access is returned at the next SPI access as shown in the following figure.



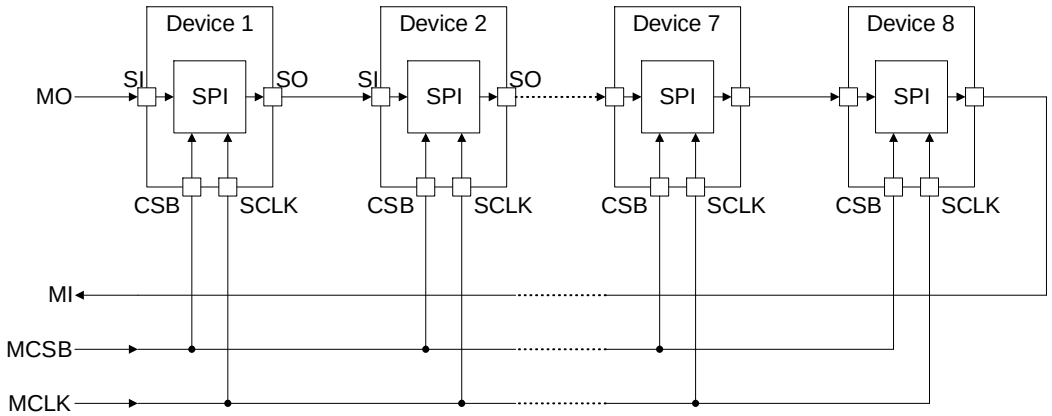

·Response when accessing with RE = 0 and with RE = 1
When accessing with RE = 0, respond “Standard diagnostic”.
When accessing with RE = 1, respond the value of the specified register.



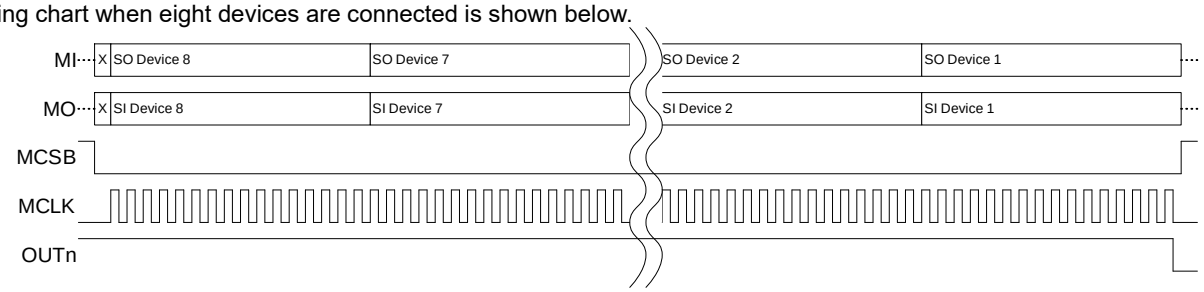
### SPI Specification – continued

Serial Daisy Chain

Multiple devices can be connected in series as shown below.
For CSB signal and SCLK signal, connect a common signal. About SI / SO line, SO of Device 1 can be connected to SI of Device 2 as shown below.

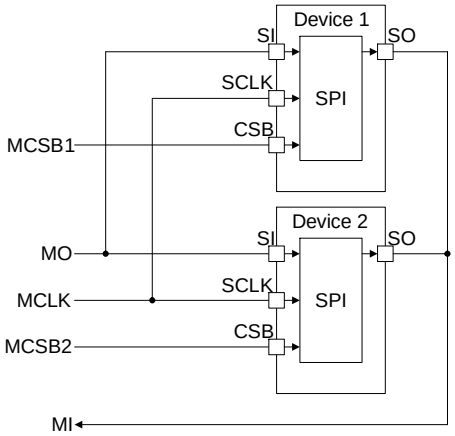



The timing chart when eight devices are connected is shown below.

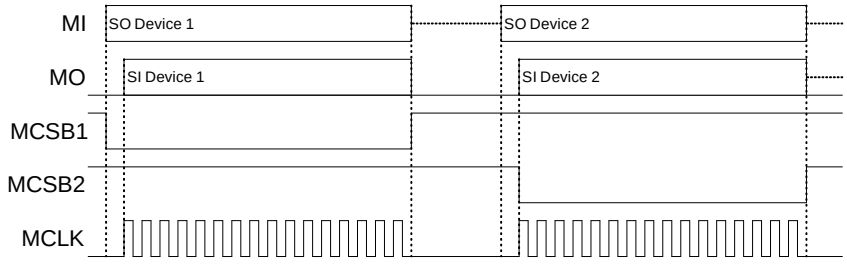



Parallel Connection

Multiple devices can be connected in parallel as shown below.
For SI signal, SCLK signal, and SO signal, connect a common signal. Separate signals are required for the CSB signal for each device.

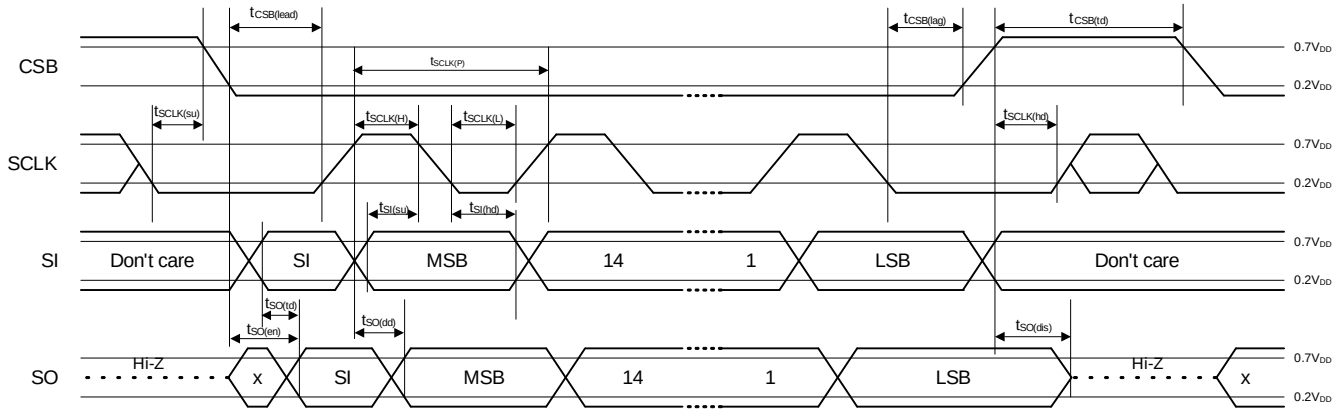



The timing chart when two devices are connected is shown below.



## SPI Specification – continued

SPI Timing chart




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCLK Frequency | $f_{SCLK}$ | 0 | - | 5 | MHz |
| SCLK Period | $t_{SCLK(P)}$ | 200 | - | - | ns |
| SCLK High Time | $t_{SCLK(H)}$ | 50 | - | - | ns |
| SCLK Low Time | $t_{SCLK(L)}$ | 50 | - | - | ns |
| SCLK Setup Time | $t_{SCLK(su)}$ | 50 | - | - | ns |
| SCLK Hold Time | $t_{SCLK(hd)}$ | 50 | - | - | ns |
| CSB Lead Time | $t_{CSB(lead)}$ | 250 | - | - | ns |
| CSB Lag Time | $t_{CSB(lag)}$ | 250 | - | - | ns |
| Transfer Delay Time | $t_{CSB(td)}$ | 250 | - | - | ns |
| Data Setup Time | $t_{SI(su)}$ | 20 | - | - | ns |
| Data Hold Time | $t_{SI(hd)}$ | 20 | - | - | ns |
| SPI Output Enable Time*(Note 1)* | $t_{SO(en)}$ | - | - | 200 | ns |
| SPI Output Disable Time*(Note 1)* | $t_{SO(dis)}$ | - | - | 250 | ns |
| SPI Output Data Delay Time*(Note 1)(Note 2)* | $t_{SO(dd)}$ | - | - | 100 | ns |
| ERR Output Through Delay Time*(Note 1)* | $t_{SO(td)}$ | - | - | 200 | ns |

*(Note 1)* Not 100 % tested.
*(Note 2)* SO capacitance = 20 pF

### SPI Specification – continued

SI data structure

| Bit[15] | Bit[14] | Bit[13] | Bit[12] | Bit[11] | Bit[10] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RE | WE | Address | | | | | TEST | Data | | | | | | | |

RE
0: SO outputs "Standard diagnostic" at the next SPI access.
1: SO outputs the register specified by Address at the next SPI access.

WE
0: Not Write.
1: Write.

TEST
Be sure to set 0.

Data
When WE = 1, various settings are enabled by writing '0' or '1' to Data.
For details, refer to "Register Map".

"Standard diagnostic" (when RE = 0 in the previous SPI access)

Initial Value 0x4000

| Bit[15] | Bit[14] | Bit[13] | Bit[12] | Bit[11] | Bit[10] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | INIT | 0 | 0 | 0 | TER | 0 | 0 | ERR8 | ERR7 | ERR6 | ERR5 | ERR4 | ERR3 | ERR2 | ERR1 |

INIT
0: Normal (after power on or IDLE = 'L'->'H', from the second time SPI access).
1: After power on or IDLE = 'L'->'H', first time SPI access.

TER
0: Normal
1: SPI communication error
When High pulse input of SCLK is other than (16 times + 8 x m, m is an integer 0 or above) in the low level section of CSB, a communication error is judged.

ERRn (n is the channel number)
0: Normal
1: The value is latched and output when over current protection or thermal shutdown of the corresponding channel is detected.
This bit is cleared by reading DIAG register (DIAG_OUT4321 or DIAG_OUT8765) of the channel on which protection is detected.

SO output data structure (when RE = 1 in the previous SPI access)

| Bit[15] | Bit[14] | Bit[13] | Bit[12] | Bit[11] | Bit[10] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | WE | Address | | | | | $ERR_{ALL}$ | Data | | | | | | | |

WE, Address
Outputs WE and Address values that were set during the previous SPI access.

$ERR_{ALL}$
Outputs 1 when either over current protection or thermal shutdown of OUT is detected on at least one channel.

Data
Outputs the register value of Address that were set during the previous SPI access.

## Register Map

| Register Name | Register Access | Address | TEST | Data | | | | | | | | Initial |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Bit[13:9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | |
| OUTCTRL | R/W | 0x00 | 0 | OUTCTRL8 | OUTCTRL7 | OUTCTRL6 | OUTCTRL5 | OUTCTRL4 | OUTCTRL3 | OUTCTRL2 | OUTCTRL1 | 0x00 |
| SRCTRL0 | R/W | 0x01 | 0 | SRCTRL4[1:0] | | SRCTRL3[1:0] | | SRCTRL2[1:0] | | SRCTRL1[1:0] | | 0x00 |
| SRCTRL1 | R/W | 0x02 | 0 | SRCTRL8[1:0] | | SRCTRL7[1:0] | | SRCTRL6[1:0] | | SRCTRL5[1:0] | | 0x00 |
| OCPCTRL | R/W | 0x03 | 0 | OCPCTRL8 | OCPCTRL7 | OCPCTRL6 | OCPCTRL5 | OCPCTRL4 | OCPCTRL3 | OCPCTRL2 | OCPCTRL1 | 0x00 |
| DIRCTRL | R/W | 0x04 | 0 | 0 | 1 | DIRCTRL6 | DIRCTRL5 | DIRCTRL4 | DIRCTRL3 | DIRCTRL2 | DIRCTRL1 | 0x55 |
| SYNC | R/W | 0x05 | 0 | 0 | 0 | 0 | 0 | SYNC87 | SYNC65 | SYNC43 | SYNC21 | 0x00 |
| STATUS_IN | RO | 0x06 | 0 | 0 | 0 | 0 | 0 | 0 | STATUS_IN65 | STATUS_IN43 | STATUS_IN21 | 0x00 |
| DIAG_OLD/OFD | R/W | 0x08 | 0 | DIAG_OLD/OFD8 | DIAG_OLD/OFD7 | DIAG_OLD/OFD6 | DIAG_OLD/OFD5 | DIAG_OLD/OFD4 | DIAG_OLD/OFD3 | DIAG_OLD/OFD2 | DIAG_OLD/OFD1 | 0x00 |
| DIAG_SGD | R/W | 0x09 | 0 | DIAG_SGD8 | DIAG_SGD7 | DIAG_SGD6 | DIAG_SGD5 | DIAG_SGD4 | DIAG_SGD3 | DIAG_SGD2 | DIAG_SGD1 | 0x00 |
| DIAG_OUT4321 | RO | 0x0A | 0 | DIAG_OCP4 | DIAG_TSD4 | DIAG_OCP3 | DIAG_TSD3 | DIAG_OCP2 | DIAG_TSD2 | DIAG_OCP1 | DIAG_TSD1 | 0x00 |
| DIAG_OUT8765 | RO | 0x0B | 0 | DIAG_OCP8 | DIAG_TSD8 | DIAG_OCP7 | DIAG_TSD7 | DIAG_OCP6 | DIAG_TSD6 | DIAG_OCP5 | DIAG_TSD5 | 0x00 |
| HWCR | WO | 0x0C | 0 | 0 | RST | 0 | 0 | 0 | 0 | 0 | 0 | 0x00 |
| T_TESTMODE | WO | 0x1E | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TESTMODE | 0x00 |

| Register Name | Register Access | Address | Explanation of Data |
|---|---|---|---|
| OUTCTRL | Read / Write | 0x00h | OUTCTRLn bit (n represents the channel number)<br>'0': OUTn off setting<br>'1': OUTn on setting |
| SRCTRL0<br>SRCTRL1 | Read / Write | 0x01h<br>0x02h | SRCTRLn[1:0] bit<br>'00': Slew Rate Setting 1.0 V/µs (Typ)<br>'01': Slew Rate Setting 2.25 V/µs (Typ)<br>'10': Slew Rate Setting 0.30 V/µs (Typ)<br>'11': Same setting as '00' |
| OCPCTRL | Read / Write | 0x03h | OCPCTRLn bit<br>'0': Over Current Threshold Value 1 0.85 A (Typ)<br>'1': Over Current Threshold Value 2 1.7 A (Typ) |
| DIRCTRL | Read / Write | 0x04h | DIRCTRLn bit<br>'0': IN control disabled<br>'1': IN control enabled |
| SYNC | Read / Write | 0x05h | SYNC21/SYNC43/SYNC65/SYNC87 bit<br>'0': Synchro mode disabled<br>'1': Synchro mode enabled |
| STATUS_IN | Read Only | 0x06h | STATUS_IN65/STATUS_IN43/STATUS_IN21 bit<br>'0': IN87/IN65/IN43/IN21 L input<br>'1': IN87/IN65/IN43/IN21 H input |
| DIAG_OLD/OFD | Read / Write | 0x08h | DIAG_OLD/OFDn bit<br>'0': OLD/OFD disabled<br>'1': OLD/OFD enabled<br><br>OLD is enabled when OUTn is off. OFD is enabled when OUTn is on. When SPI access is performed again, it automatically returns to '0' (disabled).<br><br>Read OLD/OFD result by read access (RE = 1).<br>When OLD is active, the judgement is made as below.<br>'0': OLD detection<br>'1': Normal<br><br>When OFD is active, the judgement is made as below.<br>'0': Normal<br>'1': OFD detection<br>For details, refer to "Open Load Detection" and "Output Overhead Fault Detection Function". |

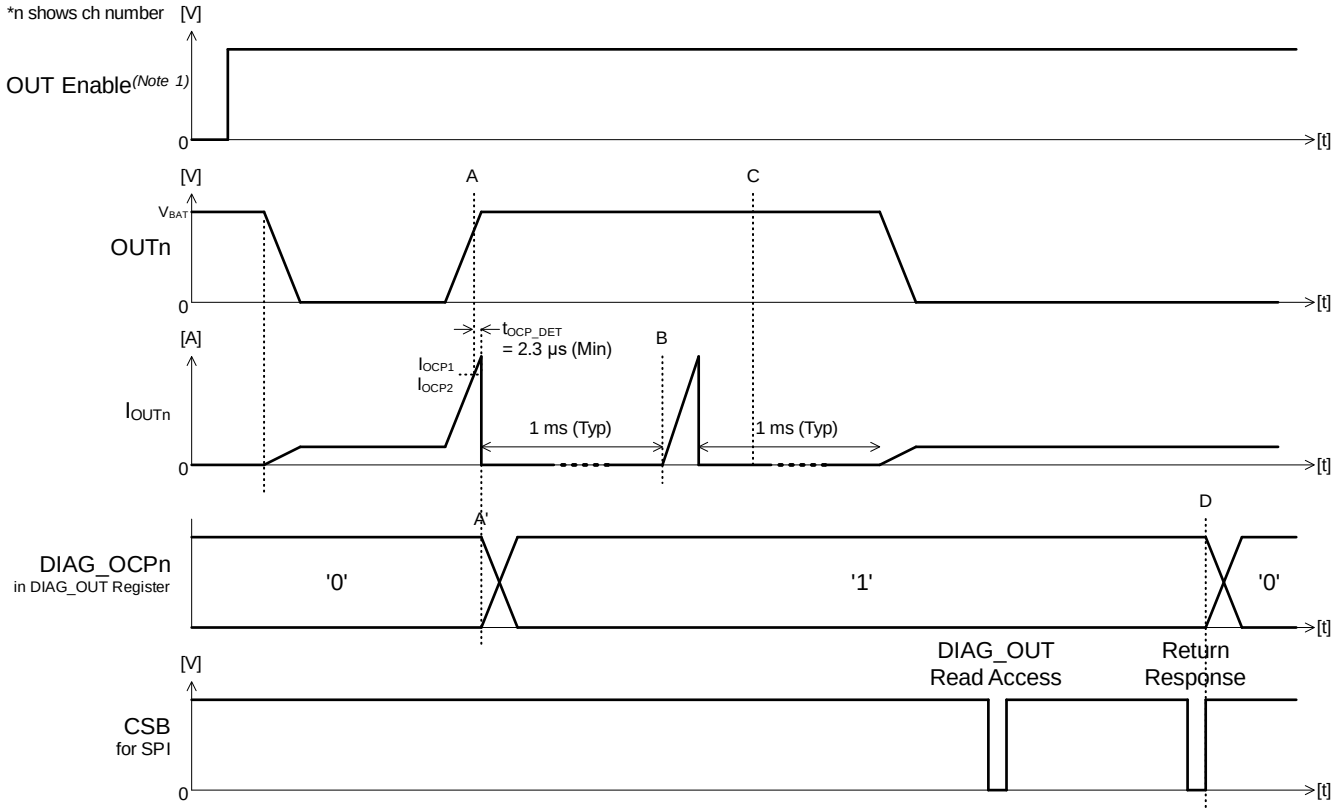
**Register Map – continued**

| Register Name | Register Access | Address | Explanation of Data |
|---|---|---|---|
| DIAG_SGD | Read / Write | 0x09h | DIAG_SGDn bit<br>'0': SGD disabled<br>'1': SGD enabled<br><br>This function is used when OUTn is off. When SPI access is performed again, it automatically returns to '0' (disabled).<br><br>Read SGD result by read access (RE = 1).<br>'0': SGD detection<br>'1': Normal<br>For details, refer to " Short Ground Detection". |
| DIAG_OUT4321 | Read Only | 0x0Ah | Read the error flag of ch1/ch2/ch3/ch4.<br>DIAG_TSDn bit<br>'0': Normal<br>'1': TSD detection<br><br>DIAG_OCPn bit<br>'0': Normal<br>'1': OCP detection<br><br>It automatically returns to '0' when DIAG_OUT4321 is accessed. |
| DIAG_OUT8765 | Read Only | 0x0Bh | Read the error flag of ch5/ch6/ch7/ch8.<br>DIAG_TSDn bit<br>'0': Normal<br>'1': TSD detection<br><br>DIAG_OCPn bit<br>'0': Normal<br>'1': OCP detection<br><br>It automatically returns to '0' when DIAG_OUT8765 is accessed. |
| HWCR | Write Only | 0x0Ch | RST<br>'0': Normal<br>'1': Hardware reset (auto clear) |
| T_TESTMODE | Write Only | 0x1Eh | TESTMODE<br>'0': Normal<br>'1': Test Mode<br>If IDLE is 5.6 V (Min) or more and "1" is written to this register, IC enters test mode. For this reason, do not access to this register. |

### Over Current Protection Function

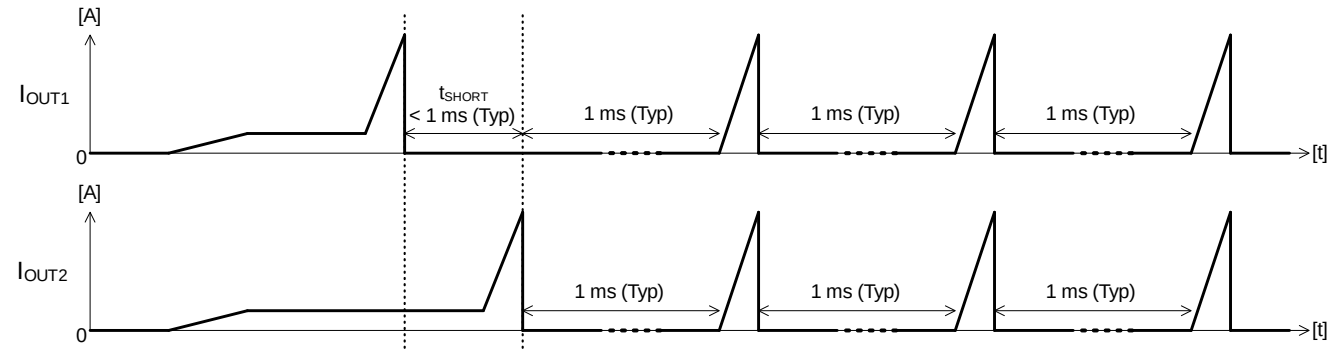
Turns off the output when an over current error occurs in the output (A in the figure). The output returns to on when the output stop time of 1 ms (Typ) has passed. However, if an over current error still continue at this time, the output will be turned off again (B in the figure). When an over current error is improved, the output recovers after the output stop time from over current error is lastly detected has passed (C in the figure).

If an over current error is detected, the internal over current detection flag outputs '1' (A' in the figure). This flag can be read from SPI read access or from Standard diagnostic. When the flag is read by SPI read access, it is cleared by the next SPI access after read access (D in the figure).




*(Note 1)* Output on/off control signal. This signal is controlled by IN65, IN43, IN21 or OUT_CTRL register.

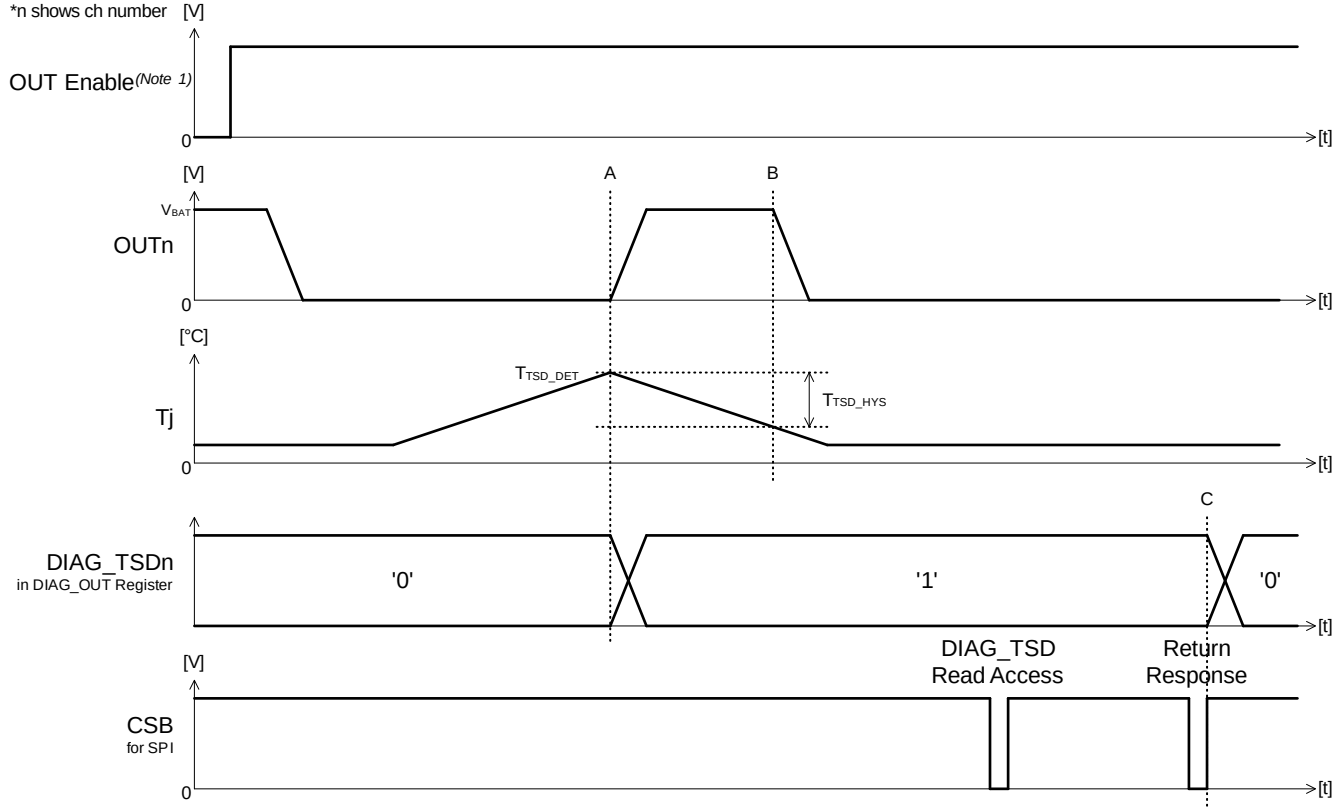
When an over current error is detected in multiple channels, the output off time is measured starting from the channel that over current error was detected lastly.
For example, if an over current error is detected in ch2 after an over current error is detected in ch1 before the output off time of ch1 passes, the time $t_{SHORT}$ from ch1 detects an error until an error is detected in ch2 will be added to the output off time of ch1.



### Thermal Shutdown Function

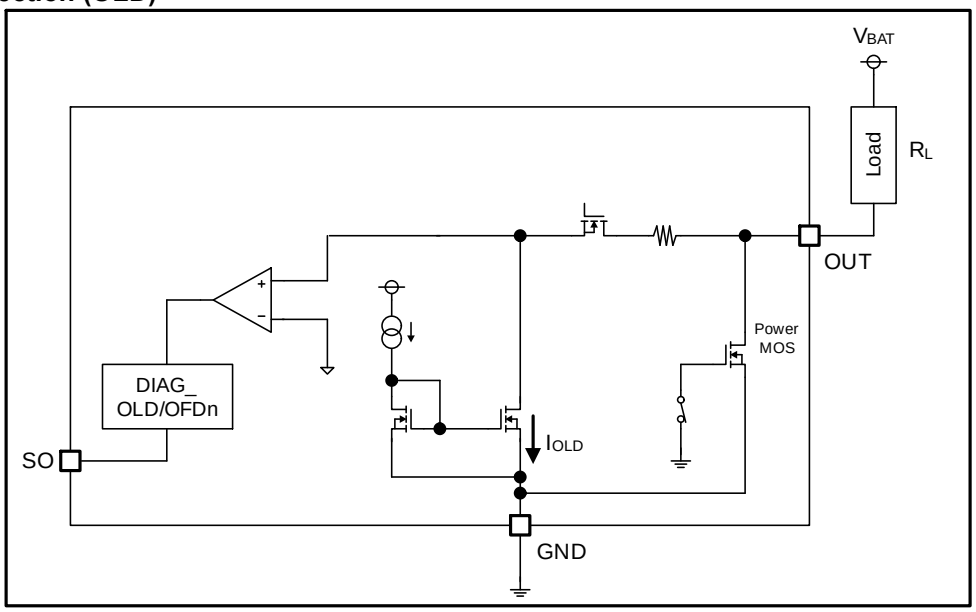
Turns off the output when the junction temperature rises 175 °C (Typ) or above (A in the figure). After that, the output automatically returns to on when the junction temperature falls 160 °C (Typ) or below (B in the figure).

When thermal shutdown is detected, the internal thermal shutdown flag outputs '1' (A in the figure). This flag can be read from SPI read access or Standard diagnostic. When the flag is read by SPI read access, it is cleared by the next SPI access after read access (C in the figure).




*(Note 1)* Output on/off control signal. This signal is controlled by IN65, IN43, IN21 or OUT_CTRL register.

### Open Load Detection (OLD)

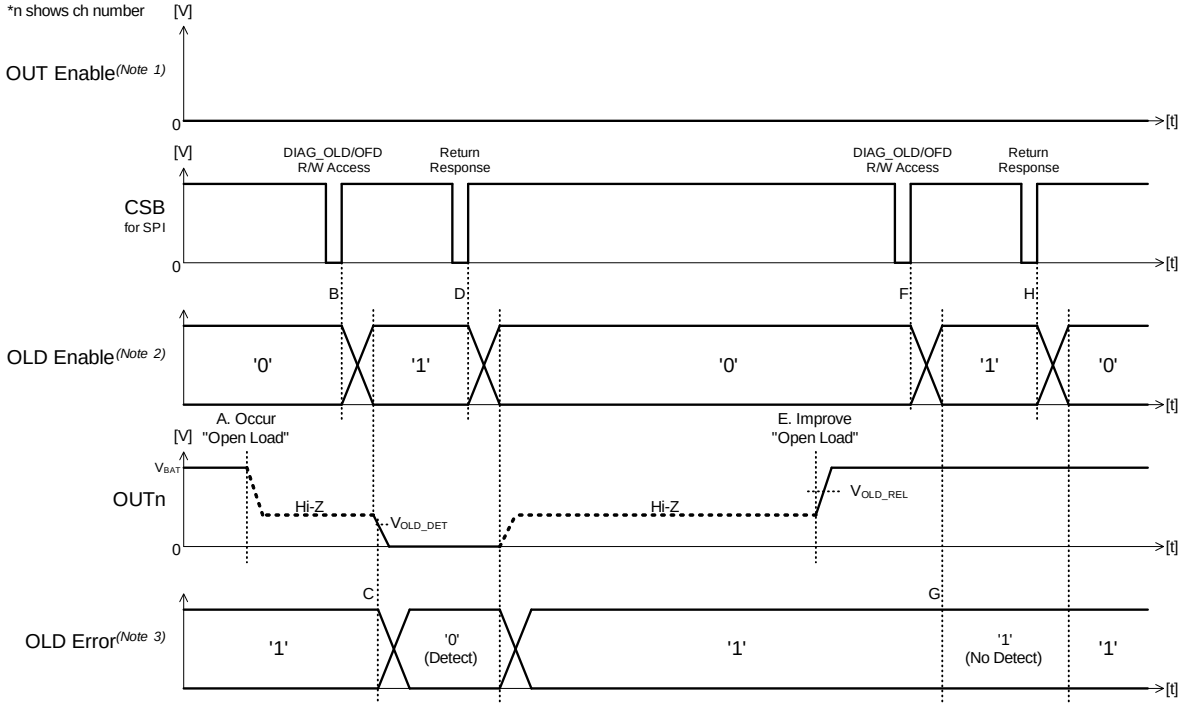



When OLD is enabled, output sink current $I_{OLD}$ flows from OUT. The output voltage $V_{OUT}$ drops when the load $R_L$ increases, and it is detected as OLD when it becomes $V_{OLD\_DET}$ or less.
$R_L$ for detecting OLDs is given by the following equation:

$$R_L \geq \frac{V_{BAT} - V_{OLD\_DET}}{I_{OLD}}$$

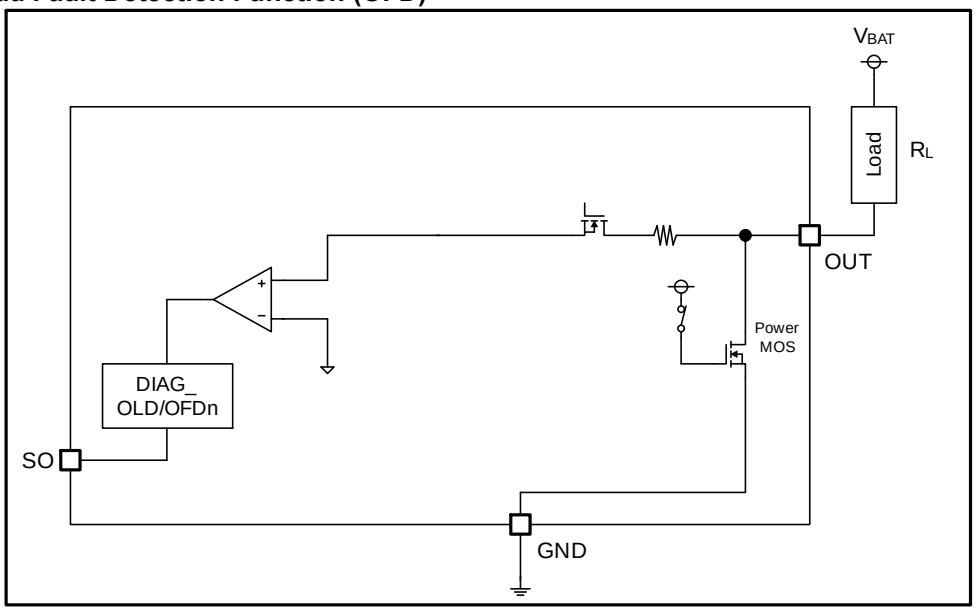
$V_{BAT}$: Battery voltage
$V_{OLD\_DET}$: Open load detection voltage 3.2 V (Max)
$I_{OLD}$: Output sink current when OLD function is active 90 µA (Max)

When the output is off, OLD can be enabled and diagnosed by one SPI access of write and read access (RE = 1, WE = 1) to DIAG_OLD/OFD register (B, F in the figure). Diagnostic is output to SO at the next SPI access (D, H in the figure).
At this time, OLD returns to inactive (D, H in the figure). When OUTn voltage is $V_{OLD\_DET}$ or less, OLD is diagnosed as detected and the error flag inside the IC outputs "0" (C in the figure). If OUTn voltage is $V_{OLD\_REL}$ or more, OLD is diagnosed as undetected and the error flag output '1' (G in the figure).

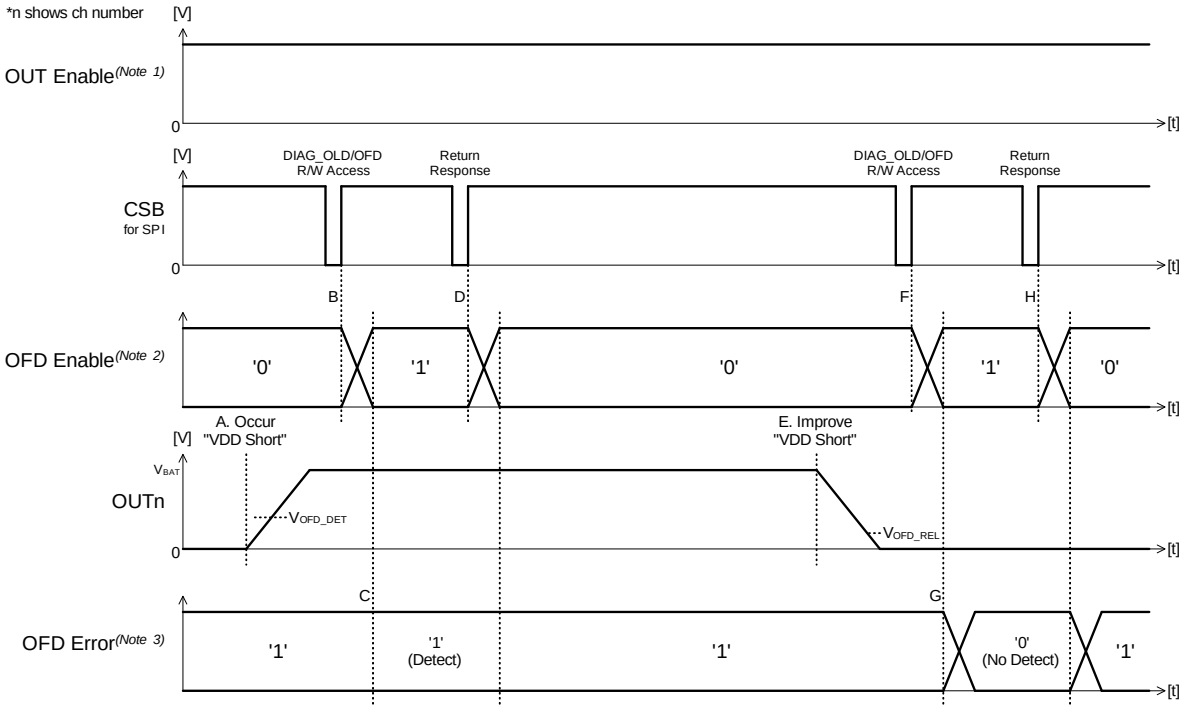



*(Note 1)* Output on/off control signal. This signal is controlled by IN65, IN43, IN21 or OUT_CTRL register.
*(Note 2)* Internal enable signal. High and Low indicates enabled and disabled, respectively. This signal is controlled by write access to DIAG_OLD/OFD register.
*(Note 3)* Internal error flag. High and Low indicates error undetected and detected, respectively. Also the flag outputs High during disable. This signal can be retrieved to SO by read access to DIAG_OLD/OFD register.

### Output Overhead Fault Detection Function (OFD)

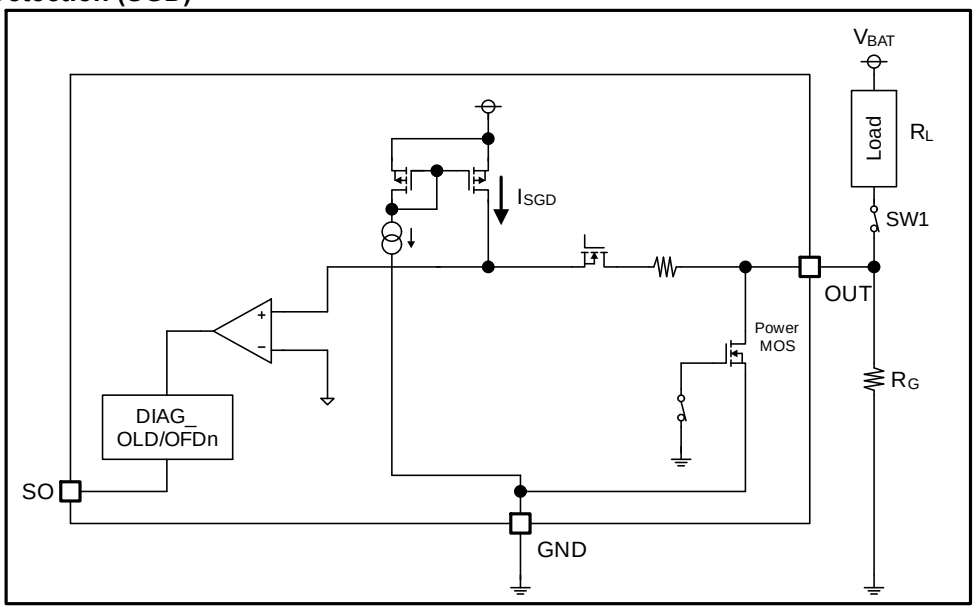



When the output is on, OFD can be enabled and diagnosed by one SPI access by write and read access (RE = 1, WE = 1) to DIAG_OLD/OFD register (B, F in the figure). Diagnostic is output to SO at the next SPI access (D, H in the figure).
At this time, OFD returns to be inactive (D, H in the figure). When OUTn voltage is $V_{OFD\_DET}$ or more, OFD is diagnosed as detected and the error flag inside the IC outputs "1" (C in the figure). If OUTn voltage is $V_{OFD\_REL}$ or less, OFD is diagnosed as undetected and the error flag output '0' (G in the figure).




*(Note 1)* Output on/off control signal. High and Low indicates on and off, respectively. This signal is controlled by IN65, IN43, IN21 or OUT_CTRL register.
*(Note 2)* Internal enable signal. High and Low indicates enabled and disabled, respectively. This signal is controlled by write access to DIAG_OLD/OFD register.
*(Note 3)* Internal error flag. High and Low indicates error detected and undetected, respectively. Also the flag outputs High during disable. This signal can be retrieved to SO by read access to DIAG_OLD/OFD register.

**Short Ground Detection (SGD)**




·When normal load is connected (SW1 is on)
The output voltage $V_{OUT}$ is determined by the divided voltage between $R_L$ (normal load) and $R_G$ (OUT-GND impedance) and it is detected as SGD when $V_{OUT}$ is $V_{SGD\_DET}$ or less.
$R_G$ for detecting SGD is given roughly by the following equation.

$$R_G \leq \frac{V_{SGD\_DET}}{V_{BAT} - V_{SGD\_DET}} * R_L$$

$V_{BAT}$: Battery voltage
$V_{SGD\_DET}$: Short ground detection voltage 0.3 V (Min)

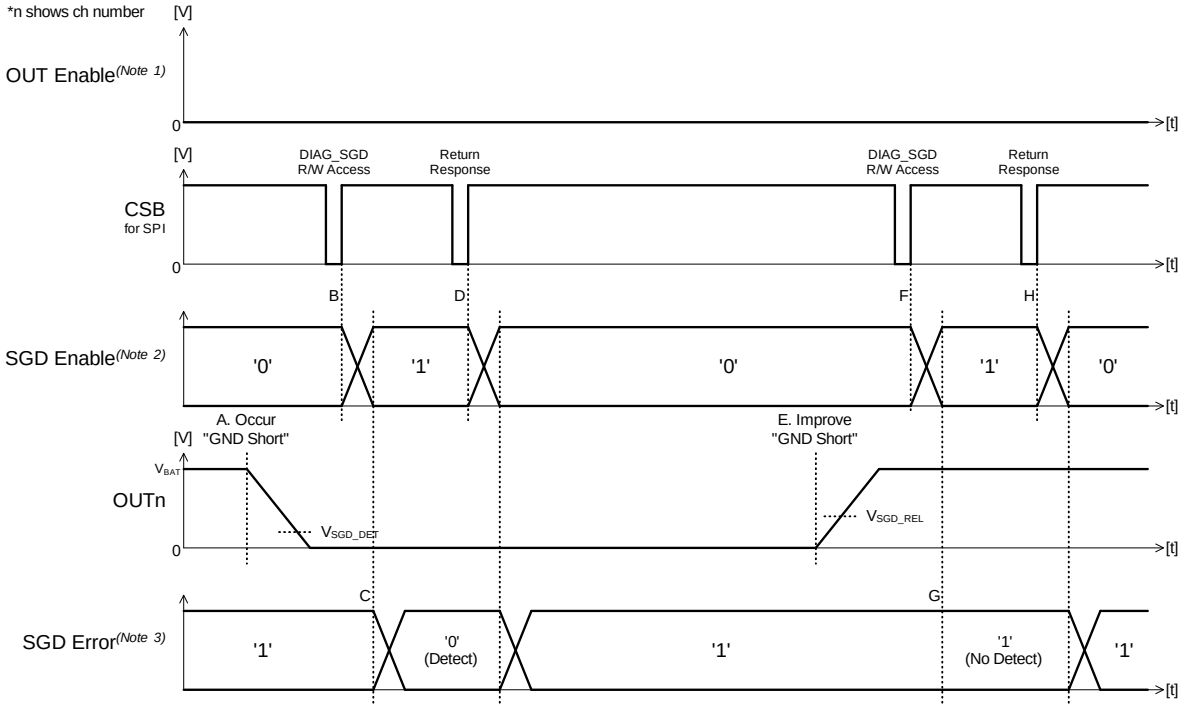
·When the load is open (SW1 is off)
The output voltage $V_{OUT}$ is obtained from output source current $I_{SGD}$ that flows into $R_G$ and it is detected as SGD when $V_{OUT}$ is $V_{SGD\_DET}$ or less.
$R_G$ for detecting SGD is given by the following equation.

$$R_G \leq \frac{V_{SGD\_DET}}{I_{SGD}}$$

$V_{SGD\_DET}$: Short ground detection voltage 0.3 V (Min)
$I_{SGD}$: Output source current when SGD function is active 40 µA (Max)

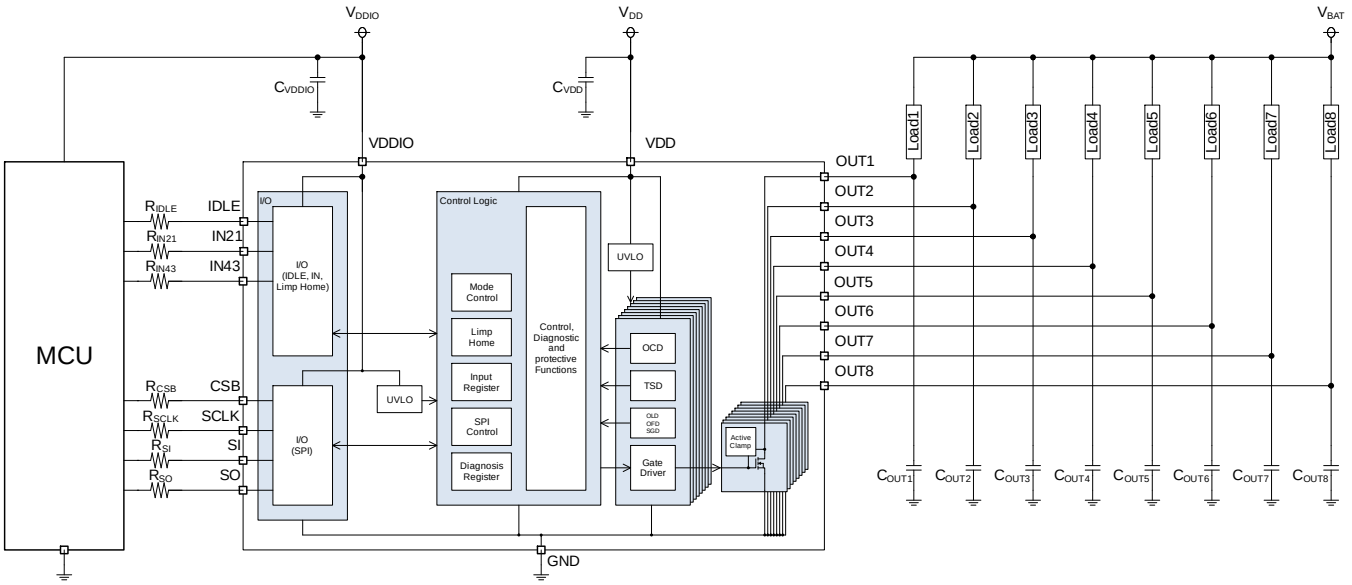
### Short Ground Detection (SGD) – continued

When the output is off, SGD can be enabled and diagnosed by one SPI access of write and read access (RE = 1, WE = 1) to DIAG_SGD register (B, F in the figure). Diagnostic is output to SO at the next SPI access. At this time, SGD returns to be inactive (D, H in the figure). When OUTn voltage is $V_{SGD\_DET}$ or less, SGD is diagnosed as detected and the error flag inside the IC outputs "0" (C in the figure). If OUTn voltage is $V_{SGD\_REL}$ or more, SGD is diagnosed as undetected and the error flag output '1' (G in the figure).




*(Note 1)* Output on/off control signal. This signal is controlled by IN65, IN43, IN21 or OUT_CTRL register.
*(Note 2)* Internal enable signal. High and Low indicates enabled and disabled, respectively. This signal is controlled by write access to DIAG_SGD register.
*(Note 3)* Internal error flag. High and Low indicates error undetected and detected, respectively. Also the flag outputs High during disable. This signal can be retrieved to SO by read access to DIAG_SGD register.

## Application Example



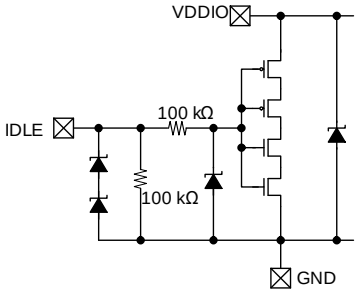
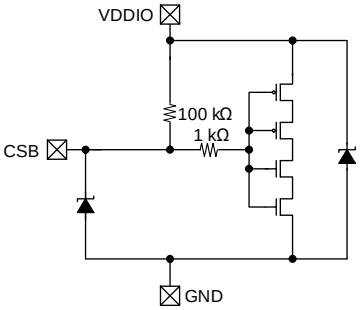
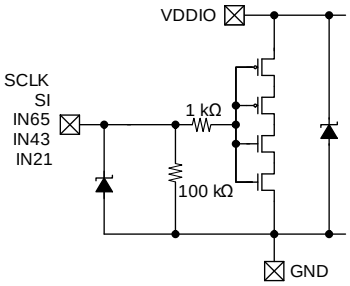
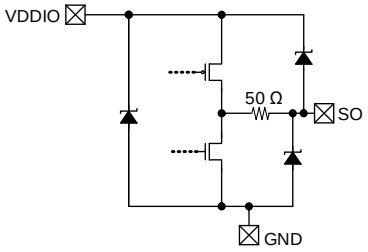
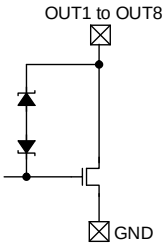

## Selection of Components Externally Connected

| Symbol | Value | Purpose |
|---|---|---|
| $R_{IDLE}$ | 1 kΩ | Register for microcontroller protection against negative voltage surge |
| $R_{IN21}$, $R_{IN43}$, $R_{IN65}$ | 1 kΩ | Register for microcontroller protection against negative voltage surge |
| $R_{CSB}$, $R_{SCLK}$, $R_{SI}$, $R_{SO}$ | 1 kΩ | Register for microcontroller protection against negative voltage surge |
| $C_{VDDIO}$, $C_{VDD}$ | 0.1 μF | Capacitor for noise removal on the power supply line |
| $C_{OUT1}$ to $C_{OUT8}$ | 0.1 μF | Capacitor for ESD surge and BCI protection |

As a precaution in selecting a $C_{OUT}$, current flows from the capacitor when the switch is turned on. Depending on the capacitance, over current protection may be detected. This current depends on the slew rate setting, over current protection setting, and $V_{BAT}$ voltage. As a reference, capacitance that can be used with $V_{BAT}$ = 18 V without over current protection when the switch is turned on is shown in the below table.

| $V_{BAT}$ = 18 V | | |
|---|---|---|
| Slew Rate setting | Over Current Protection setting | Capacitance value that over current protection is not detected (Max) |
| SRCTRLn[1:0] = 00 | OCPCTRLn = 0 | 0.22 μF |
| | OCPCTRLn = 1 | 0.22 μF |
| SRCTRLn[1:0] = 01 | OCPCTRLn = 0 | 0.47 μF |
| | OCPCTRLn = 1 | 0.83 μF |
| SRCTRLn[1:0] = 10 | OCPCTRLn = 0 | 0.68 μF |
| | OCPCTRLn = 1 | 1.5 μF |

**I/O Equivalence Circuits**

| Pin No. | Pin Name | I/O Equivalence Circuit |
|---|---|---|
| 1 | IDLE |  |
| 2 | CSB |  |
| 3, 4<br>16 to 18 | SCLK<br>SI<br>IN65<br>IN43<br>IN21 |  |
| 5 | SO |  |
| 6, 15 | GND | - |
| 7 to 14 | OUT1 to OUT8 |  |
| 19 | VDD | - |
| 20 | VDDIO | - |

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**10. Regarding the Input and Output Pins of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

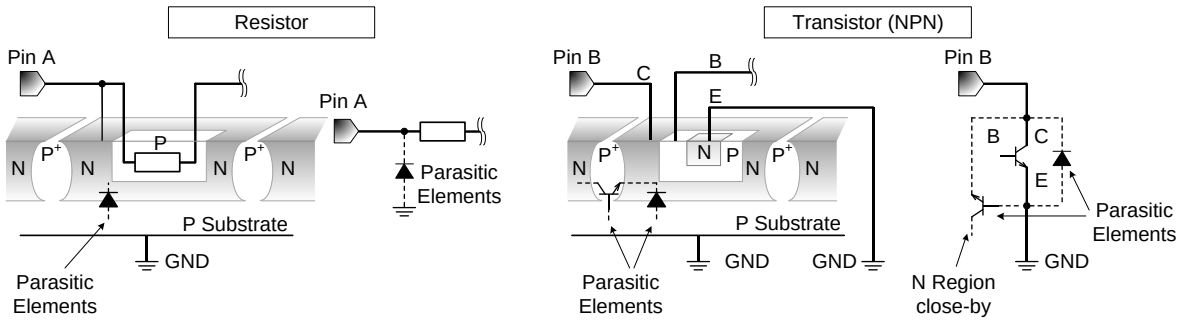



Figure 58. Example of Monolithic IC Structure

**11. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**12. Thermal Shutdown Function (TSD)**

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD function that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

**13. Over Current Protection Function (OCP)**

This IC incorporates an integrated overcurrent protection function that is activated when the load is shorted. This protection function is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection function.

**14. Active Clamp Operation**

The IC integrates the active clamp function to internally absorb the reverse energy $E_L$ which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy $E_L$ is active clamp tolerance $E_{AS}$ (refer to Figure 1.), $E_{S,AS}$ (refer to Figure 2.) or under when inductive load is used.

## Operational Notes – continued

**15. Power Supply Steep Fluctuation**

If the voltage of the power supply pin (VDD) falls sharply, the output pin (OUT) may temporarily turn off as shown in Figure 55. If the power supply pin is expected to fall sharply, take measures such as inserting a capacitor between the power supply pin and the ground pin so that it falls within the recommended usage range shown in Figure 56.

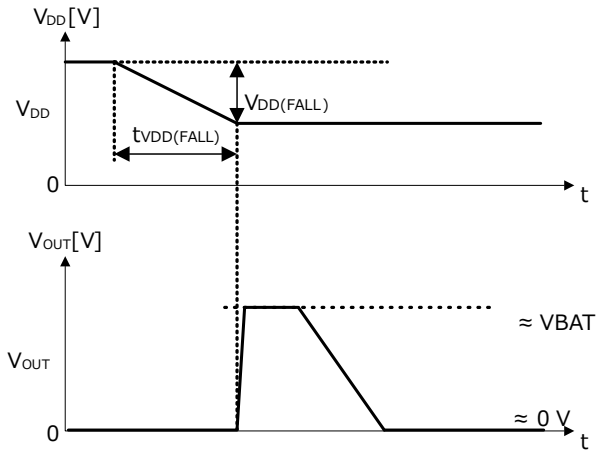



Figure 59. Output OFF operation when power supply fluctuates sharply

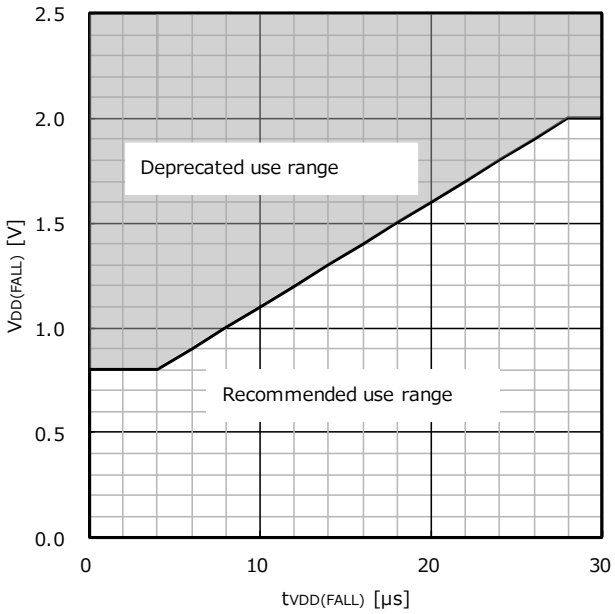



Figure 60. Recommended use range

**16. GND Pin Connection**

Connect all ground pins to ground.

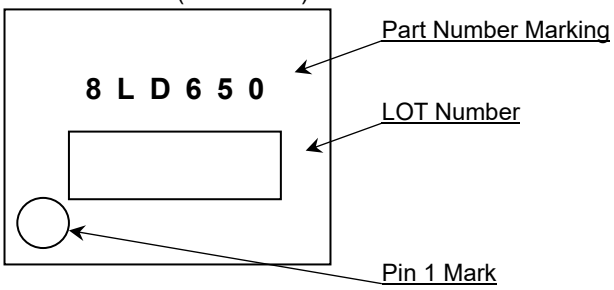
### Ordering Information

| B | D | 8 | L | D | 6 | 5 | 0 | E | F | V | - | CE 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

- 8: 8ch
  L: low side switch
- Package
  EFV: HTSSOP-B20
- Product Rank
  C: For Automotive
  Packaging Specification
  E2: Embossed tape and reel

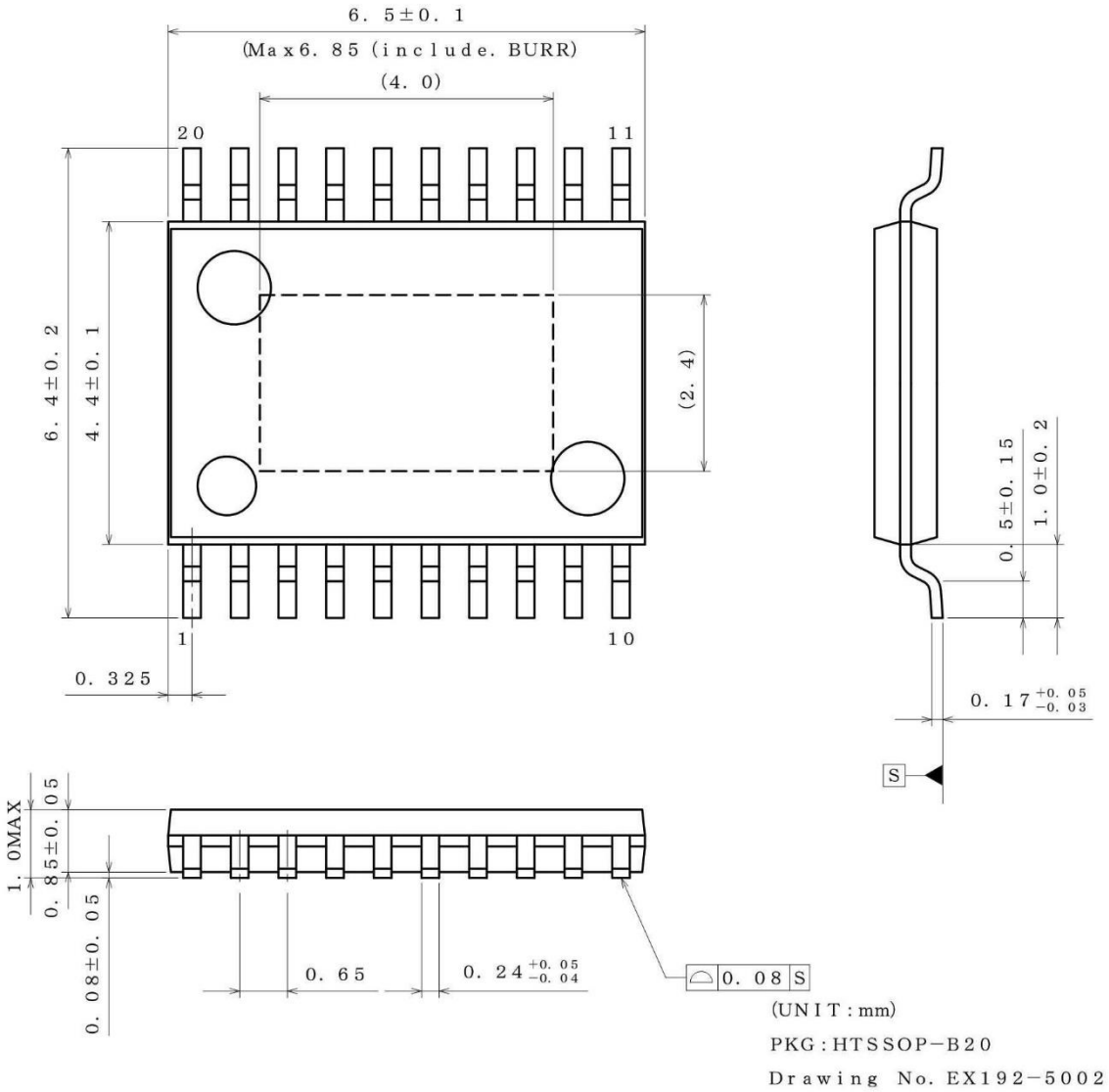
### Marking Diagram

HTSSOP-B20 (TOP VIEW)



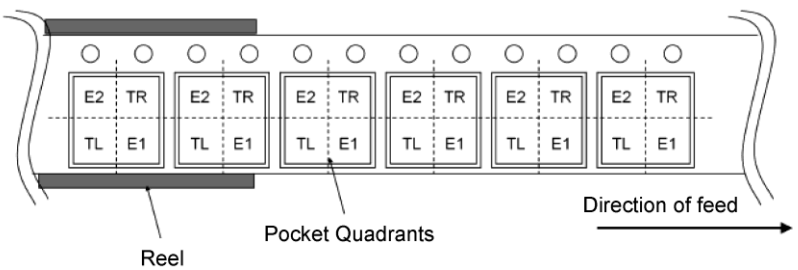
**Physical Dimension and Packing Information**

| Package Name | HTSSOP-B20 |
|---|---|




< Tape and Reel Information >

| Tape | Embossed carrier tape |
|---|---|
| Quantity | 2500pcs |
| Direction of feed | E2<br>The direction is the pin 1 of product is at the upper left<br>when you hold reel on the left hand and you pull out the tape on the right hand |



**Revision History**

| Date | Revision | Changes |
|---|---|---|
| 26.Aug.2022 | 001 | New Release |
| 03.Aug.2023 | 002 | P11 Add Over Current Detection Time $t_{OCP\_DET}$<br>P35 Add $t_{OCP\_DET}$ in OCP sequence chart |

# Notice

## Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

### Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

### Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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