Isolated DC/DC Converter IC

Isolated Type Flyback Converter IC with Integrated Switching MOSFET for Automotive

BD7F306EFV-C

General Description

BD7F306EFV-C is an optocoupler less isolated flyback converter. Feedback circuit by optocouplers or third auxiliary winding of transformers becomes unnecessary, contributing to reduction of set parts. Furthermore, the adoption of original adapted ON time control technology enables fast load response. In addition, the various protection function realizes the designs of isolated power supply application for high reliability.

Key Specifications

- Input Voltage Range:
  - VIN Pin: 3.4 V to 36.0 V
  - SW Pin: 80 V (Max)
- Switching Frequency: 363 kHz (Typ)
- Reference Voltage Precision: ± 2.8 % (Typ)
- Shutdown Current: 0 µA (Typ)
- Operating Ambient Temperature Range: -40 °C to +125 °C

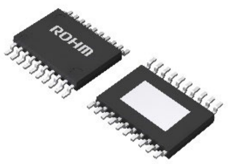
Features

- AEC-Q100 Qualified(Note 1)
- No Need for Optocoupler and Third Winding of Transformer
- Set Output Voltage with Two External Resistors and Ratio of Transformer Turns
- Adopt of Original Adapted ON Time Control Technology Fast Load Response
- High Efficiency at Light Load Mode (PFM Operation)
- Shutdown Function / Enable Control
- Built-in 80 V Switching MOSFET
- Frequency Spectrum Spread
- Soft Start Function
- Load Compensation Function
- Sampling Noise Countermeasures
- Various Protection Function
  - Input Low Voltage Lockout (UVLO)
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)
  - REF Pin Open Protection (REFOPEN)
  - REF Pin Short Protection (REFSHORT)
  - REF Pin Noise Filter
  - Short Circuit Protection (SCP)
  - Battery Short Protection (BSP)
- HTSSOP-B20 Package

(Note 1) Grade 1

Package

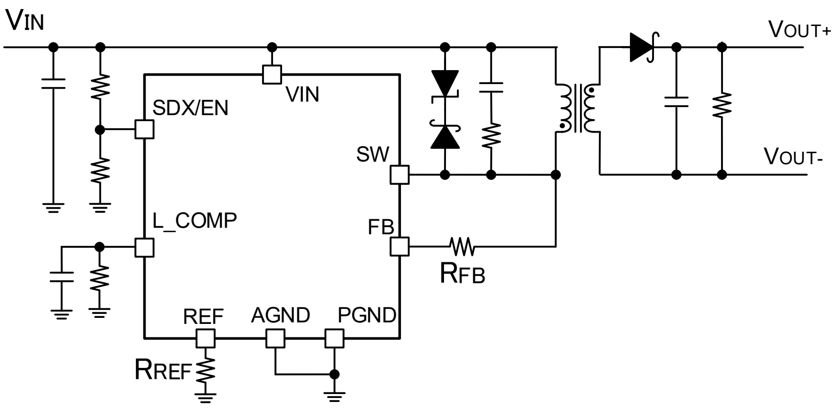
Package	W (Typ) x D (Typ) x H (Max)
HTSSOP-B20	6.5 mm x 6.4 mm x 1.0 mm



Applications

- Automotive Isolated Power Supplies (Inverter, OBC, E-heater etc)
- Isolated Power Supplies for Industry

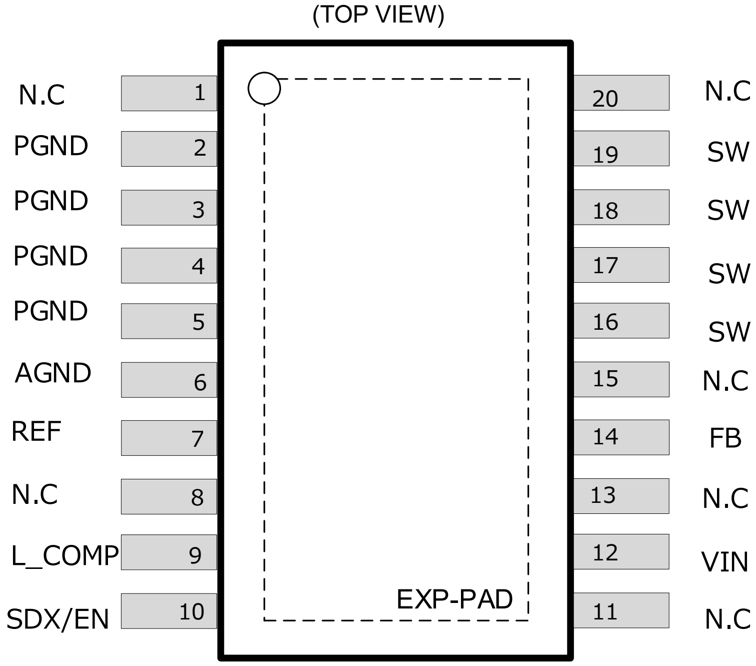
Typical Application Circuit



〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays.

Contents

Pin Configuration

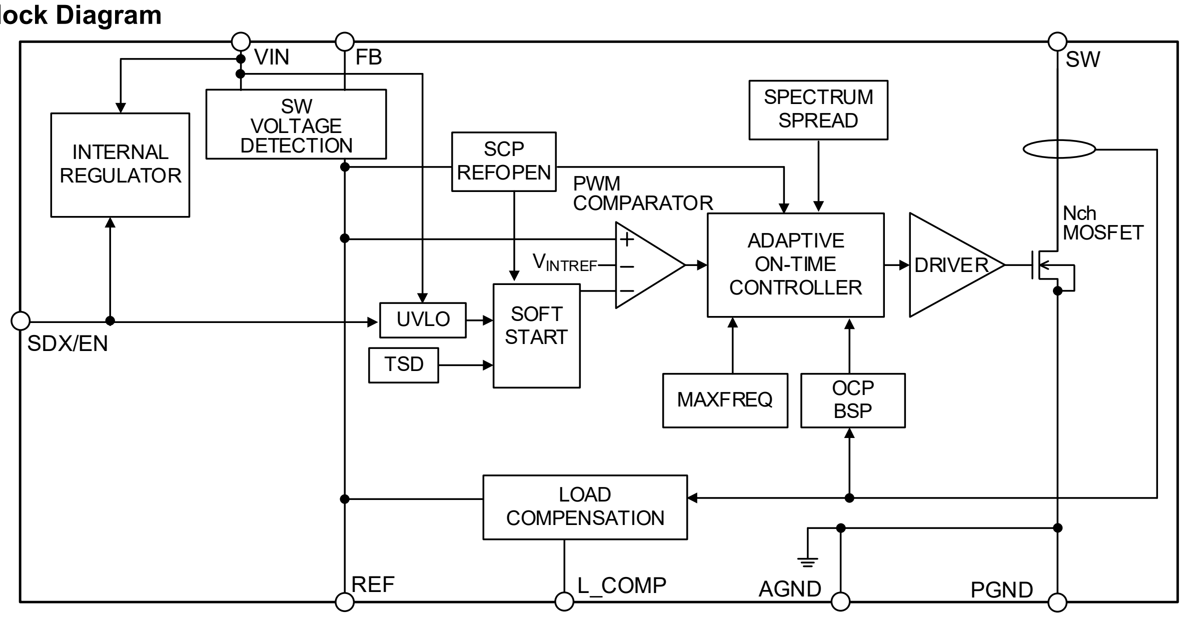


Pin Descriptions

Pin No.	Pin Name	Function
2, 3, 4, 5	PGND	Power GND pin(Note 1)
6	AGND	Analog GND pin
7	REF	Output voltage setting pin
1, 8, 11, 13, 15, 20	N.C	Non Connection (No internal connections)
9	L_COMP	Setting pin of load current compensation value pin
10	SDX/EN	Shutdown / Enable control pin
12	VIN	Power supply input pin
14	FB	Flyback voltage feedback pin
16, 17, 18, 19	SW	Switching output pin
-	EXP-PAD	Connect EXP-PAD to GND on PCB

(Note 1) Connect all PGND pins to the GND on board. Also, connect all SW pins to the board.

Block Diagram



Description of Blocks

1 Internal Regulator

This is regulator block for internal circuits.
This block shuts itself down at the shutdown status of SDX/EN pin voltage V_{SDX} or less.
When SDX/EN pin voltage rises V_{SDX} or above, IC consumption current increases.
When SDX/EN pin voltage is V_{EN1} or above, IC enters the enable status and starts switching operation.
The soft start function operates for t_{SS} period from switching start, and the output voltage rises slowly.
When SDX/EN pin voltage falls V_{EN2} or below, IC enters the disables status and the switching operation is stopped.

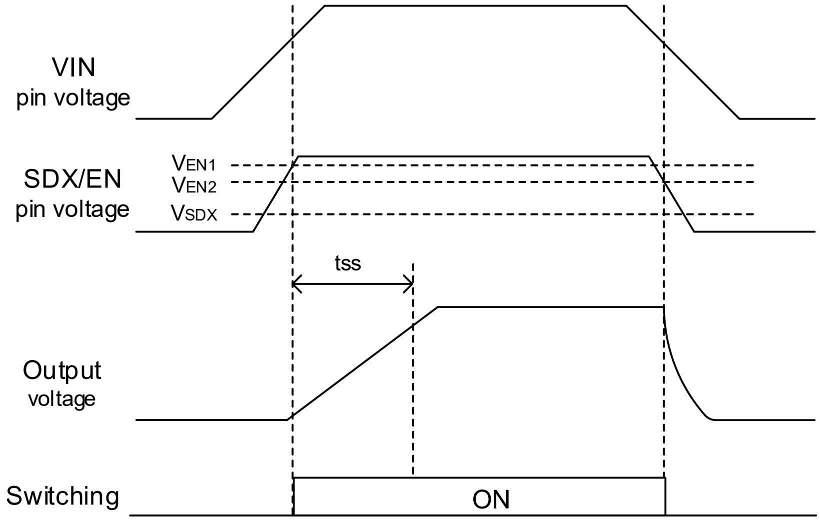


Figure 1. Startup and Stop Timing Chart

2 Input Low Voltage Lock Out (UVLO)

This is the protection function for the low input voltage of the VIN pin.
When VIN pin voltage falls V_{UVLO1} or below, IC detects UVLO and stops switching operation.
When VIN pin voltage rises V_{UVLO2} or above, IC starts switching operation and a soft start function operates during the period of t_{SS}.

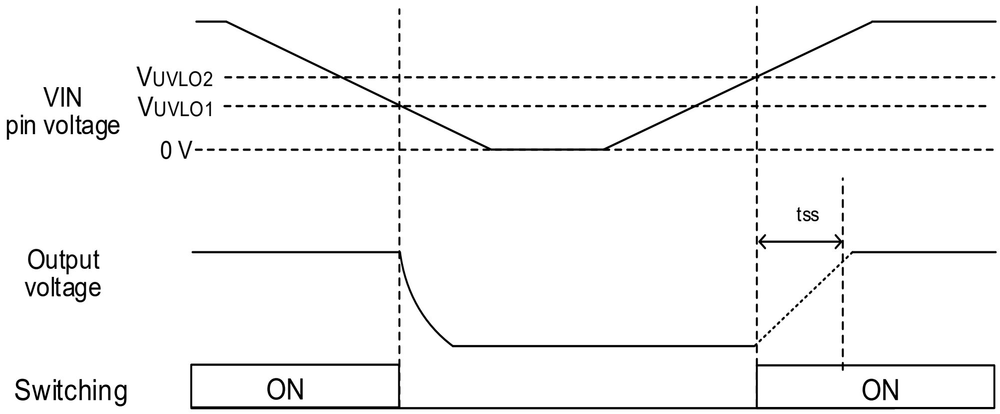


Figure 2. VIN UVLO Timing Chart

Description of Blocks – continued

3 Thermal Shutdown (TSD)

This block is the thermal shutdown circuit that prevents heat damage to the IC. When IC junction temperature rises more than 175 °C (Typ), IC stops switching operation. After that when IC junction temperature falls IC restarts. The temperature hysteresis is 25 °C (Typ). The TSD function aims to protect itself. So IC junction temperature should be designed less than Tjmax = 150 °C. For that, it should not use as over temperature protection function of application.

4 SW Voltage Detection

This block detects the flyback voltage generated in the SW pin. In turn OFF of the transformer, this block converts current to flow from the FB pin into voltage by the resistance of the REF pin and the flyback voltage is detected by this REF pin voltage.
The IC controls REF pin voltage to be equivalent to V_{INTREF}.

5 Soft Start

When IC turns to enable status that SDX/EN pin voltage is V_{EN1} or above, the comparison voltage of the PWM Comparator block increases gradually from 0 V to V_{INTREF}. PWM comparator voltage is constantly V_{INTREF} after soft start time passed.
This operation prevents from the output voltage overshooting. The soft start time is fixed to t_{SS} in the IC.
And SCP is invalid for $t_{MASKSCP}$ period from startup.

6 PWM Comparator

The output voltage of the soft start block or the IC's internal reference voltage V_{INTREF} is compared with the REF pin voltage, which corresponds to the output feedback voltage. This comparator output decides the ON timing.
Since it does not have error amplifier and constitutes a feedback loop by the comparator, IC enables fast control to load response during PWM operation.

7 Adaptive ON Time Controller

This block is ON time controlled using a unique adaptive ON time control technology.

Stable load current:	IC operates in PWM operation by constant ON time control.
Fluctuating load current:	IC operates in the constant ON time control and fluctuate the switching frequency. It results from fast response.
Light load:	The switching frequency decreases and realizes a high efficiency by PFM operation during discontinuous mode.

When the load current fluctuates, IC operates f_{SW_MAX} or below. IC raises the primary average current by shortening the OFF time. It results from increasing the secondary current and secondary output voltage is quickly stable.

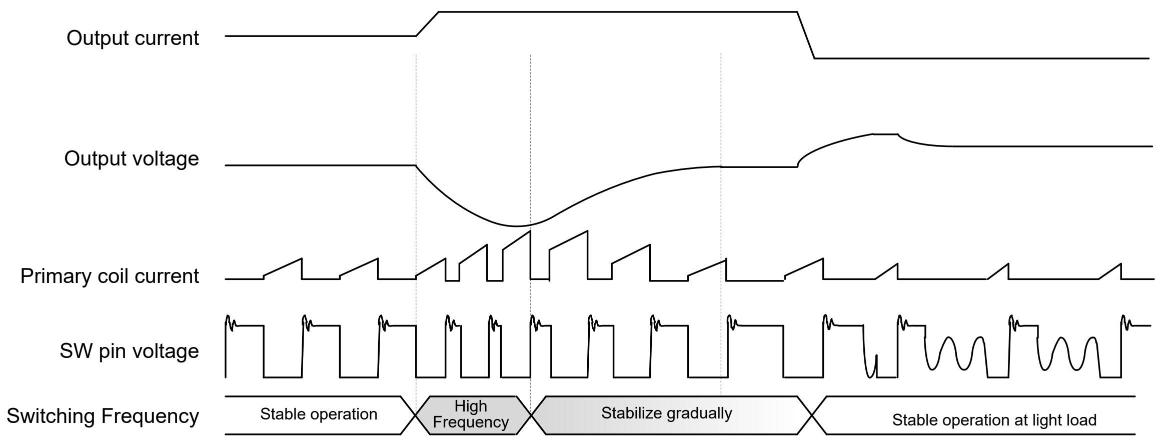


Figure 3. Load Current Response Timing Chart

8 Maximum Frequency Limit Function (MAX FREQ)

This function limits the maximum switching frequency. Even if the frequency becomes high during startup or load fluctuation, it operates at or below the maximum frequency of f_{SW_MAX}. This suppresses EMI noise.

9 DRIVER

This is the block which drives Nch MOSFET for switching.

10 Nch MOSFET

This is Nch MOSFET for switching.

Description of Blocks – continued

11 Load Compensation

This block compensates the decrease of output voltage caused by the change of V_F characteristic in the secondary output diode which is proportional to load current. It monitors the current flown to the switching MOSFET and a part of the current flows to the REF pin. The quantity of compensation determines by the external resistor and capacitor at the L_COMP pin and K_{L_COMP} which is coefficient for SW current. For that, as the current flown from the FB pin to the external resistor of the REF pin decreases, the output voltage decrease is compensated.

12 Frequency Spectrum Spread

This is the function to spread switching frequency.
The frequency spreading in the range of ±5 % contributes to low EMI.

13 Over Current Protection (OCP), Battery Short Protection (BSP)

This function is over current protection of the MOSFET.

13.1 Over Current Protection (OCP)

When the switching MOSFET is ON, as the primary transformer peak current becomes I_{LIMIT} or more, IC detects the over current and the switching MOSFET is turned OFF. Because IC detects OCP per switching cycles, ON duty is limited and the output voltage drops. In addition, to prevent miss detection by turn ON surge, the detection of OCP is invalid for t_{ON_MIN} after the switching MOSFET is turned ON.
After IC detects over current, switching MOSFET is turn OFF after a delay time. When VIN voltage is increased, I_{LIMIT} is higher by the effect of delay time. ΔI_{LIMIT} depends on L_P value of transformer.

$$\Delta I_{LIMIT} = VIN \times t_{DELAY} / L_P \quad \text{[A]}$$

where:

t_{DELAY} is the OCP detection delay time.
L_P is the primary inductance.

t_{DELAY} is always 0.2 µs or less.

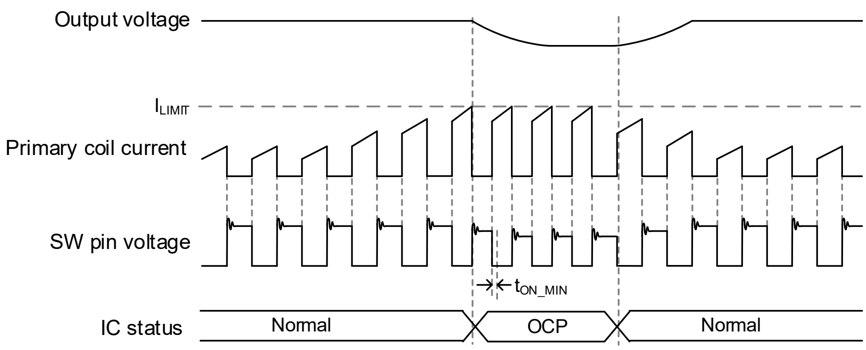


Figure 4. OCP Timing Chart

13 Over Current Protection (OCP), Battery Short Protection (BSP) – continued

13.2 Battery Short Protection (BSP)

In the case of increasing peak current by CCM (continuous conduction mode) operation such as the short of the transformer winding or output short of secondary, large current over I_{LIMIT} is flown to the switching MOSFET. To prevent this phenomenon, IC is built-in BSP function. When SW pin current becomes I_{BSP} or more at the switching MOSFET ON, the IC detects BSP. By this function, the switching operation is stopped in the period of t_{BSP}. After it passes t_{BSP}, IC recovers switching operation without soft-start function. When BSP state continues, IC stops switching operation by SCP protection because output voltage is low. BSP is affected by the delay time (t_{DELAY}) the same as OCP, and I_{BSP} increases according to VIN voltage. Also, when primary transformer is short, the function is operated.

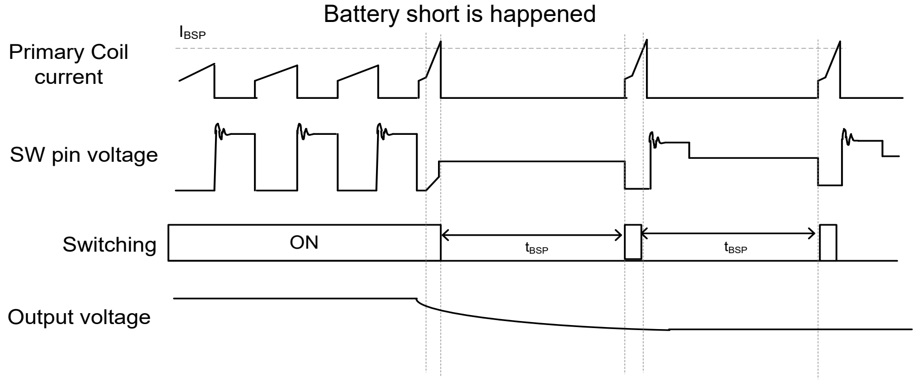


Figure 5. BSP Timing Chart

14 Short Circuit Protection (SCP), REF Pin Open Protection (REFOPEN)

This is the block of the short protection and the open protection of the REF pin.

14.1 Output Short Circuit Protection (SCP)

As IC converts the primary flyback voltage to REF pin voltage, IC detects secondary output status. When secondary output voltage drops, REF pin voltage also drops. When REF pin voltage is V_{SCP} or below, IC detects SCP. When the detection continues for t_{MASK}, the switching operation is stopped. After the time of $t_{RESTART}$ passes from the stop, IC restarts with soft start function. To prevent SCP miss detection, the detection of SCP is invalid for $t_{MASKSCP}$ at startup. When REF voltage is V_{SCP} or below for $t_{MASKSCP}$ from startup, IC stops switching for $t_{RESTART}$.

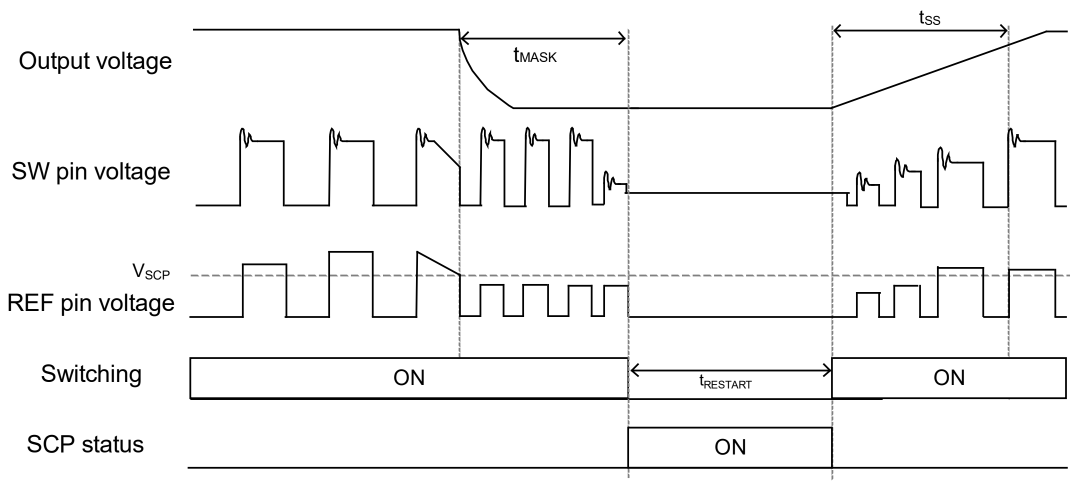


Figure 6. SCP Timing Chart

14 Short Circuit Protection (SCP), REF Pin Open Protection (REFOPEN) – continued

14.2 REF Pin Open Protection (REFOPEN)

The REF pin detects the secondary output voltage status from the primary flyback voltage. When the REF pin is open, output status is not detected, and switching MOSFET may occur malfunction. Therefore, when the REF pin voltage is V_{REFOP} or above, the IC detects REFOPEN protection. When the detection continues for t_{MASK}, the switching operation is stopped. After the time of $t_{RESTART}$ from the stop, IC restarts with soft start function.
When auto recovery, IC operates for t_{MASK} from startup. When REF pin voltage is V_{REFOP} or above for t_{MASK}, IC stops switching for $t_{RESTART}$.

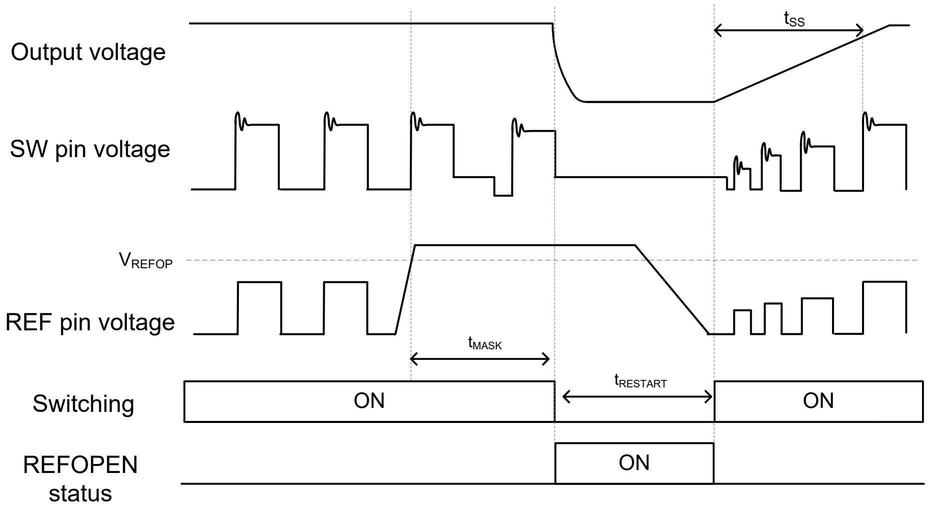


Figure 7. REFOPEN Protection Timing Chart

14.3 REF Pin Short Protection (REFSHORT)

The IC detects the REF pin resistance at startup. When VIN reaches UVLO detection voltage 2 after power on, the REF pin short circuit detection current flows from the internal power supply to the REF pin. If the REF pin resistance detection voltage 1 V_{REFR1} is not reached after the REF pin resistance detection time t_{REFR}, the IC judges the REF pin resistance to be an abnormal value and stops switching. After the restart time $t_{RESTART}$ has elapsed, the IC checks the REF pin resistance again. When the REF pin resistance returns to normal, the IC starts switching with soft start operation.

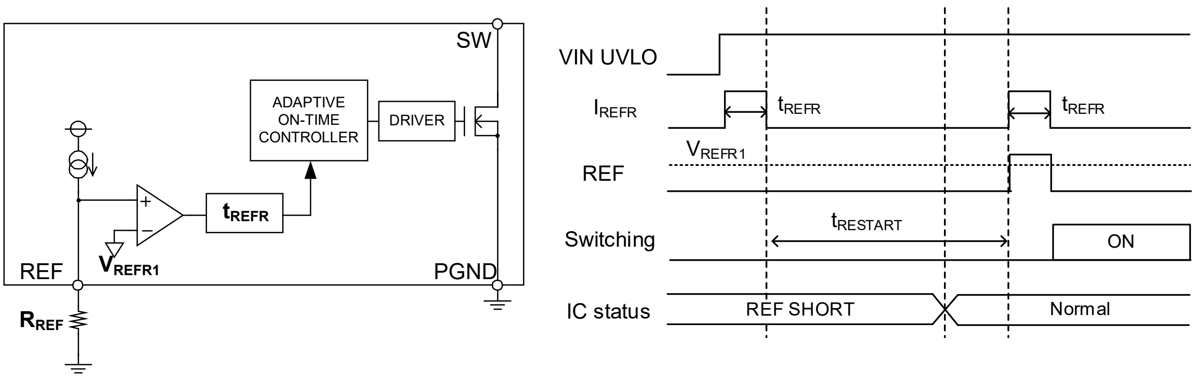


Figure 8. REFSHORT Protection Timing Chart

Description of Blocks – continued

15 REF Pin Noise Filter

This is the block of the noise filter of the REF pin

15.1 REF Pin Noise Mask Function

This IC detects the output voltage at the REF pin and performs duty control. If low-frequency noise is superimposed on this REF pin voltage, the output ripple voltage may momentarily deteriorate. To prevent this, the Nth voltage detection at the REF pin is compared with the N-1th REF pin voltage.
If this comparison voltage is greater than V_{RNOISE} (Typ = 0.06 V), feedback is not performed on the Nth data, but on the N-1th data. This operation makes it possible to mask data for one false detection.

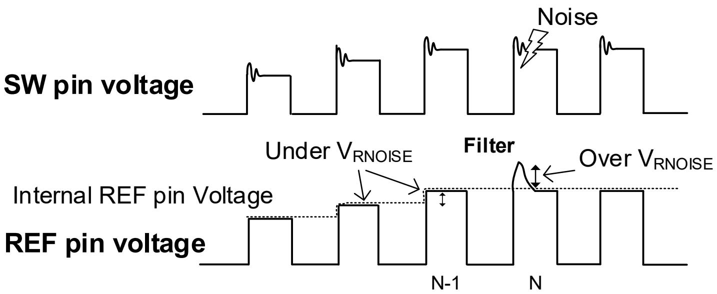


Figure 9. REF Pin Nosie Filter

15.2 2-step MAXOFF

If noise is present in the REF pin voltage, the two-stage MAXOFF1 function operates. If the REF pin voltage rises due to noise, a turn-on signal is not generated and the IC operates at MAXOFF1 (t_{OFF_MAX1} = 3.2 μs Typ). If the REF pin voltage returns to the reference voltage (V_{INTREF} = 0.54 V Typ) within two cycles, the IC will return to normal operation. If the REF pin voltage is detected as being higher than the reference voltage due to noise even after two cycles, the IC will transition from MAXOFF1 to MAXOFF2 (t_{OFF_MAX2} = 35 μs Typ).

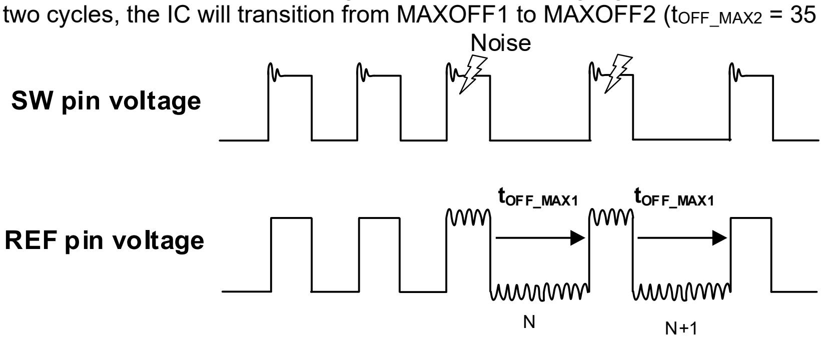


Figure 10. 2-step MAXOFF

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
VIN Pin Voltage	V_{IN}	-0.3 to +40	V
SW Pin Voltage	V_{SW}	-0.3 to +82	V
SDX/EN Pin Voltage	$V_{SDX/EN}$	-0.3 to +40	V
FB Pin Voltage	V_{FB}	-0.3 to +40	V
REF Pin Voltage	V_{REF}	-0.3 to +7	V
L_COMP Pin Voltage	V_{L_COMP}	-0.3 to +7	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
HTSSOP-B20				
Junction to Ambient	θ_{JA}	108.7	32.8	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	13.0	9.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operation Power Supply Voltage Range	V_{IN}	3.4	12.0	36.0	V	VIN pin voltage
Operation Voltage Range	V_{SW}	-	-	80	V	SW pin voltage
Operation Temperature	Topr	-40	-	+125	°C	
REF Pin Resistor	R_{REF}	-	2.7	-	kΩ	External resistor value *(Note 6)*
L_COMP Voltage Range	V_{L_COMP}	-	-	1.00	V	L_COMP pin voltage
VIN-AGND Capacitor	C_{VIN}	10	-	-	µF	

(Note 6) Set the REF resistor value of 2.7 kΩ (Typ). Choose the resistance accuracy for an output voltage accuracy.

Electrical Characteristics (Unless otherwise Tj = -40 °C to +150 °C, V_{IN} = 12 V, $V_{SDX/EN}$ = 2.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Block						
Current at Shutdown	I_{ST}	-	0	10	µA	SDX/EN pin = 0.3 V Tj ≤ 125 °C
Operating Current at No Switching	I_{CC}	0.85	1.25	1.70	mA	REF pin = 0.6 V
UVLO Detection Voltage 1	V_{UVLO1}	3.00	3.20	3.40	V	At the VIN pin falling
UVLO Detection Voltage 2	V_{UVLO2}	3.20	3.40	3.60	V	At the VIN pin rising
UVLO Voltage Hysteresis	V_{UVLO_HYS}	0.12	0.20	0.28	V	
Shutdown and Enable Control Block						
Shutdown Voltage at the SDX/EN Pin	V_{SDX}	-	-	0.3	V	
Enable Voltage 1	V_{EN1}	1.90	2.00	2.10	V	At the SDX/EN pin rising
Enable Voltage 2	V_{EN2}	1.60	1.80	2.00	V	At the SDX/EN pin falling
Enable Voltage Hysteresis	V_{EN_HYS}	0.14	0.20	0.26	V	
SDX/EN Pin Current	$I_{SDX/EN}$	0.50	1.00	2.00	µA	SDX/EN pin = 2.5 V
SDX/EN Pin Pull-down Resistance	$R_{SDX/EN}$	1250	2500	3750	kΩ	
Reference Voltage Block						
Reference Voltage	V_{INTREF}	0.525	0.540	0.555	V	
REF Pin Current	I_{REF}	140	200	260	µA	R_{REF} = 2.7 kΩ
Switching Block						
ON Resistance	R_{ON}	-	0.10	0.27	Ω	SW-PGND I_{SW} = 50 mA
Over Current Detection Current	I_{LIMIT}	4.08	5.10	6.24	A	
BSP Detection Current	I_{BSP}	5.30	6.63	8.12	A	
Averaging Switching Frequency	f_{SW}	300	363	430	kHz	At PWM operation (Duty = 40 %)
Maximum Switching Frequency	f_{SW_MAX}	-	-	498	kHz	
ON Time	t_{ON}	0.962	1.102	1.270	µs	At PWM operation (Duty = 40 %)
Minimum ON Time	t_{ON_MIN}	120	250	380	ns	
Maximum OFF Time 1	t_{OFF_MAX1}	2.2	3.2	5.5	µs	
Maximum OFF Time 2	t_{OFF_MAX2}	25	35	45	µs	
Soft Start Time	t_{SS}	6.0	10.0	14.0	ms	From switching start to V_{INTREF} x 90 %
Protection Function Block						
Short Protection Detection Voltage	V_{SCP}	0.20	0.30	0.40	V	
REF Pin Open Protection Detection Voltage	V_{REFOP}	0.60	0.70	0.80	V	
REF Pin Resistance Detection Current	I_{REFR}	150	200	250	µA	
REF Pin Resistance Detection Voltage 1	V_{REFR1}	0.35	0.40	0.45	V	
REF Pin Resistance Detection Voltage 2	V_{REFR2}	0.43	0.48	0.53	V	
REF Pin Resistance Detection Time	t_{REFR}	22	47	72	µs	
SCP/REFOPEN Detection Mask Time	t_{MASK}	1.05	1.50	1.95	ms	
SCP Mask Time at Startup	$t_{MASKSCP}$	9.0	13.5	18.0	ms	
BSP Stop Time at Detection	t_{BSP}	262	375	488	µs	
Restart Time	$t_{RESTART}$	36.0	48.0	60.0	ms	
Load Compensation Block						
KL_COMP (Compensation Coefficient of REF Current for SW Current)	K_{L_COMP}	0.028	0.040	0.052	%/MΩ	*(Note 1)*

(Note 1) Load compensation current coefficient is the coefficient which compensates output voltage decrease for output current.
It sets by L_COMP pin resistor. It is tested at R_{L_COMP} = 10 kΩ.

Typical Performance Curves

(Reference Data)

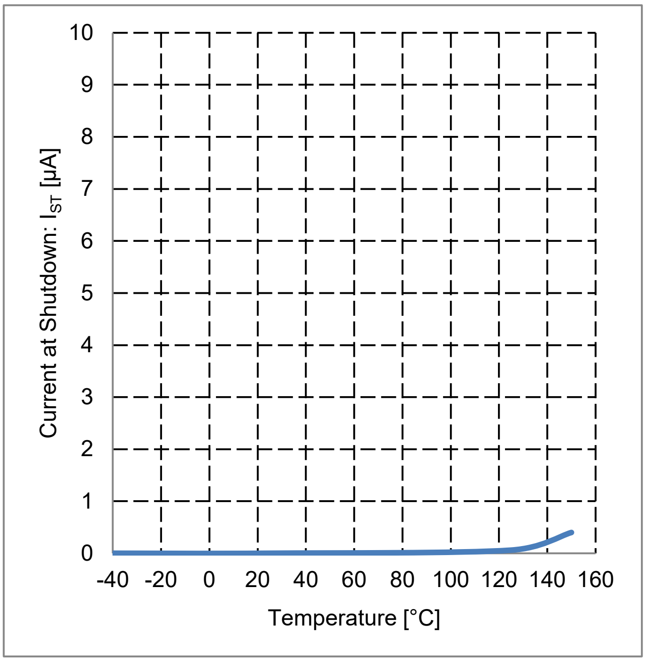


Figure 11. Current at Shutdown vs Temperature

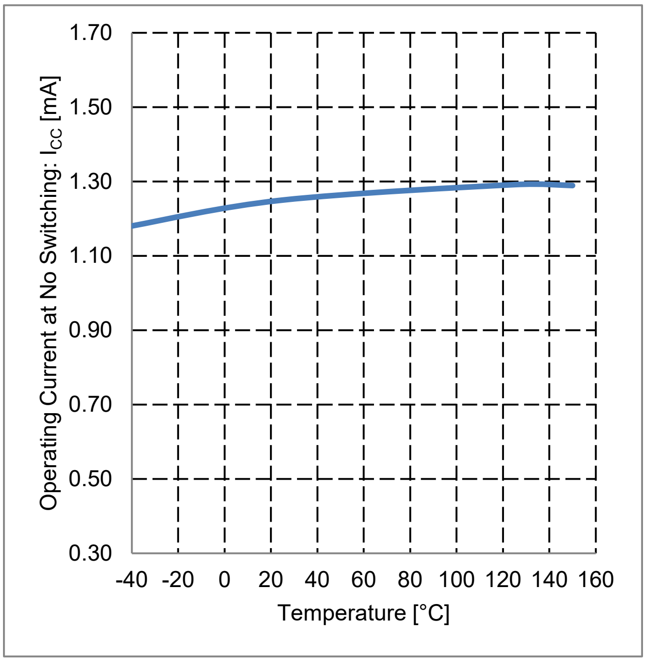


Figure 12. Operating Current at No Switching vs Temperature

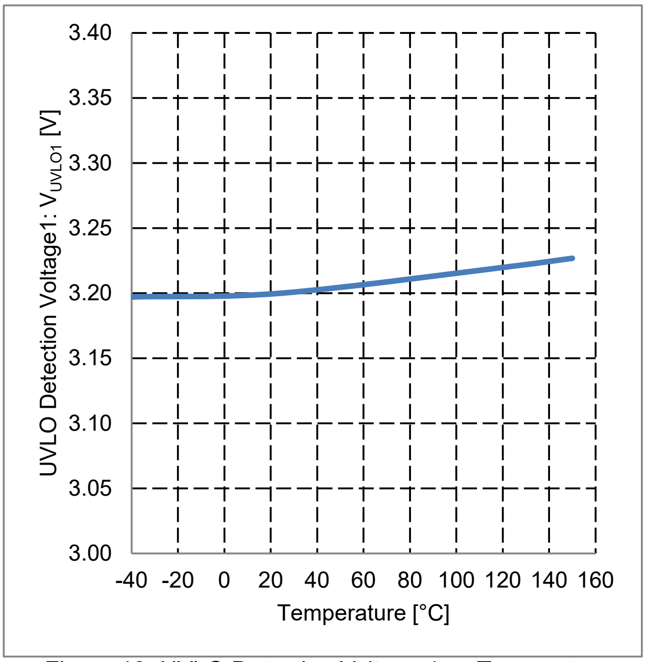


Figure 13. UVLO Detection Voltage 1 vs Temperature

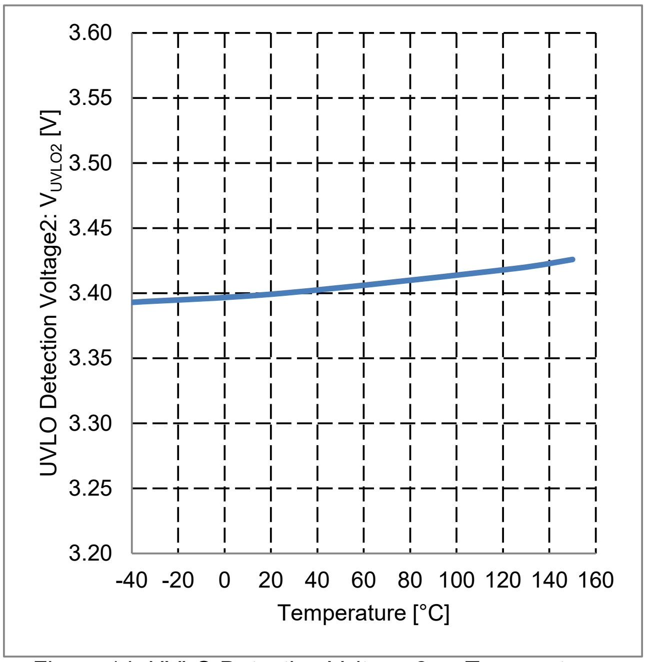


Figure 14. UVLO Detection Voltage 2 vs Temperature

Typical Performance Curves – continued

(Reference Data)

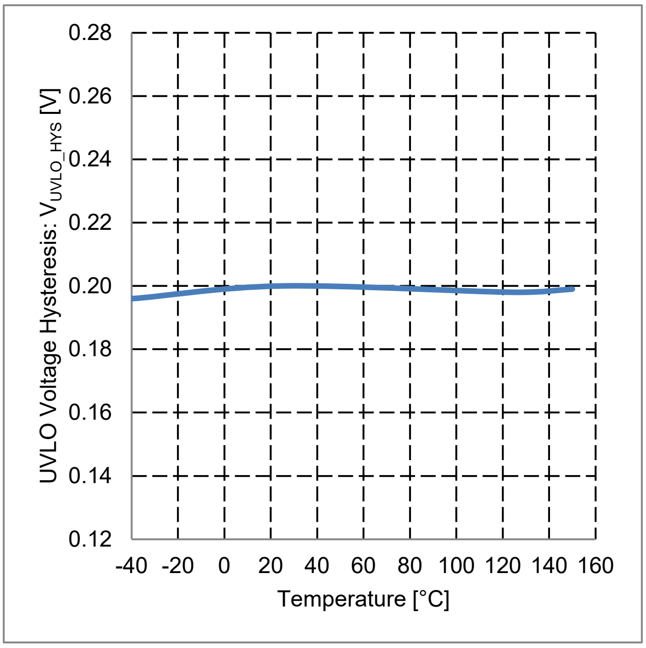


Figure 15. UVLO Voltage Hysteresis vs Temperature

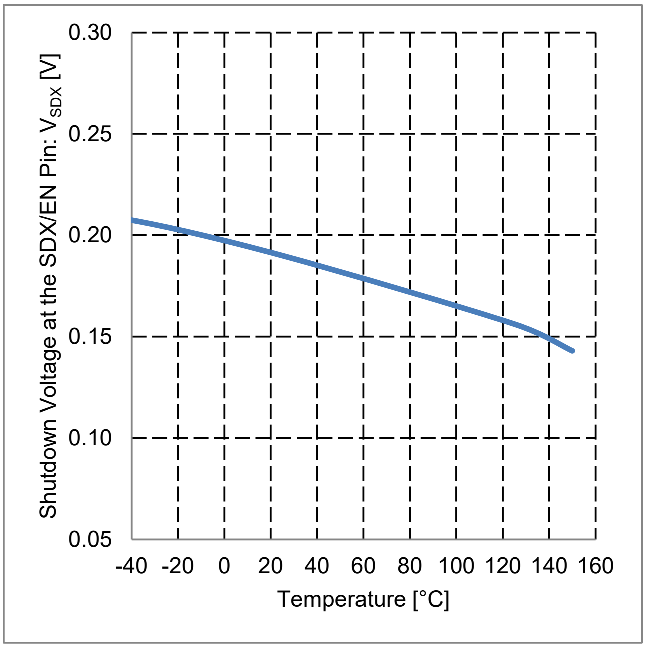


Figure 16. Shutdown Voltage at the SDX/EN Pin vs Temperature

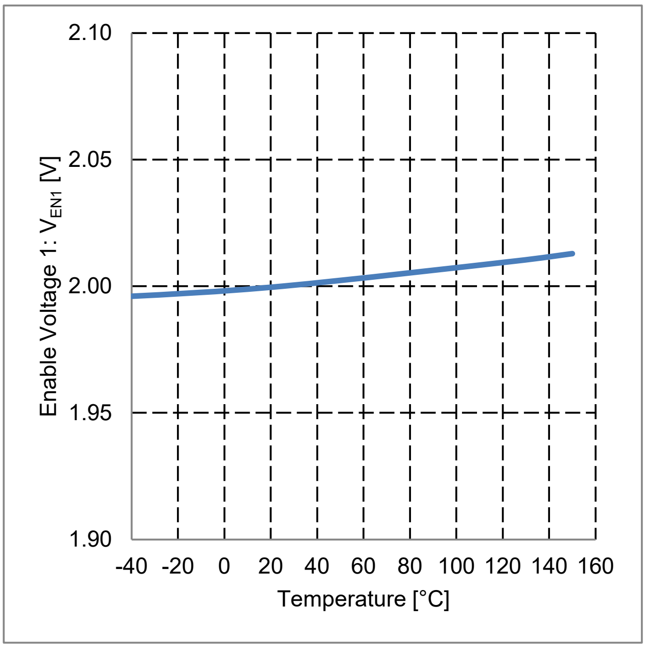


Figure 17. Enable Voltage 1 vs Temperature

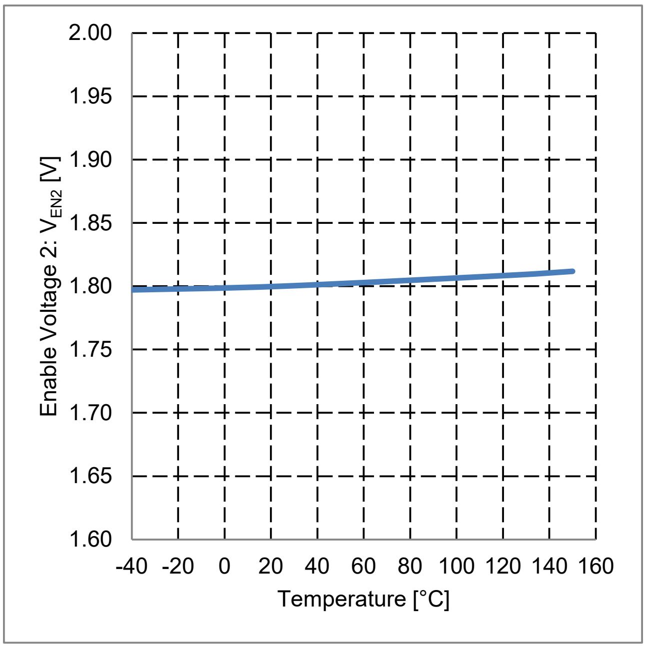


Figure 18. Enable Voltage 2 vs Temperature

Typical Performance Curves – continued

(Reference Data)

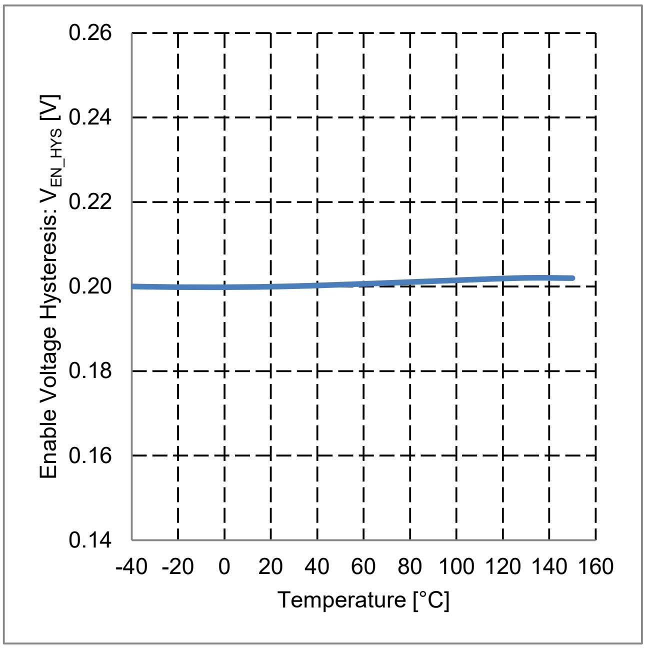


Figure 19. Enable Voltage Hysteresis vs Temperature

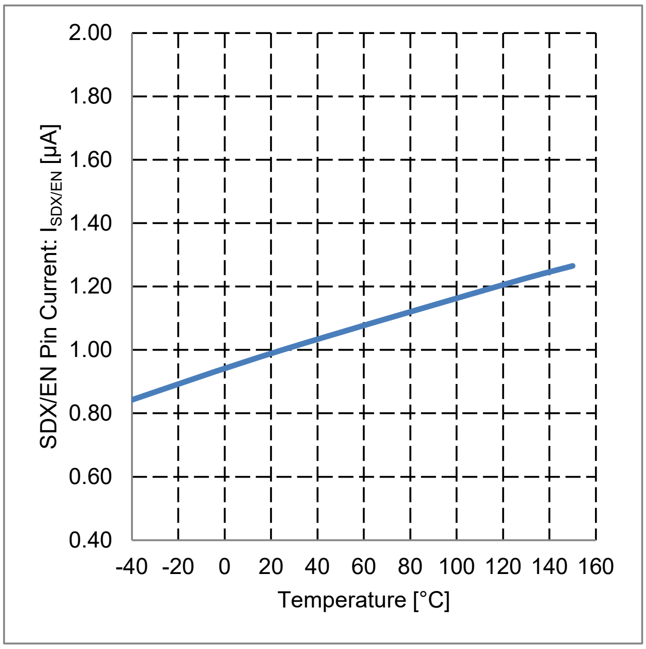


Figure 20. SDX/EN Pin Current vs Temperature

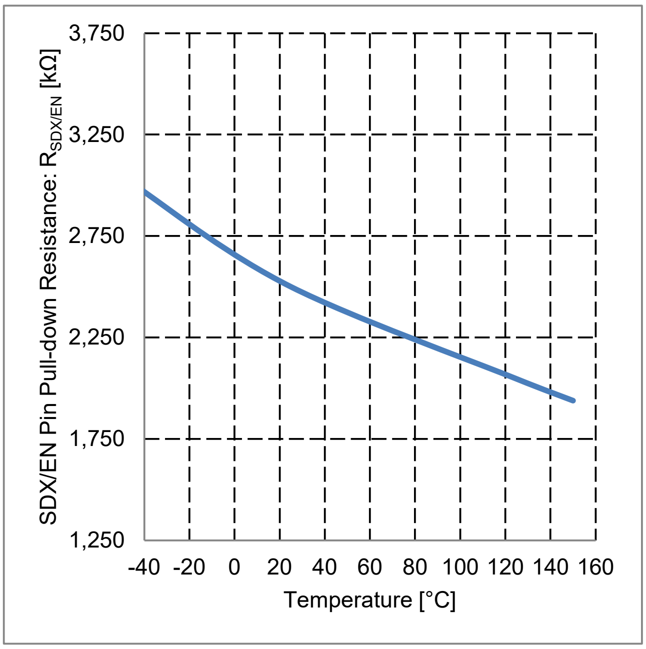


Figure 21. SDX/EN Pin Pull-down Resistance vs Temperature

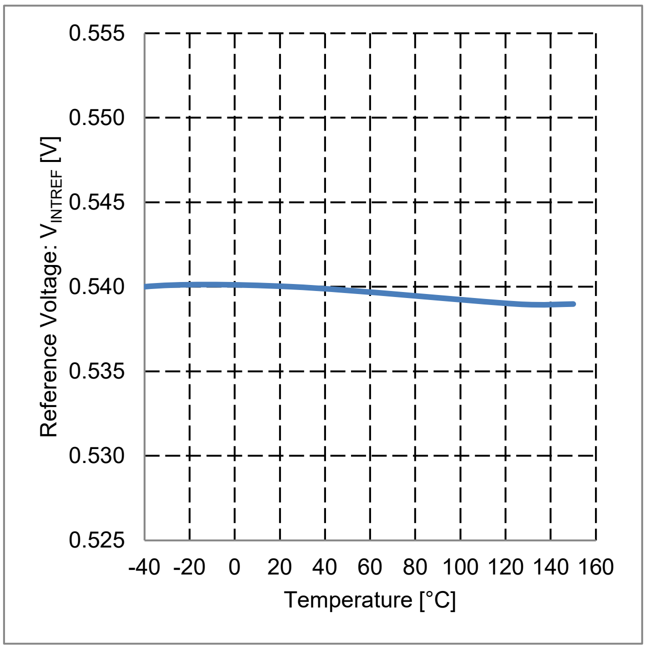


Figure 22. Reference Voltage vs Temperature

Typical Performance Curves – continued

(Reference Data)

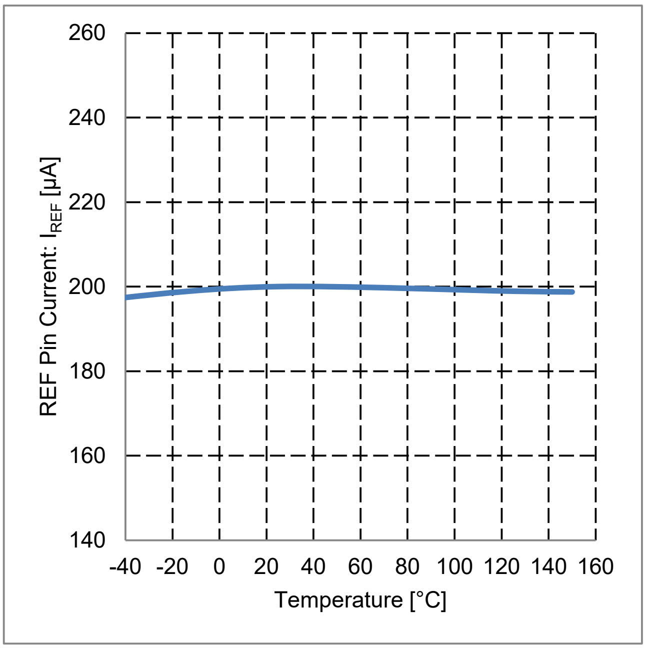


Figure 23. REF Pin Current vs Temperature

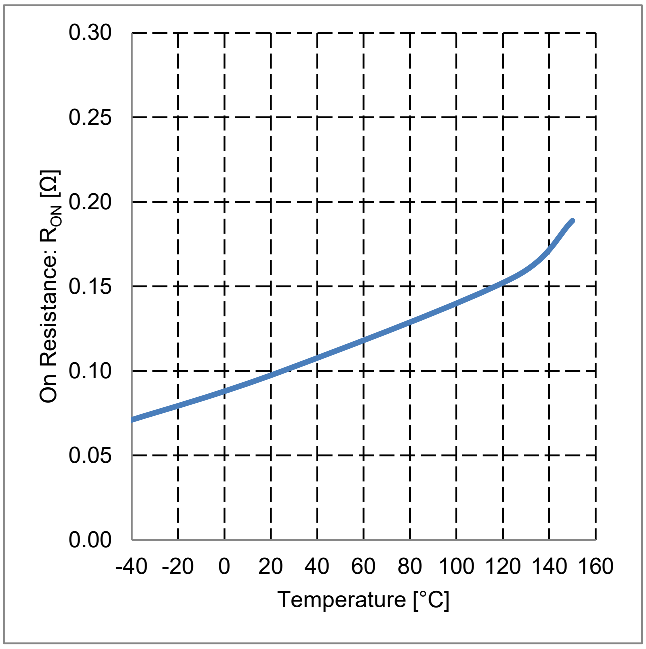


Figure 24. ON Resistance vs Temperature

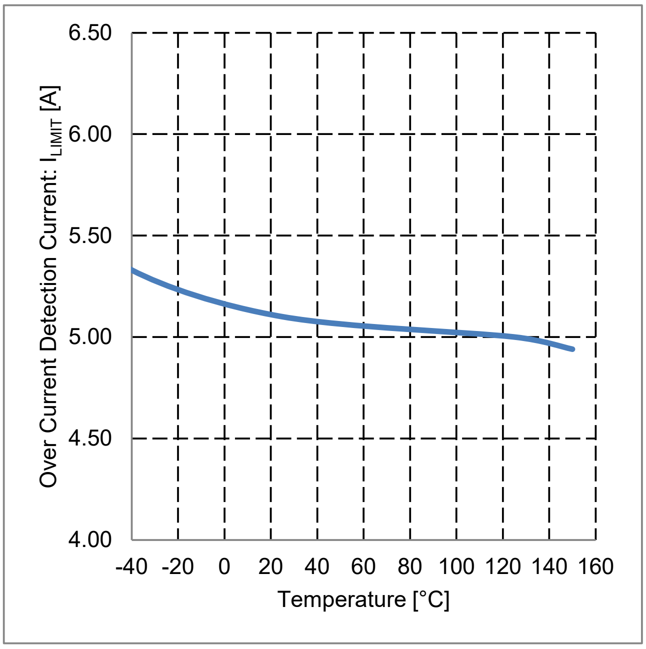


Figure 25. Over Current Detection Current vs Temperature

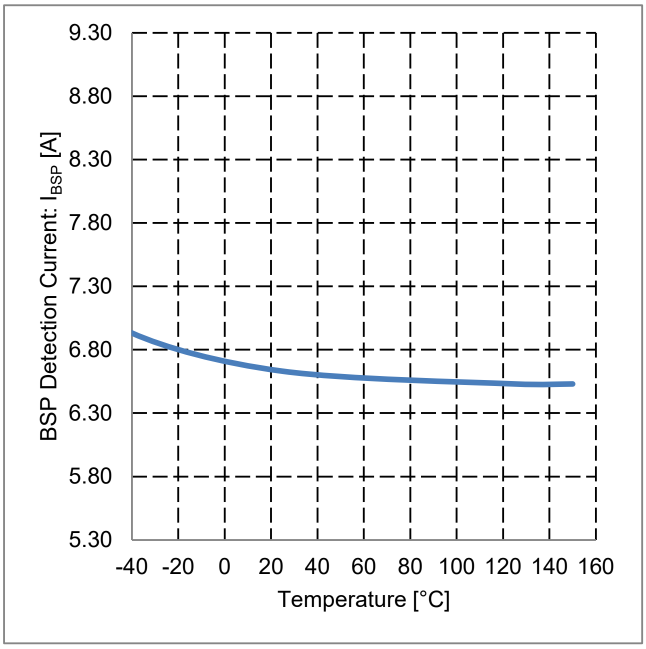


Figure 26. BSP Detection Current vs Temperature

Typical Performance Curves – continued

(Reference Data)

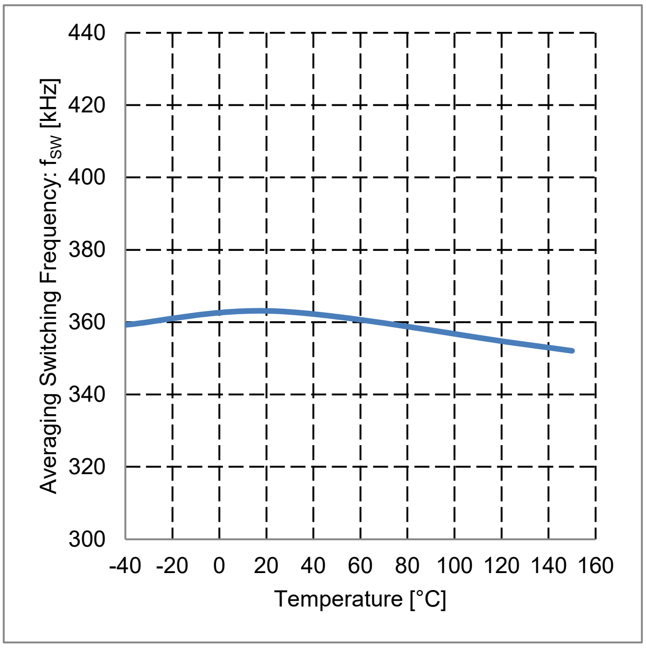


Figure 27. Averaging Switching Frequency vs Temperature

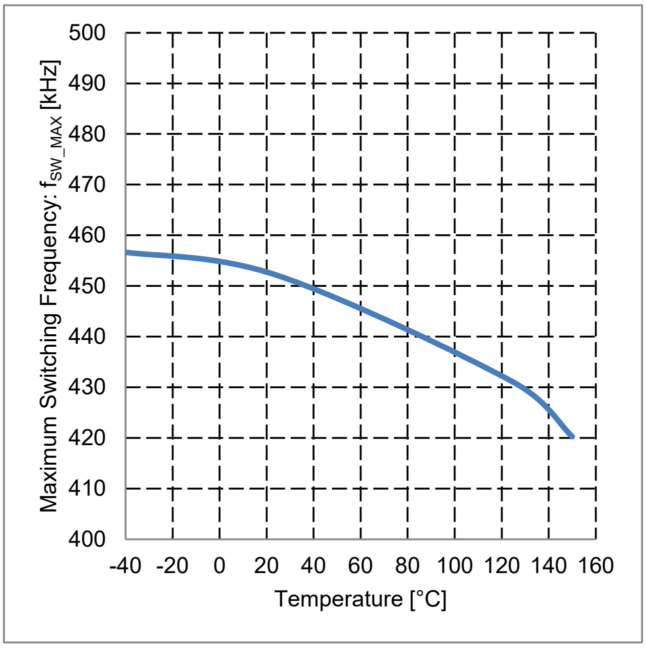


Figure 28. Maximum Switching Frequency vs Temperature

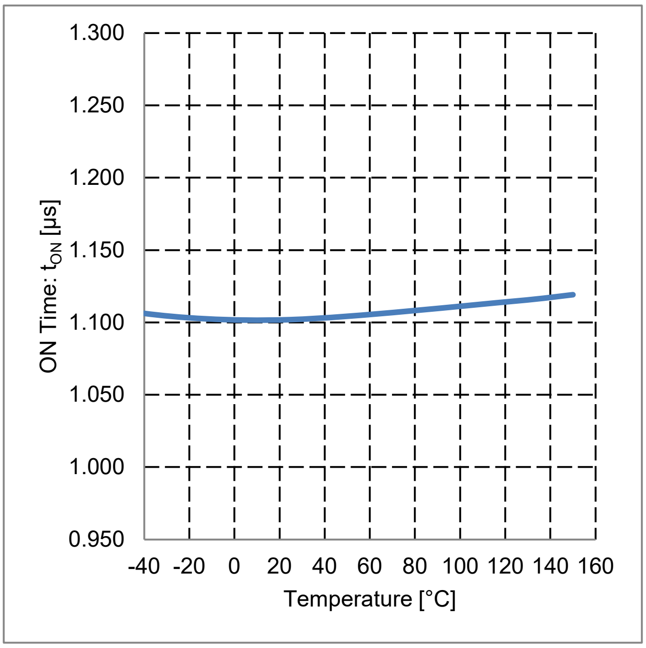


Figure 29. ON Time vs Temperature
(Duty = 40 %, f_{SW} = 363 kHz)

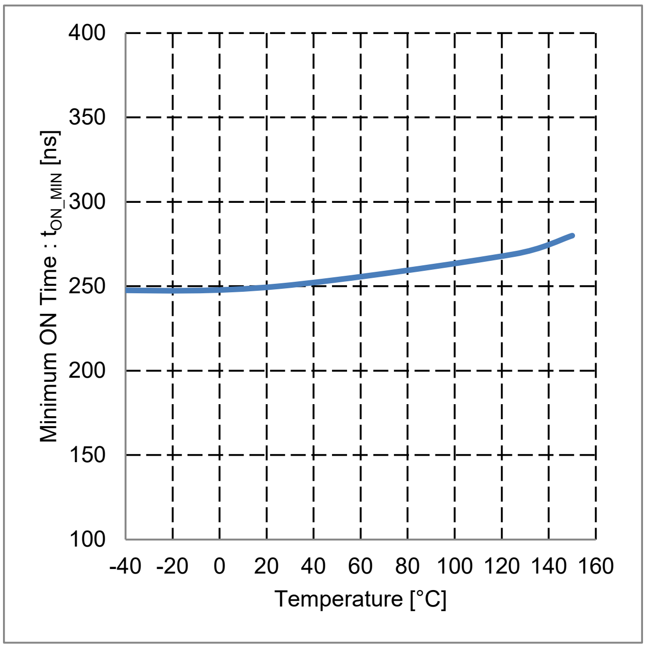


Figure 30. Minimum ON Time vs Temperature

Typical Performance Curves – continued

(Reference Data)

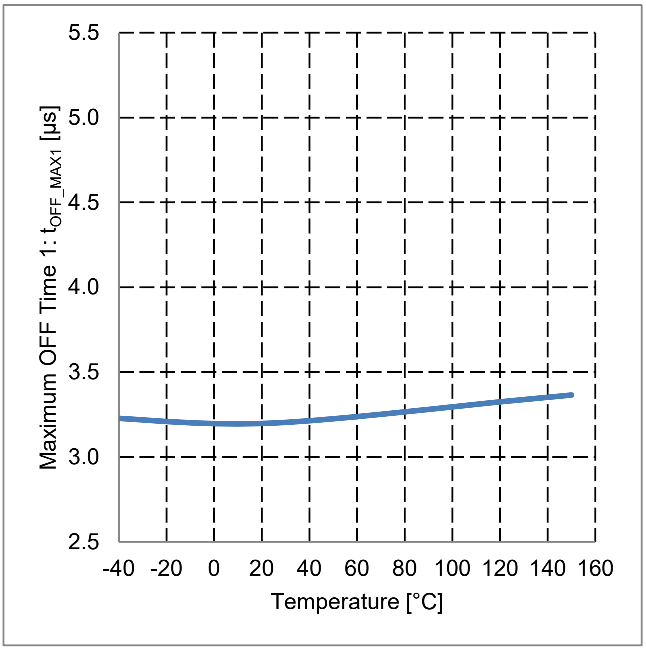


Figure 31. Maximum OFF Time 1 vs Temperature

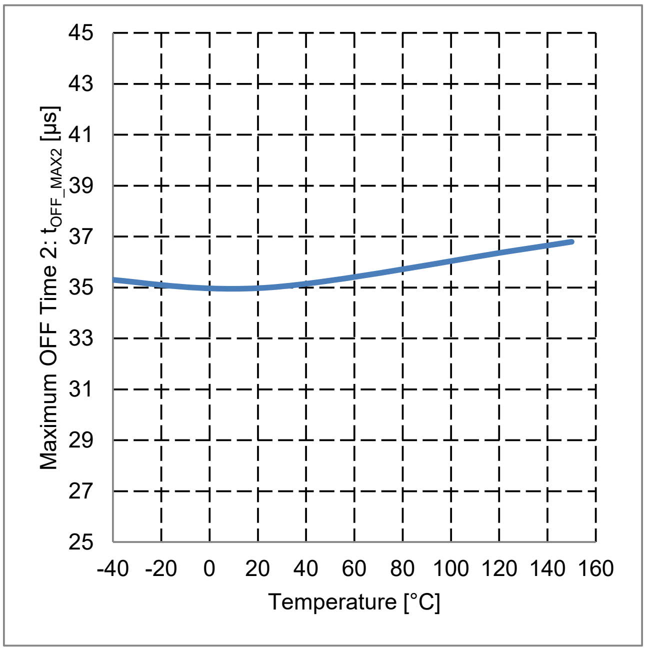


Figure 32. Maximum OFF Time 2 vs Temperature

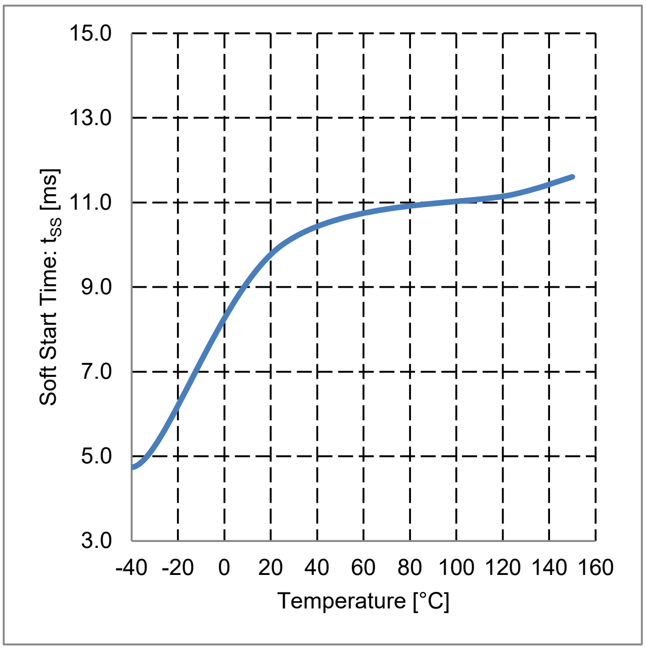


Figure 33. Soft Start Time vs Temperature

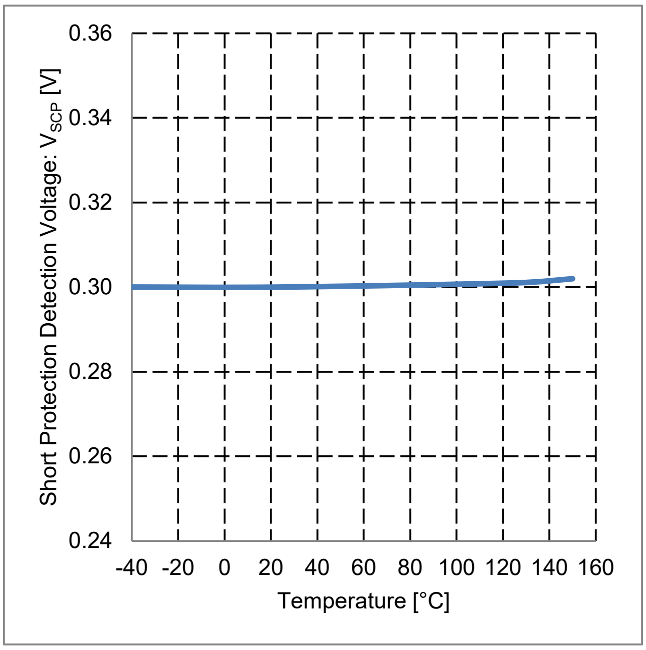


Figure 34. Short Protection Detection Voltage vs Temperature

Typical Performance Curves – continued

(Reference Data)

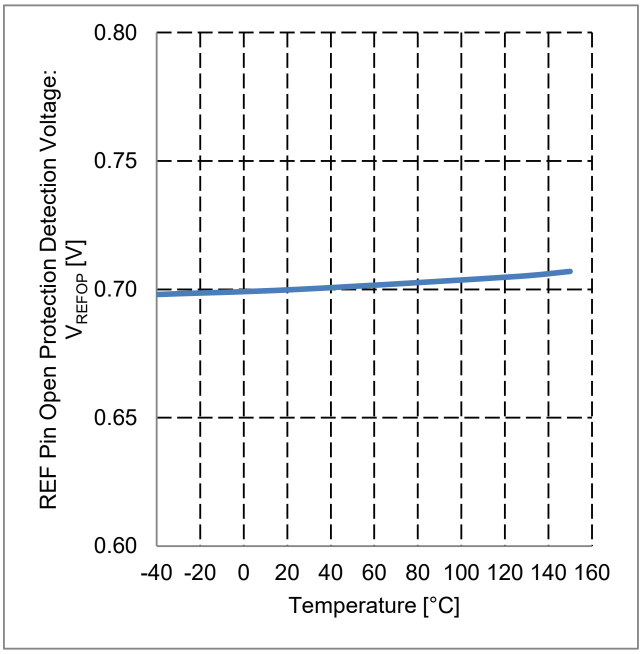


Figure 35. REF Pin Open Protection Detection Voltage vs Temperature

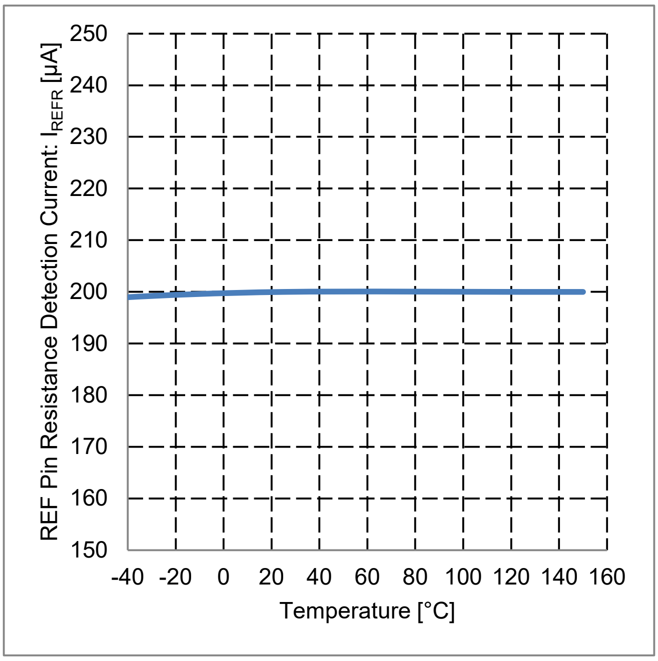


Figure 36. REF Pin Resistance Detection Current vs Temperature

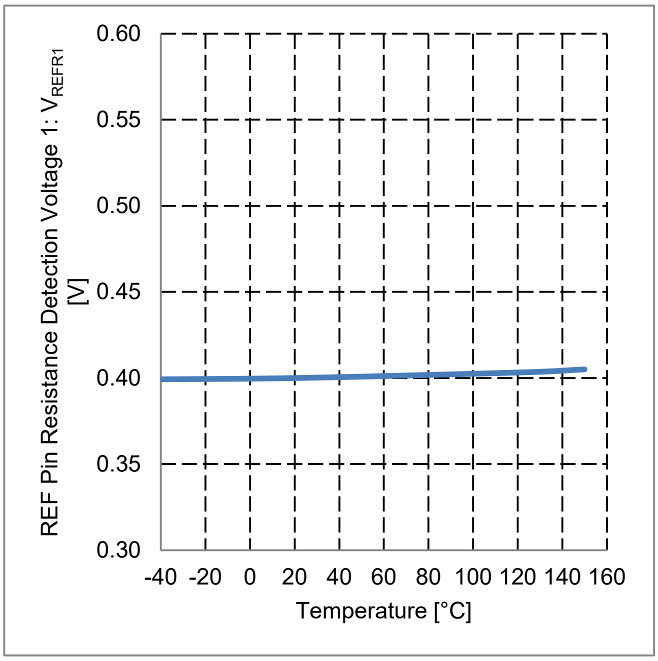


Figure 37. REF Pin Resistance Detection Voltage 1 vs Temperature

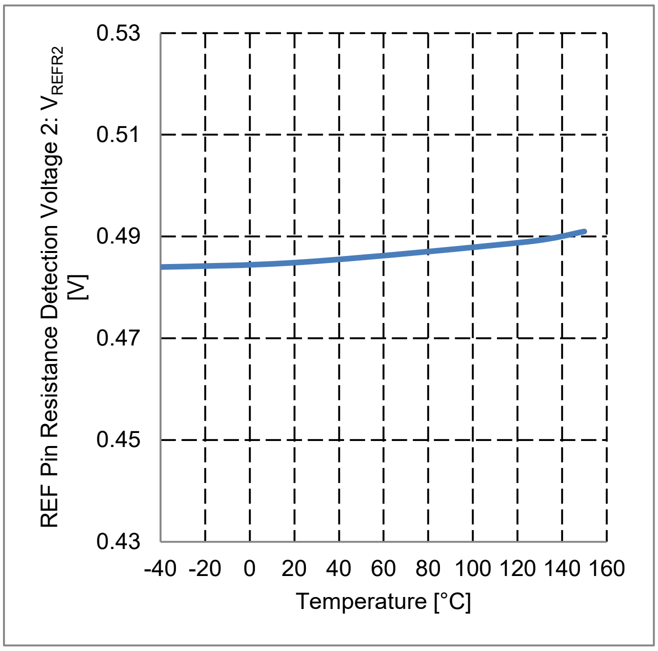


Figure 38. REF Pin Resistance Detection Voltage 2 vs Temperature

Typical Performance Curves – continued

(Reference Data)

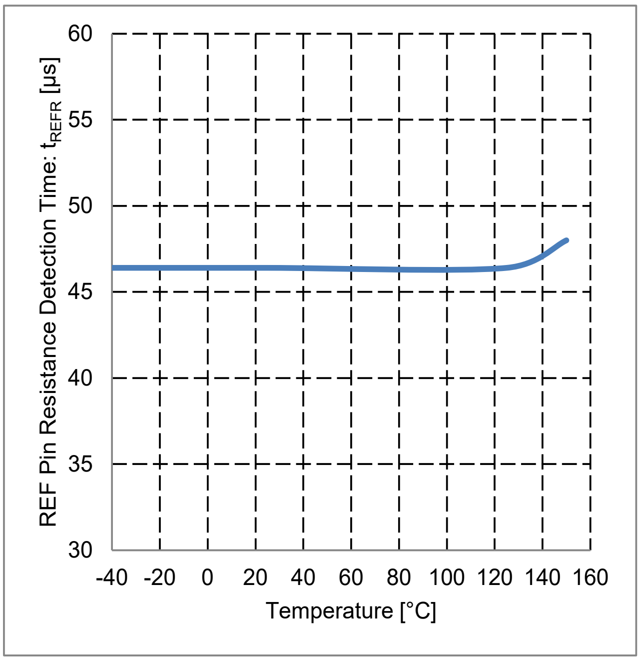


Figure 39. REF Pin Resistance Detection Time vs Temperature

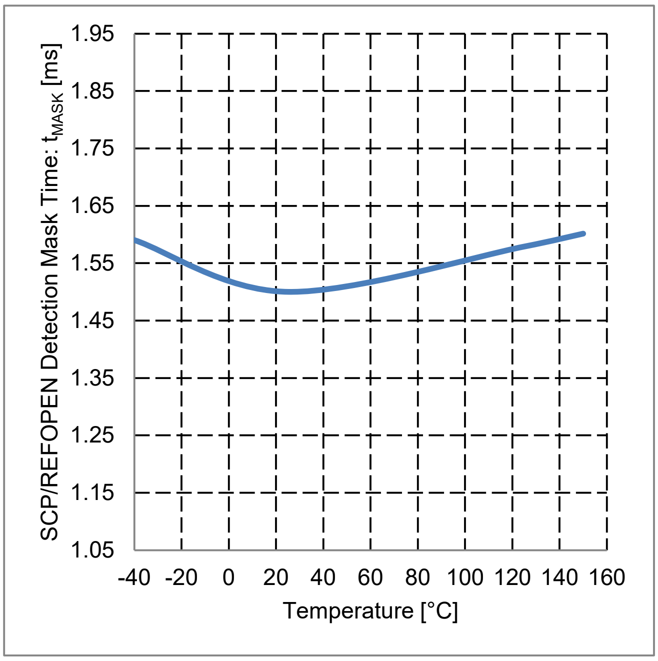


Figure 40. SCP/REFOPEN Detection Mask Time vs Temperature

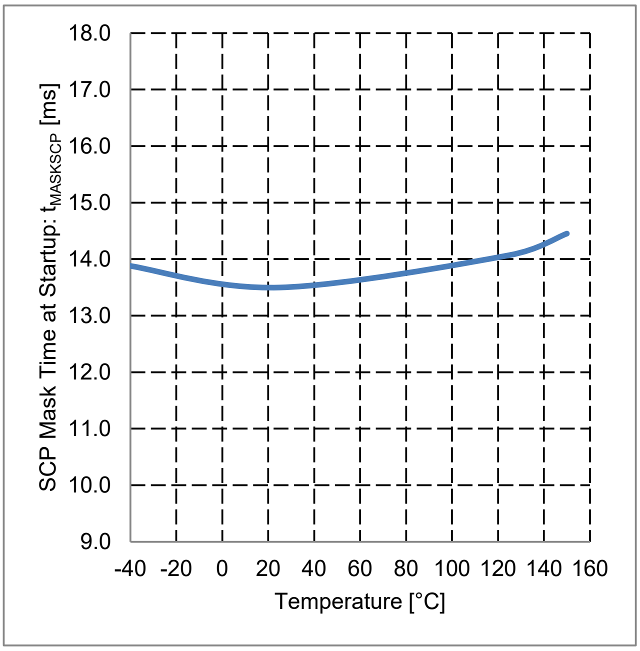


Figure 41. SCP Mask Time at Startup vs Temperature

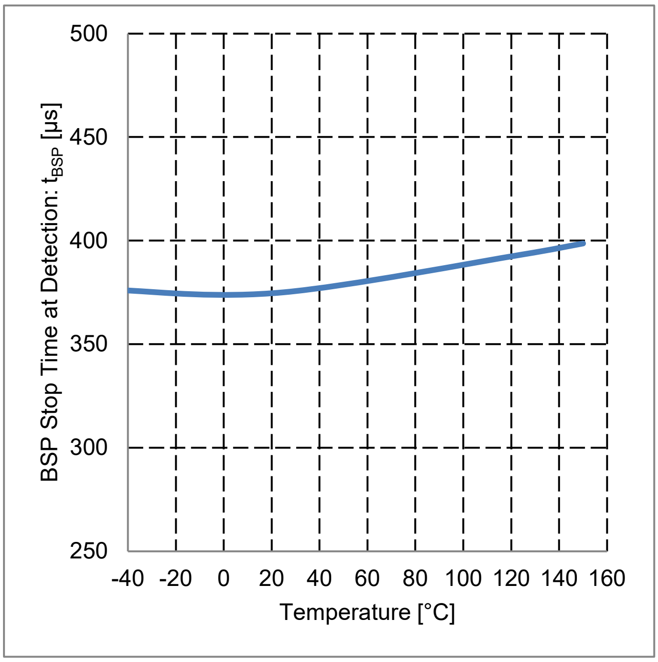


Figure 42. BSP Stop Time at Detection vs Temperature

Typical Performance Curves – continued

(Reference Data)

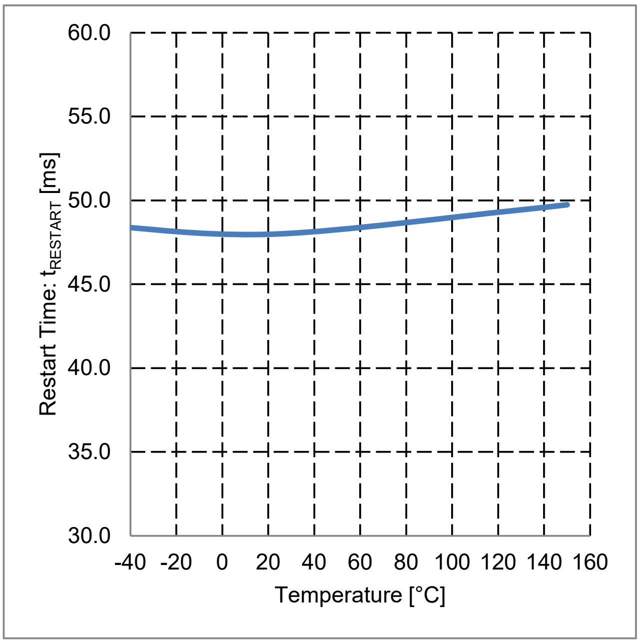


Figure 43. Restart Time vs Temperature

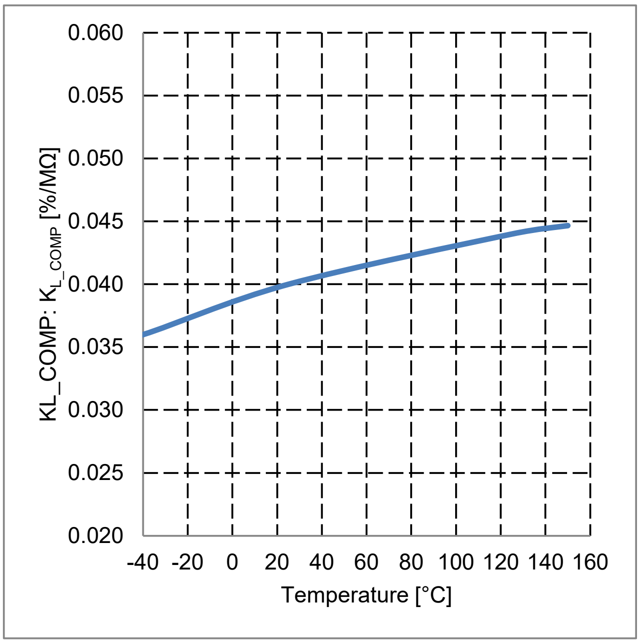


Figure 44. KL_COMP vs Temperature

Application Examples

1 Output Voltage

When the internal switching MOSFET is OFF, SW pin voltage V_{SW} is higher than VIN pin voltage. The secondary output voltage is calculated by the primary flyback voltage, which is described by the difference between this SW pin voltage and VIN pin voltage. The SW pin voltage V_{SW} at turn OFF is calculated by the following formula.

$$V_{SW} = V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad \text{[V]}$$

where:

V_{SW} is the SW pin voltage.
V_{IN} is the VIN pin voltage.
N_P is the primary transformer winding.
N_S is the secondary transformer winding.
V_{OUT} is the output voltage.
V_F is the forward voltage of the secondary output diode.

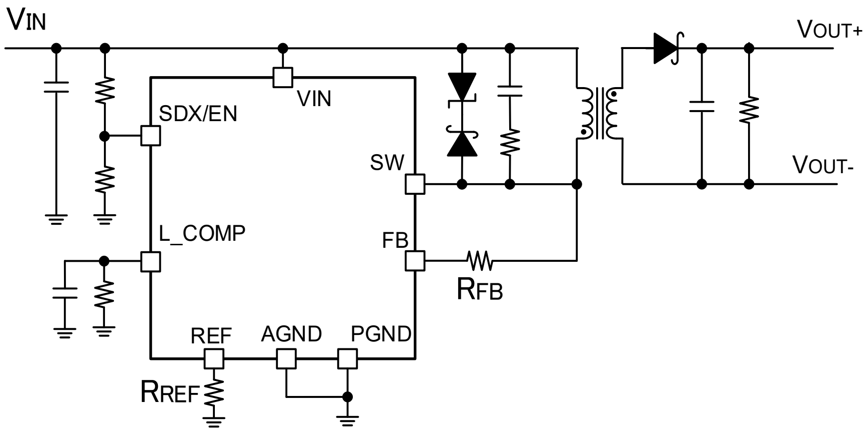


Figure 45. Application Block Diagram

The external resistor R_{FB} between the FB pin and the SW pin converts the primary flyback voltage into the FB pin inflow current I_{FB}. I_{FB} is calculated by the formula below because the FB pin voltage is nearly equal to the VIN pin voltage by IC's internal circuit.

$$I_{FB} = \frac{V_{SW} - V_{FB}}{R_{FB}} = \frac{V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F) - V_{FB}}{R_{FB}} = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F)}{R_{FB}} \quad \text{[A]}$$

where:

I_{FB} is the FB pin inflow current.
V_{FB} is the FB pin voltage.
R_{FB} is the external resistor between the FB pin and the SW pin.

1 Output Voltage – continued

FB pin inflow current I_{FB} flows to the REF pin and the external resistor R_{REF} between the REF pin and the AGND pin. REF pin voltage is calculated by below equation.

$$V_{REF} = \frac{R_{REF}}{R_{FB}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [V]$$

where:

V_{REF} is the REF pin voltage.

R_{REF} is the external resistor between the REF pin and the AGND pin.

R_{REF} is needed to set a resistance of $R_{REF} = \frac{0.54\ V}{200\ \mu A} = 2.7\ k\Omega$
because the current flowing through the REF pin is I_{REF} when the REF pin voltage = V_{INTREF}.
REF pin voltage is input to the comparator with the reference voltage V_{INTREF} in the IC. By the internal circuit, REF pin voltage is equal to the reference voltage. Therefore, the output voltage and REF pin voltage is calculated by the formula below.

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} \times \frac{N_S}{N_P} \times V_{INTREF} - V_F \quad [V]$$

To be shown to the equation, the output voltage is set by the number of winding ratio of the primary and secondary transformer (N_P/N_S) and the resistance ratio of R_{FB} and R_{REF}. According to the relational expression in above, the external resistor R_{FB} between the FB pin and the SW pin is calculated by the formula below.

$$R_{FB} = \frac{R_{REF}}{V_{INTREF}} \times \frac{N_P}{N_S} \times (V_{OUT} + V_F) \quad [\Omega]$$

The ESR of the transformer on the secondary side as well as V_F causes the output voltage drop.
And, when transformer coupling is low, the N_P / N_S turns ratio changes and output voltage is lower than the setting voltage. Therefore, adjust the output voltage by actual evaluation of power supply.

Application Examples – continued

2 Transformer

2.1 The Determine of Winding Ratio N_P/N_S

The winding ratio is the parameter for setting output voltage, Max output power, Duty, SW pin voltage.
The duty of flyback converter is calculated by the following equation:

$$Duty = \frac{\frac{N_P}{N_S} \times (V_{OUT} + V_F)}{V_{IN} + \frac{N_P}{N_S} \times (V_{OUT} + V_F)} \quad [\%]$$

where:

N_P is the primary transformer winding.
N_S is the secondary transformer winding.
V_{OUT} is the output voltage.
V_F is the forward voltage of secondary output diode.
V_{IN} is the VIN pin voltage.

The winding ratio is calculated by below equation.

$$\frac{N_P}{N_S} = \frac{D_{TYP}}{1 - D_{TYP}} \times \frac{V_{IN}}{V_{OUT} + V_F}$$

where:

D_{TYP} is the duty of VIN voltage (Typ).

In the middle VIN voltage of usual operating range, it recommends that D_{TYP} is set from 30 % to 50 %.
First, it recommends to set D_{TYP} = 40 %. The winding ratio is limited by the maximum duty (D_{MAX}) in minimum input voltage condition. D_{MAX} given by the formula below must be not over 70 %. When duty is over 70 %, change D_{TYP} to be lower. If Duty is over 70 %, OFF time is short and the output voltage may change due to the shift in flyback voltage detection.

$$\frac{N_P}{N_S} = \frac{D_{MAX}}{1 - D_{MAX}} \times \frac{V_{IN(MIN)}}{V_{OUT(MAX)} + V_{F(MAX)}}$$

where:

D_{MAX} is the maximum duty of minimum VIN voltage condition.
$V_{OUT(MAX)}$ is the maximum output voltage.
$V_{F(MAX)}$ is the maximum forward voltage (V_F) of secondary diode.

Flyback voltage V_{OR} is calculated by below calculation.

$$V_{OR} = (V_{OUT} + V_F) \times \frac{N_P}{N_S} \quad [V]$$

SW pin voltage calculated below must be set so that the withstand voltage is not exceeded.

$$V_{SW} = V_{IN(MAX)} + V_{OR} + V_{SURGE} \quad [V]$$

For example, when it has the delating of 90 % for SW pin voltage, SW pin voltage is needed to be the value which calculated 72 V or less .

$$V_{SW} = 80\,V \times (100\,\% - 10\,\%) = 72\,V$$

In the case of $V_{IN(MAX)}$ = 30 V and V_{OR} = 10 V, V_{SURGE} voltage is needed to be 32 V or less. This value is calculated below.

$$72\,V - (30\,V + 10\,V) = 32\,V$$

V_{SURGE} is occurred by the leakage of transformer. If V_{SURGE} is higher, it needs to decrease the voltage by redesigning transformation structure or snubber circuit adjustment.

2.1 The Determine of Winding Ratio N_P/N_S – continued

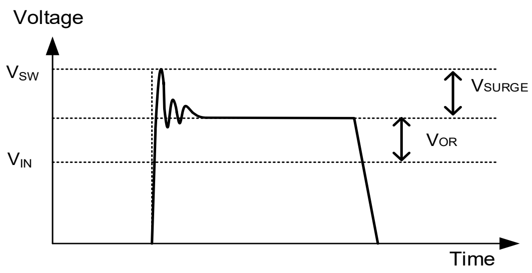


Figure 46. SW Waveform

When designed transformer, temporarily set winding ratio to satisfy above. When the winding ratio is decided, R_{FB} can be set and V_{OUT} also can be set.

2.2 The Calculation of L_P, L_S

The transformer should be set L_P and L_S value that power supply works CCM operation.
For that, L_P and L_S is determined to use "k" which is the indicator of CCM operation.
k is expressed from Figure 47 I_{SPK}, I_{SB} by the following equation.

$$k = (I_{SPK} - I_{SB}) / I_{SPK}$$

where:
I_{SPK} is the secondary transformer peak current.
I_{SB} is the secondary transformer bottom current.
k is constant representing the depth of CCM operation.
(It guides that it sets k = 0.25 when designing at first.)

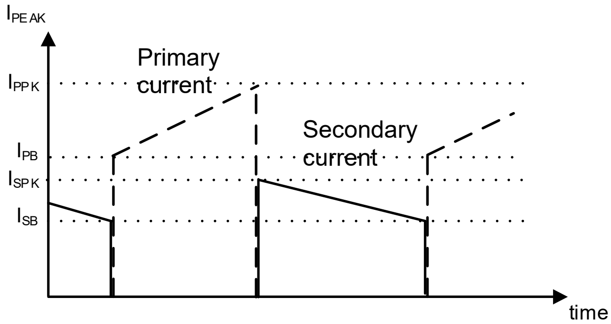


Figure 47. The Waveform Example of Primary and Secondary Current of Transformer

where:
I_{PPK} is the primary transformer peak current.
I_{PB} is the primary transformer bottom current.

I_{LIMIT} shown in electric characteristics determines maximum primary peak current.
It enables to decide capable secondary minimum peak current from minimum I_{LIMIT}.

$$I_{SPK1(MIN)} = I_{LIMIT(MIN)} \times \frac{N_P}{N_S} \quad [A]$$

Next, $I_{SPK2(MAX)}$ is calculated from secondary maximum output current ($I_{OUT(MAX)}$).

$$I_{SPK2(MAX)} = \frac{2 \times I_{OUT(MAX)}}{(1 - D_{MAX}) \times (2 - k)} \times \frac{1}{\eta} \quad [A]$$

where:
η is the efficiency of power supply, it recommends to set to about 70 %.

2.2 The Calculation of L_P, L_S – continued

In order to output $I_{OUT(MAX)}$, the condition of $I_{SPK2(MAX)} < I_{SPK1(MIN)}$ must be satisfied.
If not satisfied, re-design to change k value. The higher the k value, the wider the load area of DCM (discontinuous conduction mode) operation. k = 1 means that the operation is DCM at all loads. IC has advantage of fast response and low EMI characteristics in CCM operation. For that, k is recommended lower value. Even if k value is high, there is no problem with the power supply operation.

The secondary inductance $L_{S(MAX)}$ is calculated by the following equation.

$$L_{S(MAX)} = \frac{(2-k)\times(V_{OUT}+V_F)\times(1-D_{MAX})^2}{2\times I_{OUT(MAX)}\times f_{SW(MAX)}\times k} \quad [\mu H]$$

where:
$f_{SW(MAX)}$ is the switching frequency ($f_{SW(MAX)}$ is set to 430 kHz in IC).
$I_{OUT(MAX)}$ is the maximum secondary output current.

Primary inductance L_P is calculated by below.

$$L_P = L_S \times \left(\frac{N_P}{N_S}\right)^2 \quad [\mu H]$$

2.3 The Calculation of I_{PRMS}, I_{SRMS}

Maximum primary RMS current (I_{PRMS}) and Maximum secondary RMS current (I_{SRMS}) are calculated below.

$$I_{PRMS} = \sqrt{\frac{({I_{PPK}}^2 + I_{PPK}\times I_{PB} + {I_{PB}}^2)\times D_{MAX}}{3}} \quad [A]$$

$$I_{SRMS} = \sqrt{\frac{\left({I_{SPK}}^2 + I_{SPK}\times I_{SB} + {I_{SB}}^2\right)\times(1-D_{MAX})}{3}} \quad [A]$$

When selecting the wire diameter of transformer, refer to this RMS current.

3 Output Capacitor

The output capacitor place as close to the secondary diode as possible. Output capacitor value C_{OUT} is needed to set from the output ripple voltage (ΔV_O) and startup time. The output ripple voltage which occurs by switching is calculated by below equation.

$$\Delta V_O = \frac{I_{OUT(MAX)}\times D_{MAX}}{f_{SW(MAX)}\times C_{OUT}} \quad [V]$$

On the other hand, when output capacitor is large, startup time is long.
When SCP detection mask time ($t_{MASKSCP}$) in startup is passed, if REF voltage is lower than V_{SCP}, power supply cannot output. Therefore, C_{OUT} must be satisfied below condition.

$$C_{OUT} \le \frac{1}{2}\times\frac{t_{MASKSCP(MIN)}\times\left\{\left(I_{LIMIT(MIN)}\times\frac{N_P}{N_S}\right)\times(1-Duty) - I_{OUT(MAX)}\right\}}{V_{OUT}\times\left(\frac{V_{SCP(MAX)}}{V_{INTREF(MIN)}}\right)} \quad [\mu F]$$

Here, $\frac{V_{SCP(MAX)}}{V_{INTREF(MIN)}} = \mathbf{0.762}$

A large output capacitance is required to hold the output voltage for load response or input voltage response. As a guide for output capacitor, it recommends the capacitance of 33 µF or more. And ceramic capacitor may be lower capacitance because of temperature characteristics and variance, DC bias characteristics. It needs to select the parts to care them.

Application Examples – continued

4 Input Capacitor

It uses ceramic capacitor to input capacitor and it is placed as close to the IC as possible.
The capacitor value is set 10 μF or more.

5 Secondary Output Diode

Because the forward voltage (V_F) of secondary output diode causes an error in the output voltage, it needs to use SBD or FRD which is low forward voltage (V_F). And the peak of diode reverse voltage must not exceed the rating of the diode. The secondary RMS current (I_{SRMS}) must be set that it does not exceed the rating current. Generally, it is recommended that the reverse voltage V_R of secondary output diode sets to have margin of 30 % or more.

$$V_R = (V_{IN(MAX)} \times \frac{N_S}{N_P} + V_{OUT}) \times 1.3 + V_{SURGE} \quad [V]$$

where:
V_R is the reverse voltage of secondary output diode.
$V_{IN(MAX)}$ is the VIN maximum pin voltage.
N_P is the primary transformer winding.
N_S is the secondary transformer winding.
V_{OUT} is the output voltage.
V_{SURGE} is the surge voltage of transformer generated to the diode.

And it is recommended that rating current of output diode margin twice or more for I_{SRMS}.

6 Output Resistor and Output Zener Diode (Minimum Load Current)

The output voltage raises in no load or light load. This is the reason IC is always worked by the minimum switching frequency which is determined by maximum OFF time t_{OFF_MAX2} and minimum ON time t_{ON_MIN} at light loads.
Because power supply supplies minimum power P_{O_MIN} by this minimum switching frequency, output voltage raises when secondary power is lighter than P_{O_MIN}. P_{O_MIN} is calculated by below.

$$P_{O\_MIN} = \frac{{V_{IN(MAX)}}^2}{2 \times L_P} \times {t_{ON\_MIN(MAX)}}^2 \times \frac{1}{t_{ON\_MIN(MAX)} + t_{OFF\_MAX2(MIN)}} \quad [W]$$

$$I_{OUT\_MIN} = \frac{P_{O\_MIN}}{V_{OUT}}$$ By the equation, I_{OUT_MIN} can be also calculated.

When the raise of secondary output voltage is unacceptable, it needs to connect zener diode to secondary output. It operates output voltage suppression less than zener diode voltage.
And it can prevent to rise output voltage by losses which is occurred to connect resistors to secondary output. The secondary output resistor R_{OUT} is less than below equation is needed. Secondary resistor loss P_{LOSS} is calculated by the equation.

$$P_{LOSS} = \frac{{V_{OUT}}^2}{R_{OUT}} \quad [W]$$

$$R_{OUT} \leq \frac{{V_{OUT}}^2}{P_{O\_MIN}} = \frac{{V_{OUT}}^2}{\frac{{V_{IN(MAX)}}^2}{2 \times L_P} \times {t_{ON\_MIN(MAX)}}^2 \times \frac{1}{t_{ON\_MIN(MAX)} + t_{OFF\_MAX2(MIN)}}} \quad [\Omega]$$

In fact, even if the R_{OUT} load calculated by the above formula is used, the output voltage will rise transiently during secondary side discharge. For that, R_{OUT} should be set low enough. R_{OUT} needs to adjust through evaluation. R_{OUT} resistor is needed to notice power dissipation.
The reason of output voltage raise refers to Application Examples: “10.The Influence on Frequency and Output Voltage for Each Load”.

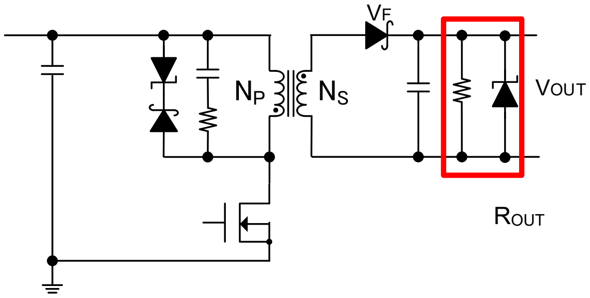


Figure 48. Zener Diode and Resistor to Secondary Output

Application Examples – continued

7 Snubber Circuit

When the combination degree of transformer is low or large current line of board is long, the large surge voltage may be occurred in the SW pin at turn OFF timing of MOSFET. Preventing it, the snubber circuit shown in Figure 49 is used. This snubber circuit clamps flyback voltage + surge voltage when the voltage exceeds snubber voltage.

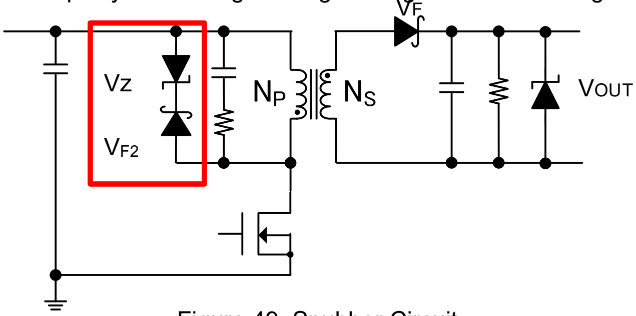


Figure 49. Snubber Circuit

The clamp voltage is determined the following equation.

$$V_{CLAMP} = V_{F2} + V_z \qquad [V]$$

where:

V_{CLAMP} is the clamp setting voltage of snubber circuit.
V_{F2} is the forward voltage of SBD.
V_z is the zener diode voltage.

When the clamp setting voltage is lower than flyback voltage (equal to $\frac{N_P}{N_S} \times (V_{OUT} + V_F)$), large current flows to Zener diode in the turn OFF. Therefore, the snubber voltage (V_{CLAMP}) must be higher than flyback voltage.
When snubber circuit is slow response, it may not clamp setting voltage.
So, SW voltage must be evaluated.

8 Setting of SDX/EN Pin Resistor

8.1 Setting of Enable Voltage

It can set enable voltage V_{IN_ENABLE} by following equation after releasing VIN UVLO.

$$V_{IN\_ENABLE} = V_{EN1} \times \frac{R_1 + (R_2 // R_{SDX/EN})}{R_2 // R_{SDX/EN}} \qquad [V]$$

where:

V_{IN_ENABLE} is the target VIN operating start voltage.
V_{EN1} is the enable voltage 1.
$R_2 // R_{SDX/EN}$ is the divided resistor between R_2 and $R_{SDX/EN}$ which is IC internal resistor.

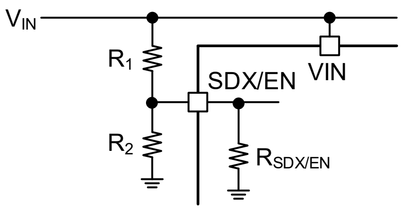


Figure 50. Resistors Connected to the SDX/EN Pin

8.2 Setting of Disabled Voltage

It can set disable voltage $V_{IN\_DISABLE}$ at VIN pin voltage falling by following equation.

$$V_{IN\_DISABLE} = V_{EN2} \times \frac{R_1 + (R_2 // R_{SDX/EN})}{R_2 // R_{SDX/EN}} \qquad [V]$$

where:

$V_{IN\_DISABLE}$ is the target VIN operating stop voltage.
V_{EN2} is the enable voltage 2.

Application Examples – continued

9 The Output Voltage Compensation Function by L_COMP Pin Resistor

This IC is built in output voltage compensation function which is prevented that output voltage V_{OUT} decrease when primary transformer peak current (I_P) increase. The cause of the drop of V_{OUT} are the forward voltage change of secondary diode and transformer leakage etc.
The example of output voltage compensation is shown in Figure 51.

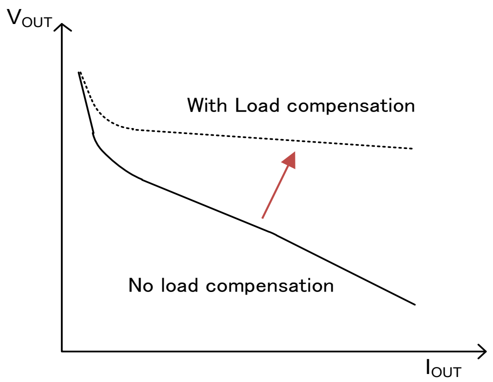


Figure 51. L_COMP Pin Voltage Compensation Example

This function compensates the output voltage by increasing $I_{REFCOMP}$ current to the REF current that determines the output voltage.

$$V_{OUT} = R_{FB} \times \frac{N_S}{N_P} \times \left(\frac{V_{INTREF}}{R_{REF}} + I_{REFCOMP}\right) - V_F \quad \text{[V]}$$

REF current $\frac{V_{INTREF}}{R_{REF}}$ is fiexed to 200 µA (Typ). $I_{REFCOMP}$ is increased for primary current increasing. As the result, output voltage is compensated by output current on the secondary side.
$I_{REFCOMP}$ is calculated to below.

$$I_{REFCOMP} = R_{L\_COMP} \times K_{L\_COMP} \times I_{SW(AVE)} \quad \text{[µA]}$$

where:
R_{L_COMP} is the resistor connected to the L_COMP pin.
$I_{SW(AVE)}$ is the averaging current flown to the SW pin.
K_{L_COMP} is the fixed value determined by IC.

Averaging current $I_{SW(AVE)}$ of the SW pin can be converted below.

$$I_{SW(AVE)} = I_{S(AVE)} \times \frac{N_S}{N_P} = I_{OUT} \times \frac{1}{\eta} \times \frac{N_S}{N_P} \quad \text{[A]}$$

where:
η is the efficiency (It recommends 70 % in design. And adjust R_{L_COMP} in application evaluation.).

Because $I_{SW(AVE)}$ is proportional to I_{OUT} as shown in the above equation, it enables to compensate output voltage. The compensation degree can adjust by resistor value of the L_COMP pin.
Because I_{SW} is triangle wave current, connect the capacitor 0.1 µF or more at the L_COMP pin to flatten it.

The resistor value of the L_COMP pin is calculated by the following equation.

$$R_{L\_COMP} = \frac{I_{REFCOMP}}{I_{SW(AVE)}} \times \frac{1}{K_{L\_COMP}} \quad \text{[kΩ]}$$

Be sure to evaluate the output voltage characteristics in the application and adjust L_COMP resistance as necessary.
And, if the function is no use, the L_COMP pin is needed to connect to AGND.

Application Examples – continued

10 The Influence on Frequency and Output Voltage for Each Load

This IC enables high efficiency to be lower switching frequency in light load. In CCM operation, the switching frequency is f_{SW} for a constant load. When the load is light, the operation is changed from CCM operation to DCM operation. Then, switching frequency is reduced from f_{SW}.
The load current $I_{OUT\_}f_{SW1}$ is calculated below.

$$I_{OUT\_}f_{SW1} = \frac{1}{2} \times \frac{(V_{IN} \times Duty)^2}{L_P \times f_{SW} \times V_{OUT}} \times \eta \qquad \text{[A]}$$

where:
$I_{OUT\_}f_{SW1}$ is the switched load current from DCM to CCM.
f_{SW} is the switching frequency.
V_{IN} is the VIN pin voltage.
L_P is the primary inductance.
V_{OUT} is the output voltage.
η is the efficiency.

As the load is further lightened, the ON time and OFF time decreases. ON time is operated by t_{ON_MIN}.
The load current operated by t_{ON_MIN} is below.

$$I_{OUT\_}f_{SW2} = \frac{1}{2} \times \frac{f_{SW} \times (V_{IN} \times t_{ON\_MIN})^2}{L_P \times V_{OUT}} \times \eta \qquad \text{[A]}$$

where:
$I_{OUT\_}f_{SW2}$ is the load current operated by minimum ON time.
t_{ON_MIN} is the minimum ON time.

As the load is further lightened, the ON time is not shorter than the t_{ON_MIN} and the OFF time is longer.
Because IC is determined maximum OFF time t_{OFF_MAX2},
f_{SW_MIN} is calculated to below.

$$f_{SW\_MIN} = \frac{1}{t_{ON\_MIN} + t_{OFF\_MAX2}} \qquad \text{[kHz]}$$

where:
f_{SW_MIN} is the minimum switching frequency.
t_{OFF_MAX2} is the maximum OFF time 2.

Therefore, constant output power is generated by f_{SW_MIN} operation in no load or light load.
For that, output voltage raises in no load or light load.
And the IC builds in frequency spectrum spread function for EMI improvement. For that, the switching frequency is changed within a constant rate. An output voltage ripple which is dependent on spectrum spread occurs by the function.

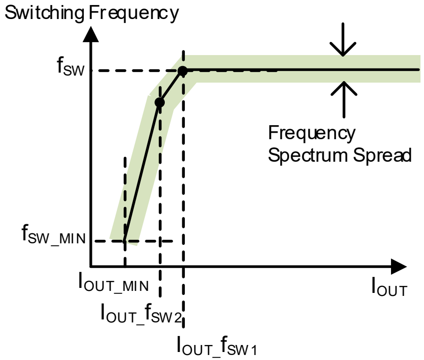
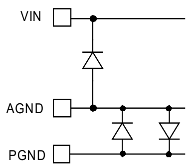
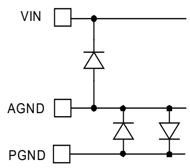
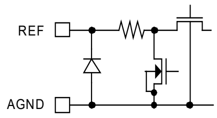
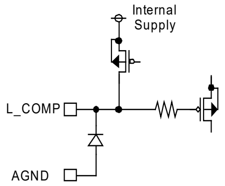
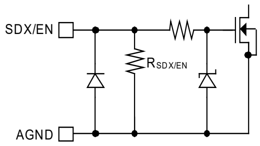
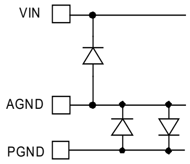
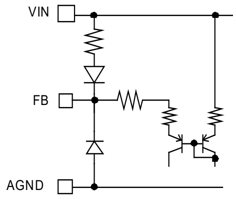
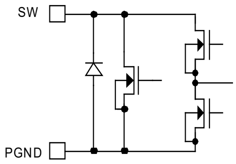
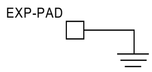


Figure 52. Switching Frequency

I/O Equivalence Circuits

2,3,4,5	PGND	6	AGND	7	REF	9	L_COMP	10	SDX/EN
									
12	VIN	14	FB	16,17,18,19	SW	-	EXP-PAD	1,8,11,13, 15,20	N.C.
								Non Connection	

(Note) N.C pin is not connected to internal.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

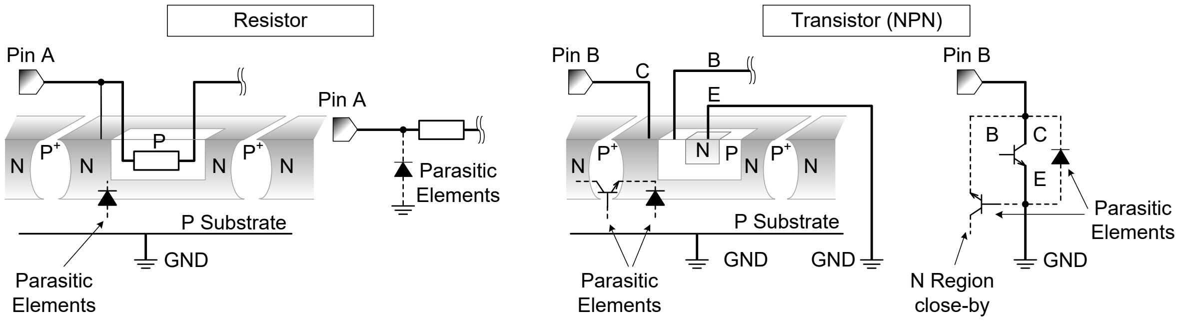


Figure 53. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B D 7 F 3 0 6 E F V - C E 2

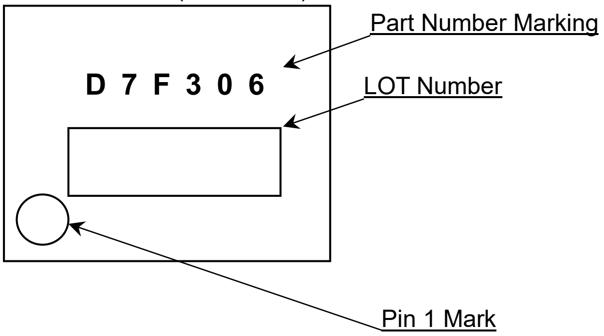
Package
EFV: HTSSOP-B20

Product Class
C: for automotive

Packaging and forming specification
E2: Embossed tape and reel

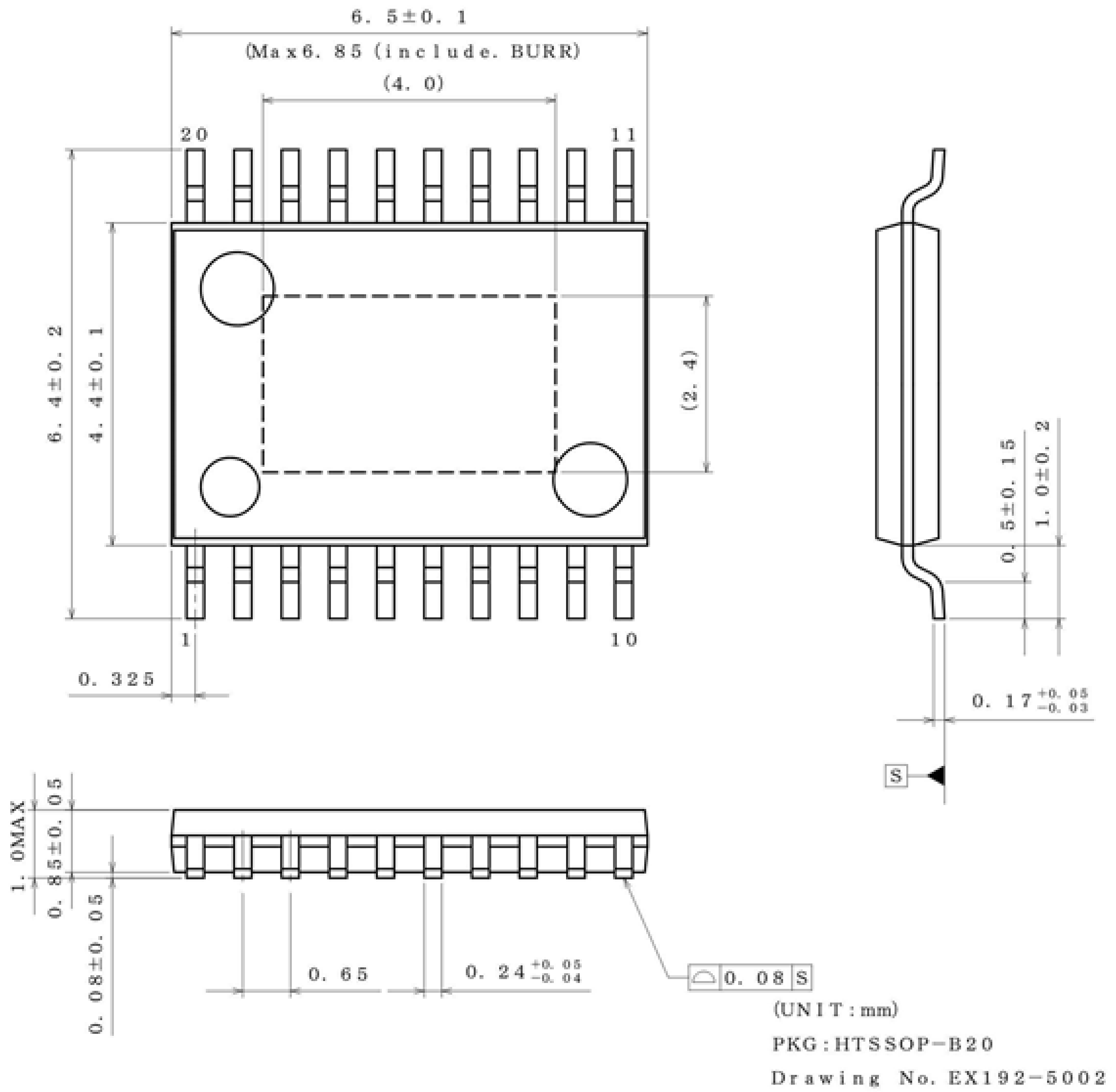
Marking Diagram

HTSSOP-B20 (TOP VIEW)



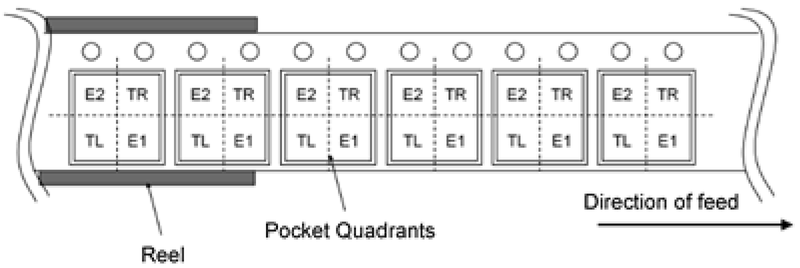
Physical Dimension and Packing Information

Package Name	HTSSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
24.Jan.2025	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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