AC/DC Converter IC

Asymmetric Half Bridge Converter IC

BM1AH001FV-LB

General Description

This is the product guarantees long time support in industrial market. BM1AH001FV-LB is an asymmetric half bridge AC/DC converter that provides an optimum system for all products which has an electrical outlet. Resonant operation enables soft switching and helps to keep the EMI low. The burst operation reduces power consumption at light load. BM1AH001FV-LB includes various protection functions, such as soft start function, burst operation function, over current protection, over voltage protection, overload protection.

Features

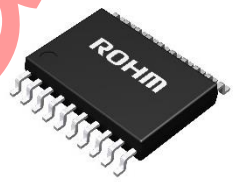
- Long Time Support Product for Industrial Applications
- Wide Operating Range for VCC Pin Voltage
- ZVS Operation for Low EMI and High Efficiency
- Bottom Skip Control
- Burst Operation at Light Load
- Soft Start Function
- VCC UVLO Protection
- AC UVLO Protection
- VS UVLO Protection
- X-Capacitor Discharge Function

Key Specifications

- Power Supply Voltage Range:
  VCC: 9.2 V to 120 V
- VCC Operating Current: 700 µA (Typ)
- VCC Quiescent Current: 500 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

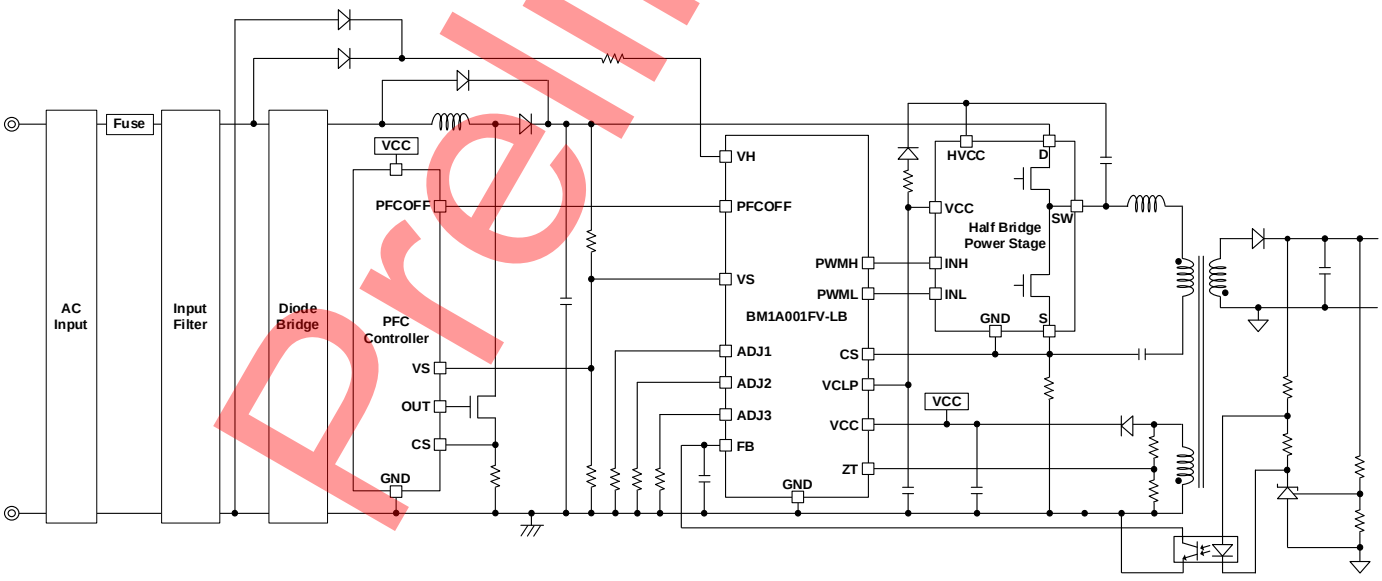
Package	W (Typ) x D (Typ) x H (Max)
SSOP-B20	6.5 mm x 6.4 mm x 1.45 mm pitch 0.65 mm



Applications

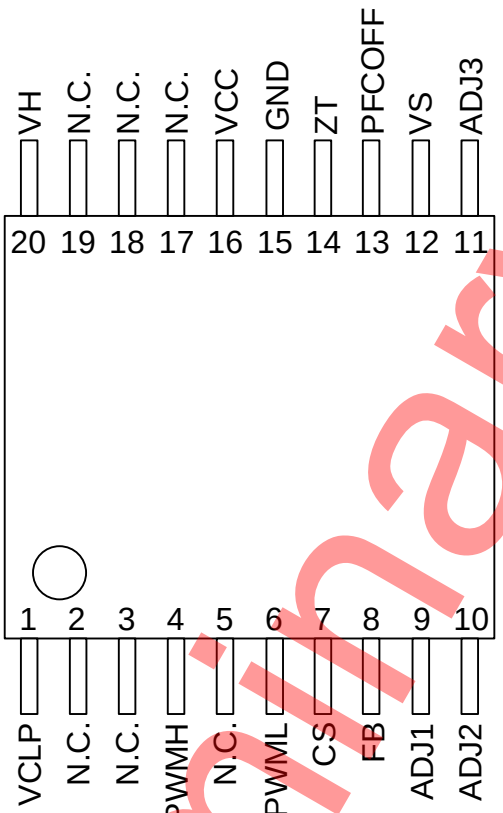
Industrial Equipment, Ultra High Density SMPS, USBPD Adaptor, etc.

Typical Application Circuit



Pin Configuration

(Top View)

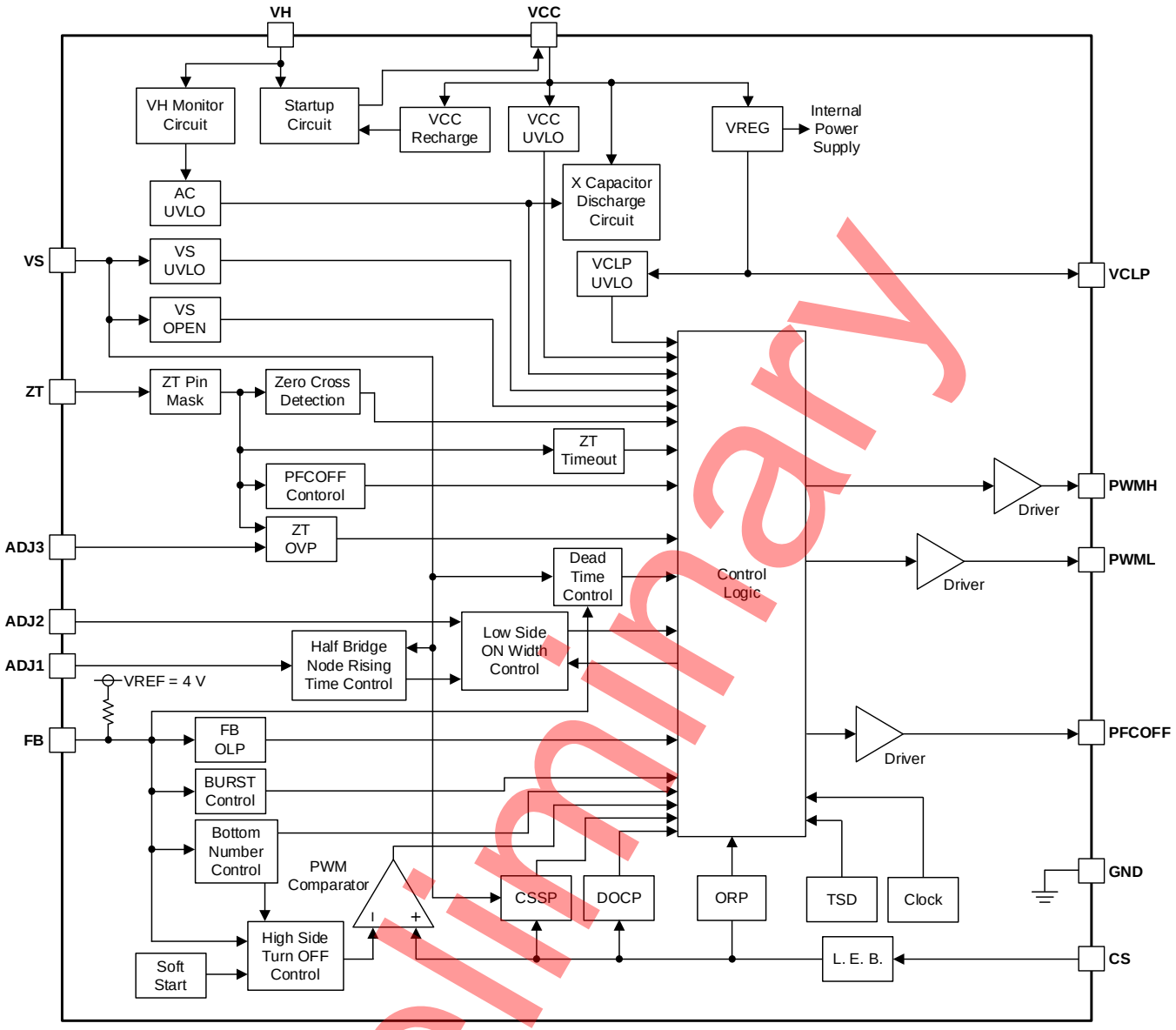


Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	VCLP	O	Clamped power supply output pin
2-3, 5, 17-19	N.C.	-	Non-connection*(Note 1)*
4	PWMH	O	High side PWM output pin
6	PWML	O	Low side PWM output pin
7	CS	I	Current sense pin
8	FB	I	Feedback signal pin
9	ADJ1	I	Parameter adjustment pin 1
10	ADJ2	I	Parameter adjustment pin 2
11	ADJ3	I	Parameter adjustment pin 3
12	VS	I	Bulk voltage sense pin
13	PFCOFF	O	PFCOFF signal output pin
14	ZT	I	Zero current detection pin
15	GND	O	Ground pin
16	VCC	I	Power supply input pin
20	VH	I	Starter circuit input pin

(Note1) Do not connect to other pins.

Block Diagram



Description of Blocks

1 Startup Circuit

This IC has a built-in start-up circuit. It achieves low standby power and high-speed startup.
When AC input voltage is applied, the start-up current is charged to VCC pin from VH pin though the startup circuit.
The charge is stopped after the VCC pin voltage rises and VCC UVLO is released.

1.1 AC Under Voltage Lockout (AC UVLO)

The AC voltage occurs at VH pin when input power supply is applied.
The switching operation does not start until the peak voltage of VH pin becomes more than V_{ACUVLO} after VCC pin voltage is charged to more than V_{UVLO1} through the start-up circuit. When VH pin peak voltage is more than V_{ACUVLO}, AC UVLO is released, and IC starts switching. If input power supply is stopped, VH pin peak voltage becomes lower than V_{ACUVLO} for t_{ACUVLO}, the AC UVLO is detected, and IC stops switching.

1.2 X Capacitor Discharge Function

When the AC voltage is not detected any more for t_{ACUVLO} (such as the plug is pulled out), X capacitor discharge function starts to operate. X capacitor is discharged to GND through start-up circuit.

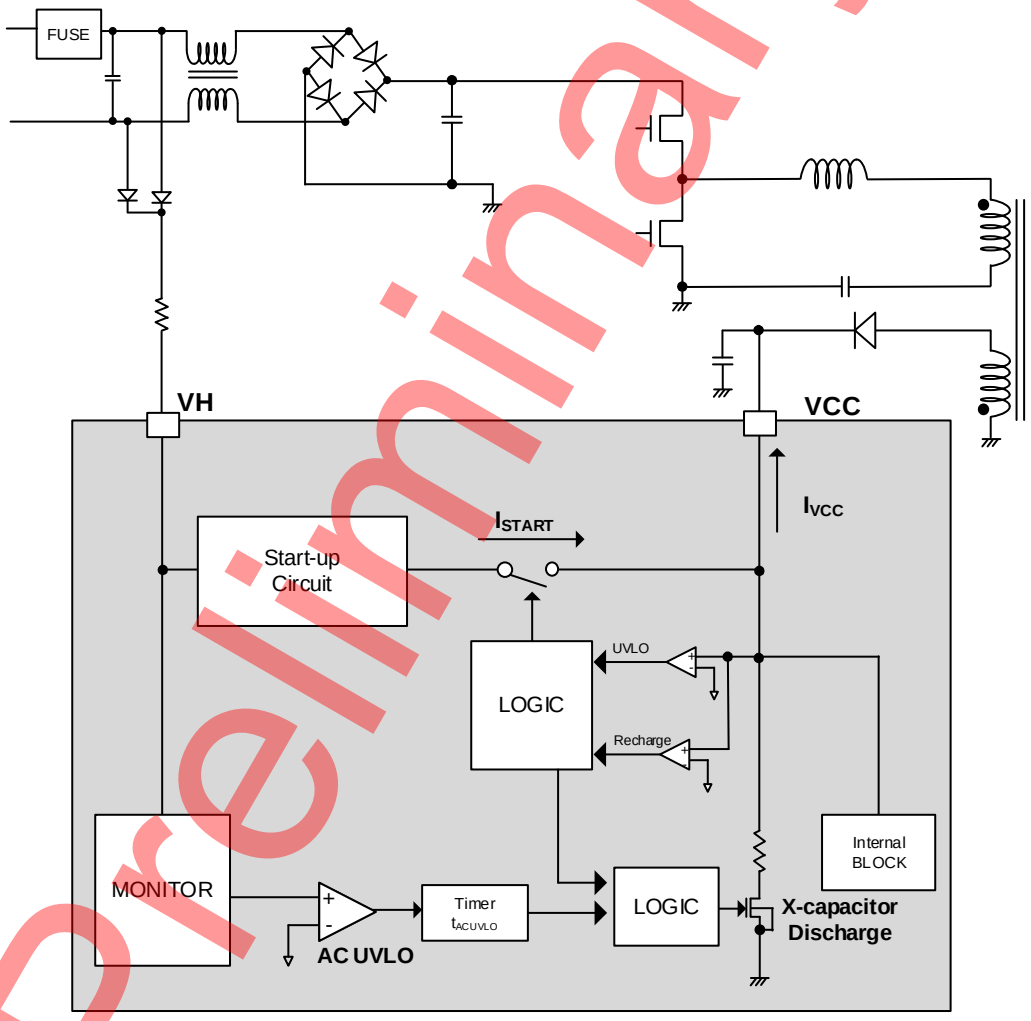


Figure 1. Block Diagram of VH Pin and VCC Pin

1.2 X Capacitor Discharge Function – continued

The timing chart of the X capacitor discharge operation is shown in figure 2.

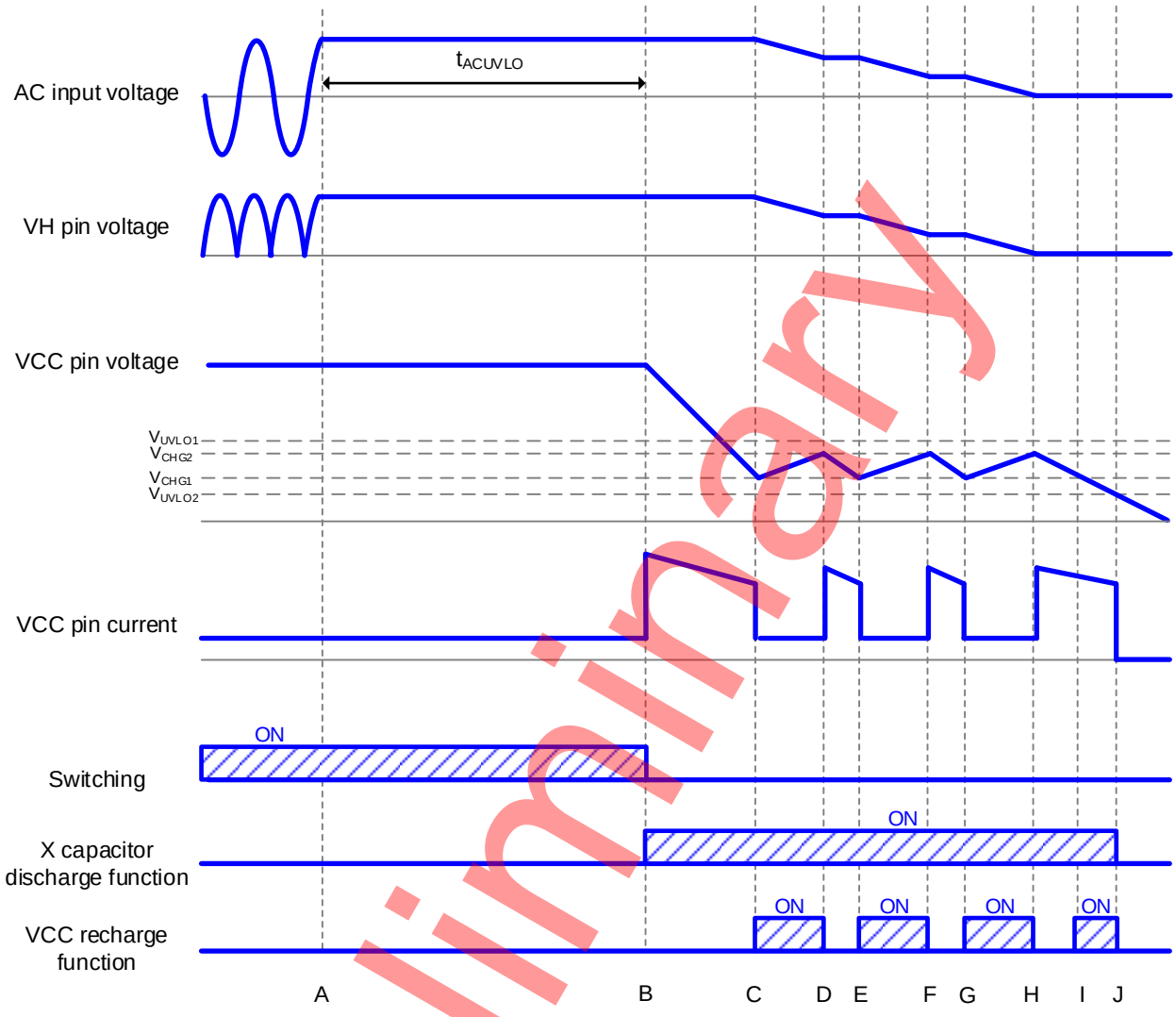


Figure 2. Timing Chart of X Capacitor Discharge Function

A: AC input voltage is turned OFF.
B: After t_{ACUVLO} from A, the switching stops and the X capacitor discharge function operates.
C: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge operation starts.
D: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge operation stops.
E: Same as C.
F: Same as D.
G: Same as C.
H: Same as D.
I: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low VH pin voltage.
J: When the VCC pin voltage becomes less than V_{UVLO2}, VCC UVLO operates.

Description of Blocks - continued

2 Startup Sequence

The startup sequence is shown in Figure 3.

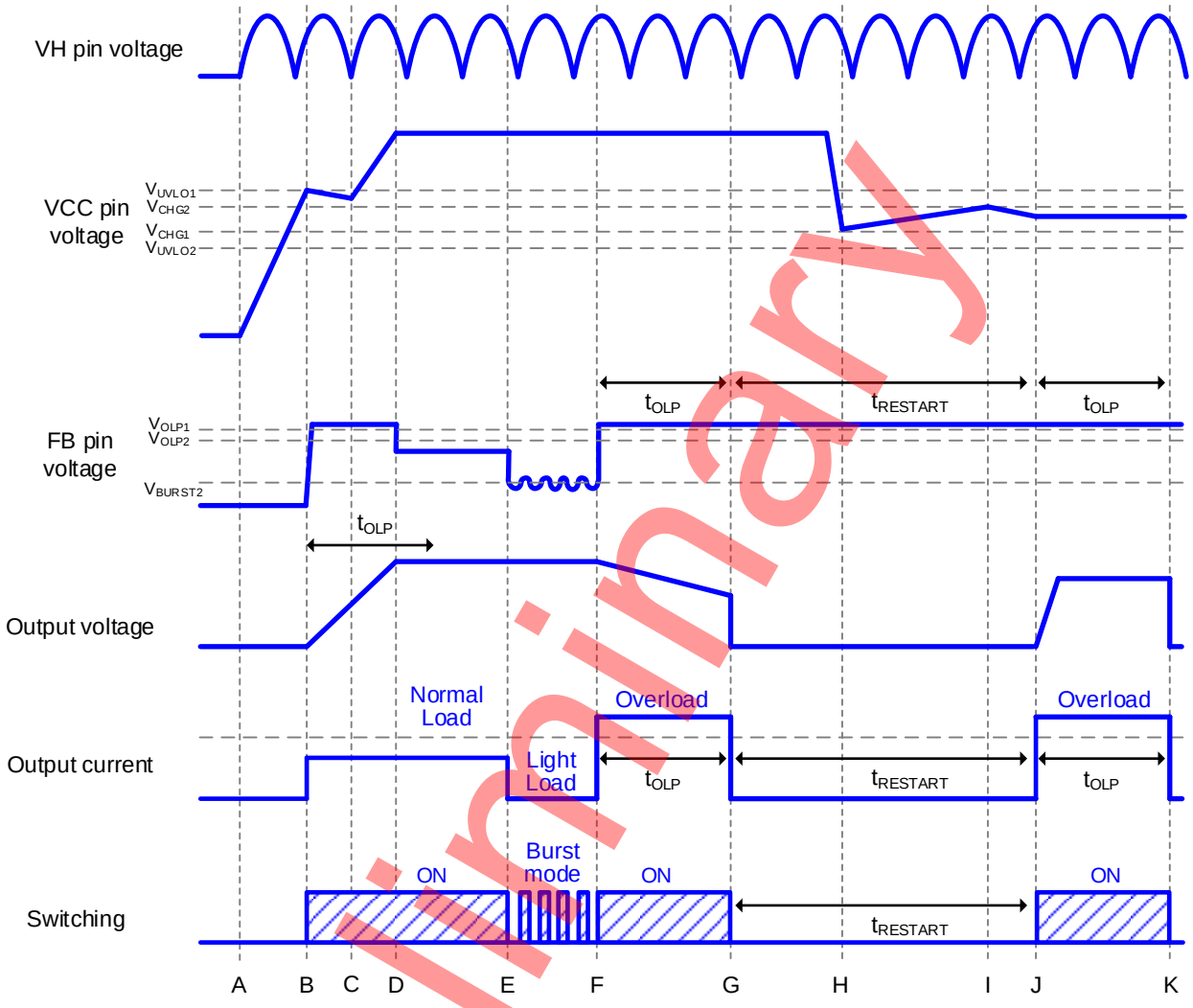


Figure 3. Startup Sequence Timing Chart

A: The VH pin voltage is applied and the VCC pin voltage rises.
B: If the VCC pin voltage becomes more than V_{UVLO1}, the IC starts to operate. And if the IC judges the other protection functions as normal condition, it starts the switching operation. The soft start function limits the over current detection current to prevent overshoot on output voltage and output current rising. When the switching operation starts, the output voltage rises.
C: Until the output voltage becomes a constant value or more from startup, the VCC pin voltage drops by the VCC pin current consumption.
D: It is necessary to set the output capacitor to ensure the output voltage rises to targeted value within t_{OLP}.
E: At light load, the burst operation starts to reduce the power consumption if the FB pin voltage becomes less than V_{BURST2}.
F: When the FB pin voltage becomes more than V_{OLP1}, the IC starts the overload operation.
G: When the condition that the FB pin voltage becomes more than V_{OLP1} for t_{OLP}, the switching stops for $t_{RESTART}$ period by FB OLP. If the FB pin voltage becomes less than V_{OLP2}, FB OLP detect timer (t_{OLP}) is reset.
H: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates.
I: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge function stops operating.
J: After $t_{RESTART}$ period from G, the switching operation restarts by soft start operation.
K: Same as G.

Description of Blocks - continued

3 VCC Pin Protection Function

This IC has the internal protection functions at the VCC pin as shown below.

3.1 VCC Under Voltage Lockout (VCC UVLO)

This is auto restart comparator with a voltage hysteresis.

3.2 VCC Recharge Function

If the VCC pin voltage drops to less than V_{CHG1} after once the VCC pin becomes more than V_{UVLO1} and the IC starts to operate, the VCC recharge function operates. At this time, the VCC pin is recharged from the VH pin through the start-up circuit. When the VCC pin voltage becomes more than V_{CHG2}, this recharge is stopped.

4 VS Pin Protection Function

This IC has the internal protection functions at the VS pin as shown below.

4.1 VS Under Voltage Lockout (VS UVLO)

This is auto restart comparator with a voltage hysteresis.

4.2 VS Open Protection

If the VS pin voltage exceeds V_{SOPEN1} for t_{VSOPEN}, the IC stops switching. If the VS pin voltage falls below V_{SOPEN2}, the IC restarts switching.

5 VCLP Under Voltage Lockout (VCLP UVLO)

This is auto restart comparator with a voltage hysteresis.

6 FB Overload Protection (FB OLP)

The overload protection function operates in auto restart mode. This function monitors the overload status of the secondary output current at the FB pin and stops switching when the overload status is detected. During overload status, current no longer flows to the photo-coupler, so the FB pin voltage rises. When the FB pin voltage keeps being over V_{OLP1} for t_{OLP}, the switching operation is stopped by the overload protection circuit for $t_{RESTART}$. If the FB pin voltage drops to lower than V_{OLP2} within t_{OLP} after once it exceeds V_{OLP1}, the overload protection timer is reset. At startup, the FB pin voltage is pulled up to the internal voltage by a pull-up resistor, so operation starts from V_{OLP1} or above. Therefore, it is necessary for the design to set the FB pin voltage at V_{OLP2} or less within t_{OLP}. In other words, the startup time of the secondary output voltage must be set to within t_{OLP} after the IC starts.

Description of Blocks - continued

7 Control System

The IC uses PFM (Pulse Frequency Modulation) mode control. The FB pin, the ZT pin are monitored to provide an optimized DC/DC system. First, the operation of asymmetric half bridge converter is shown in figure 4 and figure 5.

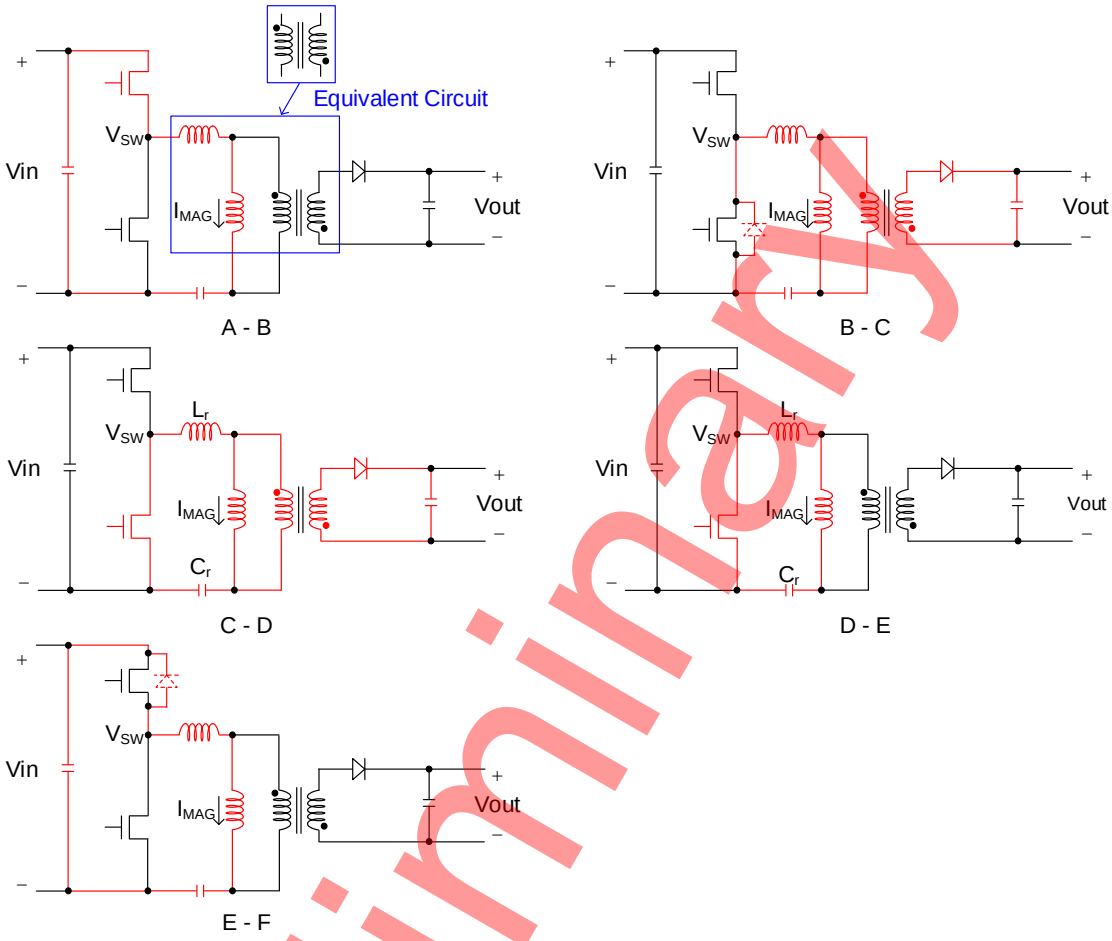


Figure 4. The Operation of Asymmetric Half Bridge Converter

7 Control System - continued

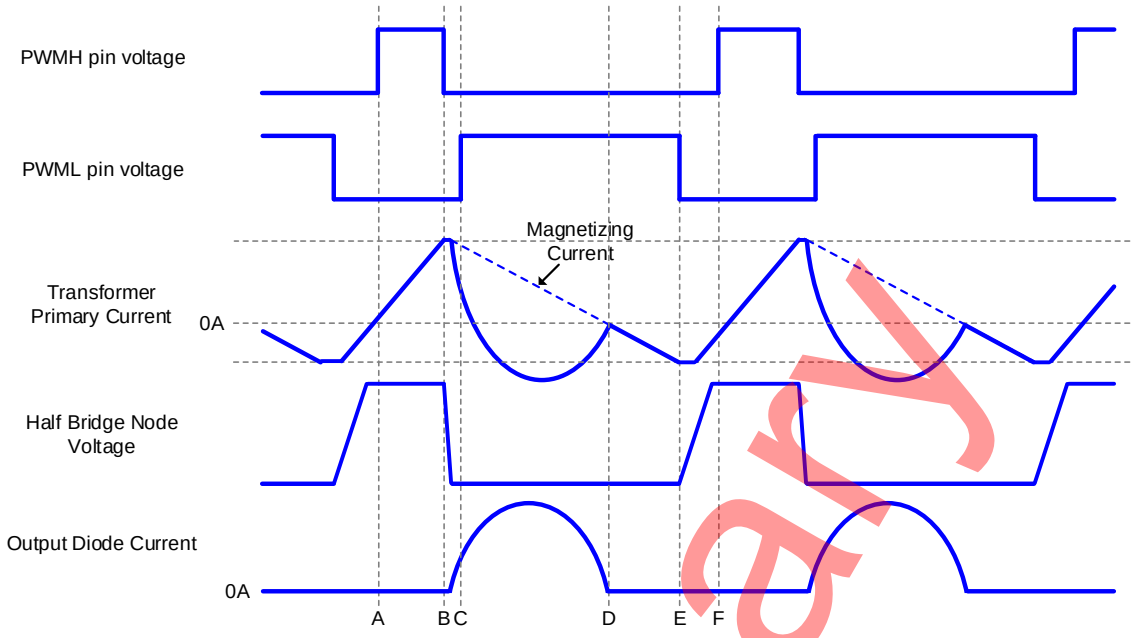


Figure 5. The Waveform of Asymmetric Half Bridge Converter

A - B: The high Side power switch is turned on and the magnetizing current I_{MAG} changes in a positive direction. The output diode is biased inversely blocking any energy transfer to the secondary side.

B - C: The high side power switch is turned off and the half bridge node voltage V_{SW} falls until the low side power switch starts to conduct reversely due to positive I_{MAG}. I_{MAG} changes in a negative direction. The output diode starts to conduct.

C - D: Zero voltage switching is achieved by turning on the low side power switch after the low side power switch conducts reversely. The output diode current is resonated with the leakage inductance of primary side transformer Lr and the resonant capacitor Cr.

D - E: The output diode is biased inversely blocking any energy transfer to the secondary side after the resonance. The low side power switch continues to be turned on until I_{MAG} becomes negative.

E - F: The low side power switch is turned off and the half bridge node voltage V_{SW} rises until the high side power switch starts to conduct reversely due to negative I_{MAG}. Zero voltage switching is achieved by turning on the high side power switch after the high side power switch conducts reversely.

7 Control System - continued

7.1 Control Mode

This IC operates in three control modes.

7.1.1 ZVS Mode

In ZVS mode, the low side ON width is determined by monitoring from the time when the PWML pin voltage outputs turn OFF signal to the time when the ZT pin voltage falls below V_{ZT2}. The detailed sequence is shown in figure 6.

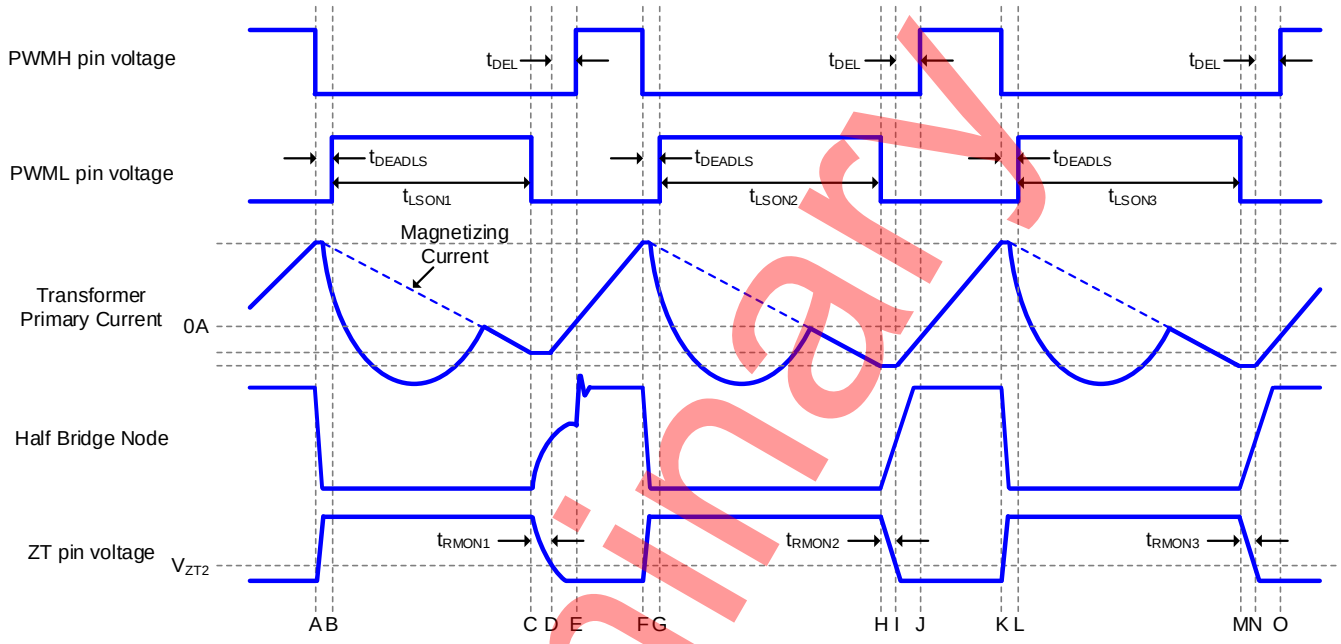


Figure 6. The Determination of The Low Side ON Width in ZVS Mode

A: The PWMH pin outputs turn OFF signal. The high side turn OFF timing is controlled by the FB pin and the CS pin.
B: After t_{DEADLS} from the PWMH pin outputs turn OFF signal, the PWML pin outputs turn ON signal.
C: After t_{LSON1} from the PWML pin outputs turn ON signal, the PWML pin outputs turn OFF signal.
D: The time between when the PWML pin outputs turn OFF signal and the ZT pin voltage falls below V_{ZT2} is monitored. The time from C to D is defined as t_{RMON1}. If t_{RMON1} is shorter than t_{RTAR}, the low side ON width of the next cycle becomes longer than t_{LSON1}. On the other hand, if t_{RMON1} is longer than t_{RTAR}, the low side ON width of the next cycle becomes shorter than t_{LSON1}.
E: After t_{DEL} from the ZT pin voltage falls below V_{ZT2}, the PWMH pin outputs turn ON signal. If t_{RMON1} is not enough, it may not be fully zero volt switching.
F: Same as A.
G: Same as B.
H: After t_{LSON2} from the PWML pin outputs turn ON signal, the PWML pin outputs turn OFF signal. t_{LSON2} is determined depending on t_{RMON1} in the previous cycle.
I: The time between when the PWML pin outputs turn OFF signal and the ZT pin voltage falls below V_{ZT2} is monitored. The time from H to I is defined as t_{RMON2}. If t_{RMON2} is same as t_{RTAR}, the low side ON width of the next cycle becomes same as t_{LSON2}.
J: After t_{DEL} from the ZT pin voltage falls below V_{ZT2}, the PWMH pin outputs turn ON signal. If t_{RMON2} is enough, it can be fully zero voltage switching.
K: Same as F.
L: Same as G.
M: After t_{LSON3} from the PWML pin outputs turn ON signal, the PWML pin outputs turn OFF signal. t_{LSON3} is determined depending on t_{RMON2} in the previous cycle.
N: The time between when the PWML pin outputs turn OFF signal and the ZT pin voltage falls below V_{ZT2} is monitored. The time from M to N is defined as t_{RMON3}. If t_{RMON3} is same as t_{RTAR}, the low side ON width of the next cycle becomes same as t_{LSON3}.
O: Same as J.

Also, the low side ON width cannot be smaller than the minimum ON width $t_{LSONMIN}$.

7.2.1 ZVS Mode - continued

The rising time of half bridge node is monitored by ZT pin voltage. The time between when the PWML pin outputs turn OFF signal and the ZT pin voltage falls below V_{ZT2} is monitored. This time is defined as t_{RMON}. To minimize unnecessary power loss, t_{RMON} is controlled to converge to the target time t_{RTAR}. t_{RTAR} varies depending on the VS pin voltage. The relationship between t_{RTAR} and the VS pin voltage is shown in figure 7. Also, t_{RTAR1} is adjustable by the ADJ1 pin pull-down resistance R_{ADJ1}. The relationship between t_{RTAR} and R_{ADJ1} is shown in table 1.

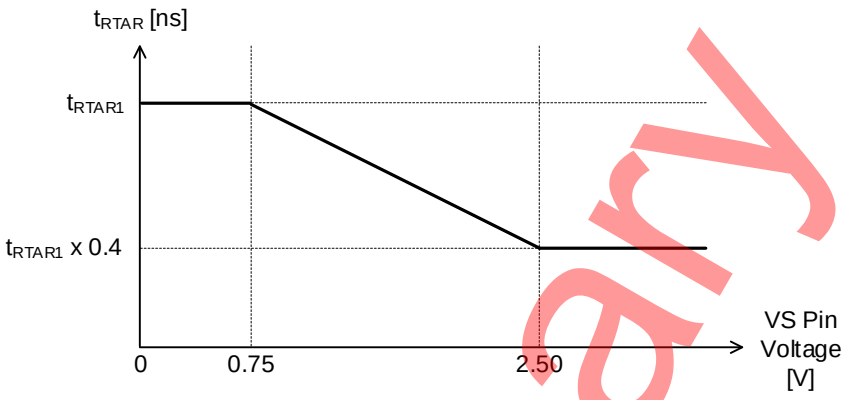


Figure 7. The Relationship between t_{RTAR} and The VS Pin Voltage

Table 1. The Relationship between t_{RTAR1} and R_{ADJ1}

R_{ADJ1} [kΩ]	t_{RTAR1} [ns]
0	t_{RTAR11}
47	t_{RTAR12}
100	t_{RTAR13}
220	t_{RTAR14}
OPEN	t_{RTAR15}

9.2 Control Mode - continued

7.2.2 Bottom Skip Mode

In bottom skip mode, the low side ON width is fixed to $t_{LSONMIN}$. The detailed sequence when the number of bottoms is three is shown in figure 8.

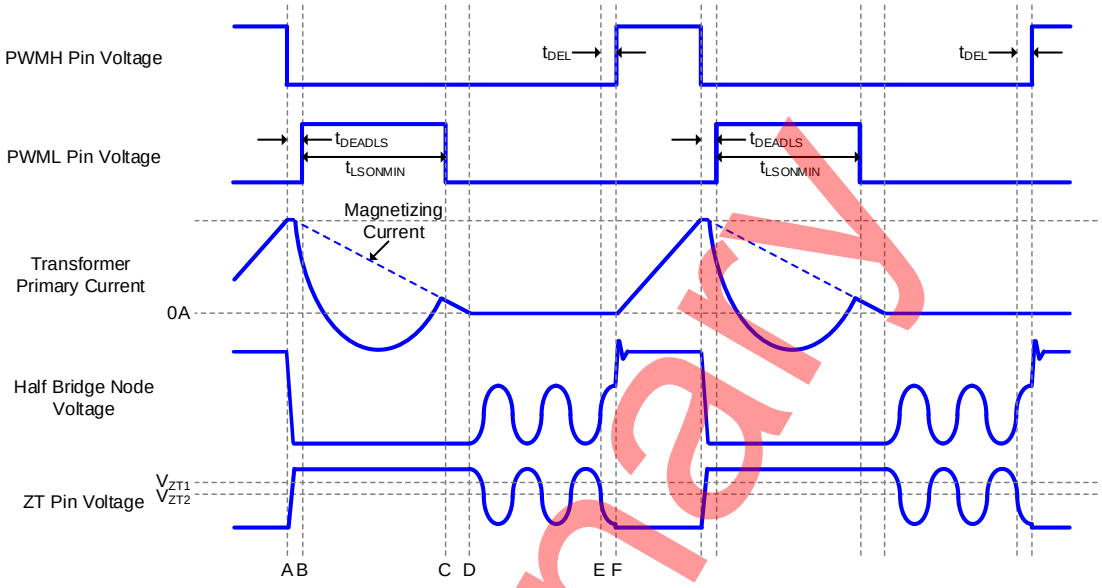


Figure 8. The Sequence in Bottom Skip Mode (The Number of Bottoms is Three.)

A: The PWMH pin outputs turn OFF signal. The high side turn OFF timing is controlled by the FB pin and the CS pin.
B: After t_{DEADLS} from the PWMH pin outputs turn OFF signal, the PWML pin outputs turn ON signal.
C: After t_{LSON1} from the PWML pin outputs turn ON signal, the PWML pin outputs turn OFF signal.
D: When the magnetizing current of the transformer reaches zero, the half bridge node voltage starts to resonate. The number of resonances at half bridge node voltage is counted when the ZT pin voltage exceeds V_{ZT1}. However, the number of resonances at half bridge node is not counted if the ZT pin voltage does not fall below V_{ZT2} before the ZT pin voltage exceeds V_{ZT1}.
E: The number of resonances at half bridge node is counted N_{BOTTOM} times. As an example, the case where N_{BOTTOM} is three is shown in figure 10.
F: After t_{DEL} from D, the PWMH pin outputs turn ON signal.

$t_{LSONMIN}$ is adjustable by the ADJ2 pin pull-down resistance R_{ADJ2}. The relationship between $t_{LSONMIN}$ and R_{ADJ2} is shown in figure 9.

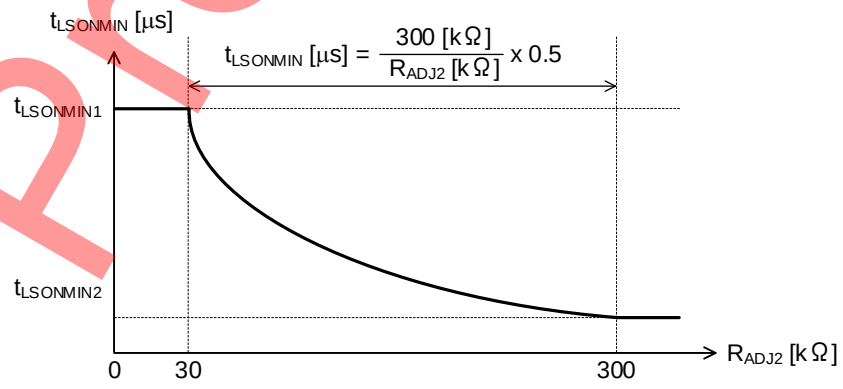


Figure 9. The Relationship between $t_{LSONMIN}$ and The R_{ADJ2}

7.2.2 Bottom Skip Mode - continued

In bottom skip mode, bottom number N_{BOTTOM} is determined by the FB pin voltage. The FB pin threshold voltage of bottom number differs when the FB pin voltage rises (output power increases) and when the FB pin voltage falls (output power decreases). If the switching frequency exceeds f_{SWMIN}, the PWMH pin is forced to output turn ON signal at the next bottom even if the bottom number is not detected N_{BOTTOM} times. The relationship between FB pin voltage and bottom number is shown in table 2. Also, the example of the relationship between output power and switching frequency is shown in figure 10. Bottom number 1 is ZVS mode.

Table 2. The Relationship between FB pin voltage and bottom number

FB pin voltage rises		FB pin voltage falls	
Bottom Number	FB pin voltage	Bottom Number	FB pin voltage
12 to 11	V_{FB1211}	11 to 12	V_{FB1112}
11 to 10	V_{FB1110}	10 to 11	V_{FB1011}
10 to 9	V_{FB109}	9 to 10	V_{FB910}
9 to 8	V_{FB98}	8 to 9	V_{FB89}
8 to 7	V_{FB87}	7 to 8	V_{FB78}
7 to 6	V_{FB76}	6 to 7	V_{FB67}
6 to 5	V_{FB65}	5 to 6	V_{FB56}
5 to 4	V_{FB54}	4 to 5	V_{FB45}
4 to 3	V_{FB43}	3 to 4	V_{FB34}
3 to 2	V_{FB32}	2 to 3	V_{FB23}
2 to 1	V_{FB21}	1 to 2	V_{FB12}

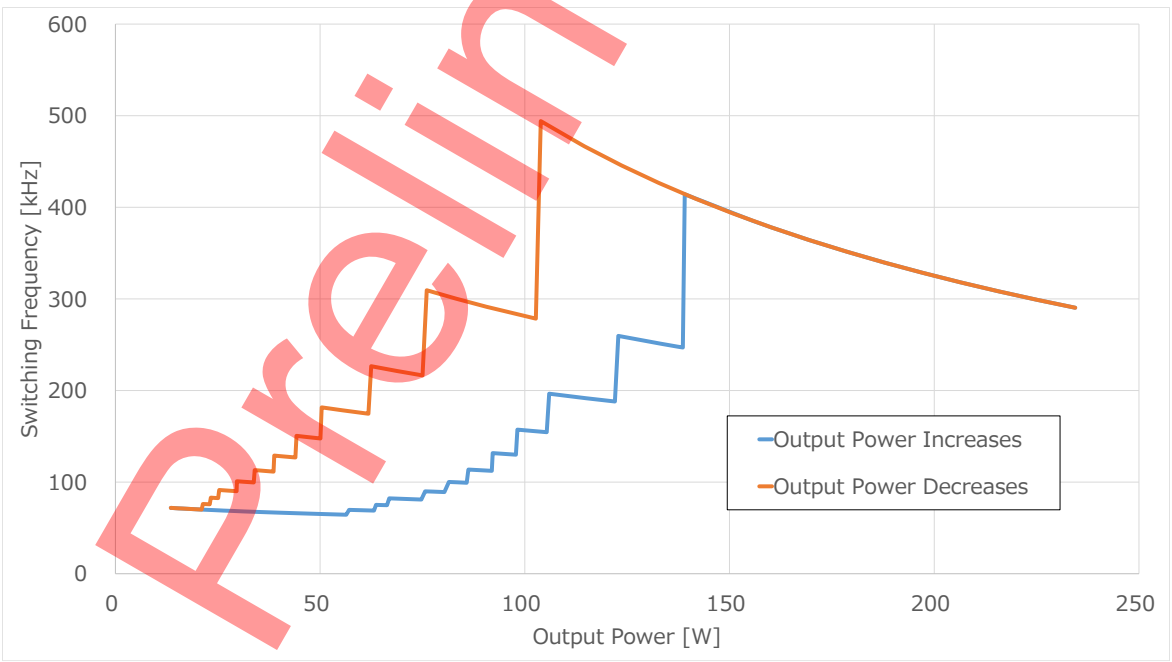


Figure 10. The Example of The Relationship between Output Power and Switching Frequency

7.2 Control Mode - continued

7.2.3 Burst Mode

When the FB pin voltage falls below V_{BURST2}, the IC enters burst mode and stops switching. When the FB pin voltage exceeds V_{BURST1}, the IC exits burst mode and restarts switching. When switching restarts, the PWML pin outputs pre-pulse signal to recharge the high side bootstrap capacitor. The number of the pre-pulses increases by one for every t_{BURST} of burst mode duration. The minimum number of the pre-pulses is two, and the maximum number of the pre-pulses is fifteen. The detailed sequence is shown in figure 11.

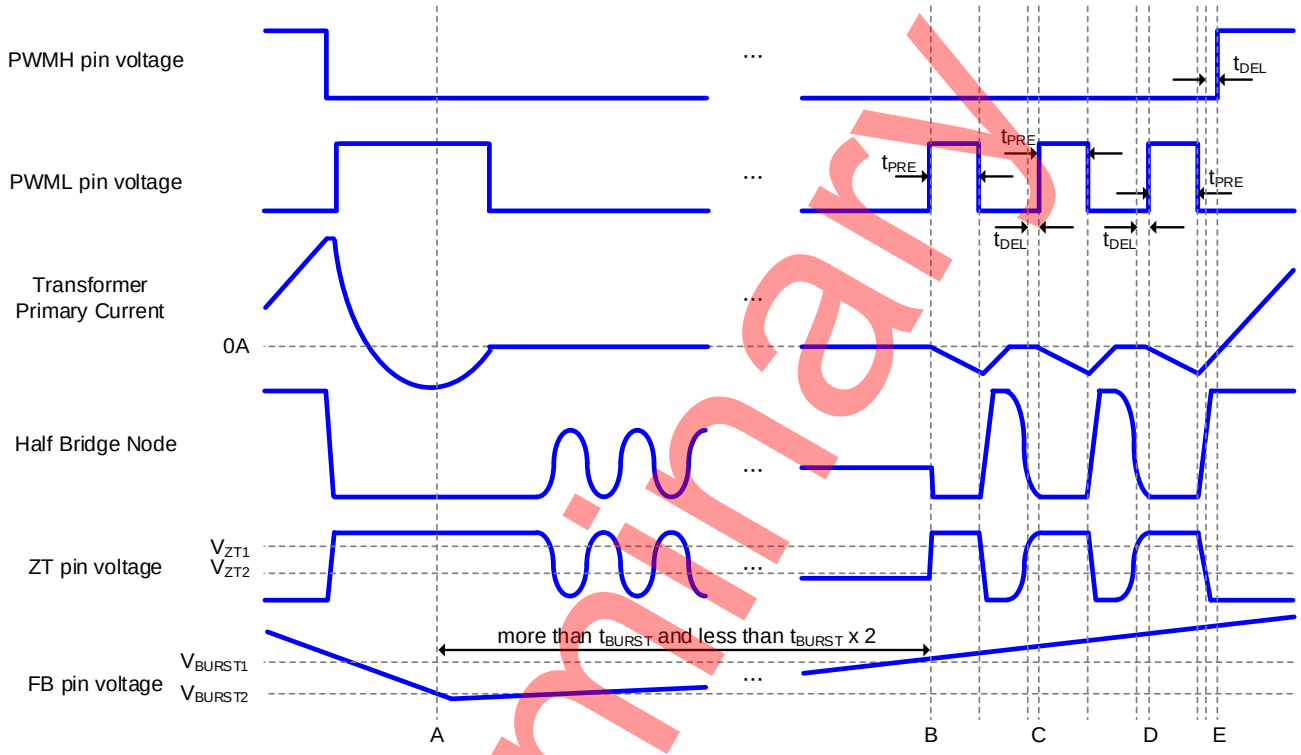


Figure 11. The Sequence of Burst Mode Exiting if The Number of Pre-pulses is three

A: The FB pin falls below V_{BURST2} and switching is stopped from the next cycle.
B: The FB pin exceeds V_{BURST1} and the condition for restarting the switching is satisfied. If the time from A to B is more than t_{BURST} and less than double t_{BURST}, the number of pre-pulses is three. the PWML pin outputs the first pre-pulse signal whose width is t_{PRE}.
C: After t_{DEL} from the ZT pin voltage exceeds V_{ZT1}, the PWML pin outputs the second pre-pulse signal whose width is t_{PRE}.
D: After t_{DEL} from the ZT pin voltage exceeds V_{ZT1}, the PWML pin outputs the third pre-pulse signal whose width is t_{PRE}.
D: After t_{DEL} from the ZT pin voltage falls below V_{ZT2}, the PWMH pin outputs the turn ON signal.

Description of Blocks – continued

8 CS Pin Function

CS pin function is shown in figure 12.

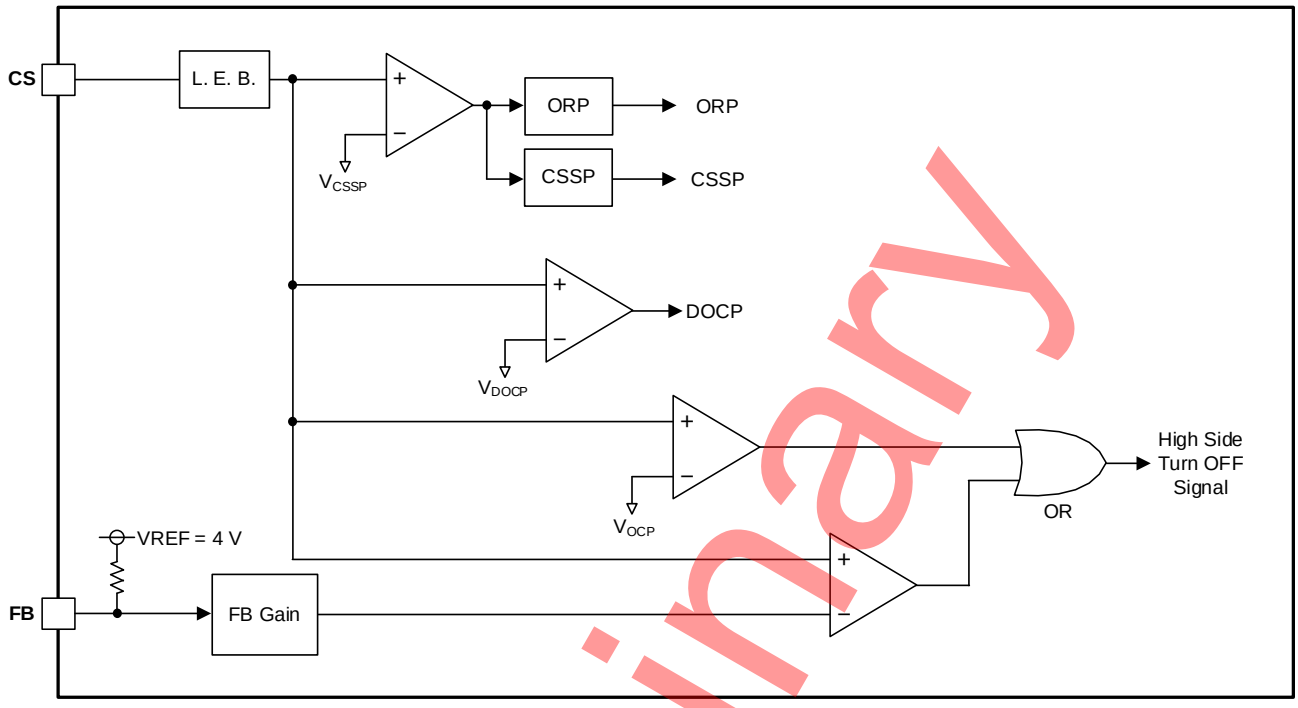


Figure 12. CS Pin Function

8.1 High Side Turn OFF Control

The high side turn OFF timing is controlled by the FB pin and the CS pin. When the CS pin voltage exceeds the FB pin voltage times FB gain, the PWMH pin outputs turn OFF signal. FB gain depends on bottom number. The relationship between FB gain and bottom number is shown in table 3. Also, the high side turn OFF signal is outputted even when CS pin voltage exceeds V_{OCP}.

Table 3. The Relationship between FB gain and bottom number

Bottom Number	FB gain
12	G_{FB12}
11	G_{FB11}
10	G_{FB10}
9	G_{FB9}
8	G_{FB8}
7	G_{FB7}
6	G_{FB6}
5	G_{FB5}
4	G_{FB4}
3	G_{FB3}
2	G_{FB2}
1	G_{FB1}

Description of Blocks – continued

8.2 Dynamic Over Current Protection (DOCP)

When the CS pin voltage exceeds V_{DOCP} in two consecutive switching cycles, the PWMH pin outputs turn OFF signal and the IC stops switching. The IC restarts switching t_{DOCP} after switching stops.

8.3 CS Pin Short Protection (CSSP)

When the CS pin voltage is below V_{CSSP} t_{CSSP} after the PWMH pin starts to output turn ON signal, the PWMH pin outputs turn OFF signal. This protection is auto restarted with pulse by pulse. t_{CSSP} varies depending on the VS pin voltage. The relationship between t_{CSSP} and the VS pin voltage is shown in figure 13.

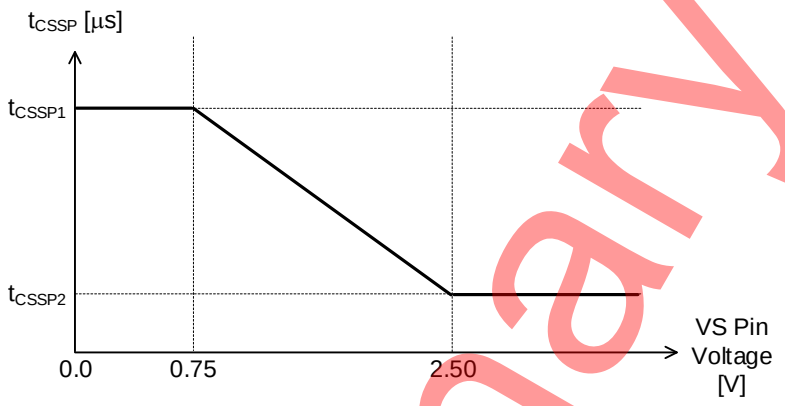


Figure 13. The Relationship between t_{CSSP} and The VS Pin Voltage

8.4 Out of Resonance Protection (ORP)

When the CS pin voltage is below V_{CSSP} t_{ORP} after the PWMH pin starts to output turn ON signal, the IC recognizes the out of resonance, and the PWMH pin outputs turn OFF signal and the IC stops switching. The IC restarts switching t_{ORP} after switching stops.

Description of Blocks - continued

9 ZT Pin Function

9.1 Zero Crossing Detection

The IC has the comparator which detects zero voltage crossing of transformer at the ZT pin voltage. The comparator has hysteresis. The IC detects zero voltage crossing at V_{ZT1} when ZT pin voltage rises, on the other hand, detects zero voltage crossing at V_{ZT2} when ZT pin voltage falls.

9.2 ZT Timeout Function 1

When the output voltage is too low such as at startup or the ZT pin is shorted to ground, the ZT pin voltage does not exceed V_{ZT1} after the PWMH pin outputs turn OFF signal. When the ZT pin voltage does not exceed V_{ZT1} for t_{ZTOUT1}, the PWMH pin is forced to outputs turn ON signal.

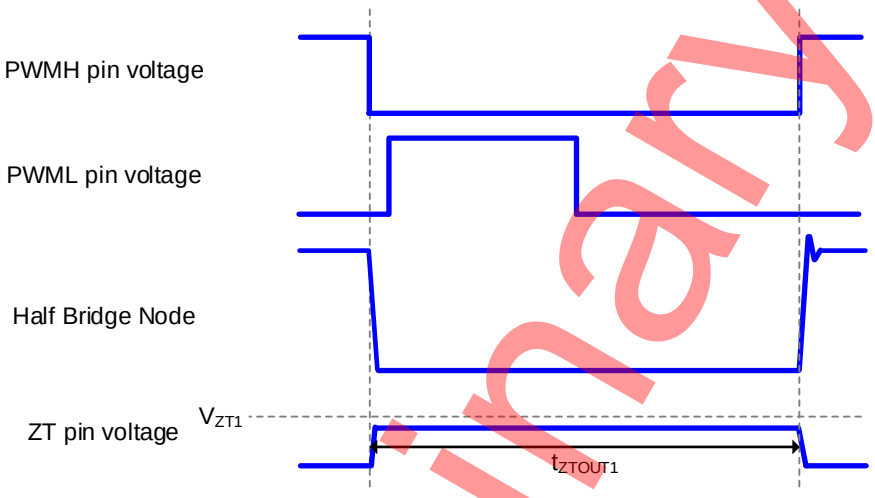


Figure 14. ZT Timeout Function 1

9.3 ZT Timeout Function 2

When the ZT pin voltage does not exceed V_{ZT1} for t_{ZTOUT2} after the ZT pin detects zero voltage crossing at V_{ZT2}, the PWMH pin is forced to outputs turn ON signal.

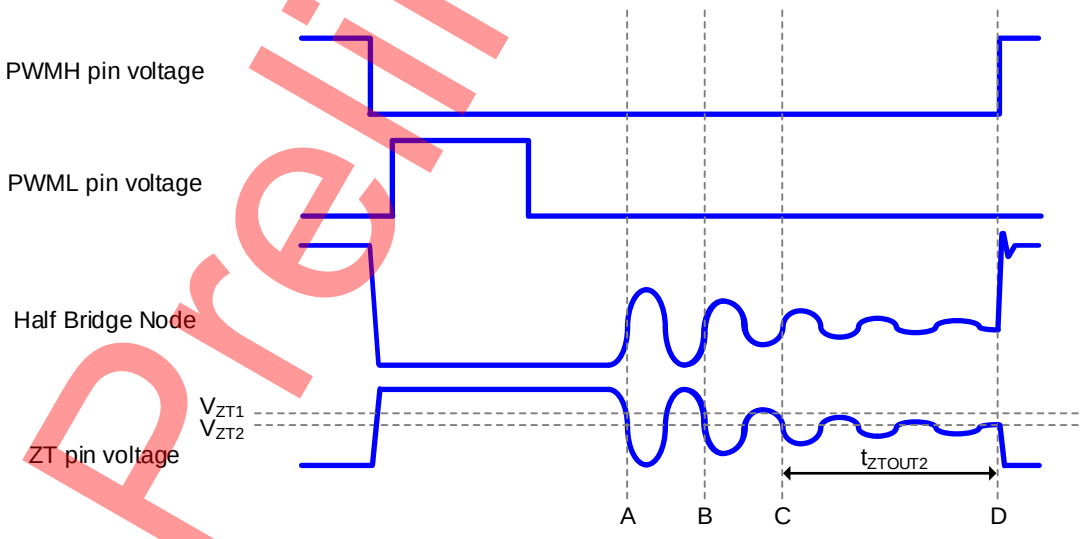


Figure 15. ZT Timeout Function 2

9 ZT Pin Function - continued

9.4 ZT Over Voltage Protection (ZT OVP)

The IC stops switching when the ZT pin voltage exceeds V_{ZTOVP} in three consecutive switching cycles. The IC restarts switching $t_{RESTART}$ after switching stops. V_{ZTOVP} is adjustable by the ADJ3 pin pull-down resistance R_{ADJ3}. The relationship between V_{ZTOVP} and R_{ADJ3} is shown in table 4.

Table 4. The Relationship between V_{ZTOVP} and R_{ADJ3}

R_{ADJ3} [kΩ]	V_{ZTOVP} [V]
0	V_{ZTOVP1}
47	V_{ZTOVP2}
100	V_{ZTOVP3}
OPEN	V_{ZTOVP4}

9.5 ZT Pin Mask Function

To prevent the false detection of the ZT pin voltage, all functions regarding the ZT pin are masked for t_{ZTMASK} after the PWMH pin outputs turn OFF signal.

10 PFCOFF Function

When the ZT pin voltage continues to exceed V_{ZTPFC1} in every switching cycle for t_{PFC}, PFCOFF pin outputs high signal. On the other hand, when the ZT pin voltage continues to not exceed V_{ZTPFC2} in every switching cycle for t_{PFC}, PFCOFF pin outputs low signal.

Description of Blocks - continued

11 Soft Start Function

The IC has a soft start function to prevent the overshoot on output voltage and abnormal current during startup. Soft start function performs the following operation after startup (Figure 16).

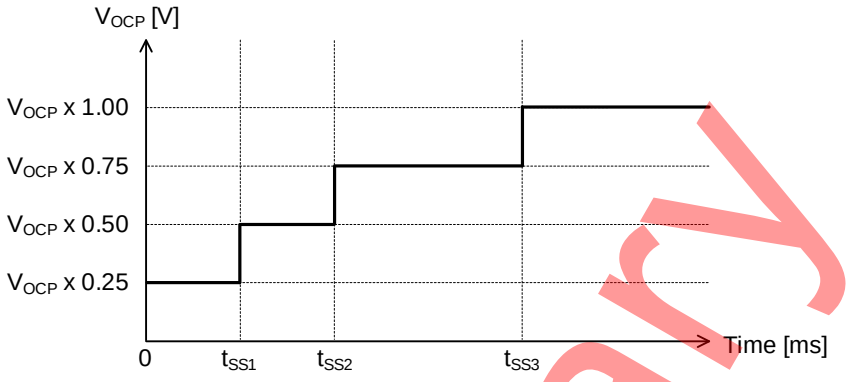


Figure 16. Soft Start Function

12 Bootstrap Capacitor Pre-charge Function

At startup, the PWML pin outputs sixty-four consecutive turn ON pulses for t_{PRE}. The interval between each pulse is t_{START}. After t_{START} from the PWML pin outputs the final pulse, the PWMH pin outputs turn ON signal. The sequence is shown in figure 17.

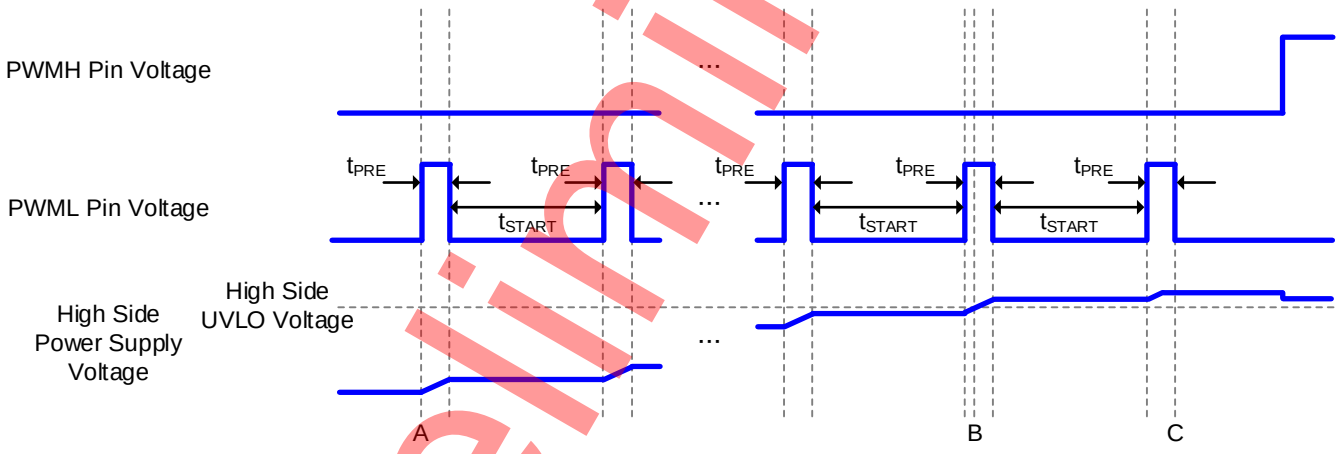


Figure 17. The Sequence of Bootstrap Capacitor Pre-charge Function

A: The bootstrap capacitor pre-charge function is started.
B: During bootstrap capacitor pre-charge function, the high side power supply voltage exceeds high side UVLO voltage.
C: The bootstrap capacitor pre-charge function is finished and the PWMH pin start to outputs turn ON signal from next cycle.

Description of Blocks - continued

13 Frequency Jitter Function

The IC realizes a frequency jitter function by spreading CS pin peak voltage at high side turn OFF by 5 % with a t_{JIT} period.

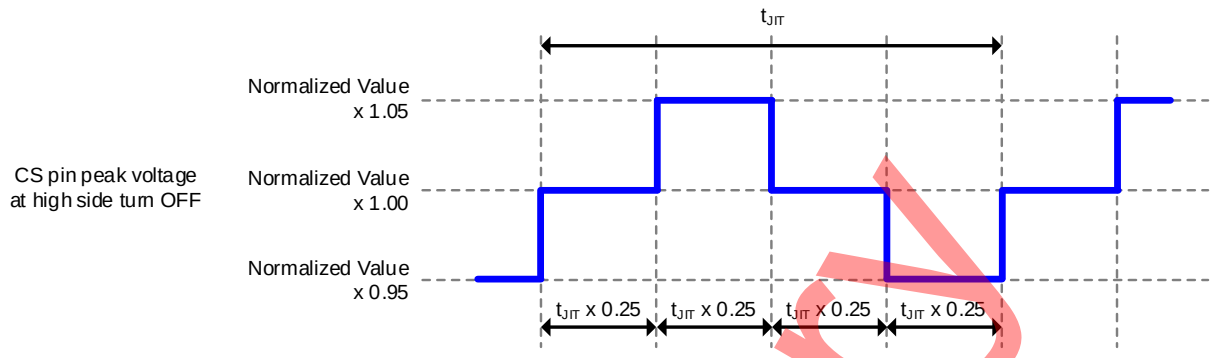


Figure 18. Frequency Jitter Function

14 Thermal Shutdown Protection

Thermal shutdown protection is auto restart type. Thermal shutdown function is worked when the junction temperature becomes more than T_{SD1} for t_{TSD}, switching is stopped. Switching restart when the junction temperature becomes less than T_{SD2}.

Description of Blocks - continued

15 Operation Mode of Protection Function

The operation modes of each protection function are shown in Table 4.

Table 4. Operation Modes of Protection Function

Protection Functions	Detection Conditions	Release Conditions	Auto Restart or Latch
AC UVLO	VH Pin Voltage < V_{ACUVLO} for t_{ACUVLO}	VH pin Voltage > V_{ACUVLO}	Auto Restart
VCC UVLO	VCC Pin Voltage < V_{UVLO2}	VCC pin Voltage > V_{UVLO1}	Auto Restart
VS UVLO	VS Pin Voltage < V_{SUVLO2} for t_{VSUVLO}	VS pin Voltage > V_{SUVLO1}	Auto Restart
VS OPEN Protection	VS Pin Voltage > V_{SOPEN1} for t_{VSOPEN}	VS Pin Voltage < V_{SOPEN2}	Auto Restart
VCLP UVLO	VCLP Pin Voltage < V_{CUVLO2}	VCLP pin Voltage > V_{CUVLO1}	Auto Restart
FB Overload Protection	FB Pin Voltage > V_{OLP1} for t_{OLP}	Auto Restart $t_{RESTART}$ after the Detection	Auto Restart
ZT Over Voltage Protection	ZT Pin Voltage > V_{ZTOVP} in Three Consecutive Switching Cycles	Auto Restart $t_{RESTART}$ after the Detection	Auto Restart
Dynamic Over Current Protection	CS Pin Voltage > V_{DOCP} in Two Consecutive Switching Cycles	Auto Restart t_{DOCP} after the Detection	Auto Restart
CS Pin Short Protection	CS Pin Voltage < V_{CSSP} t_{CSSP} after the High Side Turn ON	Auto Restart with pulse by pulse	Auto Restart
Out of Resonance Protection	CS Pin Voltage < V_{CSSP} t_{ORP} after the High Side Turn ON	Auto Restart t_{ORP} after the Detection	Auto Restart
Thermal Shutdown Protection	Tj > T_{TSD1} for t_{TSD}	Tj < T_{TSD2}	Auto Restart

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Min	Max	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1}	-0.3	+122	V	VCC pin
Maximum Applied Voltage 2	V_{MAX2}	-0.3	+30	V	VCLP pin
Maximum Applied Voltage 3	V_{MAX3}	-0.3	+6.5	V	VS, ZT, PFCOFF, ADJ1, ADJ2, ADJ3, FB, PWML, PWMH pin
Maximum Applied Voltage 4	V_{MAX4}	-1.0	+6.5	V	CS pin
ZT pin Maximum Current	I_{SZT}	-5.0	+5.0	mA	ZT pin
Maximum Junction Temperature	Tjmax	-40	+150	°C	
Storage Temperature Range	Tstg	-55	+150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note3)*	2s2p *(Note 4)*	
SSOP-B20				
Junction to Ambient	θ_{JA}	T.B.D.	T.B.D.	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	T.B.D.	T.B.D.	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range	V_{CC}	9.2	30	120	V	VCC pin
VCLP Pin Output Capacitance Range	C_{VCLP}	1	-	10	µF	
Switching Frequency Range	F_{SW}	-	-	500	kHz	
Operating Temperature	Topr	-40	-	+125	°C	Surrounding temperature

Electrical Characteristics (Unless noted otherwise, V_{CC} = 30 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VH Pin						
Startup Current 1	I_{START1}	0.1	0.3	1.0	mA	V_{CC} = 0 V
Startup Current 2	I_{START2}	1.0	3.0	6.0	mA	V_{CC} = 7 V
OFF Current	I_{START3}	-	10	25	µA	V_H = 400 V
AC UVLO Voltage	V_{ACUVLO}	75	85	95	V	VH peak voltage
AC UVLO Stop Timer	t_{ACUVLO}	102	128	154	ms	
VCC Pin						
VCC Operating Current	I_{OPE}	-	700	1200	µA	V_{FB} = 2.0 V
VCC Quiescent Current	I_{QUI}	-	500	600	µA	V_{FB} = 0 V
VCC Standby Current	I_{STB}	-	60	90	µA	V_{CC} = 6 V
VCC UVLO Release Voltage	V_{UVLO1}	9.45	10.00	10.55	V	VCC pin voltage rising
VCC UVLO Detection Voltage	V_{UVLO2}	7.45	8.00	8.55	V	VCC pin voltage falling
VCC UVLO Hysteresis Voltage	V_{UVLO3}	-	2.00	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC Recharge Start Voltage	V_{CHG1}	8.80	9.00	9.20	V	VCC pin voltage falling
VCC Recharge Stop Voltage	V_{CHG2}	8.95	9.50	10.05	V	VCC pin voltage rising
VCC Recharge Hysteresis Voltage	V_{CHG3}	-	0.50	-	V	$V_{CHG3} = V_{CHG2} - V_{CHG1}$
VS Pin						
VS Pin Outflow Current	I_{VS}	-	0.05	0.10	uA	
VS UVLO Release Voltage	V_{SUVLO1}	0.51	0.55	0.59	V	VS pin voltage rising
VS UVLO Detection Voltage	V_{SUVLO2}	0.48	0.52	0.56	V	VS pin voltage falling
VS UVLO Hysteresis Voltage	V_{SUVLO3}	-	0.03	-	V	$V_{SUVLO3} = V_{SUVLO1} - V_{SUVLO2}$
VS UVLO Detection Timer	t_{VSUVLO}	102	128	154	ms	
VS OPEN Detection Voltage	V_{SOPEN1}	3.05	3.30	3.55	V	VS pin voltage rising
VS OPEN Release Voltage	V_{SOPEN2}	2.95	3.20	3.45	V	VS pin voltage falling
VS OPEN Hysteresis Voltage	V_{SOPEN3}	-	0.10	-	V	$V_{SOPEN3} = V_{SOPEN1} - V_{SOPEN2}$
VS OPEN Detection Timer	t_{VSOPEN}	50	100	200	µs	
VCLP Pin						
VCLP Voltage	V_{CLP}	13.0	15.5	18.0	V	V_{CC} = 30 V
VCLP Maximum Output current	I_{CLP}	10	-	-	mA	DC
VCLP UVLO Release Voltage	V_{CUVLO1}	5.64	6.00	6.36	V	VCLP pin voltage rising
VCLP UVLO Detection Voltage	V_{CUVLO2}	4.70	5.00	5.30	V	VCLP pin voltage falling
VCLP UVLO Hysteresis Voltage	V_{CUVLO3}	-	1.00	-	V	$V_{CUVLO3} = V_{CUVLO1} - V_{CUVLO2}$

Electrical Characteristics – continued (Unless noted otherwise, V_{CC} = 30 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
FB Pin						
FB Burst Release Voltage	V_{BURST1}	0.37	0.41	0.44	V	FB pin voltage rising
FB Burst Detection Voltage	V_{BURST2}	0.34	0.37	0.40	V	FB pin voltage falling
FB Burst Hysteresis Voltage	V_{BURST3}	-	0.04	-	V	$V_{BURST3} = V_{BURST1} - V_{BURST2}$
FB OLP Detection Voltage	V_{OLP1}	2.5	2.8	3.0	V	FB pin voltage rising
FB OLP Release Voltage	V_{OLP2}	2.3	2.6	2.9	V	FB pin voltage falling
FB OLP Hysteresis Voltage	V_{OLP3}	-	0.2	-	V	$V_{OLP3} = V_{OLP1} - V_{OLP2}$
FB OLP Detection Timer	t_{OLP}	204	256	308	ms	
FB Pin Pullup Resistance	R_{FB}	22	30	38	kΩ	
Bottom Number from 12 to 11 Threshold Voltage	V_{FB1211}	0.47	0.50	0.53	V	FB pin voltage rising
Bottom Number from 11 to 10 Threshold Voltage	V_{FB1110}	0.51	0.55	0.59	V	FB pin voltage rising
Bottom Number from 10 to 9 Threshold Voltage	V_{FB109}	0.56	0.60	0.64	V	FB pin voltage rising
Bottom Number from 9 to 8 Threshold Voltage	V_{FB98}	0.63	0.67	0.71	V	FB pin voltage rising
Bottom Number from 8 to 7 Threshold Voltage	V_{FB87}	0.70	0.74	0.78	V	FB pin voltage rising
Bottom Number from 7 to 6 Threshold Voltage	V_{FB76}	0.77	0.81	0.85	V	FB pin voltage rising
Bottom Number from 6 to 5 Threshold Voltage	V_{FB65}	0.83	0.88	0.93	V	FB pin voltage rising
Bottom Number from 5 to 4 Threshold Voltage	V_{FB54}	0.90	0.95	1.00	V	FB pin voltage rising
Bottom Number from 4 to 3 Threshold Voltage	V_{FB43}	0.97	1.02	1.07	V	FB pin voltage rising
Bottom Number from 3 to 2 Threshold Voltage	V_{FB32}	1.04	1.10	1.16	V	FB pin voltage rising
Bottom Number from 2 to 1 Threshold Voltage	V_{FB21}	1.12	1.18	1.24	V	FB pin voltage rising
Bottom Number from 11 to 12 Threshold Voltage	V_{FB1112}	0.38	0.41	0.44	V	FB pin voltage falling
Bottom Number from 10 to 11 Threshold Voltage	V_{FB1011}	0.42	0.45	0.48	V	FB pin voltage falling
Bottom Number from 9 to 10 Threshold Voltage	V_{FB910}	0.47	0.50	0.53	V	FB pin voltage falling
Bottom Number from 8 to 9 Threshold Voltage	V_{FB89}	0.51	0.55	0.59	V	FB pin voltage falling
Bottom Number from 7 to 8 Threshold Voltage	V_{FB78}	0.56	0.60	0.64	V	FB pin voltage falling
Bottom Number from 6 to 7 Threshold Voltage	V_{FB67}	0.61	0.65	0.69	V	FB pin voltage falling
Bottom Number from 5 to 6 Threshold Voltage	V_{FB56}	0.67	0.71	0.75	V	FB pin voltage falling
Bottom Number from 4 to 5 Threshold Voltage	V_{FB45}	0.74	0.78	0.82	V	FB pin voltage falling
Bottom Number from 3 to 4 Threshold Voltage	V_{FB34}	0.80	0.85	0.90	V	FB pin voltage falling
Bottom Number from 2 to 3 Threshold Voltage	V_{FB23}	0.88	0.93	0.98	V	FB pin voltage falling
Bottom Number from 1 to 2 Threshold Voltage	V_{FB12}	1.00	1.05	1.10	V	FB pin voltage falling

Electrical Characteristics – continued (Unless noted otherwise, V_{CC} = 30 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
FB Pin						
FB Gain at Bottom Number 12	G_{FB12}	-	0.68	-	V/V	
FB Gain at Bottom Number 11	G_{FB11}	-	0.62	-	V/V	
FB Gain at Bottom Number 10	G_{FB10}	-	0.56	-	V/V	
FB Gain at Bottom Number 9	G_{FB9}	-	0.50	-	V/V	
FB Gain at Bottom Number 8	G_{FB8}	-	0.46	-	V/V	
FB Gain at Bottom Number 7	G_{FB7}	-	0.42	-	V/V	
FB Gain at Bottom Number 6	G_{FB6}	-	0.39	-	V/V	
FB Gain at Bottom Number 5	G_{FB5}	-	0.36	-	V/V	
FB Gain at Bottom Number 4	G_{FB4}	-	0.33	-	V/V	
FB Gain at Bottom Number 3	G_{FB3}	-	0.30	-	V/V	
FB Gain at Bottom Number 2	G_{FB2}	-	0.27	-	V/V	
FB Gain at Bottom Number 1	G_{FB1}	-	0.25	-	V/V	
ZT Pin						
ZT Comparator Voltage 1	V_{ZT1}	90	120	150	mV	ZT pin voltage rising
ZT Comparator Voltage 2	V_{ZT2}	60	85	110	mV	ZT pin voltage falling
ZT Comparator Hysteresis Voltage	V_{ZT3}	-	35	-	mV	$V_{ZT3} = V_{ZT1} - V_{ZT2}$
ZT OVP Voltage 1	V_{ZTOVP1}	2.06	2.20	2.34	V	R_{ADJ3} = 0 Ω
ZT OVP Voltage 2	V_{ZTOVP2}	2.82	3.00	3.18	V	R_{ADJ3} = 47 kΩ
ZT OVP Voltage 3	V_{ZTOVP3}	3.56	3.80	4.04	V	R_{ADJ3} = 100 kΩ
ZT OVP Voltage 4	V_{ZTOVP4}	4.70	5.00	5.30	V	R_{ADJ3} = OPEN
ZT Timeout 1	t_{ZTOUT1}	40	50	60	µs	
ZT Timeout 2	t_{ZTOUT2}	3.2	4.0	4.8	µs	
ZT Mask Time	t_{ZTMASK}	t_{DEADLS} +25	t_{DEADLS} +50	t_{DEADLS} +75	ns	
PFCOFF Pin						
PFCOFF Threshold Voltage 1	V_{ZTPFC1}	0.880	0.940	1.000	V	ZT pin voltage
PFCOFF Threshold Voltage 2	V_{ZTPFC2}	0.850	0.905	0.960	V	ZT pin voltage
PFCOFF Threshold Voltage Hysteresis	V_{ZTPFC3}	-	35	-	mV	$V_{ZTPFC3} = V_{ZTPFC1} - V_{ZTPFC2}$
PFCOFF Timer	t_{PFC}	6.4	8.0	9.6	ms	
PFCOFF High Voltage 1	V_{PFCH1}	4.70	5.00	5.30	V	I_{PFCOFF} = 0 mA
PFCOFF High Voltage 2	V_{PFCH2}	4.10	4.80	5.25	V	I_{PFCOFF} = -1 mA
PFCOFF Low Voltage	V_{PFCL}	0.0	0.1	0.3	V	I_{PFCOFF} = +5 mA
CS Pin						
Over Current Protection Voltage	V_{OCP}	0.475	0.500	0.525	V	
Dynamic Over Current Protection Voltage	V_{DOCP}	0.700	0.750	0.800	V	
Dynamic Over Current Protection Restart Time	t_{DOCP}	82	117	152	µs	
CS Pin Short Protection Voltage	V_{CSSP}	0.030	0.050	0.070	V	
CS Pin Short Protection Timer 1	t_{CSSP1}	6.0	8.0	10.0	µs	V_S = 0.6 V
CS Pin Short Protection Timer 2	t_{CSSP2}	1.2	1.6	2.0	µs	V_S = 2.5 V
Out of Resonance Protection Timer	t_{ORP}	t_{CSSP} +0.05	t_{CSSP} +0.10	t_{CSSP} +0.15	µs	
Leading Edge Blanking Time	t_{LEB}	-	140	-	ns	

Electrical Characteristics – continued (Unless noted otherwise, V_{CC} = 30 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DC/DC Converter Block						
High Side Maximum ON Time	$t_{HSONMAX}$	24	30	36	µs	
Low Side Maximum ON Time	$t_{LSONMAX}$	24	30	36	µs	
Low Side Dead Time	t_{DEADLS}	90	150	210	ns	
Low Side Minimum ON Time 1	$t_{LSONMIN1}$	4.50	5.00	5.50	µs	R_{ADJ2} = OPEN
Low Side Minimum ON Time 2	$t_{LSONMIN2}$	0.45	0.50	0.55	µs	R_{ADJ2} = 0 Ω
Target Rising Time of Half Bridge Node 1	t_{RTAR11}	375	450	525	ns	R_{ADJ1} = 0 Ω
Target Rising Time of Half Bridge Node 2	t_{RTAR12}	300	360	420	ns	R_{ADJ1} = 47 kΩ
Target Rising Time of Half Bridge Node 3	t_{RTAR13}	250	300	350	ns	R_{ADJ1} = 100 kΩ
Target Rising Time of Half Bridge Node 4	t_{RTAR14}	180	225	270	ns	R_{ADJ1} = 220 kΩ
Target Rising Time of Half Bridge Node 5	t_{RTAR15}	105	150	195	ns	R_{ADJ1} = OPEN
ZT Delay Time	t_{DEL}	110	200	290	ns	
Minimum Frequency	f_{SWMIN}	20	25	30	kHz	
Jitter Period	t_{JIT}	50.0	62.5	75.0	us	
Low Side Pre-Pulse Width	t_{PRE}	0.48	0.60	0.72	µs	
Start Timer at Pre-Charge	t_{START}	4.0	5.0	6.0	µs	
Burst Mode Duration Time to increase Pre-pulse by one	t_{BURST}	0.43	0.50	0.57	ms	
Soft Start Time 1	t_{SS1}	0.7	1.0	1.3	ms	
Soft Start Time 2	t_{SS2}	1.4	2.0	2.6	ms	
Soft Start Time 3	t_{SS3}	2.8	4.0	5.2	ms	
Restart Time	$t_{RESTART}$	1638	2048	2458	ms	
PWM Output Block						
PWML High Voltage 1	V_{PWMLH1}	4.70	5.00	5.30	V	I_{PWML} = 0 mA
PWML High Voltage 2	V_{PWMLH2}	4.10	4.80	5.25	V	I_{PWML} = -4 mA
PWML Low Voltage	V_{PWMLL}	0.0	0.1	0.3	V	I_{PWML} = +10 mA
PWMH High Voltage 1	V_{PWMHH1}	4.70	5.00	5.30	V	I_{PWMH} = 0 mA
PWMH High Voltage 2	V_{PWMHH2}	4.10	4.80	5.25	V	I_{PWMH} = -4 mA
PWMH Low Voltage	V_{PWMHL}	0.0	0.1	0.3	V	I_{PWML} = +10 mA
Thermal Shutdown Block						
Thermal Shutdown Detection Temperature	T_{SD1}	150	175	200	°C	*(Note 1)*
Thermal Shutdown Release Temperature	T_{SD2}	80	100	120	°C	*(Note 1)*
Thermal Shutdown Hysteresis Temperature	T_{SD3}	-	75	-	°C	*(Note 1)*
Thermal Shutdown Detection Timer	t_{TSD}	50	100	200	µs	

(Note 1) No shipping inspection.

Application Examples

T.B.D.

Typical Performance Curves (Reference Data)

T.B.D.

I/O Equivalence Circuit

T.B.D.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

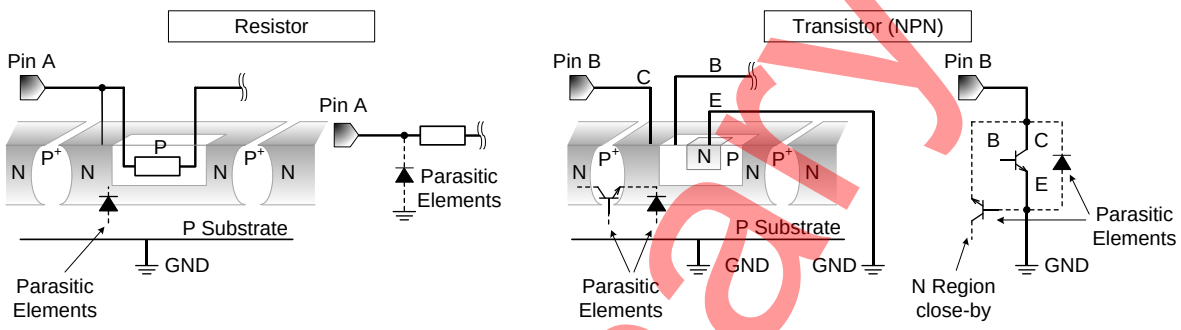


Figure 19. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

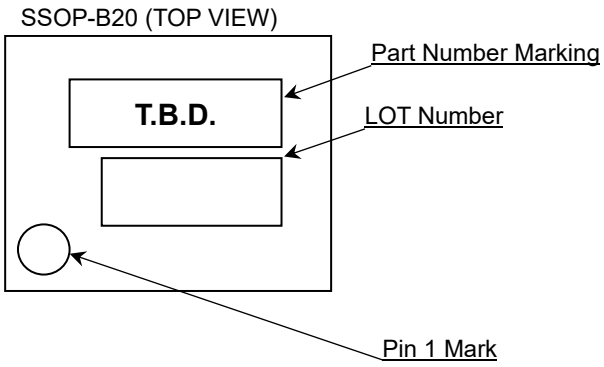
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

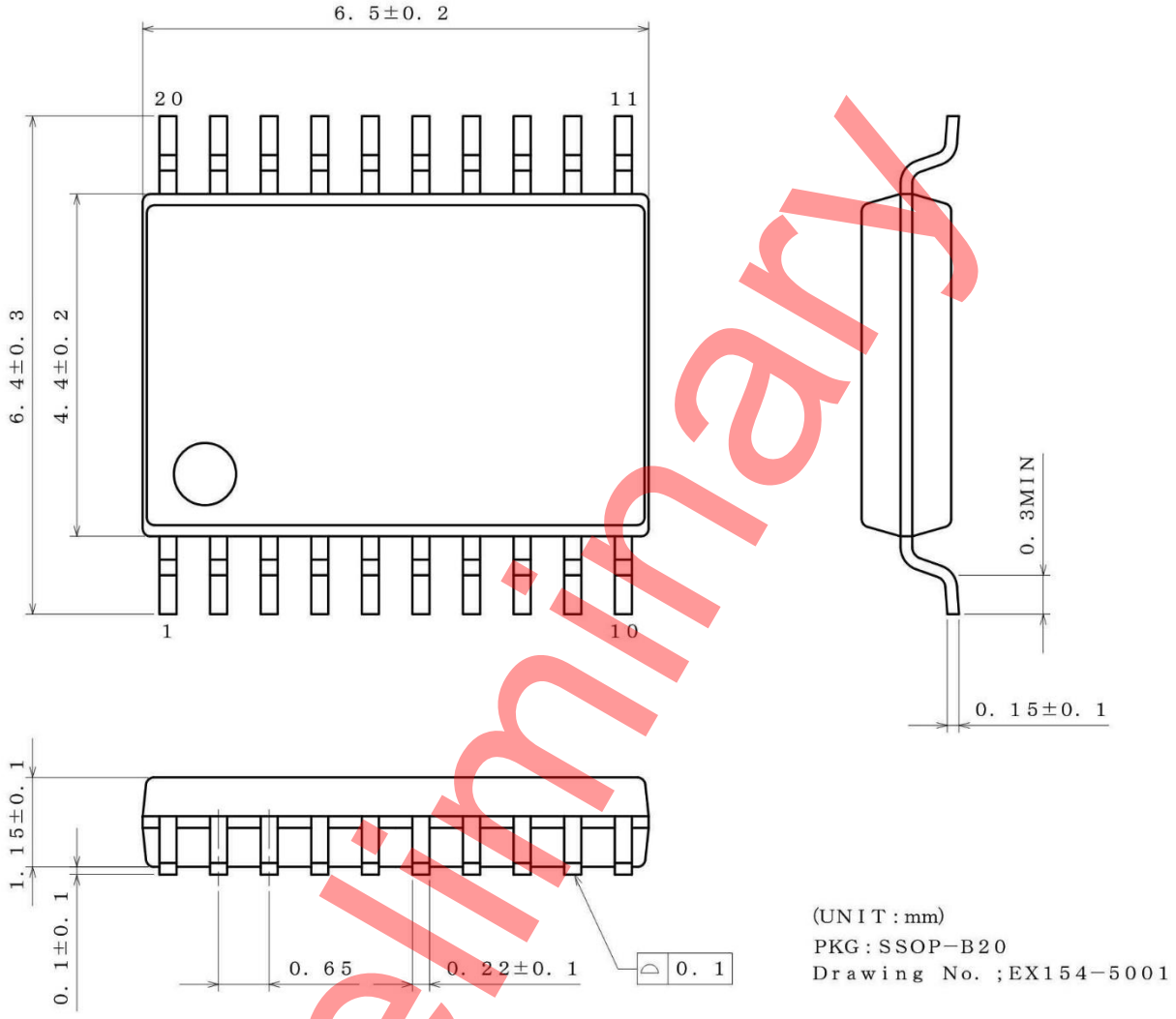
B	M	1	A	H	0	0	1	F	V	-	L	B	E	2

Marking Diagram



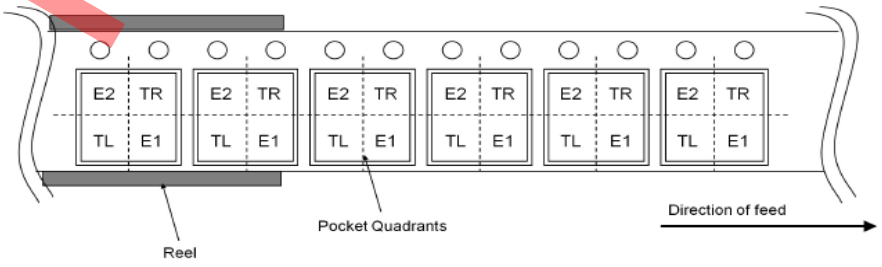
Physical Dimension and Packing Information

Package Name	SSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
12.Jul.2023	001	Target Spec Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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