AC/DC Drivers

Quasi-resonant DC/DC Converters

BM1Q0xxAFJ-LB Series

General Description

This is the product guarantees long time support in Industrial market. This product is ideal for use in these applications. The quasi-resonant controller type DC/DC converter IC BM1Q0xxAFJ-LB provides the optimal system for products with electrical outlets. For quasi-resonant vibration operation, soft switching is realized, contributing to low EMI.

The switching MOSFET and current sensing resistor are external, allowing for highly flexible power supply designs. This IC has a built-in starter circuit that contributes to low standby power and high speed startup.

When the IC is light load, the standby power is reduced due to the built-in burst operation function and the lower current consumption of the IC.

It also has a variety of built-in protection functions such as soft start function, burst function, over current protection per cycle, over voltage protection, overload protection, and built-in the CS pin open protection, providing excellent safety.

Features

- Long Time Support Product for Industrial Applications
- Quasi-resonant System
- Built-in 650 V Tolerate Starter Circuit
- Burst Operation at Light Load / Frequency Reduction Function
- Maximum Frequency 120 kHz
- AC Input Voltage Correction Circuit
- VCC Pin Under Voltage Protection
- VCC Pin Over Voltage Protection
- Over Current Protection Circuit per Cycle
- Output Driver 12 V Clamp Circuit
- Soft Start Function
- ZT Pin Trigger Mask Function
- ZT Pin Over Voltage Protection
- Output Overload Protection (Auto Restart)
- CS Pin Open Protection Circuit (Auto Restart)

Key Specifications

- Operating Power Supply Voltage Range:
  VCC: 8.9 V to 26.0 V
  VH: -0.3 V to +650 V
- Current at Switching Operation: 600 µA (Typ)
- Current at Burst Operation: 350 µA (Typ)
- Maximum Operating Frequency: 120 kHz (Typ)
- Operate Temperature Range: -40 °C to +105 °C

Package **W (Typ) x D (Typ) x H (Max)**
SOP-J7S 4.9 mm x 6.0 mm x 1.65 mm

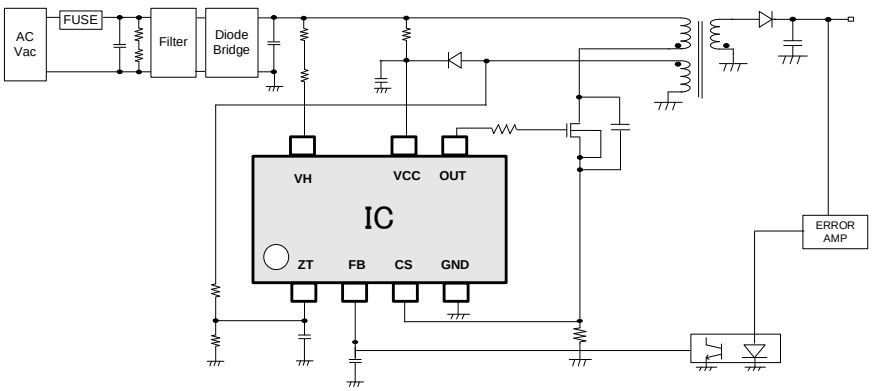
Lineup

Product Name	VCC OVP	ZT OVP
BM1Q002AFJ-LB	Latch	Latch
BM1Q021AFJ-LB	Auto Restart	Auto Restart

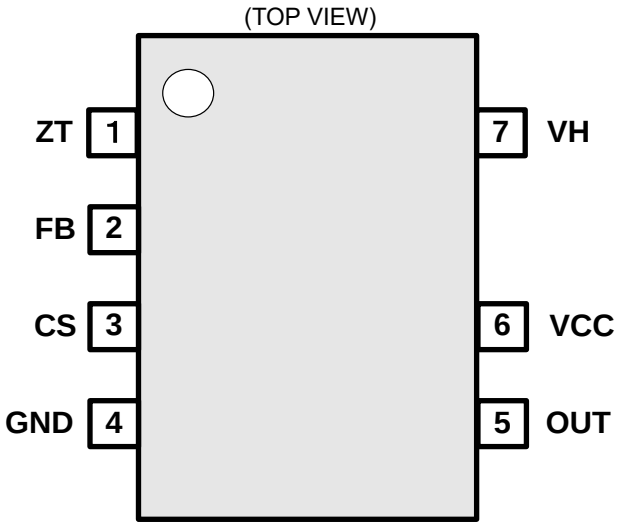
Applications

Industrial Equipment, Products that Require Electrical Outlets, Such as Air Conditioners, AC Adapters, and TVs

Typical Application Circuit



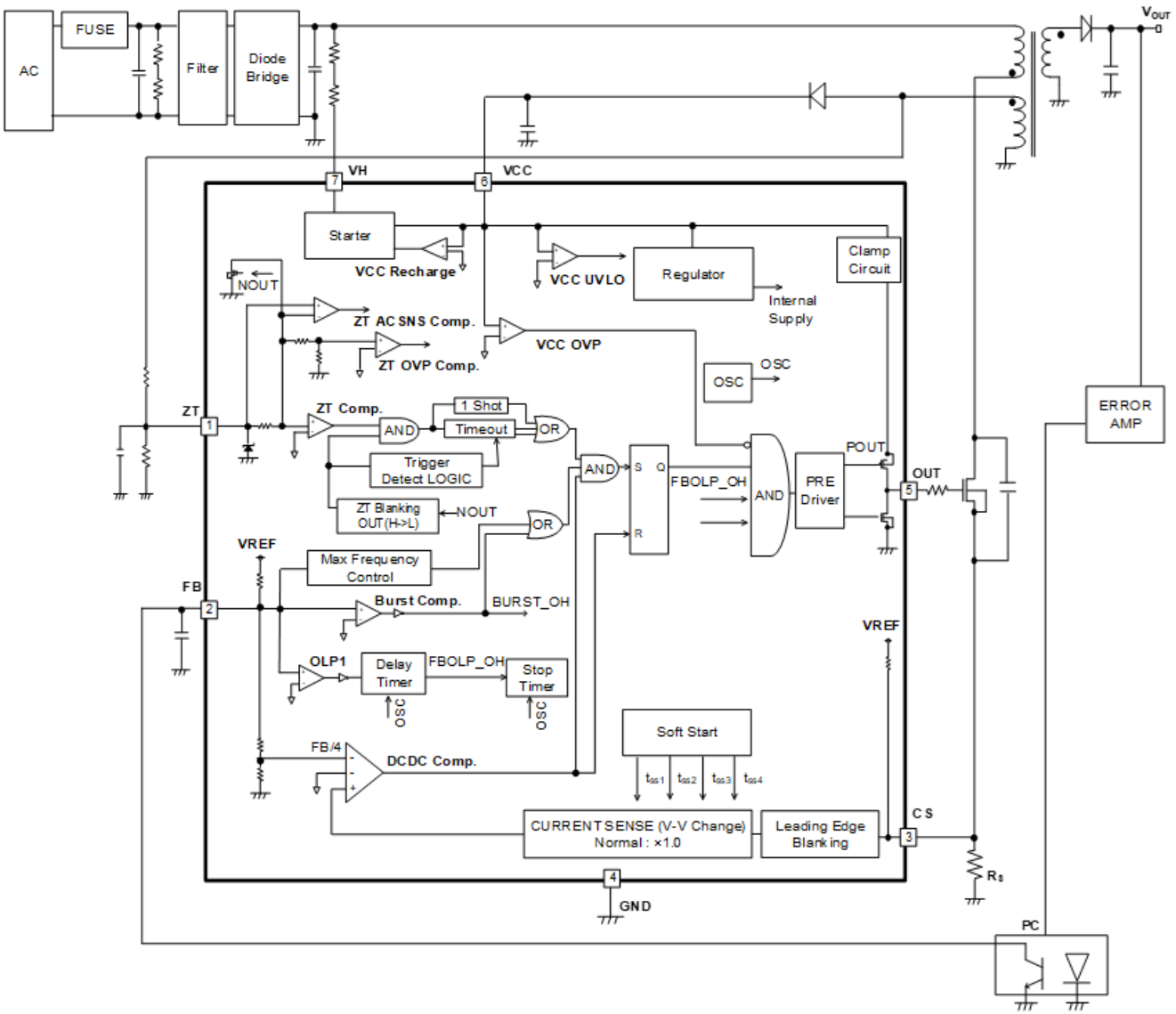
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	I/O	Function	ESD Protection System	
				VCC	GND
1	ZT	I	Zero current detect pin	-	○
2	FB	I	Feedback signal input pin	○	○
3	CS	I	Primary current sensing pin	○	○
4	GND	I/O	GND pin	○	-
5	OUT	O	External MOS drive pin	○	○
6	VCC	I/O	Power supply pin	-	○
7	VH	I	Starter circuit pin	-	○

Block Diagram



Description of Blocks

1 Starter Circuit the VH Pin

This IC has a built-in starter circuit in the VH pin. Therefore, it enables to be low standby power and high speed starting. It can also be activated by opening starter circuit of the VH pin.

1.1 In Case of Using the VH Pin

The VH pin current flowing during operation is shown in Figure 2. After the IC is started, I_{START3} flows from the VH pin. Loss due to this idling current is shown below.

ex) Power consumed by starter circuit alone

at $Vac = 100\,V$,

$$Power = 100\,V \times \sqrt{2} \times 10\,\mu A = 1.41\,mW$$

at $Vac = 240\,V$,

$$Power = 240\,V \times \sqrt{2} \times 10\,\mu A = 3.38\,mW$$

The start time is determined by the inrush current of the VH pin and the capacitor capacitance of the VCC pin. Figure 3 shows reference start times. For example, when C_{VCC} = 10 µF, it is charged within about 70 ms.
When the VCC pin is shorted to GND, the current of I_{START1} indicated by Figure 2 flows.
When the VH pin is shorted to GND, large current flows from V_A to GND. To prevent it, insert a current limiting resistor R_{VH} between V_A and the VH pin of the IC. At this time, the power of VH^2/R_{VH} is applied to R_{VH}, so check the allowable power before determining the resistor size. If one resistor cannot satisfy the allowable power, connect two or above resistors in series.

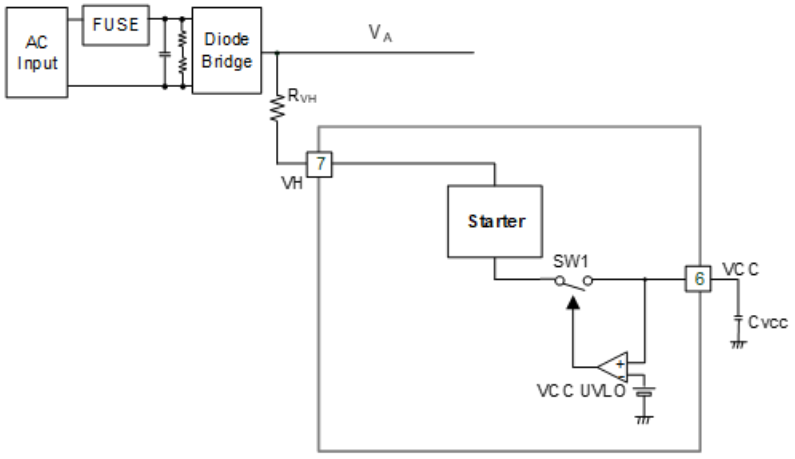


Figure 1. Starter Circuit Block Diagram

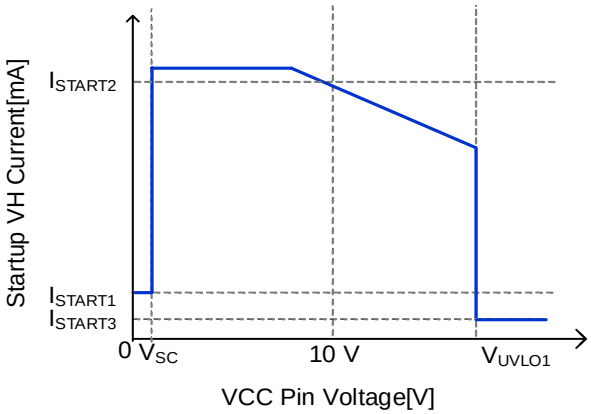


Figure 2. Startup VH Current vs VCC Pin Voltage

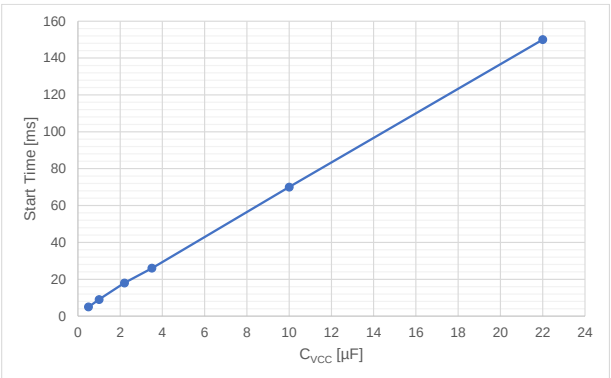


Figure 3. Start Time (Reference Value)

1.1 In Case of Using the VH Pin - continued

It shows operation waveform of startup in Figure 4.

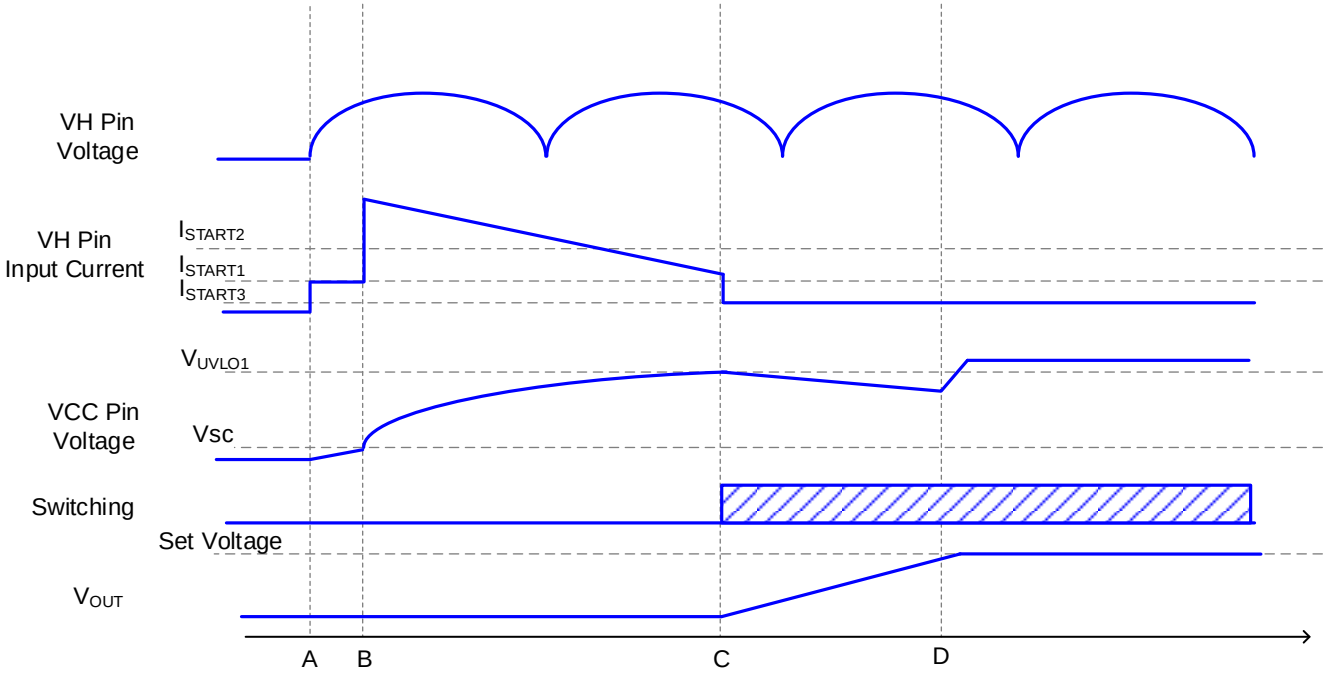


Figure 4. Startup Waveform

A: By inserting to outlet, the VH pin voltage is applied. From the time, charging to the VCC pin starts from the VH pin through starter circuit. The VCC pin voltage < V_{SC} at this point, so the VH pin input current is limited to I_{START1} by the VCC pin short protection function.

B: Because the VCC pin voltage > V_{SC}, the VCC pin short protection function is released and current flows from the VH pin input current.

C: Because the VCC pin voltage > V_{UVLO1}, starter circuit is stopped and I_{START3} flows through the VH pin input current. At this time, switching operation starts and V_{OUT} starts rising, but the VCC pin voltage drops because V_{OUT} is not rising sufficiently. Since the VCC pin voltage always drops depending on the current consumed, set it so that the VCC pin voltage > V_{UVLO2}. The fall rate of the VCC pin voltage is determined by the VCC pin capacitor capacitance and the current consumption of the IC, and the load current connected to the VCC pin. ($V/t = C_{VCC}/I_{CC}$)

D: Since V_{OUT} has risen to specific voltage, the auxiliary winding applies a voltage to the VCC pin and the VCC pin voltage stabilizes.

1 Starter Circuit the VH Pin - continued

1.2 In Case of Unused the VH Pin

The structure that do not use the VH pin is shown in Figure 5. It is activated by opening starter circuit of the VH pin and connecting a startup resistor R_{START} to the VCC pin. At startup (before VCC UVLO releasing), the current consumption I_{OFF} of the VCC pin flows through R_{START}, so set to an appropriate resistance.

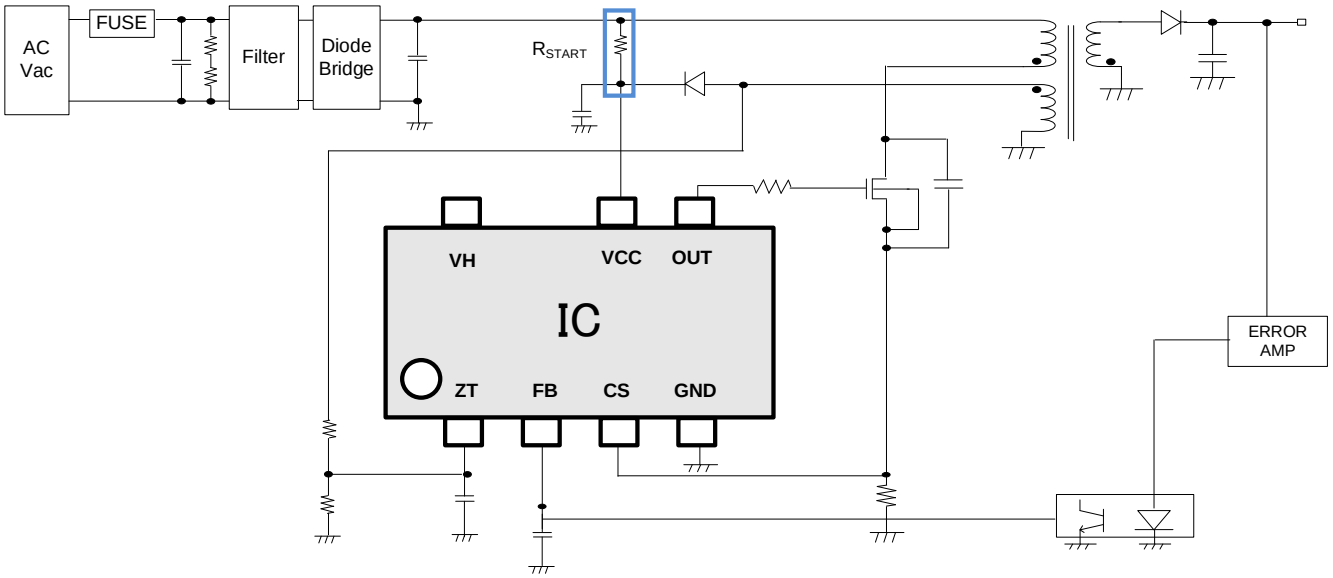


Figure 5. Application Schematic Without Using VH Pin

1.2.1 Setting Method for the Startup Resistor

If you reduce R_{START} value, standby power is increased, start time is shorter.
If you increase R_{START} on the contrary, standby power is reduced, start time will be longer.

ex) Startup resistor R_{START} setting

$$R_{START} = (V_{MIN} - V_{UVLO1}(\max)) / I_{OFF}(\max)$$

Where:
R_{START} is the startup resistor
V_{MIN} is the minimum input DC voltage
V_{UVLO1} is the VCC UVLO voltage1
I_{OFF} is the operating current in standby mode

At Vac = 100 V, a margin of -30 % results in V_{MIN} = 100 x √2 x 0.7 = 99 V.
In this case, because V_{UVLO1} (max) = 14.5 V, R_{START} = (99 - 14.5)/25 µA = 3.38 MΩ.

For example, that R_{START} = 2.0 MΩ with a margin of more than 3.38 MΩ.
For AC100 V, R_{START} consumes Pd (R_{START}) = (VH - VCC)^2/R_{START} = (141 V - 14.5 V)^2/2.0 MΩ = 8.00 mW.
Thus, when starting up in R_{START}, the standby power is increased compared to when using the VH pin.
However, confirm R_{START} and the VCC pin capacitance by evaluating the actual application.

Description of Blocks - continued

2 Startup Sequence (FB OLP: Auto Restart Mode)

The startup sequence of IC is shown in Figure 6. About each detail, explain in each section.

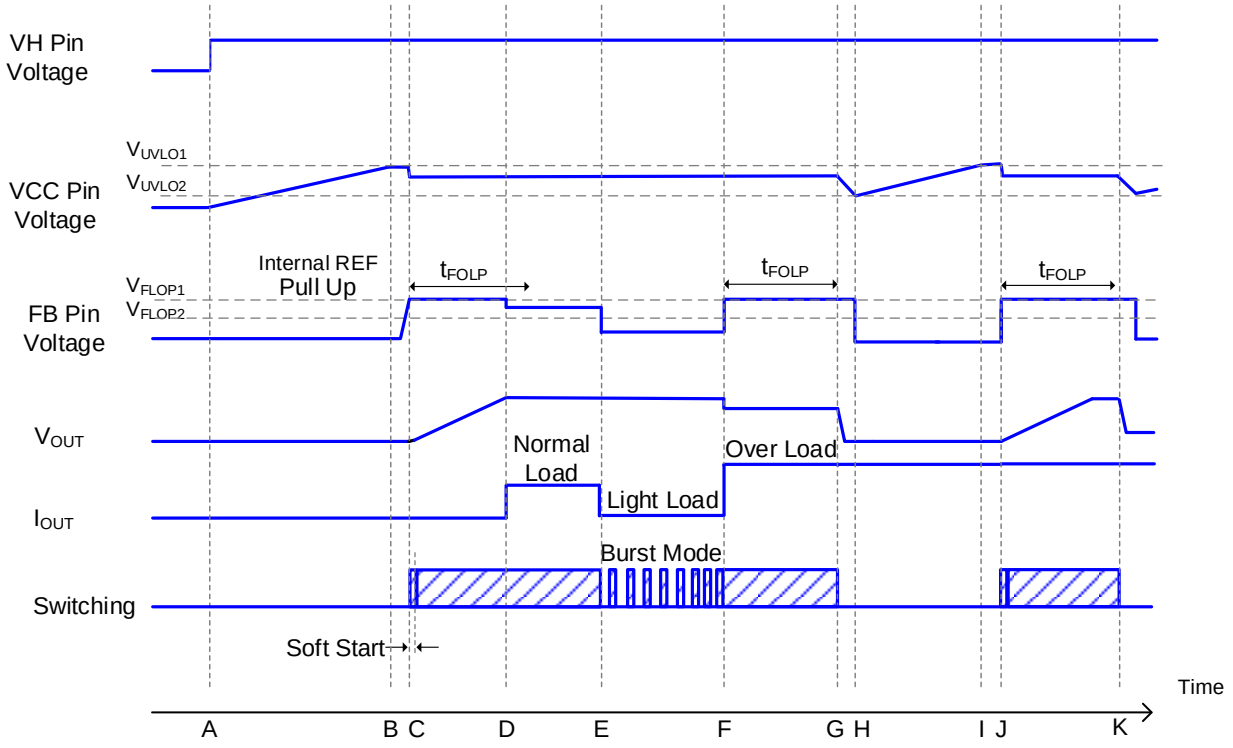


Figure 6. Startup Sequence Timing Chart

A: The VH pin voltage is applied, and the VCC pin voltage rises due to the startup resistor R_{START}.
B: When the VCC pin voltage > V_{UVLO1}, this IC starts operation.
C: When the protection function is judged to be normal, switching operation starts. At this time, the VCC pin voltage drops depending on the current consumption. Therefore, set it so that the VCC pin voltage > V_{UVLO2}. This IC has a soft start function to adjust the voltage level of the CS pin voltage so that excessive voltage rise and current rise do not occur. Also, V_{OUT} increases when switching starts.
D: At startup, set the output voltage to the specified voltage within t_{FOLP}.
E: When it is light load, burst operation is used to keep power consumption down.
F: When the FB pin voltage > V_{FOLP1}, it starts overload operation.
G: If the FB pin voltage > V_{FOLP1} persists for t_{FOLP} or above, the overload protection circuit stops switching. Once the FB pin voltage < V_{FOLP2}, FB OLP detection timer t_{FOLP} is reset.
H: When the VCC pin the voltage < V_{UVLO2}, the IC restarts.
I : Same as B.
J: Same as F.
K: Same as G.

Description of Blocks - continued

3 The VCC Pin Protective Function

This IC has a built-in VCC UVLO and VCC OVP of the VCC pin, and VCC charge function that operates when the VCC pin voltage drops. VCC UVLO and VCC OVP are for preventing the switching MOSFET from destroying for abnormal voltages.

When the VCC pin voltage drops, the VCC charge function charges the high voltage line from the starter circuit to stabilize the secondary output voltage.

3.1 VCC UVLO / VCC OVP

VCC UVLO is an auto restart mode with voltage hysteresis.

VCC OVP is a comparator with voltage hysteresis. BM1Q002AFJ-LB is latch mode and BM1Q021AFJ-LB is auto restart mode.

The latch release (reset) condition after latch detection by VCC OVP is the VCC pin voltage < V_{LATCH}.

Figure 7 shows the time chart of VCC OVP latch mode, and Figure 8 shows the time chart of VCC OVP auto restart mode. VCC OVP also has a built-in t_{LATCH} mask time. This function masks surges that occur at the VCC pin.

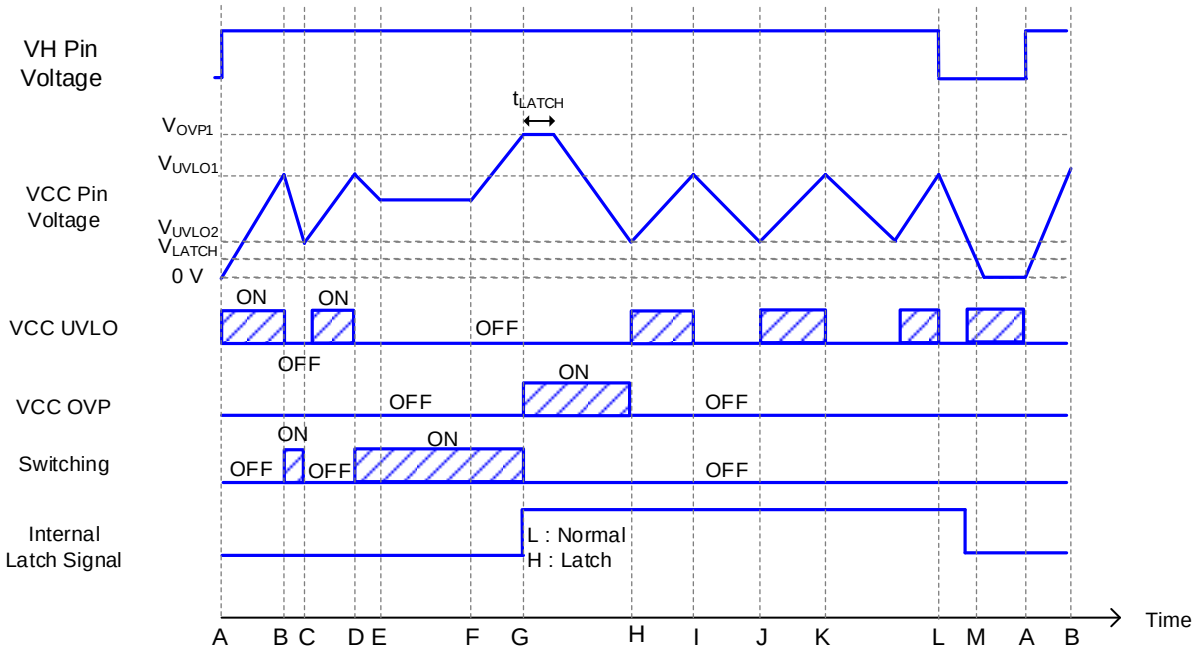


Figure 7. VCC UVLO / OVP (Latch Mode)

A: The VH pin voltage is applied and the VCC pin voltage rises.
B: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released and switching operation starts.
C: The VCC pin voltage < V_{UVLO2}, the switching operation is stopped by VCC UVLO function.
D: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released and switching operation starts.
E: The VCC pin voltage drops until the output voltage stabilizes.
F: The VCC pin voltage rises.
G: The VCC pin voltage > V_{OVP1} is t_{LATCH} on, VCC OVP activates the internal latch signal and stops the switching operation. When switching operation is stopped, power is no longer supplied from the auxiliary winding and the VCC pin voltage is reduced.
H: The VCC pin voltage < V_{UVLO2}, the VCC pin voltage rises because the current consumed by the IC drops.
I: The VCC pin voltage > V_{UVLO1}, switching does not operate because latching is in progress. The VCC pin voltage drops because switching is stopped.
J: Same as H.
K: Same as I.
L: The VH pin voltage becomes open, the VCC pin voltage drops.
M: The VCC pin voltage < V_{LATCH}, latch function is released.

3.1 VCC UVLO / VCC OVP - continued

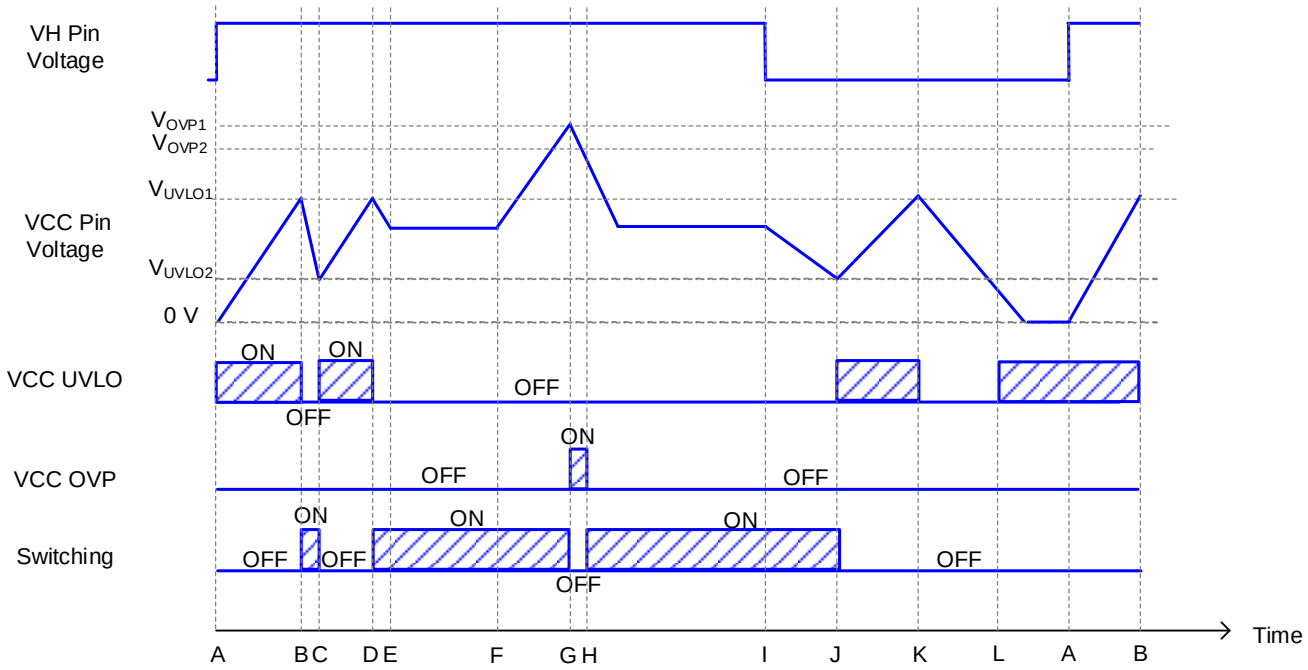


Figure 8. VCC UVLO / OVP (Auto Restart Mode)

A: The VH pin voltage is applied and the VCC pin voltage rises.
B: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released and switching operation starts.
C: The VCC pin voltage < V_{UVLO2}, the switching operation is stopped by VCC UVLO function.
D: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released and switching operation starts.
E: The VCC pin voltage drops until the output voltage stabilizes.
F: The VCC pin voltage rises.
G: The VCC pin voltage > V_{OVP1}, the switching operation is stopped by VCC OVP. When switching operation is stopped, power is no longer supplied from the auxiliary winding and the VCC pin voltage is reduced.
H: The VCC pin voltage < V_{OVP2}, switching operation is started by the auto restart.
I: The VH pin voltage becomes open, the VCC pin voltage drops.
J: Same as C.
K: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released and the VCC pin voltage drops. However, switching operation does not resume because the VH pin input voltage is open.
L: The VCC pin voltage < V_{UVLO2}, VCC UVLO function operates. However, because the VH pin voltage is open, the VCC pin voltage continues to drop.

3 The VCC Pin Protective Function

3.2 The VCC Pin External Components

3.2.1 Capacitor Value of the VCC Pin

For stable operation of ICs, set the capacitor of the VCC pin to 1 µF or above. Note that if the VCC pin capacitor is too large, the VCC pin responds slowly to V_{OUT}. In addition, if the transformer is less coupled, a large surge will be generated in the VCC pin, and the IC may be destroyed. In this case, provide a resistor of approximately 10 Ω to 100 Ω in the path between the diode and the capacitor after the auxiliary winding. For the constants, perform a waveform assessment of the VCC pin and set the VCC pin so that the surges do not exceed the absolute maximum rating of the VCC pin voltage.

3.2.2 How to Set VCC OVP Protection When V_{OUT} Is Increased

The VCC pin voltage is determined by V_{OUT} and transformer ratio (N_p: N_S).

$$VCC\ Pin\ Voltage = V_{OUT} \times N_b/N_S - V_F$$

Where:
V_{OUT} is the output voltage
N_b is the number of auxiliary winding
N_S is the number of winding on secondary side

Therefore, if V_{OUT} is increased, it can be protected by VCC OVP. VCC OVP protection setting is as follows.

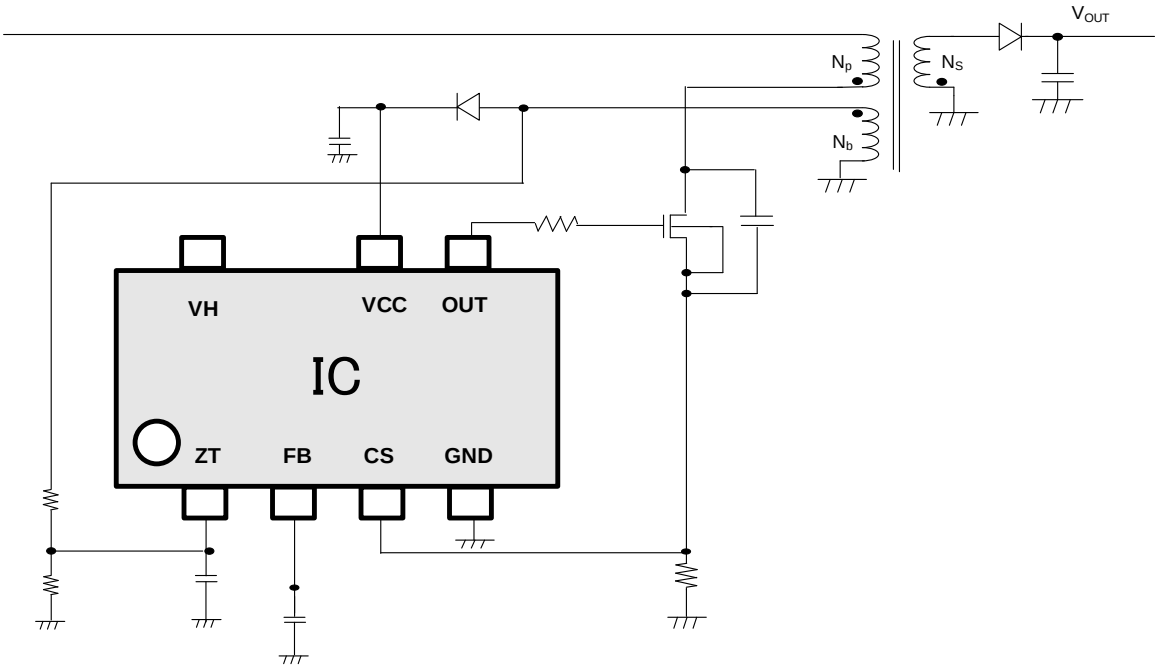


Figure 9. VCC OVP

For example, if you want to protect V_{OUT} x 1.3, set the number of winding so that it becomes 1.3 x (V_{OUT} x (N_b/N_S) - V_F) > V_{OVP1}. VCC OVP protection does not detect VCC OVP protection against instantaneous surge noise on the VCC pin because of t_{LATCH} masking times. However, if the VCC pin voltage is higher than V_{OVP1} for t_{LATCH} periods or above due to factors such as poor trans binding, a VCC OVP is detected. Therefore, be sure to check the application rating and set VCC OVP.
ZT OVP can also be used to protect V_{OUT}.

Description of Blocks - continued

4 The VCC Charge Function

Once the VCC pin > V_{UVLO1}, the VCC charge function operates when the VCC pin voltage drops to V_{CHG1} after the IC starts up. At this time, it charges the VCC pin from the VH pin through the starter circuit, it does not occur VCC start problem. When the IC charge the VCC pin and the VCC pin voltage > V_{CHG2}, the charging function is finished. This operation is shown in Figure 10.

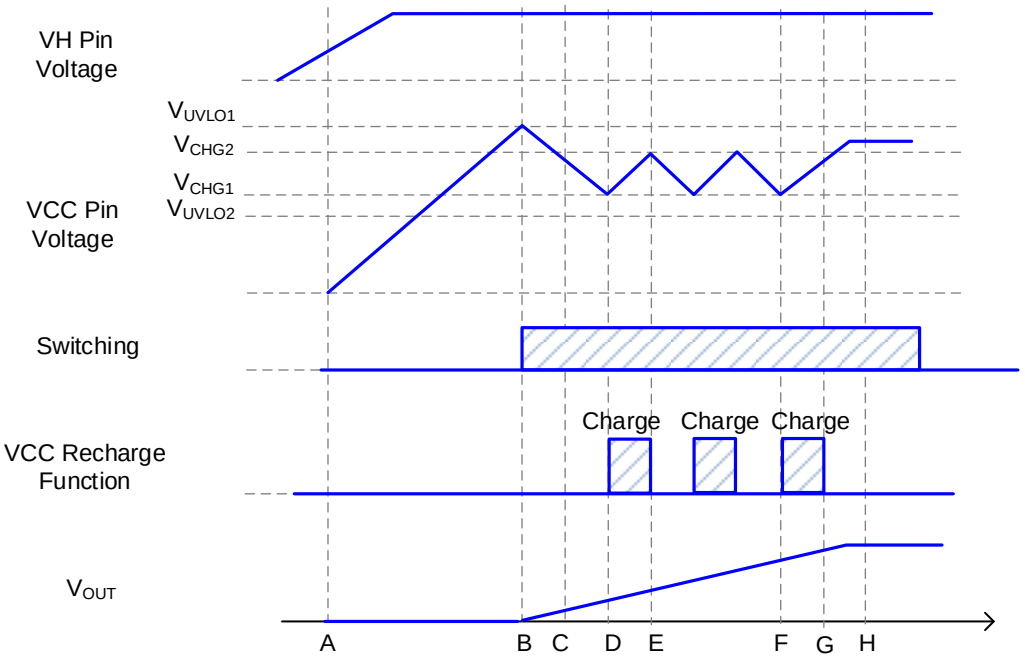


Figure 10. VCC Pin Charging Operation

A: The VH pin voltage rises and the VCC charge function starts charging to the VCC pin.
B: The VCC pin voltage > V_{UVLO1}, VCC UVLO function is released, the VCC charge function is stopped, and switching operation starts.
C: The VCC pin voltage drops because the output voltage is not rising sufficiently at startup.
D: The VCC pin voltage < V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
E: The VCC pin voltage > V_{CHG2}, the VCC charge function is stopped.
F: Same as D.
G: Same as E.
H: The output voltage rises, the auxiliary winding is charged to the VCC pin and the VCC pin voltage is stabilized.

Description of Blocks - continued

5 DC/DC Converters Function

This IC operates the PFM (Pulse Frequency Modulation) mode control method.
By monitoring the FB pin, the ZT pin, and the CS pin, the optimum system is supplied as a DC/DC. The FB pin and the CS pin control the ON width (turn OFF) of the switching MOSFET, and the ZT pin controls the OFF width (turn ON).
IC internal QR operation block diagram and QR basic operation are shown in Figure 11, Figure 12.

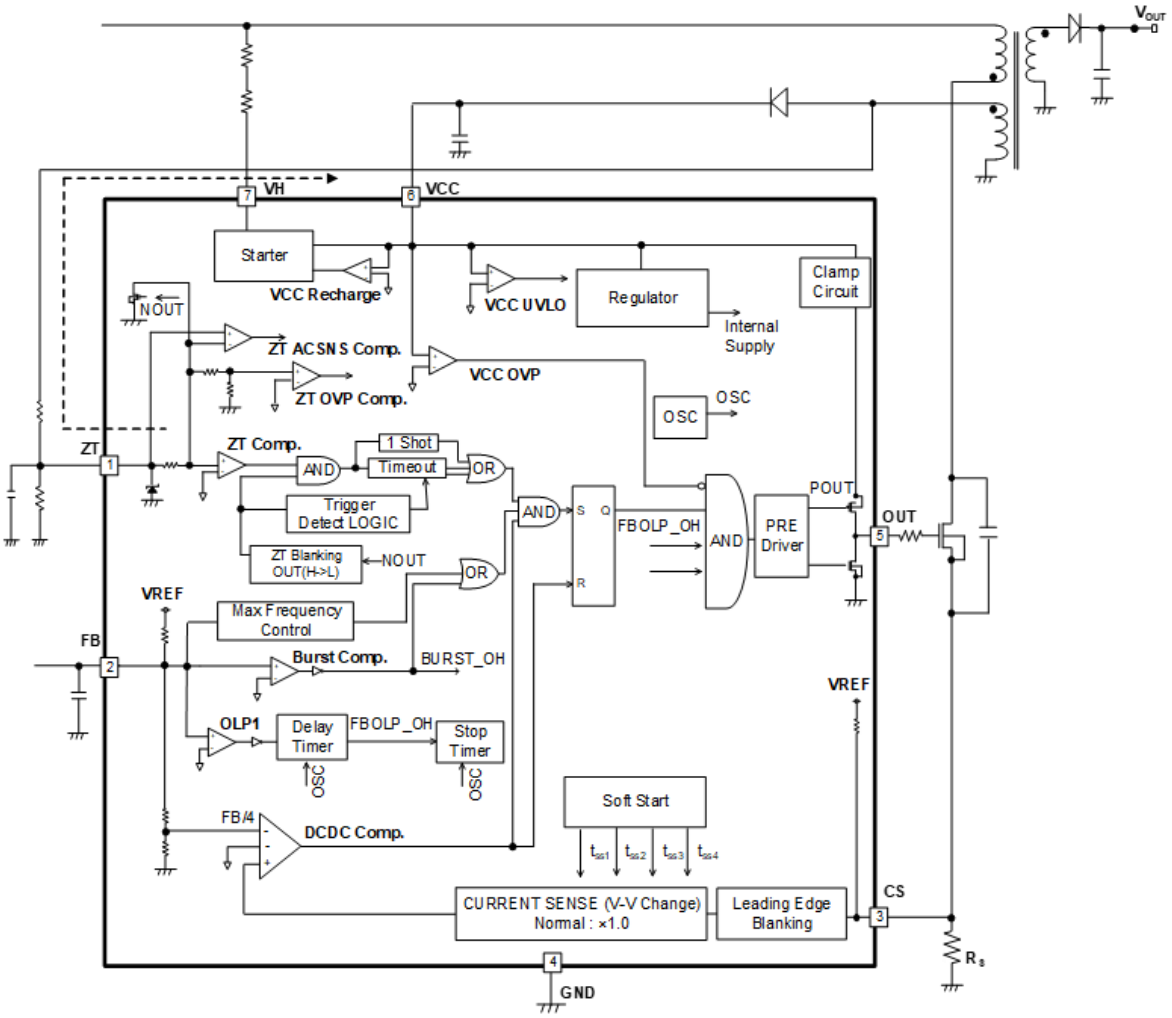


Figure 11. IC Internal QR Operation Block Diagram

5 DC/DC Converters Function - continued

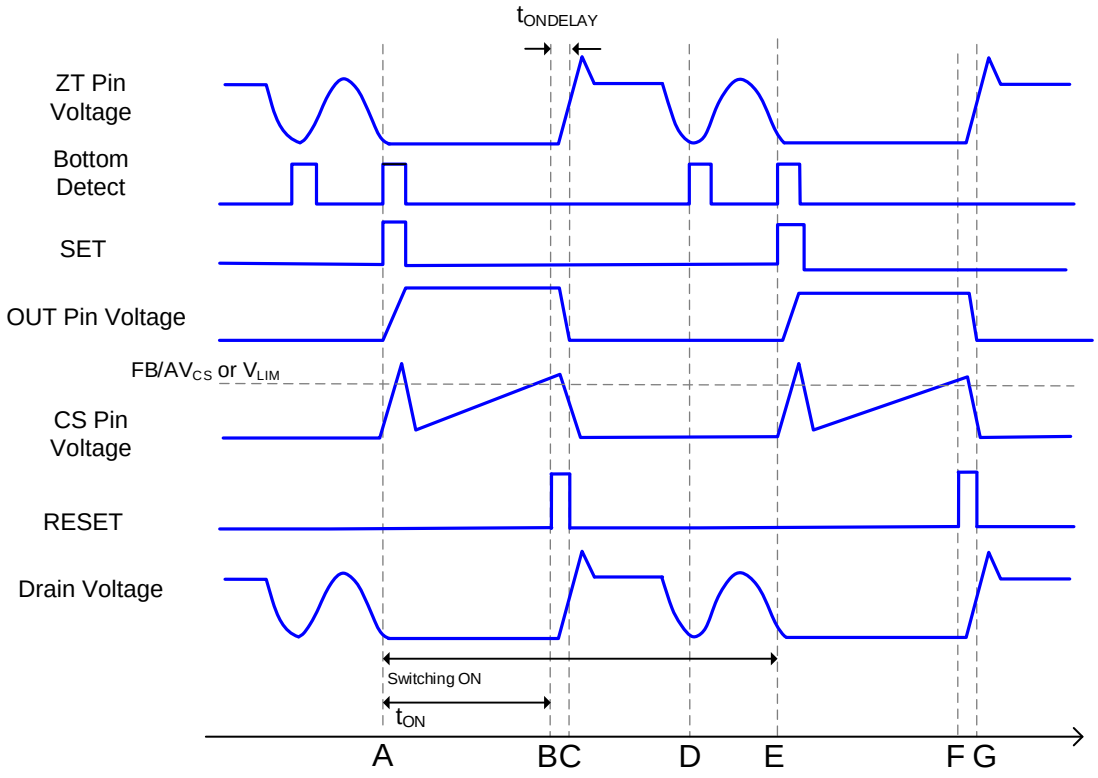


Figure 12. QR Basic Operation

A: MOSFET is turned ON by outputting the SET signal from the oscillator inside the IC.
At this time, noise is generated in the CS pin because the DRAIN - SOURCE capacitance of MOSFET is discharged. This noise is called Leading Edge. This IC has a built-in filter for this noise. The minimum ON width of the IC is t_{MIN} by this filter and the delay time. After that, the current flows through MOSFET and the voltage $V_{CS} = R_S*I_p$ is applied to the CS pin.
B: The CS pin voltage rises above the FB pin voltage/AV_{CS} or the over current detection voltage V_{LIM}, RESET signal is output and the OUT pin voltage is turn OFF.
C: There is a delay $t_{ONDELAY}$ from the point of B to turn OFF actually. This time results in a difference in maximum power due to AC voltage. This IC has a built-in function to reduce this difference.
D: The energy stored in the transformer during t_{ON} is discharged to the secondary, and the drain voltage starts free vibration due to transformer L_p value and C_{ds} (DRAIN - SOURCE capacitance) of MOSFET.
E: Since the switching frequency is determined internally in the IC, the SET signal is output from the internal oscillator and turn ON the MOSFET by process of certain time from A.
F: Same as B.
G: Same as C.

5 DC/DC Converters Function - continued

5.1 Determination of ON Width (Turn OFF)

The ON width is controlled by the FB pin and the CS pin.
The ON width is determined by comparing the FB pin voltage to 1/AV and the CS pin voltage. As shown in Figure 13, the comparator level is changed by comparing with V_{LIM1A} generated in the IC.
The CS pin is shared with over current limiter circuit by each pulse. It also changes the maximum blanking frequency and the over current limiter level by changing in the FB pin.

mode 1: Burst operation
mode 2: Frequency reduction operation (Decreases the maximum frequency.)
mode 3: Maximum frequency operation (Operates at the maximum frequency.)
mode 4: Overload operation (Detects the overload condition and stops the pulsing operation.)

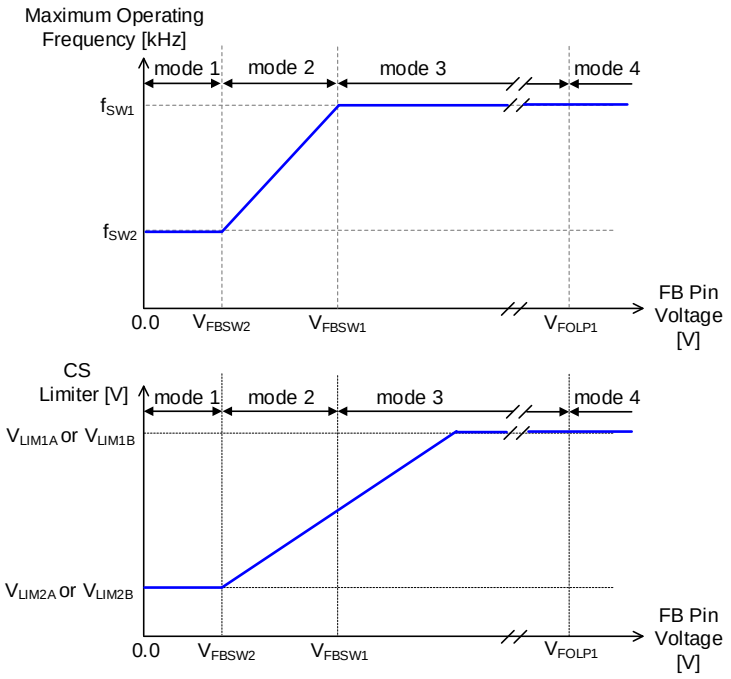


Figure 13. Relationship of FB Pin Voltage to Over Current Limiter and Maximum Frequency

The ON width t_{ON} is determined by the CS Limiter (V_{CS}).

$$t_{ON} = (L_p \times V_{CS})/(V_{IN} \times R_S)$$

Where:
L_p is the primary inductance value
V_{IN} is the VH pin voltage (Figure 11)
R_S is the sense resistor (Figure 11)

To adjust the over current limiter level to perform soft start function and over current protection switching at the input voltage.
In such cases, V_{LIM1A}, V_{LIM1B}, V_{LIM2A}, V_{LIM2B} is as follows.

Table 1. Over Current Protection Voltage

Soft Start	AC = 100 V		AC = 230 V	
	V_{LIM1A}	V_{LIM2A}	V_{LIM1B}	V_{LIM2B}
Start to 0.5 ms	0.063 V (12 %)	0.016 V (3 %)	0.044 V (10 %)	0.011 V (2 %)
0.5 ms to 1 ms	0.125 V (25 %)	0.032 V (6 %)	0.088 V (20 %)	0.022 V (4 %)
1 ms to 2 ms	0.250 V (50 %)	0.063 V (12 %)	0.175 V (40 %)	0.044 V (9 %)
2 ms to 4 ms	0.375 V (75 %)	0.094 V (19 %)	0.263 V (60 %)	0.066 V (13 %)
4 ms to	0.500 V (100 %)	0.125 V (25 %)	0.350 V (70 %)	0.087 V (18 %)

() is shown comparative value with V_{LIM1A} in AC = 100 V and normal operation.
The difference between AC100 V and AC230 V is the CS current switching function shown in (5.3).

5 DC/DC Converters Function - continued

5.2 L.E.B. (Leading Edge Blanking) Function

When the MOSFET for switching is turned ON, surge current occurs in cause of capacitance or rush current. Therefore, when the CS pin voltage rises temporarily, over current limiter circuit may miss detections.
To prevent miss detections, the IC build in blanking function. This function masks the CS pin voltage for t_{LEB} after the OUT pin switches to L→H.
This blanking function can reduce the noise filter of the CS pin.
However, if the CS pin noise does not converge less than 250 ns, attach an RC filter to the CS pin as shown in Figure 14. At this time, delay time occurs to the CS pin detection by RC filter.
Also, even if the filter in not attached, it is recommended that it is attached R_{CS} to the CS pin as surge provision.
R_{CS} recommended resistor value is 1 kΩ. If you want to filter, adjust the resistor with C_{CS}.

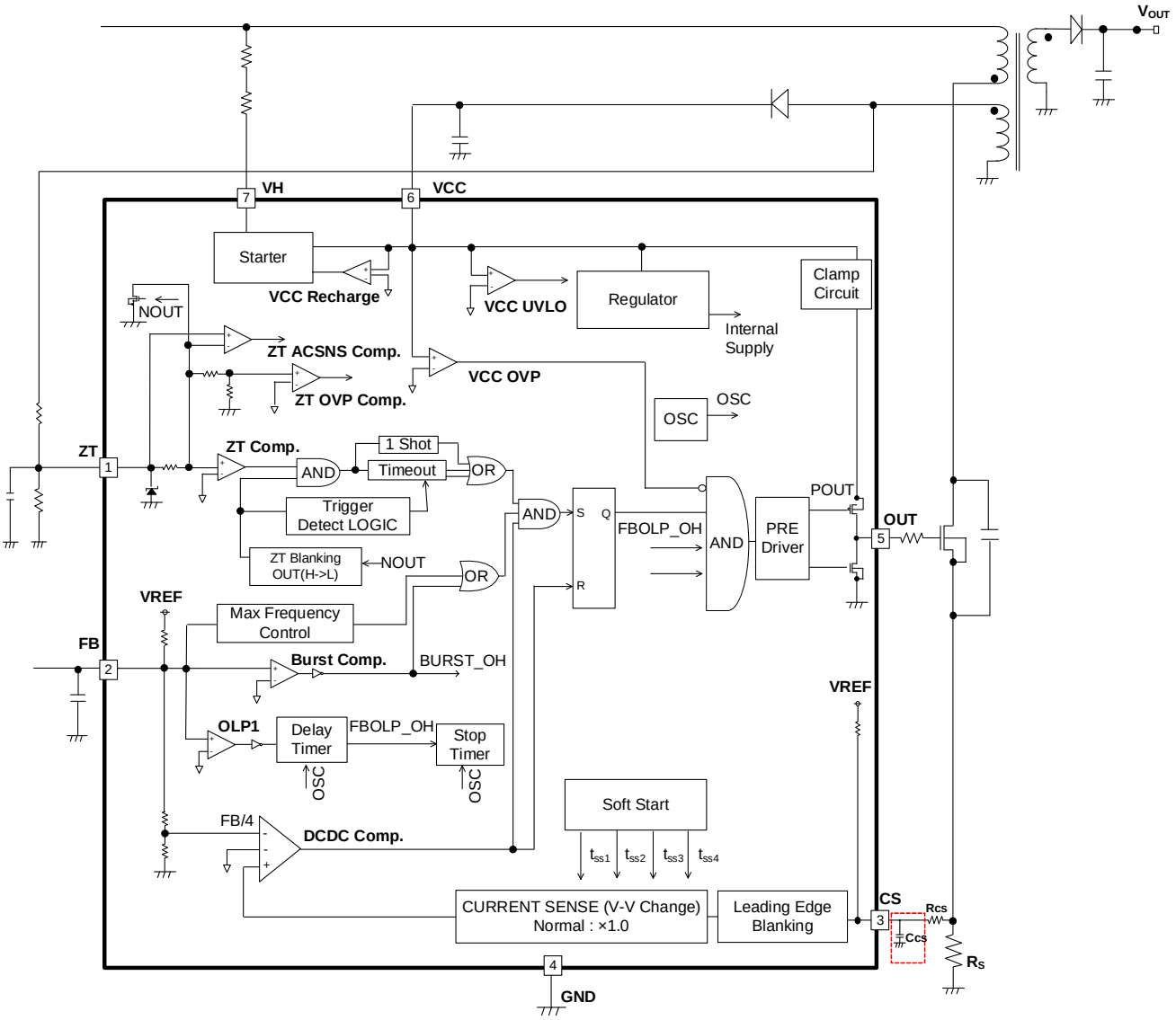


Figure 14. CS Pin Peripheral Circuit

5 DC/DC Converters Function - continued

5.3 CS Over Current Protection Switching Function

As the input voltage (VH) increases, the ON time decreases and the operating frequency also increases. As a result, the maximum capable power is increased for constant over current limiter. Therefore, it takes measures with switched the over current protection function inside the IC. In case of high voltage, set the over current limiter level that determines the ON time to 0.7 times the normal level.
The ZT pin detects an over current by monitoring the ZT inflow current and switches the protective function.
When MOSFET turns ON, the auxiliary winding voltage V_b has negative voltage to be affected input voltage VH. The ZT pin is clamped inside the IC around 0 V. The calculation formula in that case is shown below.
Figure 15 shows block diagram and Figure 16, Figure 17 shows the charts.

$$I_{ZT} = (V_b - V_{ZT})/R_{ZT1} = V_b/R_{ZT1} = (VH \times N_b)/(N_p \times R_{ZT1}) \quad [A]$$

$$R_{ZT1} = V_b/I_{ZT} \quad [\Omega]$$

Where:
I_{ZT} is the ZT inflow current
V_b is the auxiliary winding voltage
V_{ZT} is the ZT pin voltage
R_{ZT1} is the ZT pin resistor 1
VH is the input voltage
N_p is the primary winding
N_b is the auxiliary winding

From the above, set the input voltage VH with the resistor value of R_{ZT1}. At this time, set the timing with C_{ZT} because the ZT bottom detection voltage is determined.
The ZT current switched CS has I_{ZTHYS} hysteresis. Once the ZT pin current exceeds I_{ZT1} and is detected by the comparator, the gain is 0.7 times until it drops to I_{ZT2}.

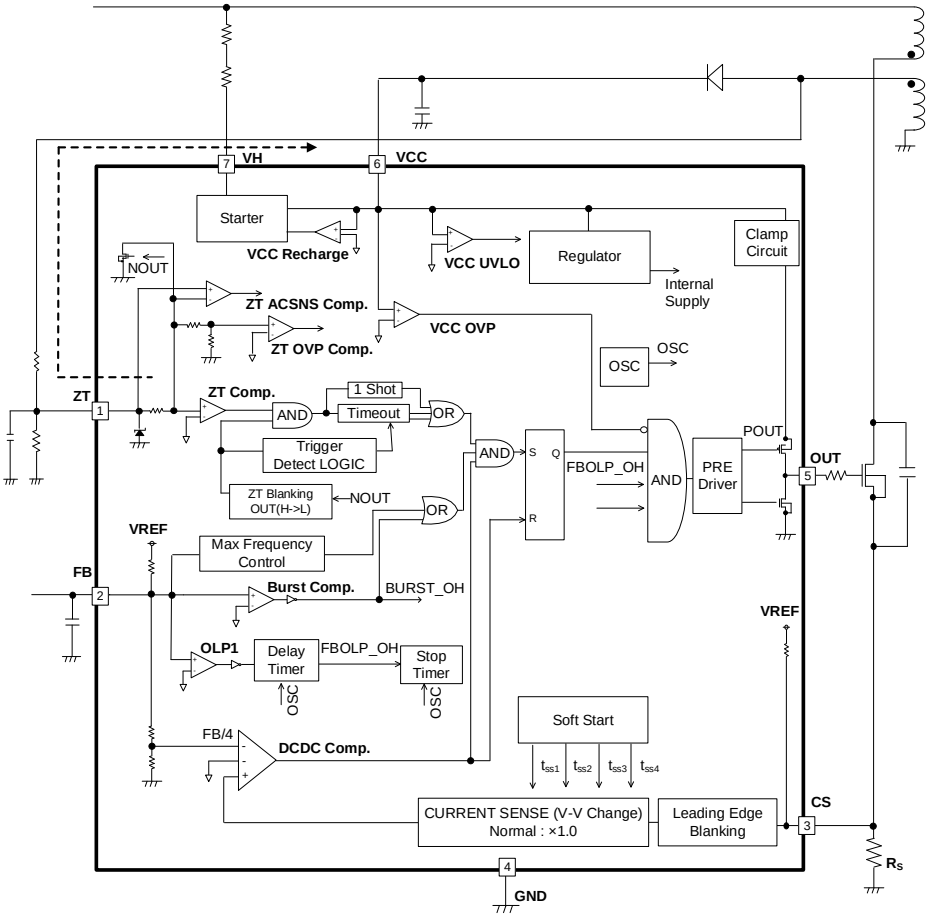


Figure 15. Block Diagram of CS Switching Current

5.3 CS Over Current Protection Switching Function - continued

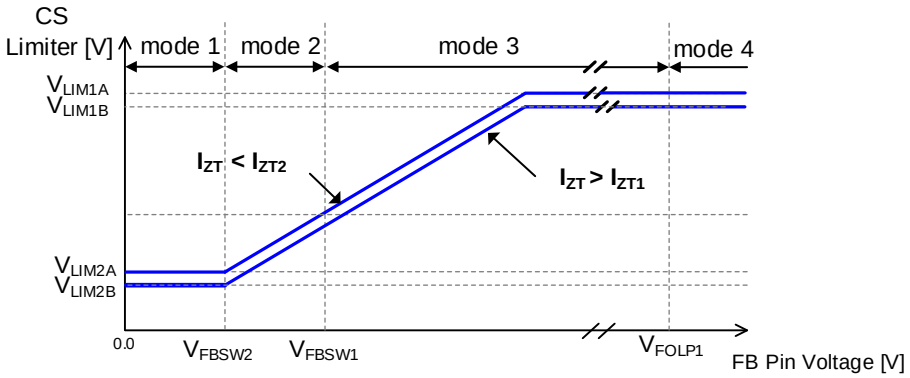


Figure 16. CS Switching: CS Limiter vs FB Pin Voltage

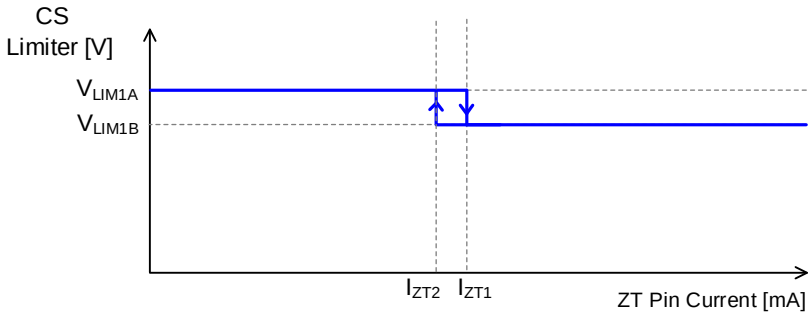


Figure 17. CS Switching: CS Limiter vs ZT Pin Current

ex) Setting Method (Switch between AC100 V and AC230 V.)
AC100 V system 141 V ± 28 V (±20 % margin)
AC230 V system 325 V ± 65 V (±20 % margin)
In the above case, set to switch the CS detection current between 169 V and 260 V. For example, when performing the switching of AC230 V from AC100 V at VH = 214 V, N_p = 100, and N_b = 15.

$$V_b = V_{IN} \times N_b/N_p = 214\,V \times 15/100 \times (-1) = -32.1 \quad [V]$$

$$R_{ZT1} = V_b/I_{ZT} = -32.1\,V/-1\,mA = 32.1 \quad [k\Omega]$$

Where:
V_b is the auxiliary winding voltage
V_{IN} is the input voltage
N_p is the primary winding
N_b is the auxiliary winding
R_{ZT1} is the ZT pin resistor
I_{ZT} is the ZT pin inrush current

Therefore, set R_{ZT1} = 32 kΩ.

5 DC/DC Converters Function - continued

5.4 Determination of OFF Width (Turn ON)

The OFF width is controlled at the ZT pin. While switching is OFF, the power stored in the coil is supplied to the secondary output capacitor. When the supply is completed, there is no current flowing to the secondary side. For that reason, the drain voltage of the switching MOSFET drops. Therefore, the voltage on the auxiliary winding side also drops.
The ZT pin is powered by the voltage divided by R_{ZT1} and R_{ZT2}. When the voltage drops V_{ZT1} or below, switching is turned ON by the ZT comparator.
To detect zero currents in the ZT pin, a time constant is created by C_{ZT} and R_{ZT1}, R_{ZT2}. However, since R_{ZT1} and R_{ZT2} must be set by the AC voltage compensation function and ZT OVP function, the bottom time adjustment is C_{ZT} setting. t_{OFF1} is calculated by the following equation.

$$t_{OFF1} = \frac{L_S}{V_{OUT} + V_F} \times I_S$$

Where:
t_{OFF1} is the transformer discharge time
L_S is the secondary inductance value
V_{OUT} is the output voltage
V_F is the forward voltage of the diode on the secondary side
I_S is the secondary peak current

For this reason, the switching frequency is as follows.

$$f_{SW} = 1/\{(t_{ON} + t_{OFF1}) + (N - 1) \times t_R + 1/2 \times t_{QR}\}$$
$$t_{QR} = 2 \times \pi \times \sqrt{L_p \times C_{ds}}$$

Where:
f_{SW} is the switching frequency
N is the number of bottoms
t_{QR} is the resonance time
L_p is the primary inductance value
C_{ds} is the MOSFET DRAIN – SOURCE capacitance

The low load frequency reduction period has a limit as shown in Figure 13, so the bottom detection operation is performed at a frequency lower than the frequency indicated by Figure 13.
In addition, the ZT pin has a built-in ZT trigger mask function and ZT trigger timeout function.

5.5 ZT Trigger Mask Function

Noise may be superimposed on the ZT pin when switching is turned from ON to OFF. In this case, the ZT comparator is masked during t_{ZTMASK} to prevent ZT comparator operation errors. This is shown in Figure 18.

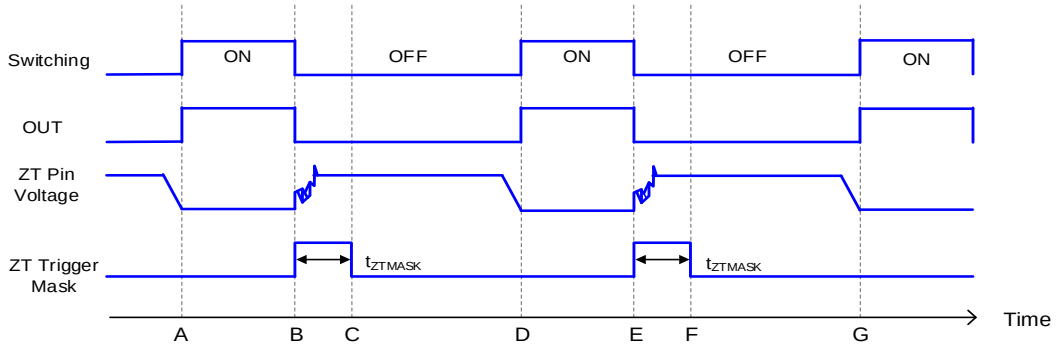


Figure 18. ZT Pin Trigger Mask Function

A: The OUT output is turned high, switching is turned ON.
B: The OUT output goes low, switching is turned OFF. At this time, the surge noise occurs to the ZT pin, but the ZT comparator does not operate during t_{ZTMASK}.
C: t_{ZTMASK} ends.
D: Same as A.
E: Same as B.
F: Same as C.
G: Same as A.

5 DC/DC Converters Function - continued

5.6 ZT Trigger Timeout Function

ZT Trigger Timeout Function 1

This is a function that forcibly turns ON switching when the ZT pin voltage does not become higher than V_{ZT2} during t_{ZTOUT1} due to a drop in the output voltage or a short at the ZT pin such as at startup.

ZT Trigger Timeout Function 2

This function forces switching to ON when the following is not detected in t_{ZTOUT2} after the ZT comparator detects the bottom. This function operates after the ZT comparator detects a signal once. It does not operate at startup or when the output voltage drops. This function works when the auxiliary winding voltage is attenuated and the bottom cannot be detected.

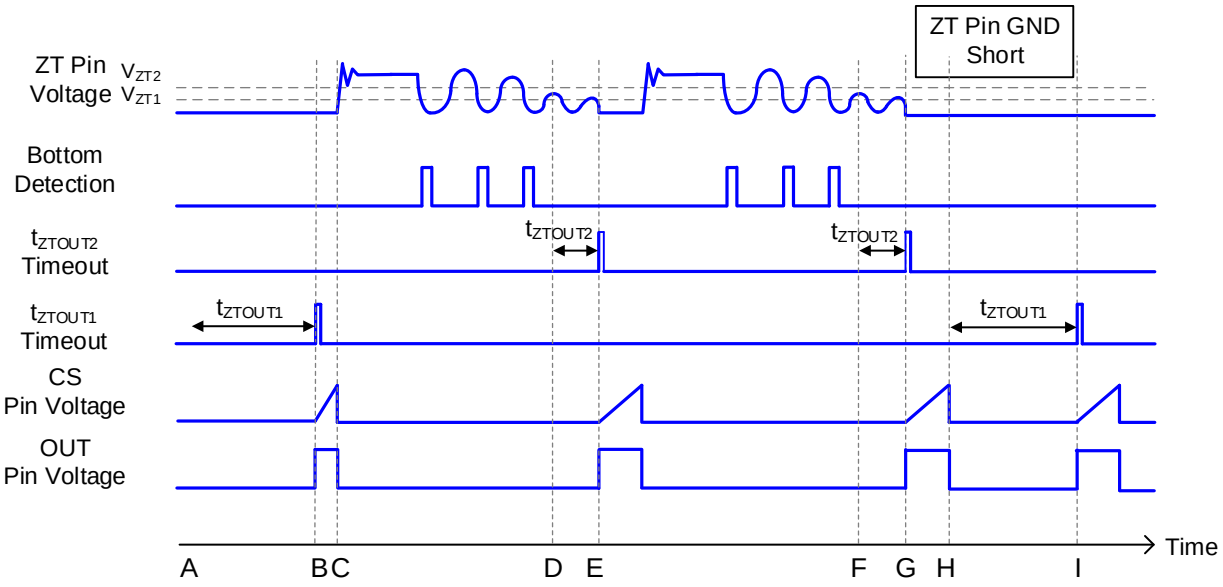


Figure 19. ZT Pin Trigger Timeout Function

A: At startup, IC starts to operate by the ZT trigger timeout function 1 because the ZT pin voltage < V_{ZT2} during t_{ZTOUT1}.
B: The OUT pin voltage turns ON.
C: The OUT pin voltage turns OFF.
D: The maximum value of the ZT pin voltage becomes lower than V_{ZT2} due to vibration damping.
E: The OUT pin voltage turned ON after t_{ZTOUT2} from the point of D by the ZT trigger timeout function 2.
F: Same as D.
G: The OUT pin voltage turned ON after t_{ZTOUT2} from the point of F by the ZT trigger timeout function 2.
H: The ZT pin and GNDs are short circuited.
I: The OUT pin voltage turned ON after t_{ZTOUT1} by the ZT trigger timeout function 1.

Description of Blocks - continued

6 Soft Start Function

Normally, when the AC voltage is applied, a large current flow through AC/DC power supply. This IC has a built-in soft start function to prevent large changes in the output voltage and output current during startup. This function is reset when the VCC pin voltage falls V_{UVLO2} or below, and soft start is executed at the next AC power on.

The soft start function performs the following operations after starting. (Refer to 5.1)
Start to t_{SS1} → Sets CS limiter to 12.5 % when normal.
t_{SS1} to t_{SS2} → Sets CS limiter to 25 % when normal.
t_{SS2} to t_{SS3} → Sets CS limiter to 50 % when normal.
t_{SS3} to t_{SS4} → Sets CS limiter to 75 % when normal.
t_{SS4} to → Normal operation

7 ZT OVP

ZT OVP is detected when the ZT pin voltage > V_{ZTL}.
BM1Q002AFJ-LB is latch operation and BM1Q021AFJ-LB is auto restart operation.
BM1Q002AFJ-LB has a built-in mask time t_{LATCH}. This function masks surges that occur at the pin. This t_{LATCH} is built-in VCC OVP.
When BM1Q021AFJ-LB is ZT OVP protected, switching is stopped for t_{ZTOVP}. After $t_{ZTOVP,}$ switching restarts.
ZT OVP supports DC detection and pulse detection for the ZT pin.

7.1 DC Detection

In the case of BM1Q002AFJ-LB, switching stops when the ZT pin Voltage > V_{ZTL} continues for $t_{LATCH.}$
in the case of BM1Q021AFJ-LB, switching stops when the ZT pin Voltage > V_{ZTL} continues for t_{ZTMASK}.
The operation of BM1Q002AFJ-LB is shown in Figure 20.

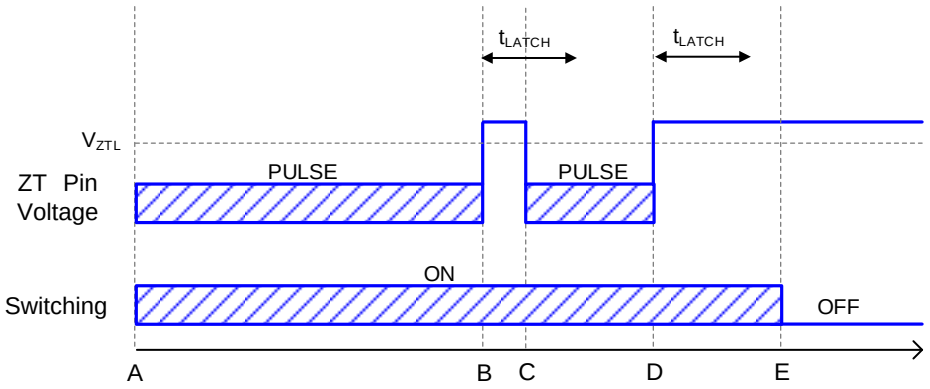


Figure 20. ZT OVP and Latch Mask Function

A: Switching turn ON and the ZT pin voltage starts pulsed operation.
B: The ZT pin voltage is higher than V_{ZTL}.
C: The ZT pin voltage > V_{ZTL} status is within t_{LATCH}, so switching resumes normal operation.
D: Same as B.
E: The ZT pin voltage > V_{ZTL} status continued for t_{LATCH}, so switching turn OFF to operate latched.

7 ZT OVP - continued

7.2 Pulse Detection

The ZT pin voltage > V_{ZTL} pulse detects 3 pulses. Switching stops when BM1Q002AFJ-LB is detected for t_{LATCH} or BM1Q021AFJ-LB is continuously detected for t_{ZTMASK}. Figure 21 shows the time chart of the latch mode of ZT OVP pulse detection, and Figure 22 shows the time chart of the auto restart mode of ZT OVP pulse detection.

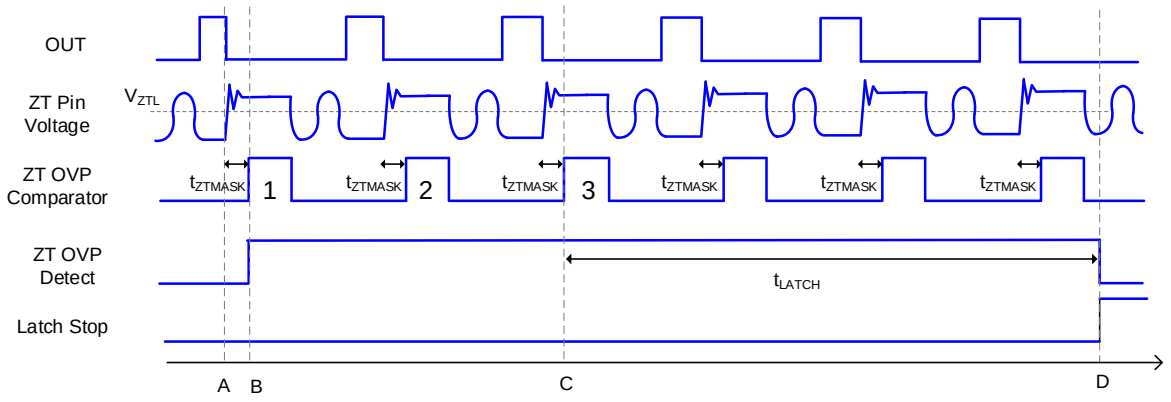


Figure 21. ZT OVP Pulse Detection (Latch)

A: The OUT pin H→L, ringing occurs in the ZT pin, but ZT OVP is not detected by t_{ZTMASK}.
B: ZT OVP is detected by ZT OVP comparator when the ZT pin voltage > V_{ZTL} after t_{ZTMASK} has elapsed from A.
C: B is detected consecutively in three occurrences, the timer t_{LATCH} starts operating.
D: Switching is stopped by ZT OVP when it continues t_{LATCH} from C.

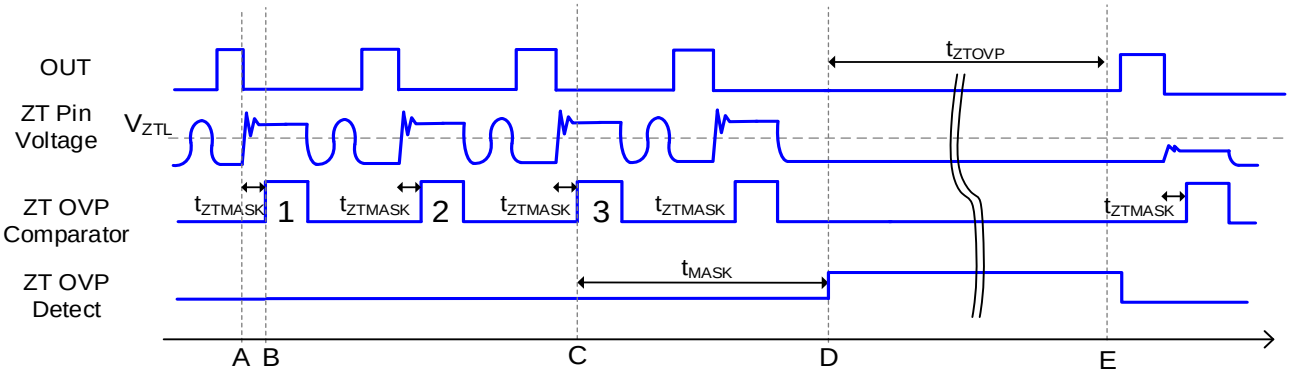


Figure 22. ZT OVP Pulse Detection (Auto Restart)

A: The OUT pin H→L, the ZT pin is ringed, but t_{ZTMASK} does not detect any ZT OVP.
B: ZT OVP is detected by ZT OVP comparator when the ZT pin voltage > V_{ZTL} after t_{ZTMASK} has elapsed from A.
C: B is detected consecutively in three occurrences, the timer t_{MASK} starts operating.
D: Switching is stopped by ZT OVP when pulsing continues for t_{MASK}.
E: Switching starts again after t_{ZTOVP} has elapsed.

ZT OVP voltage setting procedure is as follows.

$$V_{OVP} = \left(\frac{N_b}{N_S}\right) \times V_b = \left(\frac{N_b}{N_S}\right) \times \{V_{ZT} \times (R_{ZT1} + R_{ZT2})/R_{ZT2} + R_{ZT1} \times I_{ZT}\}$$

Where:
V_b is the auxiliary winding voltage
R_{ZT1} is the ZT upper resistor
R_{ZT2} is the ZT lower resistance
N_b/N_s is the transformer winding number ratio (secondary side auxiliary winding)
I_{ZT} is the ZT inflow current
V_{OVP} is the voltage for which over voltage protection is to be applied on the secondary side

7.2 Pulse Detection - continued

Because I_{ZT3} (max) = 28 μA when the ZT pin voltage = 5.35 V, the OVP voltage max is as follows:

$$V_{OVP}\ (\max) = \left(\frac{N_b}{N_s}\right) \times \{5.3 \times (R_{ZT1} + R_{ZT2})/R_{ZT2} + R_{ZT1} \times 28\ \mu A\}$$

R_{ZT1} setting is determined by the AC voltage compensation function in (5.3). R_{ZT2} setting is calculated by the following equation.

$$R_{ZT2} = V_{ZTOVP} \times R_{ZT1}/\{V_{OVP} \times \left(\frac{N_b}{N_s}\right) - I_{ZT} \times R_{ZT1} - V_{ZTOVP}\}$$

8 Overload Protection Function (FB Over Limited Protection)

The overload protection function operates in auto restart mode. This function monitors the overload status of the secondary side output current with the FB pin and fixes the OUT pin to L in the event of an overload condition. In the overload condition, no current flows to the photocoupler, and the FB pin voltage rises. If this condition persists for a t_{FOLP} period, it is judged as an overload condition and the OUT pin is fixed to L. The overload protection timer is reset when the FB pin voltage exceeds V_{FOLP1} and then drops below V_{FOLP2} in t_{FOLP}.
At startup, the FB pin voltage is pulled up by a resistor to the internal voltage, so it operates from a voltage equal to or higher than V_{FOLP1}. Therefore, the FB pin must be designed to be less than or equal to V_{FOLP2} within t_{FOLP}. In other words, the start time of the secondary output voltage should be set within t_{FOLP} after the IC is activated.
After the overload is detected, t_{OLPST} is stopped, and then auto restart is performed. In this case, perform a soft start. When stopped, the VCC pin voltage drops, but the VCC pin voltage is charged by starter circuit so that the VCC pin voltage > V_{UVLO2} is kept.

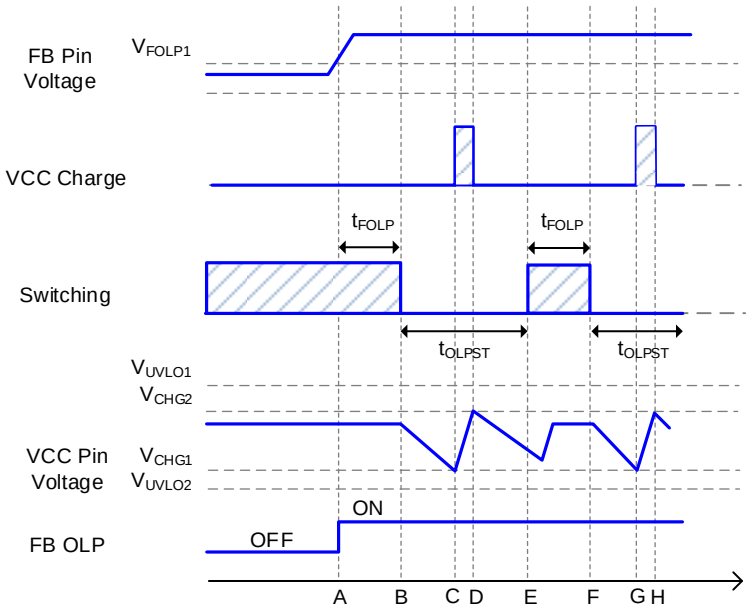


Figure 23. Overload Protection Auto Restart

A: FB OLP comparator detects an overload because the FB pin voltage > V_{FOLP1}.
B: If the status of A lasts for t_{FOLP} period, switching is stopped by overload protection.
C: When switching is stopped due to overload protection, if the VCC pin voltage drops to the VCC pin voltage < V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
D: The VCC charge function stops when the VCC pin voltage > V_{CHG2} due to the VCC charge function.
E: When t_{OLPST} elapses from B, switching starts with a soft start operation.
F: If the overload condition persists, the FB pin voltage > V_{FOLP1} status continues and switching is stopped after t_{FOLP} period from E.
G: When switching is stopped and the VCC pin voltage drops to the VCC pin voltage < V_{CHG1}, the VCC charge function operates and the VCC pin voltage rises.
H: The VCC charge function stops when the VCC pin voltage > V_{CHG2} due to the VCC charge function.

Description of Blocks - continued

9 The CS Pin Open Protection

When the CS pin is turned open, a CS pin open circuit is built-in to prevent the OUT pin from malfunctioning due to noises. This function stops switching the OUT pin when the CS pin is open. (Auto restart protection)

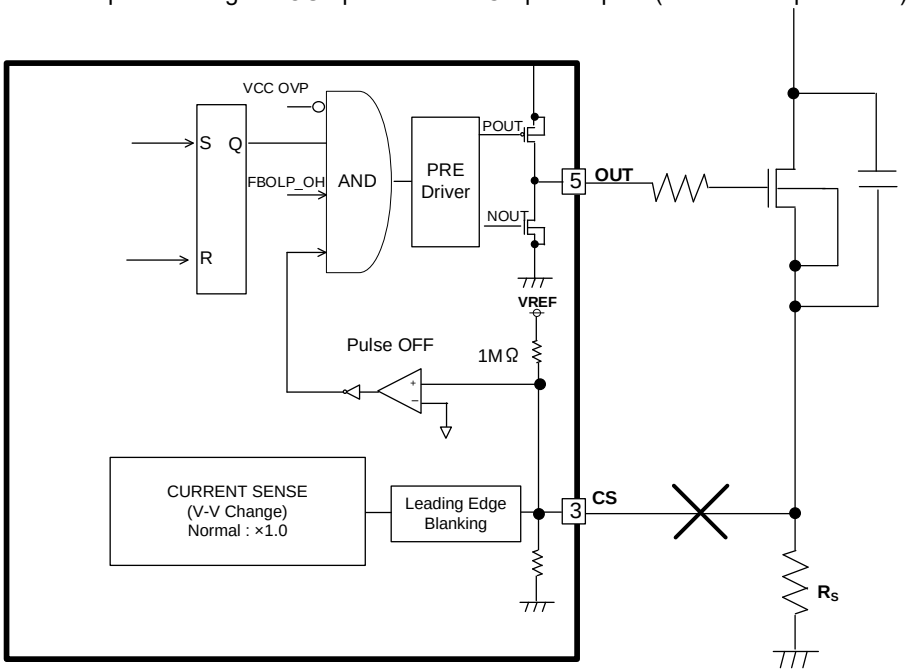


Figure 24. CS Open Protection Circuit

10 The OUT Pin Clamping Function

Clamps the H level of the OUT pin to V_{OUTH} to protect the external MOSFET. This function prevents MOSFET gate breakage due to increasing the VCC pin voltages. This is shown in Figure 25. The OUT pin has a R_{PDOUT} pull down internally.

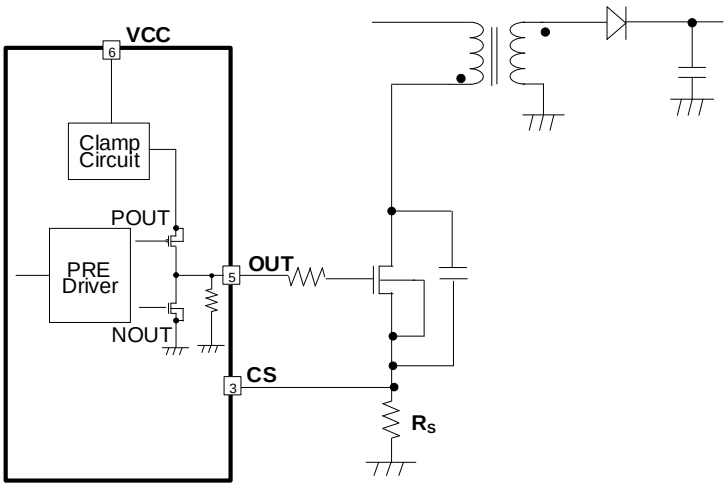


Figure 25. OUT Pin Clamp Circuit

Operation Mode of the Protection Function

Table 2 shows the operation modes of the protective functions.

Table 2. Operation Modes of Protection Circuit

Parameter	Protective Operation Mode	
	BM1Q002AFJ-LB	BM1Q021AFJ-LB
VCC UVLO	Auto Restart	Auto Restart
VCC OVP	Latch	Auto Restart
FB OLP	Auto Restart	Auto Restart
CS Open Protection	Auto Restart	Auto Restart
ZT OVP	Latch	Auto Restart
VCC Charge Function	Auto Restart	Auto Restart

Thermal Dissipation

Operate under the following conditions in thermal design.
(The following temperatures are guaranteed temperatures. Be sure to consider such as a margin.)

1. The ambient temperature Ta must be 105 °C or below.
2. The power dissipation of the IC is below or equal to the power dissipation Pd.

Thermal derating characteristics are shown in Figure 26.
(At mounting on a glass epoxy single layer PCB which size is 74.2 mm x 74.2 mm x 1.6 mm)

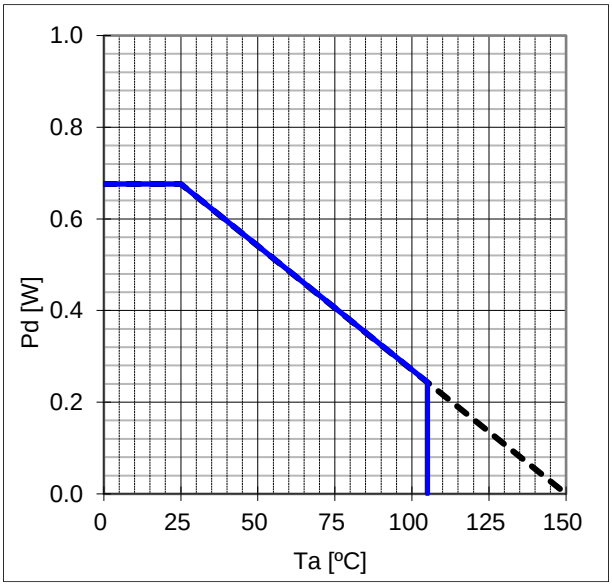


Figure 26. SOP-J7S Thermal Dissipation Characteristics

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Conditions
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +32.0	V	VCC pin
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +6.5	V	CS pin, FB pin
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +15.0	V	OUT pin
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +650	V	VH pin
Power Dissipation	Pd	0.67	W	*(Note 1)*
OUT Pin Out Peak Current1	I_{OH}	-0.5	A	
OUT Pin Out Peak Current2	I_{OL}	1.0	A	
ZT Pin Maximum Current	I_{SZT}	±3.0	mA	
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) At mounted on a glass epoxy single layer PCB (74.2 mm x 74.2 mm x 1.6 mm). Derate by 5.4 mW/°C if the IC is used in the ambient temperature 25 °C or above.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating Power Supply Voltage Range 1	V_{CC}	8.9	-	26.0	V	VCC pin voltage
Operating Power Supply Voltage Range 2	VH	-0.3	-	+650	V	VH pin voltage
Operating Temperature	Topr	-40	-	+105	°C	

Electrical Characteristics (V_{CC} = 15 V, Ta = 25 °C, Unless Otherwise Specified)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Circuit Current]						
Current at Switching Operation	I_{ON1}	-	600	1000	µA	FB pin voltage = 2.0 V (At switching operation)
Current at Burst Operation	I_{ON2}	-	350	450	µA	FB pin voltage = 0.5 V (At switching operation OFF)
Circuit Current (OFF)	I_{OFF}	-	-	25	µA	VCC pin voltage = 12 V, VH open VCC UVLO = disable
[VH Pin Starter Circuit]						
VH Start Current 1	I_{START1}	0.4	0.7	1.0	mA	VCC pin voltage = 0 V
VH Start Current 2	I_{START2}	1.0	3.0	6.0	mA	VCC pin voltage = 10 V
VH OFF Current	I_{START3}	-	10	20	µA	After releasing VCC UVLO VH pin inrush current
VH Start Current Switched Voltage	V_{SC}	0.40	0.80	1.40	V	VCC pin
[VCC Pin Protective Function]						
VCC UVLO Voltage 1	V_{UVLO1}	12.50	13.50	14.50	V	At VCC pin rising
VCC UVLO Voltage 2	V_{UVLO2}	7.50	8.20	8.90	V	At VCC pin falling
VCC UVLO Hysteresis	V_{UVLO3}	-	5.30	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC Recharge Start Voltage	V_{CHG1}	7.70	8.70	9.70	V	Starter circuit operating voltage
VCC Recharge End Voltage	V_{CHG2}	12.00	13.00	14.00	V	Stop voltage from V_{CHG1}
VCC OVP Voltage 1	V_{OVP1}	26.00	27.50	29.00	V	At VCC pin voltage rising
VCC OVP Voltage 2	V_{OVP2}	-	23.50	-	V	At VCC pin voltage falling (BM1Q021AFJ-LB only)
VCC OVP Hysteresis	V_{OVP3}	-	4.00	-	V	(BM1Q021AFJ-LB only)
[OUT Pin]						
OUT Pin H Voltage	V_{OUTH}	10.5	12.5	14.5	V	I_O = -20 mA, VCC pin voltage = 15 V
OUT Pin L Voltage	V_{OUTL}	-	-	0.30	V	I_O = +20 mA
OUT Pin Pull Down Resistor	R_{PDOUT}	75	100	125	kΩ	-

Electrical Characteristics (V_{CC} = 15 V, Ta = 25 °C, Unless Otherwise Specified) - continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[DC/DC Converter Unit (Turn OFF)]						
FB Pin Pull Up Resistor	R_{FB}	22.5	30.0	37.5	kΩ	-
CS Over Current Detection Voltage 1A	V_{LIM1A}	0.475	0.500	0.525	V	FB pin voltage = 2.2 V (ACSNS = L) *(Note 1)*
CS Over Current Detection Voltage 1B	V_{LIM1B}	0.310	0.350	0.390	V	FB pin voltage = 2.2 V (ACSNS = H)
CS Over Current Detection Voltage 2A	V_{LIM2A}	0.100	0.125	0.150	V	FB pin voltage = 0.5 V (ACSNS = L)
CS Over Current Detection Voltage 2B	V_{LIM2B}	0.062	0.088	0.113	V	FB pin voltage = 0.5 V (ACSNS = H)
Voltage Gain 1 (⊿VFB/⊿VCS)	AV_{CS1}	3.40	4.00	4.60	V/V	ACSNS = L
Voltage Gain 2 (⊿VFB/⊿VCS)	AV_{CS2}	4.86	5.71	6.57	V/V	ACSNS = H
CS Switched ZT Current 1	I_{ZT1}	0.93	1.00	1.07	mA	-
CS Switched ZT Current 2	I_{ZT2}	0.82	0.90	0.98	mA	-
CS Switched ZT Current Hysteresis	I_{ZTHYS}	-	0.10	-	mA	-
CS Leading Edge Blanking Times	t_{LEB}	-	0.25	-	µs	-
Turn OFF Time	t_{OFF}	-	0.15	-	µs	At PULSE is applied to the CS pin
Minimum ON Width	t_{MIN}	-	0.40	-	µs	t_{LEB} + t_{OFF}
Maximum ON Width	t_{MAX}	30.0	39.0	50.7	µs	-
[DC/DC Converter Unit (Turn ON)]						
ZT Inrush Current 1	I_{ZT1}	4	14	24	µA	OUT pin voltage = L ZT pin voltage = 4.65 V
ZT Inrush Current 2	I_{ZT2}	6	16	26	µA	OUT pin voltage = L ZT pin voltage = 5.00 V
ZT Inrush Current 3	I_{ZT3}	8	18	28	µA	OUT pin voltage = L ZT pin voltage = 5.35 V
Maximum Operating Frequency 1	f_{SW1}	108	120	132	kHz	FB pin voltage = 2.0 V
Maximum Operating Frequency 2	f_{SW2}	21	30	39	kHz	FB pin voltage = 0.5 V
Frequency Reduction Start FB Voltage	V_{FBSW1}	1.10	1.25	1.40	V	-
Frequency Reduction End FB Voltage	V_{FBSW2}	0.42	0.50	0.58	V	-
ZT Comparator Voltage 1	V_{ZT1}	60	100	140	mV	At ZT pin voltage falling
ZT Comparator Voltage 2	V_{ZT2}	120	200	280	mV	At ZT pin voltage rising
ZT Trigger Mask Time	t_{ZTMASK}	-	0.6	-	µs	OUT pin voltage H→L, Prevent noise
ZT Trigger Timeout Time 1	t_{ZTOUT1}	10.5	15.0	19.5	µs	Operation without bottom detection
ZT Trigger Timeout Time 2	t_{ZTOUT2}	3.5	5.0	6.5	µs	Count from final bottom
[DC/DC Protective Function]						
Soft Start Time 1	t_{SS1}	0.35	0.50	0.65	ms	-
Soft Start Time 2	t_{SS2}	0.70	1.00	1.30	ms	-
Soft Start Time 3	t_{SS3}	1.40	2.00	2.60	ms	-
Soft Start Time 4	t_{SS4}	2.80	4.00	5.20	ms	-
FB Burst Voltage	V_{BURST}	0.42	0.50	0.58	V	Burst ON
FB OLP Voltage 1	V_{FOLP1}	2.6	2.8	3.0	V	FB OLP detection (At FB pin voltage rising)
FB OLP Voltage 2	V_{FOLP2}	-	2.6	-	V	FB OLP detection (At FB pin voltage falling)
FB OLP Detection Timer	t_{FOLP}	44.8	64.0	83.2	ms	-
FB OLP Stop Timer	t_{OLPST}	358	512	666	ms	-
Latching Release Voltage (VCC Pin Voltage)	V_{LATCH}	-	V_{UVLO2} – 0.50	-	V	BM1Q002AFJ-LB only
Latch Mask Time	t_{LATCH}	50	100	200	µs	BM1Q002AFJ-LB only
ZT OVP Voltage	V_{ZTL}	4.65	5.00	5.35	V	
ZT OVP Stopping Timer	t_{ZTOVP}	358	512	666	ms	BM1Q021AFJ-LB only

(Note 1) ACSNS is defined. (L: ZT pin current < I_{ZT1}, H: ZT pin current > I_{ZT1})

Typical Performance Curves (Reference Data)

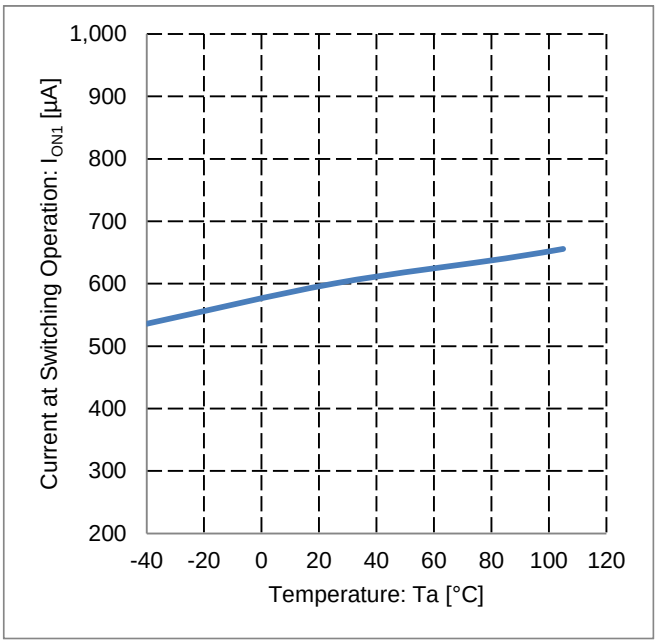


Figure 27. Current at Switching Operation vs Temperature

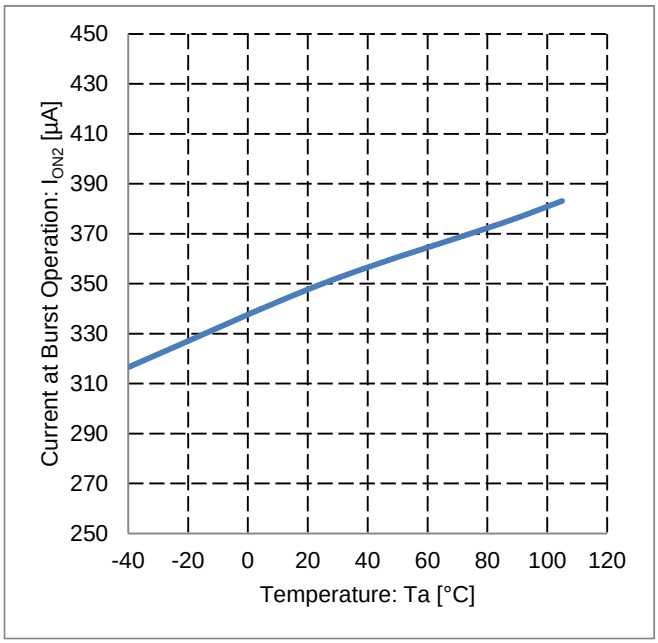


Figure 28. Current at Burst Operation vs Temperature

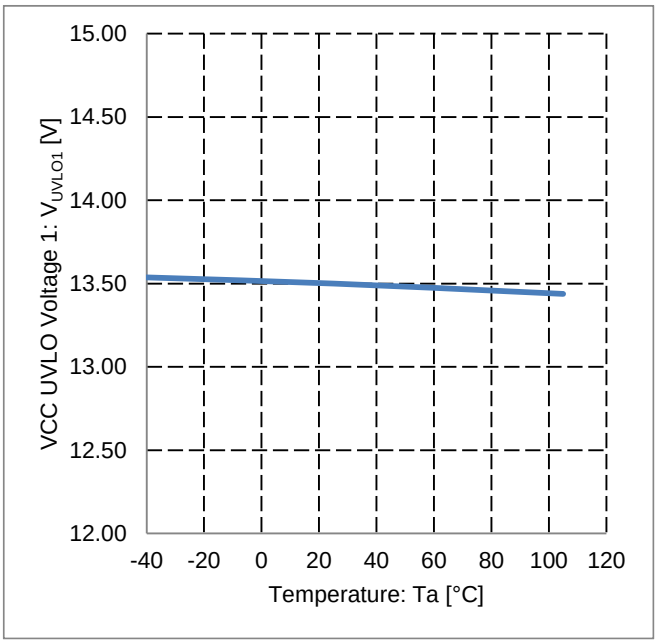


Figure 29. VCC UVLO Voltage 1 vs Temperature

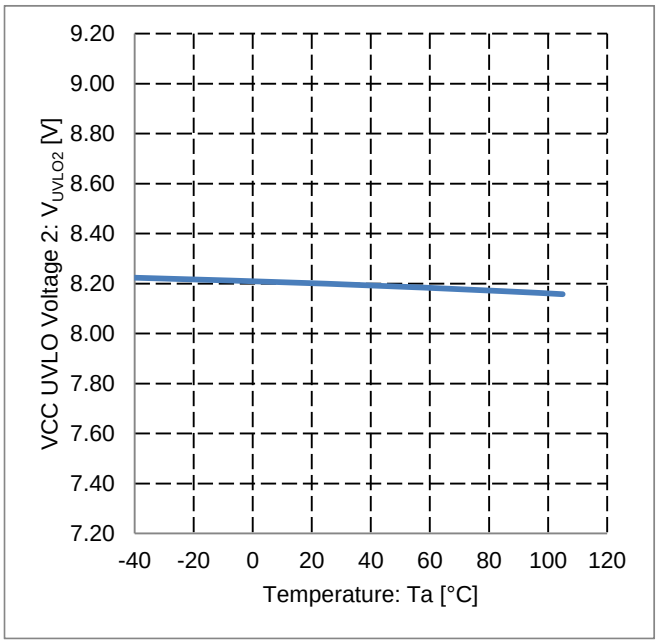


Figure 30. VCC UVLO Voltage 2 vs Temperature

Typical Performance Curves - continued
(Reference Data)

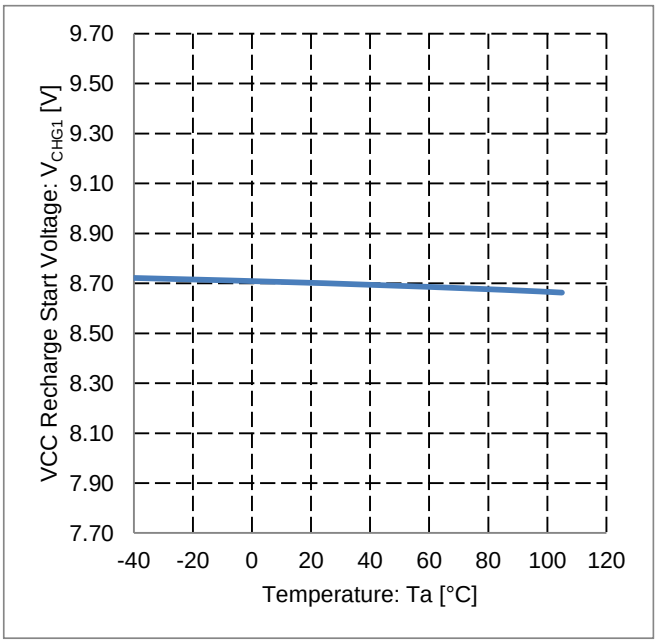


Figure 31. VCC Recharge Start Voltage vs Temperature

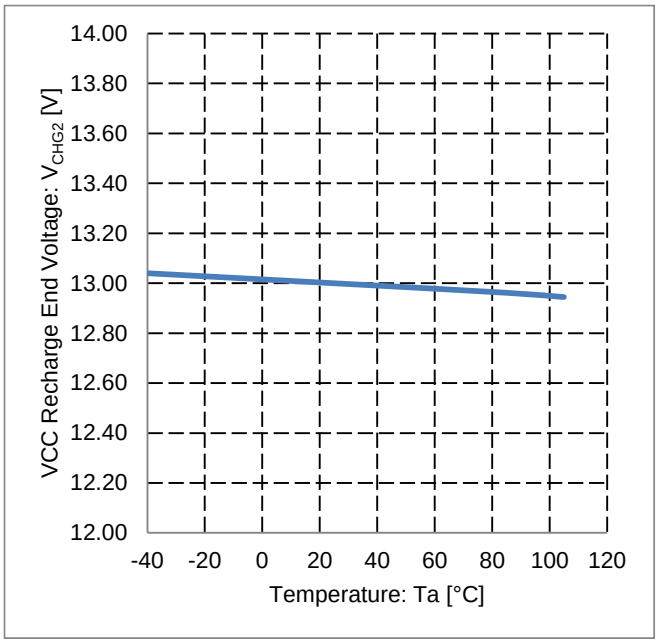


Figure 32. VCC Recharge End Voltage vs Temperature

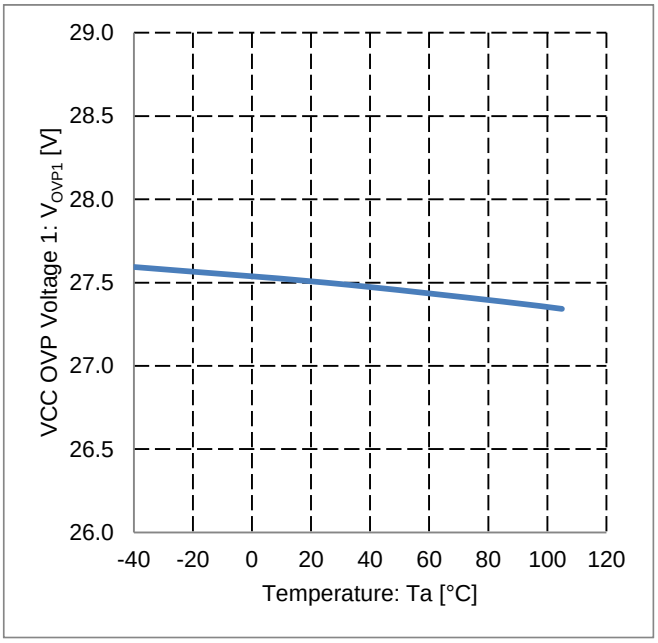


Figure 33. VCC OVP Voltage 1 vs Temperature

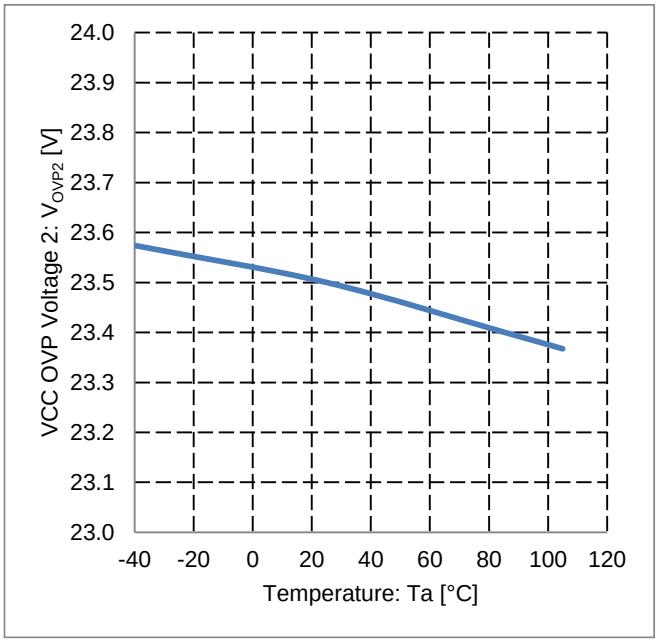


Figure 34. VCC OVP Voltage 2 vs Temperature

Typical Performance Curves - continued
(Reference Data)

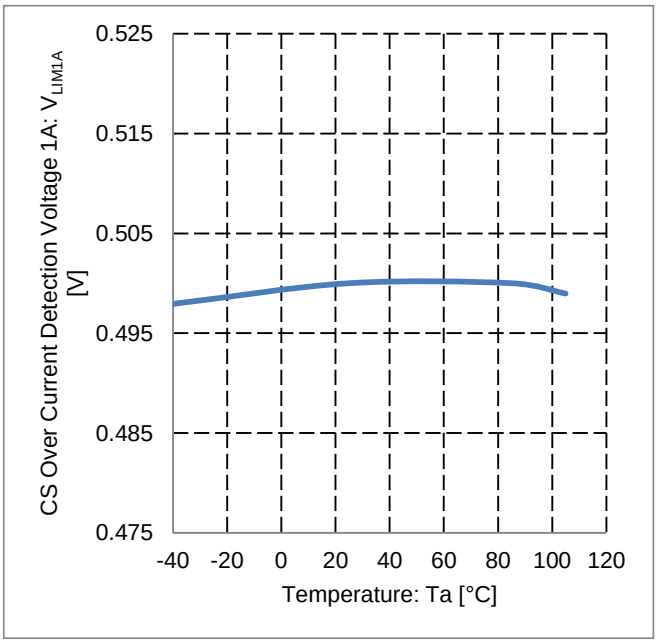


Figure 35. CS Over Current Detection Voltage 1A vs Temperature

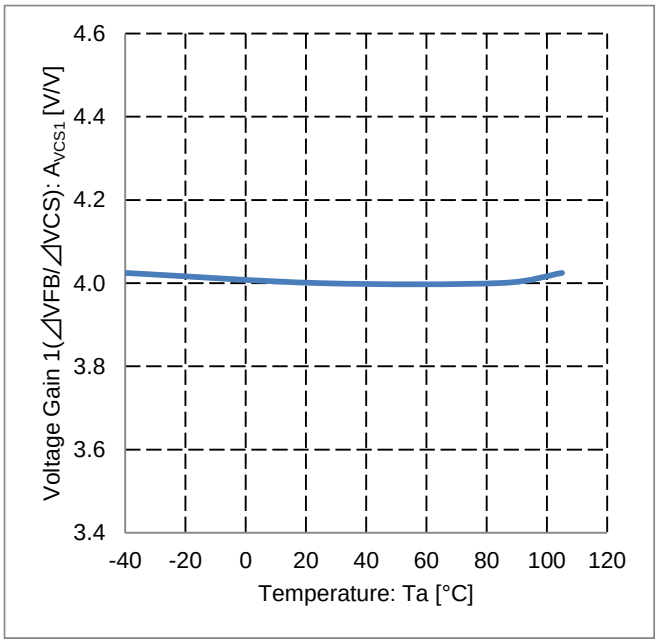


Figure 36. Voltage Gain 1 (⊿VFB/⊿VCS) vs Temperature

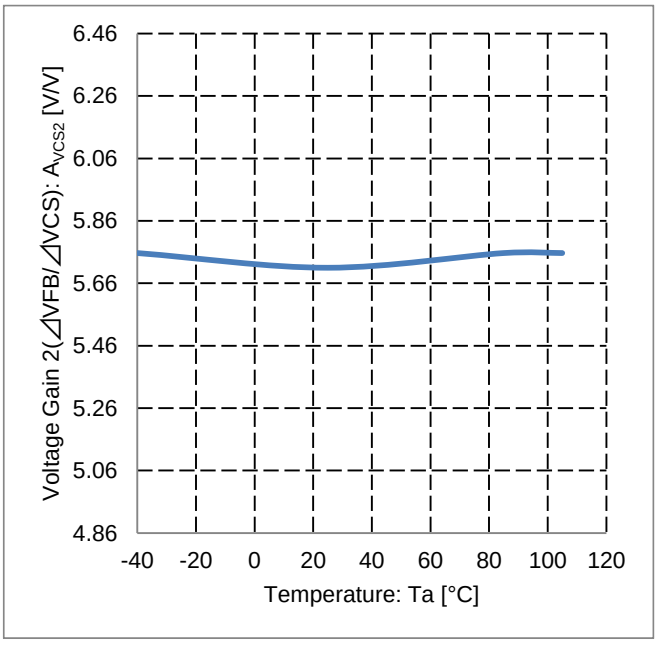


Figure 37. Voltage Gain 2 (⊿VFB/⊿VCS) vs Temperature

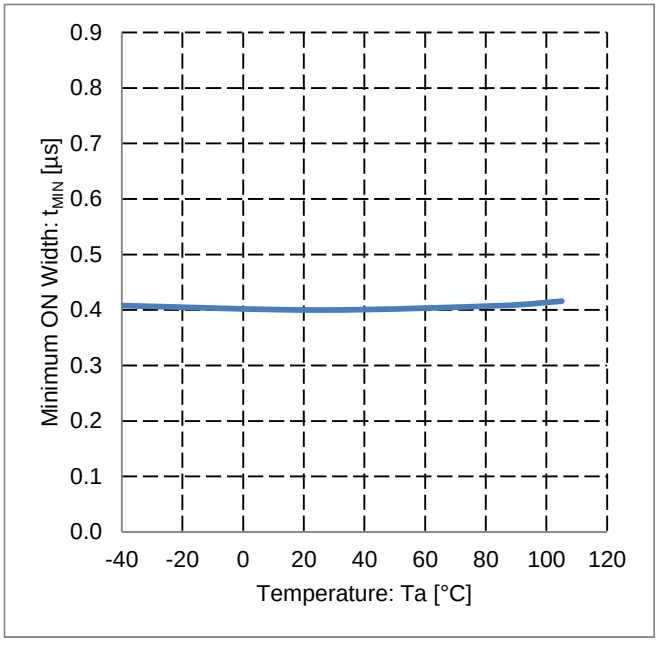


Figure 38. Minimum ON Width vs Temperature

Typical Performance Curves - continued
(Reference Data)

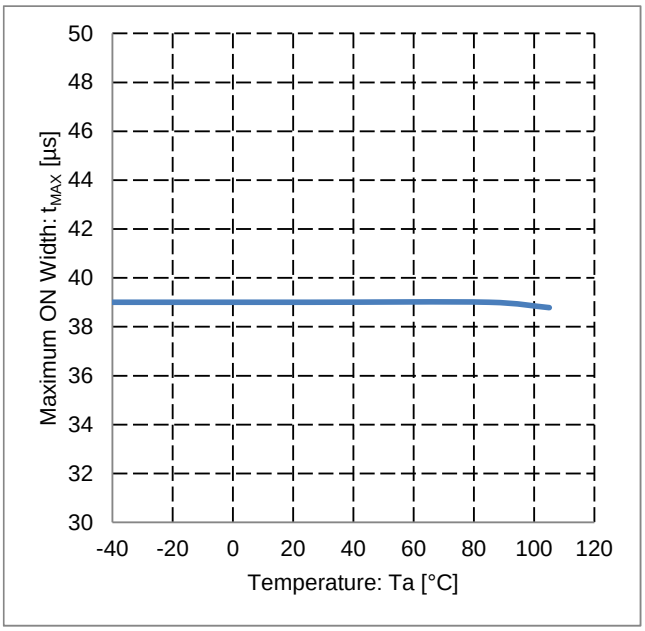


Figure 39. Maximum ON Width vs Temperature

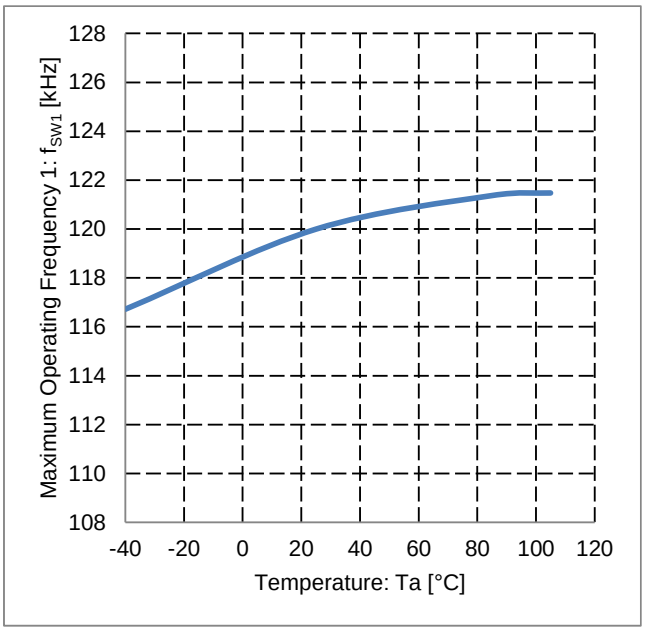


Figure 40. Maximum Operating Frequency 1 vs Temperature

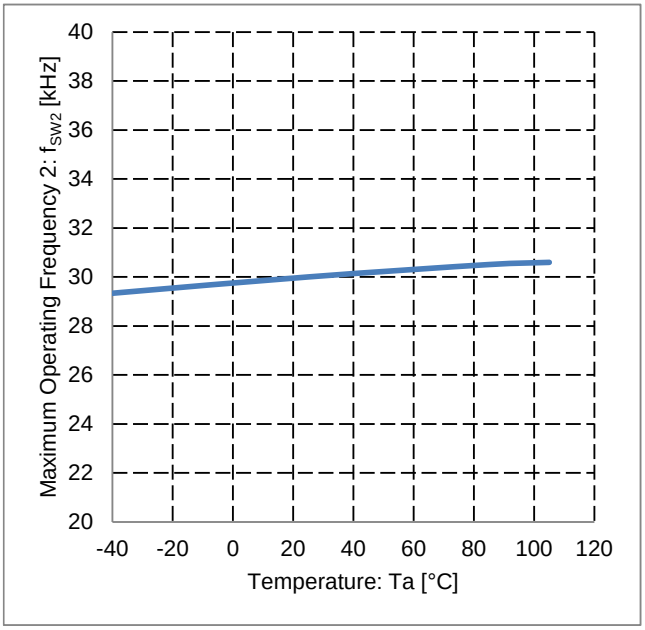


Figure 41. Maximum Operating Frequency 2 vs Temperature

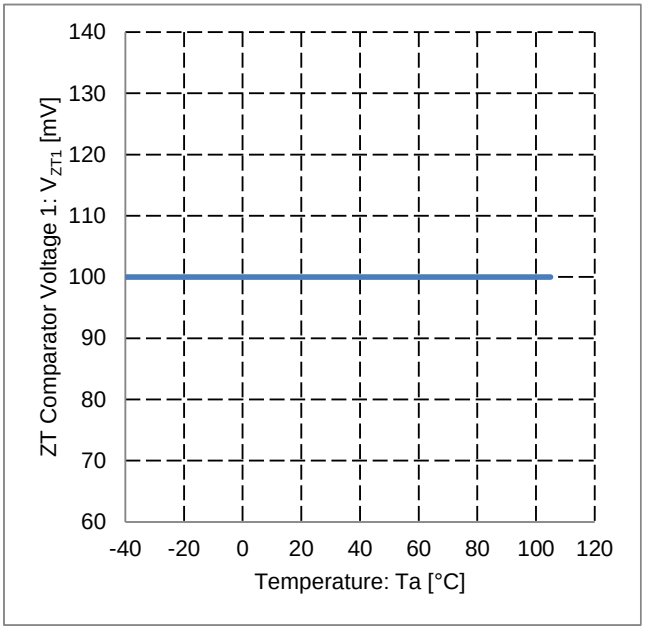


Figure 42. ZT Comparator Voltage 1 vs Temperature

Typical Performance Curves - continued
(Reference Data)

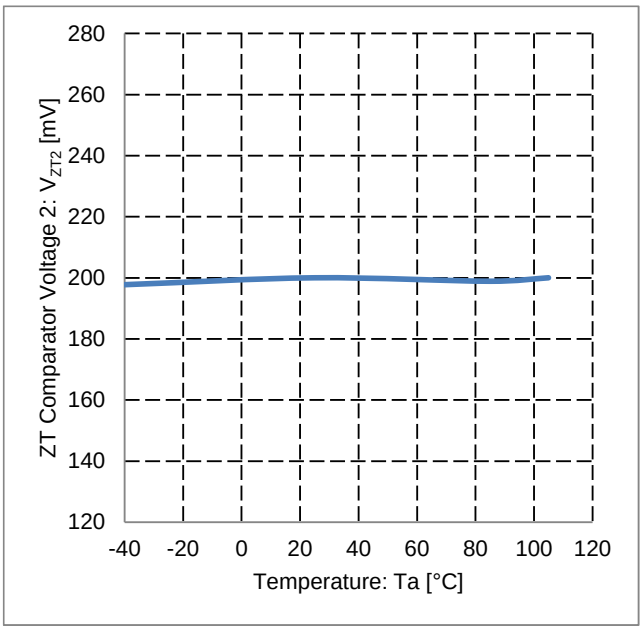


Figure 43. ZT Comparator Voltage 2 vs Temperature

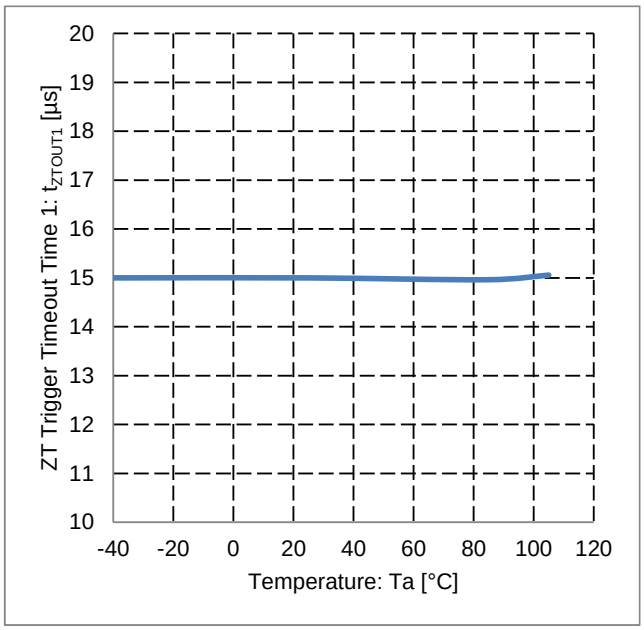


Figure 44. ZT Trigger Timeout Time 1 vs Temperature

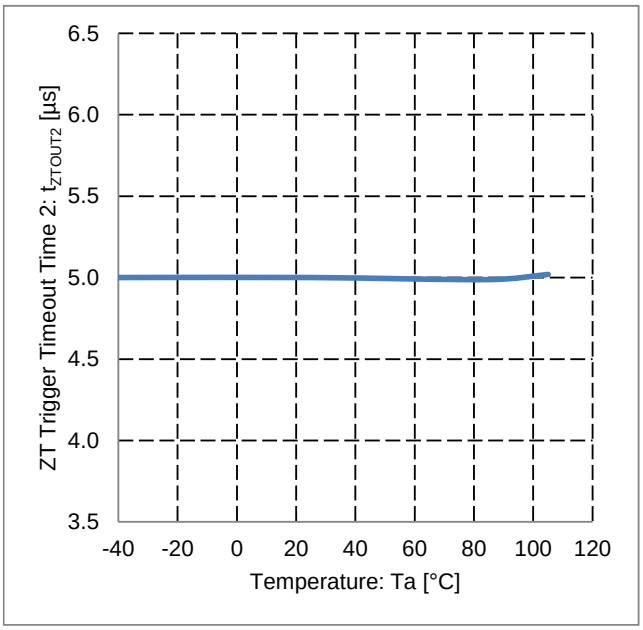


Figure 45. ZT Trigger Timeout Time 2 vs Temperature

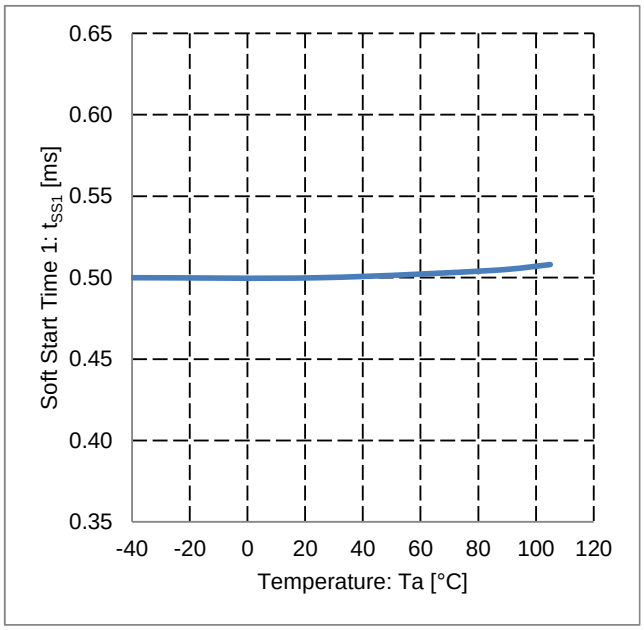


Figure 46. Soft Start Time 1 vs Temperature

Typical Performance Curves - continued
(Reference Data)

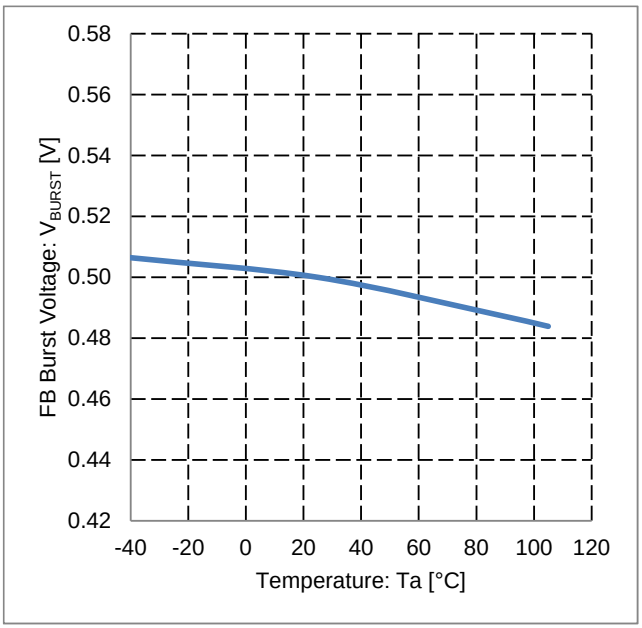


Figure 47. FB Burst Voltage vs Temperature

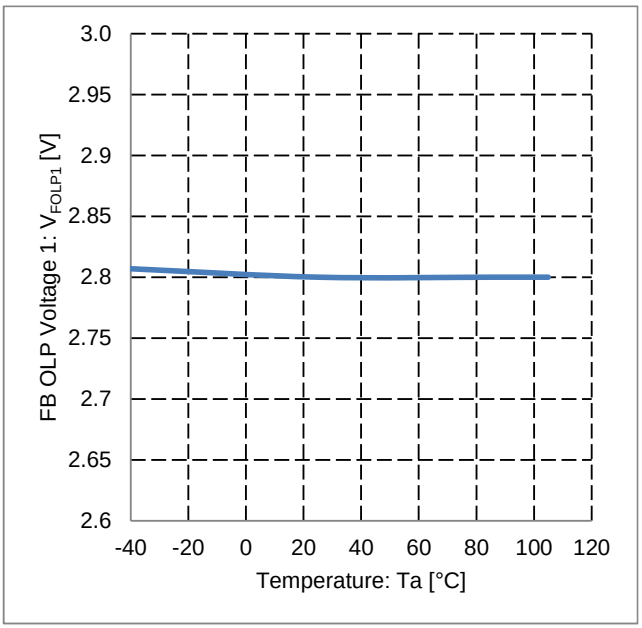


Figure 48. FB OLP Voltage 1 vs Temperature

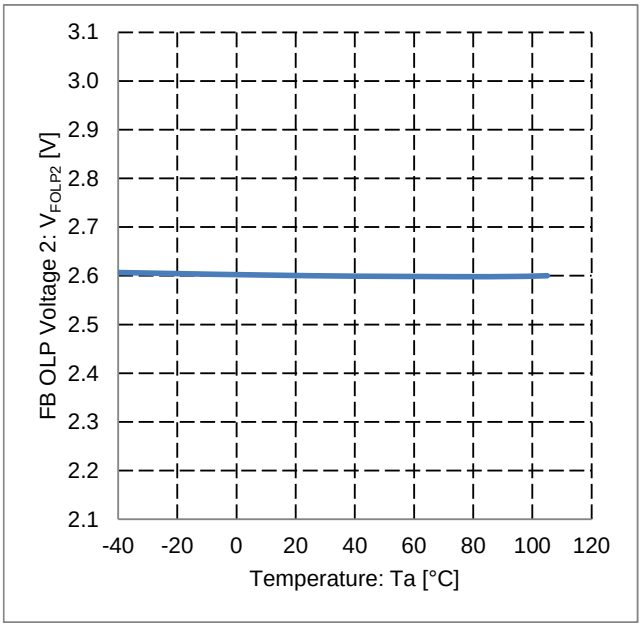


Figure 49. FB OLP Voltage 2 vs Temperature

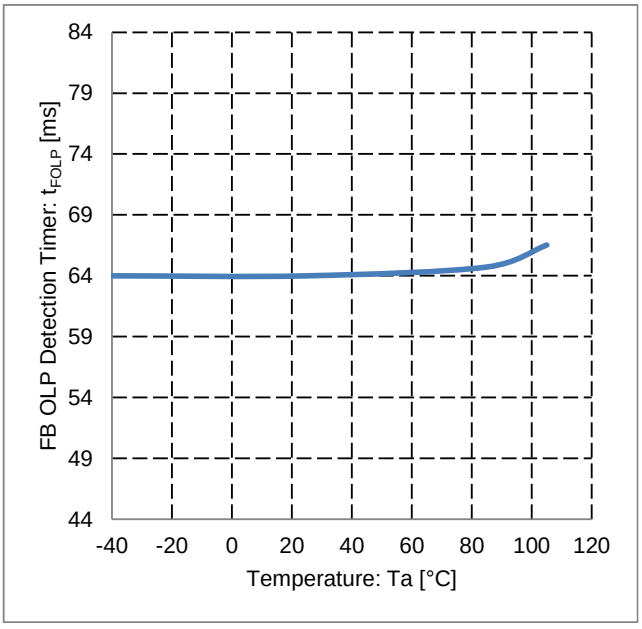


Figure 50. FB OLP Detection Timer vs Temperature

Typical Performance Curves - continued
(Reference Data)

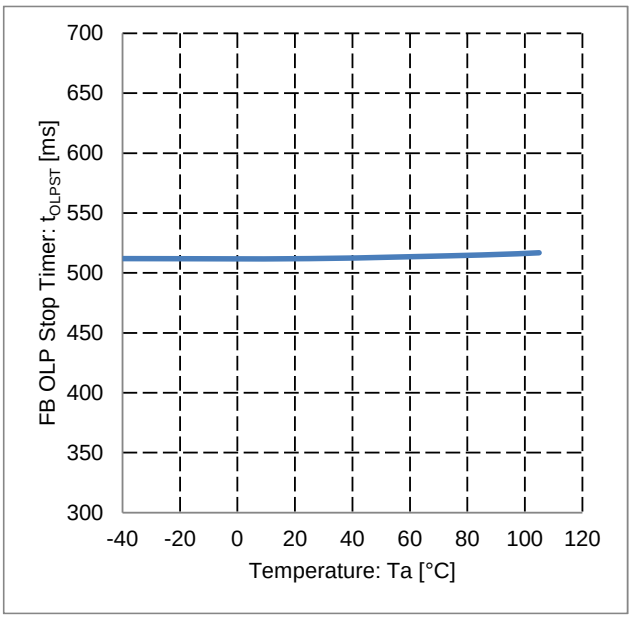


Figure 51. FB OLP Stop Timer vs Temperature

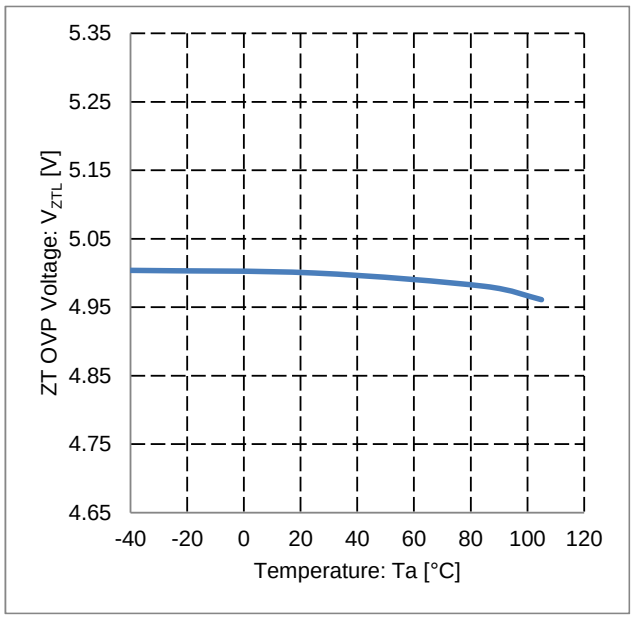
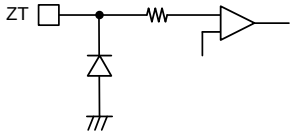
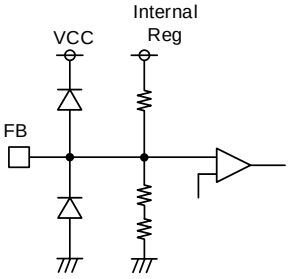
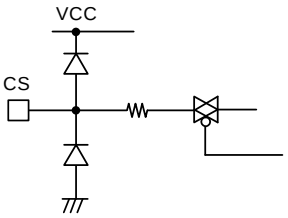
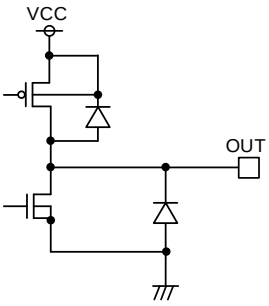
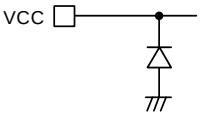
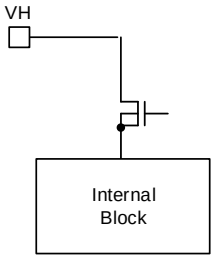


Figure 52. ZT OVP Voltage vs Temperature

I/O Equivalence Circuit

1	ZT	2	FB	3	CS	4	GND
							
5	**OUT**	**6**	**VCC**	**-**	**-**	**7**	**VH**
				–			

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Line**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes - continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

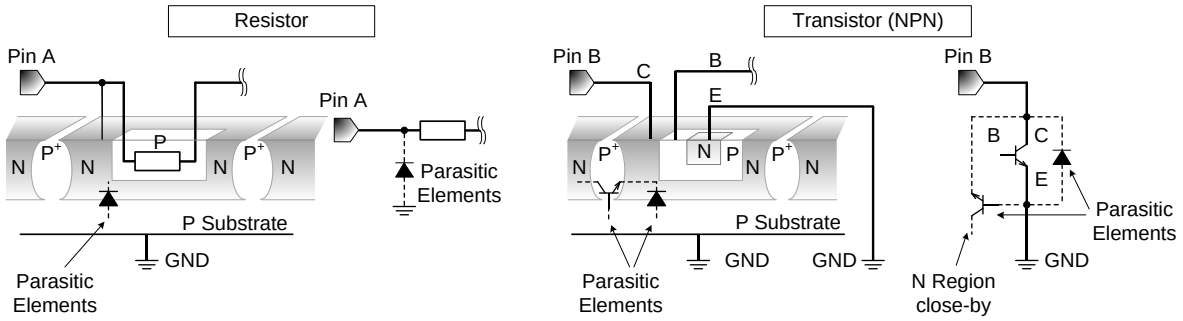


Figure 53. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

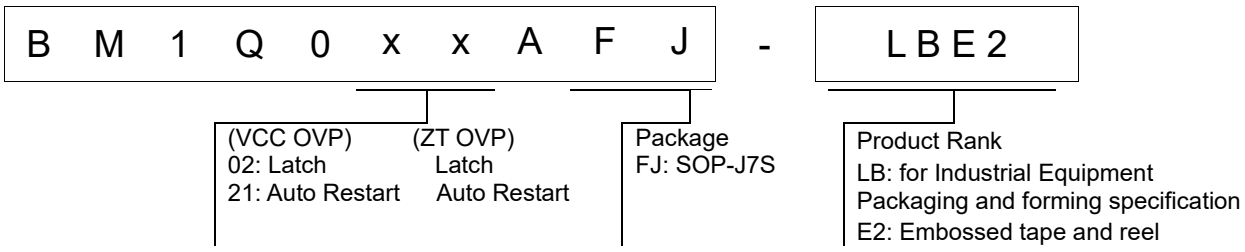
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated over current protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

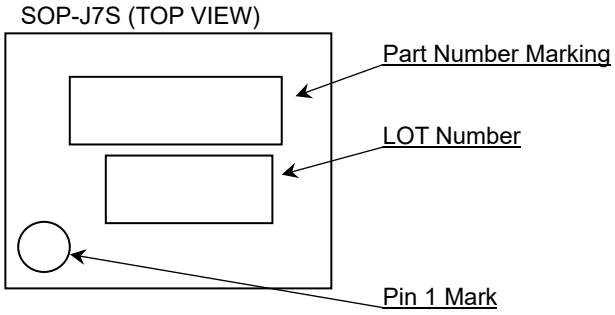
Ordering Information



Lineup

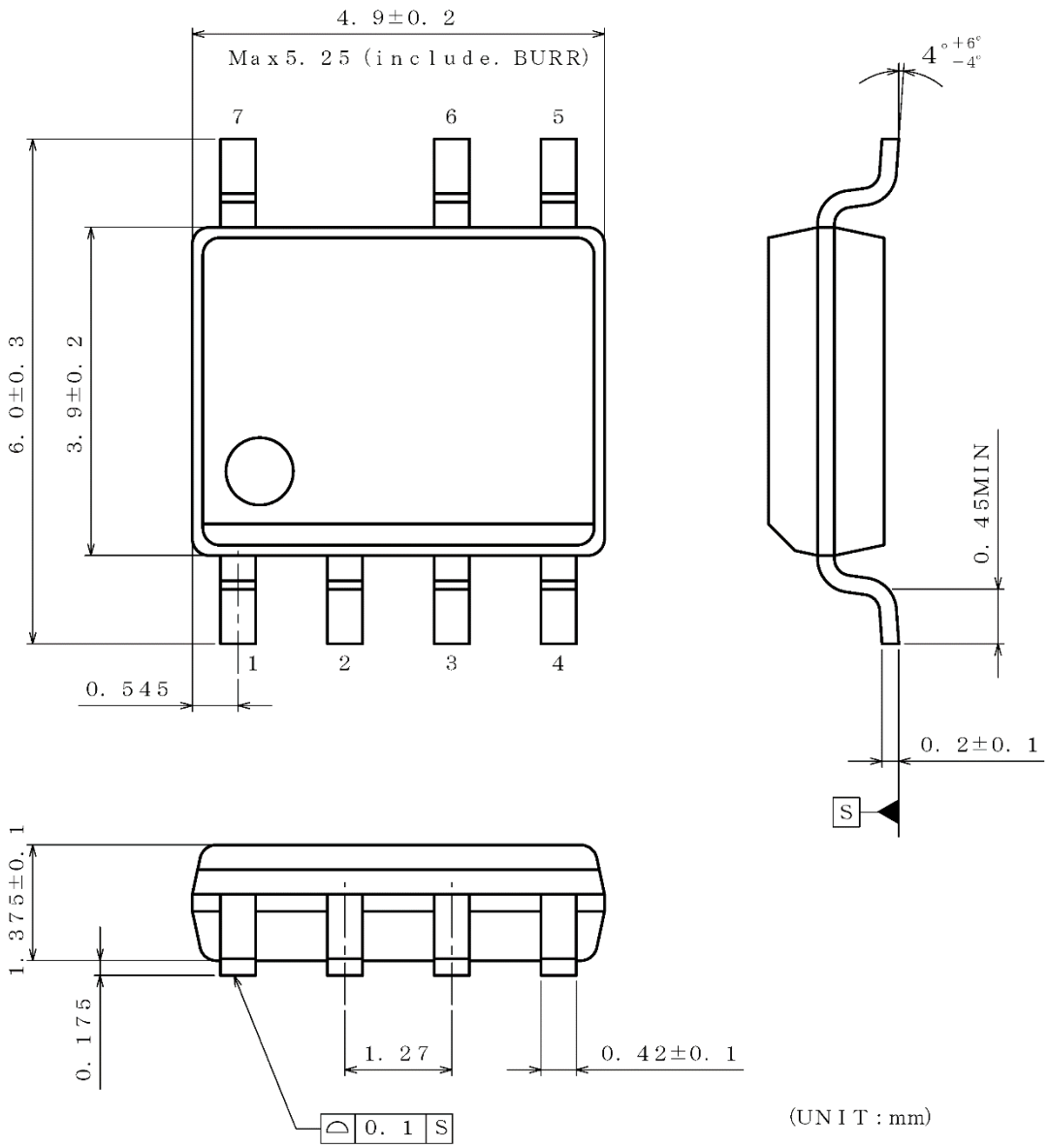
Orderable Part Number	VCC OVP	ZT OVP	Package	Part Number Marking
BM1Q002AFJ-LBE2	Latch	Latch	SOP-J7S	1Q02A
BM1Q021AFJ-LBE2	Auto Restart	Auto Restart		1Q21A

Marking Diagram



Physical Dimension and Packing Information

Package Name	SOP-J7S

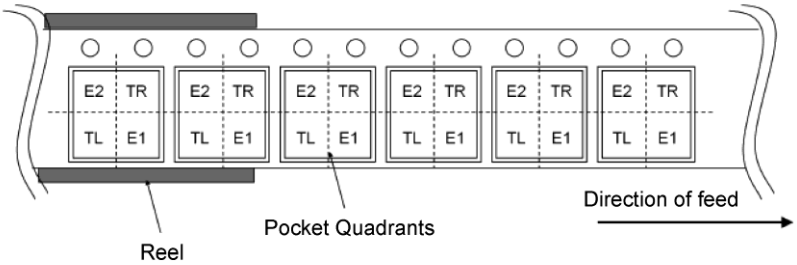


(UNIT:mm)

PKG:SOP−J7S
Drawing No.:EX095−5002−1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
09.Feb.2023	001	New Release