AC/DC Converter IC

PWM Type DC/DC Converter IC With Integrated Switching MOSFET

BM2P060NF-Z BM2P061NF-Z

General Description

The PWM Type DC/DC Converter for AC/DC provides an optimal system for all products that include an electrical outlet. This IC supports isolated power supply and enables simpler designs of various low power consumption electrical converters.
It realizes the high flexibility in power supply design by incorporating a switching MOSFET and with external current detection resistor.
This IC can make high efficiency power supply because it operates frequency reduction and burst operation at light load. Also, it has under voltage lockout and over voltage protection.
This IC has following various protection functions.

Features

- VCC Pin Under Voltage Lockout (VCC UVLO)
- VCC Pin Over Voltage Protection (VCC OVP)
- VCC OVP Voltage Setting Function
- PWM Type Current Mode Control
- Frequency Reduction Function
- Burst Operation at Light Load
- Burst Voltage Hysteresis Setting Function
- Minimum ON Width Adjustment
- Soft Start Function
- FB Pin Overload Protection Function (FB OLP)
- Over Current Protection Function by Cycle
- Over Current Detection Compensation Function by VH Voltage Detection
- Dynamic Over Current Protection
- Leading Edge Blanking Function

Key Specifications

- Operating Power Supply Voltage Range
  VCC Pin Voltage: 11 V to 52 V
  DRAIN Pin Voltage: 730 V (Max)
- Current at Switching Operation:
  BM2P060NF-Z: 1400 µA (Typ)
  BM2P061NF-Z: 1100 µA (Typ)
- Current at Burst Operation: 440 µA (Typ)
- Switching Frequency: 65 kHz (Typ)
- Operating Temperature Range: -40 °C to +105 °C
- MOSFET ON Resistor: BM2P060NF-Z: 0.70 Ω (Typ)
  BM2P061NF-Z: 1.00 Ω (Typ)

Package

Package	W (Typ) x D (Typ) x H (Max)
SOP20A	12.8 mm x 10.3 mm x 2.65 mm

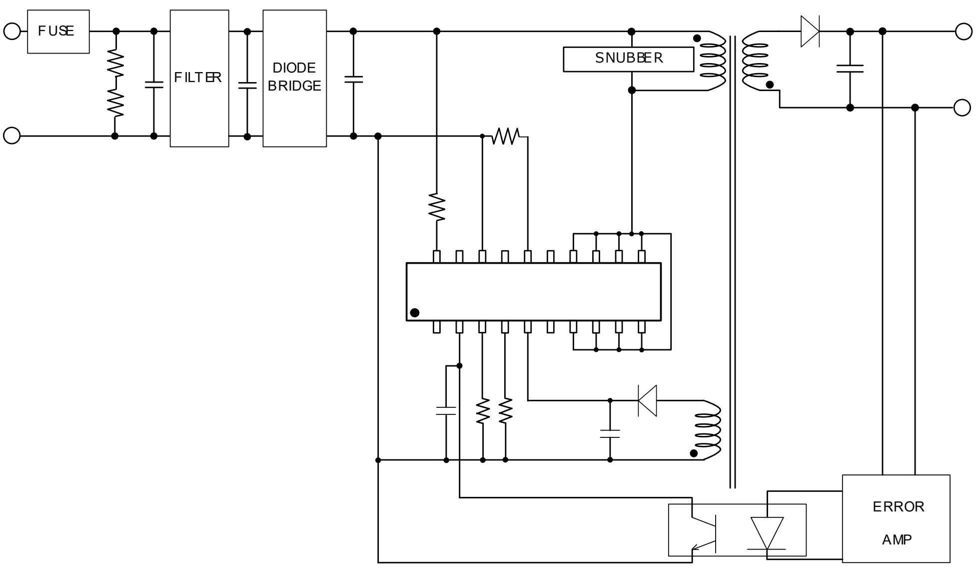
Lineup

Product Name	MOSFET ON Resistor
BM2P060NF-Z	0.70 Ω
BM2P061NF-Z	1.00 Ω

Applications

AC Adapters, Each Household Applications and Power Supplies for Motor

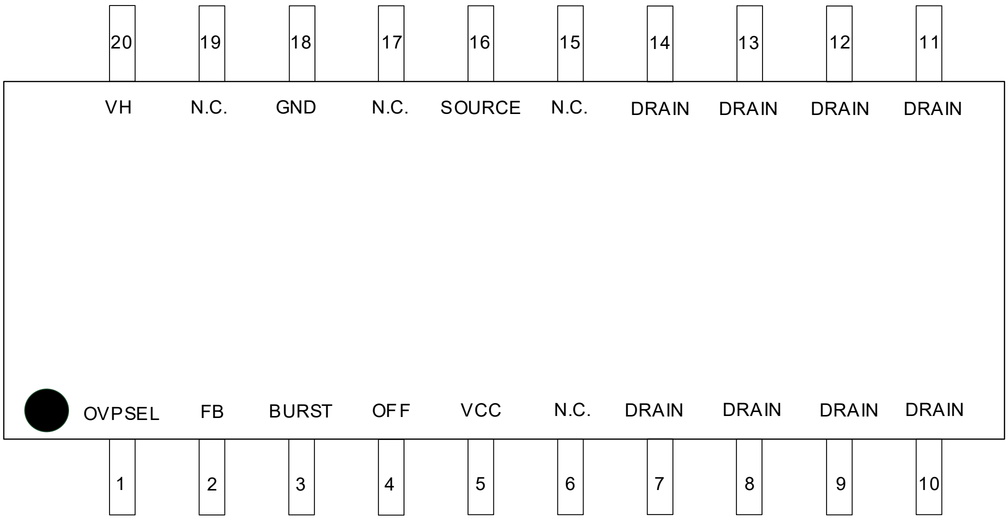
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

(TOP VIEW)

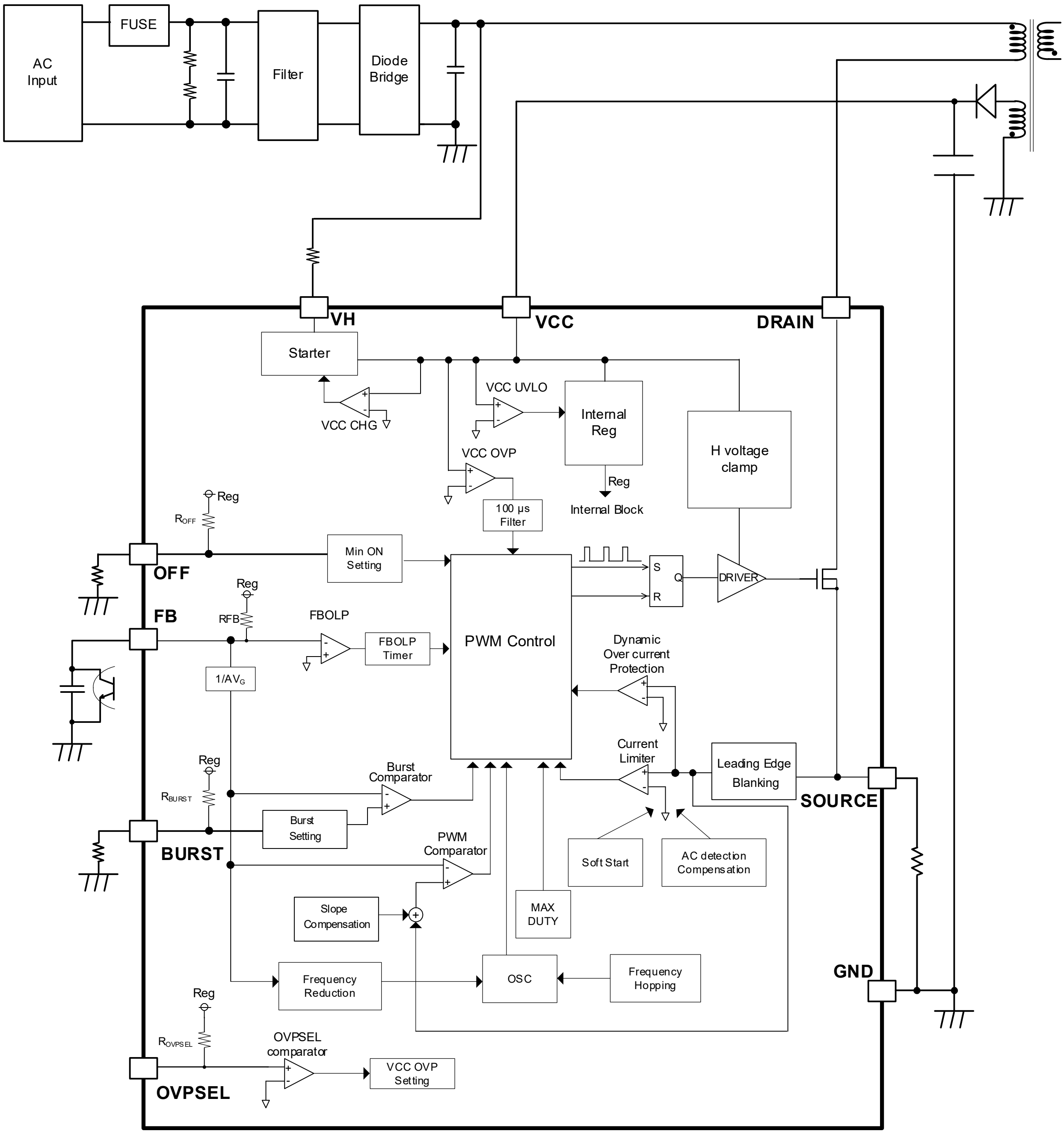


Pin Descriptions

No	Pin name	I/O	Function	ESD Diode	
				VCC	GND
1	OVPSEL	I	VCC OVP voltage setting pin	-	○
2	FB	I/O	Feedback pin	-	○
3	BURST	I	Burst setting pin	-	○
4	OFF	I	MIN on setting pin	-	○
5	VCC	I/O	Power supply input pin	-	○
6	N.C.	-	No connection(Note 1)	-	-
7	DRAIN	I/O	MOSFET Drain pin	-	○
8	DRAIN				
9	DRAIN				
10	DRAIN				
11	DRAIN				
12	DRAIN				
13	DRAIN				
14	DRAIN				
15	N.C.	-	No connection(Note 1)	-	-
16	SOURCE	I/O	MOSFET source pin	-	○
17	N.C.	-	No connection(Note 1)	-	-
18	GND	I/O	GND pin	○	-
19	N.C.	-	No connection(Note 1)	-	-
20	VH	I	Start-up pin	-	○

(Note 1) The N.C. pin must be open on the board. It means not to connect GND etc.

Block Diagram



Description of Blocks

1 Start-up Circuit

This IC has a built-in start-up circuit. When the AC input voltage is applied, charge is stored in the capacitor after rectification and the VH pin is also applied the voltage.
Then the VCC pin voltage is charged by applied current to the VCC pin through the start-up circuit. This charge is stopped after the VCC pin voltage rises and VCC UVLO is released.

2 VCC Pin Protection Function

This IC has VCC UVLO, VCC OVP and VCC recharge function at the VCC pin.

2.1 VCC UVLO (Under Voltage Lockout)

This is an auto recovery comparator with voltage hysteresis. When the VCC pin voltage becomes less than V_{UVLO2}, the IC stops the operation. When the VCC pin voltage becomes more than V_{UVLO1}, the operation is restarted.

2.2 VCC OVP (Over Voltage Protection)

This is an auto recovery comparator with voltage hysteresis. When the VCC pin voltage becomes more than V_{OVP1X}, the IC stops the operation. When the VCC pin voltage becomes less than V_{OVP2X}, the operation is restarted. V_{OVP1X} means V_{OVP1A} and V_{OVP1B}, and V_{OVP2X} means V_{OVP2A} and V_{OVP2B}. The value is set by the OVPSEL pin.

2.3 VCC Recharge Function

If the VCC pin voltage drops to less than V_{CHG1} after once the VCC pin becomes more than V_{UVLO1} and the IC starts to operate, the VCC recharge function operates. At this time, the VCC pin is recharged from the VH pin through the start-up circuit. When the VCC pin voltage becomes more than V_{CHG2}, this recharge is stopped.

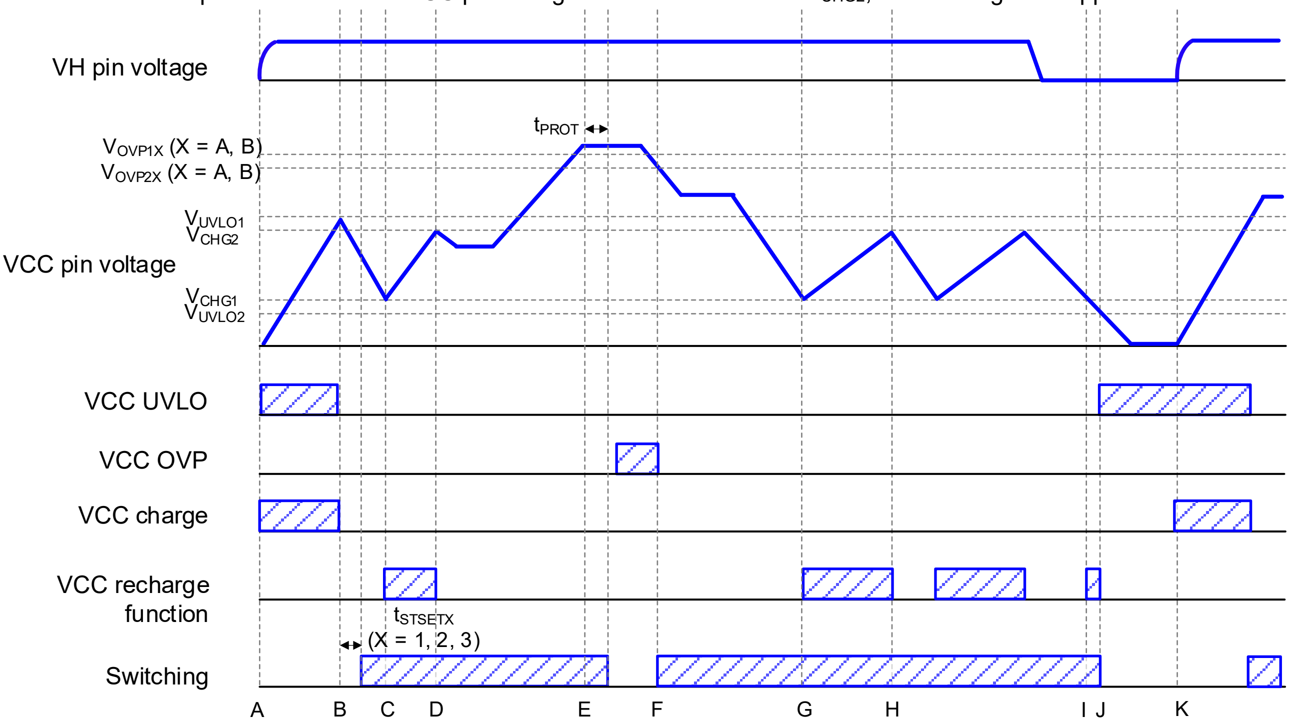


Figure 1. Timing Chart of VCC UVLO, VCC OVP and VCC Recharge Function

- A: The VH pin is applied voltage and the VCC pin voltage rises.
- B: When the VCC pin voltage becomes more than V_{UVLO1}, the switching operation starts t_{STSETX} later.
- C: When the VCC pin voltage becomes less than V_{CHG1}, the VCC pin is recharged from the VH pin by VCC recharge function.
- D: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge function is stopped.
- E: When the VCC pin voltage becomes more than V_{OVP1X} for t_{PROT}, the switching operation is stopped by VCC OVP function.
- F: When the VCC pin voltage becomes less than V_{OVP2X}, the switching operation resumes.
- G: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates.
- H: When the VCC pin voltage becomes more than V_{CHG2}, the VCC recharge function stops. By the operation of G and H, the VCC pin voltage is maintained constantly.
- I: When the VCC pin voltage becomes less than V_{CHG1}, the VCC recharge function operates. However, the current does not supply to the VCC pin and the VCC pin voltage continues to drop because the VH pin voltage dropped.
- J: When the VCC pin voltage becomes less than V_{UVLO2}, VCC UVLO operates.
- K: The VH pin is applied voltage and the IC operation restarts.

Description of Blocks - continued

3 DC/DC Driver Block

This IC performs a current mode PWM control and it has the following characteristics.

- The switching frequency operates in the range of f_{SW2} to f_{SW1} by an internal oscillator. It has a built-in frequency hopping function and the fluctuation cycle is at random. It makes the EMI low by swaying the switching frequency within ±6 %.
- This IC controls the ON width by detecting the peak current using the SOURCE pin voltage correspond to the FB pin voltage. The SOURCE pin voltage is restricted to $1/AV_G$ of the FB pin voltage.
- Maximum duty is fixed at D_{MAX}.
- In the current mode control, a sub-harmonic oscillation may occur when the duty cycle exceeds 50 %. As a countermeasure, this IC has a built-in slope compensation circuit.
- It has a built-in burst mode and frequency reduction circuit to achieve lower power consumption at light load.
- The FB pin is pulled up to the internal power supply by R_{FB}.
- The FB pin voltage is changed by the secondary output power. This IC monitors this and changes a switching operation status.

3.1 Transition of Switching Frequency by FB Pin Voltage

IC works burst operation which moves between mode a and mode b by repetition.
The BURST pin enables to set burst voltage hysteresis.
V_{BST*} means V_{BST1} to V_{BST8} and it is able to select by the BURST pin.
Refer to the description of 3.7 about setting by the BURST pin.

IC does not work switching operation when the FB pin voltage is less than burst stop voltage at light load.
After burst stop status, as the FB pin voltage is more than burst release voltage, IC rework switching operation.
IC switching frequency increases from fsw2 to fsw1 in proportion to the FB voltage at mode c.

mode a:	Burst operation	(Operate intermittently)
mode b:	Fix frequency operation	(Operate for f_{SW2})
mode c:	Frequency modulated operation	(Change switching frequency)
mode d:	Fix frequency operation	(Operate for f_{SW1})

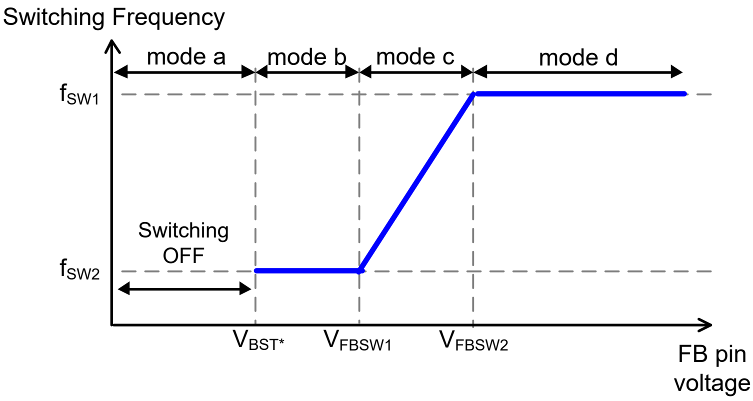


Figure 2. State Transition of Switching Frequency

3. DC/DC Driver Block - continued

3.2 Transition of SOURCE Pin Voltage by FB Pin Voltage

This IC operates as shown below.
Over current detection protection voltage (V_{OCP}) means from V_{OCP1} to V_{OCP8}, the value is set by VH voltage.
The setting by VH voltage refers to 3.5.1.
V_{BST*} means from V_{BST1} to V_{BST8}, the value is set by the BURST pin voltage.
The setting by the BURST pin refers to 3.7.

mode A: Burst operation
mode B: Normal load operation (The SOURCE pin voltage is changed by the FB pin voltage.)
mode C: Overload operation (The SOURCE pin peak voltage is limited by V_{OCP}.
When the status continues for t_{FBOLP1}, IC is stopped by FB OLP.)

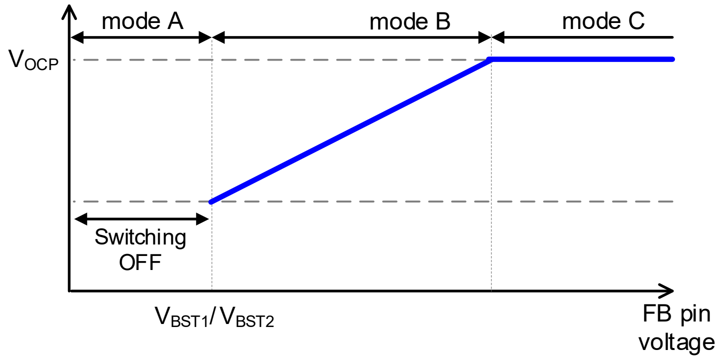


Figure 3. State Transition of SOURCE Pin Voltage by FB Pin Voltage

3.3 Soft Start Function

This function controls the over current protection voltage in order to prevent any excessive voltage or current rising at start-up. This IC enables the soft start operation by changing the over current protection voltage with time.

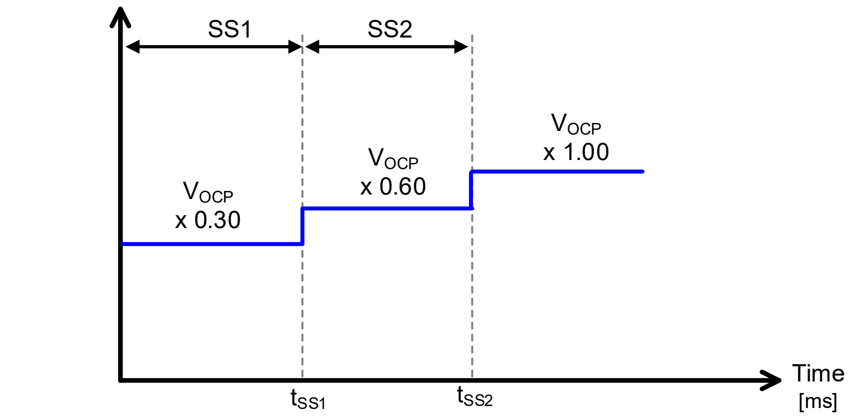


Figure 4. Soft Start Function

3. DC/DC Driver Block - continued

3.4 FB Pin Overload Protection Function (FB OLP)

This IC is switched off when status that the FB pin voltage more than V_{FBOLP1} during t_{FBOLP1}.
When the FB pin voltage is less than V_{FBOLP2} during t_{FBOLP1}, the detection timer t_{FBOLP1} is released.
It restarts with soft start after f_{FBOLP2} when switching off.

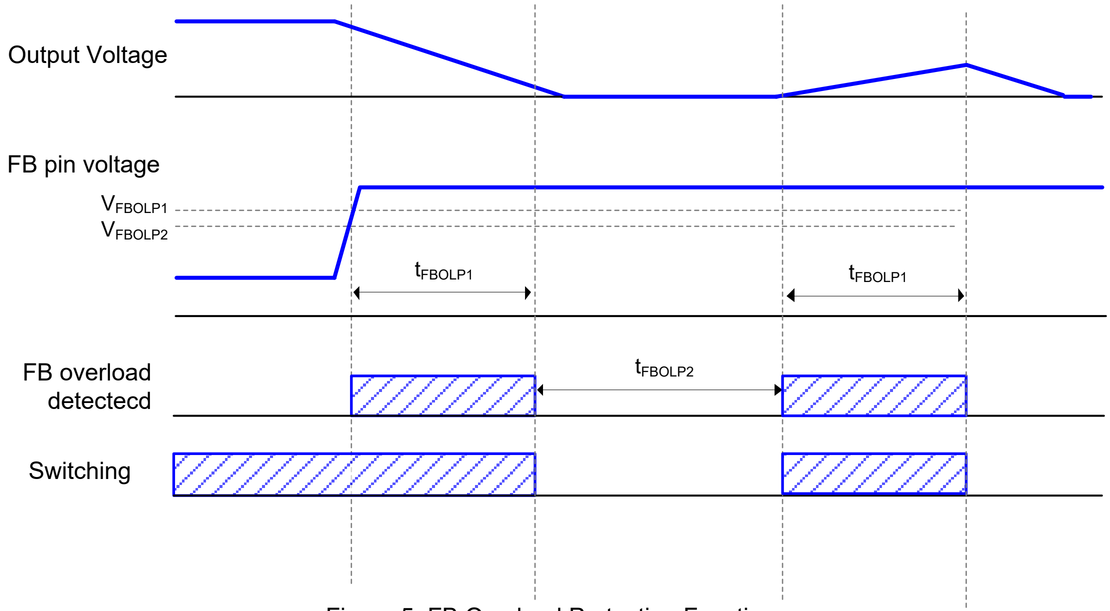


Figure 5. FB Overload Protection Function

3. DC/DC Driver Block - continued

3.5 SOURCE Pin Protection Function

This IC has a built-in OCP for cycle and Dynamic OCP in the SOURCE pin.

Table 1. Operation Status of SOURCE Pin Protection Functions

Function	Load Status at Operation to Protect	Detection Voltage	Operation to Protect
OCP	Over the peak load (Lowing the output voltage)	SOURCE pin peak voltage > V_{OCP} (V_{OCP}: It is set from V_{OCP1} to V_{OCP8})	Turned off by pulse
Dynamic OCP	SOURCE pin voltage is increased for CCM operation	SOURCE pin peak voltage > V_{DOC} Operate at the time of the detection in two continuations. (V_{DOC}: set by from V_{DOC1} to V_{DOC8})	Switching stop for t_{DOC}

3.5.1 Over Current Protection Function (OCP)

This IC is built-in OCP function by switching cycle.
As the SOURCE pin peak voltage is more than V_{OCP1} to V_{OCP8}, MOSFET is turned to OFF.
OCP is built-in input voltage compensation function. IC detects the VH pin voltage, OCP voltage is switched from V_{OCP1} to V_{OCP8} according to Table 2.
This function compensates the AC voltage dependency of overload protection power.
At this time, the maximum power has the characteristics shown in Figure 7.

Table 2. OCP Voltage by VH Voltage Detection

VH Voltage[V]	OCP Symbol	OCP[V] (Typ)
to 85	V_{OCP1}	0.680
85 to 127	V_{OCP2}	0.670
127 to 170	V_{OCP3}	0.640
170 to 212	V_{OCP4}	0.615
212 to 255	V_{OCP5}	0.600
255 to 297	V_{OCP6}	0.590
297 to 339	V_{OCP7}	0.580
339 to	V_{OCP8}	0.570

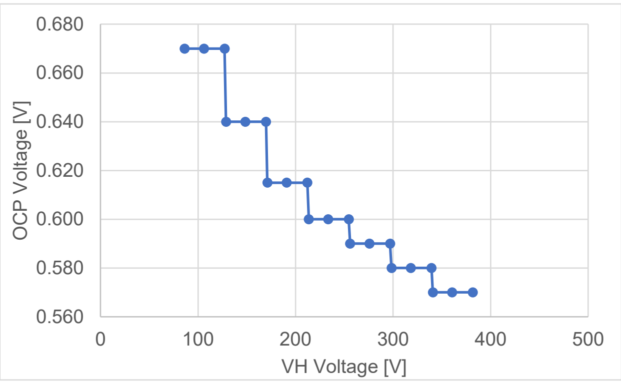


Figure 6. OCP Voltage vs VH Voltage

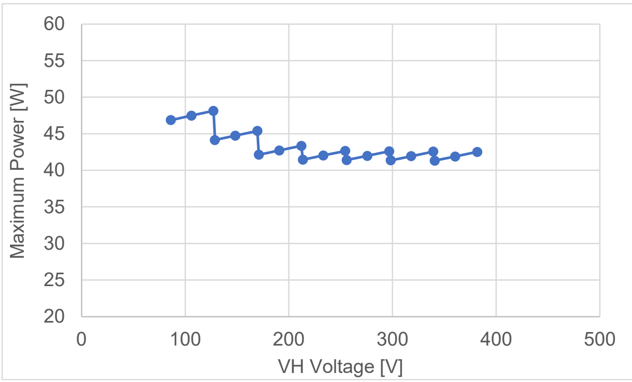


Figure 7 (Note 2). Sample of Maximum Power
(L_p = 255 μH, R_s = 0.29 Ω)

(Note 2) Figure 7 is reference graph. It changes to depend on external condition.

3.5 SOURCE Pin Protection Function - continued

3.5.2 Dynamic Over Current Protection Function

This IC is built-in dynamic over current protection.
When the SOURCE pin voltage detects over V_{DOC} voltage in continuous two pulses, IC stops switching operation for t_{DOC}.

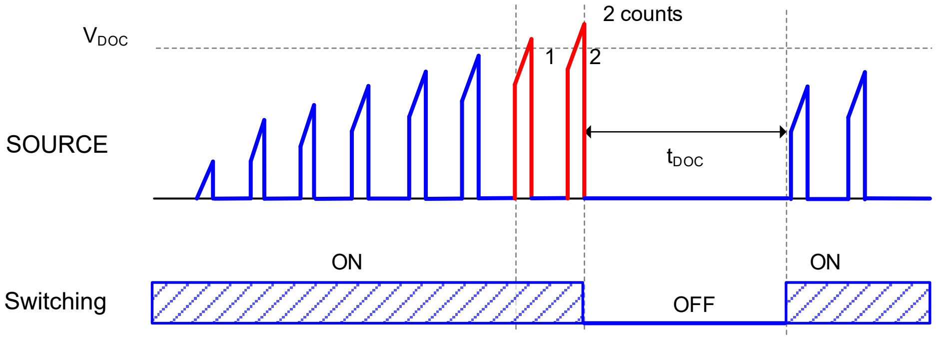


Figure 8. Dynamic OCP Timing Chart

3.5.3 Leading Edge Blanking

Normally, when the MOSFET for switching is turned to ON, surge current is generated at each capacitor component and drive current and so on. At this time, detection errors may occur in the over current protection function because the SOURCE pin voltage rises temporary. To prevent these errors, Leading Edge Blanking function is built-in this IC. This function masks the SOURCE pin voltage for t_{LEB} from the switch of the Drain pin H to L.

3.6 Minimum ON Width Switching Function by the OFF Pin

Minimum ON width can be switched external resistor at the OFF pin.
IC detects the OFF pin external resistor value at the timing of t_{STSET2} from VCC UVLO released.
Then IC sets minimum ON width below. The OFF pin is set L after the detection of external resistor.
The function is reset when VCC UVLO is detected.
When IC detects OCP, it switches minimum ON width to t_{MIN4}.

Table 3. Minimum ON Setting Width

R_1 (kΩ)	Minimum ON Width Symbol
OPEN	t_{MIN1}
180	t_{MIN2}
47 or less	t_{MIN3}

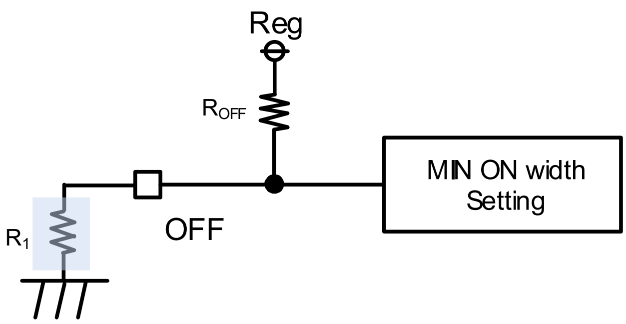


Figure 9. OFF Setting Circuit

3. DC/DC Driver Block - continued

3.7 BURST Voltage Switching Function by the BURST Pin

BURST voltage can be switched external resistor at the BURST pin.
IC detects the BURST pin external resistor value at the timing of t_{STSET1} from VCC UVLO released.
Then IC sets BURST voltage below. The BURST pin is set L after the detection of external resistor.
The function is reset when VCC UVLO is detected.

Table 4. BURST Voltage Setting

R_2 (kΩ)	BURST Detection Voltage Symbol	BURST Release Voltage Symbol
OPEN	V_{BST1}	V_{BST2}
180	V_{BST3}	V_{BST4}
47	V_{BST5}	V_{BST6}
GND	V_{BST7}	V_{BST8}

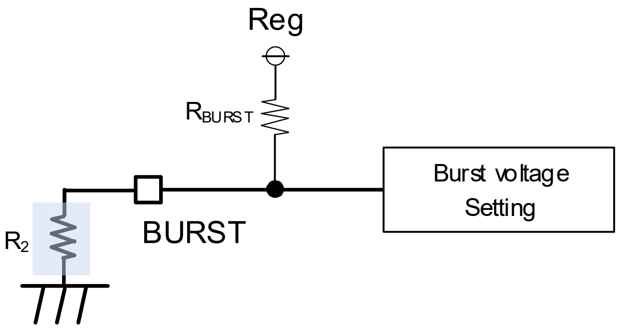


Figure 10. BURST Setting Circuit

4 VCC OVP Voltage Switching Function by the OVPSEL Pin

VCC OVP voltage can be switched by the status of the OVPSEL pin.
IC detects the status of OVPSEL pin at the timing of t_{STSET3} from VCC UVLO released.
Then IC sets VCC OVP voltage below. The OVPSEL pin is set L after the detection of status of the OVPSEL pin.
The function is reset when VCC UVLO is detected.
The OVPSEL pin is pulled up in the IC inside by R_{OVPSEL}.

Table 5. VCC OVP Voltage Setting

OVPSEL Pin Condition	VCC OVP Detection Voltage Symbol	VCC OVP Release Voltage Symbol
V_{OVPSEL} or more	V_{OVP1A}	V_{OVP2A}
V_{OVPSEL} or less	V_{OVP1B}	V_{OVP2B}

Operation Mode of Protection Functions
The operation modes of each protection function are shown in Table 6.

Table 6. Operation Modes of Protection Functions

	VCC UVLO	VCC OVP(Note 3)	Dynamic OCP
Detection Conditions	VCC pin voltage < V_{UVLO2} (voltage drop)	VCC pin voltage > V_{OVP1X} (voltage rise)	SOURCE pin voltage > V_{DOC}
Release Conditions	VCC pin voltage > V_{UVLO1} (voltage rise)	VCC pin voltage < V_{OVP2X} (voltage drop)	Release after past for t_{DOC}
Detection Timer (Reset Conditions)	–	t_{PROT} (VCC pin voltage < V_{OVP2X})	Detect continuous two pulses
Auto restart or Latch	Auto restart	Auto restart	Auto restart

	FB OLP	TSD (Thermal Protection)
Detection Conditions	FB pin voltage > V_{FBOLP1} (Voltage rise)	Tj > T_{TSD1} (Temperature rise)
Release Conditions	Elapsed period by t_{FBOLP2}	Tj < T_{TSD2} (Temperature drop)
Detection Timer (Reset Conditions)	t_{FBOLP1} (FB pin voltage < V_{FBOLP2})	t_{PROT} (Tj < T_{TSD2})
Auto restart or Latch	Auto restart	Auto restart

(Note 3) X is set by the OVPSEL pin (X = A, B).

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Condition
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +650	V	DRAIN
		730	V	DRAIN (tpulse < 10 μs)(Note 4)
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +6.5	V	SOURCE, FB, OFF, BURST, OVPSEL
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +62.0	V	VCC
Maximum Applied Voltage 4	V_{MAX4}	-0.3 to +650.0	V	VH
Drain Current 1 (Pulse)	I_{DP1}	21	A	P_w = 10 μs, duty cycle = 1 % (BM2P060NF-Z)
Drain Current 2 (Pulse)	I_{DP2}	12	A	P_w = 10 μs, duty cycle = 1 % (BM2P061NF-Z)
Power Dissipation	Pd	2.30	W	(Note 5)
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 4) Duty is less than 1 %.
(Note 5) When IC mounted singly. Derate by 18.3 mW / °C if the IC is used in the ambient temperature 25 °C or more.

Thermal Dissipation

Make the thermal design so that the IC operates in the following conditions.
(Because the following temperature is guarantee value, it is necessary to consider margin.)

1. The ambient temperature Ta must be 105 °C or less.
2. The IC's loss must be the power dissipation Pd or less.

The thermal abatement characteristic is as follows.
(At mounting singly)

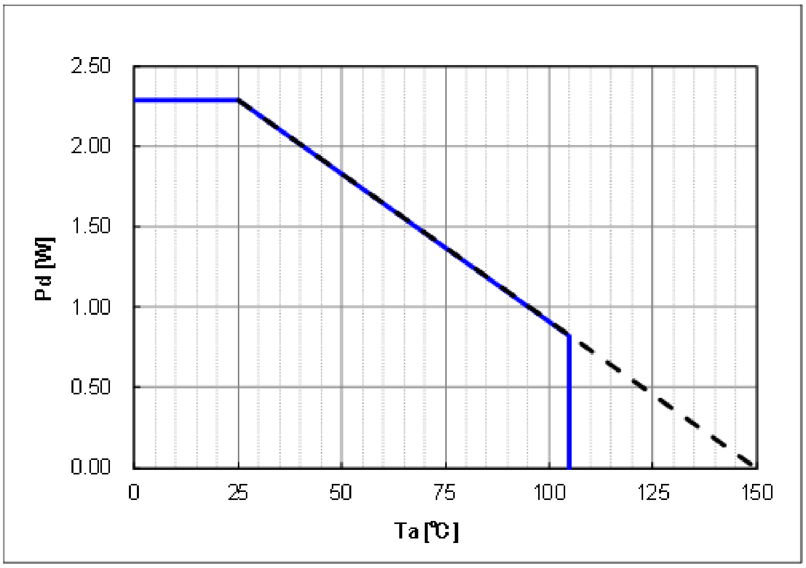


Figure 11. SOP20A Thermal Dissipation Characteristic

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating VCC Pin Voltage Range	V_{CC}	11	-	52	V
VH Pin Voltage Range	V_H	-	-	450	V
VCC Pin Capacitor	C_{VCC}	4.7	-	-	μF
VH Pin Resistor	R_{VH}	-	-	4.7	kΩ
Operating Temperature	Topr	-40	-	+105	°C

Electrical Characteristics in MOSFET Part (Unless otherwise specified Tj = 25 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Drain Voltage	V_{DS}	650	-	-	V	I_D = 1 mA, V_{GS} = 0 V
		730	-	-	V	I_D = 1 mA, V_{GS} = 0 V tpulse < 10 μs *(Note 6)*
DRAIN Pin Leak Current	I_{DSS}	-	-	100	μA	V_{DS} = 650 V, V_{GS} = 0 V
ON Resistor 1	$R_{DS(ON)1}$	-	0.70	0.86	Ω	BM2P060NF-Z
ON Resistor 2	$R_{DS(ON)2}$	-	1.00	1.35	Ω	BM2P061NF-Z

(Note 6) Duty is less than 1 %.

Electrical Characteristics in Start-up VH Part (Unless otherwise specified Tj = 25 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Start-up Current	I_{START1}	8	15	25	mA	VH = 100 V, VCC = 10 V
VH Pin OFF Current	I_{START2}	5	12	20	μA	VH = 100 V, VCC = 15 V

Electrical Characteristics in Control IC Part (Unless otherwise specified Tj = -40 °C to +105 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current at Switching Operation 1A	I_{ON1A}	900	1400	2000	μA	BM2P060NF-Z FB = 3.0 V *(Note 7)*
Current at Switching Operation 1B	I_{ON1B}	500	1100	1700	μA	BM2P061NF-Z FB = 3.0 V *(Note 7)*
Current at Burst Operation	I_{ON2}	290	440	590	μA	FB = 0.2 V *(Note 7)*
VCC UVLO Release Voltage	V_{UVLO1}	13.0	14.0	15.0	V	VCC rising *(Note 7)*
VCC UVLO Detection Voltage	V_{UVLO2}	8.2	9.0	9.8	V	VCC falling *(Note 7)*
VCC UVLO Hysteresis	V_{UVLO3}	-	5.0	-	V	V_{UVLO3} = V_{UVLO1} - V_{UVLO2} *(Note 7)*
VCC OVP Detection Voltage A	V_{OVP1A}	52.0	55.0	58.0	V	VCC rising *(Note 7)* OVPSEL: OPEN
VCC OVP Detection Voltage B	V_{OVP1B}	26.0	27.5	29.0	V	VCC rising *(Note 7)* OVPSEL: GND
VCC OVP Release Voltage A	V_{OVP2A}	48.0	51.0	54.0	V	VCC falling *(Note 7)* OVPSEL: OPEN
VCC OVP Release Voltage B	V_{OVP2B}	22.0	23.5	25.0	V	VCC falling *(Note 7)* OVPSEL: GND
VCC OVP Hysteresis	V_{OVP3}	-	4	-	V	V_{OVP3} = V_{OVP1} - V_{OVP2} *(Note 7)*
VCC Recharge Start Voltage	V_{CHG1}	9	10	11	V	*(Note 7)*
VCC Recharge Stop Voltage	V_{CHG2}	11	12	13	V	*(Note 7)*
Protection Mask Time	t_{PROT}	-	100	-	μs	
TSD Temperature 1	T_{TSD1}	150	-	-	°C	
TSD Temperature 2	T_{TSD2}	-	T_{TSD1} -25	-	°C	

(Note 7) Tj = 25 °C guaranteed.

Electrical Characteristics in Control IC Part – continued

(Unless otherwise specified Tj = -40 °C to +105 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DC/DC Driver Block						
Switching Frequency 1	f_{SW1}	60	65	70	kHz	(Note 7)
Switching Frequency 2	f_{SW2}	20	25	30	kHz	
Frequency Hopping Width	f_{DEL}	-	4	-	kHz	FB = 3.0 V
Voltage Gain (FB/SOURCE)	AV_G	-	5	-	V/V	
Maximum Duty	D_{MAX}	67	75	83	%	(Note 7)
FB Pin Burst Voltage 1	V_{BST1}	0.20	0.30	0.40	V	FB Falling BURST: OPEN
FB Pin Burst Voltage 2	V_{BST2}	-	0.35	-	V	FB Rising BURST: OPEN
FB Pin Burst Voltage 3	V_{BST3}	0.20	0.30	0.40	V	FB Falling BURST: 180 kΩ
FB Pin Burst Voltage 4	V_{BST4}	-	0.40	-	V	FB Rising BURST: 180 kΩ
FB Pin Burst Voltage 5	V_{BST5}	0.20	0.30	0.40	V	FB Falling BURST: 47 kΩ
FB Pin Burst Voltage 6	V_{BST6}	-	0.50	-	V	FB Rising BURST: 47 kΩ
FB Pin Burst Voltage 7	V_{BST7}	0.20	0.30	0.40	V	FB Falling BURST: GND
FB Pin Burst Voltage 8	V_{BST8}	-	0.60	-	V	FB Rising BURST: GND
Frequency Reduction Start FB Pin Voltage	V_{FBSW1}	0.75	0.90	1.05	V	(Note 7)
Frequency Reduction End FB Pin Voltage	V_{FBSW2}	1.15	1.30	1.45	V	(Note 7)
Leading Edge Blanking Time	t_{LEB}	-	0.25	-	μs	
SOURCE Pin Pull up Resistor	R_{SOCE}	1.4	2.0	2.6	MΩ	During normal operation (Note 7)
FB Pin Pull up Resistor	R_{FB}	24	30	36	kΩ	(Note 7)
Minimum ON Width 1	t_{MIN1}	0.50	0.70	0.90	μs	OFF: OPEN (Note 7)
Minimum ON Width 2	t_{MIN2}	0.95	1.20	1.45	μs	OFF: 180 kΩ (Note 7)
Minimum ON Width 3	t_{MIN3}	1.45	1.75	2.05	μs	OFF: 47 kΩ or less (Note 7)
Minimum ON Width 4	t_{MIN4}	-	0.50	-	μs	During detection of OCP
DC/DC Driver Block (SOURCE Pin Over Current Protection Function)						
SOURCE Pin OCP Voltage 1	V_{OCP1}	0.645	0.680	0.715	V	VH < 85 V
SOURCE Pin OCP Voltage 2	V_{OCP2}	0.635	0.670	0.705	V	85 V < VH < 127 V
SOURCE Pin OCP Voltage 3	V_{OCP3}	0.605	0.640	0.675	V	127 V < VH < 170 V
SOURCE Pin OCP Voltage 4	V_{OCP4}	0.580	0.615	0.640	V	170 V < VH < 212 V
SOURCE Pin OCP Voltage 5	V_{OCP5}	0.565	0.600	0.635	V	212 V < VH < 255 V
SOURCE Pin OCP Voltage 6	V_{OCP6}	0.555	0.590	0.625	V	255 V < VH < 297 V
SOURCE Pin OCP Voltage 7	V_{OCP7}	0.545	0.580	0.615	V	297 V < VH < 339 V
SOURCE Pin OCP Voltage 8	V_{OCP8}	0.535	0.570	0.605	V	VH > 339 V
SOURCE Pin Dynamic OCP Voltage 1	V_{DOC1}	0.934	1.005	1.076	V	VH < 85 V
SOURCE Pin Dynamic OCP Voltage 2	V_{DOC2}	0.920	0.990	1.060	V	85 V < VH < 127 V
SOURCE Pin Dynamic OCP Voltage 3	V_{DOC3}	0.886	0.953	1.020	V	127 V < VH < 170 V
SOURCE Pin Dynamic OCP Voltage 4	V_{DOC4}	0.858	0.923	0.988	V	170 V < VH < 212 V
SOURCE Pin Dynamic OCP Voltage 5	V_{DOC5}	0.837	0.900	0.963	V	212 V < VH < 255 V
SOURCE Pin Dynamic OCP Voltage 6	V_{DOC6}	0.823	0.885	0.947	V	255 V < VH < 297 V
SOURCE Pin Dynamic OCP Voltage 7	V_{DOC7}	0.809	0.870	0.931	V	297 V < VH < 339 V
SOURCE Pin Dynamic OCP Voltage 8	V_{DOC8}	0.795	0.855	0.915	V	VH > 339 V
SOURCE Pin Dynamic OCP Stop Timer	t_{DOC}	100	160	220	μs	(Note 7)

(Note 7) Tj = 25 °C guaranteed.

Electrical Characteristics in Control IC Part – continued
(Unless otherwise specified Tj = -40 °C to +105 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DC/DC Driver Block (Soft Start Function)						
Soft Start Timer 1	t_{SS1}	1.79	2.56	3.33	ms	
Soft Start Timer 2	t_{SS2}	7.17	10.24	13.31	ms	
DC/DC Driver Block (FB Pin Overload Protection Function)						
FB OLP Detection Voltage	V_{FBOLP1}	3.9	4.2	4.5	V	
FB OLP Release Voltage	V_{FBOLP2}	-	4.0	-	V	
FB OLP Detection Timer	t_{FBOLP1}	60	82	104	ms	*(Note 7)*
FB OLP STOP Timer	t_{FBOLP2}	484	656	828	ms	*(Note 7)*
BURST Pin Setting Block						
BURST Pin Pull up Resistor	R_{BURST}	150	200	250	kΩ	*(Note 7)*
BURST Pin External Resistor Detection Timer in Start-up	t_{STSET1}	160	320	480	μs	*(Note 7)*
OFF Pin Setting Block						
OFF Pin Pull up Resistor	R_{OFF}	150	200	250	kΩ	*(Note 7)*
OFF Pin External Resistor Detection Timer in Start-up	t_{STSET2}	160	320	480	μs	*(Note 7)*
OVPSEL Pin Setting Block						
VCC OVP Switch Voltage	V_{OVPSEL}	0.4	0.5	0.6	V	
OVPSEL Pin Pull up Resistor	R_{OVPSEL}	19.4	25.9	32.3	kΩ	*(Note 7)*
OVPSEL Pin External Resistor Detection Timer in Start-up	t_{STSET3}	160	320	480	μs	*(Note 7)*

(Note 7) Tj = 25 °C guaranteed.

Application Examples

Show a flyback circuitry example in Figure 12.
Be careful that when the DRAIN voltage turn off it is occur high voltage with ringing.
With this IC, it become able to operate to 730 V.

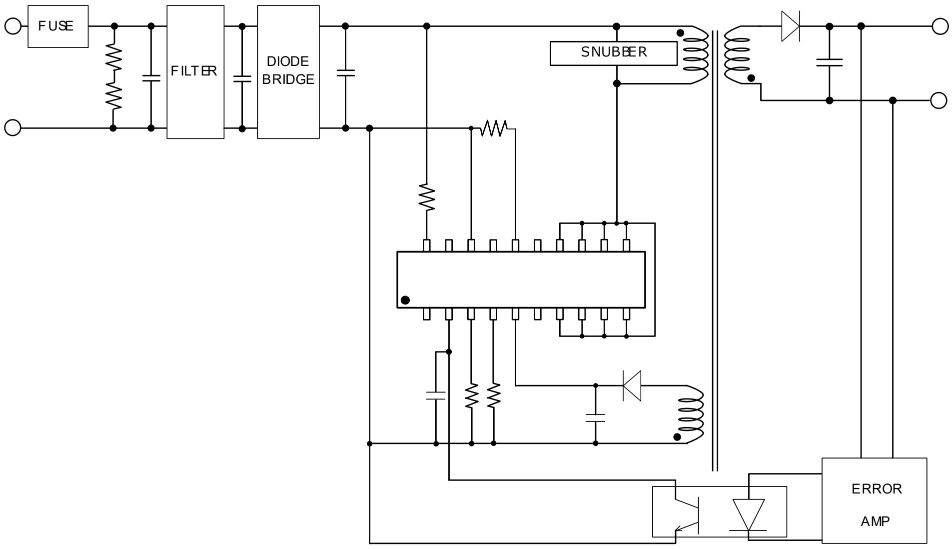


Figure 12. Flyback Application Diagram

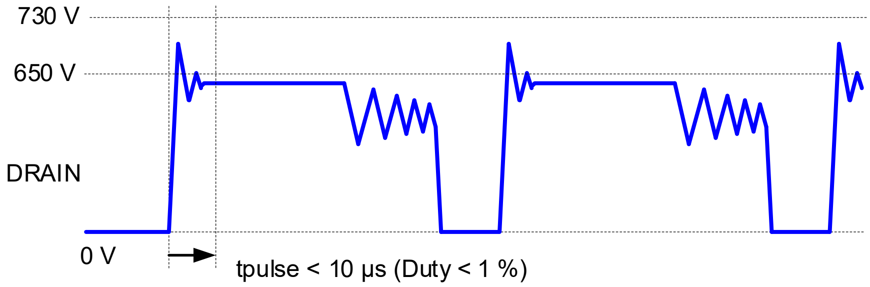


Figure 13. DRAIN Pin Ringing Waveform

Typical Performance Curves

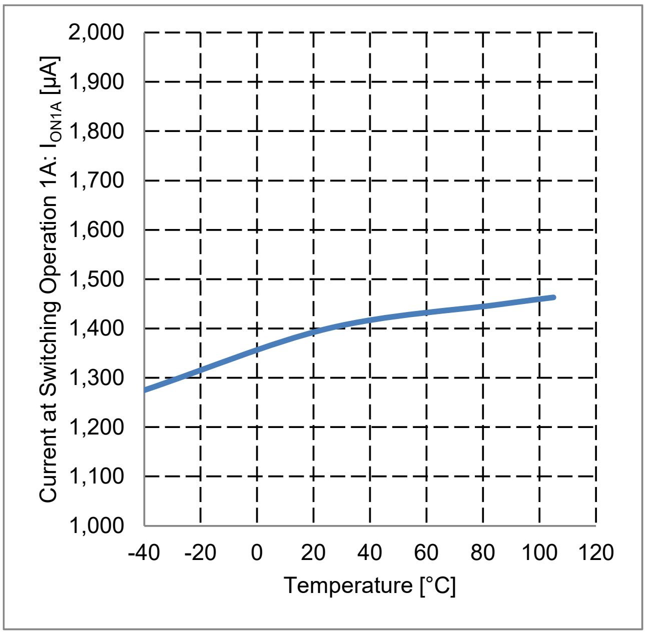


Figure 14. Current at Switching Operation 1A vs Temperature

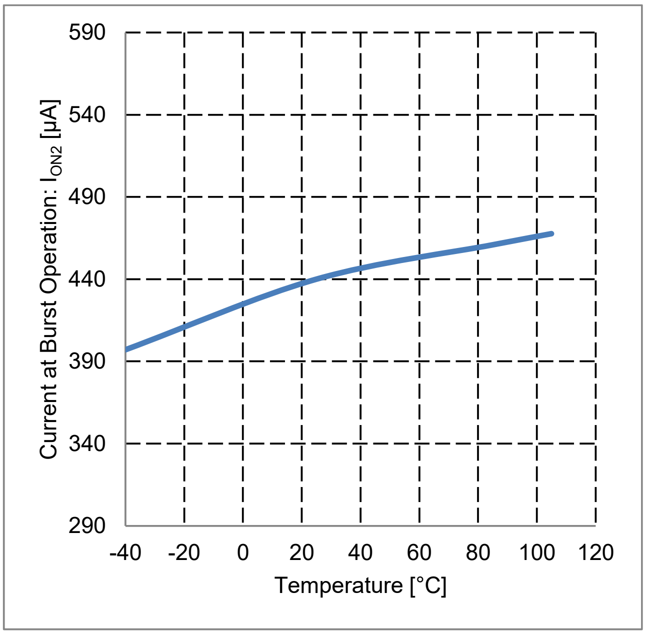


Figure 15. Current at Burst Operation vs Temperature

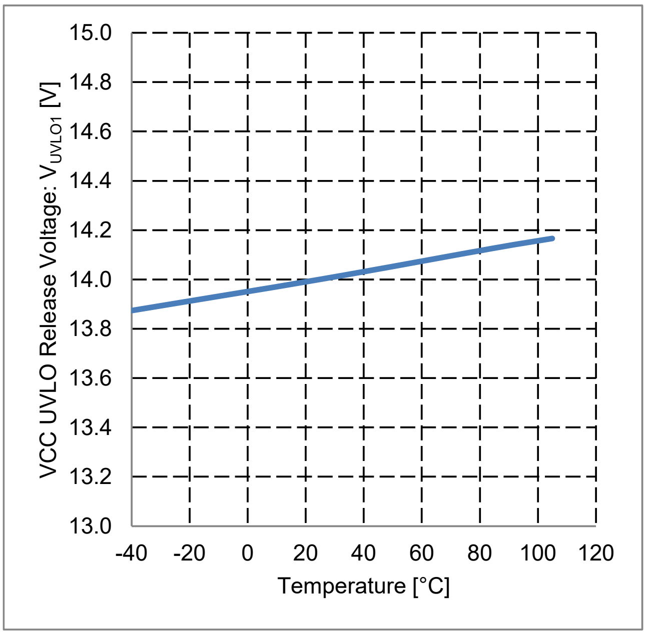


Figure 16. VCC UVLO Release Voltage vs Temperature

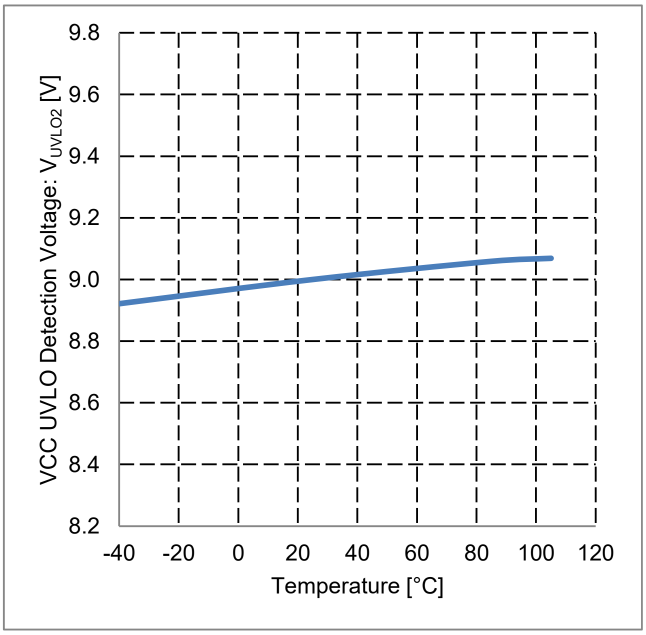


Figure 17. VCC UVLO Detection Voltage vs Temperature

Typical Performance Curves - continued

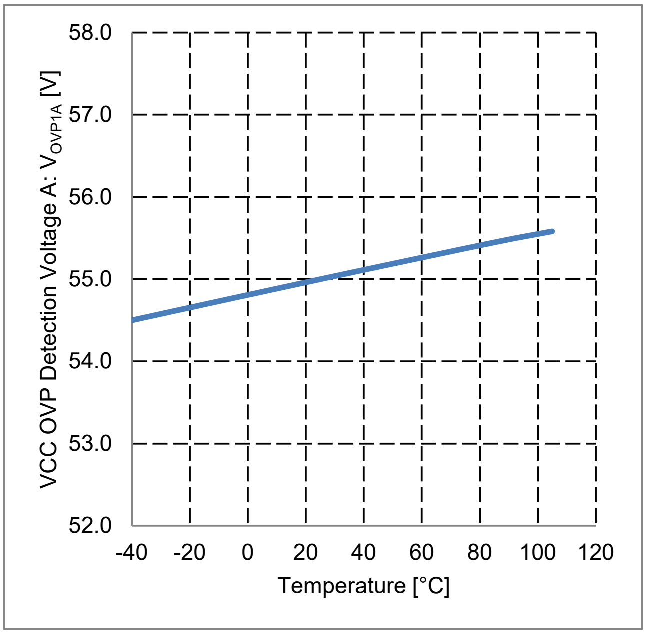


Figure 18. VCC OVP Detection Voltage A vs Temperature

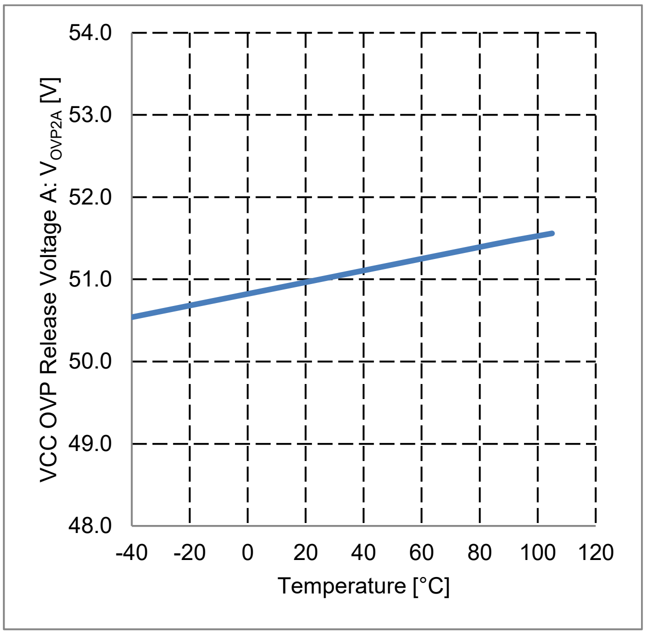


Figure 19. VCC OVP Release Voltage A vs Temperature

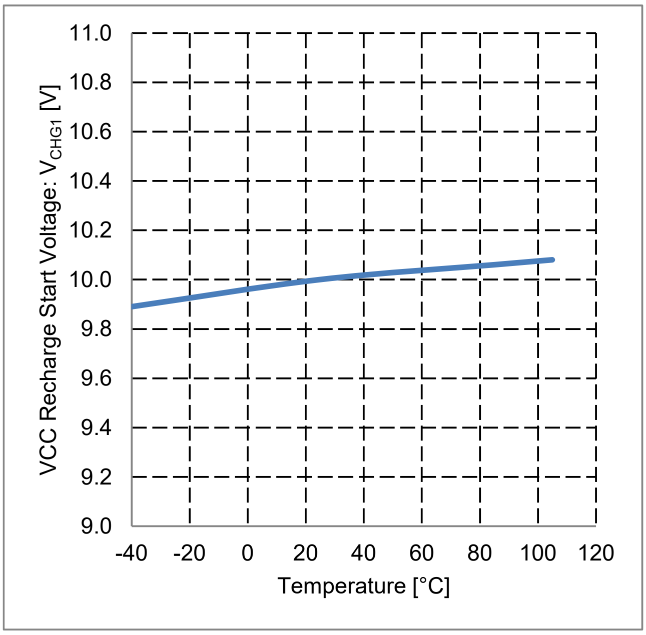


Figure 20. VCC Recharge Start Voltage vs Temperature

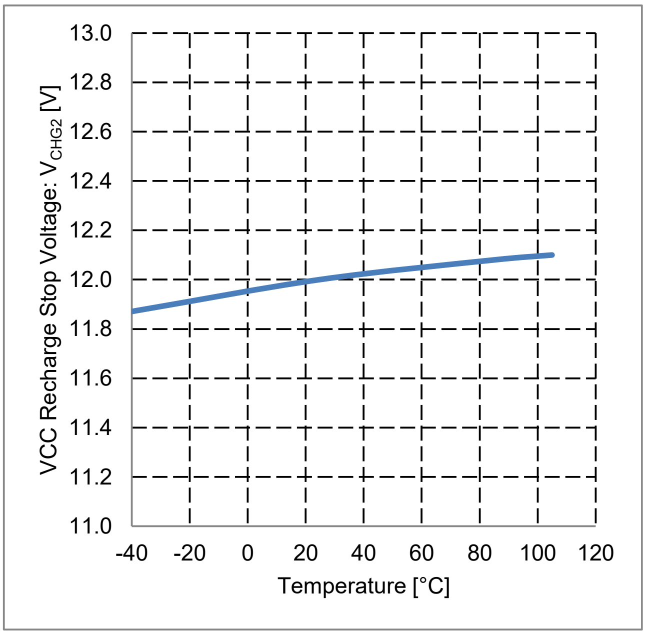


Figure 21. VCC Recharge Stop Voltage vs Temperature

Typical Performance Curves - continued

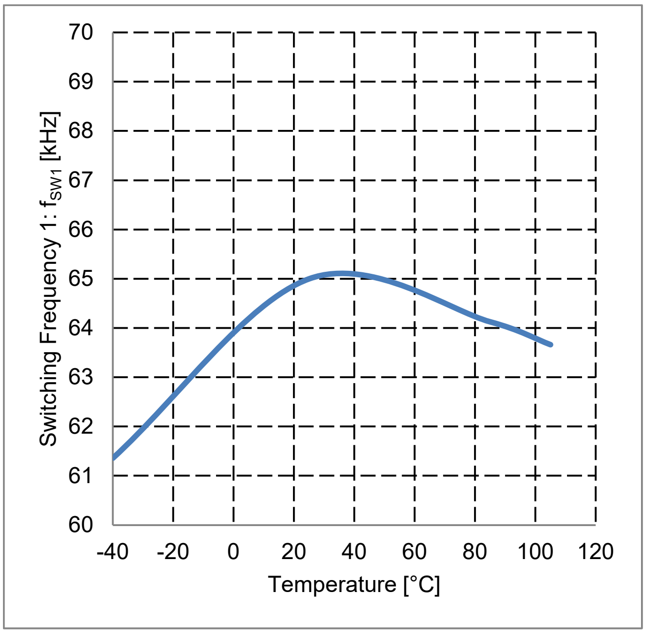


Figure 22. Switching Frequency 1 vs Temperature

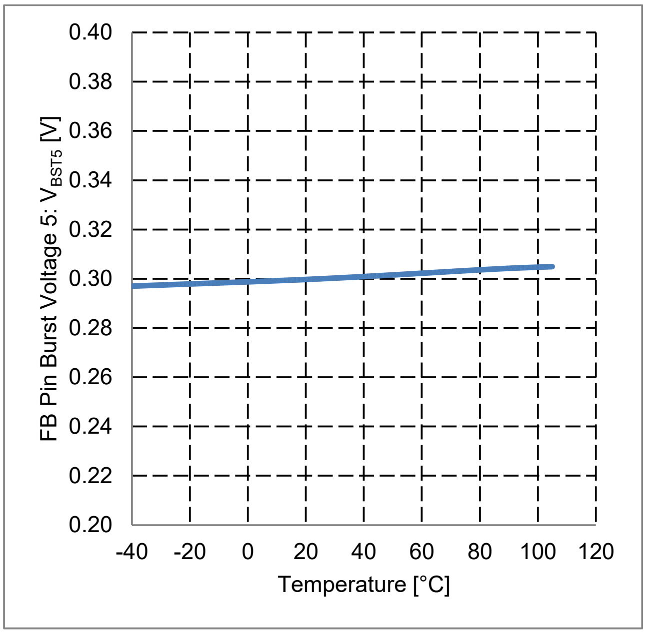


Figure 23. FB Pin Burst Voltage 5 vs Temperature

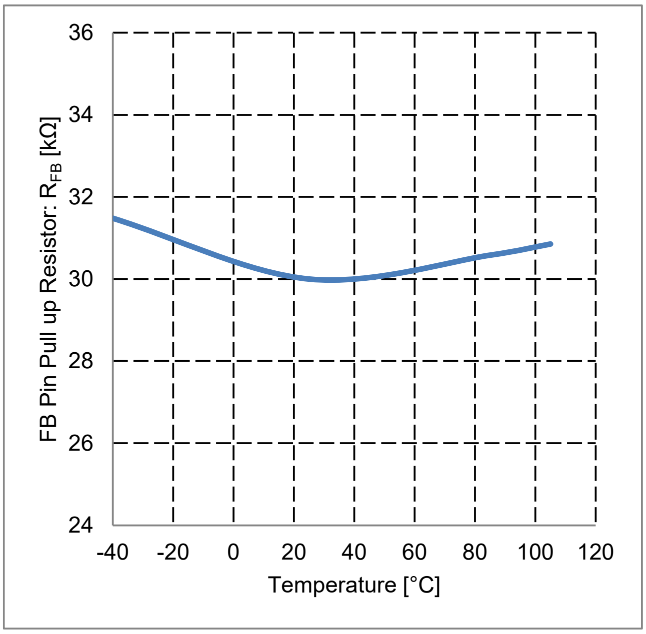


Figure 24. FB Pin Pull up Resistor vs Temperature

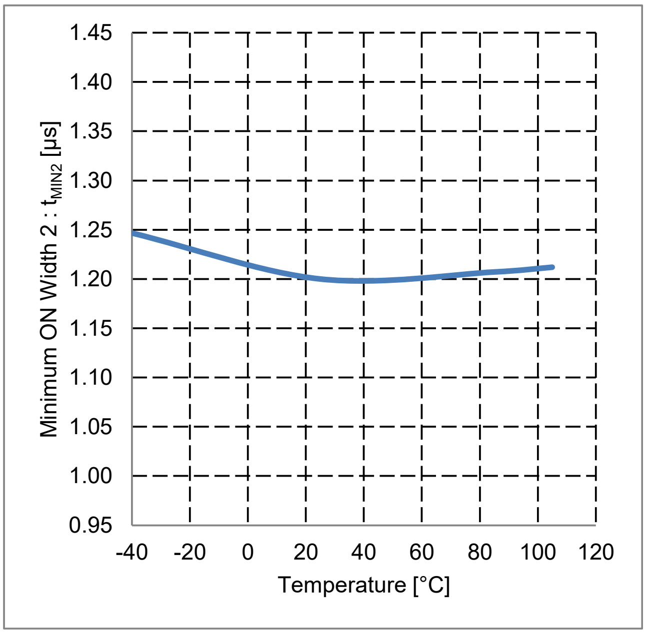


Figure 25. Minimum ON Width 2 vs Temperature

Typical Performance Curves - continued

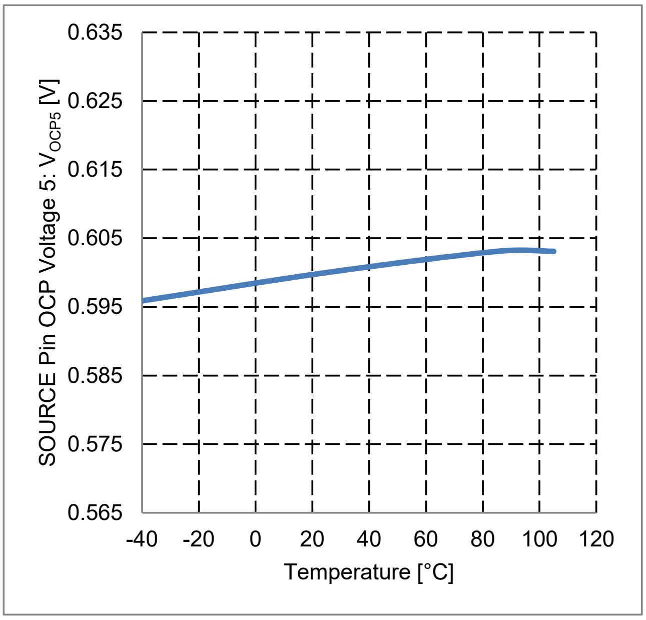


Figure 26. SOURCE Pin OCP Voltage 5 vs Temperature

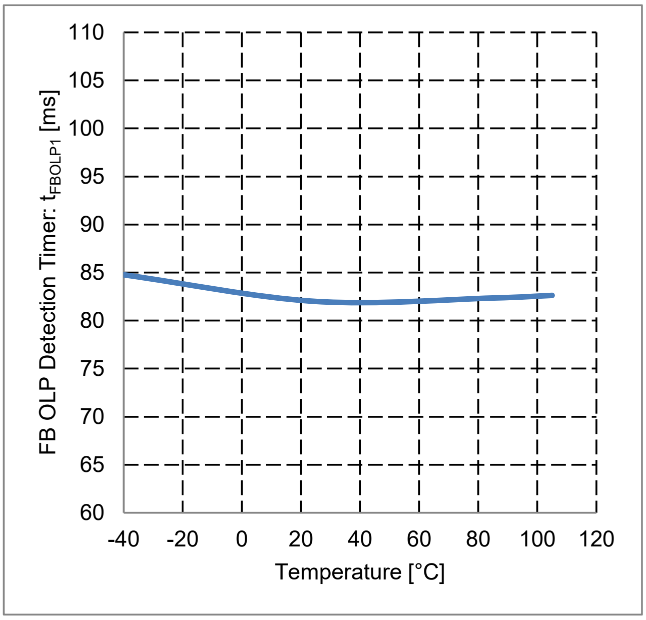
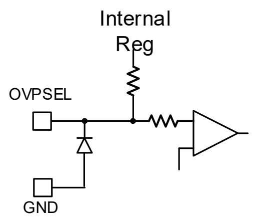
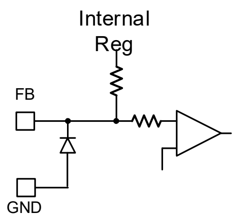
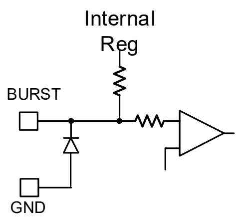
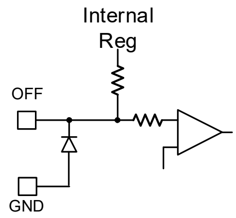
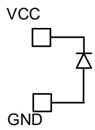
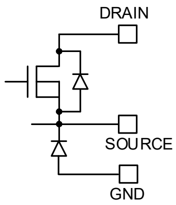
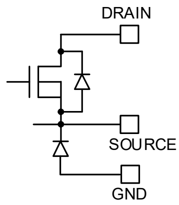
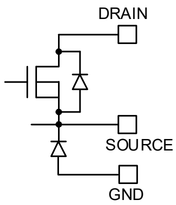
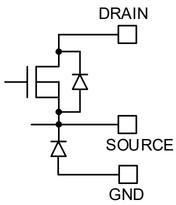
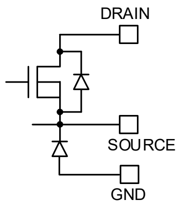
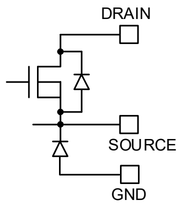
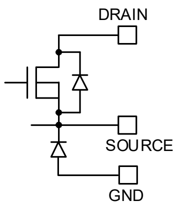
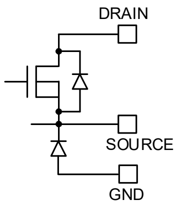
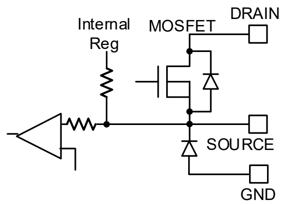
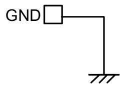
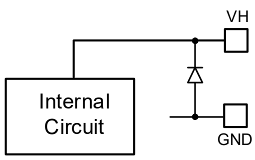


Figure 27. FB OLP Detection Timer vs Temperature

I/O Equivalence Circuit

Pin No.	Pin Name	Circuit
1	OVPSEL	
2	FB	
3	BURST	
4	OFF	
5	VCC	
6	N.C.	-
7	DRAIN	
8	DRAIN	
9	DRAIN	
10	DRAIN	
11	DRAIN	
12	DRAIN	
13	DRAIN	
14	DRAIN	
15	N.C.	-
16	SOURCE	
17	N.C.	-
18	GND	
19	N.C.	-
20	VH	

(Note) The N.C pin must be open on the board. It means not to connect GND etc.

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

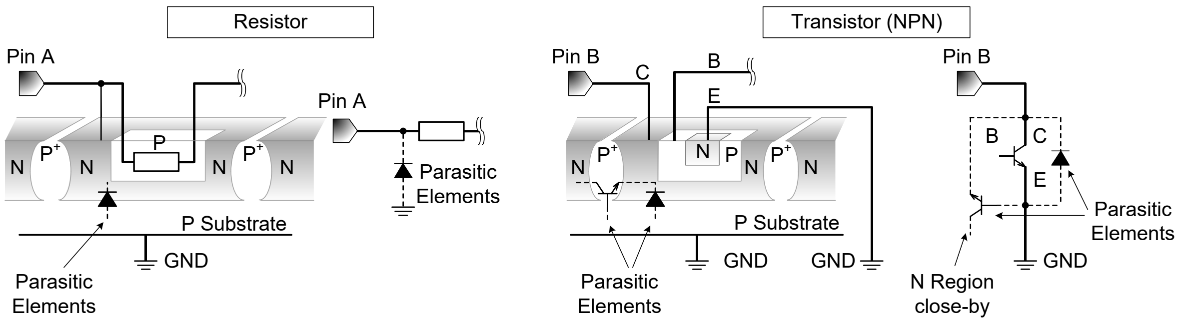


Figure 28. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

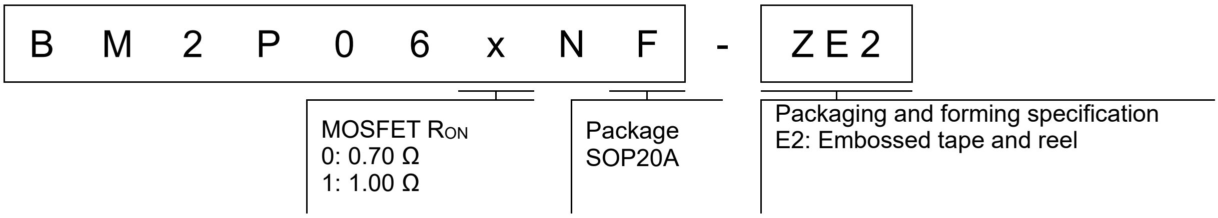
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

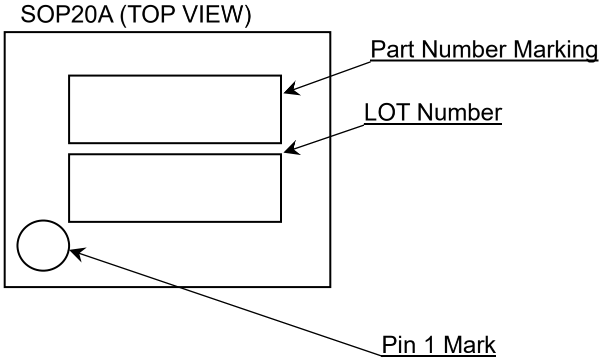
Ordering Information



Lineup

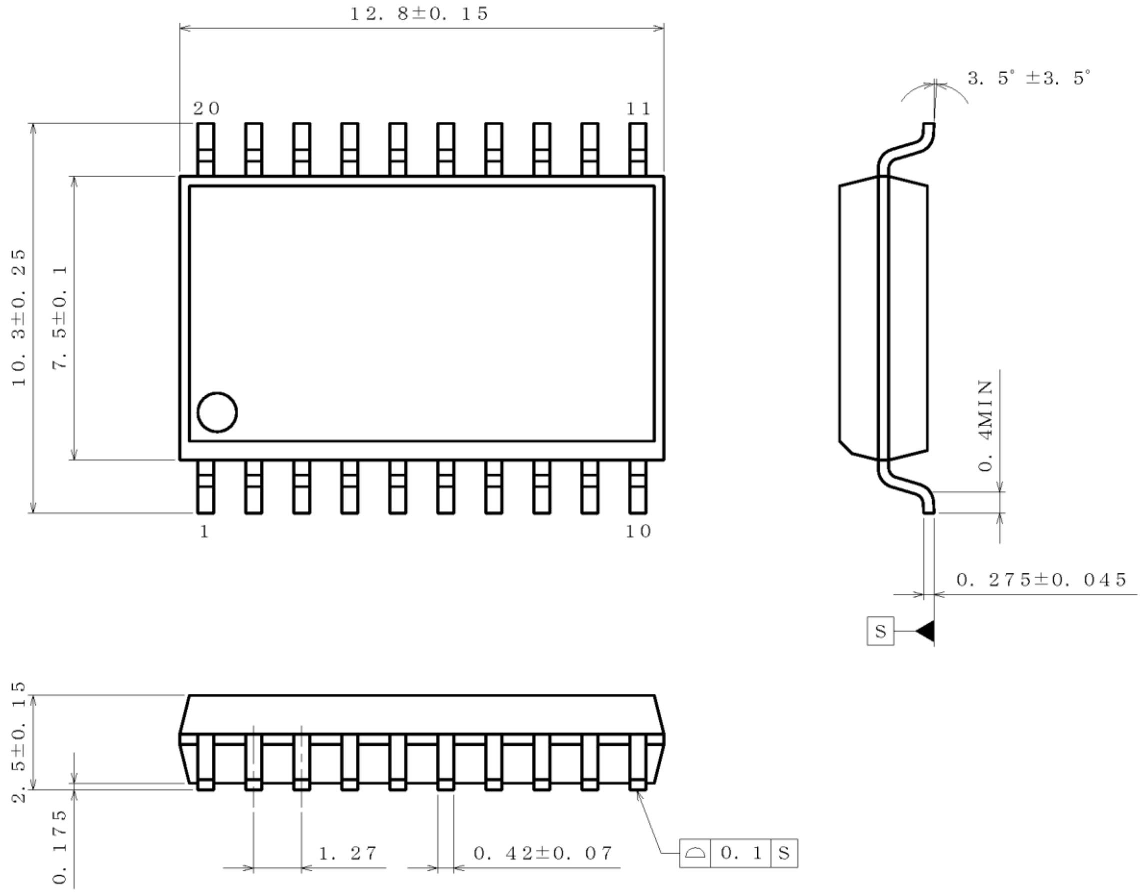
Part Number Marking	MOSFET R_{ON}	Package	Orderable Part Number
BM2P060NF	0.70 Ω	SOP20A	BM2P060NF-ZE2
BM2P061NF	1.00 Ω		BM2P061NF-ZE2

Marking Diagram



Physical Dimension and Packing Information

Package Name	SOP20A

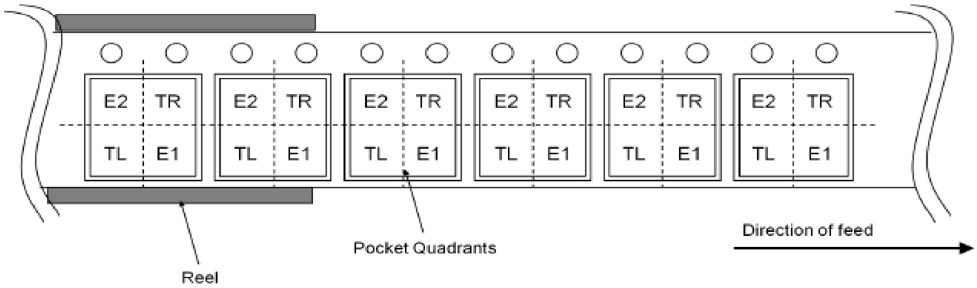


(UNIT : mm)

PKG : SOP20A
Drawing No. EX001−0095

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
18.Mar.2025	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property (“Specific Applications”), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM’s Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM’s Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM’s internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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