ROHM SEMICONDUCTOR

Datasheet

Boundary Conduction Mode

Power Factor Correction Controller IC Built-in 650 V GaN HEMT

BM3GF01MUV-LBZ BM3GF02MUV-LBZ

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.
BM3GF01MUV-LBZ, BM3GF02MUV-LBZ incorporates the 650 V GaN HEMT and power factor correction converter (Power Factor Correction: PFC) that serve as switching devices to provide a compact, optimal system for all products that require power factor improvement.
Boundary conduction mode control is adopted for the PFC IC and switching loss reduction and noise reduction are possible by zero current detection.
Built-in GaN HEMT contributes to miniaturization and high-efficiency.
Additionally, this IC enables external control of PFC ON/OFF by combining ROHM's QR IC with built-in GaN HEMT. It contributes to low standby power by stopping PFC during standby when PFC is not required.

Features

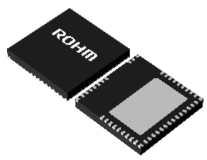
- Built-in 650 V Withstand Voltage GaN HEMT
- Built-in 650 V Startup Circuit
- Boundary Conduction Mode PFC
- Turn-off Slew Rate Adjusting Pin
- Built-in Low THD Circuit
- ON/OFF Control with PFCOFF Pin
- UVLO Function of VCC Pin
- ZCD by Auxiliary Winding
- Static OVP Function by VS Pin
- Error Amplifier Input Short Protection by VS Pin
- Over Voltage Boost Reduction Function at Startup
- Over Current Protection per Cycle

Key Specifications

- Power Supply Voltage Range
  - VCC Pin: 10 V to 38 V
  - DRAIN Pin: 650 V (Max)
- Operating Current:
  - BM3GF01MUV-LBZ 0.80 mA (Typ)
  - BM3GF02MUV-LBZ 0.90 mA (Typ)
- Current when PFC OFF state: 130 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C
- GaN HEMT D-S ON Resistor:
  - BM3GF01MUV-LBZ 150 mΩ
  - BM3GF02MUV-LBZ 70 mΩ

Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN41V8080K	8.0 mm x 8.0 mm x 1.0 mm Pitch 0.5 mm



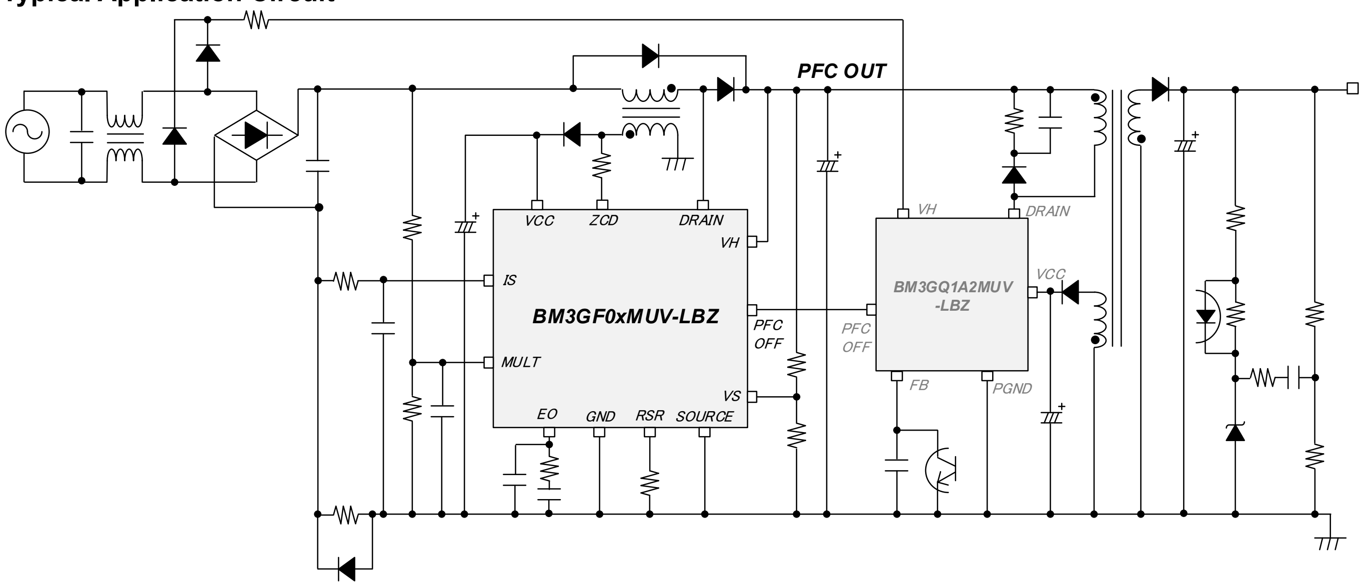
Lineup

Product Name	GaN HEMT D-S ON Resistor
BM3GF01MUV-LBZ	150 mΩ
BM3GF02MUV-LBZ	70 mΩ

Applications

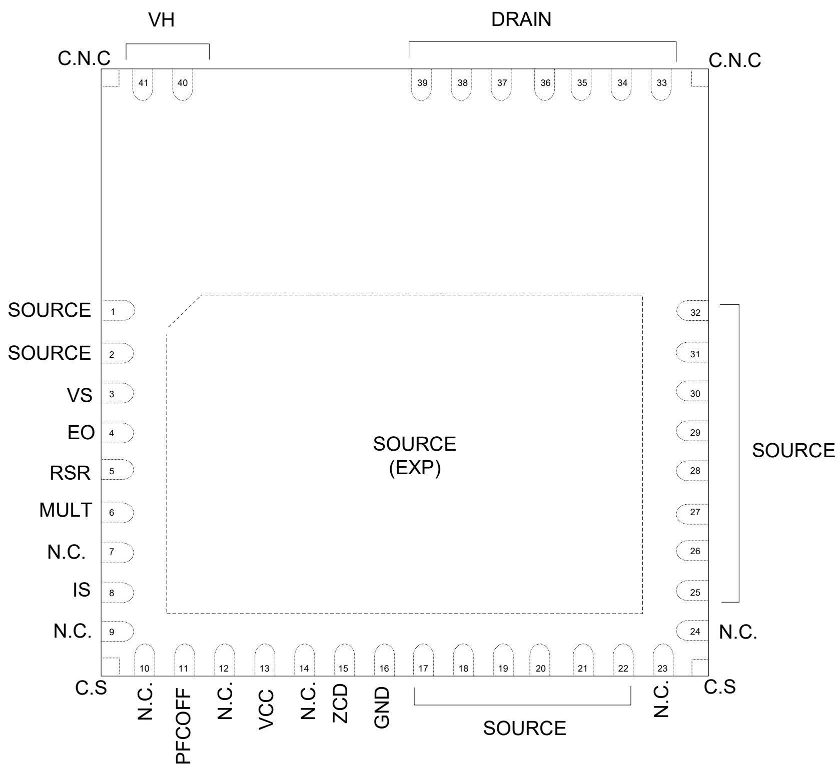
Industrial Equipment, AC Adapter etc.

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

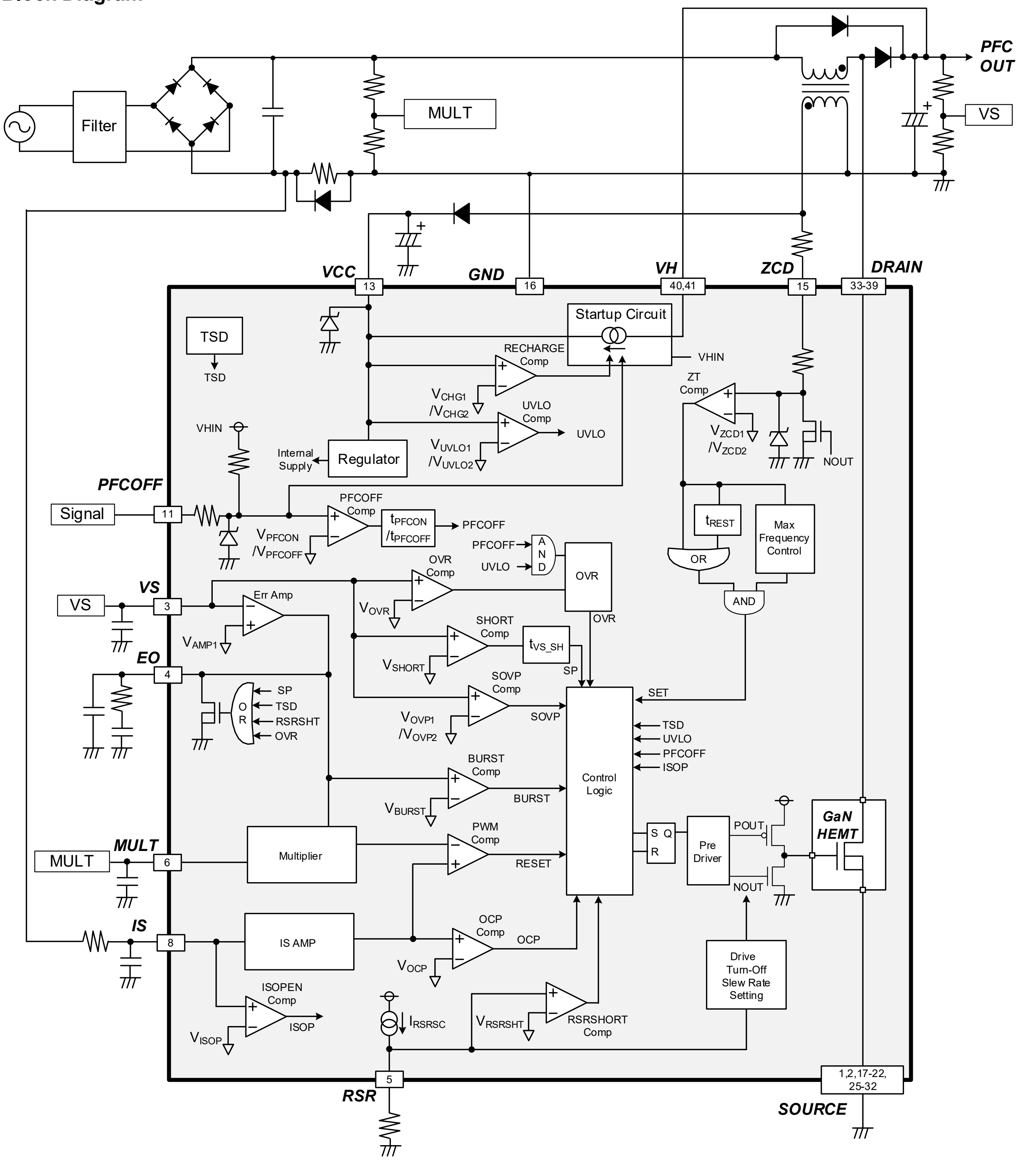


Pin Descriptions

Pin No.	Pin Name	I/O	Function
1, 2	SOURCE	I/O	GaN HEMT SOURCE pin
3	VS	I	Feedback input pin
4	EO	I/O	Error amplifier output pin
5	RSR	I	Turn-off slew rate adjusting pin
6	MULT	I	Multiplier input pin
7	N.C.	-	Non connected
8	IS	I	Over current detection pin
9, 10	N.C.	-	Non connected
11	PFCOFF	I	PFC ON/OFF setting pin
12	N.C.	-	Non connected
13	VCC	I	Power supply pin
14	N.C.	-	Non connected
15	ZCD	I	Zero current detection pin
16	GND	-	GND pin
17 to 22	SOURCE	I/O	GaN HEMT SOURCE pin
23, 24	N.C.	-	Non connected
25 to 32	SOURCE	I/O	GaN HEMT SOURCE pin
33 to 39	DRAIN	I	GaN HEMT DRAIN pin
40, 41	VH	I	Starter circuit pin
-	C.S	-	Corner pin *(Note 1) (Note 2)*
-	EXP	O	SOURCE pin *(Note 3)*
-	C.N.C	-	Corner pin, Non connected *(Note 2)*

(Note 1) Internally connected to SOURCE pin.
(Note 2) Do not connect to other pins.
(Note 3) It is connected to the SOURCE pin internally but also connects to the SOURCE pin on the PCB.

Block Diagram



Description of Blocks

1 Startup Circuit

This IC has a built-in startup circuit. It enables low standby power and high-speed startup.
When the PFCOFF pin voltage is H, I_{START1} to I_{START3} flow.
The consumption power after startup is only OFF current I_{START3}.
When the PFCOFF pin voltage is L, since only I_{START4} flows, the standby power is even lower.
If the PFCOFF pin is not used for control, leave the PFCOFF pin open.

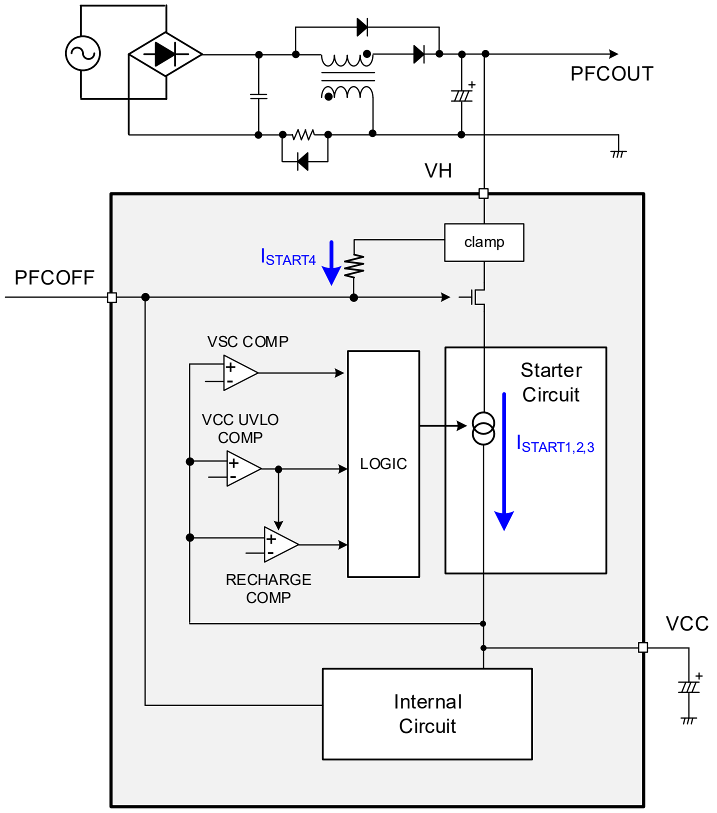


Figure 1. Block Diagram of Startup Circuit

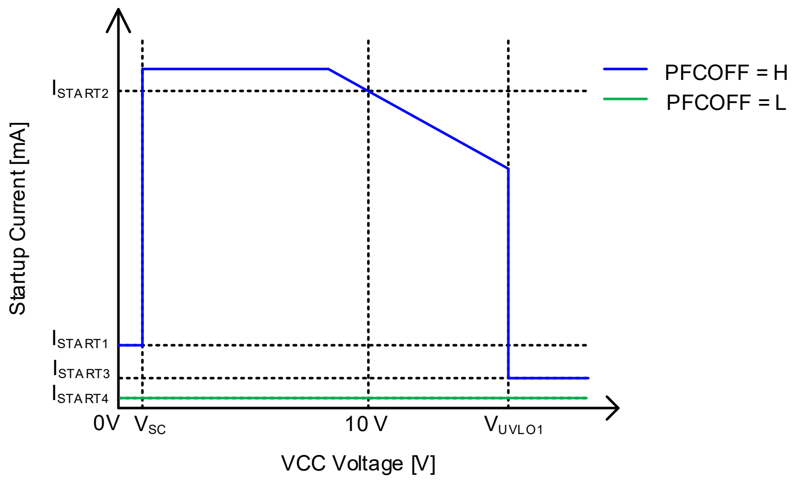


Figure 2. Startup Current vs VCC Pin Voltage

2 Enhancement Mode GaN HEMT

This IC is built-in enhancement mode (normally off) GaN device.
Compared to cascode topologies that connect depletion-mode (normally-on) GaN devices and Si MOSFET in series, enhancement-mode GaN devices have less parasitic inductance and switching loss introduced by the additional connection between the cascode-mode GaN devices and Si MOSFET. These characteristics provide better switching performance and are particularly noticeable in high-current applications.

Description of Blocks – continued

3 VCC Pin Protective Function

This IC has a built-in the VCC pin undervoltage protective function VCC UVLO (Under Voltage Lock Out) and VCC recharge function that operates when the VCC pin voltage drops.

3.1 VCC UVLO Function

Switching starts when the VCC pin voltage > V_{UVLO1}. When the VCC pin voltage < V_{UVLO2}, switching stops. At this time, the EO pin voltage is discharged to 0 V.

3.2 VCC Recharge Function

Once the VCC pin voltage > V_{UVLO1} and the IC starts, then when the VCC pin voltage < V_{CHG1}, the VCC recharge function operates. At this time, the VCC pin is charged from the VH pin through startup circuit. This operation does not cause VCC startup failure.
When the VCC pin voltage is charged and the VCC pin voltage > V_{CHG2}, charging ends.

4 PFC ON/OFF Function

This IC can be used to external control of PFC ON/OFF by combining with ROHM's QR IC with built-in GaN HEMT for. This function contributes to low standby power consumption by stopping PFC during standby when PFC is not required.

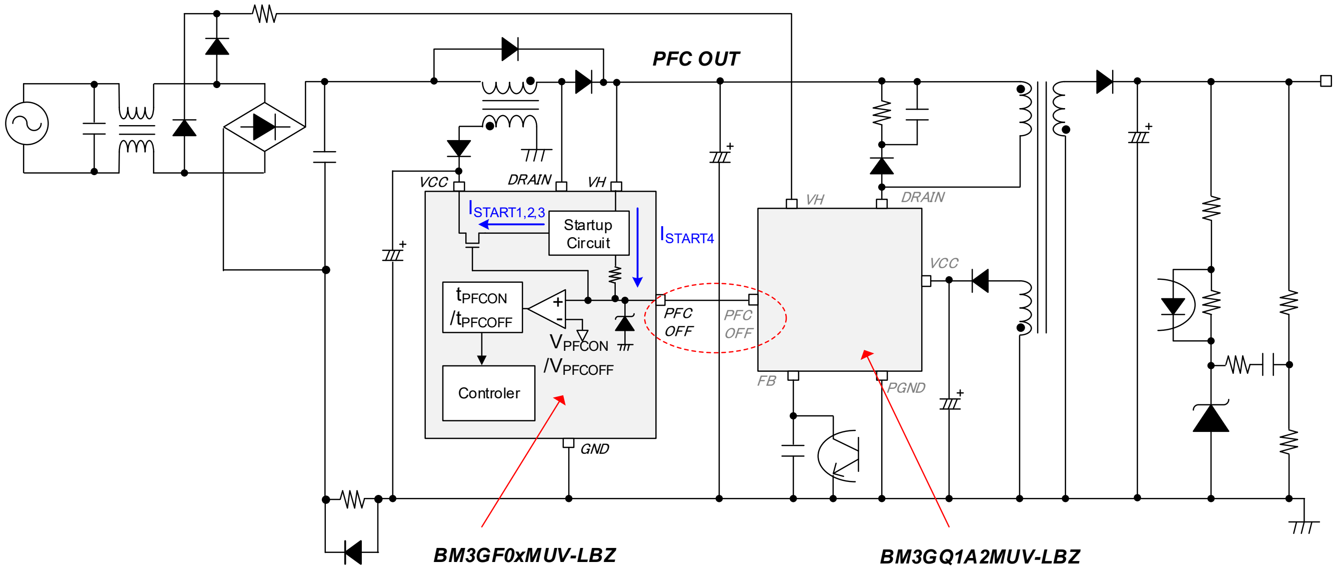


Figure 3. PFCOFF Pin Block Diagram

When the PFCOFF pin voltage < V_{PFCOFF}, PFC is stopped after t_{PFCOFF}. At this time, the current line between the VCC pin and the VH pin is cut off, so the IC's standby current consumption is only I_{START4}. The EO pin voltage is discharged to 0 V.
When the PFCOFF pin voltage > V_{PFCON}, PFC switches to ON after t_{PFCON}.

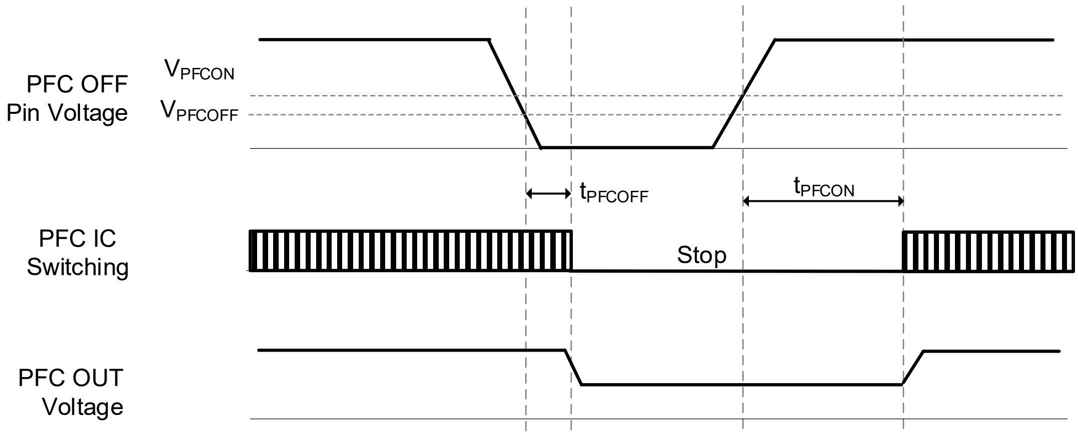


Figure 4. PFC ON/OFF Function

If you do not use this function, open the PFCOFF pin.
Because the PFCOFF pin has an input pull-up resistor, the PFCOFF pin voltage is H when the pin is open.

Description of Blocks – continued

5 PFC: Power Factor Correction Section

The power factor correction circuit is a voltage control method in the boundary conduction mode.
The schematic operation circuit diagram is shown in Figure 5, and the switching operation is shown in Figure 6.

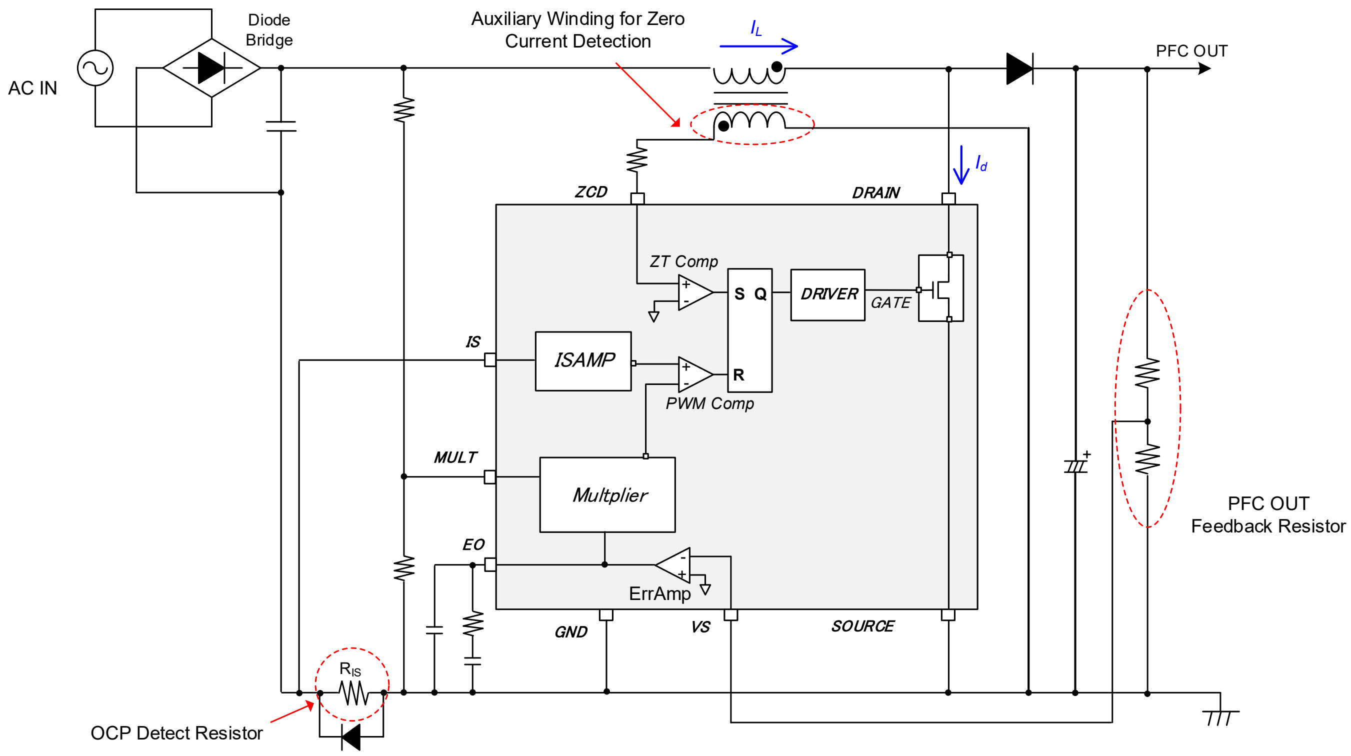


Figure 5. Operation Circuit Outline

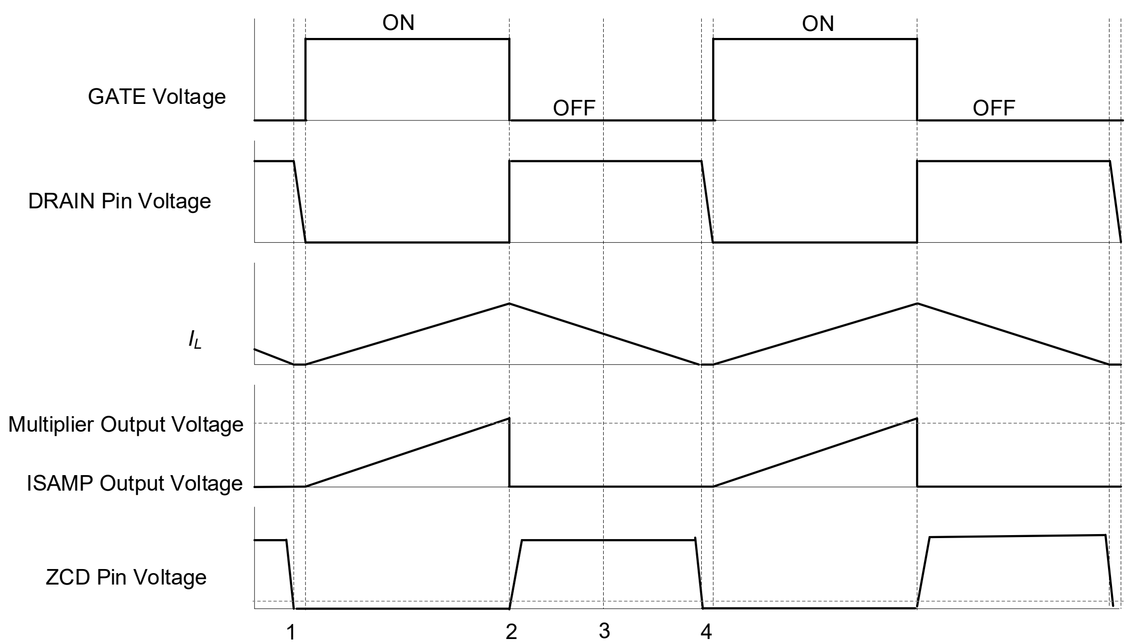


Figure 6. Switching Operation Timing Chart

Switching Operation

1. GaN HEMT is turned ON and inductor current I_L increases.
2. The IC compares Multiplier output voltage with the ISAMP output voltage, GaN HEMT is turned OFF when the generated signal voltage increases.
3. While GaN HEMT is turned OFF, I_L is decreased to 0 A.
4. The ZCD pin detects the zero point of the I_L, and GaN HEMT is turned ON.

Description of Blocks – continued

6 ErrAMP

6.1 GmAMP

The VS pin monitors the resistor divided point of the output voltage. The ripple voltage of AC-frequency (50 Hz / 60 Hz) is overlapped on the VS pin. GmAMP removes this ripple voltage and controls the EO pin voltage level according to the error between the removed voltage and V_{AMP1}. When the EO pin voltage rises, the DRAIN pin ON time becomes longer. When the EO pin voltage drops below V_{BURST}, the switching operation stops. Therefore, the switching operation can be stopped by forcibly shorting the EO pin to GND from the outside.
Set the error amplifier constants so that the AC frequency does not appear in the EO pin. In doing so, be sure to check in the actual application.

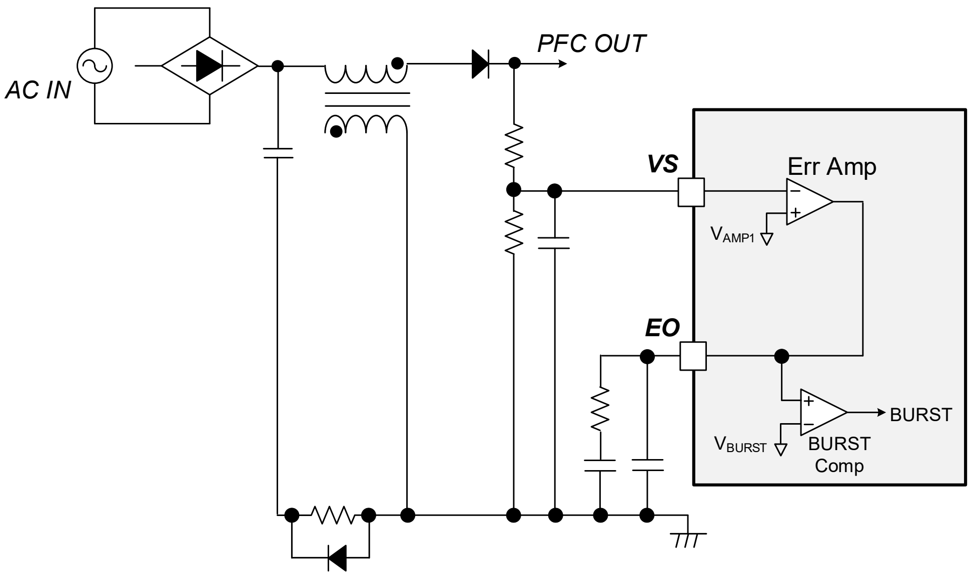


Figure 7. GmAMP Block Diagram

6.2 VS Short Protection Function (SP)

The VS pin has a short protection function. When the VS pin voltage < V_{SHORT} status continues for t_{VS_SH} or more, IC stops switching. At that time, the EO pin voltage is discharged to 0 V.

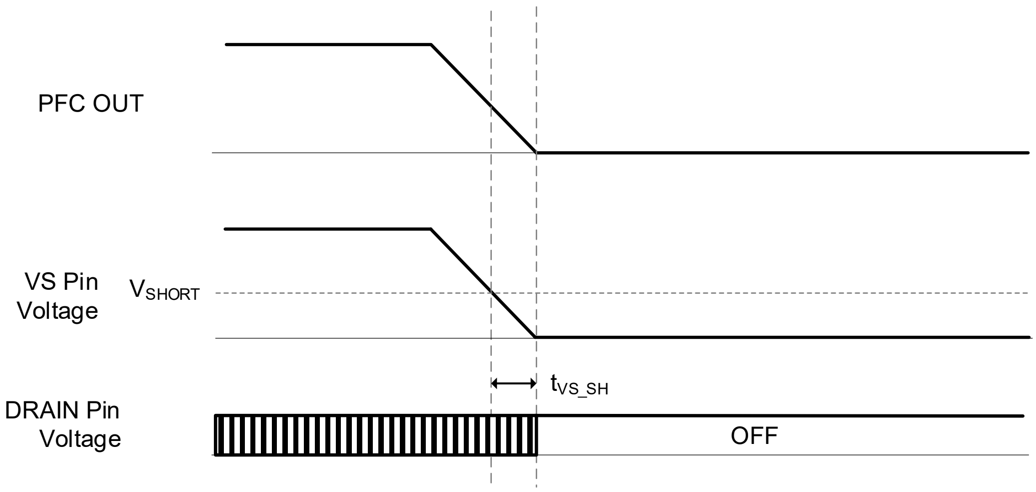


Figure 8. Operation of VS Short Protection

6 ErrAMP – continued

6.3 VS Over Voltage Protection Function (SOVP)

When the VS pin voltage > V_{OVP1}, switching is stopped immediately. When the VS pin < V_{OVP2}, switching starts.

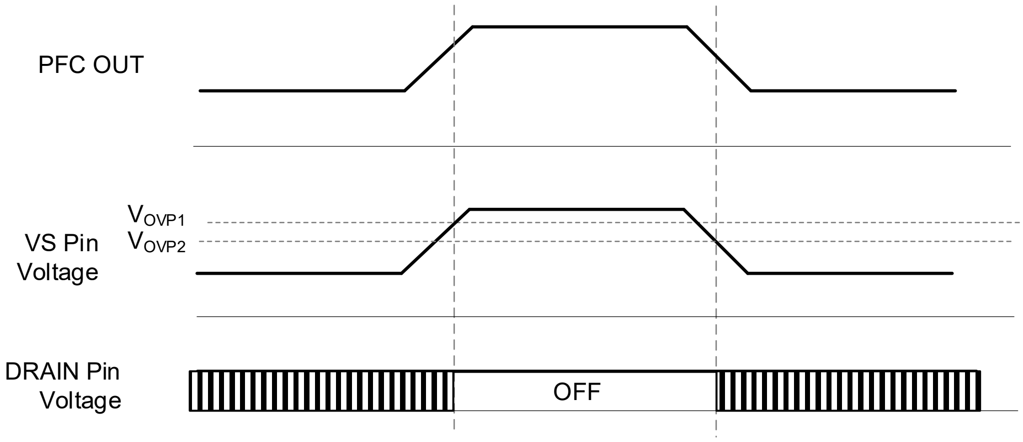


Figure 9. VS Over Voltage Protection Operation

6.4 Over Voltage Boost Reduction Function at Startup (OVR)

When the VS pin voltage rises to V_{OVR} (corresponding to -10 % of the output voltage) at startup, the EO pin voltage is forcibly discharged to V_{BURST}. When the EO pin voltage is low, the pulse width of the DRAIN pin becomes narrower, which slows the rise of the output voltage and reduces the over boost at startup. This function is valid only once after VCC UVLO is released or after switching operation by the PFCOFF pin is started.

Description of Blocks – continued

7 ZCD Pin

The zero current detection circuit is a function to detect a zero cross of the inductor current (refer to Figure 10, Figure 11).
After the ZCD pin voltage is higher than V_{ZCD1}, when the ZCD pin voltage is lower than V_{ZCD2}, the GATE output is turned to H after t_{ZCD}. If the ZCD pin voltage is less than V_{ZCD1}, the restart timer operation is operated.
In the operation, when the GATE is turned to L and it takes $t_{REST,}$ the GATE is turned to H (refer to Figure 12).
At light loads, the switching frequency becomes high, but since this IC is limited by f_{SWMAX}, zero cross detection operates at a frequency lower than f_{SWMAX}.

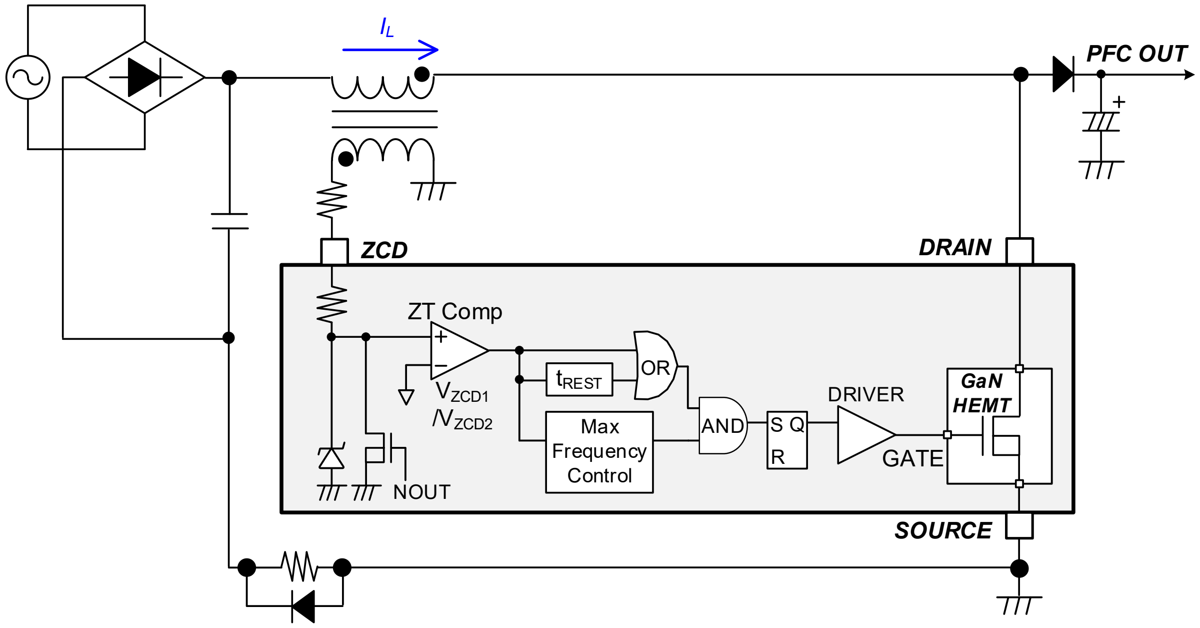


Figure 10. Zero Current Detection Circuit

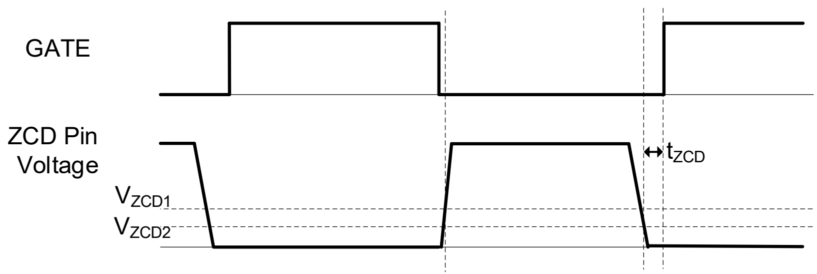


Figure 11. Zero Current Detection Operation

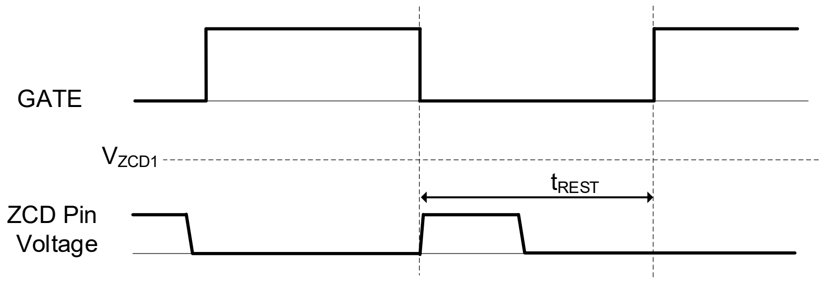


Figure 12. Restart Time Operation

Description of Blocks – continued

8 Multiplier

As shown in Figure 13, the DRAIN pin ON time is determined by Multiplier output and V_{IS}.
V_{IS} can be expressed in the following formula.

$$V_{IS} = -K \times V_{MULT} \times (V_{EO} - V_{BURST}) \qquad \text{[V]}$$

where:

K is the Multiplier gain
V_{MULT} is the MULT pin voltage
V_{EO} is the EO pin voltage
V_{BURST} is the burst voltage

The AC voltage of the MULT pin is input to V_{MULT}. This function improves the power factor by controlling the AC current along with the AC voltage.
Multiplier has an offset voltage. This offset voltage causes the GATE ON width to become longer when the AC voltage is 0 V (V_{MULT} = 0 V).
The diode-bridge output voltage can be discharged more by increasing the ON time. This improves the AC current distortion because current supplied from the diode-bridge is less likely to stop (refer to Figure 13).

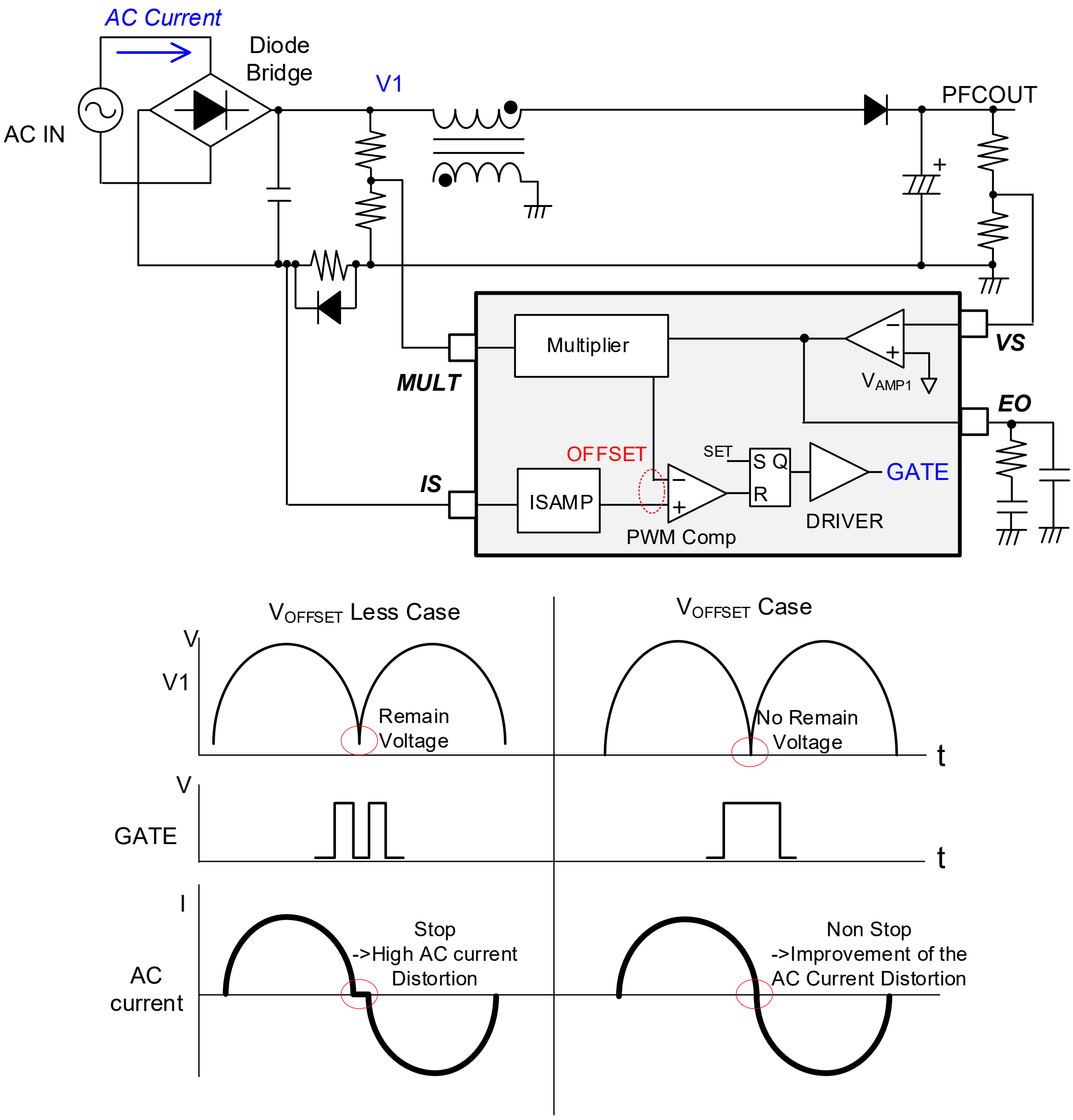


Figure 13. Improvement of the AC Current Distortion

Description of Blocks – continued

9 Over Current Protect Function (OCP)

In the normal operation, turn OFF is determined by the ON time determined from the EO pin voltage and the MULT pin voltage.
However, when the IS pin voltage < V_{OCP}, over current protection is operated and the GATE is turned OFF per pulse. This protection prevents over current to GaN HEMT.
Since the over current protection function is operated to limit the ON time, the PFC output voltage drops when PFC load is heavy and operate this protective function.

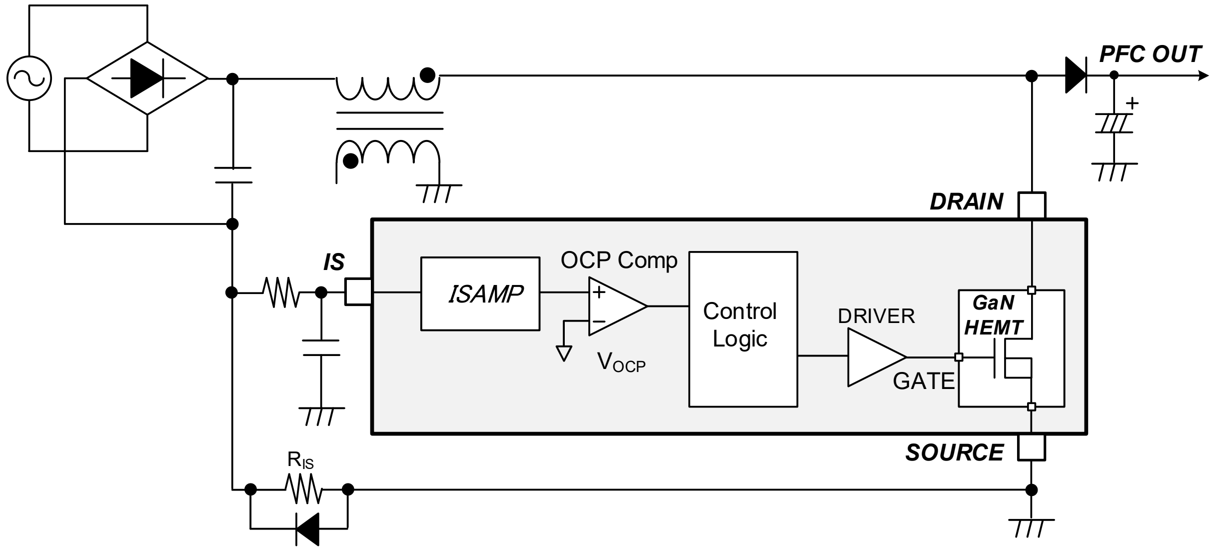


Figure 14. Current Limit Operation

10 IS Pin Open Protection (ISOP)

If the IS pin becomes open, excessive heat may cause IC destruction.
To prevent damage, this IC built-in Open protection circuit (auto recovery protection).
Switching stops when the IS pin voltage > V_{ISOP}.

11 RSR Pin Function

The RSR pin is able to be adjusted GaN HEMT turn-off slew rate. Depending on the resistor connected to the RSR pin, turn-off slew rate can be adjusted. The slew rate of turn ON is fixed.
The RSR pin resistor is needed to connect 10 kΩ or more. When the RSR pin is open, the turn-off slew rate is SR1.
The RSR pin also has a built-in short circuit protection. Switching operation stops when the RSR pin voltage < V_{RSRSHT}. At this time, the EO pin voltage is discharged to 0 V.

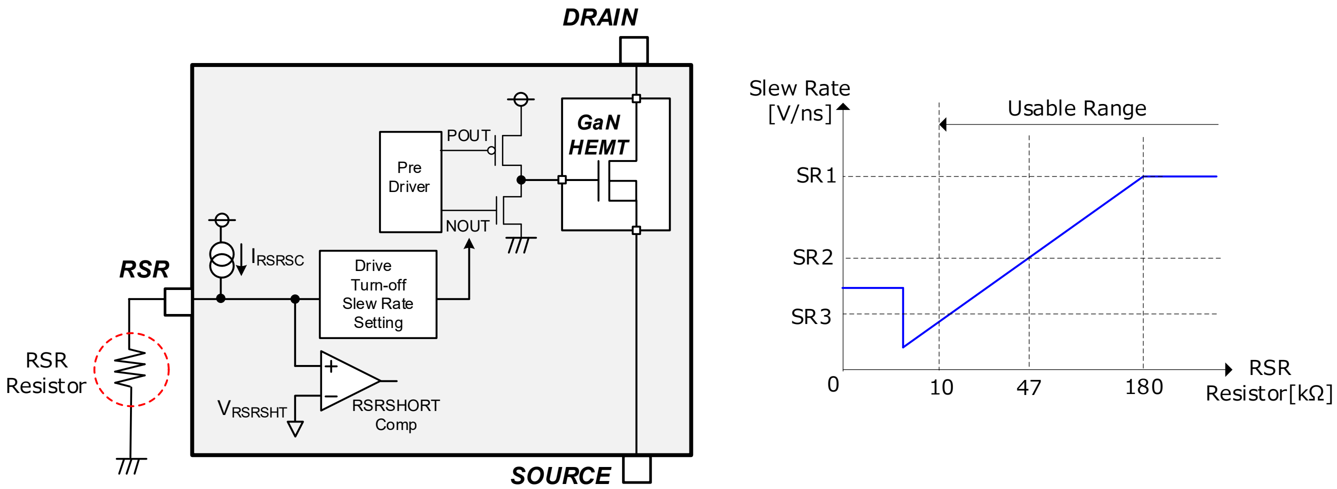


Figure 15. Turn-off Slew Rate Adjust Function

12 TSD

Thermal shutdown function is auto restart type. Thermal shutdown function is worked when the junction temperature becomes more than T_{SD1}, switching is stopped. At this time, the EO pin voltage is discharged to 0 V.
Switching restart when the junction temperature becomes less than T_{SD2}.

Operation Mode of the Protection Circuit

Table 1 shows the operation modes of the protective functions.

Table 1. Operation Mode of Each Protective Circuit

Item	Content	Protective Action			
		Detection Method	Operation at Detection	How to Cancel	Operation at Release
VCC UVLO	VCC pin Undervoltage Protection Function	$VCC < V_{UVLO2}$ (when VCC falls)	Switching stop EO pin voltage discharge	$VCC > V_{UVLO1}$ (when VCC rises)	Start of starting operation
OCP	Overcurrent Protection Function	$IS < V_{OCP}$ (at IS falls)	Switching stop	Each cycle	Normal operation
ISOP	IS Pin Open Protection Function	$IS > V_{ISOP}$ (when IS rises)	Switching stop	$IS < V_{ISOP}$ (when IS falls)	Normal operation
SP	VS Pin Short Protection Function	$VS < V_{SHORT}$ (when VS falls)	Switching stop EO pin voltage discharge	$VS > V_{SHORT}$ (when VS rises)	Normal operation
SOVP	VS Pin Overvoltage Protection Function	$VS > V_{OVP1}$ (when VS rises)	Switching stop	$VS < V_{OVP2}$ (when VS falls)	Normal operation
RSRSHT	RSR Pin Short Protection Function	$RSR < V_{RSRSHT}$	Switching stop EO pin voltage discharge	$RSR > V_{RSRSHT}$	Normal operation
TSD	Thermal Shutdown	$Tj > T_{SD1}$	Switching stop EO pin voltage discharge	$Tj < T_{SD2}$	Normal operation

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit	Conditions
Maximum Voltage 1	V_{MAX1A}	-0.3 to +650	V	DRAIN pin voltage, VH pin voltage
	V_{MAX1B}	-0.3 to +800	V	DRAIN pin voltage (tpulse < 1 μs)(Note 1)
Maximum Voltage 2	V_{MAX2}	-0.3 to +40	V	VCC pin
Maximum Voltage 3	V_{MAX3}	-0.3 to +6.5	V	SOURCE pin, MULT pin, VS pin, EO pin, RSR pin, PFCOFF pin
Maximum Voltage 4	V_{MAX4}	-4.0 to +0.3	V	IS pin
Maximum Current 1 BM3GF01MUV-LBZ	$I_{D1(RMS)}$	13.4	A	DRAIN pin RMS current
	$I_{D1(PULSE)}$	42.3	A	DRAIN pin pulse current (tpulse < 1 μs)(Note 1)
Maximum Current 2 BM3GF02MUV-LBZ	$I_{D2(RMS)}$	20.9	A	DRAIN pin RMS current
	$I_{D2(PULSE)}$	66.1	A	DRAIN pin pulse current (tpulse < 1 μs)(Note 1)
Maximum Current 3	I_{ZCD1}	-3 to +3	mA	ZCD current
Maximum Junction Temperature	Tjmax	+150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Duty is less than 1 %.

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
VQFN41V8080K				
Junction to Ambient	θ_{JA}	87.7	25.8	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	30.6	12.7	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5,7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Voltage Range	V_{CC}	10	15	38	V	VCC pin voltage
Operating Temperature	Topr	-40	+25	+125	°C	

Recommended External Range (Tj = 25 °C)

Parameter	Symbol	Range	Unit
VCC Pin Connecting Capacitance	C_{VCC}	10 to	μF
RSR Pin Connecting Resistor	R_{RSR}	12 to	kΩ
IS Pin Filter Resistor	R_{ISFIL}	to 2.0	kΩ

Electrical Characteristics (Unless otherwise specified Tj = -40 °C to +125 °C, V_{CC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[GaN HEMT]						
DRAIN-SOURCE Withstand Voltage	$V_{(BR)DSS1}$	650	-	-	V	VCC pin voltage = 0 V
	$V_{(BR)DSS2}$	800	-	-	V	VCC pin voltage = 0 V tpulse < 1 µs (Note 1)
DRAIN Pin Leakage Current	I_{DSS1}	-	-	100	µA	V_{DS} = 650 V, Tj = 25 °C
	I_{DSS2}	-	4.5	-	µA	V_{DS} = 650 V, Tj = 150 °C
DRAIN-SOURCE ON Resistor 1	$R_{DS1A(ON)}$	-	150	195	mΩ	I_D = 0.5 A VCC pin voltage = 15 V Tj = 25 °C BM3GF01MUV-LBZ
	$R_{DS1H(ON)}$	-	295	-	mΩ	I_D = 0.5 A VCC pin voltage = 15 V Tj = 150 °C BM3GF01MUV-LBZ
DRAIN-SOURCE ON Resistor 2	$R_{DS2A(ON)}$	-	70	85	mΩ	I_D = 0.5 A VCC pin voltage = 15 V Tj = 25 °C BM3GF02MUV-LBZ
	$R_{DS2H(ON)}$	-	135	-	mΩ	I_D = 0.5 A VCC pin voltage = 15 V Tj = 150 °C BM3GF02MUV-LBZ
SOURCE-DRAIN Reverse Voltage	V_{SD}	-	3.5	-	V	I_D = 9.5 A VCC pin voltage = 0 V
Output Capacity 1	C_{OSS1}	-	24.5	-	pF	VCC pin voltage = 0 V V_D = 400 V f = 1 MHz
Output Capacity 2	C_{OSS2}	-	49.9	-	pF	VCC pin voltage = 0 V V_D = 400 V f = 1 MHz
[Circuit Current]						
Circuit Current (ON)1A	I_{ON1A}	-	0.70	1.20	mA	VS pin voltage = 0 V BM3GF01MUV-LBZ
Circuit Current (ON)1B	I_{ON1B}	-	0.75	1.25	mA	VS pin voltage = 0 V BM3GF02MUV-LBZ
Circuit Current (ON)2A	I_{ON2A}	-	0.80	1.50	mA	At 50 kHz switching BM3GF01MUV-LBZ
Circuit Current (ON)2B	I_{ON2B}	-	0.90	1.60	mA	At 50 kHz switching BM3GF02MUV-LBZ
Circuit Current (ON)3	I_{ON3}	70	130	230	µA	PFC OFF state
[VCC Protective Function]						
VCC UVLO Voltage1	V_{UVLO1}	12	13	14	V	At VCC pin voltage rising
VCC UVLO Voltage2	V_{UVLO2}	7	8	9	V	At VCC pin voltage falling
VCC UVLO Hysteresis	V_{UVLO3}	-	5	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
VCC Pin Recharge Start Voltage	V_{CHG1}	8	9	10	V	
VCC Pin Recharge Stop Voltage	V_{CHG2}	9	10	11	V	
TSD Temperature 1	T_{SD1}	150	175	200	°C	At temperature rising
TSD Temperature 2	T_{SD2}	-	150	-	°C	At temperature falling
[Gm Amplifier Block]						
VS Pin Pull-up Current	I_{VS}	-	0.1	0.5	µA	VS pin voltage = 0 V
Gm Amplifier Reference Voltage 1	V_{AMP1}	2.465	2.500	2.535	V	Tj = 25 °C
Gm Amplifier Reference Voltage 2	V_{AMP2}	2.455	2.500	2.545	V	Tj = -40 °C to +125 °C
Gm Amplifier Reference Voltage Line Regulation	V_{AMP_LINE}	-	-	10	mV	VCC pin voltage = 10 V to 38 V
Gm Amplifier Transconductance	T_{VS}	80	100	130	µA/V	EO pin voltage = 2.5 V Tj = 25 °C
Gm Amplifier Source Current	I_{EO_SOURCE}	6.25	12.50	25.00	µA	VS pin voltage = 2.3 V
Gm Amplifier Sink Current	I_{EO_SINK}	6.25	12.50	25.00	µA	VS pin voltage = 2.7 V

(Note 1) Duty is less than 1 %

Electrical Characteristics (Unless otherwise specified Tj = -40 °C to +125 °C, V_{CC} = 15 V) – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[EO Block]						
EO Pin L Voltage	V_{EOL}	-	1.6	1.8	V	VS pin voltage = 2.7 V
Burst Voltage	V_{BURST}	1.8	1.9	-	V	
EO Pin Discharge Current	I_{EO}	0.8	1.8	3.6	mA	VCC pin voltage = 12 V EO pin voltage = 1.0 V
[MULT Block]						
MULT Pin Pull-up Current	I_{MULT}	-	0.12	0.50	µA	MULT pin voltage = 0 V
MULT Pin Operating Voltage Range	V_{MULT}	0 to 2.5	0 to 3.5	-	V	
EO Pin Operating Voltage Range	V_{EOD}	V_{BURST} to 2.9	V_{BURST} to 3.4	-	V	
Multiplier Gain	K	0.09	0.14	0.19	1/V	MULT pin voltage = 0.5 V EO pin voltage = 3.0 V
[ZCD Block]						
ZCD Pin Threshold Voltage 1	V_{ZCD1}	0.8	0.9	1.0	V	At ZCD pin voltage rising
ZCD Pin Threshold Voltage 2	V_{ZCD2}	0.55	0.67	0.79	V	At ZCD pin voltage falling
ZCD Pin Output Delay Time	t_{ZCD}	-	200	520	ns	
Input Clamp Voltage (High)	V_{IH}	6.2	6.8	-	V	Sink current = 3 mA
Input Clamp Voltage (Low)	V_{IL}	-0.40	-0.18	-	V	Source current = -3 mA
Restart Timer	t_{REST}	15	30	45	µs	
Max Switching Frequency	f_{SWMAX}	225	250	275	kHz	Tj = 25 °C
[VS Protection Block]						
VS Pin Short Protection Detection Voltage	V_{SHORT}	0.090 x V_{AMP1}	0.120 x V_{AMP1}	0.150 x V_{AMP1}	V	
VS Pin Short Protection Detection Time	t_{VS_SH}	50	150	300	µs	
Overvoltage Boost Reduction Detection Voltage at Startup	V_{OVR}	-	0.9 x V_{AMP1}	-	V	
VS Pin Overvoltage Protection Detection Voltage 1	V_{OVP1}	1.065 x V_{AMP1}	1.080 x V_{AMP1}	1.095 x V_{AMP1}	V	At VS pin voltage rising Tj = 25 °C
VS Pin Overvoltage Protection Detection Voltage 2	V_{OVP2}	1.020 x V_{AMP1}	1.040 x V_{AMP1}	1.060 x V_{AMP1}	V	At VS pin voltage falling Tj = 25 °C
[IS Block]						
Over Current Protect Voltage	V_{OCP}	-0.415	-0.400	-0.385	V	
Output Delay Time	t_{DELAY}	-	400	600	ns	
IS Pin Source Current	I_{IS_SOURCE}	-	10	-	µA	IS pin voltage = 0 V
IS Pin Open Protection Detection Voltage	V_{ISOP}	0.05	0.20	0.35	V	

Electrical Characteristics (Unless otherwise specified Tj = -40 °C to +125 °C, V_{CC} = 15 V) – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[PFCOFF Block]						
PFC ON Voltage	V_{PFCON}	1.5	1.6	1.7	V	
PFC OFF Voltage	V_{PFCOFF}	1.3	1.4	1.5	V	
PFC ON/OFF Hysteresis	V_{PFCHYS}	-	0.20	-	V	
PFC ON Delay Time	t_{PFCON}	1.15	1.92	2.70	ms	
PFC OFF Delay Time	t_{PFCOFF}	50	100	150	µs	
[RSR Block]						
Turn-off Slew Rate 1	SR1	-	30	-	V/ns	RSR pin open V_D = 400 V *(Note 2)*
Turn-off Slew Rate 2	SR2	-	11	-	V/ns	RSR pin = 47 kΩ V_D = 400 V *(Note 2)*
Turn-off Slew Rate 3	SR3	-	5	-	V/ns	RSR pin = 10 kΩ V_D = 400 V *(Note 2)*
RSR Pin Short Detection Voltage	V_{RSRSHT}	0.015	0.040	0.065	V	
RSR Pin Source Current	I_{RSRSC}	7	10	13	µA	
[Startup Circuit Block]						
Startup Current 1	I_{START1}	0.1	0.3	1.0	mA	VCC pin voltage = 0 V Tj = 25 °C
Startup Current 2	I_{START2}	1.0	3.0	6.0	mA	VCC pin voltage = 10 V Tj = 25 °C
OFF Current	I_{START3}	-	32	50	µA	The inrush current from the DRAIN pin after releasing UVLO (at MOSFET OFF)
OFF Current_PFCOFF Mode	I_{START4}	-	4	15	µA	PFCOFF pin = L
Startup Current Switching Voltage	V_{SC}	0.7	1.1	1.5	V	Tj = 25 °C

(Note 2) No shipping inspection

Typical Performance Curves

(Reference Data)

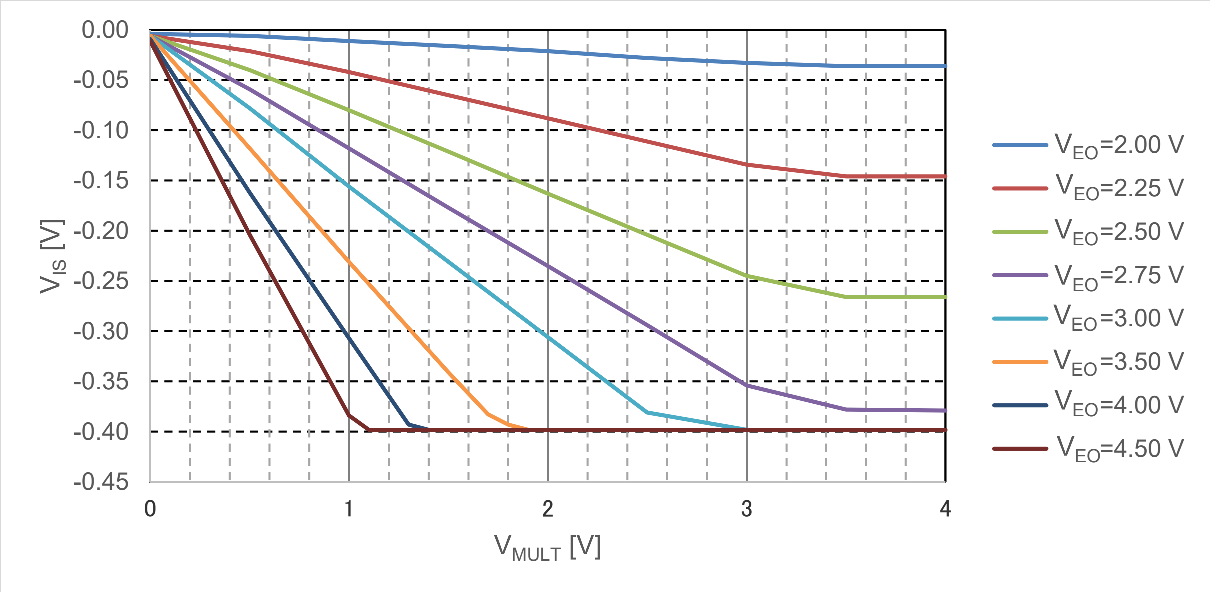


Figure 16. V_{IS} vs V_{MULT}

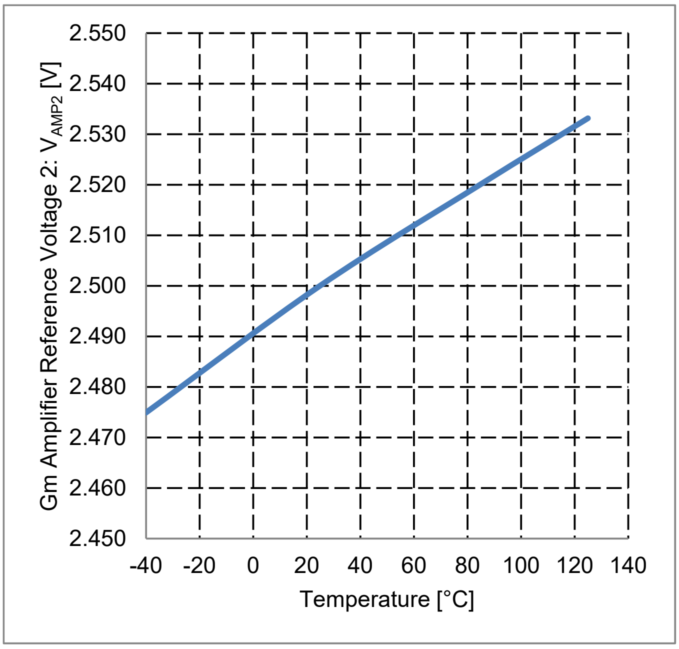


Figure 17. Gm Amplifier Reference Voltage 2 vs Temperature

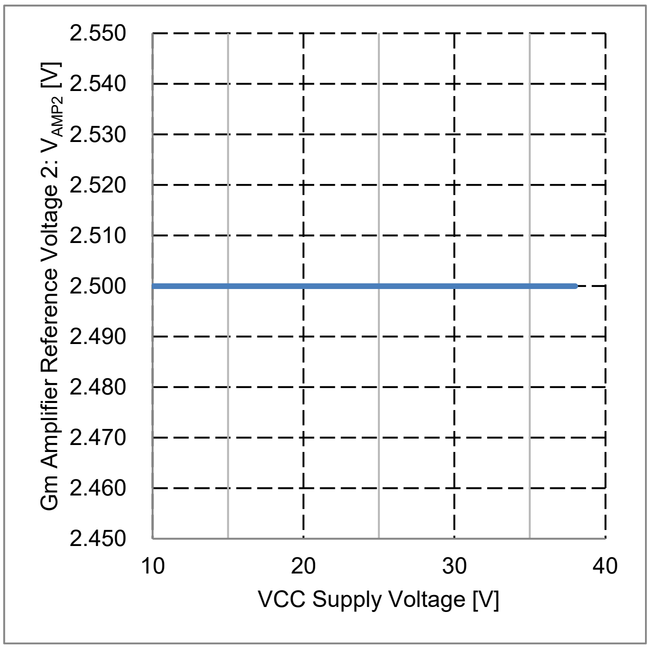


Figure 18. Gm Amplifier Reference Voltage 2 vs VCC Supply Voltage

Typical Performance Curves – continued
(Reference Data)

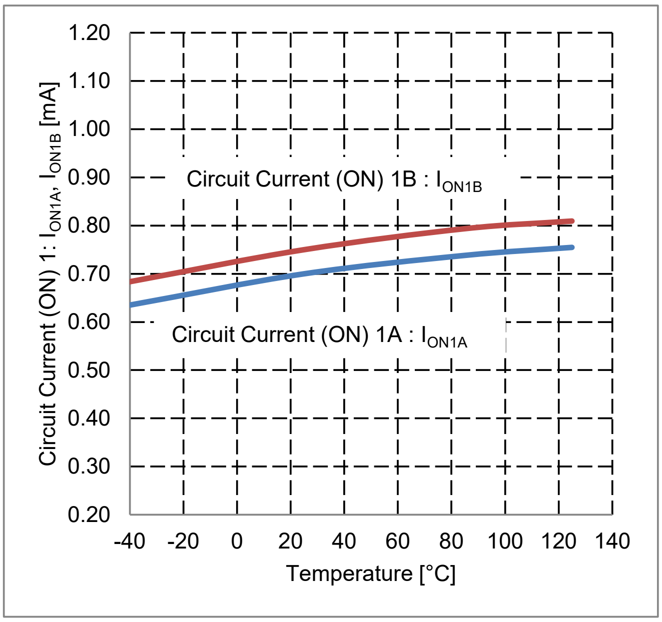


Figure 19. Circuit Current (ON) 1 vs Temperature

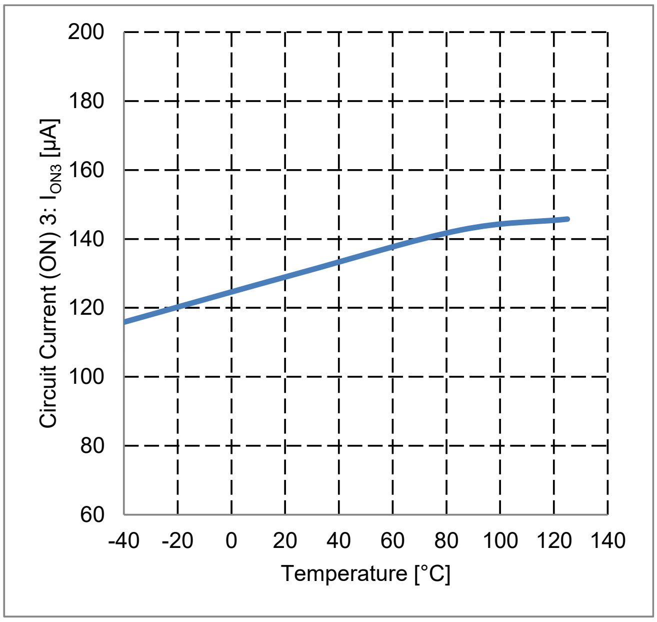


Figure 20. Circuit Current (ON) 3 vs Temperature

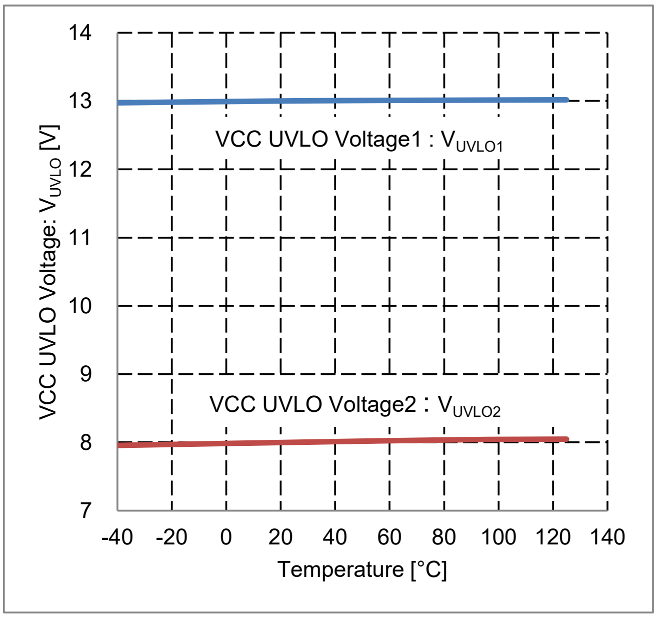


Figure 21. VCC UVLO Voltage vs Temperature

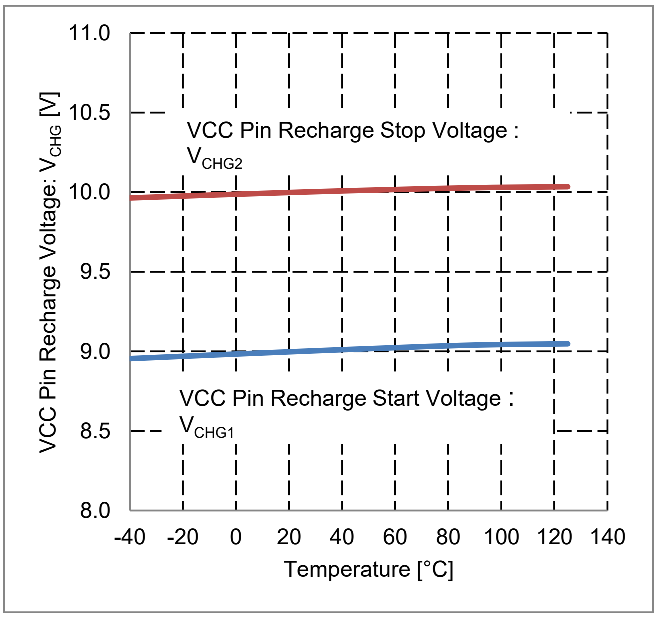


Figure 22. VCC Pin Recharge Voltage vs Temperature

Typical Performance Curves – continued

(Reference Data)

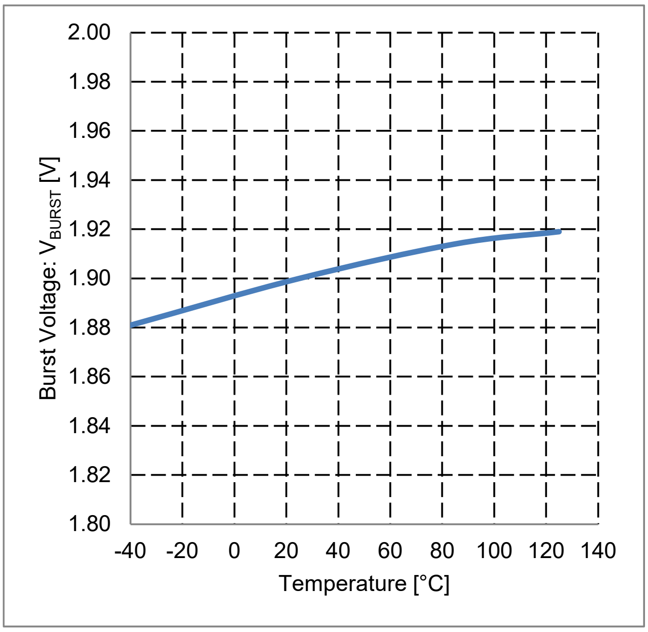


Figure 23. Burst Voltage vs Temperature

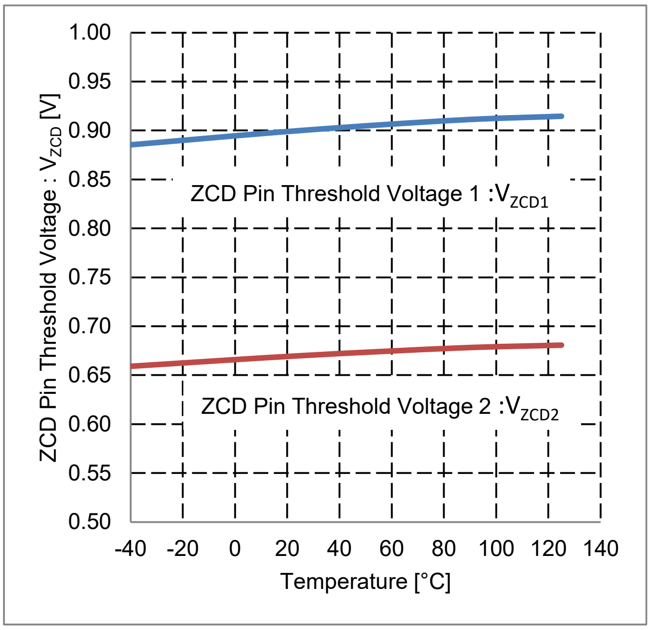


Figure 24. ZCD Pin Threshold Voltage vs Temperature

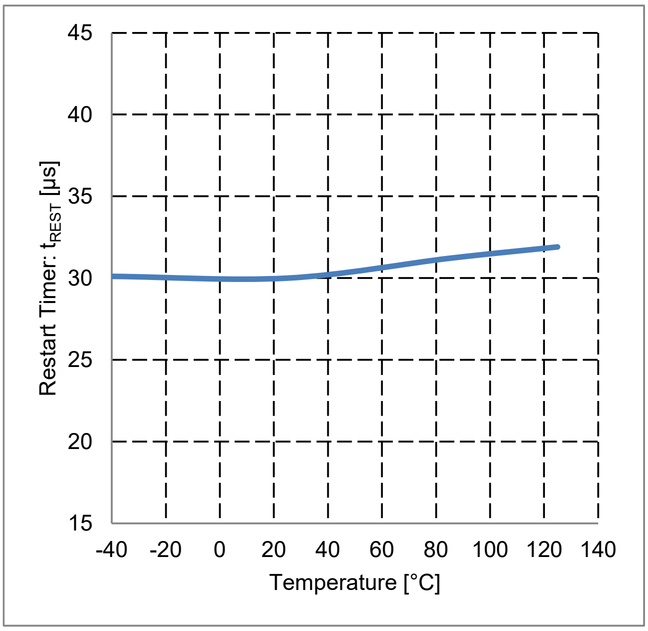


Figure 25. Restart Timer vs Temperature

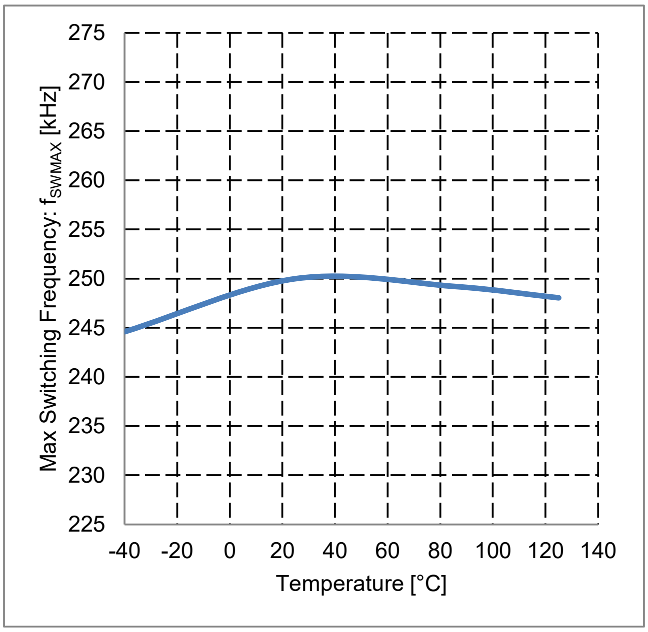


Figure 26. Max Switching Frequency vs Temperature

Typical Performance Curves – continued

(Reference Data)

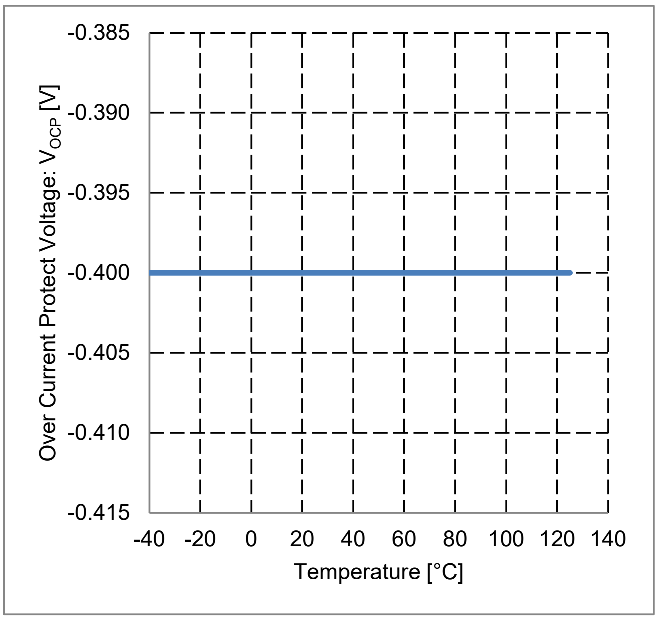


Figure 27. Over Current Protect Voltage vs Temperature

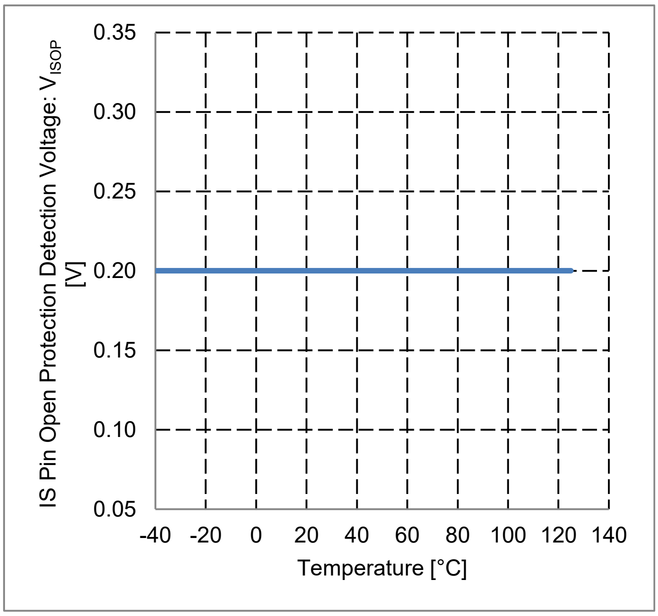


Figure 28. IS Pin Open Protection Detection Voltage vs Temperature

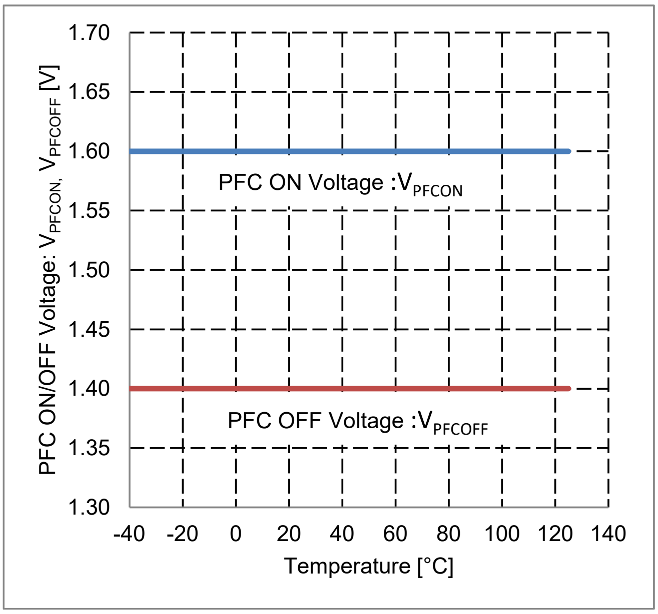


Figure 29. PFC ON/OFF Voltage vs Temperature

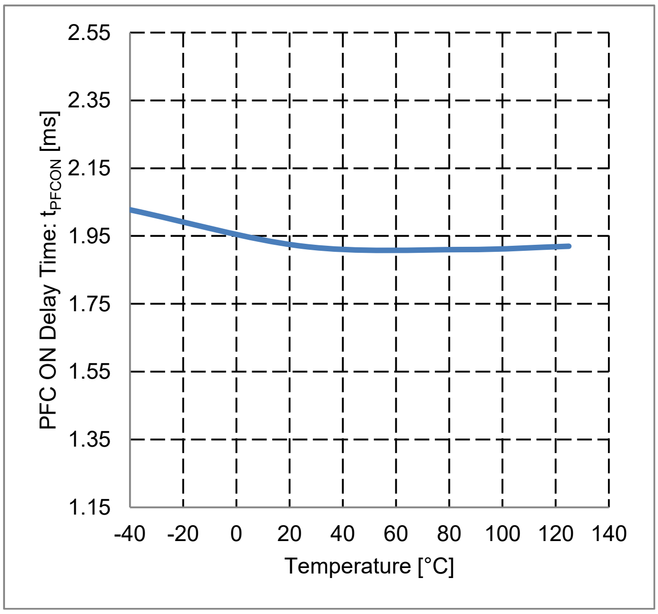


Figure 30. PFC ON Delay Time vs Temperature

Typical Performance Curves – continued
(Reference Data)

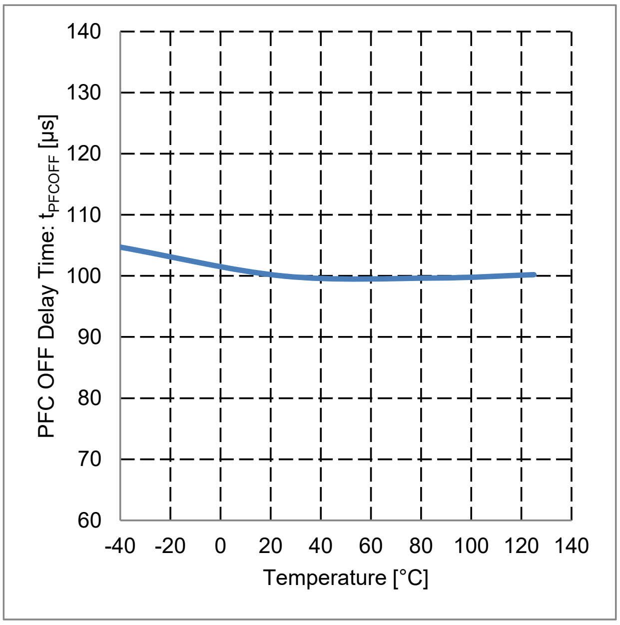


Figure 31. PFC OFF Delay Time vs Temperature

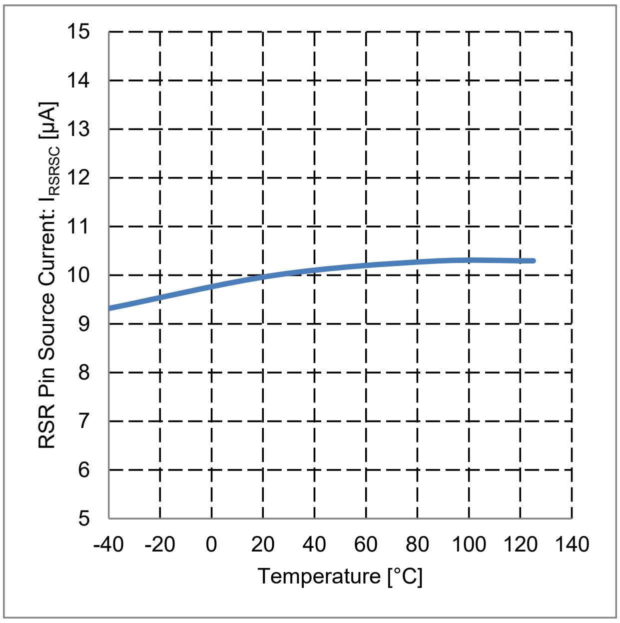


Figure 32. RSR Pin Source Current vs Temperature

Application Examples

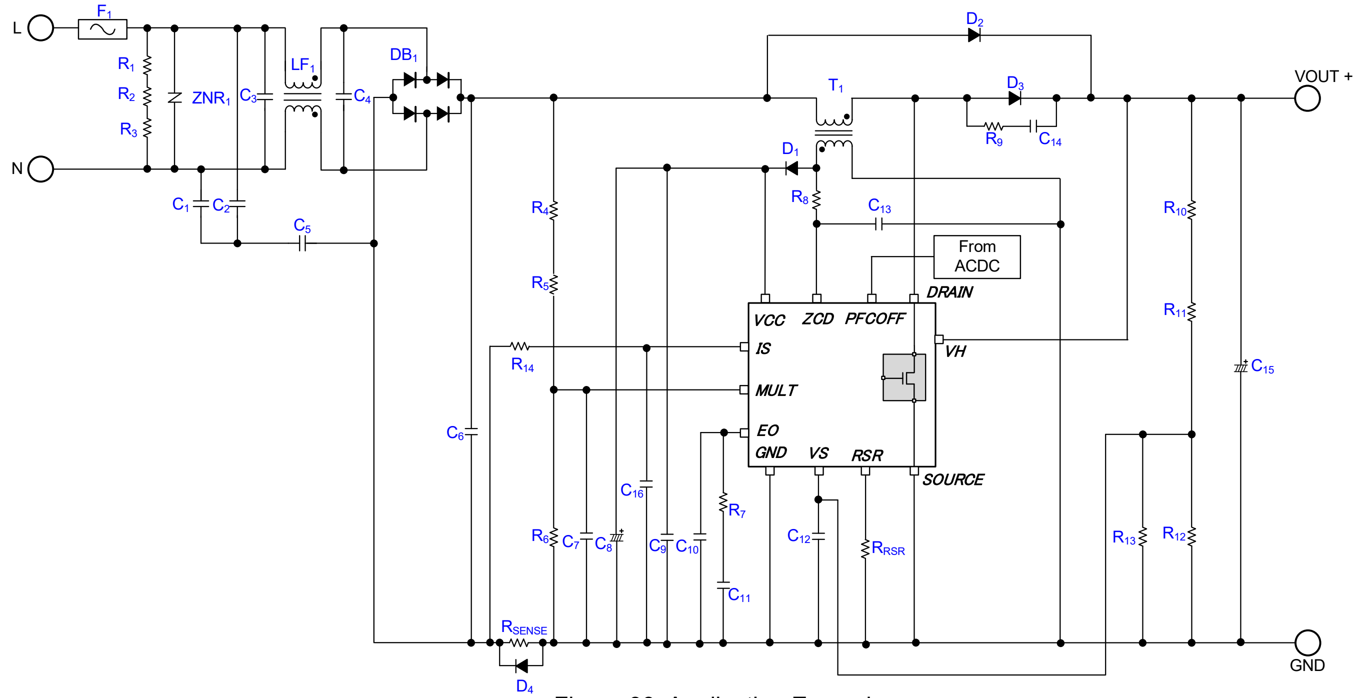


Figure 33. Application Example

1 Output Voltage Setting

The output voltage is determined by the feedback resistor connected to the VS pin.

$$V_{OUT} = \left(1 + \frac{(R_{10}+R_{11})}{(R_{12}//R_{13})}\right) \times V_{AMP1} = \left(1 + \frac{1582\ k\Omega}{10\ k\Omega}\right) \times 2.5\ V = 398 \qquad \text{[V]}$$

where:

$R_{10} + R_{11}$ is the upper resistance value of output feedback

$R_{12}//R_{13}$ is the lower combined resistance value of output feedback

V_{AMP1} is the Gm amplifier reference voltage 1

2 Calculation of Inductance

Reference when V_{OUT} = 400 V and power = 200 W

$$L = 250\ \mu H$$

If L is set to a larger value, THD will be lowered, but the part size will be larger.

3 External Setting of VCC Pin

The VCC pin voltage variation during switching can be reduced by installing a capacitor on the VCC pin.
We recommend using an electric-field capacitor that has a withstand voltage of 50 V or more and 10 µF or more for the VCC pin capacitor.
In addition, when generating the VCC pin voltage from the start resistor and the auxiliary winding of the transformer, check the VCC pin voltage evaluation when starting time and protection are detected on the actual device. When switching is stopped after starting, the current consumption of the IC decreases. Therefore, the VCC pin voltage may rise depending on the starting resistor. The VCC pin voltage discharge function prevents overvoltage breakdown of the VCC pin.
This function makes it possible to reduce the starting resistance value and make the starting time faster.

Board Design Notes

1　Parts Arrangement

The components in Figure 34 dashed lines should be located as close to the ICs as possible. Also, arrange components to avoid interfering with switching lines, inductors, DRAIN, and other high current lines.

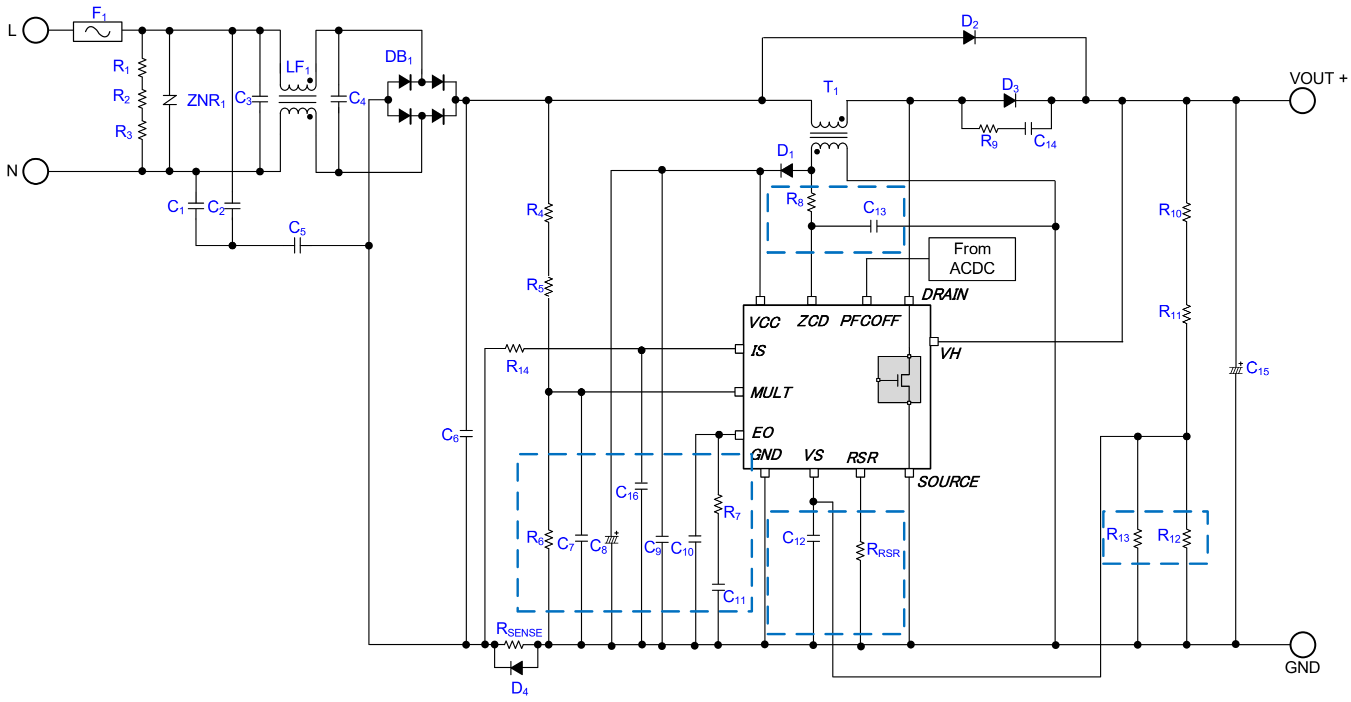


Figure 34. Parts Placement

2　GND Wiring Routing

The red wire of Figure 35 is a ground wire through which a large current flows. Wire each line independently and pull it thick and short. The blue line is the GND of the IC. Make the GND of IC and the GND of IC peripheral parts common.

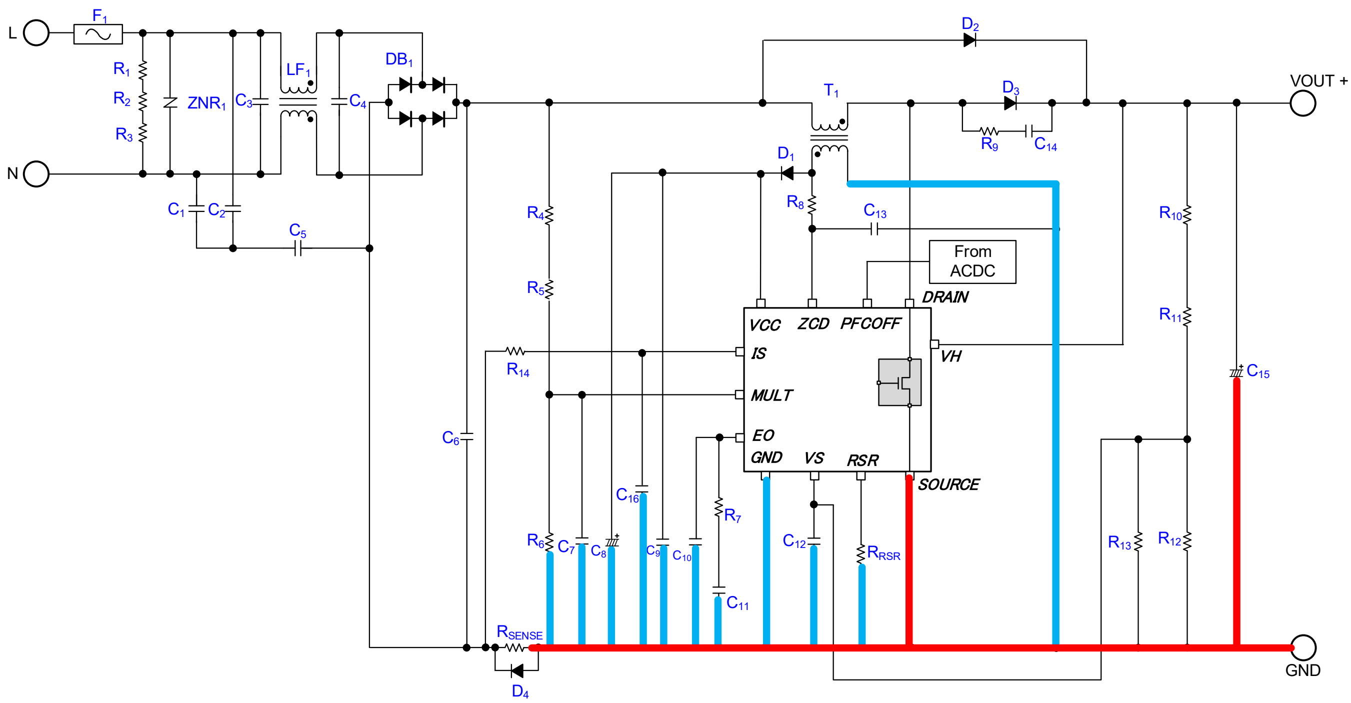


Figure 35. GND Line Layout

Board Design Notes – continued

3 High Current Line

The red line of Figure 36 carries a large amount of circuit current. Draw the red line part thick and short. Also, avoid routing lines with high IC or impedance nearby, as this may result in lines with high noise.

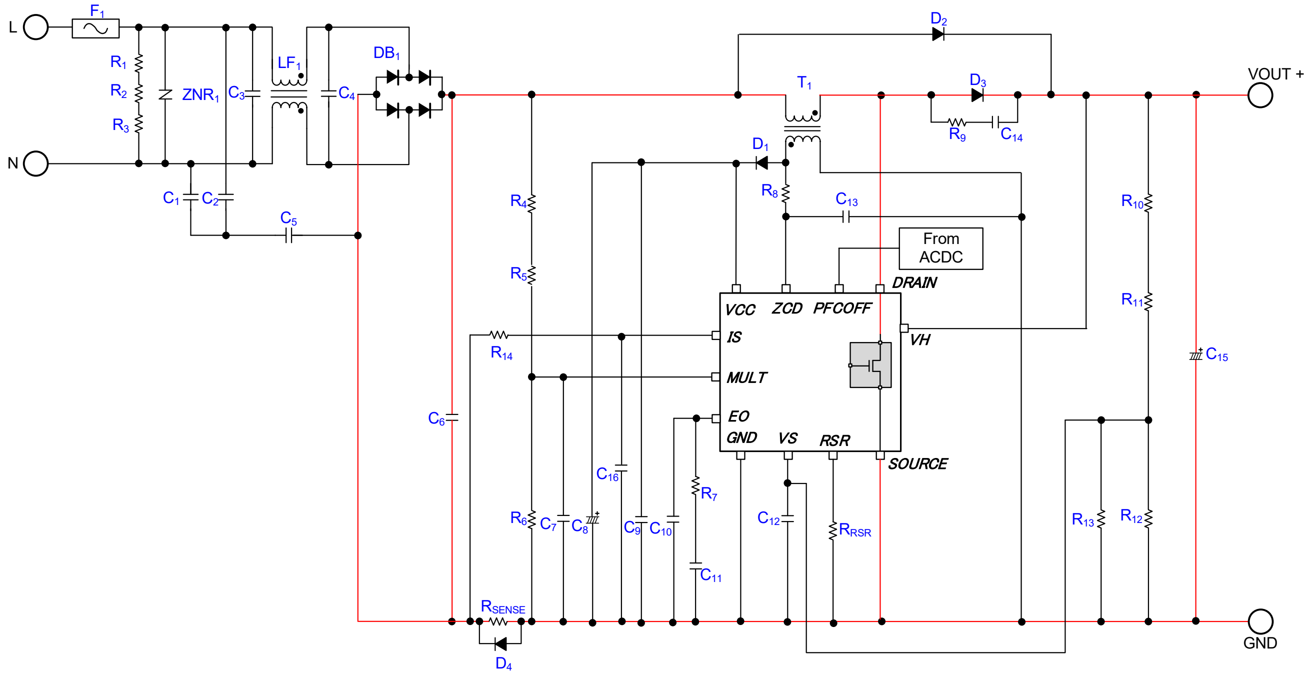
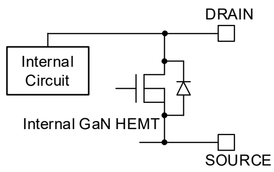
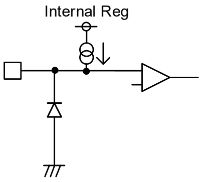
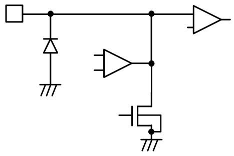
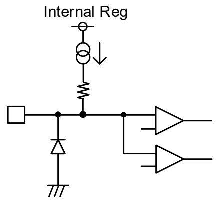
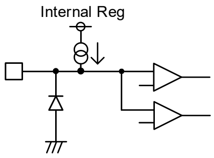
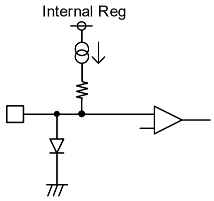
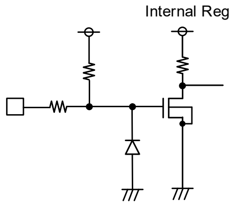
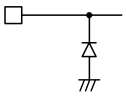
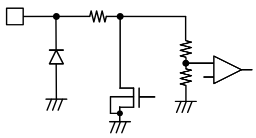
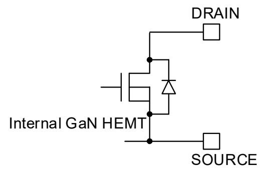
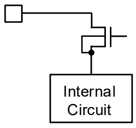


Figure 36. High Current Line Layout

I/O Equivalence Circuit

1,2,17-22,25-32	SOURCE	3	VS	4	EO	5	RSR
							
6	MULT	7,9,10,12,14,23,24	N.C.	8	IS	11	PFCOFF
		No Connection					
13	VCC	15	ZCD	16	GND	33-39	DRAIN
							
40,41	VH						
							

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

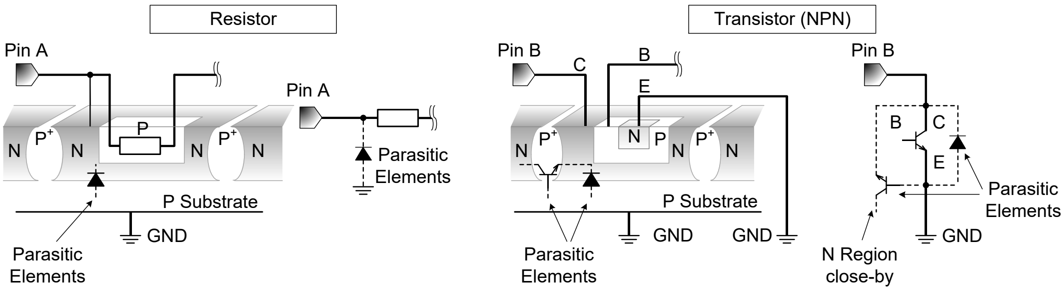


Figure 37. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B M 3 G F 0 x M U V - L B Z E 2

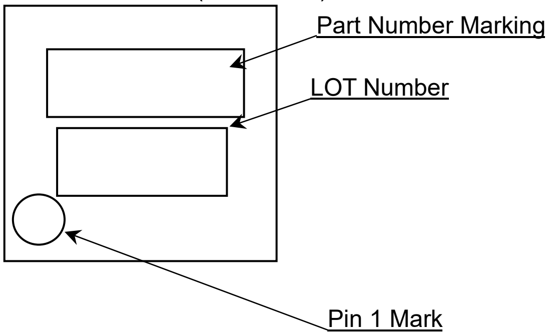
GaN HEMT D-S ON Resistor (Typ)
1: 150 mΩ
2: 70 mΩ

Package
MUV: VQFN41V8080K

Product Class
LB: for Industrial Applications
Packaging and Forming Specifications
Z: Outsourced Package
E2: Embossed Tape and Reel

Marking Diagram

VQFN41V8080K (TOP VIEW)

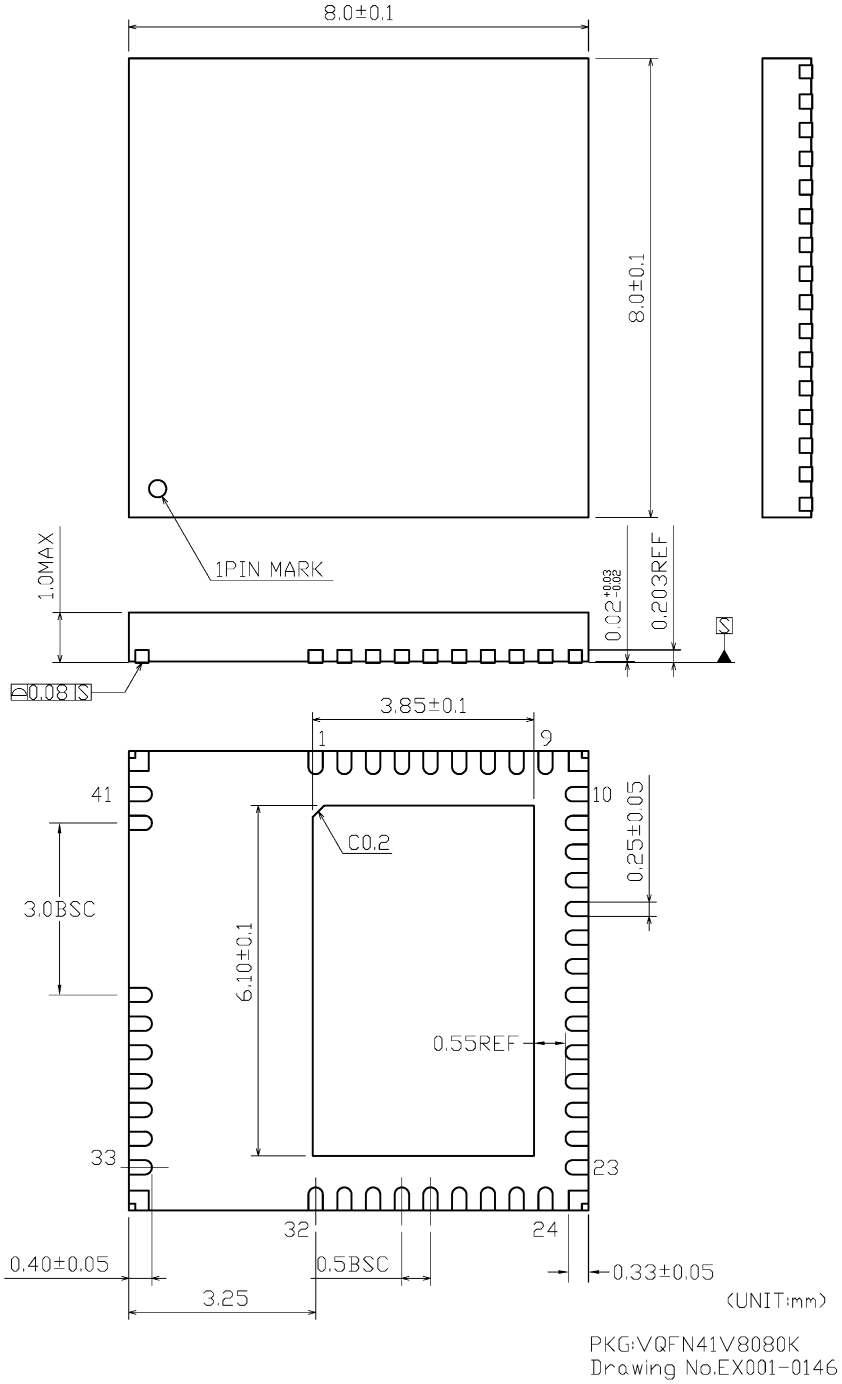


Lineup

Part Number Marking	Orderable Part Number	GaN HEMT D-S ON Resistor (Typ)
M3GF01MUV	BM3GF01MUV-LBZE2	150 mΩ
M3GF02MUV	BM3GF02MUV-LBZE2	70 mΩ

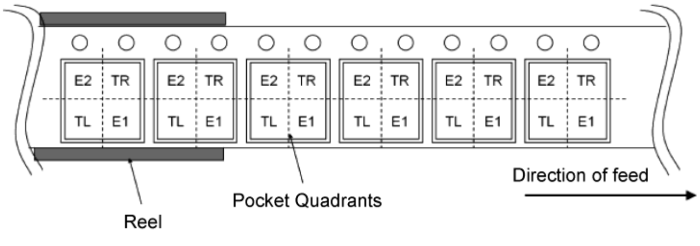
Physical Dimension and Packing Information

Package Name	VQFN41V8080K



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
21.Jan.2025	001	New release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
<tr><td>CLASSⅢ</td><td rowspan="2">CLASSⅢ</td><td>CLASSⅡb</td><td rowspan="2">CLASSⅢ</td></tr>
<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
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2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.
2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).
3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

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2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.
3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.
4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.