

AC / DC Controller IC

# CRM Totem Pole PFC Controller IC

## BM85060FV

### General Description

The BM85060FV is a critical conduction mode (CrM) power factor correction (PFC) controller IC designed to drive a bridgeless totem pole PFC topology. Bridgeless totem pole PFC consists of two totem pole legs: a fast-switching leg driven at high switching frequencies and a second leg operating at AC line frequency. This topology eliminates the need for a diode bridge, which is essential in conventional PFC circuits, and significantly improves efficiency and power density.

### Features

- Critical conduction Mode (CrM) and Discontinuous Conduction Mode (DCM) Operation
- Burst Mode Operation at Very Light Loads
- Brownout Detection
- X Capacitor Discharge Function
- High Voltage Startup
- Dynamic Response Enhancer
- Protections
  - Output Over Voltage Protection (Fast Over Voltage, Second Over Voltage)
  - Output Under Voltage Protection (UVP)
  - Input Over Voltage Protection (VAC OVP)
  - Overload and Peak Current Limit Protection (Peak Current Limit, Soft Over Current)
  - Inrush Current Limit
  - Open Loop Detection
  - Internal TSD
  - AC Voltage Sudden Change Detection
  - Negative Over Current Limiter

### Key Specifications

- Operating Power Supply Voltage Range  
VCC Pin Voltage: 8.0V to 36V (rated 40V)  
HV Pin Voltage: 650 V (Max)
- Frequency Range: 25kHz to 1MHz
- Operating Temperature Range: -40 °C to +125 °C

### Package

SSOP-B20

W (Typ) x D (Typ) x H (Max)  
6.5 mm x 6.4 mm x 1.45 mm



### Application

- Power Supplies for 5G / Telecom
- Power Supplies for Industrial Applications
- Power Supplies for Gaming consoles
- Ultra High Definition (UHD) Power Supplies
- Commercial Power Supplies

### Typical Application Circuit

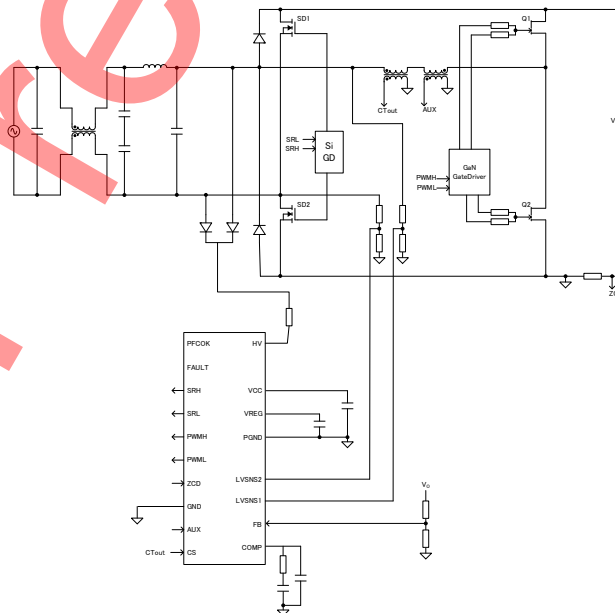


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Preliminary

Pin Configuration

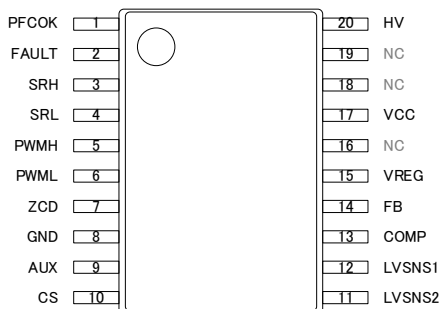


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	PFCOK	The pin is held low when the PFC output voltage is out of regulation or during fault conditions. The pin becomes active when the PFC output achieves regulation in nominal operation.
2	FAULT	Dedicated fault trigger pin.
3	SRH	Control signal for high side slow leg device.
4	SRL	Control signal for low side slow leg device.
5	PWMH	PWM logic level output for control of high side fast leg switch.
6	PWML	PWM logic level output for control of low side fast leg switch.
7	ZCD	The pin senses the inductor downslope current and short-circuit current of half-bridge.
8	GND	Ground connection
9	AUX	The pin is used to monitor the switch node resonance on the auxiliary winding and enable valley turn-on during CrM.
10	CS	Connected to current sensing transformer. Current limit is based on the signal on this pin.
11	LVSNS2	Low voltage input for AC line voltage monitoring. LVSNS2 resistor divider should be connected to the neutral of the AC line voltage.
12	LVSNS1	Low voltage input for AC line voltage monitoring. LVSNS1 resistor divider should be connected to AC line side of the boost inductor.
13	COMP	Connection pin to the loop compensation network.
14	FB	This pin senses the PFC output voltage for loop regulation.
15	VREG	Internal regulator output. Capacitor must be connected.
16	NC	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
17	VCC	Bias supply input
18	NC	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
19	NC	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
20	HV	High voltage startup and X capacitor discharge function.

Block Diagram

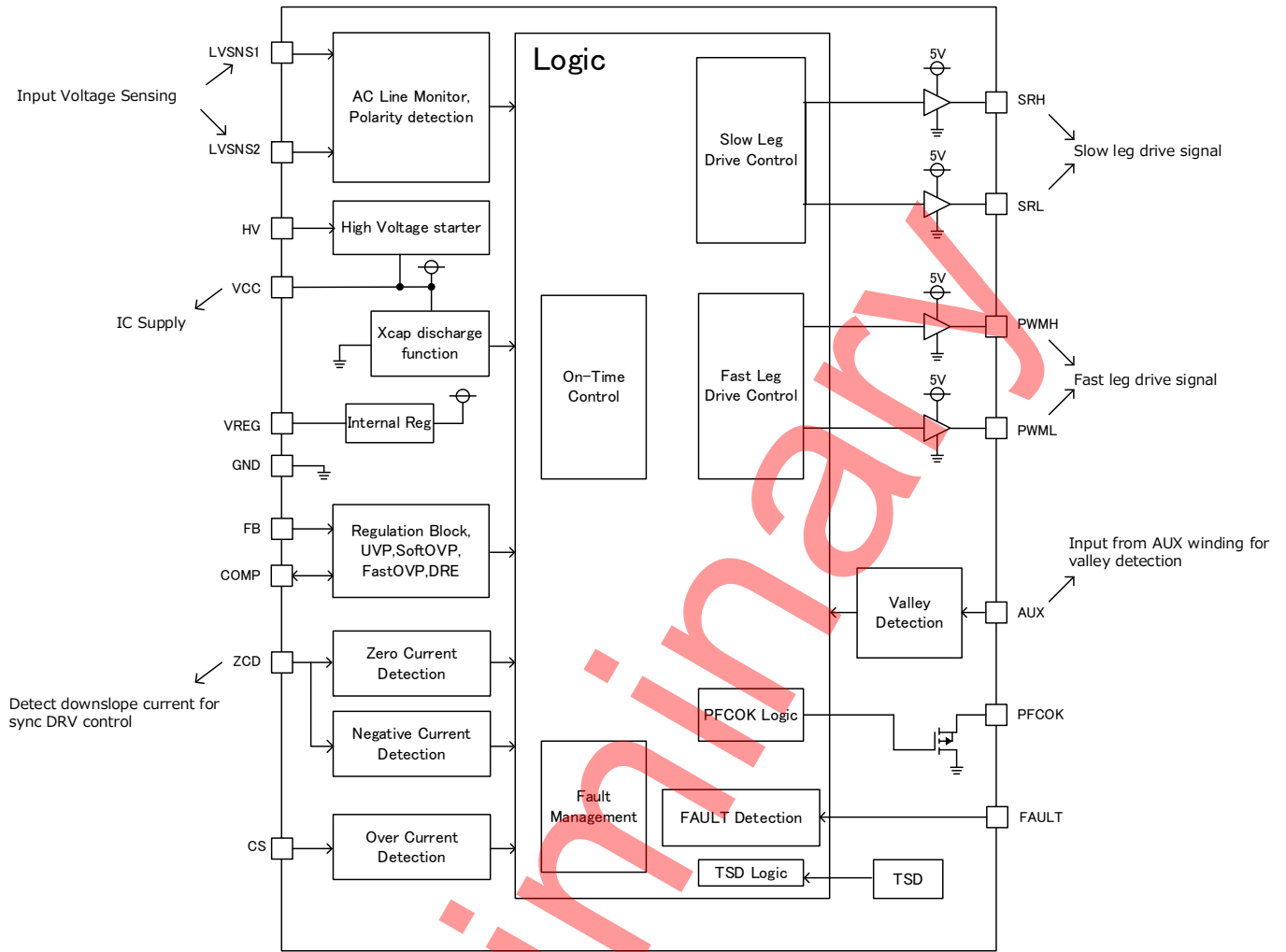


Figure 3. Block Diagram

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
High Voltage Start-Up Circuit Input Voltage range, HV Pin	V <sub>HV(MAX)</sub>	-0.3 to +650	V
Supply Input Voltage range, VCC Pin	V <sub>VCC</sub>	-0.3 to +40	V
Internal Regulator Voltage range, VREG Pin	V <sub>VREG</sub>	-0.3 to +7.0	V
Current sensing Voltage range, CS Pin ZCD Pin	V <sub>(MAX)</sub>	-0.6 to +7.0	V
Pins - LVSNS1, LVSNS2, FB, COMP, FAULT, PFCOK, SRH, SRL, AUX, PWMH, PWML Voltage	V <sub>LVSNS1</sub> , V <sub>LVSNS2</sub> , V <sub>FB</sub> , V <sub>COMP</sub> , V <sub>FAULT</sub> , V <sub>PFCOK</sub> , V <sub>SKIP</sub> , V <sub>ZCD</sub> , V <sub>SRH</sub> , V <sub>SRL</sub> , V <sub>AUX</sub> , V <sub>PWMH</sub> , V <sub>PWML</sub>	-0.3 to +7.0	V
Junction Temperature	T <sub>jmax</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

**Thermal Resistance**

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
<b>SSOP-B20</b>				
Junction to Ambient	θ <sub>JA</sub>	115.4	57.3	°C / W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	Ψ <sub>JT</sub>	10	8	°C / W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7..

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note5)</sup>	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mm	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connect with the copper pattern of layers 1, 2, and 4. The placement and dimensions obey a land pattern.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for HV	V <sub>HV</sub>	80	-	600	V
Supply Voltage for VCC	V <sub>VCC</sub>	8	-	36	V
Operating Temperature	T <sub>OPR</sub>	-40	+25	+125	°C
VCC Capacitor	C <sub>VCC</sub>	-	-	70	µF
VREG output Capacitor <sup>(Note7)</sup>	C <sub>VREG</sub>	1	2.2	-	µF
Total X Capacitance	C <sub>XCAP</sub>	-	-	4.7	µF

(Note 6) This parameter is for 10 A output. Not 100 % tested.

(Note 7) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered.

Electrical Characteristics (Unless otherwise specified  $V_{HV} = 320\text{ V}$ ,  $V_{CC} = 12\text{ V}$ ,  $T_j = -40\text{ to }+125\text{ }^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>SUPPLY CIRCUITS</b>						
VCC UVLO Release Voltage	$V_{UVLO1}$	9.75	10.5	11.25	V	$V_{CC}$ rising
VCC UVLO Detection Voltage	$V_{UVLO2}$	5.9	6.5	7.1	V	$V_{CC}$ falling
VCC Hysteresis	$V_{CC(HYS)}$		4	-	V	$V_{UVLO1} - V_{UVLO2}$
Quiescent Current (Before Startup)	$I_{CC1}$	-	330	680	$\mu\text{A}$	$V_{CC} = 9.5\text{V}$
Quiescent Current (CrM operation)	$I_{CC2}$	-	2.2	4.4	mA	Non switching
Quiescent Current (Burst mode)	$I_{CC3}$	-	180	380	$\mu\text{A}$	Burst mode
<b>VREG</b>						
VREG Voltage	$V_{REG1}$	4.8	5.0	5.2	V	
VREG UVLO Release Voltage	$V_{REG\_UVLO1}$	3.96	4.4	4.84	V	$V_{REG}$ rising
VREG UVLO Detection Voltage	$V_{REG\_UVLO2}$	2.79	3.1	3.41	V	$V_{REG}$ falling
<b>High Voltage Startup &amp; X capacitor discharger</b>						
HV Minimum Operation Voltage	$V_{HV-START(ON)}$	30	-	-	V	
VCC Recharge Start Voltage	$V_{CHG1}$	8.5	9.5	10.5	V	$V_{CC}$ falling
VCC Recharge Stop Voltage	$V_{CHG2}$	9.0	10.0	11.0	V	$V_{CC}$ rising
Start Current 1	$I_{START1}$	0.24	0.6	1.8	mA	$V_{CC}=0\text{V}$
Start Current 2	$I_{START2}$	3	6.5	12	mA	$V_{CC}=10\text{V}$
OFF Current	$I_{START-OFF}$	-	8	16	$\mu\text{A}$	HV current after $V_{CC}$ UVLO released
Start Current Charging Voltage	$V_{SC}$	0.8	1.5	2.1	V	$V_{CC}$ voltage
VCC Charging Timer	$t_{vcc\_charge\_max}$	240	300	360	ms	
VCC Charging Restart Timer	$t_{vcc\_charge\_restart}$	360	450	540	ms	
<b>AC ZERO CROSSING MANAGEMENT</b>						
PWM Zero Crossing Blanking Thresholds Detection						$V_{ZCBx} =  V_{LVSNs1} - V_{LVSNs2} $
Threshold to start PWML / H Pulses	$V_{ZCB\_START(HLine)}$	120	200	280	mV	at High-Line
	$V_{ZCB\_START(LLine)}$	120	200	280	mV	at Low-Line
Slow Leg Zero Crossing Blanking Thresholds Detection						$V_{SRx} =  V_{LVSNs1} - V_{LVSNs2} $
Threshold to stop SRL / H Pulses	$V_{SR\_STOP(HLine)}$	240	320	400	mV	at High-Line
	$V_{SR\_STOP(LLine)}$	240	320	400	mV	at Low-Line
Threshold to start SRL / H Pulses	$V_{SR\_START(HLine)}$	300	380	460	mV	at High-Line
	$V_{SR\_START(LLine)}$	300	380	460	mV	at Low-Line
SYNC(1-d) Zero Crossing Blanking Threshold Detection						$V_{SYNC} =  V_{LVSNs1} - V_{LVSNs2} $
Threshold to stop Sync Pulses	$V_{SYNC\_STOP(HLine)}$	300	380	460	mV	at High-Line
	$V_{SYNC\_STOP(LLine)}$	300	380	460	mV	at Low-Line
Threshold to start Sync Pulses	$V_{SYNC\_START(HLine)}$	360	440	520	mV	at High-Line
	$V_{SYNC\_START(LLine)}$	360	440	520	mV	at Low-Line
Zero Crossing Softstart Time	$t_{AC\_SOFTSTART}$	154	192	230	$\mu\text{s}$	
Zero Crossing Softstop Time	$t_{AC\_SOFTSTOP}$	154	192	230	$\mu\text{s}$	
Polarity Detection Filter	$t_{POL\_FILTER}$	102	128	154	$\mu\text{s}$	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>ZCD pin Detection</b>						
ZCD Arming Threshold (Synchronous Drive Threshold)	$V_{ZCD\_HLine(ARM)}$	70	100	130	mV	at High-Line
	$V_{ZCD\_LLine(ARM)}$	70	100	130	mV	at Low-Line
ZCD Trigger Threshold	$V_{ZCD\_HLine(TRIG)}$	25	50	75	mV	at High-Line
	$V_{ZCD\_LLine(TRIG)}$	25	50	75	mV	at Low-Line
Current Limit Detection	$V_{ZCDLIM\_HLine}$	700	800	900	mV	at High-Line
	$V_{ZCDLIM\_LLine}$	1500	1600	1700	mV	at Low-Line
Threshold for Inrush Current Protection	$V_{INRUSH}$	20	50	80	mV	
Negative Over Current Limiter (NOCL) Threshold	$V_{NOCL}$	-845	-768	-691	mV	
<b>BROWN-OUT, LINE SAG, LINE FAULT AND LINE RANGE DETECTION</b>						
Line Sag and Brown-Out Detection Upper Threshold	$V_{BO(START)}$	0.96	1.04	1.12	V	$ V_{LVSNS1} - V_{LVSNS2} $ rising
Line Sag and Brown-Out Detection Lower Threshold	$V_{BO(STOP)}$	0.86	0.94	1.02	V	$ V_{LVSNS1} - V_{LVSNS2} $ falling
Brown-Out Detection Hysteresis	$V_{BO(HYS)}$	60	100	-	mV	$ V_{LVSNS1} - V_{LVSNS2} $ rising
Line Sag Detection Blanking Timer	$t_{SAG(blank)}$	20	25	30	ms	$ V_{LVSNS1} - V_{LVSNS2}  < V_{BO(STOP)}$ , Delay to Soft Stop Enable
Brown-Out Detection Blanking Timer	$t_{BO(blank)}$	520	650	780	ms	$ V_{LVSNS1} - V_{LVSNS2} $ falling, Delay to Polarity Disable
High-Line Level Detection Threshold	$V_{HLine}$	2.20	2.36	2.52	V	$ V_{LVSNS1} - V_{LVSNS2} $ rising 200Vac range
Low-Line Level Detection Threshold	$V_{LLine}$	2.07	2.22	2.37	V	$ V_{LVSNS1} - V_{LVSNS2} $ falling 100Vac range
Low to High Line Mode Selector Timer Filter	$t_{blank(HLine)}$	200	300	400	$\mu$ s	$ V_{LVSNS1} - V_{LVSNS2}  > V_{HLine}$
High to Low Line Mode Selector Timer Filter	$t_{blank(LLine)}$	20	25	30	ms	$ V_{LVSNS1} - V_{LVSNS2}  < V_{LLine}$
<b>AC LINE FREQUENCY MONITORING</b>						
Line Frequency Upper Threshold	$f_{LINE(HI)}$	64	72	80	Hz	
Line Frequency Lower Threshold	$f_{LINE(LO)}$	36	41	46	Hz	
<b>VALLEY DETECTION CIRCUIT</b>						
Valley Detection Thresholds in Positive Half Line Cycle	$V_{VD1\_TH(rising)}$	150	200	250	mV	$V_{LVSNS1} = 1.2$ V, $V_{LVSNS2} = 0$ V, $V_{AUX}$ rising (Arm) $V_{AUX}$ falling (Trigger)
	$V_{VD1\_TH(falling)}$	50	100	150		
Valley Detection Hysteresis in Positive Half Line Cycle	$V_{VD1\_HYS}$	50	100	-	mV	
Valley Detection Thresholds in Negative Half Line Cycle	$V_{VD2\_TH(rising)}$	50	100	150	mV	$V_{LVSNS1} = 0$ V, $V_{LVSNS2} = 1.2$ V, $V_{AUX}$ falling (Arm) $V_{AUX}$ rising (Trigger)
	$V_{VD2\_TH(falling)}$	150	200	250		
Valley Detection Hysteresis in Negative Half Line Cycle	$V_{VD2\_HYS}$	50	100	-	mV	

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>DCM mode control and Burst mode control</b>						
DCM Mode Threshold 1	$V_{DCM\_TH1\_LLine}$	540	600	660	mV	$V_{COMP}$ rising at Low-Line at High-Line
	$V_{DCM\_TH1\_HLine}$	540	600	660		
DCM Mode Threshold 2	$V_{DCM\_TH2\_LLine}$	500	550	600	mV	$V_{COMP}$ falling at Low-Line at High-Line
	$V_{DCM\_TH2\_HLine}$	400	450	500		
Burst Mode Threshold	$V_{CLAMP\_TH\_LLine}$	160	180	200	mV	$V_{COMP}$ falling at Low-Line at High-Line
	$V_{CLAMP\_TH\_HLine}$	160	180	200		
Burst Threshold Ratio ( $V_{BURST\_TH} / V_{REF}$ )	$R_{BURST}$	92	95	98	%	$V_{FB}$ falling
<b>FAST LEG DRIVE SIGNALS (PWML &amp; PWMH)</b>						
Source Resistance	$R_{ON\_OH}$	-	15	32	$\Omega$	
Sink Resistance	$R_{ON\_OL}$	-	5	12	$\Omega$	
<b>SLOW LEG DRIVE SIGNALS (SRL &amp; SRH)</b>						
Source Resistance	$R_{ON\_OH2}$	-	15	32	$\Omega$	
Sink Resistance	$R_{ON\_OL2}$	-	5	12	$\Omega$	
<b>ON TIME MODULATION CIRCUIT</b>						
Maximum Frequency Clamp	$F_{CLAMP}$	800	1000	1200	kHz	
Minimum Frequency Clamp	$F_{MIN}$	21	25	29	kHz	
<b>REGULATION BLOCK</b>						
Feedback Voltage Reference	$V_{REF}$	2.45	2.50	2.55	V	
Error Amplifier Sink Current	$I_{COMP\_SINK}$	1.2	2.2	3.2	$\mu A$	
Error Amplifier Source Current	$I_{COMP\_SOURCE}$	-3.2	-2.2	-1.2	$\mu A$	
FB Input Bias Current	$I_{FB}$	-0.5	0	0.5	$\mu A$	
<b>UNDERVOLTAGE &amp; OVERVOLTAGE PROTECTION</b>						
Ratio (Soft OVP Threshold over $V_{REF}$ ) ( $V_{softOVP} / V_{REF}$ )	$R_{softOVP}$	103	105	108	%	$V_{FB}$ rising
Ratio (Fast OVP Threshold over $V_{REF}$ ) ( $V_{fastOVP} / V_{REF}$ )	$R_{fastOVP}$	105	108	111	%	$V_{FB}$ rising
Ratio (OVP recovery threshold over $V_{REF}$ ) ( $V_{OVPrecover} / V_{REF}$ )	$R_{OVPrecover}$	100	103	106	%	$V_{FB}$ falling
Ratio (Static OVP Threshold over $V_{REF}$ ) ( $V_{staticOVP} / V_{REF}$ )	$R_{staticOVP}$	118	120	122	%	$V_{FB}$ rising
Undervoltage Protection Ratio ( $V_{UVP} / V_{REF}$ )	$R_{UVP}$	10	12	14	%	$V_{FB}$ falling
BUV Threshold Ratio ( $V_{BUV} / V_{REF}$ )	$R_{BUV}$	77	80	83	%	$V_{FB}$ falling
<b>PFCOK</b>						
PFCOK Threshold Ratio ( $V_{PFCOK} / V_{REF}$ )	$R_{PFCOK}$	96.5	98	99.5	%	$V_{FB}$ rising
PFCOK ON Resistance	$R_{ON\_PFCOK}$	11	22	35	$\Omega$	
PFCOK Leak Current	$I_{LEAK\_PFCOK}$	-0.5	0	0.5	$\mu A$	
<b>FAULT PROTECTION</b>						
FAULT Threshold 1	$V_{TH\_FLT1}$	800	900	1000	mV	$V_{FAULT}$ rising
FAULT Threshold 2	$V_{TH\_FLT2}$	350	400	450	mV	$V_{FAULT}$ falling
Detection Filter Delay	$t_{FLT\_DLY}$	22.5	30	37.5	$\mu s$	$V_{FAULT}$ falling
FAULT Source Current	$I_{FLT}$	90	100	110	$\mu A$	



Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>Current Limit Protection - CS pin Detection</b>						
Current Limit Detection at High-Line Detection (Cycle by cycle protection)	$V_{CS1\_LIM\_Pos(HLine)}$ $V_{CS1\_LIM\_Neg(HLine)}$	32 -96	64 -64	96 -32	mV	in Positive Half Line Cycle in Negative Half Line Cycle
Current Limit Detection at Low-Line Detection (Cycle by cycle protection)	$V_{CS1\_LIM\_Pos(LLine)}$ $V_{CS1\_LIM\_Neg(LLine)}$	104 -184	144 -144	184 -104	mV	in Positive Half Line Cycle in Negative Half Line Cycle
Current Limit Detection at High-Line Fault Detection (Latch protection)	$V_{CS2\_LIM\_Pos(HLine)}$ $V_{CS2\_LIM\_Neg(HLine)}$	88 -168	128 -128	168 -88	mV	in Positive Half Line Cycle in Negative Half Line Cycle
Current Limit Detection at Low-Line Fault Detection (Latch protection)	$V_{CS2\_LIM\_Pos(LLine)}$ $V_{CS2\_LIM\_Neg(LLine)}$	238 -338	288 -288	338 -238	mV	in Positive Half Line Cycle in Negative Half Line Cycle
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Threshold	$T_{SD}$	-	140	-	°C	Temperature rising
Thermal Shutdown Hysteresis	$T_{SD(HYS)}$	-	25	-	°C	Temperature falling
<b>Dynamic response enhancer (DRE)</b>						
DRE Detection Threshold Ratio ( $V_{DRE\_LO} / V_{REF}$ )	$R_{DRE\_LO}$	94.5	95	96.5	%	$V_{FB}$ falling
DRE Recovery Threshold Ratio ( $V_{DRE\_HI} / V_{REF}$ )	$R_{DRE\_HI}$	96.5	98	99.5	%	$V_{FB}$ rising

Function Explanation

1. Basic Operation of Totem Pole PFC

The Totem Pole PFC (TPPFC) circuit consists of two half-bridges. “Fast Leg” switches at the PWM frequency. “Slow Leg” switches at the AC line frequency. The fast leg switches perform the role of the switch and the diode in a classical boost PFC, that is these switches function to regulate the output voltage and shape the input current to provide high power factor and low harmonic distortion. The slow leg switches perform the role of the diode bridge in a classical boost PFC. Active switch with low ON resistance are utilized instead of diodes resulting in improved efficiency.

The TPPFC operates with bidirectional current flow in the inductor, and the command of the fast and slow leg switches change depending on the polarity of the AC line cycle. Operation of the TPPFC during the positive and negative half line cycles is shown in Figure 4. Cycle operation.

positive AC line cycle:

During the positive AC line cycle the PWML signal is responsible for performing pulse width modulation or duty cycle control of the converter.

PWML toggles high turning on the low side fast leg device, allowing current to charge and store energy in the inductor, as shown (1) in Figure 4. Cycle operation.

When the PWML signal toggles low the inductor current diverts through the high side fast leg switch, transferring energy from the inductor to the load, as shown (2) in Figure 4. Cycle operation.

In this half line cycle the high side fast leg device does not need to conduct for proper PFC operation, however the PWMH signal can toggle high turn on the high side device, providing enhanced system efficiency at medium to high load levels. Throughout the positive half line cycle current is flowing left to right through the inductor and always returning to the source through the low side slow leg device, hence the SRL signal can toggle high to turn on the low side slow leg device for optimum converter efficiency.

negative AC line cycle:

During a negative AC line cycle, the following points change from a positive AC line cycle. The roles of PWMH and PWML are interchanged. The roles of SRH and SRL are interchanged. The direction of the inductor current is reversed.

In summary:

Positive Half Cycle Operation

- output PWM(d) signal to PWML pin
- output SYNC(1-d) signal to PWMH pin I at medium to high load level
- output high to SRL pin
- output low to SRH pin

Negative Half Cycle Operation

- output SYNC(1-d) signal to PWML pin at medium to high load level
- output PWM(d) signal to PWMH pin
- output low to SRL pin
- output high to SRH pin

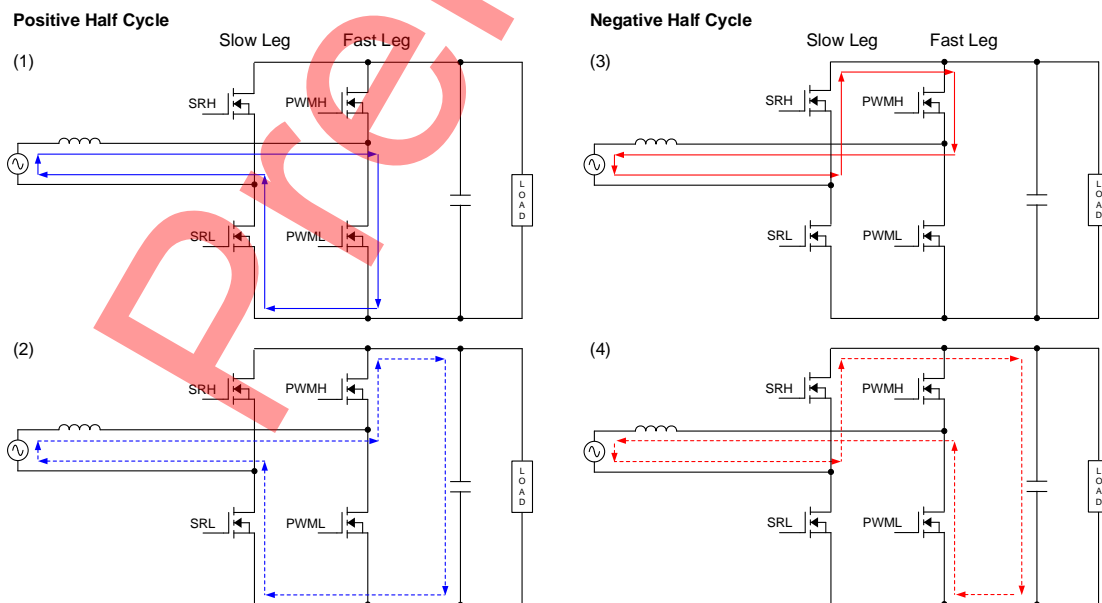


Figure 4. Cycle operation

2. High Voltage Startup, X capacitor discharge function

Figure 5 shows the IC has built-in starter circuit which withstand voltage is 650V. Two diode rectifiers and current limiting resistor must be placed between AC-lines and HV pin to use this function.

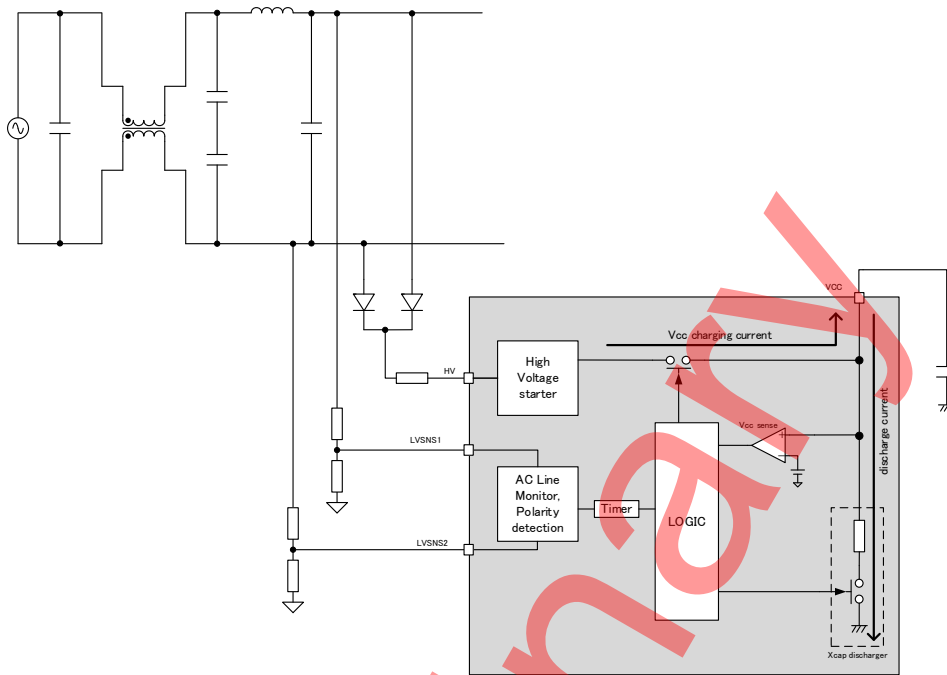


Figure 5. Configuration of HV startup circuit

When HV pin voltage is higher than  $V_{HV-START(ON)}$ , starter circuit is enabled and initial current flow to VCC pin (Point: A). VCC charging current will increase to higher level when VCC pin voltage ( $V_{CC}$ ) reaches  $V_{SC}$  (Point: B). IC stops charging when  $V_{CC}$  reaches  $V_{UVLO1}$  (Point: C).

If the VCC pin voltage drops to  $V_{CC} < V_{CHG1}$  after starting with  $V_{CC} > V_{UVLO1}$ , the VCC charging function starts again (Point: D). After charging the VCC pin again, charging is terminated when the VCC pin rises to  $V_{CHG2}$  (Point: E). If external power supply applies to VCC pin, HV pin stops charging. These operations are shown in Figure 6. VCC startup charging operation. A protection circuit is built in to prevent overheating of the startup circuit. If the external circuit becomes short-circuited, the startup circuit will continue to operate for an extended period of time, causing the startup circuit to overheat. If  $t_{vcc\_charge\_max}$  elapses after the startup circuit starts operating, this circuit automatically stops.  $t_{vcc\_charge\_restart}$  is restarted when  $t_{vcc\_charge\_restart}$  is exceeded.

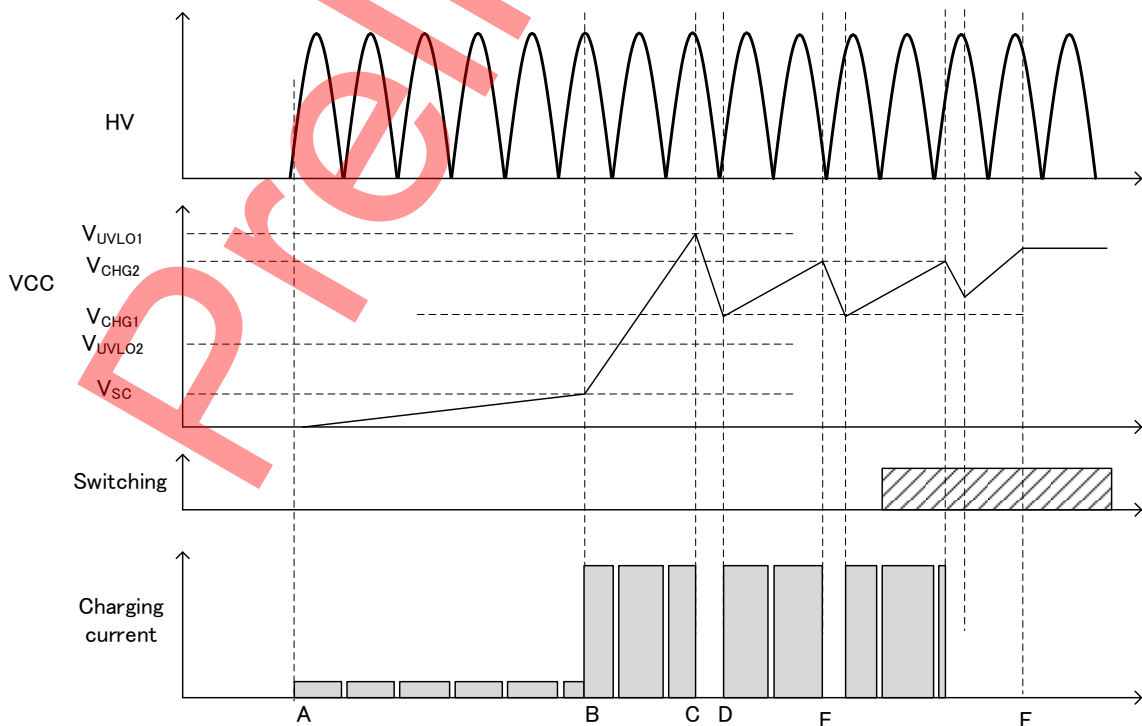


Figure 6. VCC startup charging operation

Figure 7 shows when IC detect the disconnection of AC input, X capacitor discharge function starts operation. This function is achieved by repeatedly charging from HV-pin to VCC-pin and discharging from VCC pin.

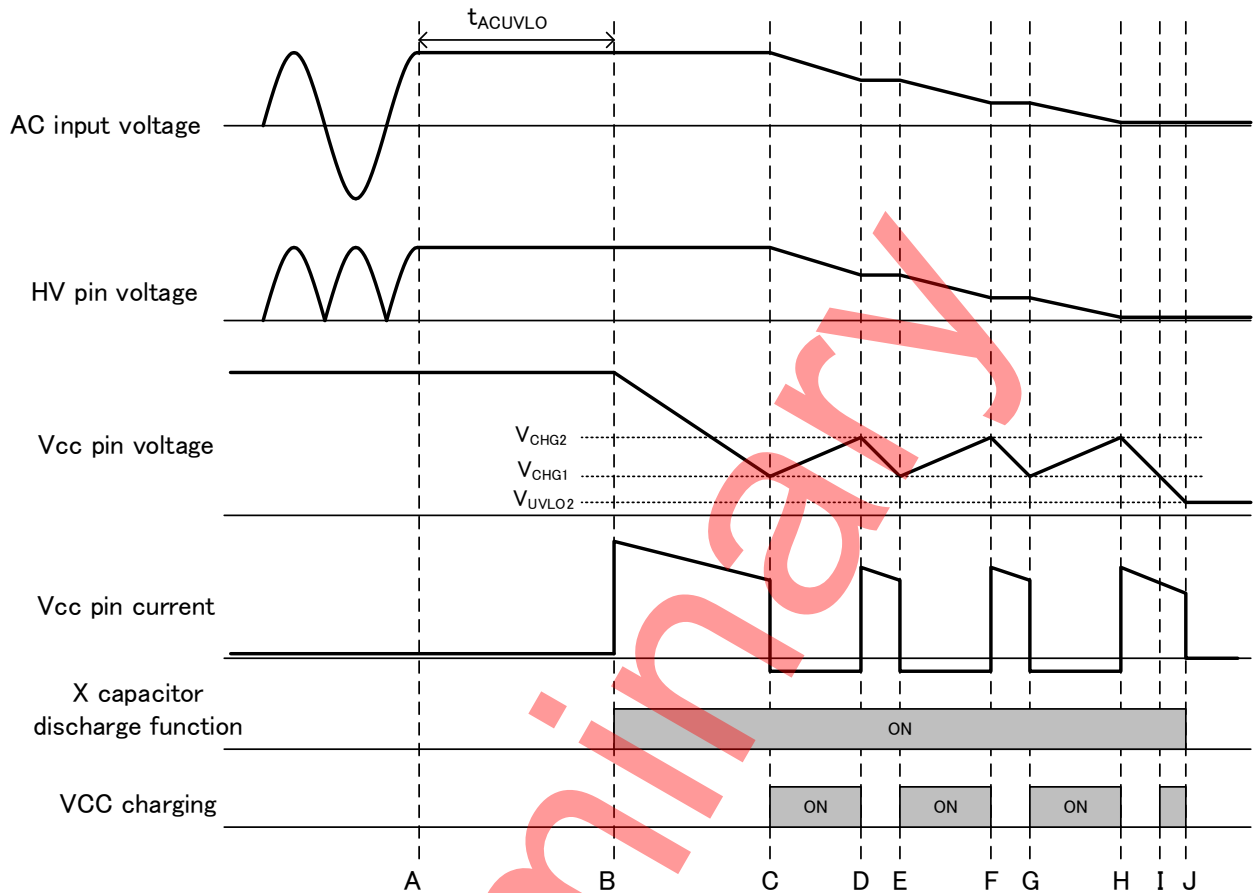


Figure 7. Timing Chart of X Capacitor Discharge Function.

- A: The AC input voltage is turned OFF.
- B: After  $t_{ACUVLO}$  (128 ms) from A, X capacitor discharge function is enabled. VCC capacitor is discharged until VCC voltage reaches  $V_{CHG1}$ .
- C: When the VCC pin voltage becomes less than  $V_{CHG1}$ , the VCC recharge operation starts and discharging starts from HV pin.
- D: When the VCC pin voltage becomes more than  $V_{CHG2}$ , the VCC recharge operation stops and VCC capacitor is discharged.
- E: The Same as C.
- F: The Same as D.
- G: The Same as C.
- H: The Same as D.
- I: When the VCC pin voltage becomes less than  $V_{CHG1}$ , the VCC recharge function operates. However, the current supply to the VCC pin decreases and the VCC pin voltage continues to drop because of the low HV pin voltage.
- J: When the VCC pin voltage becomes less than  $V_{UVLO2}$ , IC stops operation.

### 3. Startup Sequence

Figure 8 shows when AC voltage ( $V_{AC}$ ) is applied to circuit, High voltage startup circuit is activated and  $V_{CC}$  begins to rise. Switching operation is initiated when the following four conditions are met.

- Brown-out protection is cleared..
- $V_{CC}$  reaches  $V_{UVLO1}$  even once.
- Detects 4 consecutive polarity edges that are within the expected ac line frequency range.
- Polarity rising edge

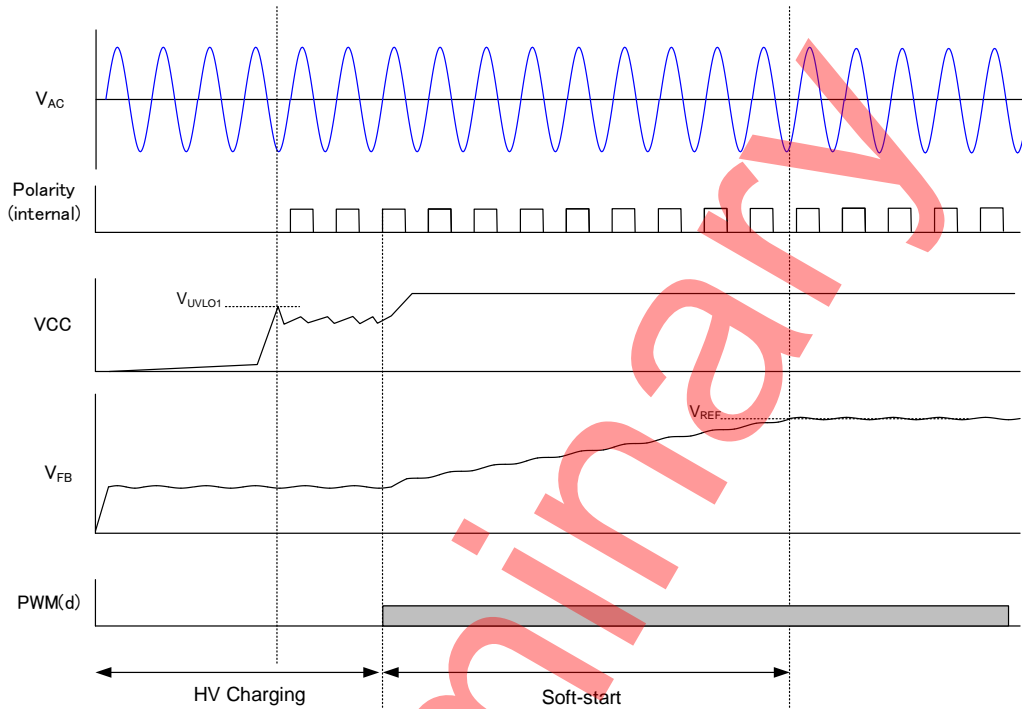


Figure 8. Startup Sequence

Soft-start sequence starts after switching started. Internal  $V_{REF}$  signal gradually increases from 0V. This allows a gradual increase in  $V_{FB}$  voltage and suppresses inrush current on the input side. Soft-start period is 80ms typ.

### 4. PWM generation

Figure 9 shows the IC operates with a constant on-time control algorithm. Figure 9. Structure of PWM generation circuit shows structure of PWM generation circuit.

The on time of the main PWM switch is determined by the compensation voltage, a ramp voltage and integrated functions. FB pin monitors a divided voltage of the output voltage. This voltage and  $V_{REF}$  voltage are connected to gmAMP. GmAMP controls base signal of PWM on time. The gain and phase characteristics of the gmAMP can be adjusted using the RC circuit network on the terminal (COMP) and the internal gain switching function (DRE and Vin-Range control function). Output of gmAMP is controlled by Digital Limiter. This function is used to realize AC zero cross control and soft-OVP. The PWM reset timing (PWM\_RST) is determined by comparing the two signals  $V_{RAMP}$  and Digital Limiter out.  $V_{RAMP}$  is a sawtooth wave for outputting PWM. The waveform can be adjusted by Frequency control function and ZCD over-current control. When COMP voltage rises, width of PWM\_RST signal becomes shorter. This means increase of On-time of PWM.

The PWM reset signal is input to the PWM generator. In PWM generator, there are several functions for default PWM operation, zero current detection and circuit protection. Minimum on-time is 100ns.

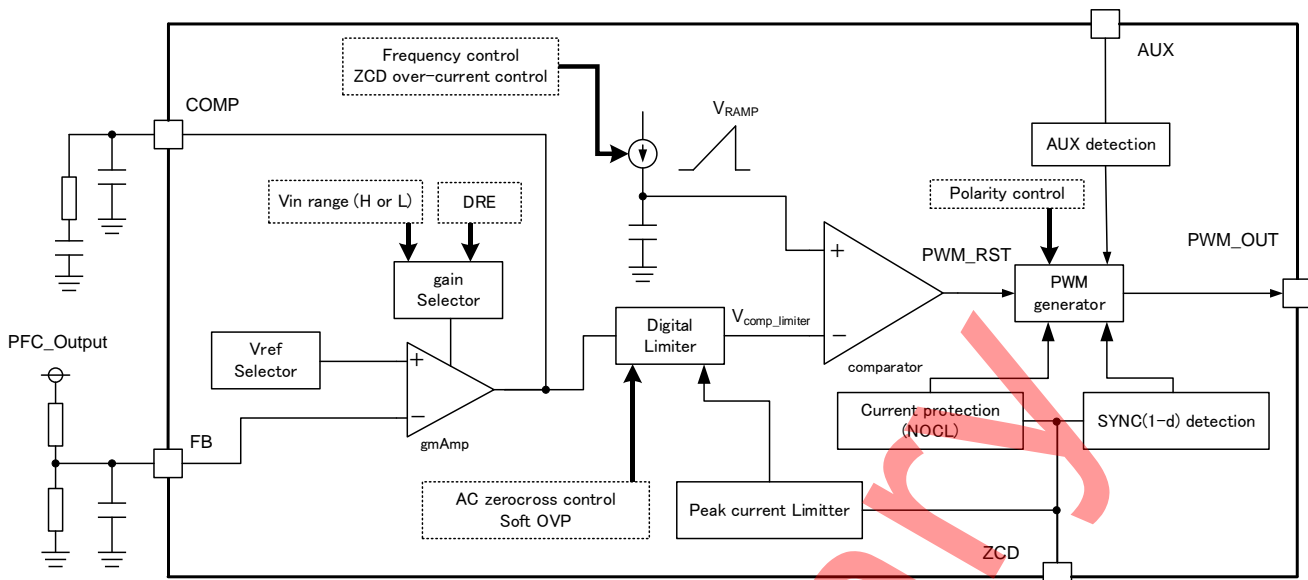


Figure 9. Structure of PWM generation circuit

5. AUX Detection

This IC uses an auxiliary winding and a quasi-resonant control method that detects the valley of the ringing waveform of the drain voltage and turns on the switching device at that timing as shown in Figure 10.

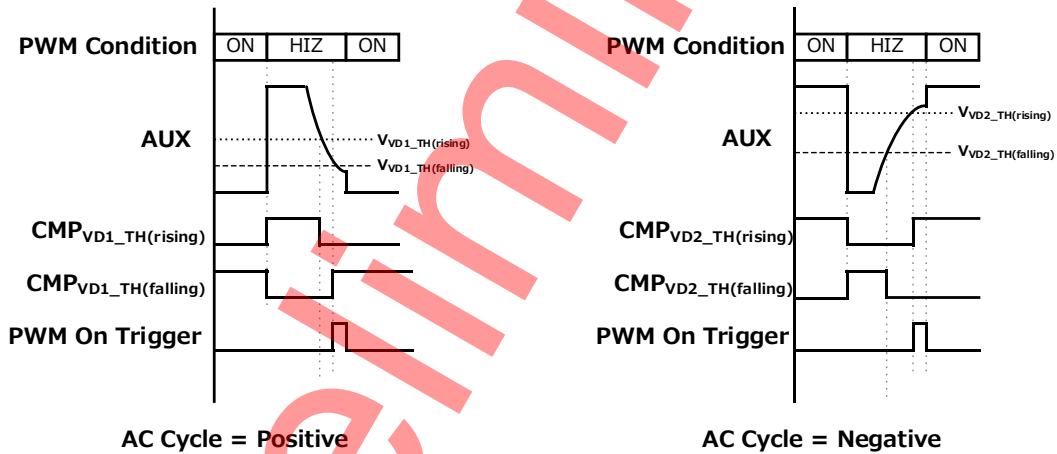


Figure 10. AUX Detection

6. GmAMP

Figure 11 shows the FB pin monitors a divided point for resistance of the output voltage. The ripple voltage of the AC frequency (50 Hz / 60 Hz) overlaps with the FB pin. GmAMP removes this ripple voltage. GmAMP compares  $V_{REF}$  (2.5 V Typ.) with the removed voltage, GmAMP controls the COMP voltage by this gap. When the COMP pin voltage rises, the ON width of the PWMH/PWML pin becomes wide.

Also, you must set the error amplifier constant so that the AC frequency does not overlap on the COMP pin. And, please confirm it with an actual board.

A typical trans-conductance gain of 70uS typ.

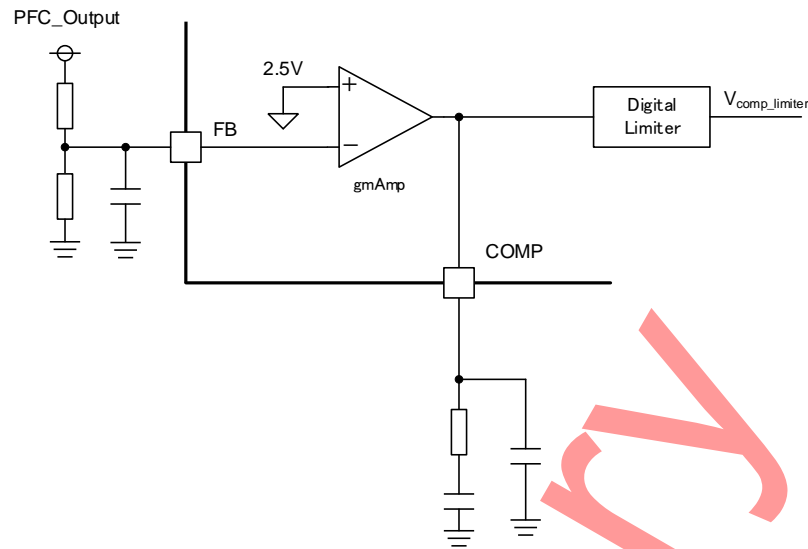


Figure 11. GmAMP Block Diagram

**7. Dynamic Response Enhancer (DRE)**

This IC has a function to suppress output undershoot.

When the FB pin voltage falls below ratio  $[R_{DRE\_LO}]$  of  $V_{REF}$ , the control loop gain is increased to suppress output undershoot. The high gain state continues until the FB pin voltage returns to ratio  $[R_{DRE\_HI}]$  of  $V_{REF}$ .

**8. Light load operation (DCM)**

Figure 12 shows this controller enters light load operation mode (DCM) when output load becomes light load and COMP voltage falls below  $V_{DCM\_TH2}$  threshold.

In DCM, the interval during which the inductor current becomes 0A ( $t_{HIz}$ ) becomes longer and the switching frequency gradually decreases.

$t_{HIz}$  becomes longer in proportion to the difference between COMP and  $V_{DCM\_TH2}$  voltage, COMP- $V_{DCM\_TH2}$  voltage.

If ON pulse widths are equal in DCM and CrM, entering DCM from CrM reduces the switching frequency and current supply to the output capacitor, so the COMP voltage rises in the next AC half cycle and returns to CrM mode.

To prevent such CrM and DCM from alternating in the AC half-cycle and worsening THD, the ON pulse width of DCM is controlled to be thicker than that of CrM.

During the  $t_{HIz}$  interval, the  $V_{DS}$  voltage resonates.

The next ON is initiated at the timing of the trough of the  $V_{DS}$  resonance.

When the load current increases and the COMP voltage rises above the  $V_{DCM\_TH1}$  voltage, it enters CrM.

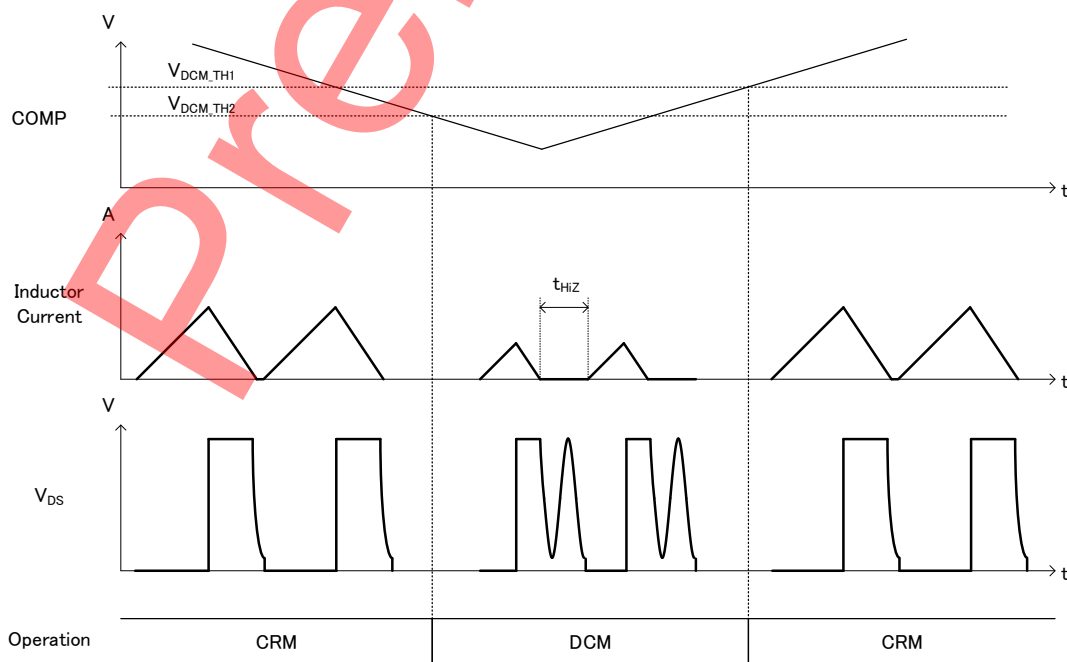


Figure 12. Transition from CRM Mode to DCM Mode

**9. Burst Mode Operation**

Burst mode operation at light load is implemented.

Figure 13 shows when the load becomes light and the COMP voltage reaches  $V_{CLAMP\_TH}$ , the error amplifier output COMP pin clamps and the FB voltage increases, after the FB voltage reaches  $V_{softOVP}$ , the controller enters the sleep state.

The quiescent current in sleep state is reduced to  $I_{CC3}$ . When the FB voltage reaches  $V_{BURST\_TH}$ , the controller automatically returns from sleep state and starts PWM.

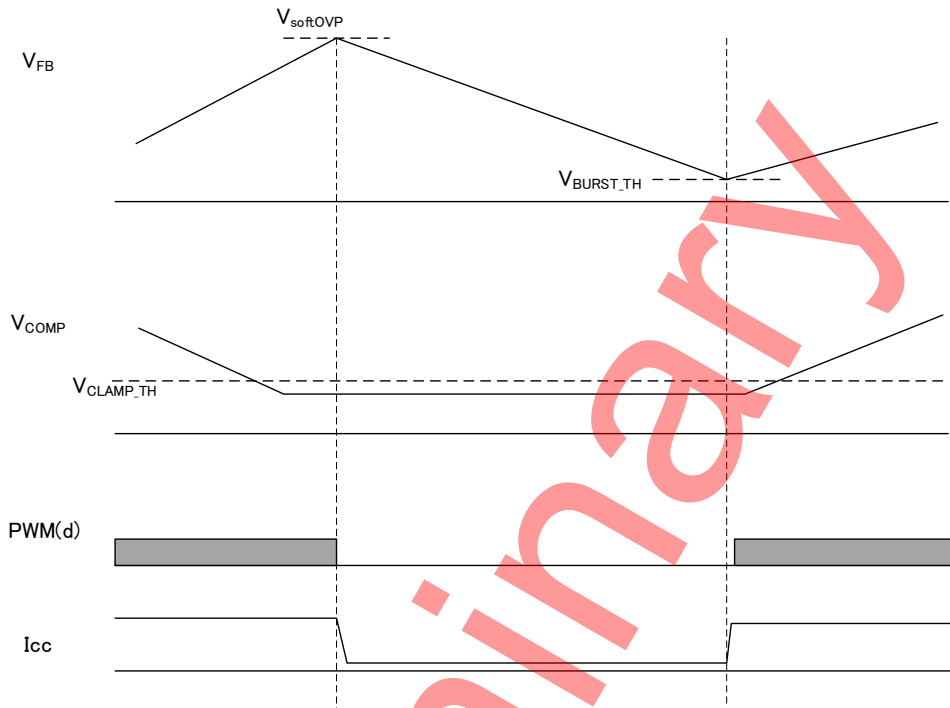


Figure 13. Burst mode operation

**10. Zero Current Detection and synchronous PWM Drive Control**

Figure 14 shows the zero current is detected by using the shunt resistor in series with the output capacitor to detect commutation timing. The inductor discharge current that flows to the load during the 1-D period of the switching cycle can be monitored by using a series sensing element.

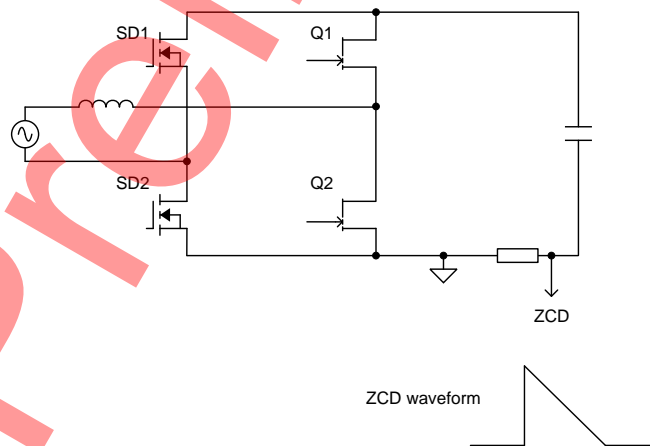


Figure 14. Zero Current Detection via ZCD pin

Figure 15 shows synchronous PWM driving pulses are only enabled at higher loads when the ZCD voltage is above the  $V_{ZCD(ARM)}$  threshold. The conditions to enable synchronous PWM drive are as follows.

- ZCD voltage crosses the  $V_{ZCD(ARM)}$  threshold
- $V_{LINE}[absolute\ value\ of\ (V_{LVNS1} - V_{LVNS2})]$  voltage exceeds  $V_{SYNC}$
- PFCOK is high



SYNC(1-D) pulses are enabled only at higher loads for efficiency improvement across all load conditions. This avoids premature enabling of the SYNC(1-D) pulses and enhances efficiency. This also prevents reverse currents during startup.

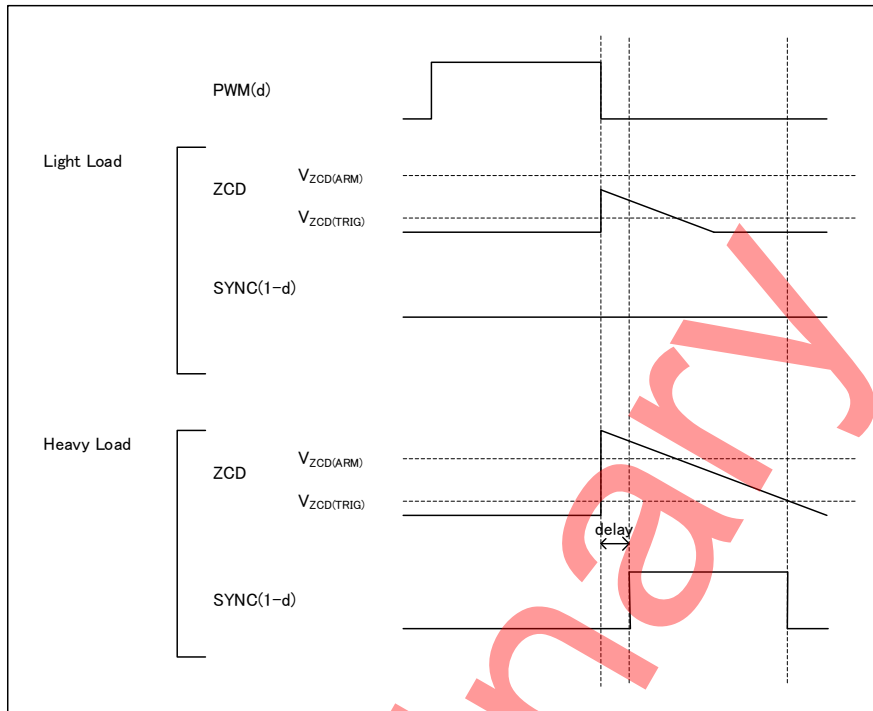


Figure 15. Synchronous PWM Drive Control

**11. Line Range Detection**

Since PFC must operate correctly over a wide input voltage range, the PFC controller must control and limit the operation of external components as input voltage changes. When  $V_{LINE}$  exceeds the high line threshold  $V_{HLine}$ , the IC transitions to high line mode. When  $V_{LINE}$  falls below the low line threshold  $V_{LLine}$  in high line mode, the IC returns to low line mode. This mode switching switches the parameters inside the IC. This allows the control characteristics to be switched according to the input voltage.

**12. PWM polarity control, AC Zero Crossing Management**

Figure 16 shows PWM polarity control and AC zero-crossing management is a feature that determines when to enable or disable the various drive signals at the beginning and end of each half-line cycle. This feature is controlled by LVSNS1 pin and LVSNS2 pin. IC detects difference between these 2 pins. The polarity of PWM depends on the polarity of this difference. When  $(V_{LVSNS1} - V_{LVSNS2})$  is positive, PWML pin works as PWM(d) signal source and PWMH pin works as SYNC(1-d) signal. When  $(V_{LVSNS1} - V_{LVSNS2})$  is negative, PWMH pin works as PWM(d) signal source and PWML pin works as SYNC(1-d) signal. The same can be applied for SRL and SRH pins. This function change is controlled by Polarity signal generated internally from LVSNS1 pin and LVSNS2 pin.

Following 2 types of PWM control function is implemented to avoid large current flow around AC zero-crossing.

[ACZ SoftStart]

Function to gradually increase PWM pulse width from minimum value.

This function is triggered when  $V_{LINE}$  (absolute value of  $V_{LVSNS1}-V_{LVSNS2}$ ) is larger than  $V_{ZCB}$  and stops when following 2 conditions detected.

- (A)  $V_{LINE}$  is larger than  $V_{SR}$ .
- (B)  $t_{AC\_SOFTSTART}$  period timeout.

[ACZ SoftStop]

Function to gradually decrease PWM pulse width to minimum value.

This function is triggered when  $V_{LINE}$  (absolute value of  $V_{LVSNS1}-V_{LVSNS2}$ ) is smaller than  $V_{SR}$  and stops when following 2 conditions detected.

- (A) Polarity change is detected.
- (B)  $t_{AC\_SOFTSTOP}$  period timeout.

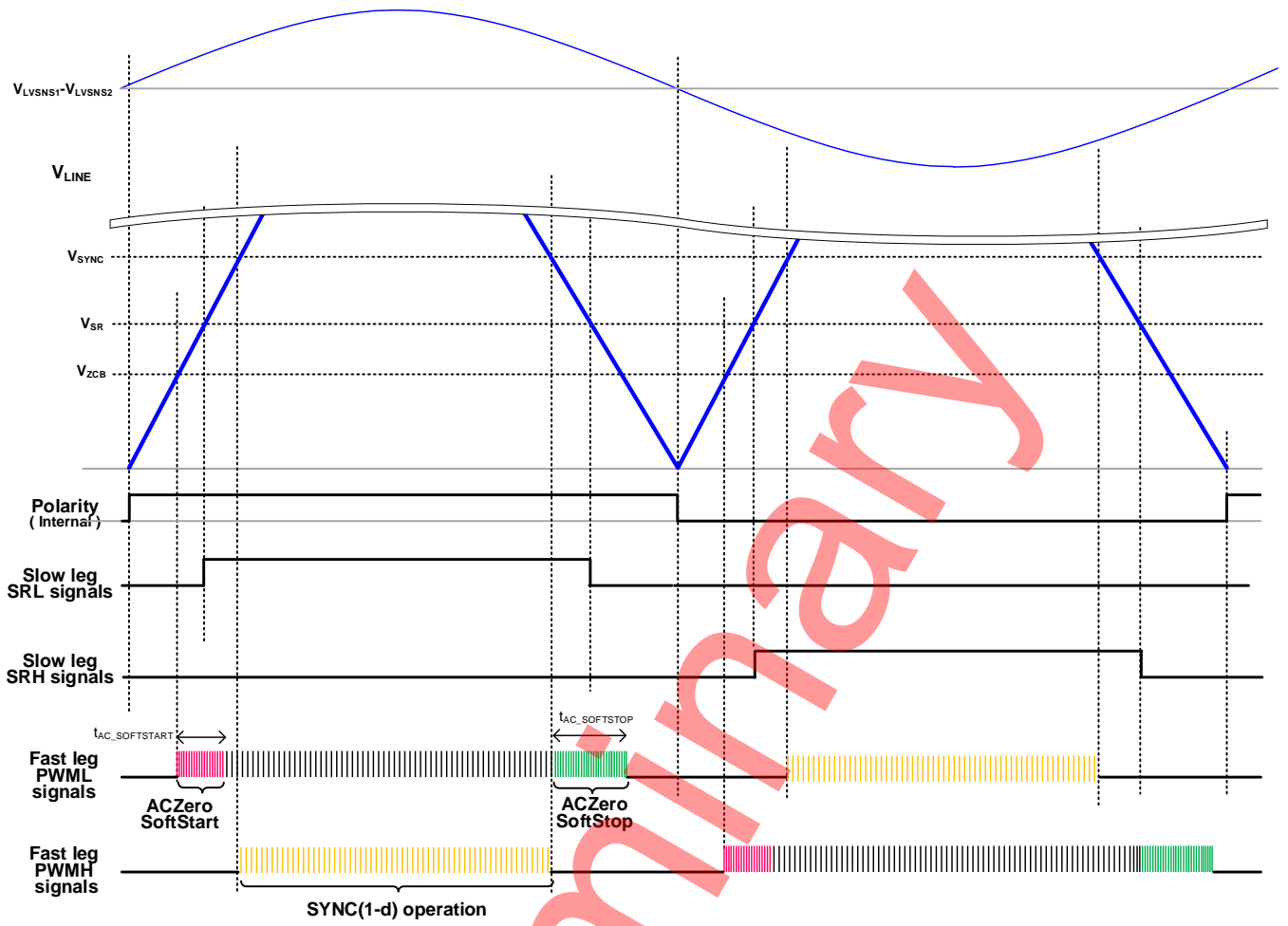


Figure 16. AC Zero Crossing Management

**13. Cycle-by-Cycle Peak Current Limit Protection**

Cycle-by-cycle peak current limitation is used to protect flowing large current into inductor or transistor. This function can be achieved by following 2 methods.

(a) CS pin detection (optional)

Figure 17 shows CS pin is connected to current transformer and signal conditioning circuit. This enables to measure the inductor current at both AC positive cycle and negative cycle. When CS pin voltage ( $V_{CS}$ ) reaches to  $V_{CS1\_LIM\_Pos}$  or  $V_{CS1\_LIM\_Neg}$ , controller stops PWM(d) state to prevent large current flow. If the AC line voltage level is changed from Low-line level(100Vac range) to High-line level(200Vac range), threshold of  $V_{CS1\_LIM}$  is decreased.

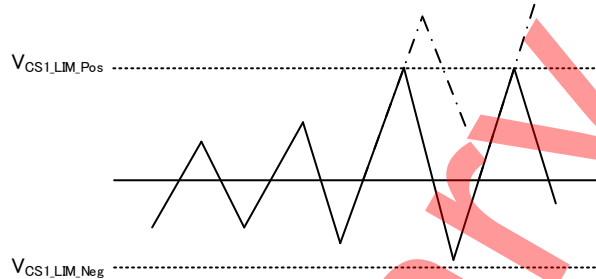


Figure 17. Cycle-by-Cycle Peak Current Limit Protection at CS pin

(b) ZCD pin detection

Figure 18 shows ZCD pin can detect the commutation current. Internal control logic detects peak voltage and limits PWM on time when ZCD pin voltage exceeds specified value ( $V_{ZCDLIM}$ ). When  $V_{ZCD}$  exceeds  $V_{ZCDLIM}$ , limit level of digital limiter in PWM block is increased. If  $V_{ZCD}$  is lower than  $V_{ZCDLIM}$  at next switching, limit level is decreased.

If the AC line voltage level is changed from Low-line level (100Vac range) to High-line level (200Vac range), threshold of  $V_{ZCDLIM}$  is decreased.

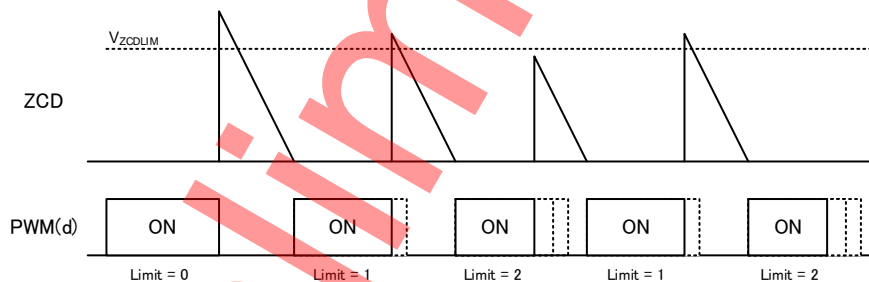


Figure 18. Peak current limiter via ZCD pin

**14. Inductor Saturation Protection (optional)**

Figure 19 shows CS pin has second voltage threshold ( $V_{CS2\_LIM}$  and  $-V_{CS2\_LIM}$ ) to prevent over current destruction of semiconductors caused by inductor saturation current.

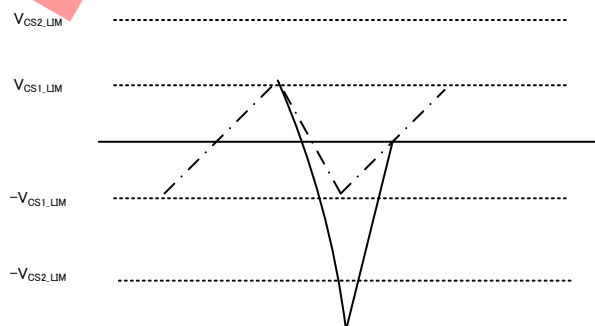


Figure 19. Inductor Saturation Protection

After CS voltage reaches to  $V_{CS2\_LIM}$ , controller stops all PWM and become latch-off state.

15. Inrush Current Protection

Figure 20 shows after power-on (when waiting for start-up), if the voltage at the ZCD pin is higher than  $V_{INRUSH}$ , switching is not performed.

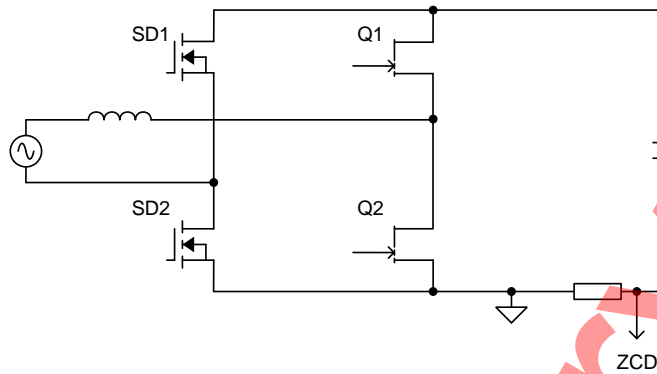


Figure 20. Inrush Current Protection

16. Negative Over Current Limiter (NOCL)

Figure 21 shows if SD1 turns on while SD2 has a short-circuit fault, a short circuit occurs between output (+) and GND. This is also same to Q1 and Q2. Large current flows from the output capacitor (shoot through current). To protect against this, this function stops PWM and SRL / SRH when negative voltage detects at ZCD pin.

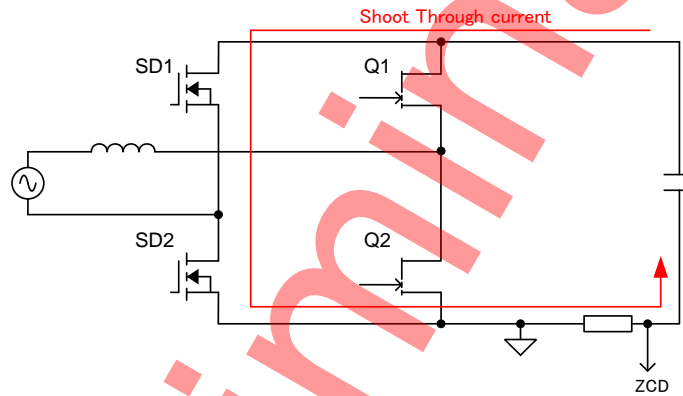


Figure 21. Target current of NOCL function

Figure 22 shows when shoot through current occurs and ZCD voltage decrease less than  $V_{NOCL}$ , IC stops PWMs and SRL / SRH.

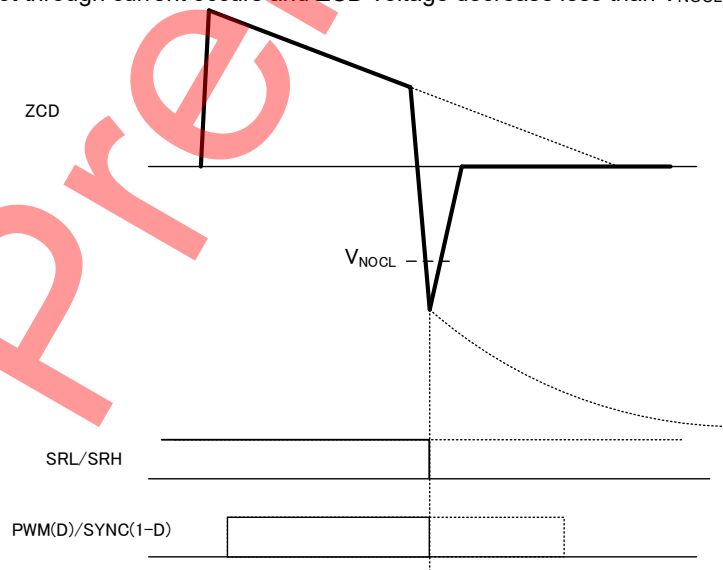


Figure 22. Abnormal current protection of NOCL function

Figure 23 shows this function has latch-stop protection. When NOCL protection occurs several times and protection count reach to 3 times, internal fault flag is set and IC stop operation (Latch-stop). This counter is reset in each AC zero crossing timing if counter is less than 3.

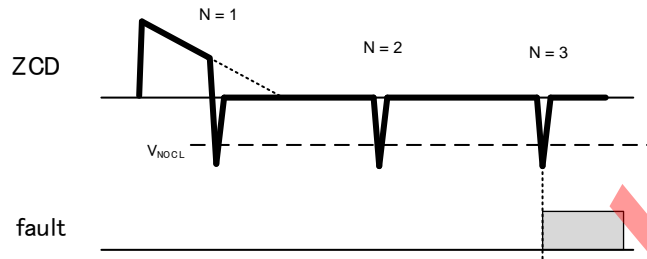


Figure 23. Latch protection in NOCL detection

## 17. UVP, BUV

IC has 2 levels of protection for output under voltage, UVP and BUV.

[UVP (Output Under Voltage Protection)]

UVP is detected when  $V_{FB}$  is lower than  $V_{UVP}$ . After detected, both fast leg and slow leg are stopped. Main reset is needed to reset UVP.

[BUV (Bulk Under Voltage)]

BUV is detected when  $V_{FB}$  is lower than  $V_{BVP}$  once after PFCOK is set. After detected, both fast leg and slow leg are stopped. After  $t_{BUV}=500ms$  is passed since BUV flag is set, BUV is automatically reset.

## 18. OVP (Output Over Voltage Protection)

Figure 24 shows IC has 3 level of over voltage protection threshold to protect system and circuits.

### (a) Static OVP

Static OVP detects a feedback pin anomaly and immediately stop the PWM pulses. When  $V_{FB}$  voltage exceeds ratio  $[R_{StaticOVP}]$  of  $V_{REF}$ , static OVP is triggered and PWM stops. This fault cannot be reset until main reset occur.

### (b) Fast OVP

Fast OVP detects a feedback pin anomaly and immediately stop the PWM pulses. When  $V_{FB}$  voltage exceeds ratio  $[R_{fastOVP}]$  of  $V_{REF}$ , fast OVP is triggered and PWM stops. After fastOVP triggered and  $V_{FB}$  voltage decreases to ratio  $[R_{OVPrecover}]$  of  $V_{REF}$ , fastOVP function is reset and PWM will recover.

### (c) Soft OVP

Soft OVP detects feedback pin anomaly and slowly stops the PWM pulses. This function is achieved by controlling Error amplifier output limiter  $[V_{comp\_limiter}]$ . When  $V_{FB}$  voltage exceeds ratio  $[R_{softOVP}]$  of  $V_{REF}$ , following softOVP actions will start.

Step 1:  $V_{comp\_limiter}$  drops to 75% of the  $V_{comp}$  value for 100us.

Step 2:  $V_{comp\_limiter}$  drops to 50% of the  $V_{comp}$  value for 100us.

Step 3:  $V_{comp\_limiter}$  drops to 25% of the  $V_{comp}$  value for 100us.

Step 4:  $V_{comp\_limiter}$  drops to 0 until the Soft OVP fault is reset.

After softOVP triggered and  $V_{FB}$  voltage decreases to ratio  $[R_{OVPrecover}]$  of  $V_{REF}$ , softOVP function is reset and PWM will recover.

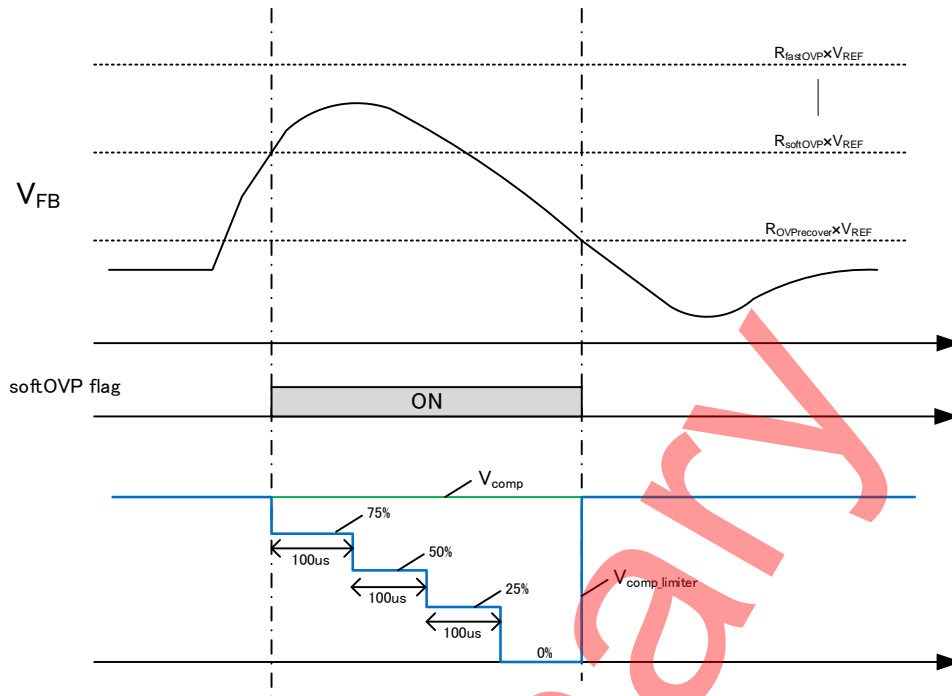


Figure 24. soft OVP (Output Over Voltage Protection)

**19. VAC OVP (Input Over Voltage Protection)**

If a higher than typical mains voltage is applied to this IC, the output voltage can easily rise to the fastOVP or staticOVP level. To suppress this fault, a second overvoltage protection is implemented on the input side. When  $V_{LINE}$  voltage exceeds 4V typ, IC detects over voltage of input side and stop PWM operation. After  $V_{LINE}$  decreases 4V, this fault is reset and PWM will be restarted.

**20. Brown-out (BO) and Line sag**

Figure 25 shows the IC feature set includes line voltage Brown-out (BO) and Line sag (SAG) detection. Both BO and SAG are activated when Line voltage falls below  $V_{BO(STOP)}$ . When  $V_{LINE} > V_{BO(START)}$ , the controller will return from the BO or SAG fault state.

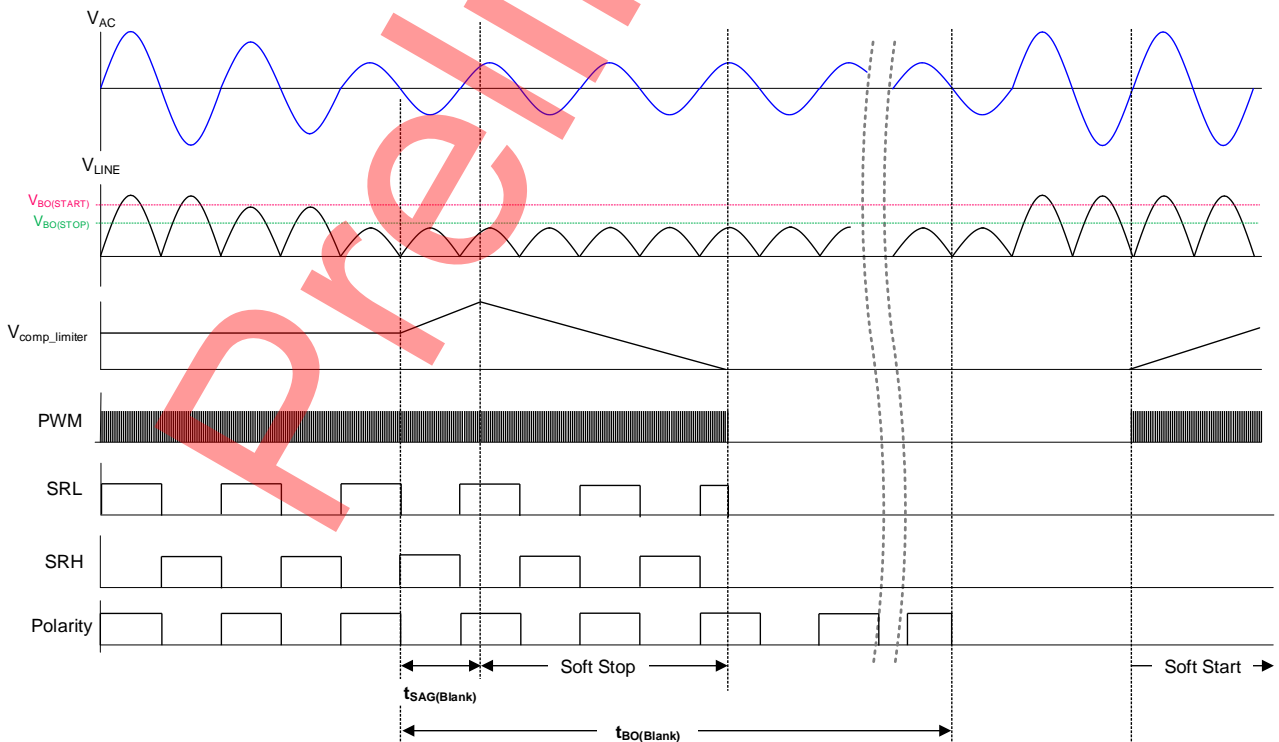


Figure 25. Brown-out (BO) and Line sag

[SAG function]

(1)Detect Condition

$V_{LINE}$  is lower than  $V_{BO(STOP)}$  for  $t_{SAG(blank)}$  or more.

(2)Action

Soft stop operation is started.

(3)Release condition

$V_{LINE}$  is larger than  $V_{BO(START)}$ .

[BO function]

(1)Detect Condition

$V_{LINE}$  is lower than  $V_{BO(STOP)}$  state for  $t_{BO(blank)}$  or more.

(2)Action

Disables the polarity detection circuit.

(3)Release condition

$V_{LINE}$  is larger than  $V_{BO(START)}$ .

**21. Line Frequency Fault**

Figure 26 shows IC monitors whether the AC line frequency is within the mains frequency specification ( $f_{LINE(LO)}$  to  $f_{LINE(HI)}$ ). If abnormal mains frequency detects, following steps are operated.

[Step1] If outside of the expected frequency range, stops slow leg. PWM continues operation.

[Step2] If 100ms elapsed since abnormal mains frequency detected, Both fast leg and slow leg is stopped. IC will recovery from this fault state if IC detects 4 consecutive polarity edges that are within the expected frequency range (same as a startup).

The IC measures the time between every edge transition of the filtered polarity signal.

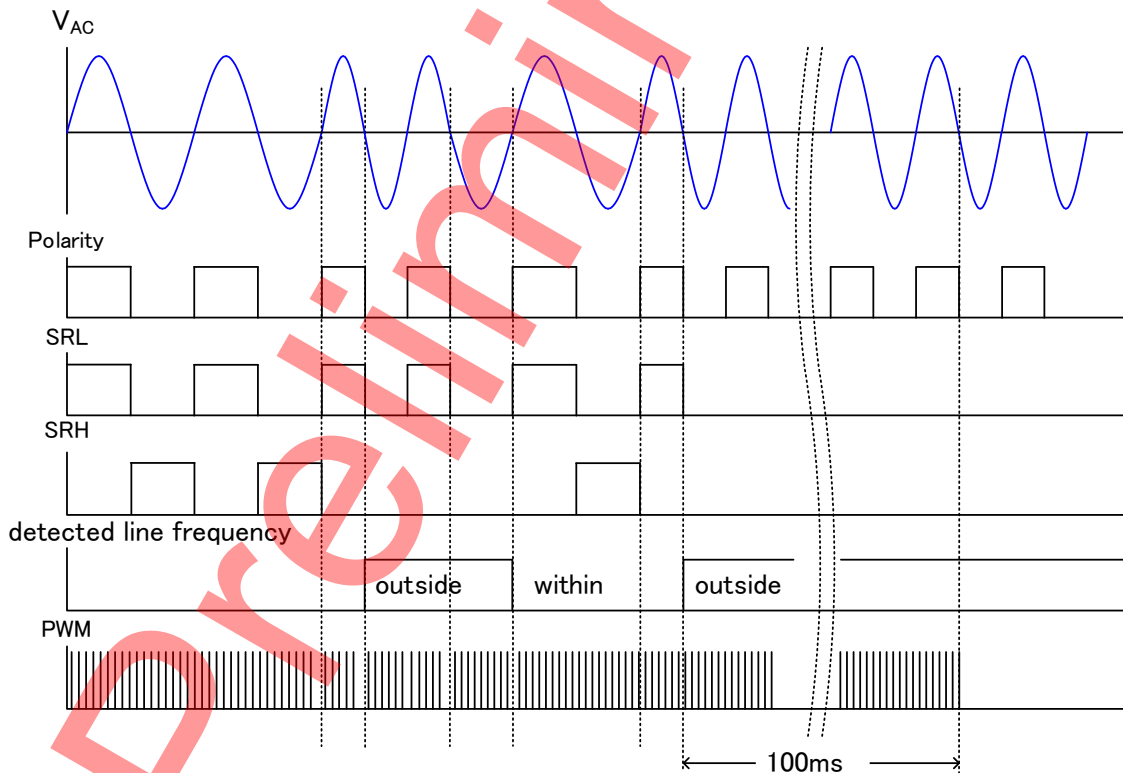


Figure 26. Line Frequency Fault

**22. AC Line Voltage sudden change protection**

Figure 27 shows If the AC input voltage changes suddenly due to the application of lightning surge voltage, etc., the sudden voltage change may cause current to flow back from the output side. To prevent FET failure due to excessive current, controller turns off the gate signals of slow leg and SYNC(1-D) when  $dv / dt$  of input voltage exceeds a certain level or abnormal timing change of polarity occurs.

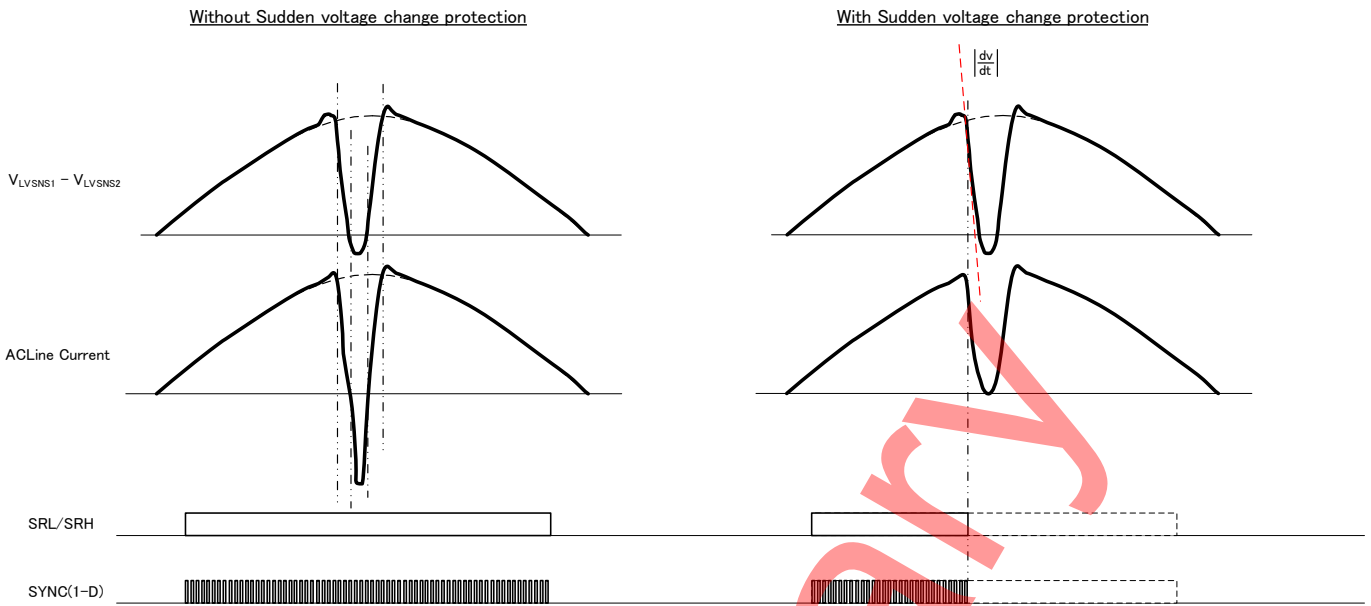


Figure 27. AC Line Voltage sudden change protection

**23. Internal TSD**

Detect Condition:

Junction temperature ( $T_j$ ) exceeds TSD detection temperature ( $140^{\circ}\text{C}$ )

Action:

stops fast leg and slow leg.  
Polarity signal remains active.

Release condition:

$T_j$  falls below the  $T_{SD}-T_{SD(HYS)}$  release temperature ( $115^{\circ}\text{C}$ )

**24. External fault control (FAULT pin)**

FAULT pin has comparator for detecting faults as shown in Figure 28.

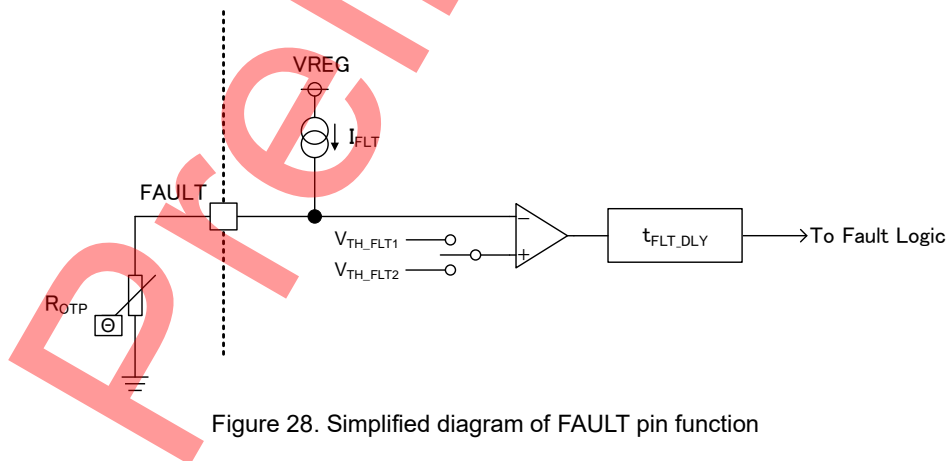


Figure 28. Simplified diagram of FAULT pin function

External TSD can be achieved by connecting thermistor to fault pin. Internal current source ( $I_{FLT}$ ) is used for this function. This pin also can be used as OVP by adding detection circuit.



## 25. Fault summary

Following table shows protection features, the conditions needed to set or reset the fault, and the action of the IC for the given fault.

Fault	Set condition	Reset condition	Controller Action
Line SAG	$(V_{LINE} < V_{BO(STOP)}) + t_{SAG(blank)}$ expired	$V_{LINE} > V_{BO(START)}$	- Begin soft stop sequence - PWM and SR drives disabled after soft stop - PFCOK pulled low (OFF Mode) after soft stop - Cancels $t_{BUV}$
Brownout	$(V_{LINE} < V_{BO(STOP)}) + t_{BO(blank)}$ expired	$V_{LINE} > V_{BO(START)}$	- Disables the polarity detection circuit - PFCOK pulled low (OFF Mode)
Line Frequency 1	$t_{LINE} < t_{LINE(45)}$ or $> t_{LINE(65)}$	$t_{LINE(45)} < t_{LINE} < t_{LINE(65)}$	- SR drives disabled - Starts 100ms timer
Line Frequency 2	100ms timer expired	$N_{DRV\_EN} = 4 : t_{LINE(45)} < t_{LINE} < t_{LINE(65)}$ for 4 consecutive polarity toggles	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
UVP	$V_{FB} < V_{UVP}$	$V_{FB} > V_{UVP} + V_{UVP(HYS)}$	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
Bulk Under Voltage (BUV)	PFCOK high & $(V_{FB} < V_{BUV})$	$t_{BUV}$ expires	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode) - Automatic restart after $t_{BUV}$
Soft OVP	$V_{FB} > V_{softOVP}$	$V_{FB} < V_{OVPrecover}$	- Begin soft OVP sequence - PWM Drive disables after soft OVP sequence - SR remains active
Fast OVP	$V_{FB} > V_{fastOVP}$	$V_{FB} < V_{OVPrecover}$	- PWM Drive disables immediately - SR remains active
Static OVP	$V_{FB} > V_{staticOVP}$	Main Reset	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
VAC OVP	$V_{LINE} > V_{ACOVP}$	$V_{LINE} < V_{ACOVP}$	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
$V_{CC}$ UVLO	$V_{CC} < V_{UVLO2}$	$V_{CC} > V_{UVLO1}$	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
External Fault	$V_{FAULT} < V_{TH\_FLT2}$	$V_{FAULT} > V_{TH\_FLT1}$	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
CS OCP2	$V_{CS} > V_{CS\_LIM2\_Pos}$ OR $V_{CS} < V_{CS\_LIM2\_Neg}$	Main Reset	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
NOCL latch	NOCL detected $N_{NOCL\_detect}$ times	Main Reset	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)
TSD	$T_J > T_{SHDN}$	$T_J < (T_{SD} - T_{SN(HYS)})$	- PWM and SR drives disabled - PFCOK pulled low (OFF Mode)

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

## 10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

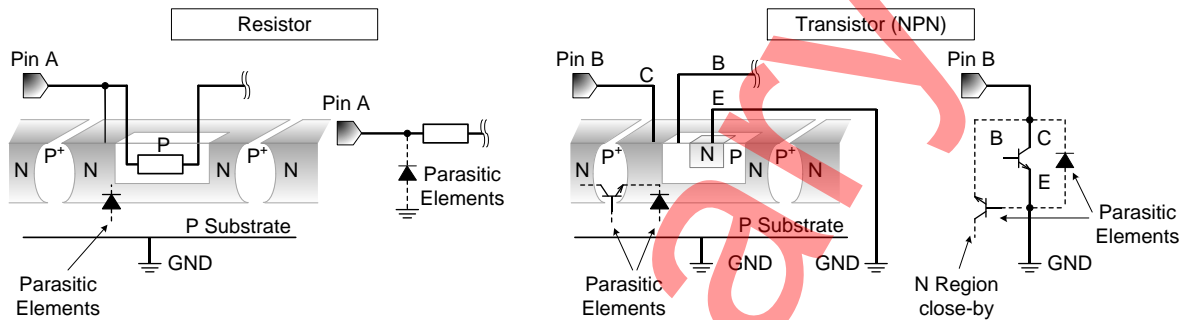


Figure 29. Example of Monolithic IC Structure

## 11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

## 12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

## 13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

## Revision History

Date	Revision	Changes
19.May.2023	001	New Release
01.Jun.2023	002	Single
26.Oct.2023	005	DS1 design reflected.
11.Oct.2024	006	DS2 design reflected.

Preliminary

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment <sup>(Note 1)</sup>, aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
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  - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

**Precautions Regarding Application Examples and External Circuits**

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

**Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

**Precaution for Storage / Transportation**

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

**Precaution for Product Label**

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

**Precaution for Disposition**

When disposing Products please dispose them properly using an authorized industry waste company.

**Precaution for Foreign Exchange and Foreign Trade act**

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