AC/DC Controller IC

LLC Controller IC

BM85080FV-LB

General Description

BM85080FV is the product guarantees long time support in industrial market. This is a high frequency available current mode controller for LLC half bridge resonant converter, which helps low EMI because of soft switching. And controller outputs are ideal for gate drivers for GaN. This controller has built-in HV start-up circuit. And the built-in Brown-Out protection helps to implement in any AC/DC application.

Key Specifications

- Input Voltage Range: 8V to 30V
- Absolute Maximum Rating: 33V
- Frequency Range: 25kHz～2MHz
- Quiescent Current: 150uA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W(Typ) x D (Typ) x H (Max)
SSOP-B20	6.5 mm x 6.4 mm x 1.45 mm

Features

- LLC Topology
- Current Mode Operation
- Burst Mode Operation at Light Load
- Wide Operating VCC Voltage Range
- Wide Operating Frequency Range
- Integrated HV Startup Circuit
- Auto Adjustment Deadtime Control
- X2-Capacitor Discharge Function
- Protections
  - AC Under Voltage Lockout
  - VS Under Voltage Lockout
  - VCC Under Voltage Lockout
  - VREG Under Voltage Lockout
  - Over Voltage Protection
  - Over Temperature Protection
  - Overload Protection
  - Over Current Protection
  - Open Feedback Loop Detection
  - Out of Resonance Switching Protection
  - Thermal Shut Down

Applications

- Adapters
- Computing Power Supplies
- Flat Panel Display Power Converters

Typical Application Circuit

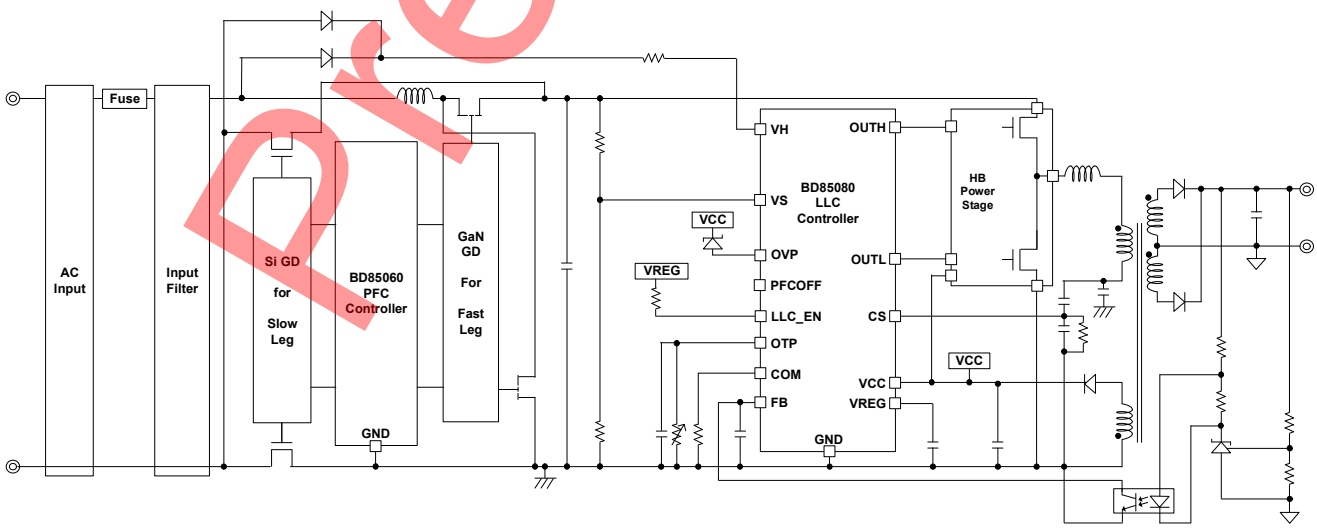


Figure 1. Typical Application Circuit

Contents

Pin Configuration

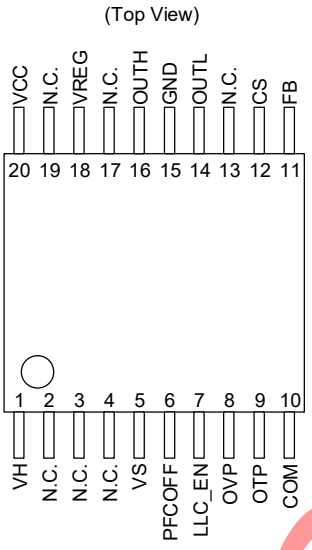


Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1	VH	High voltage startup.
2	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
3	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
4	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
5	VS	Bulk voltage sense input.
6	PFCOFF	Output signal for controlling PFC device.
7	LLC_EN	Enable input. H is enable, L is disable.
8	OVP	Over voltage protect detection pin.
9	OTP	Over temperature protect detection pin.
10	COM	Test pin.
11	FB	Output feedback voltage input.
12	CS	Current sense voltage input.
13	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
14	OUTL	Control output signal for low side FET of Half-bridge power stage.
15	GND	Ground connection.
16	OUTH	Control output signal for high side FET of Half-bridge power stage.
17	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
18	VREG	Internal regulator output.
19	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements. *(Note1)*
20	VCC	Input power supply.

(Note1) Do not connect to other pins.

Block Diagram

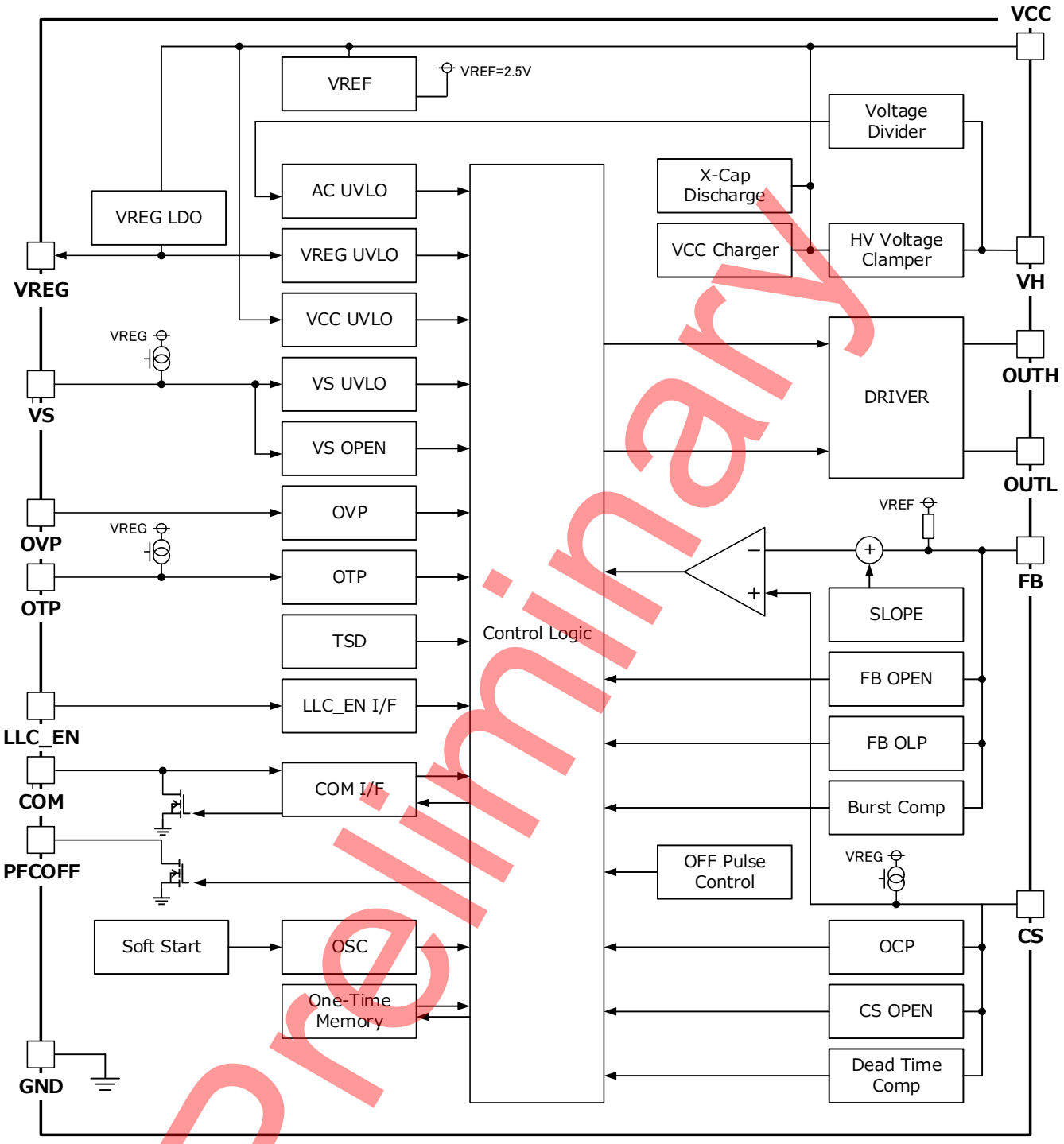


Figure 3. Block Diagram

Description of Blocks

- VREG LDO
  Block creating internal reference voltage 5V (Typ.).
- VREF
  Reference voltage for internal blocks.
- AC UVLO
  AC input disconnection detection circuit. When the AC input disconnection is detected, OUTH/OUTL turns off, and when XCAP_DIS_OFF=1, it initiates X capacitor discharge.
- VREG UVLO
  An internal low-voltage detection circuit. When low voltage is detected, all registers are reset and OUTH/OUTL are turned off. When the VREG voltage recovers over $V_{VREGUVLO\_R}$, this protection releases immediately.
- VCC UVLO
  VCC low-voltage detection circuit. When low voltage is detected, OUTH/OUTL are turned off. When the VCC voltage recovers over $V_{VCCUVLO\_R}$, this protection releases immediately.
- VS UVLO
  VS low-voltage detection circuit. When low voltage is detected, OUTH/OUTL are turned off. When the VS voltage recovers over V_{VSUVLO_R}, this protection releases immediately.
- VS OPEN
  VS open detection circuit. VS open detection functions only before OUTH/OUTL activation. OUTH/OUTL remain OFF until the VS voltage falls below V_{VSOPEN_F}.
- OVP
  OVP terminal over voltage detection circuit. When high voltage is detected, all OUTH/OUTL are turned off. Latch-type or Recovery-type protection is determined by RECOV_OVP register.
- OTP
  OTP terminal under voltage detection circuit. When low voltage is detected, all OUTH/OUTL are turned off. Latch-type or Recovery-type protection is determined by RECOV_OTP register.
- TSD
  IC internal over temperature detection circuit. When over temperature is detected, OUTH/OUTL are turned off. When IC temperature recovers below T_{TSD_F}, this protection releases immediately.
- LLC_EN I/F
  LLC_EN terminal H/L detection circuit. When LLC_EN is low level, OUTH/OUTL are turned off. When LLC_EN is high level, this constraint releases immediately.
- COM I/F
  This is a test circuit intended for test purposes. Ensure to connect the COM terminal to a pull-down resistor.
- Soft Start
  Soft start timer control circuit. This block controls OUTH/OUTL ON period during soft start. The soft start deration is set by the SS_TIMER register.
- OSC
  Oscillation circuit for Control Logic.
- One-Time Memory
  The register map function is implemented using One-Time Memory.
- Voltage Divider
  Divided voltage of VH for judging AC UVLO.
- X-Cap Discharge
  When VH is unplugged from external power supply, X-Cap Discharge is activated to loose current of X capacitor. When XCAP_DIS_OFF=1, it initiates X capacitor discharge.
- VCC Charger
  Charge support of VCC to reach at $V_{VCCUVLO\_R}$ (10.5V Typ.), then current charge stops. Charge current is restart at VCC drops to V_{CHG_SP} (9V Typ.) once it reached $V_{VCCUVLO\_R}$. And then current charge stops at V_{CHG_ST} (10V Typ.).
- HV Voltage Clamper
  To clamp VH voltage to supply low voltage for control chip.
- DRIVER
  Driven output for H-side and L-side gate driver.
- SLOPE
  Slope is merged to internal FB signal during OUTH is high.
- FB OPEN
  FB terminal over voltage detection circuit. When high voltage is detected, OUTH/OUTL are turned off. Latch-type or Recovery-type protection is determined by RECOV_OPEN_FB register.
- FB OLP
  FB terminal over voltage detection circuit. When high voltage is detected, OUTH/OUTL are turned off. Latch-type or Recovery-type protection is determined by RECOV_OLP register.
- Burst Comp
  FB terminal under voltage detection circuit. When low voltage is detected, OUTH/OUTL are turned off. When FB terminal voltage recovers over $V_{FB\_BURST\_R}$, OUTH/OUTL are turned on immediately.
- OFF Pulse Control
  Timing generator circuit. Generating active period of OUTL same duration as that of OUTH.

- OCP

CS terminal over voltage detection circuit. When high voltage is detected, OUTH turns off.
Once the number of overcurrent detection cycles exceeds the predetermined count set by OCP_COUNT, both OUTH and OUTL are turned off. Latch-type or Recovery-type protection is determined by RECOV_OCP register.

- CS OPEN
  CS open detection circuit. CS open detection functions only before OUTH/OUTL activation. OUTH/OUTL remain OFF until the CS voltage falls below V_{CSOPEN_F}.
- Dead Time Comp
  These comparators judge current level for controlling adjustable dead time.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
High Voltage Start-Up Circuit Input Voltage (Pin1)	V_{VH}	-0.3 to +650	V
Supply Input Voltage (Pin 20)	V_{VCC}	-0.3 to +33	V
Internal Regulated Voltage (Pin 18)	V_{VREG}	-0.3 to +7.0	V
Input Signal (Pin 5, 7, 8, 9, 10, 11)	V_{VS}, V_{LLC_EN}, V_{OVP}, V_{OTP}, V_{COM}, V_{FB}	-0.3 to +7.0	V
Input Signal (Pin 12)	V_{CS}	-7.0 to +7.0	V
Output Signal (Pin 6, 14,16)	V_{PFCOFF}, V_{OUTL}, V_{OUTH}	-0.3 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 ～ +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
SSOP-B20				
Junction to Ambient	θ_{JA}	115.4	57.3	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	10	8	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for VH	V_{VH}	80	-	600	V
Supply Voltage for VCC	V_{VCC}	8	-	30	V
Operating Temperature	T_{OP}	-40	+25	+125	°C
VREG output Capacitor *(Note2)*	C_{VREG}	1	4.7	-	µF

(Note1) This parameter is for 10 A output. Not 100 % tested.
(Note2) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered. If a bulk capacitor is used with Input ceramic capacitors, please select capacitors referring page 30.

Electrical Characteristics (Unless otherwise specified V_{VCC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
GENERAL						
Quiescent Current (Standby)	I_{VCC1}	-	50	150	µA	V_{LLCEN} = 0 V
Quiescent Current (Latch Mode)	I_{VCC2}	-	150	350	µA	
Quiescent Current (Auto Recovery Mode)	I_{VCC3}	-	150	350	µA	
Operating Current (Operating)	I_{VCC4}	-	1.6	3.2	mA	F_{SW} = 1MHz
Operating Current (Burst Mode)	I_{VCC5}	-	150	350	µA	No Switching, V_{FB}=1.45V
VCC Under Voltage Lockout Detect Voltage	$V_{VCCUVLO\_F}$	6.15	6.5	6.85	V	V_{VCC} Falling
VCC Under Voltage Lockout Release Voltage	$V_{VCCUVLO\_R}$	10	10.5	11	V	V_{VCC} Rising
VREG Output Voltage	V_{VREG}	4.8	5.0	5.2	V	
VREG Under Voltage Lockout Detect Voltage	$V_{VREGUVLO\_F}$	4.05	4.3	4.55	V	V_{VREG} Falling
VREG Under Voltage Lockout Release Voltage	$V_{VREGUVLO\_R}$	4.25	4.5	4.75	V	V_{VREG} Rising
VH STARTUP						
VCC Recharge Start Voltage	V_{CHG_ST}	8.55	9	9.45	V	V_{VCC} Falling
VCC Recharge Stop Voltage	V_{CHG_SP}	9.55	10	10.45	V	V_{VCC} Rising
Startup Current 1	I_{START1}	0.1	0.3	1.0	mA	V_{VCC} = 0 V
Startup Current 2	I_{START2}	1.3	3	6.5	mA	V_{VCC} = 10.05 V
Startup Off Current	I_{START_OFF}	-	10	25	µA	V_{VH} = 400 V
VH SENSE						
AC Unplug Detect Voltage 0	$V_{ACUVLO0\_F}$	50	57	63	V	V_{VH} Falling
AC Unplug Release Voltage 0	$V_{ACUVLO0\_R}$	75	85	95	V	V_{VH} Rising
AC Unplug Detect Voltage 1	$V_{ACUVLO1\_F}$	87	99	111	V	V_{VH} Falling
AC Unplug Release Voltage 1	$V_{ACUVLO1\_R}$	112	127	142	V	V_{VH} Rising
AC Unplug Detect Voltage 2	$V_{ACUVLO2\_F}$	125	141	158	V	V_{VH} Falling
AC Unplug Release Voltage 2	$V_{ACUVLO2\_R}$	150	170	190	V	V_{VH} Rising
AC Unplug Detect Voltage 3	$V_{ACUVLO3\_F}$	162	184	205	V	V_{VH} Falling
AC Unplug Release Voltage 3	$V_{ACUVLO3\_R}$	187	212	237	V	V_{VH} Rising
AC Unplug Detect Voltage 4	$V_{ACUVLO4\_F}$	200	226	253	V	V_{VH} Falling
AC Unplug Release Voltage 4	$V_{ACUVLO4\_R}$	225	255	285	V	V_{VH} Rising
AC Unplug Detect Voltage 5	$V_{ACUVLO5\_F}$	237	269	300	V	V_{VH} Falling
AC Unplug Release Voltage 5	$V_{ACUVLO5\_R}$	262	297	332	V	V_{VH} Rising
AC Unplug Detect Voltage 6	$V_{ACUVLO6\_F}$	275	311	348	V	V_{VH} Falling
AC Unplug Release Voltage 6	$V_{ACUVLO6\_R}$	299	339	379	V	V_{VH} Rising
AC Under Voltage Lockout Timer	t_{ACUVLO}	TBD	TBD	TBD	ms	

Electrical Characteristics (Unless otherwise specified V_{VCC} = 15 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BULK PROTECTION						
VS Pin Outflow Current	I_{VS}	-	0.05	0.10	µA	
VS Open Protection Detect Voltage	V_{VSOPEN_R}	V_{VREG} × 0.60	V_{VREG} × 0.70	V_{VREG} × 0.80	V	V_{VS} Rising
VS Open Protection Release Voltage	V_{VSOPEN_F}	V_{VREG} × 0.525	V_{VREG} × 0.625	V_{VREG} × 0.725	V	V_{VS} Falling
VS Under Voltage Lockout Detect Voltage	V_{VSUVLO_F}	0.525	0.570	0.615	V	V_{VS} Falling
VS Under Voltage Lockout Release Voltage	V_{VSUVLO_R}	0.575	0.620	0.665	V	V_{VS} Rising
VS Under Voltage Lockout Timer	t_{VSUVLO}	102	128	154	ms	
PFC OFF						
VS Drop Detect Voltage	$V_{VS\_DROP\_F}$	1.04	1.13	1.22	V	V_{VS} Falling
VS Drop Release Voltage	$V_{VS\_DROP\_R}$	0.99	1.08	1.17	V	V_{VS} Rising
PFC OFF On Resistance	R_{PFCOFF}	5	20	100	Ω	I_{PFCOFF} = 1mA
PFC OFF Leak Current	I_{PFCOFF_LEAK}	-	0	10	µA	V_{PFCOFF} = 5V
CONTROLLER OUTPUTS						
Output Voltage Rise time	t_{OH}	-	-	10	ns	Cload = 100 pF 10 - 90% of Output Signal
Output Voltage Fall time	t_{OL}	-	-	10	ns	Cload = 100 pF 10 - 90% of Output Signal
Output Voltage High	V_{OH}	V_{VREG} - 0.1	V_{VREG} - 0.05	V_{VREG}	V	Iload = -1mA
Output Voltage Low	V_{OL}	0	0.05	0.1	V	Iload = +1mA
Maximum Frequency	F_{SW_MAX}	1200	1500	1800	kHz	
Minimum Frequency	F_{SW_MIN}	240	300	360	kHz	
COM						
COM Leak Current	I_{COM}	-	0	10	µA	V_{COM} = 5V
LLC_EN						
LLC_EN high level threshold	V_{LLCEN_HI}	4	-	V_{VREG}	V	V_{LLCEN} Rising
LLC_EN low level threshold	V_{LLCEN_LO}	0	-	1	V	V_{LLCEN} Falling
OUTPUT PROTECTION						
FB Pin Pullup Resistance	R_{FB}	15	18	21	kΩ	
FB Burst Mode Detect Voltage	$V_{FB\_BURST\_F}$	1.15	1.29	1.43	V	V_{FB} Falling
FB Burst Mode Release Voltage	$V_{FB\_BURST\_R}$	1.30	1.45	1.60	V	V_{FB} Rising
FB Overload Protection Detect Voltage	$V_{FB\_OLP\_R}$	2.05	2.2	2.35	V	V_{FB} Rising
FB Overload Protection Release Voltage	$V_{FB\_OLP\_F}$	1.95	2.1	2.25	V	V_{FB} Falling
FB Overload Protection Timer	t_{FBOLP}	44	64	84	ms	
FB Open Protection Detect Voltage	V_{FBOPEN_R}	2.3	2.45	2.6	V	V_{FB} Rising
FB Open Protection Release Voltage	V_{FBOPEN_F}	2.2	2.35	2.5	V	V_{FB} Falling
FB Open Protection Timer	t_{FBOPEN}	1.4	2	2.6	ms	
OUTPUT CURRENT PROTECTION						
Over Current Protection Detect Voltage	V_{OCP}	1.8	1.9	2.0	V	
CS Open Protection Detect Voltage	V_{CSOPEN_R}	2.35	2.5	2.65	V	V_{CS} Rising
FAULT FUNCTION						
OTP Pin Outflow Current	I_{OTP}	3	4	5	uA	
Over Temperature Protection Detect Voltage	$V_{OTP\_FAULT\_F}$	0.36	0.4	0.44	V	V_{OTP} Falling
Over Temperature Protection Release Voltage	$V_{OTP\_FAULT\_R}$	0.81	0.9	0.99	V	V_{OTP} Rising

Over Temperature Protection Filter Delay	t_{OTP_DLY}	22.5	35.0	50.0	us	V_{OTP} Falling
Over Temperature Protection Blanking During Startup	t_{OTP_BLANK}	4	5	6	ms	
Over Voltage Protection Detect Voltage	$V_{OVP\_FAULT\_R}$	0.81	0.9	0.99	V	V_{OVP} Rising
Over Voltage Protection Release Voltage	$V_{OVP\_FAULT\_F}$	0.36	0.4	0.44	V	V_{OVP} Falling
Over Voltage Protection Filter Delay	t_{OVP_DLY}	22.5	35.0	50.0	us	V_{OVP} Rising
Thermal Shutdown Threshold Rising	T_{TSD_R}	-	175	-	°C	Tj Rising
Thermal Shutdown Threshold Falling	T_{TSD_F}	-	150	-	°C	Tj Falling

Function Explanation

1. Basic Control (Current Mode Control)

Mode Control operation

(1) High to Low transition of OUTH
Comparing FB proportional signal and CS proportional signal. Current slope is available to prevent subharmonic oscillation. Current slope ends to rise when OUTH falls.

(2) Low to High transition of OUTL
Switching is done passing after dead time.

(3) High to Low transition of OUTH
Used by analog timer, OUTL high period equals previous OUTH high period.

(4) Low to High transition of OUTH
Switching is done passing after dead time.

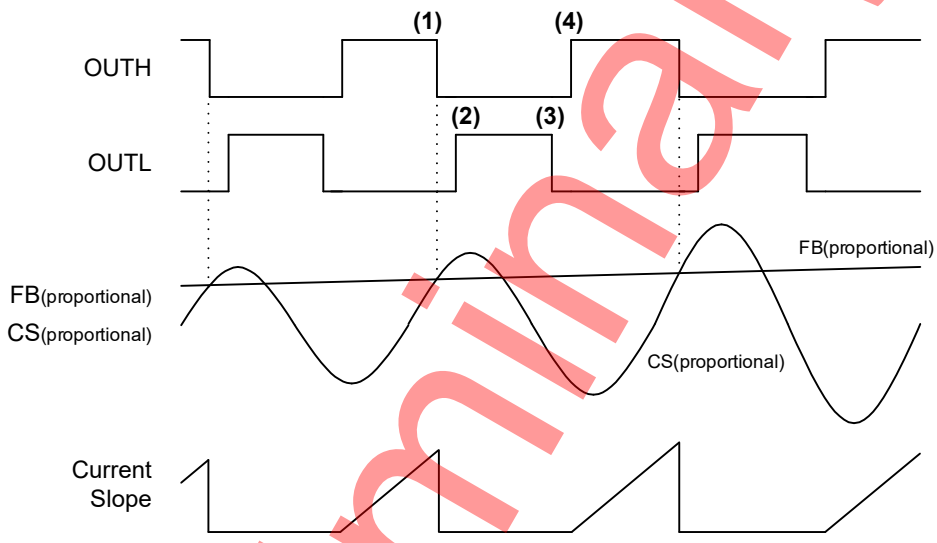


Figure 4. Basic Operation

Function Explanation – continued

2. Startup Sequence

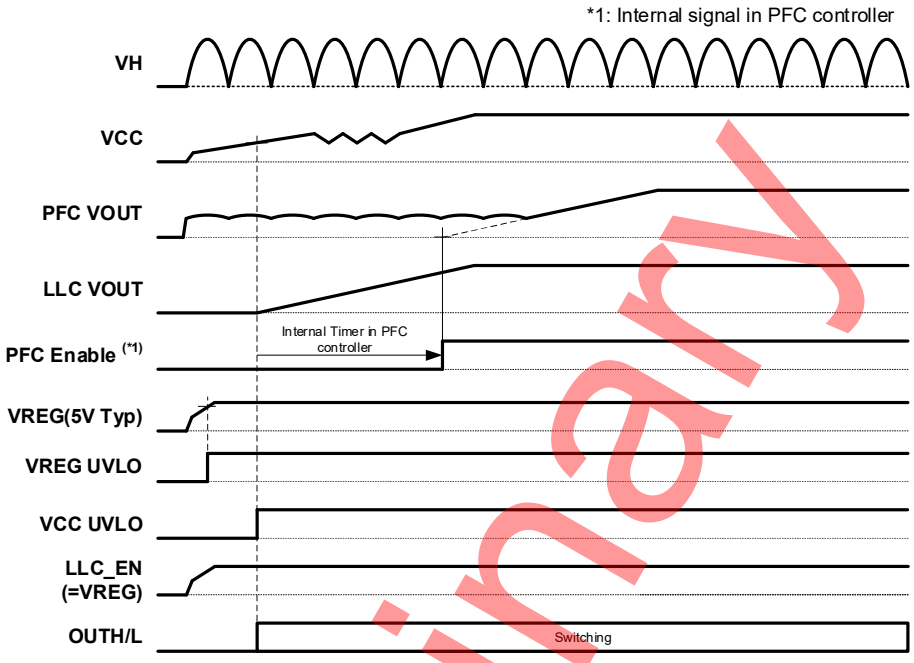


Figure 5. Startup Sequence

Shut down sequence caused by LLC_EN pin.

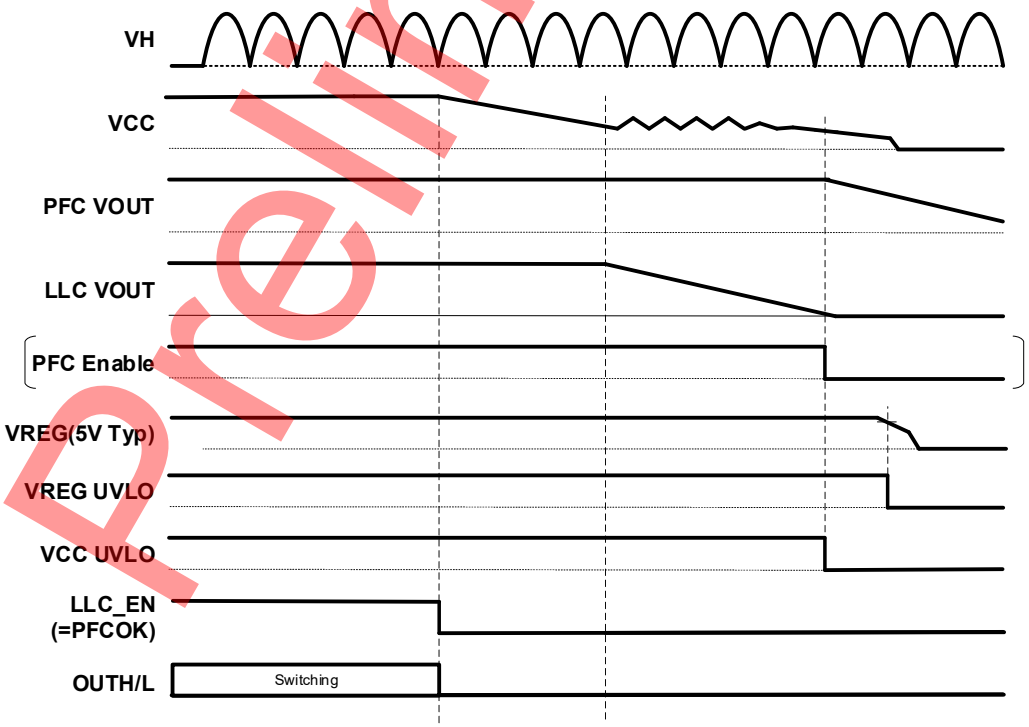


Figure 6. Shutdown Sequence

Function Explanation – continued

3. Starting up circuit and x2 Cap discharge function

This IC has a built-in start-up circuit. It achieves low standby power and high-speed startup.
When AC input voltage is applied, the start-up current is charged to VCC pin from VH pin though the startup circuit.
The charge is stopped after the VCC pin voltage rises and VCC UVLO is released.

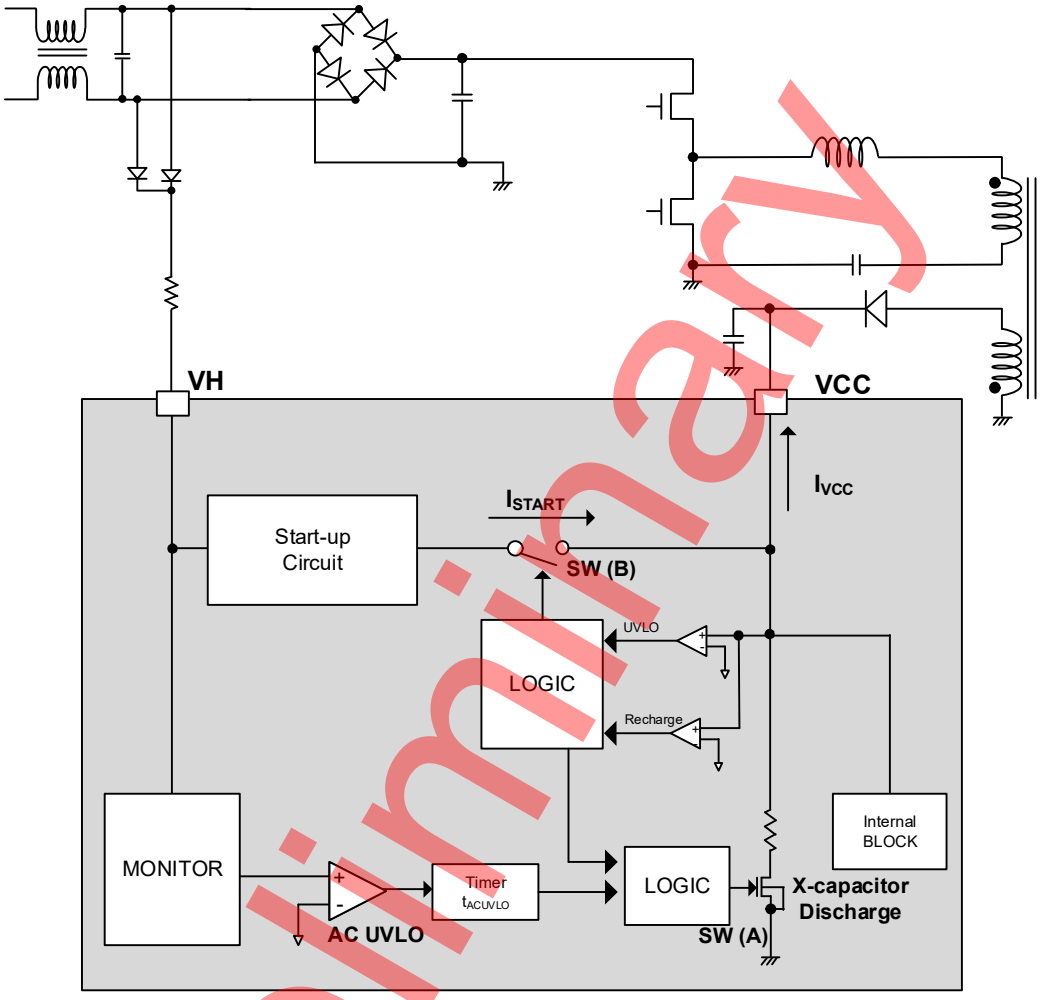
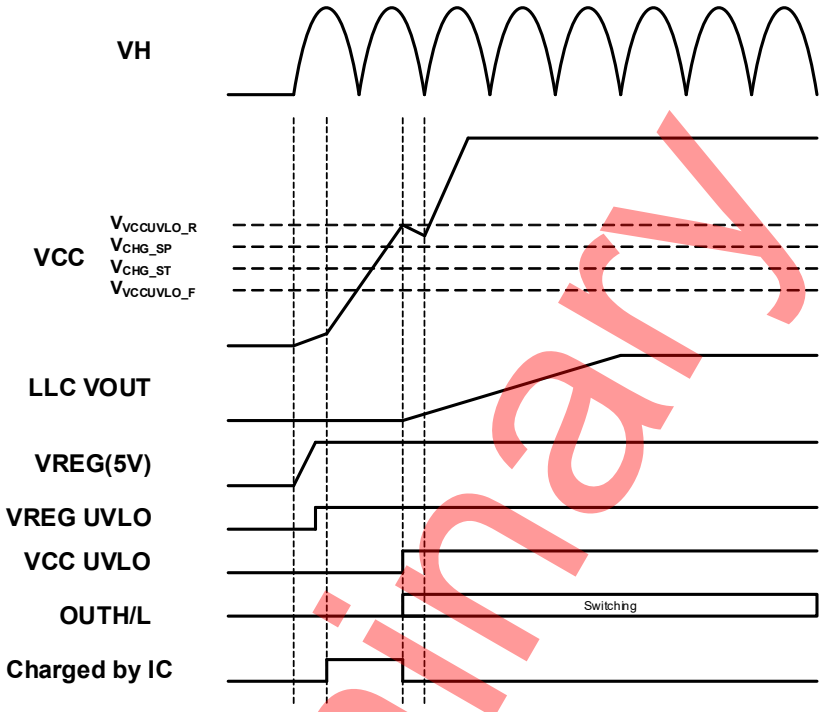


Figure 7. Configuration of HV Startup Circuit

Function Explanation – continued

High Voltage Startup
The IC has built-in starter circuit that withstands 650V.
At startup, $V_{VCCUVLO\_R}$ < VCC, the IC releases the inside UVLO and ON the inside regulator.



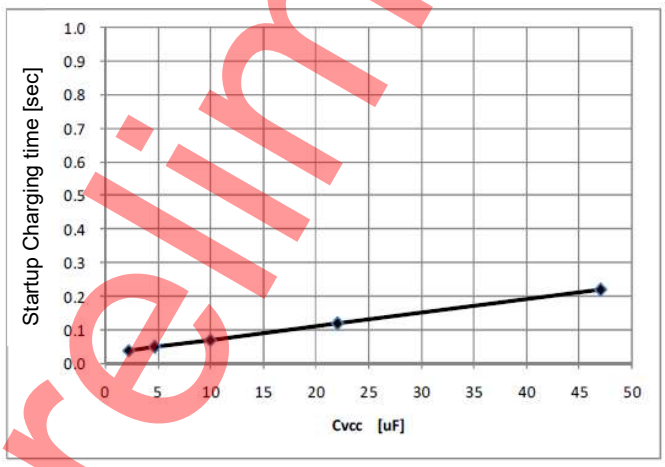


Figure 8. Startup Charging Time

Function Explanation – continued

VCC recharge function

If the VCC pin voltage drops to less than V_{CHG_ST} after once the VCC pin becomes more than $V_{VCCUVLO\_R}$ and the IC starts to operate, the VCC recharge function operates. At this time, the VCC pin is recharged from the VH pin by the start-up circuit. After charging the VCC pin, charging is terminated when the VCC pin rises to V_{CHG_SP}. This operation is shown in the figure below.

Figure 9. VCC Startup Charging Operation shows VCC recharge function when OUTH/L switching stops in case of brown out or fault state.

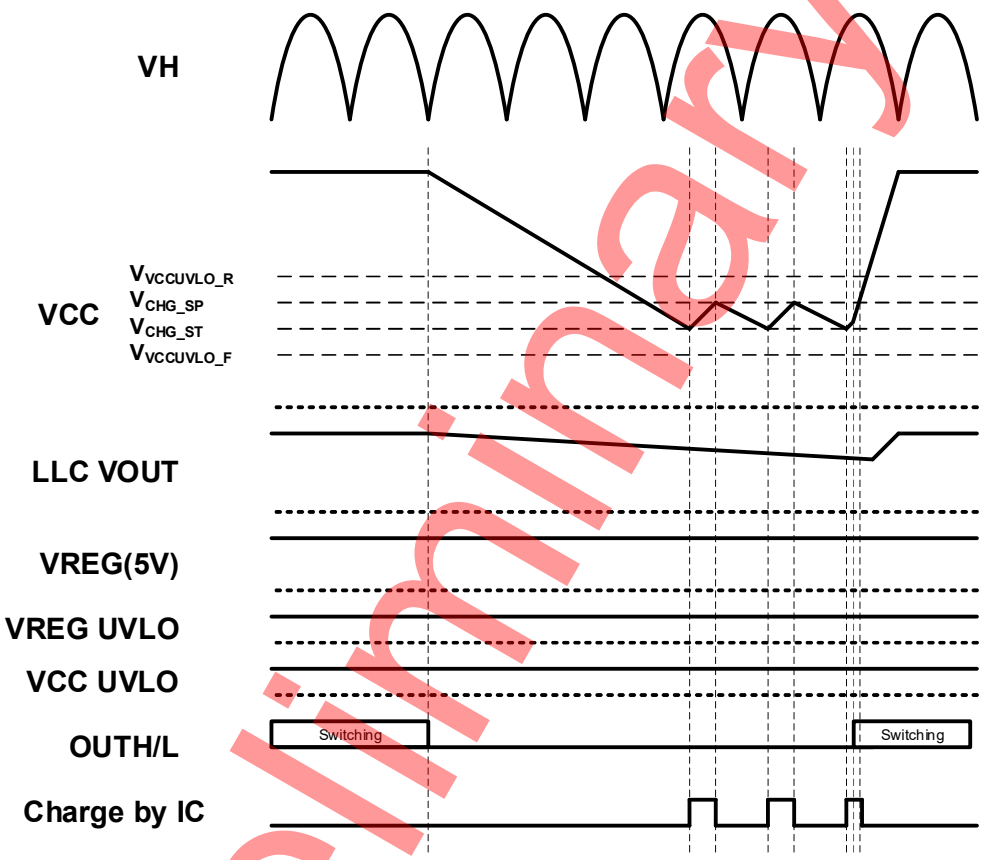


Figure 9. VCC Startup Charging Operation

Function Explanation – continued

X2 Cap Discharge Function (**optional**)

When the AC voltage is not detected longer than t_{ACUVLO} (such as the plug is pulled out), X capacitor discharge function starts to operate. X capacitor is discharged to GND through start-up circuit.

The timing chart of the X capacitor discharge operation is shown below.

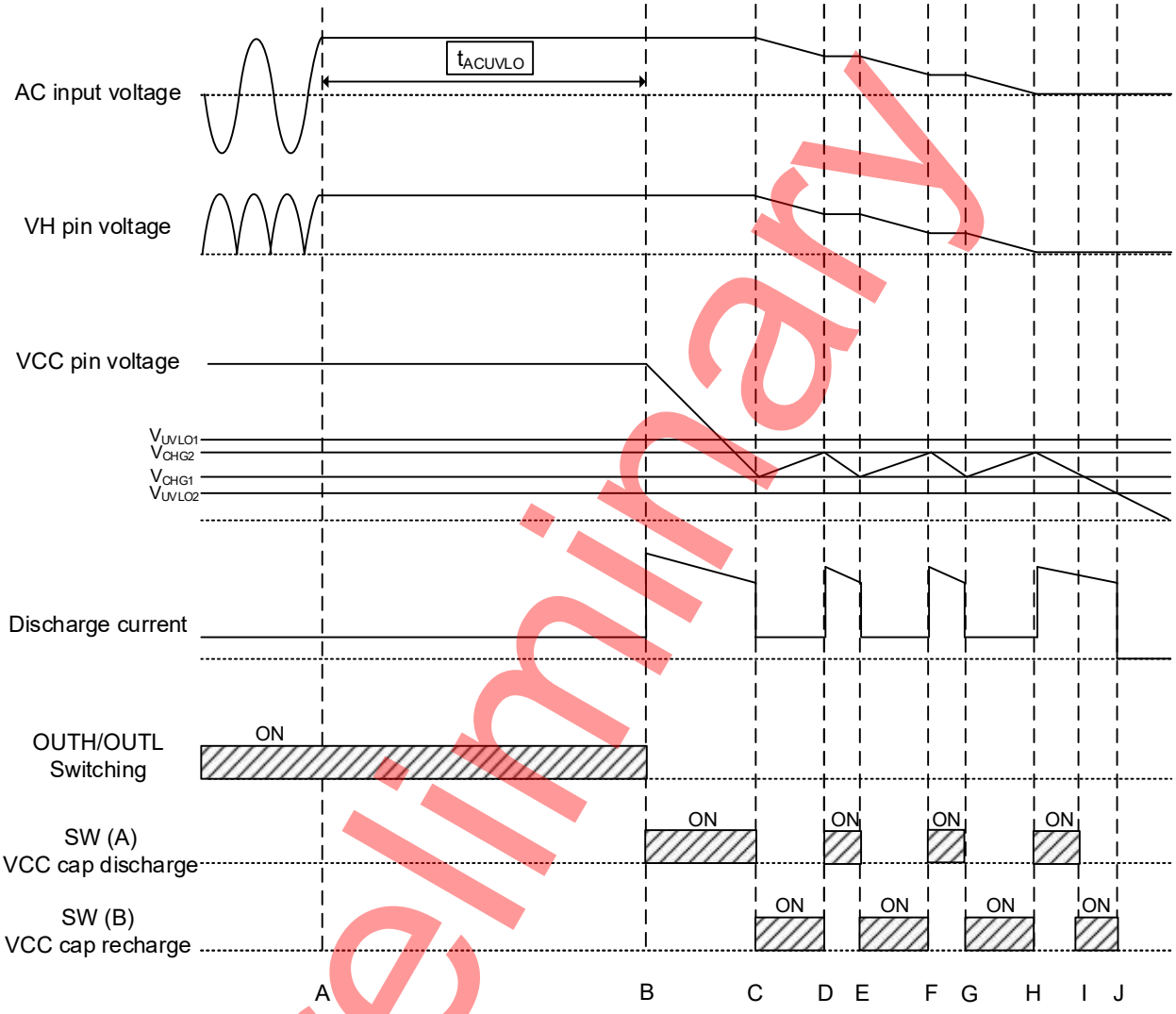


Figure 10. X2 Cap Discharge

Function Explanation – continued

4. Soft start function

SS_TIMER is soft start period.

SS_TIMER (ms)	23

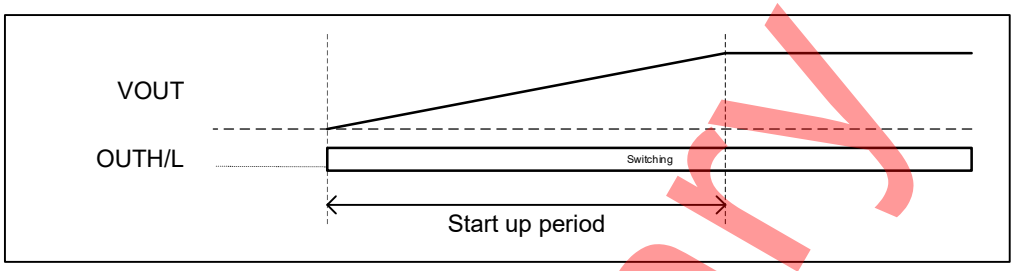


Figure 11. Start Up Period

Function Explanation – continued

5. Resonant tank stabilization at startup

At startup, switching is skipped when CS voltage exceeds Vcs_st. By this, resonant tank can quickly stabilize and reduce the number of hard switching.

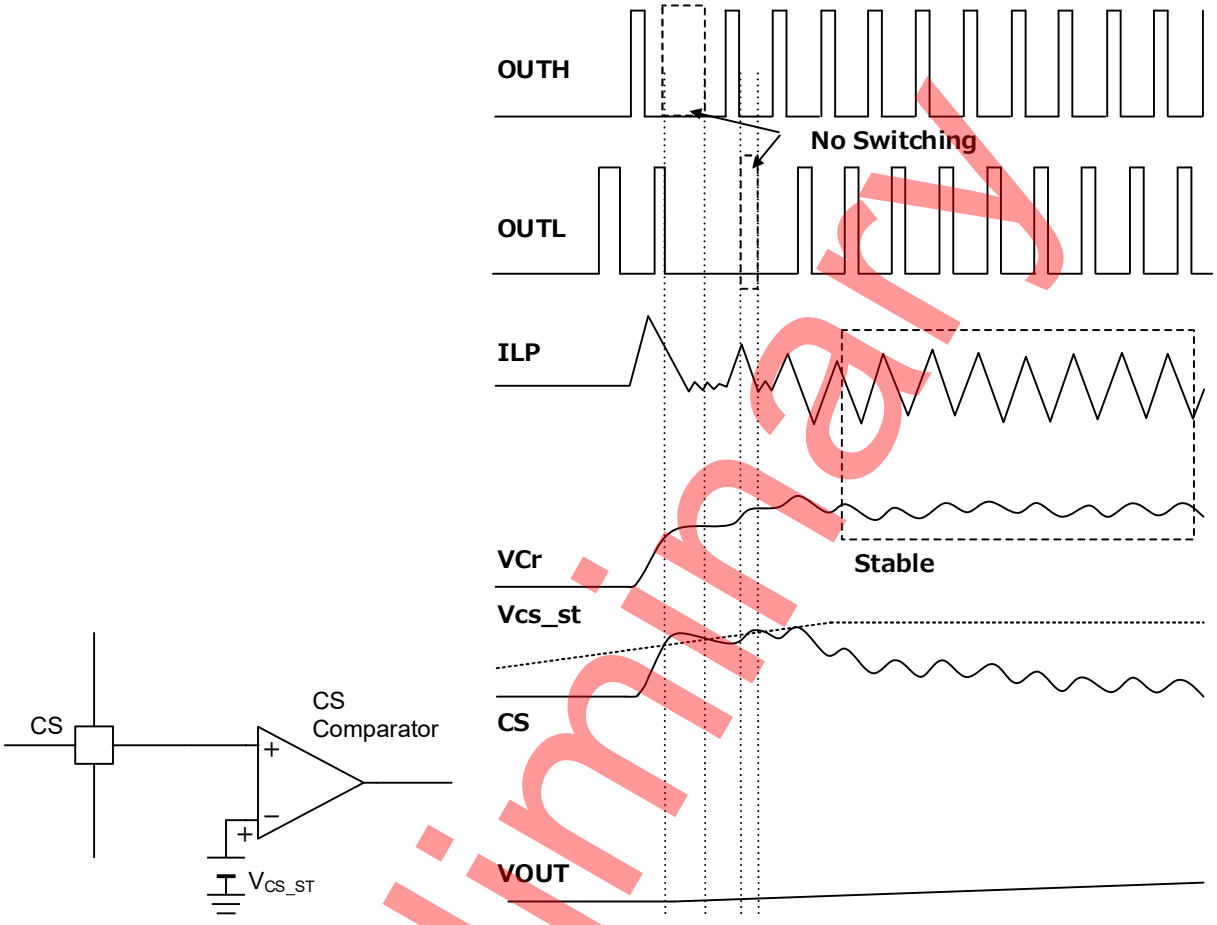


Figure 12.Startup Waveform for Fast Resonant Tank Stabilization

Also, First OUTL period is set 2us (Typ) in order to charge bootstrap capacitor.

The internal CS is pulled down at the start of switching when the CS voltage cannot reflect the current information. The pull-down period (t_{CS_PD}) is CS_PD_STRT_CYC.

CS_PD_STRT_CYC (Number of switching cycles)	16

Function Explanation – continued

6. Limiting SW frequency

FREQ_MAX defines the maximum switching frequency, which corresponds to the minimum OUTH/OUTL on time.

FREQ_MAX (kHz)	1500

FREQ_MIN defines the minimum switching frequency, which corresponds to the maximum OUTH/OUTL on time.

FREQ_MIN (kHz)	300

7. Output ripple cancelation function (**optional**)

Line Feed Forward (LFF) system is implemented in the controller to compensate for Bulk voltage variation.
The LFF signal that is apply to internal FB voltage is VS pin voltage proportional.
The different input voltage sensed by VS pin creates change on internal FB signal.

Function Explanation – continued

8. Burst Mode Operation at Light Load

There are 3 burst optional modes.

Quiet burst mode (**optional**)
In burst mode, the burst frequency does not fall below 25(TBD) KHz.

High efficiency burst mode
In this burst mode, the burst frequency drops below 25 KHz.

High efficiency quiet burst mode (**optional**)
In this burst mode, the burst frequency falls below 25 KHz.
However, the noise is minimized through a proprietary method.

Off burst mode (**optional**)
There is no burst mode behavior.

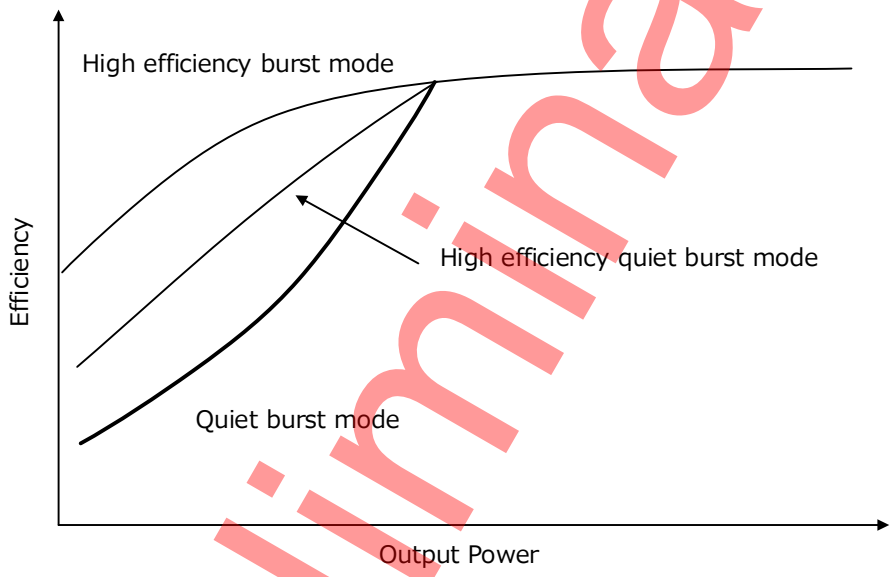


Figure 13. 3 burst modes

Function Explanation – continued

Quiet burst mode (**optional**)

After FB reaches below $V_{FB\_BURST\_F}$, the IC enters burst mode and stops switching.
In the quiet burst mode, the IC exits burst mode after FB exceeds VFB_BURST_R, or when the OUTH/L skipping period reaches 40(TBD) us. It then restarts switching from OUTL on, and the on-time period is defined by FREQ_MAX.
In quiet burst mode, PFCOFF pin is always low.

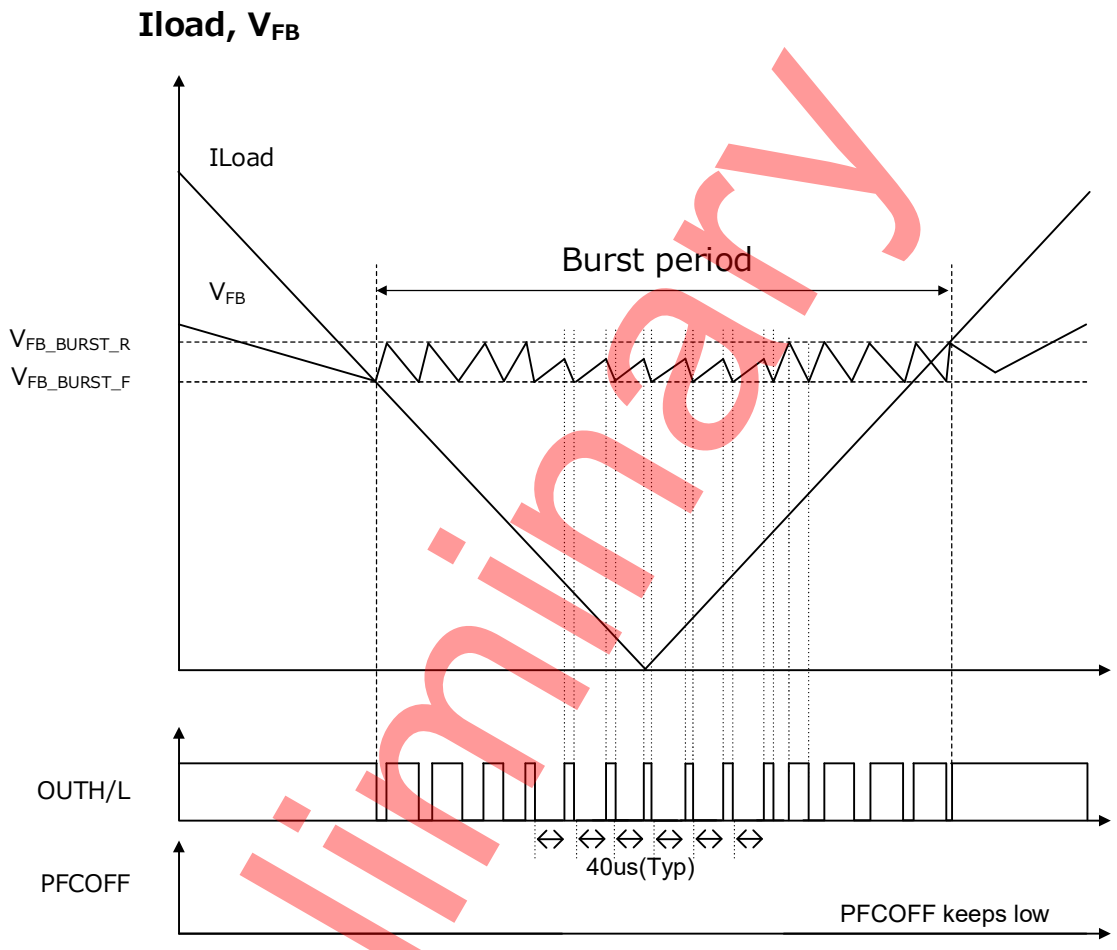


Figure 14. Light Load Operation

Function Explanation – continued

High efficiency burst mode

After FB reaches below $V_{FB\_BURST\_F}$, the IC enters burst mode and stops switching.
After FB exceeds $V_{FB\_BURST\_R}$, the IC exits burst mode and restarts switching from OUTL on and the on time period is defined by FREQ_MAX.

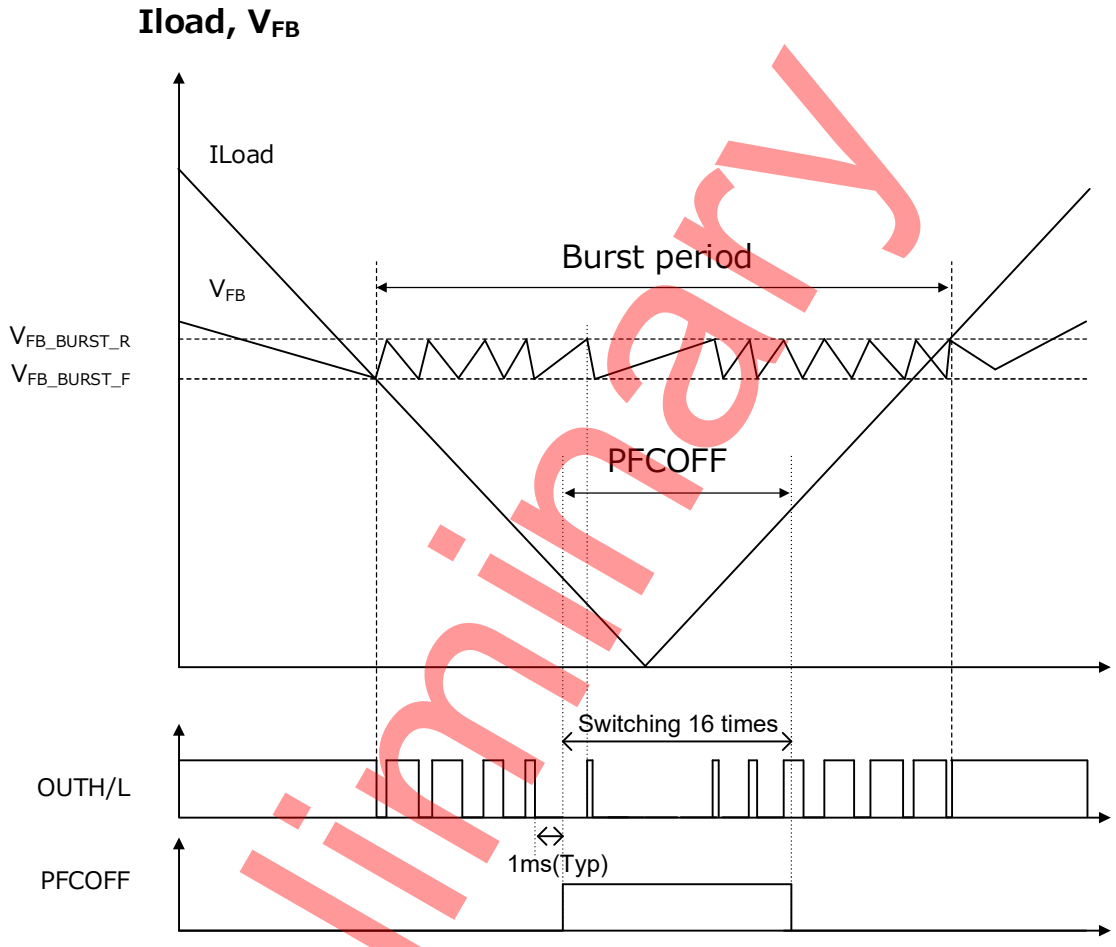


Figure 15. Light Load Operation

High efficiency quiet burst mode (**optional**)
In high efficiency quiet burst mode, $V_{FB\_BURST\_F}$ is not a fixed value.
After FB exceeds $V_{FB\_BURST\_R}$, the IC exits burst mode and restarts switching from OUTL on and the on time period is defined by FREQ_MAX.

Function Explanation – continued

9. PFCOFF

When output load is very low, PFCOFF pin goes high, allowing this IC to halt PFC.

[Detect Condition]
1. OUTH/OUTL toggling stopped continuously more than 1ms.

[Release Condition]
1. OUTH/OUTL toggles 16 times
2. Or V_{VS} is lower than $V_{VS\_DROP\_R}$

10. Avoiding the out of resonance condition (**optional**)

Out-of-resonance would occur below f1 frequency.
Operating frequency is set by minimum (f1) and maximum (f2) switching frequency register.

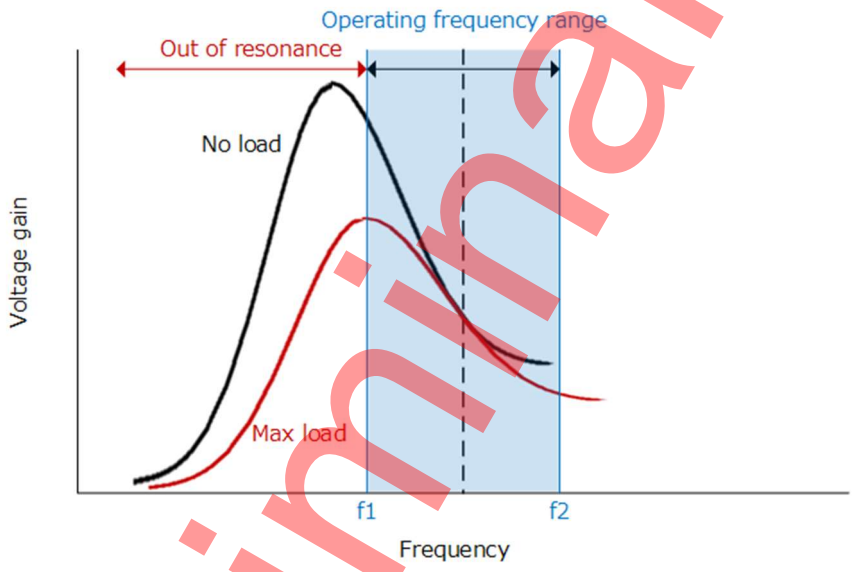


Figure 16. Avoiding the Out of Resonance Condition

Function Explanation – continued

11. Adjustable Dead Time by load current

Load current adjust dead time after soft start. During soft start, dead time is fixed period.

Dead time is adjusted by 3 levels of Load and their thresholds of their voltage are DEADTIME_TH_LM and DEADTIME_TH_MH.
Each levels of Load has its dead time which is DEADTIME_LIGHT, DEADTIME_MID and DEADTIME_HEAVY.

Load current adjusts dead time after soft start. During soft start, dead time is fixed at DEADTIMD_LIGHT.

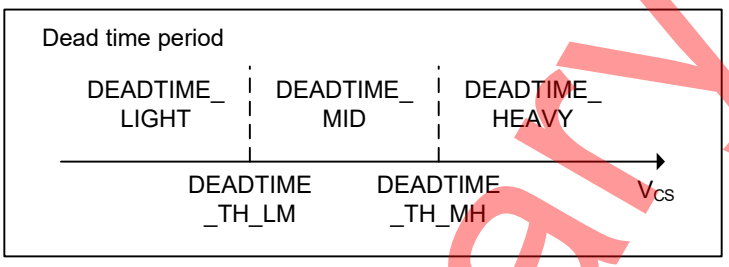


Figure 17. Light Load Operation

DEADTIME_LIGHT	100ns
DEADTIME_MID	80ns
DEADTIME_HEAVY	60ns

DEADTIME_TH_LM	800mV
DEADTIME_TH_LM	1300mV

Function Explanation – continued

Figure 18. Dead Time Adjust Timing shows V_{CS} judgement period and dead time affect timing.
(A) : V_{CS} judgement period is one switching cycle.
(B), (C): Judged dead time affects next switching cycle.

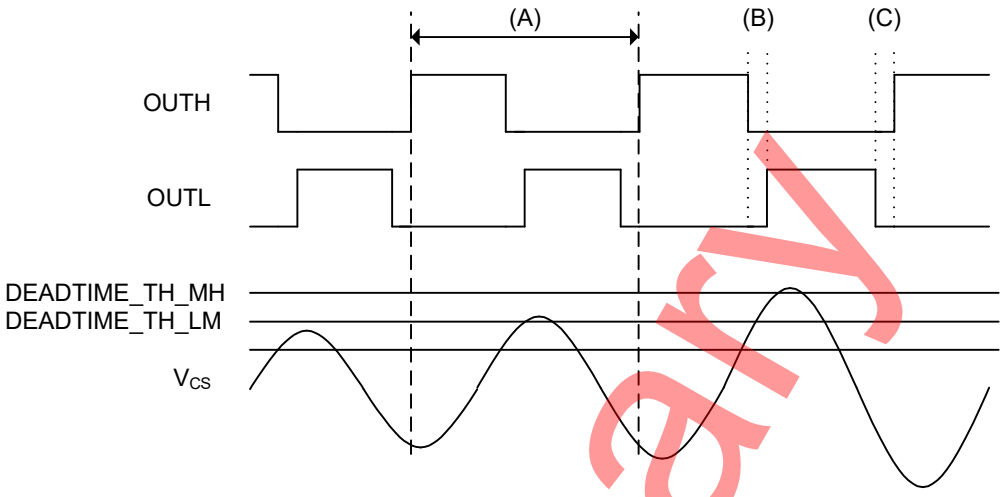


Figure 18. Dead Time Adjust Timing

Function Explanation – continued

12. Line Feed Forward (**optional**)

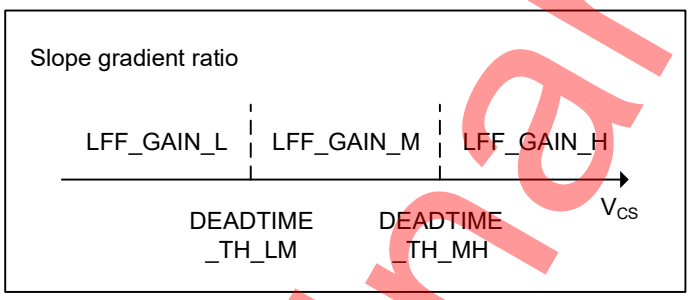
Line feed forward compensate bulk voltage variation.
Bulk voltage variation changes slope inclination.

In LLC topology, Vout gain depends on output load. In general, if load is light, gain is large and vice versa.
And output load affects bulk ripple voltage. In general, if load is light, ripple is smaller and vice versa.
Also, Vout gain depends on transformer.

There are 3 parameters to adjust them.
Slope = (Selected FB_SLOPE) x (LFF_GAIN_L or LFF_GAIN_M or LFF_GAIN_H)

LFF_GAIN_L, LFF_GAIN_M and LFF_GAIN_H are coefficients for slope gradient ratio.

V_{CS} and iload have proportional relationship. DEADTIME_TH_LM and DEADTIME_TH_MH classify 3 ranges of output current load. And those classification assign LFF_GAIN_L, LFF_GAIN_M and LFF_GAIN_H.



LFF_GAIN_L	TBD
LFF_GAIN_M	TBD
LFF_GAIN_H	TBD

Function Explanation – continued

13. Latched Protection

Once being in latched protection mode, recovery method is AC plug after AC unplug. When AC line is unplugged, VCC voltage drops and VREG UVLO makes IC reset.
Figure 19. Latched Protection shows a latched protection recovery example caused by OVP.

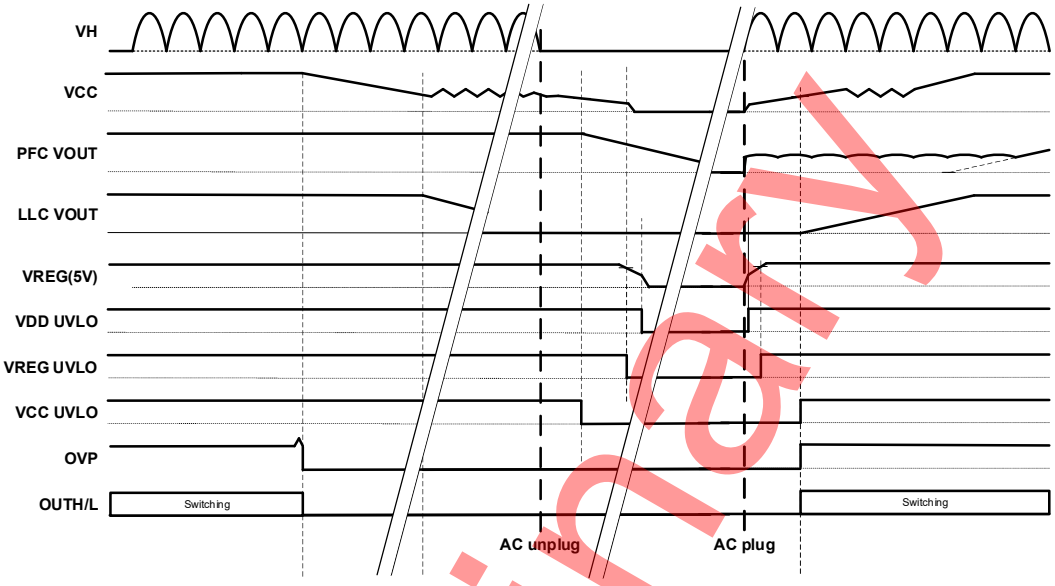


Figure 19. Latched Protection

14. Auto-recovery Protection (**optional**)

In auto-recovery protection mode, after detecting a fault, internal timer counts up until it reaches $t_{AUTOREC}$.
Even if some other faults or same fault would be detected again, its internal timer continues counting up without reset the counter.
When it reaches $t_{AUTOREC}$, this controller restart from soft start.

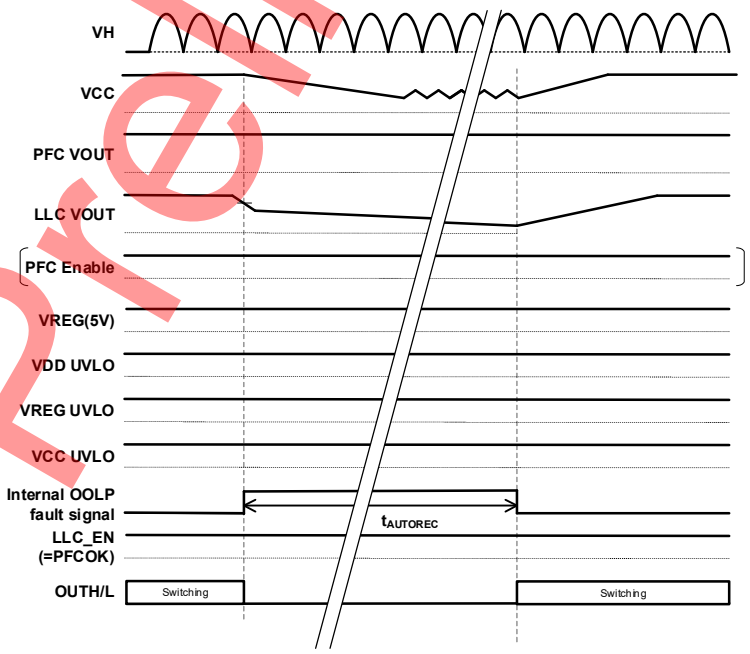


Figure 29. Auto-recovery Protection

Function Explanation – continued

Protections

1. Fault summary

Table X shows protection features, the conditions needed to set or reset the fault, and the action of the IC.for the given fault.

	Protection	Detect Condition	Release Condition	Controller Action	Related PIN
	VCC UVLO	$V_{VCC} < V_{VCCUVLO\_F}$	$V_{VCC} > V_{VCCUVLO\_R}$	- Disable OUTH/OUTL - Disable all analog blocks except LDO, VREF, OSC, VCC charger	VCC
	VREG UVLO	$V_{VREG} < V_{VREGUVLO\_F}$	$V_{VREG} > V_{VREGUVLO\_R}$	- Disable OUTH/OUTL - Disable all analog blocks	VREG
optional	AC UVLO (Line BO)	$V_{VH} < V_{ACUVLO0\_F}$ $V_{VH} < V_{ACUVLO0\_R}$ & t_{ACUVLO} expieres	$V_{VH} > V_{ACUVLO0\_R}$	- Disable OUTH/OUTL - Maintain VCC by VH current source	VH
	VS UVLO (Bulk UVLO)	$V_{VS} < V_{VSUVLO\_F}$	$V_{VS} > V_{VSUVLO\_R}$	- Disable OUTH/OUTL - Maintain VCC by VH current source	VS
	OCP	$V_{CS} > V_{OCP}$ (Cycle by Cycle) $V_{CS} > V_{OCP}$ & Det-count > 32 (OCP_COUNT)	Master Reset (Latch mode) $t_{autorec}$ expires (Auto restart mode)	- Disable OUTH/OUTL - Maintain VCC by VH current source	CS
optional	Over Temperature Protection	$V_{OTP} < V_{OTP\_FAULT}$ & T_{OTP_BLANK} elapses	Master Reset (Latch mode) $t_{autorec}$ expires (Auto restart mode)	- Disable OUTH/OUTL - Maintain VCC by VH current source	OTP
optional	OVP	$V_{OVP} > V_{OVP\_FAULT}$	Master Reset (Latch mode) $t_{autorec}$ expires (Auto restart mode)	- Disable OUTH/OUTL - Maintain VCC by VH current source	OVP
	OLP	$V_{FB} > V_{FBOLP}$ & t_{FBOLP} expieres	Master Reset (Latch mode) $t_{autorec}$ expires (Auto restart mode)	- Disable OUTH/OUTL - Maintain VCC by VH current source	FB
optional	Open Feedback Loop Detection	$V_{FB} > V_{FBOPEN}$ & t_{FBOPEN} expieres	Master Reset (Latch mode) $t_{autorec}$ expires (Auto restart mode)	- Disable OUTH/OUTL - Maintain VCC by VH current source	FB
	VS Open Protection	$V_{VS} > V_{VSOPEN\_R}$ valid only in Startup state	$V_{VS} < V_{VSOPEN\_F}$ valid only in Startup state	- Staying in Startup state - Maintain VCC by VH current source	VS
	CS Open Protection	$V_{CS} > V_{CSOPEN\_R}$ valid only in Startup state	$V_{CS} < V_{CSOPEN\_F}$ valid only in Startup state	- Staying in Startup state - Maintain VCC by VH current source	CS
	Thermal Shutdown Protection	$T_j > T_{TSD\_R}$	$T_j > T_{TSD\_F}$	- Disable OUTH/OUTL - Maintain VCC by VH current source	internal

Protections – continued

1. VCC UVLO

VCC UVLO detects when V_{VCC} is lower than $V_{VCCUVLO\_F}$.
VCC UVLO releases when V_{VCC} exceeds $V_{VCCUVLO\_R}$.

In the case of VCC UVLO, the states goes to “Standby”, and OUTH/OUTL are disabled.
And disabling all analog blocks except VREF, OSC and VCC charger.

2. VREG UVLO

VREG UVLO detects when V_{VREG} is lower than $V_{VREGUVLO\_F}$.
VREG UVLO releases when V_{VREG} exceeds $V_{VREGUVLO\_R}$.

In the case of VREG UVLO, the states goes to “Standby”, and OUTH/OUTL are disabled.
And disabling all analog blocks except VCC charger.

3. AC UVLO (**optional**)

To detect AC unplug and AC UVLO, there are 7 comparator for VH pin. ACCMP_0, ACCMP_1, ACCMP_2, ACCMP_3, ACCMP_4, ACCMP_5, ACCMP_6 are those comparator outputs. AC_STP_CNT is a counter and it counts up to t_{ACUVLO} period. AC_STP_CNT resets at any rising edge of ACCMP. AC_UVLO (AC unplug) is detected when the AC_STP_CNT reaches t_{ACUVLO}.

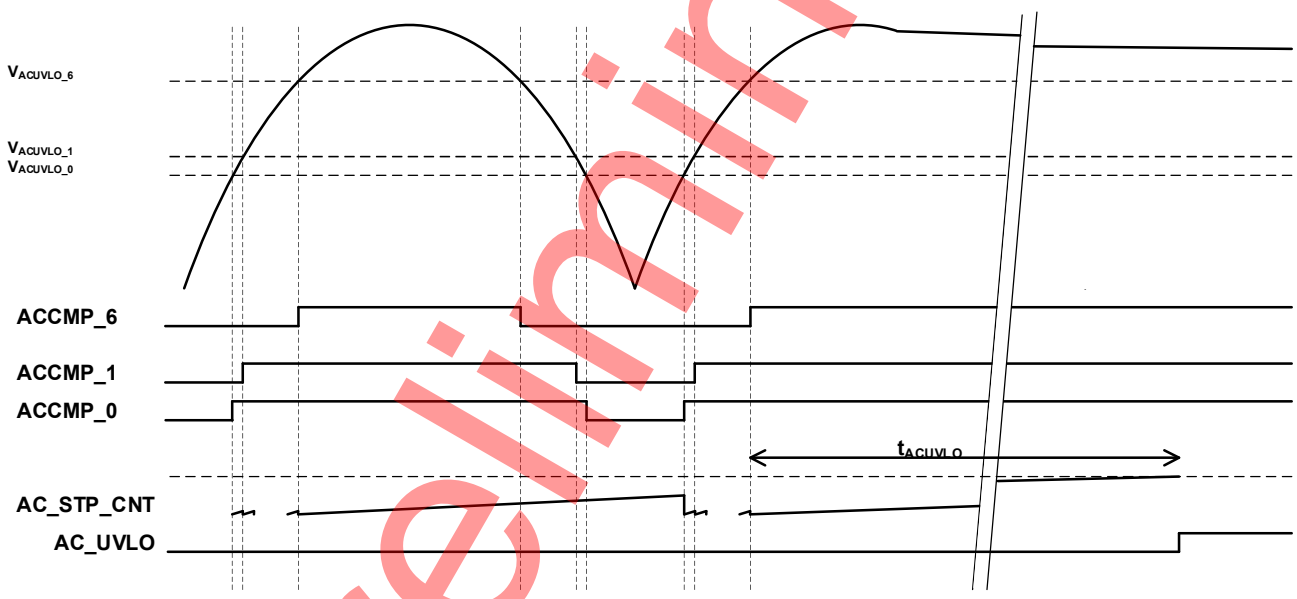


Figure 3020. AC Unplug

Protections – continued

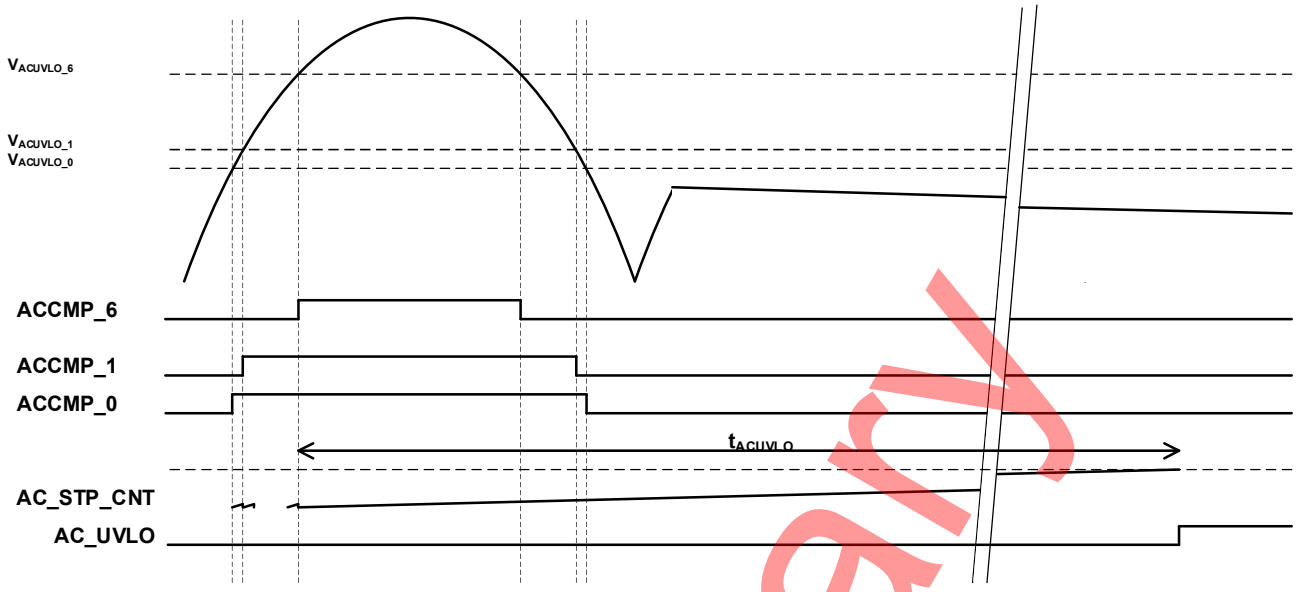


Figure 21. AC UVLO

If AC UVLO is detected, the system transitions to the 'Startup' state, disabling OUTH/OUTL. Additionally, the X capacitor discharge function is activated until detecting rising edge of ACCMP.

AC UVLO detection timer (t_{ACUVLO}) is defined by AC_UVLO_TIMER.

AC_UVLO_TIMER (ms)	TBD

4. VS UVLO

VS UVLO detects when V_{VS} is lower than V_{VSUVLO_F}.
VS UVLO releases when V_{VS} exceeds V_{VSUVLO_R}.

If VS UVLO detection keeps more than t_{VSUVLO}, the states goes to "Startup", and OUTH/OUTL are disabled.
OUTH/OUTL restarts toggling if V_{VS} exceeds V_{VSUVLO_R}.

VS UVLO detection timer (t_{VSUVLO}) is defined by VS_UVLO_TIMER.

VS_UVLO_TIMER (t_{VSUVLO})	128ms

Protections – continued

5. OCP (Protection)

OCP detection from the CS terminal is much faster than from the FB terminal. This helps to reduce stress on power stage components.

The CS pin signal is monitored by the dedicated CS fault comparator.

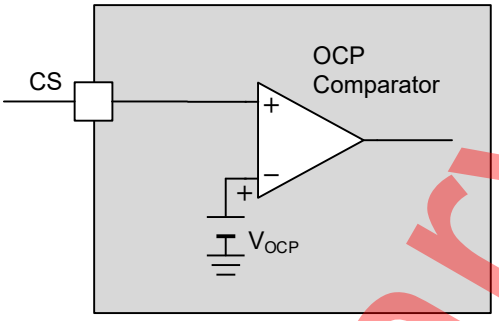


Figure 32. OCP

OCP checking occurs every switching cycle. When the OCP counter (ocp_det_cnt) reaches or exceeds the defined threshold by OCP_COUNT, OUTH/OUTL is disabled. The OCP counter (ocp_det_cnt) can be reset by the ocp_undet_cnt counter when ocp_undet_cnt equals the defined threshold by OCP_COUNT. ocp_undet_cnt can be reset if OCP detection occurs.

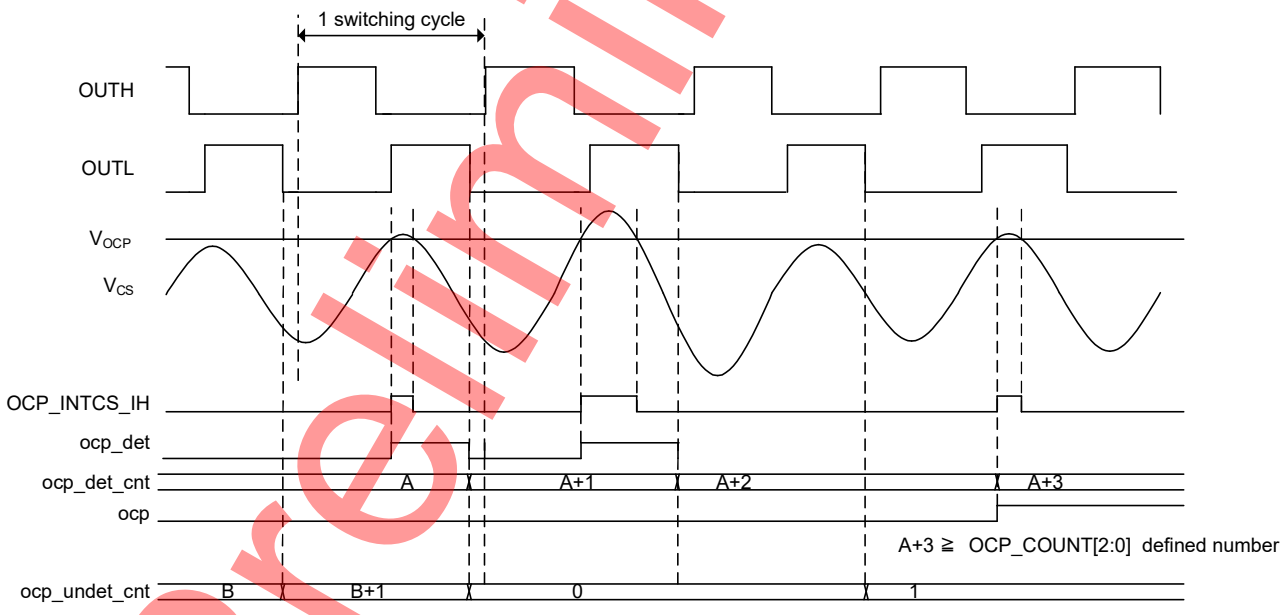


Figure 33. OCP Timing Chart

OCP_COUNT	48

Protections – continued

6. OCP (pulse-by-pulse)

Detect OCP at CS voltage threshold and OUTH is turned-OFF.
OUTL is turned-ON for the time OUTH was ON.
When OCP is detected, the frequency is increased, Gain is lowered, and output current is reduced.
This operation is repeated every cycle.

When OCP is detected at the CS voltage threshold (V_{OCP}), OUTH is turned OFF. Additionally, OUTL is turned ON for the duration that OUTH was previously ON. Upon detecting OCP, the frequency is increased, gain is lowered, and output current is reduced. This entire operation is repeated every cycle.

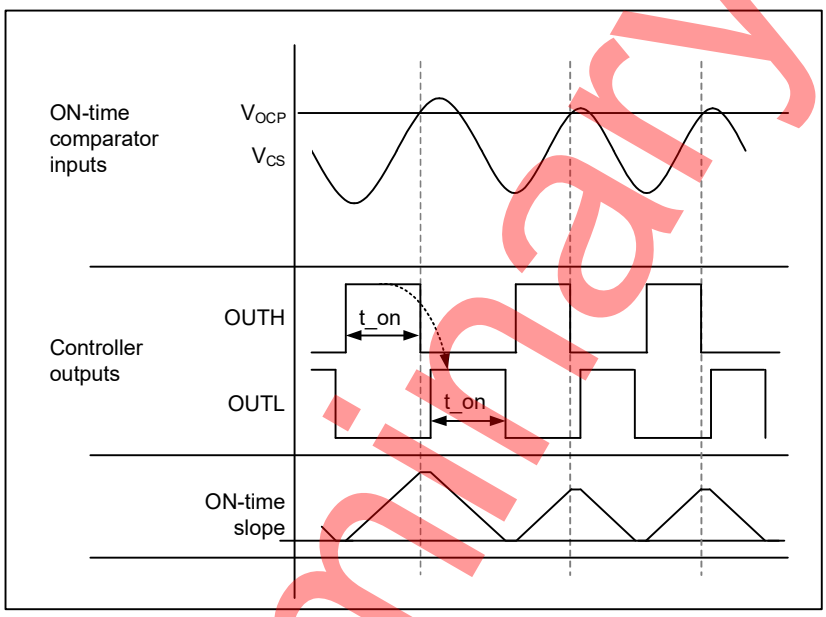


Figure 34. OCP (pulse-by-pulse)

7. OVP (Over Voltage Protection) (**optional**)

OVP detects when V_{OVP} is lower than V_{OVP_F}.
OVP releases when V_{OVP} exceeds V_{OVPR}.

In the case of OVP, the states goes to “Standby”, and OUTH/OUTL are disabled.
Maintain VCC by VH current source

When the OVP terminal is not in use, connect GND through a pull-down resistor.
The figure below provides an example of how to implement VCC OVP."

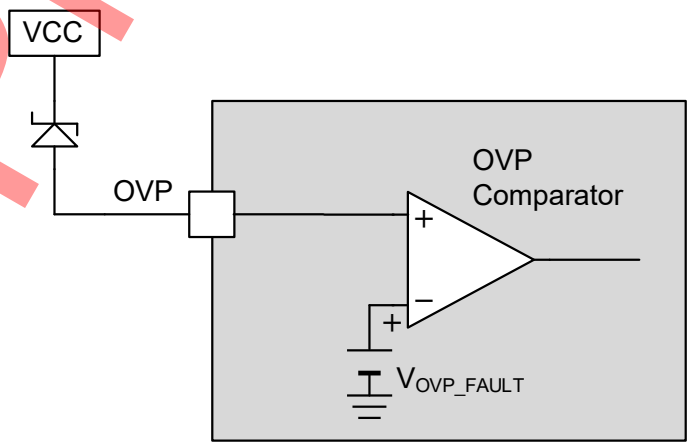


Figure 35. OVP (Over Voltage Protection)

Protections – continued

8. OLP (Overload Protection)

The overload protection is implemented by monitoring the voltage of the FB pin. When the FB pin voltage reaches the V_{FB_OLP} level, the FB OLP comparator is triggered, and the FB OLP timer is activated. Once the FB OLP condition is resolved, the FB OLP timer is reset. Upon confirmation of the FB OLP condition by the FB OLP timer (t_{FB_OLP}), the controller disables OUTH/OUTL and enters protection mode.

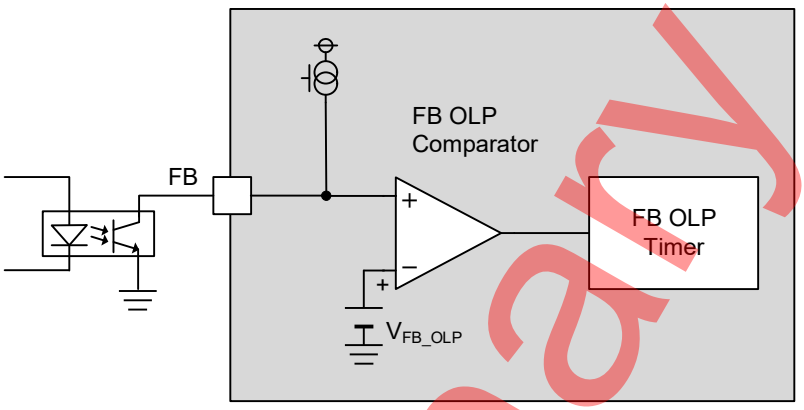


Figure 36. Overload Protection

9. FB OPEN (**optional**)

The FB OPEN protection is implemented by monitoring the voltage of the FB pin. When the FB pin voltage reaches the V_{FB_OPEN} level, the FB OPEN comparator is triggered, and the FB OPEN timer is activated. Once the FB OPEN condition is resolved, the FB OPEN timer is reset. Upon confirmation of the FB OPEN condition by the FB OPEN timer (t_{FB_OEPN}), the controller disables OUTH/OUTL and enters protection mode.

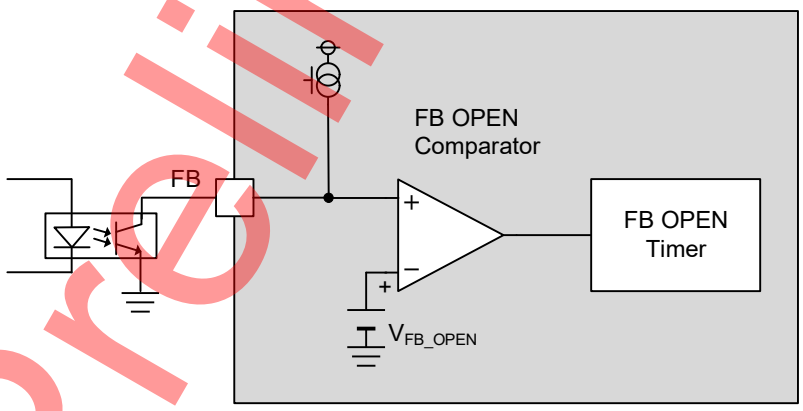


Figure 37. FB OPEN Protection

Protections – continued

10. OTP (Over Temperature Protection) (**optional**)

OTP detects when V_{OTP} is below $V_{OVP\_FAULT\_F}$.
OTP releases when V_{OTP} exceeds $V_{OTP\_FAULT\_R}$.

In the case of OTP, the states goes to “Standby”, and OUTH/OUTL are disabled.
Maintain VCC by VH current source

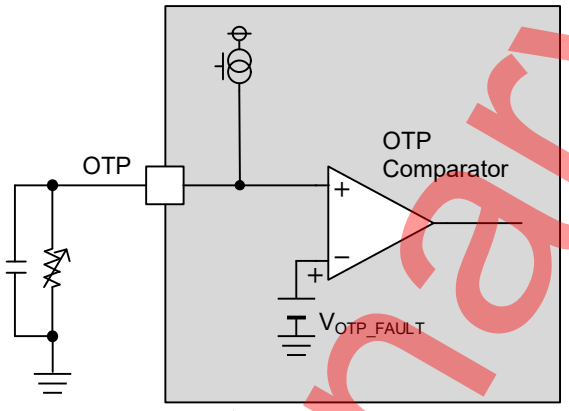


Figure 38. OTP (Over Temperature Protection)

11. VS Open Protection

VS open protection detects when V_{VS} exceeds V_{VSOPEN_R}.
VS open protection releases when V_{VS} is lower than V_{VSOPEN_F}.

VS Open Protection is assessed only before OUTH/OUTL starts toggling. If VS Open Protection is detected, OUTH/OUTL toggling will not start.

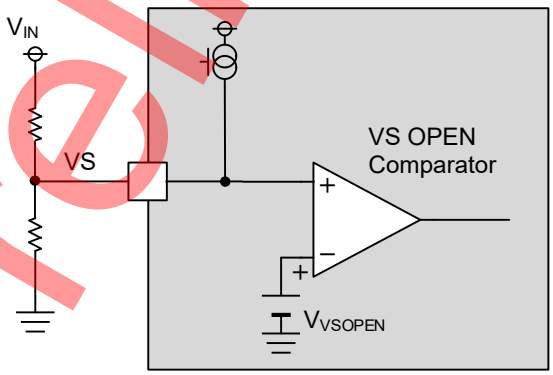


Figure 39. VS Open Protection

Protections – continued

12. CS Open Protection

CS open protection detects when V_{CS} exceeds V_{CSOPEN_R}.
CS open protection releases when V_{CS} is lower than V_{CSOPEN_F}.

CS Open Protection is assessed only before OUTH/OUTL starts toggling. If CS Open Protection is detected, OUTH/OUTL toggling will not start.

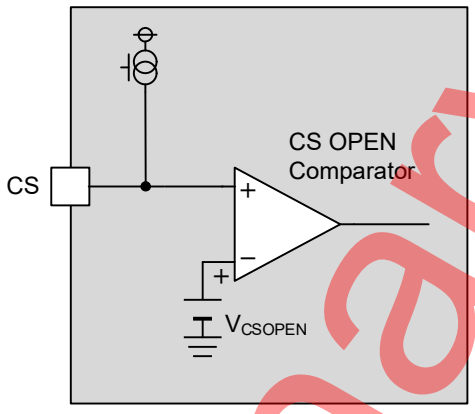


Figure 40. CS Open Protection

13. Internal TSD

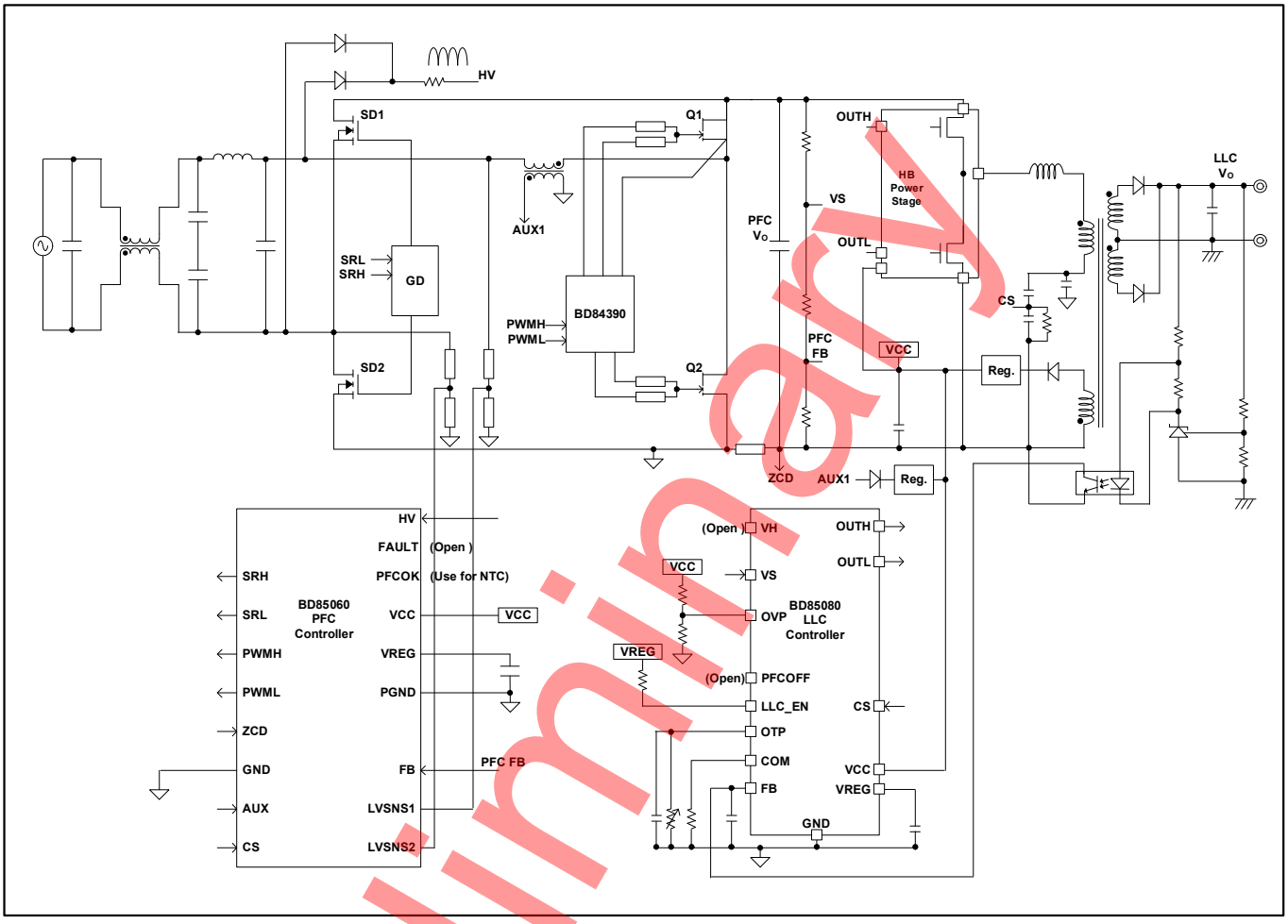
Internal TSD detects when Junction temperature (Tj) exceeds TSD detection temperature (T_{TSD_R}).
Internal TSD releases when Tj falls below the TSD release temperature (T_{TSD_F})

In the case of internal TSD, the states goes to “Standby”, and OUTH/OUTL are disabled.
And disabling all analog blocks except VCC charger by VH current source.

Application Examples

1. Typical application example without line signal for LLC controller

VCC is controlled from PFC controller by HV startup function. LLC starts up by releasing VS UVLO.



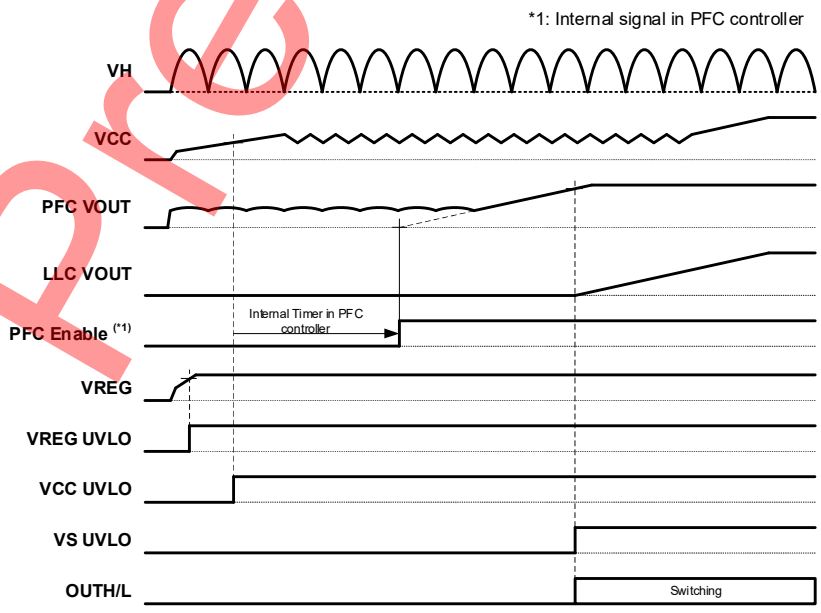


Figure 41. Startup Sequence

Application Examples - continued

Shutdown by VS UVLO
This is a LLC shutdown example caused by AC unplug. LLC is shut down by detecting VS UVLO.

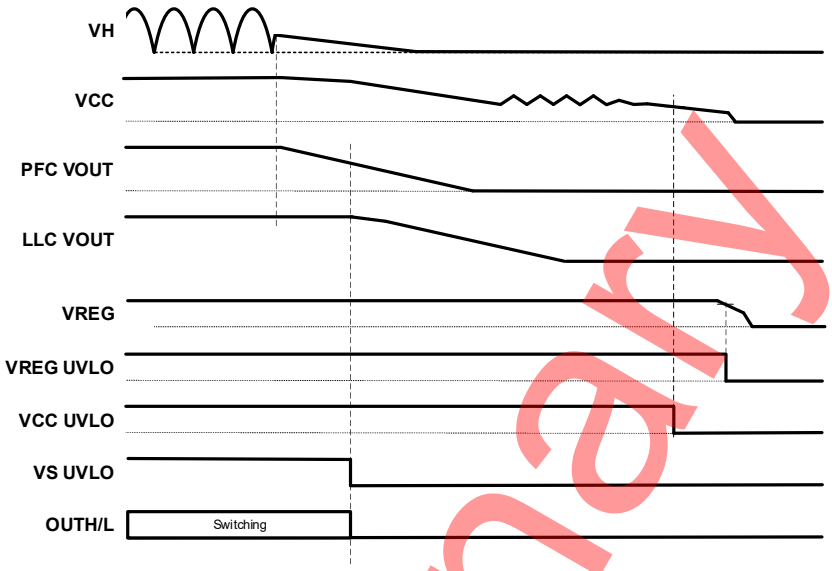


Figure 42. Shutdown by VS_UVLO

Where VO is the output voltage, and VIN_DC_NOM is the typical DC input voltage.

I/O Equivalent Circuits

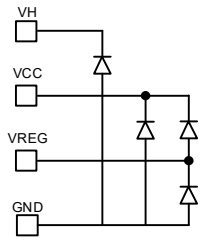
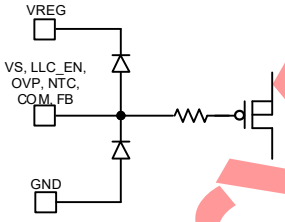
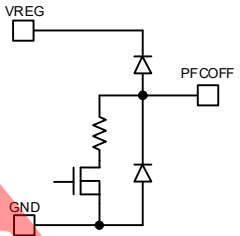
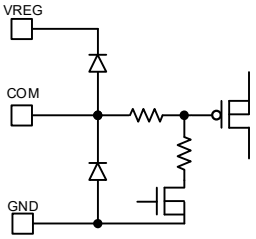
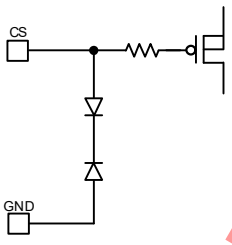
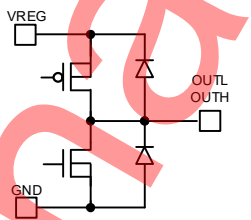
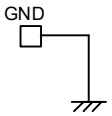
1, 18, 20	VH, VREG, VCC	2, 3, 4, 13, 17, 19	N.C.	5, 7, 8, 9, 11	VS, LLC_EN, OVP, NTC, FB	6	PFCOFF
		–					
10	COM	12	CS	14, 16	OUTL, OUTH	15	GND
							

Figure 4722. I/O Equivalent Circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

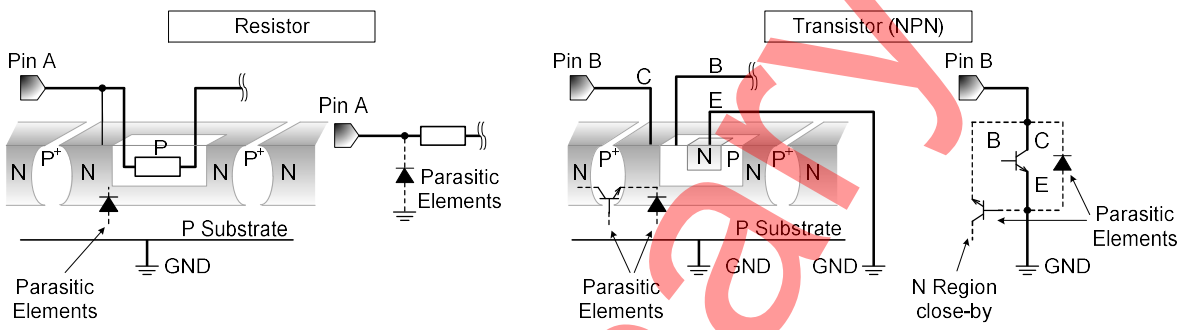


Figure 23. Example of Monolithic IC Structure

11. Ceramic Capacitor

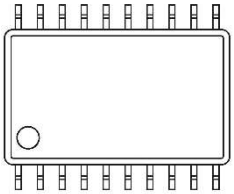
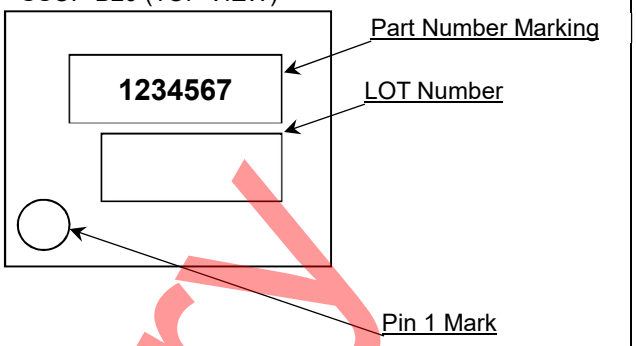
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

SSOP-B20		
6.5 mm x 6.4 mm x 1.45 mm		
	SSOP-B20 (TOP VIEW) 	SSOP-B20 (TOP VIEW) 

Revision History

Date	Revision	Changes
21.Aug.2023	001	New Release
17.Jan.2024	005	Update
22.Feb.2024	006	Update
6.Dec.2024	007	Update

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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