Boost LED Driver

2ch Constant Current/Voltage Controller with SPI and I2C Interface for Automotive

BD18354MUF-M

General Description

BD18354MUF-M is a 2ch Constant-Current and Voltage Controller. High side current detection amplifier is built in. PWM dimming duty can be freely set with built-in PWM generation circuit. PWM dimming realizes by driving an external P-ch FET. The BD18354MUF-M can support individual 10-bit analog dimming and 10-bit PWM dimming for LED current by programing the 10-bit register via SPI. BD18354MUF-M can be started up by reading data from the EEPROM by setting the MODE pin without SPI communication.

The BD18354MUF-M will support LIMP-HOME mode and STAND-ALONE mode if SPI communication has an error. In the LIMP-HOME mode, it operates by loading the register settings stored in the connected EEPROM. In the STAND-ALONE mode, individual LED current can be set by the external pins and can keep LED current sourcing during applying input power without SPI communication.

Features

- AEC-Q100 Qualified *(Note 1)*
- Functional Safety Supportive Automotive Products
- PWM Dimming Signal Generator
- Analog Dimming
- Thermal Shutdown (TSD)
- Thermal Sensor Reading
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I2C)
- LIMP-HOME Mode
- Outputs Abnormal LED Status (FAULT_Bx)
- Spread Spectrum Frequency Modulation

(Note 1) Grade1

Key Specifications

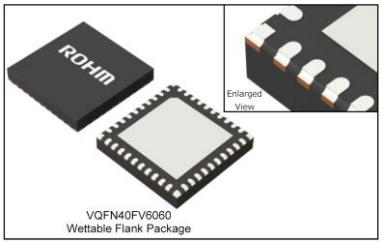
- Input Voltage Range: 5.0 V to 70.0 V
- Maximum Output Voltage: 70 V
- LED Average Current Accuracy: ±3 %
- 10-bit Analog Dimming Range 5 % to 100 %
- Programmable Switching Frequency Range: 100 kHz to 2.5 MHz
- Junction Temperature Range: -40 °C to +150 °C

Applications

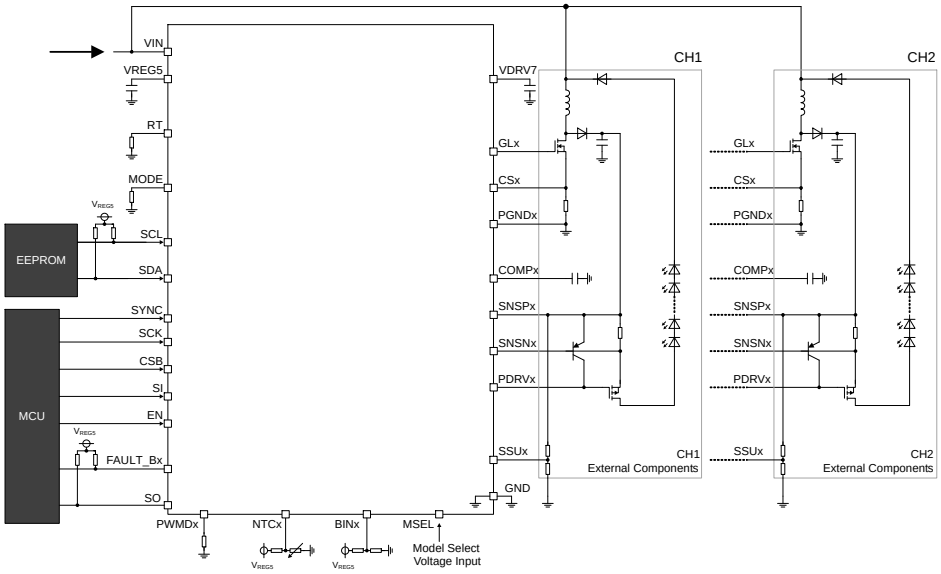
- Automotive Exterior Lamps
  Rear, Turn, DRL/Position, Fog, High/Low Beam etc.

Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN40FV6060	6.0 mm x 6.0 mm x 1.0 mm



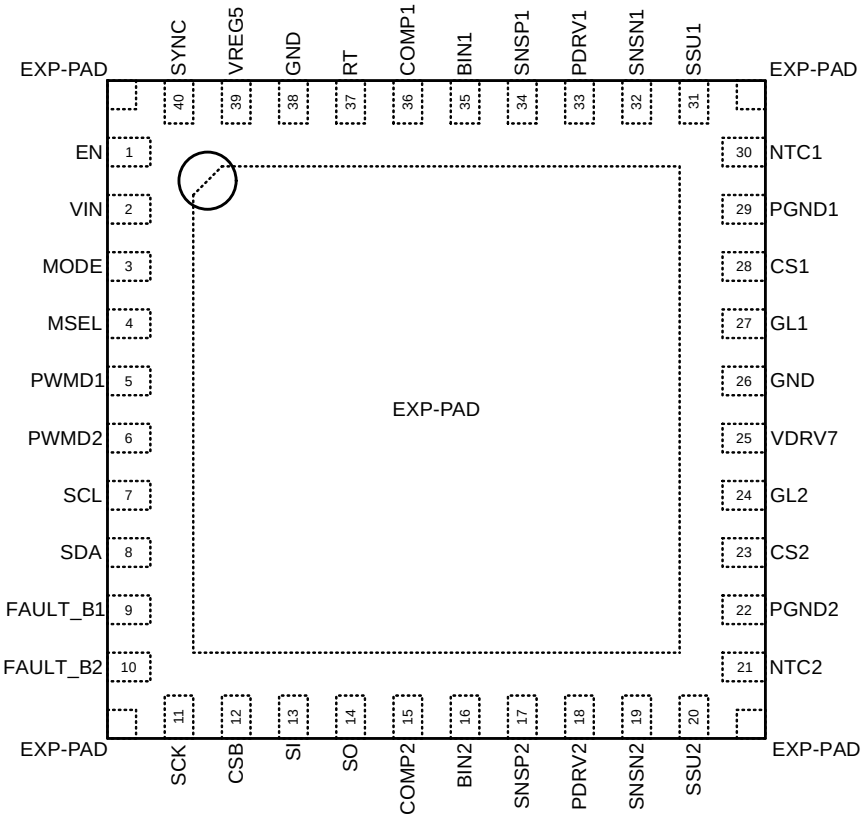
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

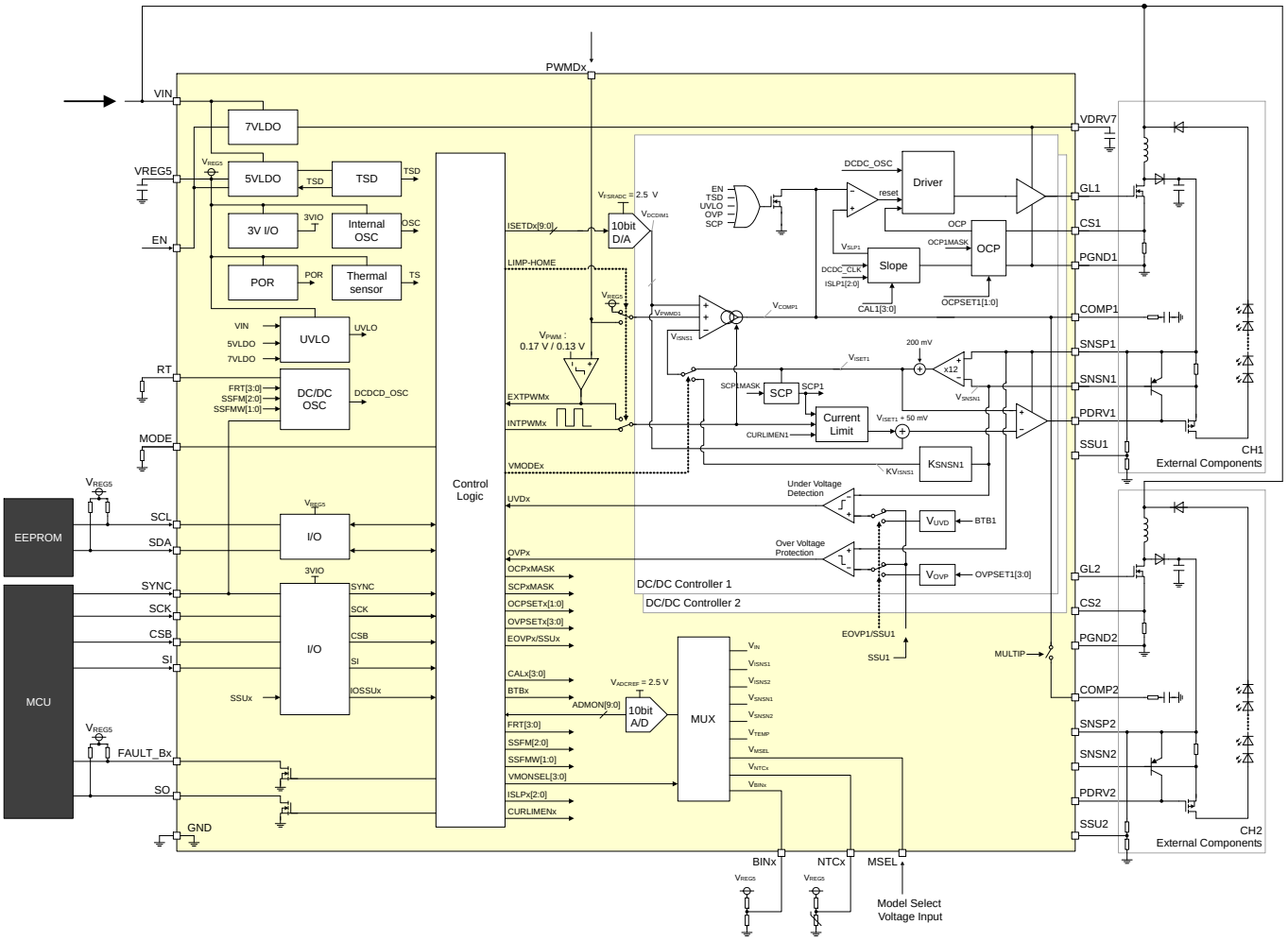
VQFN40FV6060
(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	EN	Enable input
2	VIN	Power supply input
3	MODE	MODE select input (L: normal mode, H: EEPROM read mode)
4	MSEL	EEPROM setting model select voltage input
5	PWMD1	CH1 LED current setting in the STAND-ALONE mode / PWM dimming
6	PWMD2	CH2 LED current setting in the STAND-ALONE mode / PWM dimming
7	SCL	Serial clock output
8	SDA	Serial data input / output
9	FAULT_B1	CH1 open drain output for fault flag
10	FAULT_B2	CH2 open drain output for fault flag
11	SCK	Serial clock input for SPI
12	CSB	Chip select input for SPI
13	SI	Serial data input for SPI
14	SO	Serial data open drain output for SPI
15	COMP2	Connecting compensation capacitor CH2
16	BIN2	Connect BIN resistor for CH2 LED BINNING
17	SNSP2	CH2 current sense input +
18	PDRV2	P-ch FET gate drive for CH2 PWM dimming and protection
19	SNSN2	CH2 current sense input -
20	SSU2	CH2 slow startup voltage input / output voltage divider input
21	NTC2	Connect NTC Thermistor to set CH2 temperature derating
22	PGND2	CH2 power GND
23	CS2	CH2 Inductor current sense input
24	GL2	CH2 output for N-ch FET gate drive
25	VDRV7	Reference voltage output for FET gate drive
26	GND	GND (connect capacitor for VDRV7)
27	GL1	CH1 output for N-ch FET gate drive
28	CS1	CH1 inductor current sense input
29	PGND1	CH1 power GND
30	NTC1	Connect NTC Thermistor to set CH1 temperature derating
31	SSU1	CH1 slow startup voltage input / output voltage divider input
32	SNSN1	CH1 current sense input -
33	PDRV1	P-ch FET gate drive for CH1 PWM dimming and protection
34	SNSP1	CH1 current sense input +
35	BIN1	Connect BIN resistor for CH1 LED BINNING
36	COMP1	Connecting compensation capacitor CH1
37	RT	Connect resistor to set switching frequency
38	GND	GND
39	VREG5	Internal 5 V regulator output connecting 4.7 μF capacitor
40	SYNC	External synchronization input pin
-	EXP-PAD	Connect EXP-PAD to GND. The center EXP-PAD and the corner EXP-PAD are shorted inside the package.

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Pin Voltage (VIN)	V_{IN}	-0.3 to +72.0	V
MODE, EN Pin Voltage	V_{MODE}, V_{EN}	-0.3 to V_{IN}	V
SNSPx, SNSNx Pin Voltage	V_{SNSPx}, V_{SNSNx}	-0.3 to +72.0	V
SNSPx to SNSNx Pin Voltage	V_{SNSPx_SNSNx}	-0.3 to +0.6	V
NTCx, SSUx, BINx Pin Voltage	V_{NTCx}, V_{SSUx}, V_{BINx}	-0.3 to +72.0 ≤ V_{SNSPx} +7.0	V
PDRVx Pin Voltage	V_{PDRVx}	-0.3 to +72.0 ≤ V_{SNSPx} +0.3	V
SNSPx to PDRVx Pin Voltage	V_{SNSPx_PDRVx}	-0.3 to +10.0	V
VREG5 Pin Voltage	V_{REG5}	-0.3 to +7.0 ≤ V_{IN}+0.3	V
VDRV7 Pin Voltage	V_{DRV7}	-0.3 to +10.0 ≤ V_{IN}+0.3	V
GLx, CSx Pin Voltage	V_{GLx}, V_{CSx}	-0.3 to +10.0 ≤ V_{DRV7}+0.3	V
RT, MSEL, SYNC, PWMDx, COMPx Pin Voltage	V_{RT}, V_{MSEL}, V_{SYNC}, V_{PWMDx}, V_{COMPx}	-0.3 to +7.0 ≤ V_{REG5}+0.3	V
SI, SCK, CSB, SCL, SDA Pin Voltage	V_{SI}, V_{SCK}, V_{CSB}, V_{SCL}, V_{SDA}	-0.3 to +7.0	V
SO, FAULT_Bx Pin Voltage	V_{SO}, V_{FAULT_Bx}	-0.3 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(x = 1, 2)

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
VQFN40FV6060				
Junction to Ambient	θ_{JA}	93.7	32.8	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	7	4	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VIN)*(Note 1)*	V_{IN}	5	13	70	V
Output Voltage (SNSPx)	V_{SNSP}	0	-	70	V
PWM Frequency Input	f_{PWMI}	30	-	2000	Hz
PWM Minimum Pulse Width	t_{MIN}	10	-	-	µs
Switching Frequency	f_{SW}	100	-	2500	kHz
External Synchronized Frequency	f_{SYNC}	100 or f_{SW} x 0.8	-	2500 or f_{SW} x 1.2	kHz
External Synchronized Pulse Duty	D_{SYNC}	40	-	60	%
Operating Temperature	Topr	-40	-	+125	°C

(x = 1, 2)

(Note 1) ASO should not be exceeded.

Recommended Setting Parts Range

Parameter	Symbol	Min	Typ	Max	Unit
Capacitor Connecting to the VIN Pin*(Note 2)*	C_{VIN}	0.2	1.0	-	µF
Capacitor Connecting to the VDRV7 Pin*(Note 2)*	C_{VDRV7}	2.0	4.7	6.8	µF
Capacitor Connecting to the VREG5 Pin*(Note 2)*	C_{VREG5}	2.0	4.7	6.8	µF
Total DC/DC Output Capacitor*(Note 2)*	C_{OUT}	10	-	-	µF
400 kHz Switching Compensation Capacitor Connecting to the COMPx Pin*(Note 2)*	C_{COMPx}	0.02	0.47	2.20	µF
Resistor Connecting to the MSEL, BINx Pin	R_{MSEL}, R_{BINx}	1	-	100	kΩ
Resistor Connecting to the RT Pin	R_{RT}	6.8	-	100.0	kΩ
Pull Up to VIN Pin Resistor Connecting to the EN, MODE, SSUx Pin	R_{EN}, R_{MODE}, R_{SSUx}	10	-	100	kΩ
Resistor Connecting to the FAULT_Bx Pin	R_{FAULT_Bx}	4.7	-	-	kΩ
Resistor Connecting to the SO, SDA, SCL Pin	R_{SO}, R_{SDA}, R_{SCL}	1	-	-	kΩ
Current Sense Resistor	R_{SNSx}	91	-	-	mΩ

(x = 1, 2)

(Note 2) Set the capacitor in consideration of temperature characteristics and DC bias characteristics.

Electrical Characteristics

(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Total]						
VIN Sleep Circuit Current	I_{INSLP}	-	0.7	-	mA	
VIN Stand-by Circuit Current	I_{INSTB}	-	10	20	µA	V_{EN} = 0 V, V_{MODE} = 0 V
VIN Circuit Current	I_{INCC}	-	4.5	-	mA	V_{EN} = 5 V, V_{SNSPx} = 0 V, CHONx = 0
VIN UVLO Threshold Voltage	V_{INUVD}	3.80	4.10	-	V	Falling detect threshold
	V_{INUVR}	-	4.50	4.79	V	Rising release threshold
	$V_{INUVHYS}$	-	0.40	-	V	Hysteresis
VDRV7 UVLO Threshold Voltage	$V_{DRV7UVD}$	3.80	4.10	-	V	Falling detect threshold
	$V_{DRV7UVR}$	-	4.50	4.79	V	Rising release threshold
	$V_{DRV7UVHYS}$	-	0.40	-	V	Hysteresis
VREG5 UVLO Threshold Voltage	$V_{REG5UVD}$	3.78	4.10	-	V	Falling detect threshold
	$V_{REG5UVR}$	-	4.20	4.48	V	Rising release threshold
	$V_{REG5UVHYS}$	-	0.10	-	V	Hysteresis
VREG5 POR Threshold Voltage	V_{PORD}	2.50	2.70	-	V	Falling detect threshold
	V_{PORR}	-	2.90	3.10	V	Rising release threshold
	V_{PORHYS}	-	0.20	-	V	Hysteresis
[Reference Voltage]						
VDRV7 Reference Voltage	V_{DRV7}	6.5	7.5	9.0	V	C_{VDRV7} = 4.7 µF, No load
VDRV7 Drop Voltage	V_{DRV7DP}	-	0.25	-	V	V_{IN} = 4.75 V, I_{DRV7} = 25 mA
VDRV7 Output Current Limit	I_{DRV7LM}	40	-	-	mA	
VREG5 Reference Voltage	V_{REG5}	4.85	5.00	5.15	V	C_{VREG5} = 4.7 µF, No load
VREG5 Drop Voltage	V_{REG5DP}	-	0.15	0.40	V	V_{IN} = 4.75 V, I_{VREG5} = 10 mA
VREG5 Output Current Limit	I_{REG5LM}	40	-	-	mA	

Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[N-ch Gate Driver]						
GLx ON Resistor High	R_{GLxH}	-	1.2	3.0	Ω	I_{GLx} = 10 mA load
GLx ON Resistor Low	R_{GLxL}	-	1.0	2.0	Ω	I_{GLx} = 10 mA input
Minimum OFF Time	t_{OFFMIN}	-	40	-	ns	R_{RT} = 47 kΩ FRT[3:0] = 15
[DC/DC Current Detection]						
Over Current Protection Detection Voltage	V_{CSOCPx}	270	300	330	mV	OCPSETx[1:0] = 3
		132	150	168	mV	OCPSETx[1:0] = 1 (initial)
Over Current Detection Cycle	t_{CSOCP}	-	8	-	cycle	
The CSx Pin Leading Edge Blanking Time	t_{CSBLKx}	-	120	-	ns	
CS Level Shift Bias Current (No Slope Compensation Added)	I_{CSSLPx}	-	20	-	µA	
CSx to COMPx Level Shift Voltage	V_{CSLOWx}	-	0.9	-	V	No slope compensation added
[Error Amplifier]						
Trans Conductance	gm	-	130	-	µS	V_{SNSPx_SNSNx} = 191.5 mV
COMPx Sink Current	$I_{COMPxSI}$	-	230	-	µA	V_{SNSPx_SNSNx} = 0.2 V ISETx[9:0] = 901 (initial)
COMPx Source Current	$I_{COMPxSO}$	-	230	-	µA	V_{SNSPx_SNSNx} = 0 V ISETx[9:0] = 901 (initial)

(x = 1, 2)

Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Current Sense Amplifier]						
SNSPx to SNSNx Average Current Sense Threshold Voltage	$V_{SNSxAVE\ 100\%H}$	185.7	191.5	197.2	mV	V_{SNSNx} = 13 V ISETx[9:0] = 1023
	$V_{SNSxAVE\ 87\%H}$	161.6	166.6	171.6	mV	V_{SNSNx} = 13 V ISETx[9:0] = 901 (initial)
	$V_{SNSxAVE\ 50\%H}$	90.7	95.6	100.5	mV	V_{SNSNx} = 13 V ISETx[9:0] = 552
	$V_{SNSxAVE\ 10\%H}$	15.1	19.1	23.1	mV	V_{SNSNx} = 13 V, ISETx[9:0] = 176
	$V_{SNSxAVE\ 87\%L}$	150.0	166.6	183.0	mV	V_{SNSNx} = 0 V, Low-side-sense ISETx[9:0] = 901 (initial)
Current Sense Threshold Resolution	$\Delta V_{SNSxLSB}$	-	0.203	-	mV	
Current Sense Threshold Differential Non-Linearity	$\Delta V_{SNSxDNL}$	-	±2	-	LSB	
SNSPx Input Current	I_{SNSPx}	-	300	-	µA	V_{SNSPx_SNSNx} = 191.5 mV V_{SNSNx} = 4 V, CHONx = 1, PWMx = L
SNSNx Input Current	I_{SNSNx}	-	20	-	µA	V_{SNSPx_SNSNx} = 191.5 mV V_{SNSNx} = 4 V, CHONx = 1, PWMx = L
LED Current Limit Threshold Voltage	$V_{SNSxCLIM}$	-	241.5	-	mV	V_{SNSPx} - V_{SNSNx} ,V_{SNSNx} = 15 V, ISETx[9:0] = 1023, CURLIMENx = 3
LED Over Current Limit Enable Threshold Voltage	$V_{CLIMxENH}$	-	7.4	-	V	V_{SNSNx} rising detect threshold
	$V_{CLIMxENL}$	-	7.1	-	V	V_{SNSNx} falling release threshold
LED Status Good Threshold Voltage	V_{SNSxSG}	-	$V_{SNSxAVE}$ – 20	-	mV	V_{SNSNx} = 13 V
Short Circuit Protection Threshold Voltage	$V_{SNSxSCP}$	-	330	-	mV	V_{SNSPx} - V_{SNSNx}, V_{SNSNx} = 4 V ISETx[9:0] = 901 $V_{SNSxSCP}$ = $V_{SNSxAVE}$ + 163.4 mV
Short Circuit Protection Delay Time	t_{SCPDLY}	40	50	60	µs	
Hiccup Time	t_{HICCUP}	32	40	48	ms	Short circuit detect
[Voltage Sense]						
SNSNx Voltage Sense Resistor Divider Ratio	K_{SNSNx}	-	0.033	-	-	
SNSNx Voltage (Voltage Regulation Mode)	V_{SNSNx_1}	64.0	66.0	68.0	V	ISETx[9:0] = 901, VMODEx = 1
	V_{SNSNx_2}	46.5	48.0	49.5	V	ISETx[9:0] = 655, VMODEx = 1
	V_{SNSNx_3}	23.2	24.0	24.8	V	ISETx[9:0] = 328, VMODEx = 1
SNSNx Voltage Resolution	$\Delta V_{SNSNxLSB}$	-	0.073	-	V	

(x = 1, 2)

Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[PWM Dimming]						
PWMDx Input for DC/DC Switching ON Threshold	V_{PWMDxH}	0.14	0.17	0.20	V	Rising, STAND-ALONE state
PWMDx Input for DC/DC Switching OFF Threshold	V_{PWMDxL}	0.12	0.15	0.18	V	Falling, STAND-ALONE state
PWMDx Input for DC/DC Switching ON Threshold	V_{PWMDxH}	0.42	0.46	0.50	V	Rising
PWMDx Input for DC/DC Switching OFF Threshold	V_{PWMDxL}	0.40	0.44	0.48	V	Falling
PWMDx to DC/DC Switching ON Transition Delay Time	t_{PWMDxH}	-	1	-	µs	
PWMDx to DC/DC Switching OFF Transition Delay Time	t_{PWMDxL}	-	1	-	µs	
Internal PWM Frequency	f_{PWM}	-	203	-	Hz	PWMDIV[2:0] = 1 (initial)
		-	407	-	Hz	PWMDIV[2:0] = 4
		-	610	-	Hz	PWMDIV[2:0] = 6
		-	814	-	Hz	PWMDIV[2:0] = 7
PDRVx Pull Up ON Resistor	R_{PDRVx_U}	-	20	50	Ω	I_{PDRVx} = -10 mA
PDRVx Pull Down Current	I_{PDRVx_D}	-	38	70	mA	V_{SNSPx_PDRVx} = 0 V, V_{SNSPx} = 30 V
PDRVx Output Low Voltage	$V_{PDRVxOL}$	-9.5	-8.0	-6.5	V	V_{SNSPx} = 30 V
[NTC Dimming]						
NTCx Threshold Voltage	V_{NTCx_TH}	-	1.25	-	V	NTCSETx[7:0] = 127, falling
NTCx GAIN	V_{NTCx_GAIN}	-	166.8	-	mV/V	GAIN = V_{SNSx} / V_{NTCx} NTCSETx[7:0] = 255, NTCGAINx[1:0] = 2
NTCx Pin Input Current	I_{NTCx}	-	0	10	µA	V_{NTCx} = 3.0 V
[BIN]						
BINx Pull Down Current	I_{BINx}	-	2	10	µA	V_{BINx} = 5 V
[EN]						
EN Pull Down Current	I_{EN}	-	15	35	µA	V_{EN} = 5 V
EN Pin Threshold Voltage	V_{ENIH}	-	-	1.5	V	Rising detect threshold
	V_{ENIL}	0.5	-	-	V	Falling release threshold
	V_{ENHYS}	-	0.1	-	V	Hysteresis
[MODE, MSEL]						
MODE Pull Down Current	I_{MODE}	-	35	60	µA	V_{MODE} = 5 V
MODE Pin Threshold Voltage	V_{MODEIH}	-	-	2.3	V	Rising detect threshold
	V_{MODEIL}	0.8	-	-	V	Falling release threshold
	$V_{MODEHYS}$	-	0.35	-	V	Hysteresis
MSEL Pull Down Current	I_{MSEL}	-	2	10	µA	V_{MSEL} = 5 V
[Soft Start]						
Soft Start Time	t_{SSx2}	4.0	4.5	5.0	ms	R_{RT} = 47 kΩ, FRT[3:0] = 5 (initial) SSSETx[2:0] = 2 (initial) Time for ISETx[9:0] to increase from 0 to 901.
[SSU]						
SSUx Pull Down Current	I_{SSUx}	-	0	10	µA	V_{SSUx} = 5 V
SSUx Pin Threshold Voltage	V_{SSUxIH}	-	-	2.3	V	Rising detect threshold
	V_{SSUxIL}	0.8	-	-	V	Falling release threshold
	$V_{SSUxHYS}$	-	0.35	-	V	Hysteresis

(x = 1, 2)

Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[OSCILLATOR Circuit]						
Switching Frequency Setting	f_{SW1}	360	399	440	kHz	R_{RT} = 47 kΩ FRT[3:0] = 5 (initial)
	f_{SW2}	912	1014	1115	kHz	R_{RT} = 47 kΩ FRT[3:0] = 15
	f_{SW3}	1963	2230	2453	kHz	R_{RT} = 7.5 kΩ FRT[3:0] = 5 (initial)
	f_{SSFM}	-	3968	-	Hz	R_{RT} = 47 kΩ, FRT[3:0] = 5 (initial), SSFM[2:0] = 7
		-	506	-	Hz	R_{RT} = 47 kΩ, FRT[3:0] = 5 (initial), SSFM[2:0] = 4 (initial)
		-	64	-	Hz	R_{RT} = 47 kΩ, FRT[3:0] = 5 (initial), SSFM[2:0] = 1
		Not applicable			Hz	SSFM[2:0] = 0
	f_{SSFMW}	-	15	-	%	SSFMW[1:0] = 3
		-	5	-	%	SSFMW[1:0] = 1 (initial)
[SYNC]						
SYNC Pull Down Current	I_{SYNC}	-	10	25	µA	V_{SYNC} = 5 V
SYNC Pin Threshold Voltage	V_{SYNCIH}	-	-	2.1	V	Rising detect threshold
	V_{SYNCIL}	0.6	-	-	V	Falling release threshold
[Over Voltage Protection / Under Voltage Detection]						
Over Voltage Protection Detect Voltage	V_{OVPx_15}	64.0	67.5	71.0	V	V_{SNSPx} rising OVPSETx[3:0] = 15 (initial)
	V_{OVPx_10}	53.0	56.6	60.0	V	V_{SNSPx} rising OVPSETx[3:0] = 10
	V_{OVPx_0}	32.5	34.8	37.0	V	V_{SNSPx} rising OVPSETx[3:0] = 0
Over Voltage Protection Hysteresis Voltage	$V_{OVPxHYS}$	-	1.6	-	V	
Over Voltage Protection Flag Release Delay Time	t_{OVR}	14	20	26	ms	
External Over Voltage Protection Detect Voltage	V_{EOVPx}	2.420	2.500	2.580	V	V_{SSUx} rising EOVPx/SSUx = 0 (initial)
External Over Voltage Protection Hysteresis Voltage	$V_{EOVPxHYS}$	-	65	-	mV	EOVPx/SSUx = 0 (initial)
External Under Voltage Detect Voltage	V_{EUVDx}	-	185	-	mV	V_{SSUx} falling EOVPx/SSUx = 0 (initial)
External Under Voltage Detect Hysteresis Voltage	$V_{EUVDxHYS}$	-	65	-	mV	EOVPx/SSUx = 0 (initial)
Under Voltage Detect Release Voltage 1	V_{UVRx1}	-	-	2.2	V	V_{SNSNx} rising BTBx = 0 (initial) EOVPx/SSUx = 1
Under Voltage Detect Voltage 1	V_{UVDx1}	0.6	-	-	V	V_{SNSNx} falling BTBx = 0 (initial) EOVPx/SSUx = 1
Under Voltage Detect Release Voltage 2	V_{UVRx2}	-	-	15.2	V	V_{SNSNx} rising BTBx = 1 EOVPx/SSUx = 1
Under Voltage Detect Voltage 2	V_{UVDx2}	13.6	-	-	V	V_{SNSNx} falling BTBx = 1 EOVPx/SSUx = 1
Under Voltage Detect Flag Set Delay Time	t_{UVD}	14	20	26	ms	

(x = 1, 2)

Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, V_{EN} = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[LOGIC I/O SCK, CSB, SI, SO, FAULT_B]						
Internal Oscillator Frequency	f_{OSC}	2.0	2.5	3.0	MHz	
Input Voltage High	V_{IHxx}	2.2	-	-	V	The SCK, CSB and SI pins
Input Voltage Low	V_{ILxx}	-	-	0.6	V	The SCK, CSB and SI pins
Input Pull-down Resistor	R_{INxx_PD}	250	500	1000	kΩ	The SCK and SI pins
CSB Pull-up Current	I_{CSB_LEAK}	-	10	-	µA	V_{CSB} = 0 V
SO Output Low Voltage	V_{SO_OL}	-	-	0.6	V	I_{SO_O} = 10 mA input
SO Output Leakage Current	I_{SO_LEAK}	-	-	1	µA	V_{SO} = 5 V
FAULT_Bx Output Low Voltage	$V_{FLT\_Bx\_OL}$	-	-	0.6	V	I_{FAULT_Bx} = 10 mA input
FAULT_Bx Output Leakage Current	$I_{FLT\_Bx\_LEAK}$	-	-	1	µA	V_{FAULT_Bx} = 5 V
[I²C BUS Interface]						
SCL Clock Frequency	f_{SCL}	0	-	400	kHz	
SCL Low Duration	t_{LOW}	1.3	-	-	µs	
SCL High Duration	t_{HIGH}	0.6	-	-	µs	
Data Hold Time	$t_{HD;DAT}$	0.0	-	0.9	µs	
Data Setup Time	$t_{SU;DAT}$	100	-	-	ns	
Setup Time – Restart Condition	$t_{SU;STA}$	0.6	-	-	µs	
Hold Time – Restart Condition	$t_{HD;STA}$	0.6	-	-	µs	
Setup Time – Stop Condition	$t_{SU;STO}$	0.6	-	-	µs	
Bus Free Time Between Start and Stop	t_{BUF}	1.3	-	-	µs	
Interface Startup Time	t_{EN}	-	-	350	µs	Bus startup time
[A/D Converter]						
A/D Resolution	-	-	10	-	bit	
A/D Conversion Time	t_{ADC}	-	11.2	-	µs	
A/D Full Scale Reference Voltage	V_{FSRADC}	2.43	2.50	2.57	V	
Integral Nonlinearity	INL	-	±3	-	LSB	
Differential Nonlinearity	DNL	-	±3	-	LSB	
ADC Monitoring Nodes Full Scale Range	V_{FSR1}	-	77.5	-	V	V_{IN}
	V_{FSR2}	-	75.0	-	V	V_{SNSx}
	V_{FSR3}	-	V_{FSRADC}	-	mV	V_{ISNSx}, V_{NTCx}
	V_{FSR4}	-	5.0	-	V	V_{BINx}, V_{MSEL}
	V_{FSR5}	-	10.0	-	V	V_{INDIM}
ADC Monitoring Nodes Read Values Total Accuracy	ΔADC	-6	-	+6	%	Monitor Voltage = V_{FSRx} / 2
Thermal Sensor ADC Read Value	ADC_{TEMP25}	-	418	-	-	Tj = 25 °C
	$ADC_{TEMP150}$	-	602	-	-	Tj = 150 °C

(x = 1, 2)

Description of Blocks

From this page onward, 'x' used in the symbol means x = 1, 2.

1 Power Supply for N-ch MOSFET Gate Driver and Internal Circuit (VDRV7)

The VDRV7 pin voltage 7.5 V (Typ) is generated from the VIN pin voltage. This voltage is used as the power supply for driving the DC/DC N-ch MOSFET. The total current supplied to the DC/DC N-ch MOSFET and the resistor must be I_{DRV7LM} (VDRV7 output current limit) or less.

The current supplied to the DC/DC N-ch MOSFET (I_{MOSFET}) can be calculated by the following formula.

$$I_{MOSFET} = Q_G \times f_{SW}$$

Where:

Q_G is the gate charge of the MOSFET.

f_{SW} is the switching frequency.

Connect C_{VDRV7} = 4.7 µF as feedback compensation capacitor to the VDRV7 pin. Place ceramic capacitor close to the IC to minimize trace length to the VDRV7 pin and also to the IC ground.

Do not use the VDRV7 pin as a power supply other than this IC.

2 Internal Reference Voltage (VREG5)

The VREG5 pin voltage 5.0 V (Typ) is generated from the VIN pin voltage. This voltage is used as the internal power supply of the IC. The total current drawn from the VREG5 pin must be I_{REG5LM} (VREG5 Output Current Limit) or less. Connect C_{VREG5} = 4.7 µF as feedback compensation capacitor to the VREG5 pin. Place ceramic capacitor close to the IC to minimize trace length to the VREG5 pin and also to the IC ground. Do not use the VREG5 pin as a power supply other than this IC.

3 LED Current Setting (CURRENT SENSE)

LED current (I_{LED}) can be set by resistor R_{SNSx} connected between the SNSPx pin and the SNSNx pin and can be programmed by SPI register ISETx[9:0]. The internal Rail-to-Rail current sense amplifier monitors the LED current with the differential voltage (V_{SNSx}) divided by R_{SNSx} between the SNSPx pin and SNSNx pin and generates a scaled output voltage V_{ISETx} given as V_{SNSx} x12 plus 0.2 V offset. The internally scaled output voltage V_{ISETx} will be compared to the reference voltage V_{DCDIMx} by the GM error amplifier to generate an error signal. This output error signal will be integrated by the compensation capacitor C_{COMPx} connected to the COMPx pin. The Internal reference voltage V_{DCDIMx} is the output of the 10bit DAC converter and the DAC full scale range is 2.5 V (V_{FSRADC}), same with the internal 10 bit ADC.

Programmable LED average current can be calculated by the following formula.

$$I_{LEDxAVE} = \frac{V_{SNSxAVE}}{R_{SNSx}} = \frac{V_{DCDIMx} - 0.2\,V}{12 \times R_{SNSx}} = \left(\frac{ISETx[9:0]}{1024} \times V_{FSRADC} - 0.2\,V\right) \times \frac{1}{12 \times R_{SNSx}} \quad [A]$$

Where:

$V_{SNSxAVE}$ is the average current sense regulation voltage set by ISETx[9:0].

V_{DCDIMx} is the internal reference voltage of the GM amplifier to define the V_{SNSx}.

V_{FSRADC} is the reference voltage of the 10bit DAC that outputs the V_{DCDIMx}.

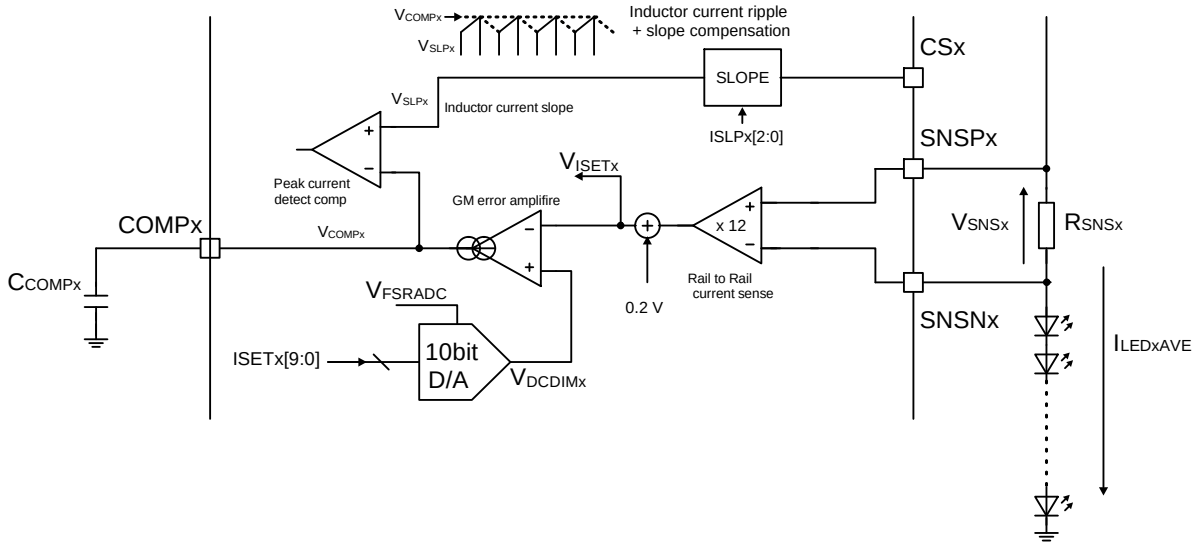


Figure 1. LED Current Setting

3 LED Current Setting (CURRENT SENSE) - continued

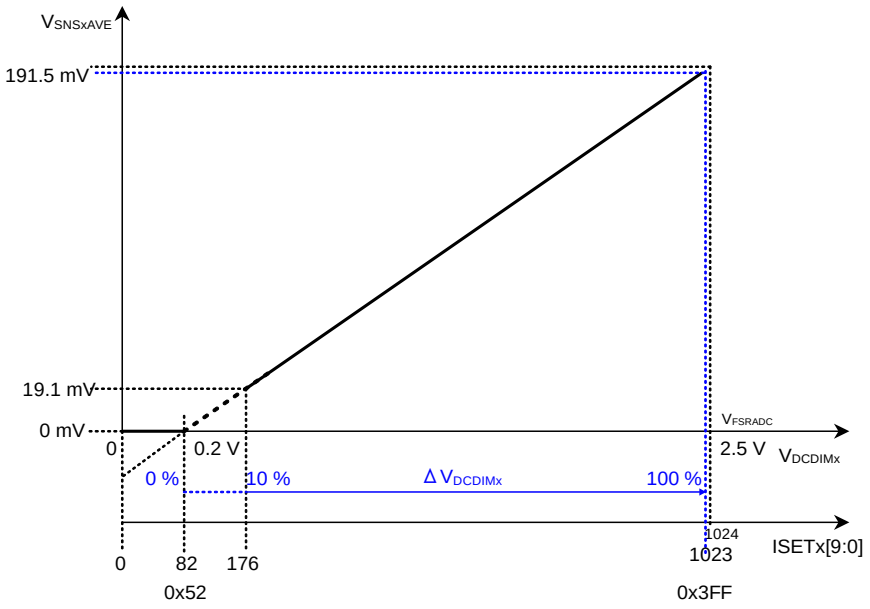


Figure 2. Current Sense Regulation Voltage Setting

ISETx[9:0]	$V_{SNSxAVE}$ [mV]
82	0.0
131	10.0
190	22.0
244	33.0
313	47.0
333	51.1
416	68.0
485	82.0
529	91.0
574	100.1
623	110.1
672	120.1
721	130.0
819	150.0
901	166.6
1023	191.5

Description of Blocks - continued

4 Slow Startup

BD18354MUF-M can select slow startup function by setting the SPI register EOVPx/SSUx = 1 and the SSUx pin H/L.
When the SSUx pin = H, ISETx[9:0] is incremented from ISETx[0] to ISETx[9:0] for each t_{SSUx} at startup.
t_{SSUx} can be calculated by the following formula.

$$t_{SSUx} = \frac{1}{f_{PWM} \times SSU_{DIVx}} \times ISETx[9:0] \text{ [s]}$$

Where:
f_{PWM} is the PWM dimming frequency.
SSU_{DIVx} is the is a division factor provided in slow startup register.
$ISET_x[9:0]$ is the SPI register to set LED current.

SSUSETx[1:0]	SSU_{DIVx}
0 (initial)	1
1	2
2	4
3	8

PWMDIV[2:0]	f_{PWM} [Hz]	ISETx[9:0]	SSUSETx[1:0]	SSU_{DIVx}	t_{SSUx} [s]
2	244	901	0	1	3.69
			1	2	1.85
			2	4	0.92
			3	8	0.46

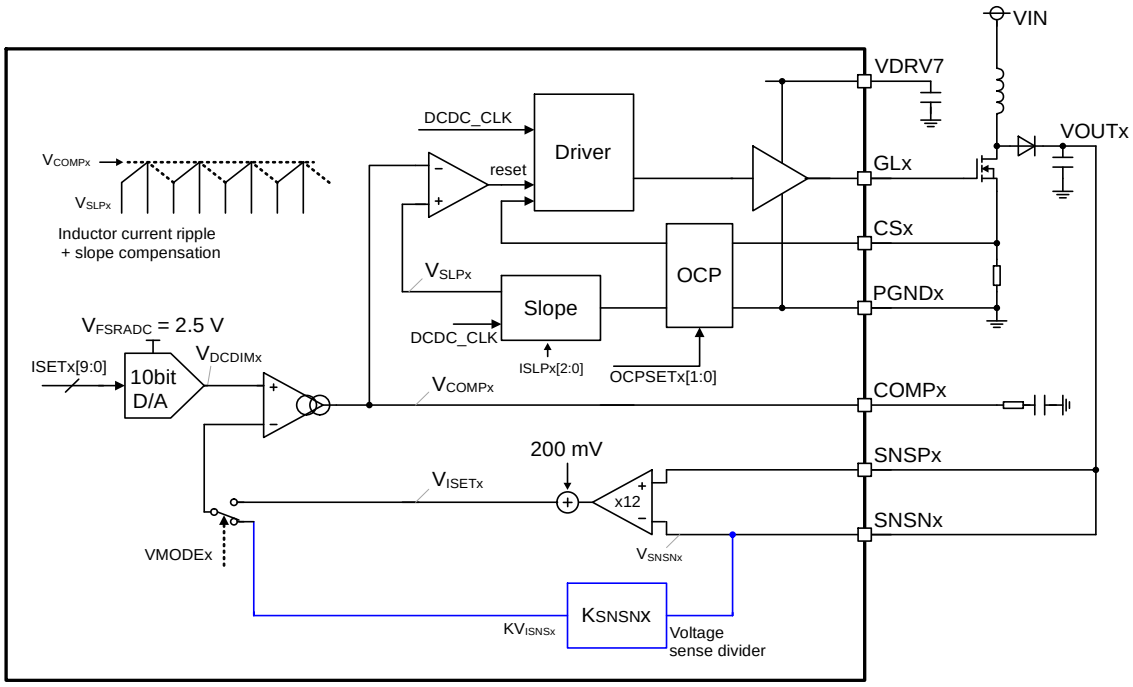
Description of Blocks - continued

5 Voltage Regulation

The BD18354MUF-M supports “voltage regulation mode” when the VMODEx bit is set in the DCDCSET2 register. In the voltage regulation mode, the BD18354MUF-M regulates the SNSNx pin voltage (V_{SNSNx}) by control inductor peak current in average voltage sensing feedback loop. The Internal reference voltage V_{DCDIMx} is the output of the 10bit DAC converter and this DAC full scale range is 2.5 V (V_{FSRADC}) same with the internal 10bit ADC.
Programmable VOUTx average ($V_{OUTxAVE}$) voltage can be calculated by the following formula.
When VMODEx = 1, it is automatically set to $V_{SNSxSCP}$ = 163.4 mV ($V_{SNSxAVE}$ = 0 V).
Short the SNSPx and SNSNx pins or mask the SCP function with the register setting SCPxMASK = 1.

$$V_{OUTx\_AVE} = \frac{V_{DCDIMx} \times 75}{2.5} = \frac{ISETx[9:0]}{1024} \times \frac{V_{FSRADC} \times 75}{2.5} \quad [V]$$

Where:
V_{DCDIMx} is the internal reference voltage of the GM amplifier to define the V_{SNSx}.
V_{FSRADC} is the reference voltage of the 10bit DAC that outputs V_{DCDIMx}.



ISETx[9:0]	$V_{OUTxAVE}$ [V]
328	24.0
492	36.0
655	48.0
751	55.0
901 (initial)	66.0

Description of Blocks - continued

6 PWM Dimming (PWMDIM)

6.1 External P-ch MOSFET Drive

The PDRVx pin drives an external P-ch MOSFET to achieve PWM dimming. Connect the gate of the P-ch MOSFET to the PDRVx pin. The PDRVx pin outputs SNSPx and SNSPx - 8 V (Typ).

At start up and restart (After UVLO, TSD, SCP, OVP is released or start up.), after DC/DC starts switching, the PDRVx pin can output SNSPx - 8 V (Typ).

The PDRVx output voltage and the DC/DC output voltage (SNSPx pin voltage) have the characteristics shown below figure. When the number of LED lights is small, design and evaluate in consideration of the characteristics shown below figure. There is a possibility that the external P-ch MOSFET cannot be driven.

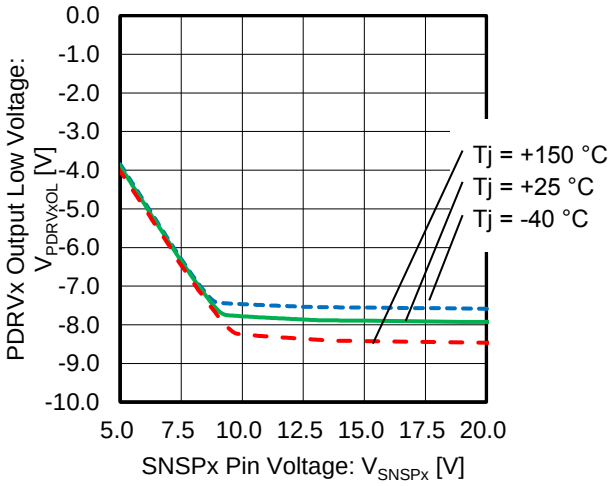


Figure 3. PDRVx Output Low Voltage vs SNSPx Pin Voltage

6.2 Rush Current Limit Drive Circuit

Rush current limit (CLIM) function is enabled when register CURLIMENx = 1. This is a function that suppresses inrush current flowing into the LED due to the discharge current that occurs when the number of LED lights changes.

The limited current value when the CLIM function is activated is $V_{SNSxCLIM}$ = V_{SNSx} + 50 mV(Typ). When ISETx[9:0] = 1023, $V_{SNSxCLIM}$ = 241.5 mV.

When an overcurrent occurs to the LED and the voltage between the SNSPx pin and SNSNx pin exceeds $V_{SNSxCLIM}$, the external PMOS turns OFF. 10 µs after PMOS = OFF, the LED will restart lighting with the current suppressed by the $V_{SNSxCLIM}$ voltage. At this time, the output current is linearly controlled by an external PMOS. When the discharge current disappears, the external PMOS returns to the ON state. This function is effective when PWM dimming is not used and the SNSNx pin voltage > 7.4 V or more. The function is automatically turned off when SNSNx pin voltage = 7.1 V or less. In addition, the current limit drive function is masked when the SNSNx pin voltage drops below VIN pin voltage + 2.2 V.

$$I_{LED\_LIM} = \frac{V_{SNSxCLIM}}{R_{SNSx}} = \frac{V_{SNSx}+50\ mV}{R_{SNSx}}\ [A]$$

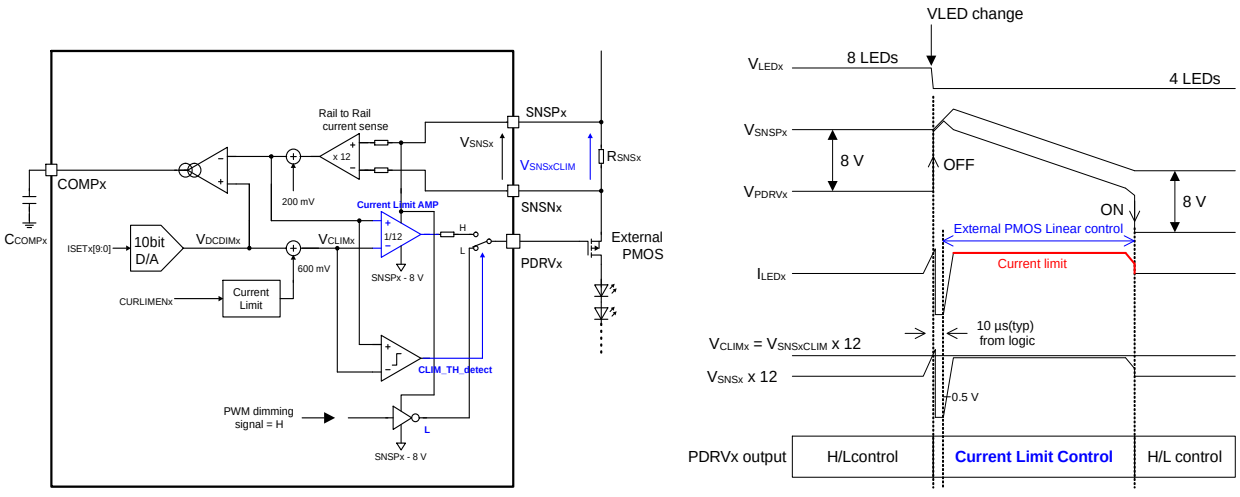


Figure 4. Current Limit Drive Circuit and Waveforms

6 PWM Dimming (PWMDIM) - continued

6.3 Internal PWM Dimming Setting

The BD18354MUF-M has an internal 10-bit PWM dimming generator to make timing for individual Boost converter switching ON/OFF. The internal PWM dimming ON duty cycle (D_{PWMONx}) is set by the SPI register the DPWMx[9:0]. PWM dimming frequency f_{PWM} can be set by the SPI register the PWMDIV[2:0] and this PWM dimming frequency setting is common to all boost channels for synchronous PMW dimming within the device itself.
Except for DPWMx[9:0] = 0 setting.

$$D_{PWMONx} = \frac{DPWMx[9:0] + 1}{1024}, \qquad t_{PWMONx} = \frac{D_{PWMONx}}{f_{PWM}}$$

Regardless of the above formula, the internal PWM dimming ON duty cycle (D_{PWMONx}) is set to 0 % when DPWMx [9:0] = 0 is set.

PWMDIV[2:0]	f_{PWM} [Hz]
0	81.4
1 (initial)	203.0
2	244.0
3	305.0
4	407.0
5	488.0
6	610.0
7	814.0

6.4 External PWM Dimming Setting

PWM dimming ON time t_{PWMONx} is controlled by the internal PWM dimming generator or an external PWM dimming control thru the PWMDx pin. If the PWMDx pin is set to high level, t_{PWMONx} is 100 % ON duty.
If the PWMDx pin is set to low level, t_{PWMONx} is equal to the internal PWM ON cycle (D_{PWMONx}).
In case of PWM dimming setting $D_{PWMONx0\%}$ (initial), the PWMDx pin can be used for external PWM dimming control for LED current ON/OFF.

6.5 Hybrid External Analog and PWM Dimming Setting

The BD18354MUF-M supports “external analog dimming mode” when the STAND-ALONE state.
In the external analog dimming mode, internal reference voltage for current regulation can be defined by the PWMDx pin voltage (V_{PWMDx}). When the external reference voltage V_{PWMDx} is lower than internal reference voltage V_{DCDIMx}, feed-back voltage V_{ISNSx} will be regulated by the external one. In case of using analog dimming and PWM dimming by the PWMDx pin, applying PWM peak voltage defines analog dimming level $I_{LEDxAVE}$ and PWM duty (D_{PWMON}) defines PWM dimming ON time t_{PWMON}. The analog dimming reference peak voltage V_{PDxPK} can be set by the voltage divider (R_{PDx1} and R_{PDx2}) and PWM duty (D_{PWMON}) control by external NPN transistor by applying invert PWM signals (PWMx_B).

Current Setting Definition for CHx	
LEDACTIVE	STAND-ALONE
ISETx[9:0]	ISETx[9:0] & PWMDx pin
$V_{DCDIMx} = V_{ISETx\_DAC} - 0.2\,V$	if $V_{ISETx\_DAC} > V_{PWMDx}$, $V_{DCDIMx} = V_{PWMDx} - 0.2\,V$ if $V_{ISETx\_DAC} < V_{PWMDx}$, $V_{DCDIMx} = V_{ISETx\_DAC} - 0.2\,V$

6.5 Hybrid External Analog and PWM Dimming Setting – continued

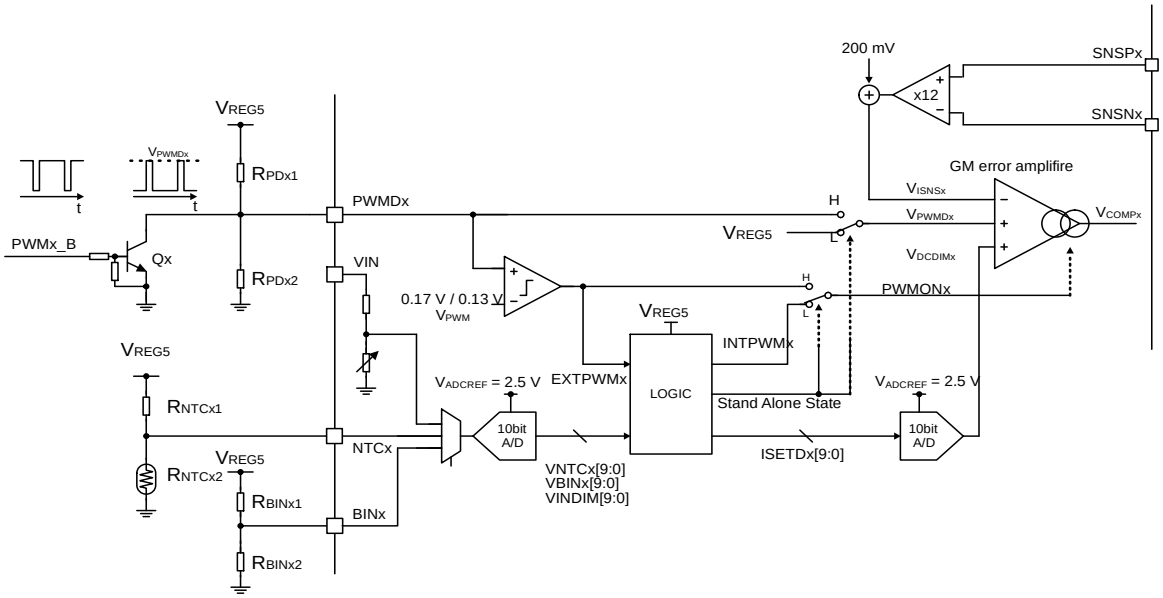


Figure 5. Hybrid External Analog and PWM Dimming

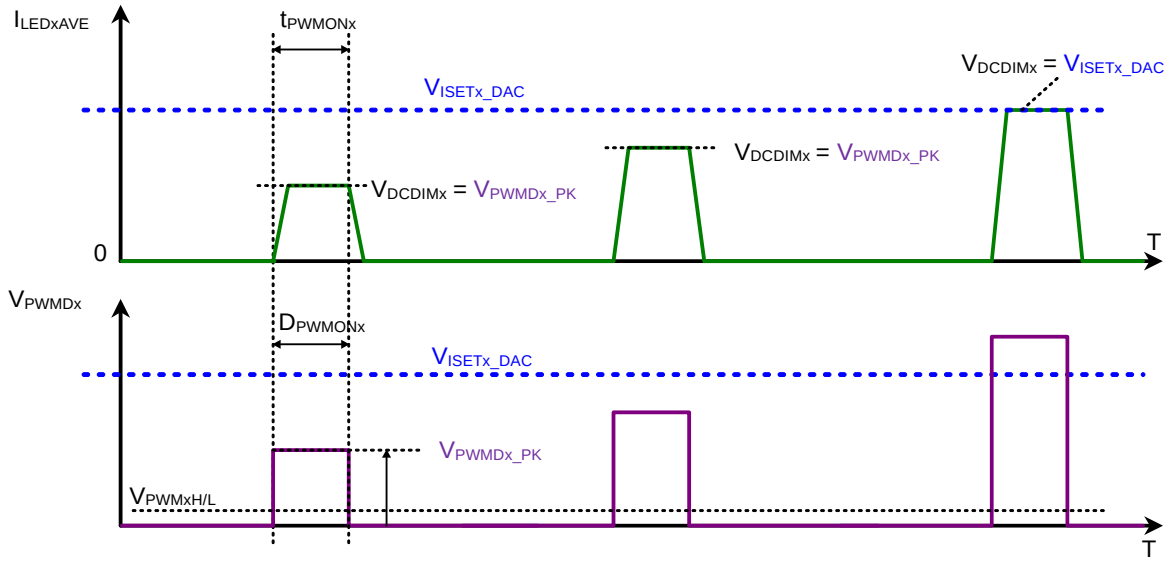


Figure 6. Hybrid External Analog and PWM Dimming Waveforms

Description of Blocks - continued

7 Analog Dimming

BD18354MUF-M has two systems of analog dimming function in addition to the analog dimming by the PWMDx pins.

7.1 PWMDx Pin Analog Dimming Setting

When the STAND-ALONE state, Internal reference voltage for current regulation can be defined by the PWMDx pin voltage (V_{PWMDx}). When the external reference voltage V_{PWMDx} is lower than the internal reference voltage V_{DCDIMx}, feed-back voltage V_{ISNSx} will be regulated by the external one. When the PWMDx pin (The lower voltage takes precedence) becomes V_{DCDIMx} or less, the LED current decreases. When not using the analog dimming function, set it to 3 V or more.

When the analog dimming rate is low, DC/DC control may become unstable and the LED may flicker.
Confirm enough in the evaluation.

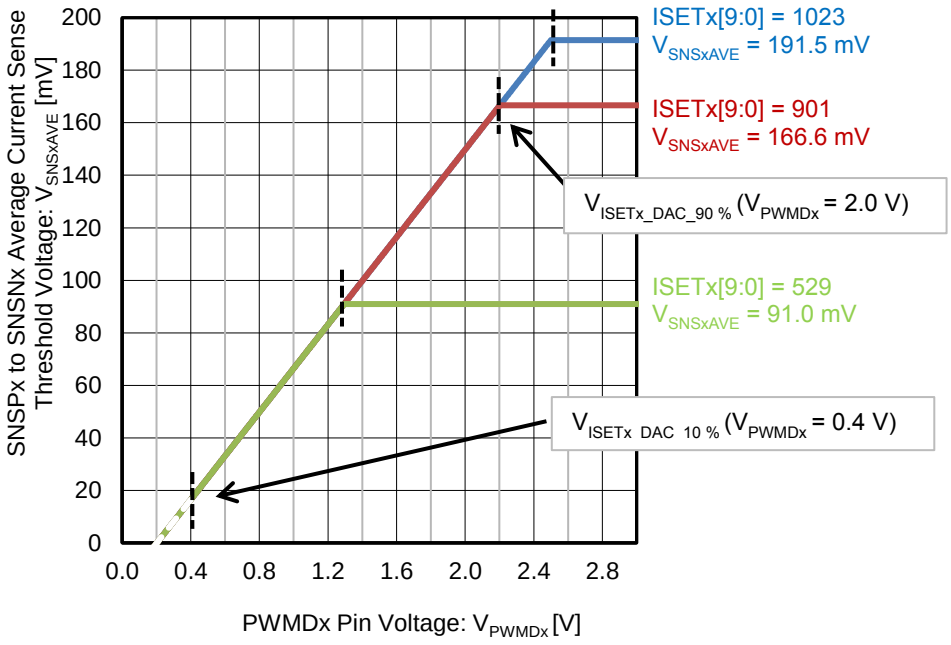


Figure 7. $V_{SNSxAVE}$ vs V_{PWMDx} (PWMDx Pin Analog Dimming)

7 Analog Dimming - continued

7.2 VIN Pin, NTCx Pin and BINx Pin Dimming Setting

Setting the SPI register ADMODE = 1 enables input voltage dimming using the VIN pin, temperature dimming using the NTCx pin, and BIN dimming using the BINx pin.

In input voltage dimming, when the input voltage (V_{IN}) drops, the output current is reduced to prevent the input current from increasing. The derating start voltage V_{INDIM} can be set by the SPI register the VINDSETx[1:0]. The derating gain ($V_{INDGAIN}$) is set by the SPI register the VINDGAINx[1:0].

The thermal derating performs dimming control according to temperature changes by connecting an NTC element. The derating start voltage V_{NTCx} can be set by the SPI register the NTCSETx[7:0]. The derating gain (V_{NTCx_GAIN}) is set by the SPI register the NTCGAINx[1:0].

Voltage sampling of VIN pin and NTCx pin is performed every 128 µs, and the value of ISETDx[9:0] is updated. In the BIN dimming, the LED current can be adjusted by selecting the BINx pin voltage (V_{BINx}) and the BIN table set by the BINSELx[1:0] register. BIN dimming is reflected when starting with CHONx = 1.

The LED average current during derating can be calculated by the following formula.

$$I_{LEDxAVE} = \frac{V_{SNSxAVE}}{R_{SNSx}} = \left(\frac{ISETDx[9:0]}{1024} \times V_{FSRADC} - 0.2\,V\right) \times \frac{1}{12 \times R_{SNSx}} \text{ [A]}$$

$$ISETDx[9:0] = ISETNTCx[9:0] + (VIND[9:0] - VINDSETx[1:0]) \times VINDGAINx[1:0]$$

$$ISETNTCx[9:0] = ISETx[9:0] + BINVALx + (VNTCx[9:0] - NTCSETx[7:0]) \times NTCGAINx[1:0]$$

Where:

$V_{SNSxAVE}$ is the average current sense regulation voltage.
R_{SNSx} is the resistor of the LED current setting.
$ISETDx$[9:0] is the SPI register for setting LED average current during all derating operation.
V_{FSRADC} is the reference voltage of the 10bit A/D.

$ISETNTCx$[9:0] is the SPI register for setting LED average current during NTC derating operation.
$VIND[9:0]$ is the voltage of the AD conversion of the VIN pin voltage.
$VINDSETx[1:0]$ is the SPI register that sets the input voltage derating start voltage.
$VINDGAINx[1:0]$ is the SPI register that sets the input voltage derating gain.

$ISETx[9:0]$ is the SPI register to set LED average current.
$BINVALx$ is the value from the BIN table set by the SPI register BINSELx[1:0].
$VNTCx[9:0]$ is the voltage of the AD conversion of the NTCx pin voltage.
$NTCSETx[7:0]$ is the SPI register that sets the NTC start voltage.
$NTCGAINx[1:0]$ is the SPI register that sets the derating gain.

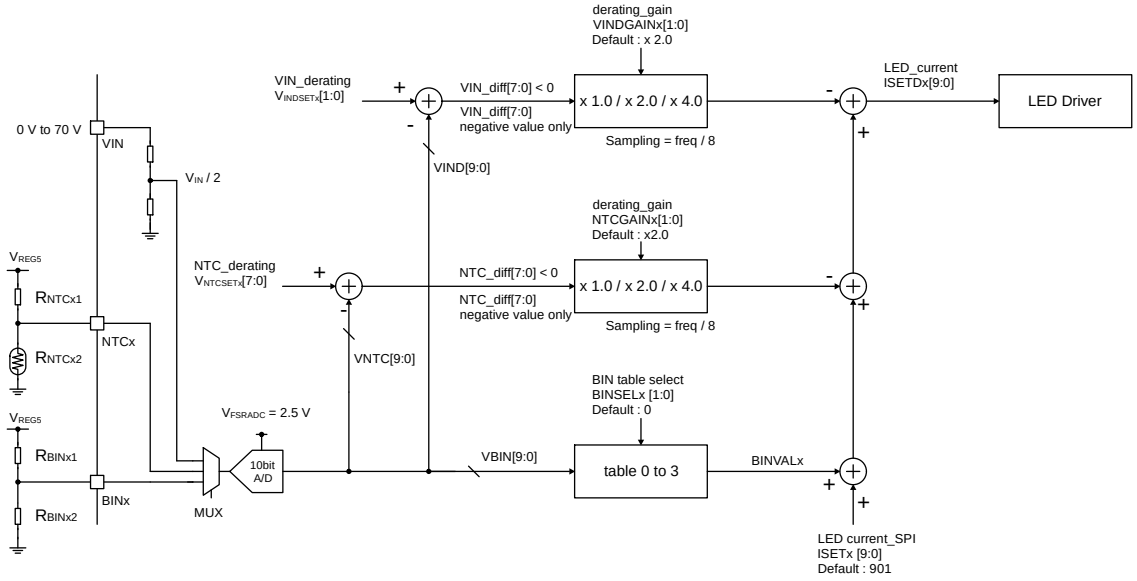


Figure 8. LED Current During Derating

7.2 VIN Pin, NTCx Pin and BINx Pin Dimming Setting - continued
The Functions enabled by ADMODE setting.

ADMODE	Input Voltage Derating	BIN Derating	NTC Derating
0	OFF	OFF	OFF
1 (initial)	ON	ON	ON

The input voltage derating start voltage V_{INDSET} set by the SPI register VINDSETx[1:0].

VINDSETx[1:0]	V_{INDSET} [V]
0	8.5
1 (initial)	8.0
2	7.5
3	7.0

The input voltage derating GAIN VINDGAIN set by the SPI register VINDGAINx[1:0].

VINDGAINx[1:0]	VINDGAINx	GAIN ($V_{SNSxAVE}$ / V_{IN}) [mV/V]
0	0 (mask function)	0.0
1	1	20.8
2 (initial)	2	41.5
3	4	83.0

Dimming example of the VIN pin:
Condition: VINDSETx[1:0] = 1 (initial), VINDGAINx[1:0] = 2 (initial),
BINSELx[1:0] = 0, NTCSETx[7:0] = 127 (initial), NTCGAINx[1:0] = 2 (initial)

VIN pin voltage [V]	ISETx[9:0]	VINDSETx[1:0]	VINDGAINx[1:0]	ISETDx[9:0]	$V_{SNSxAVE}$ [mV]
	901 (initial)	1 (initial)	2 (initial)	Calculation	
		$V_{INDSETx}$ [V]	VINDGAINx		
13.0	901	8.00	2	901	166.6
9.0				901	166.6
8.0				901	166.6
7.5				799	145.9
7.0				697	125.1
6.5				595	104.4
6.0				493	83.6

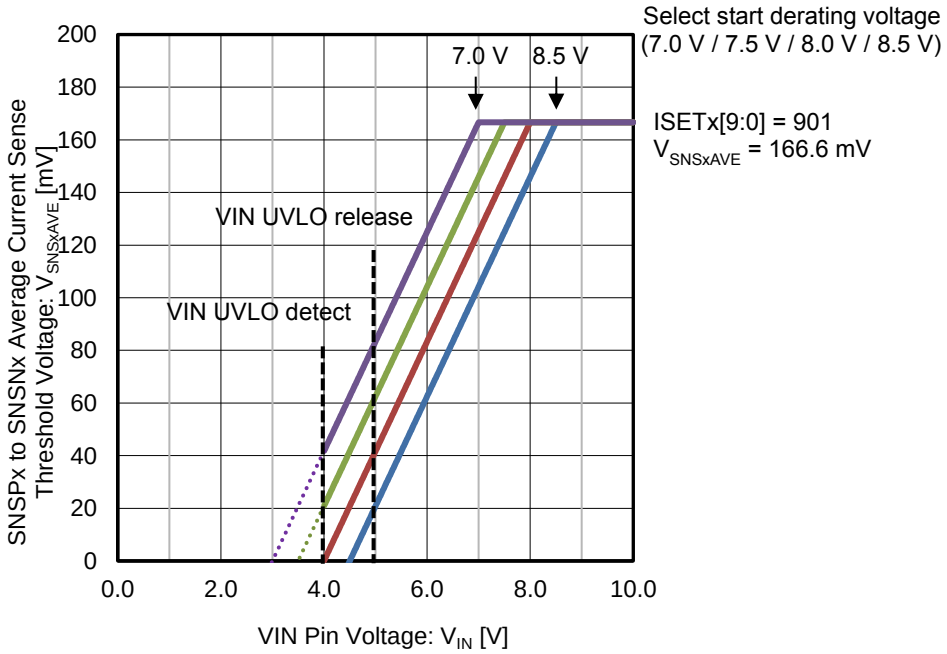


Figure 9. $V_{SNSxAVE}$ vs V_{IN} (Input Voltage Derating)
(ISETx[9:0] = 901, VINDGAINx[1:0] = 2)

7.2 VIN Pin, NTCx Pin and BINx Pin Dimming Setting - continued

The BINVALx set by the SPI register BINSELx[1:0] (See BIN table below).

BINx Pin Voltage [V]	BIN Rank	VREG5 Pin Voltage Divider Resistor Setting Example		BINSELx[1:0]			
		Upper Side [kΩ]	Lower Side [kΩ]	0	1	2	3 (initial)
4.375 - 5.000	7	1	20	0	30	60	120
3.750 – 4.375	6	4.7	20	0	20	40	80
3.125 – 3.750	5	9.1	20	0	10	20	40
2.500 – 3.125	4	15	20	0	0	0	0
1.875 – 2.500	3	24	20	0	-10	-20	-40
1.250 – 1.875	2	47	20	0	-20	-40	-80
0.625 – 1.250	1	91	20	0	-30	-60	-120
0.000 – 0.625	0	-	20	0	-40	-80	-160

Dimming example of the BINx pin:
Condition: ISETx[9:0] = 901 (initial), BINSELx[1:0] = 2

BINx Pin Voltage [V]	BIN Rank	ISETx[9:0]	BINSELx[1:0]	ISETDx[9:0]	$V_{SNSxAVE}$ [mV]
		901 (initial)	2	Calculation	
4.375 - 5.000	7	901	60	961	178.9
3.750 – 4.375	6		40	941	174.8
3.125 – 3.750	5		20	921	170.7
2.500 – 3.125	4		0	901	166.6
1.875 – 2.500	3		-20	881	162.6
1.250 – 1.875	2		-40	861	158.5
0.625 – 1.250	1		-60	841	154.4
0.000 – 0.625	0		-80	821	150.4

7.2 VIN Pin, NTCx Pin and BINx Pin Dimming Setting - continued

The thermal derating start voltage $V_{NTCSETx}$ set by the SPI register NTCSETx[7:0].

$$V_{NTCSETx} = \frac{NTCSET_x[7:0] + 1}{256} \times 2.5\ V$$

NTCSETx[7:0]	$V_{NTCSETx}$ [V]
127 (initial)	1.25
153	1.5
204	2.0
255	2.5

The thermal derating GAIN NTCGAINx set by the SPI register NTCGAINx[1:0].

NTCGAINx[1:0]	NTCGAINx	GAIN ($V_{SNSxAVE}$ / V_{NTCx}) [mV/V]
0	0	0.0
1	1	83.4
2 (initial)	2	166.8
3	4	333.7

Dimming example of NTCx pin:
Condition: BINSELx[1:0] = 0, NTCSETx[7:0] = 127 (initial), NTCGAINx[1:0] = 2 (initial)

NTCx Pin Voltage [V]	ISETx[9:0]	NTCSETx[7:0]	NTCGAINx[1:0]	ISETDx[9:0]	$V_{SNSxAVE}$ [mV]
	901 (initial)	127 (initial)	2 (initial)	Calculation	
		$V_{NTCSETx}$ [V]	NTCGAINx		
1.25	901	1.25	2	901	166.6
1.1				779	141.8
1.0				697	125.1
0.9				615	108.5
0.8				533	91.8
0.7				451	75.1
0.6				369	58.4

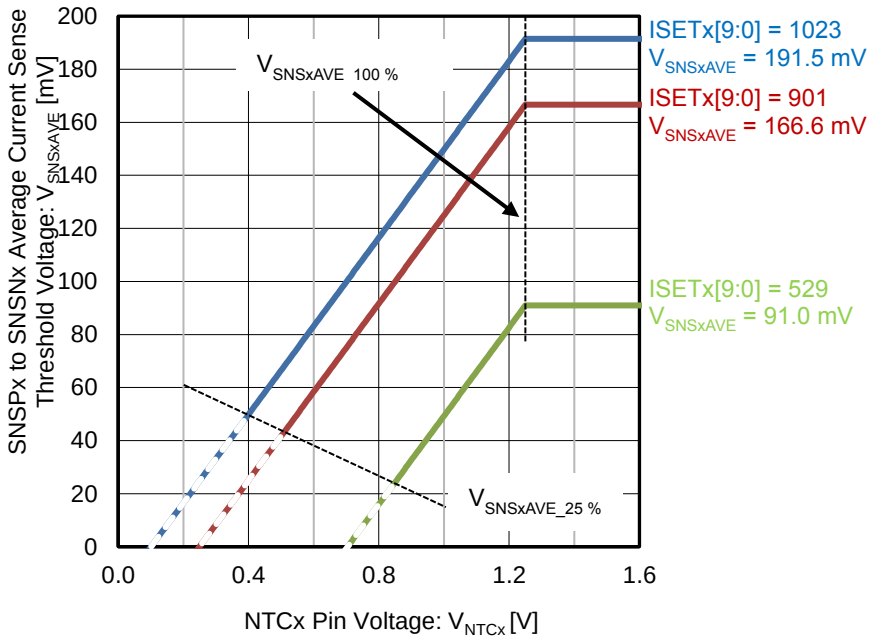


Figure 10. $V_{SNSxAVE}$ vs V_{NTCx} (Thermal Derating)
(NTCSETx[7:0] = 127, NTCGAINx[1:0] = 2)

Description of Blocks - continued

8 Enable Setting (the EN Pin, the MODE Pin)

8.1 Device Enable (the EN Pin)

The BD18354MUF-M can be enabled or disabled via the EN pin. When the EN pin is pulled low, the device is shutdown and the device's quiescent current is reduced to I_{INSTB}. In the shutdown state, the internal regulator is turned off and the registers are reset. When the voltage is ON and the EN pin increases beyond the voltage threshold of V_{EN}, two channels can be enabled. (Refer to "Start-up & Turn-off Sequence".)

When pulling up the EN pin to the power supply, be sure to connect it with a resistor of 10 kΩ or more. (If the adjacent pin is short-circuited, the power supply - GND will be short-circuited.)

8.2 Startup Mode Select (the MODE Pin)

The BD18354MUF-M can select startup sequence by the MODE pin H/L. When the MODE pin = L, CHx can be turned ON/OFF individually by the SPI signal. When the MODE pin = H, it starts up in EEPROM read operation. (Refer to "Start-up & Turn-off Sequence".)

8.3 Startup Model Select (the MSEL Pin)

When booting with EEPROM read operation, the data set to be read from the EEPROM can be specified by setting the MSEL pin voltage.

The table below shows the relationship between the MSEL pin voltage and the data set to be read. It also shows an example of the resistance value connected to the VREG5 pin voltage.

MSEL Pin Voltage [V]	Data Set	VREG5 Pin Voltage Divider Resistor Setting Example	
		Upper Side [kΩ]	Lower Side [kΩ]
4.375 - 5.000	7	1.0	20
3.750 – 4.375	6	4.7	20
3.125 – 3.750	5	9.1	20
2.500 – 3.125	4	15.0	20
1.875 – 2.500	3	24.0	20
1.250 – 1.875	2	47.0	20
0.625 – 1.250	1	91.0	20
0.000 – 0.625	0	-	20

Description of Blocks - continued

9 Soft Start (SSDAC)

For soft-start to reduce rush charge output current, a programmed soft-ramp-up reference voltage (V_{DCDIMx}) or a soft-ramp-up the COMPx pin voltage by more compensation capacitor (C_{COMPx}) can be used. The COMPx pin voltage clamped by SSDAC output until the LED current or the output voltage approaches the regulation threshold. The soft-start is controlled with a 10bit DAC which ramps from 0 V to 2.5 V during startup of an associated channel. The rate of the soft-start ramp (or the ramp time) can be controlled by programming the clock of the internal digital ramp counter. When the soft-start is completed, the internal SSENDx signal becomes H.
Set SSSETx[2:0] when CHONx = 0.

Programmable soft-output-start can be calculated by the following formula.

$$t_{SSx} = \frac{ISETx[9:0] \times SS_{DIVx}}{f_{SWx}} \text{ [s]}$$

Where:
f_{SWx} is the switching frequency set by the SPI register FRT[3:0] and the external resistor (R_{RT}).
SS_{DIVx} is the is a division factor provided in soft-start register.

SSSETx[2:0]	SS_{DIVx}
0	Disabled
1	1
2 (initial)	2
3	4
4	6
5	12
6	24
7	36

t_{SSx}									
SSSETx[2:0]	ISETx[9:0]	f_{SWx}							[kHz]
		100	200	300	400	500	1000	2200	
0	901 (initial)	-	-	-	-	-	-	-	[ms]
1		9.0	4.5	3.0	2.3	1.8	0.9	0.4	
2 (initial)		18.0	9.0	6.0	4.5	3.6	1.8	0.8	
3		36.0	18.0	12.0	9.0	7.2	3.6	1.6	
4		54.1	27.0	18.0	13.5	10.8	5.4	2.5	
5		108.1	54.1	36.0	27.0	21.6	10.8	4.9	
6		216.2	108.1	72.1	54.1	43.2	21.6	9.8	
7		324.4	162.2	108.1	81.1	64.9	32.4	14.7	

Set the soft-start time longer than the time required to charge the output capacitor. The soft-start time is counted up only the PWM dimming signal = H section. The count value is retained in the PWM dimming signal = L section.

Description of Blocks - continued

10 Switching Frequency Setting (OSC)

The BD18354MUF-M has the OSC circuit generating an adjustable frequency f_{SW} set by the SPI. The switching frequency is set by the SPI register FRT[3:0] and an external resistor (R_{RT}).
With a clock signal input to the SYNC pin, the internal oscillation frequency can be synchronized externally. Input a 50 % duty external input frequency with less than ±20 % of internal oscillating frequency set by the RT pin resistance. When PHSHFT = 0 is set, the falling edge of the clock input to the SYNC pin is synchronized with the oscillation frequency. When PHSHFT = 1 is set, the falling edge of the clock input to the SYNC pin is synchronized with the oscillation frequency of CH1, and the rising edge is synchronized with the oscillation frequency of CH2.
Since OSC signal dropout occurs when switching operations, it is recommended that switching between internal OSC and SYNC operations be performed with CHONx = 0.
For SYNC operation, set SSFM[2:0] = 0.

$$f_{SW} \approx \frac{(FRT[3:0]+1)\times k}{R_{RT}} \quad , \qquad (k = 3125 \times 10^6)$$

*Only the range from 100 kHz to 2.25 MHz can be set.

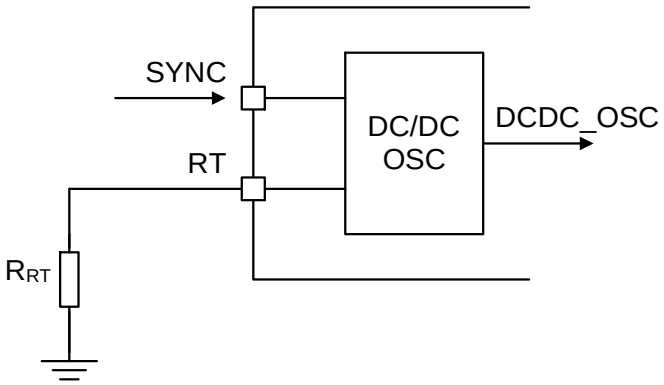


Figure 11. DC/DC OSC Setting by the SYNC and RT Pins

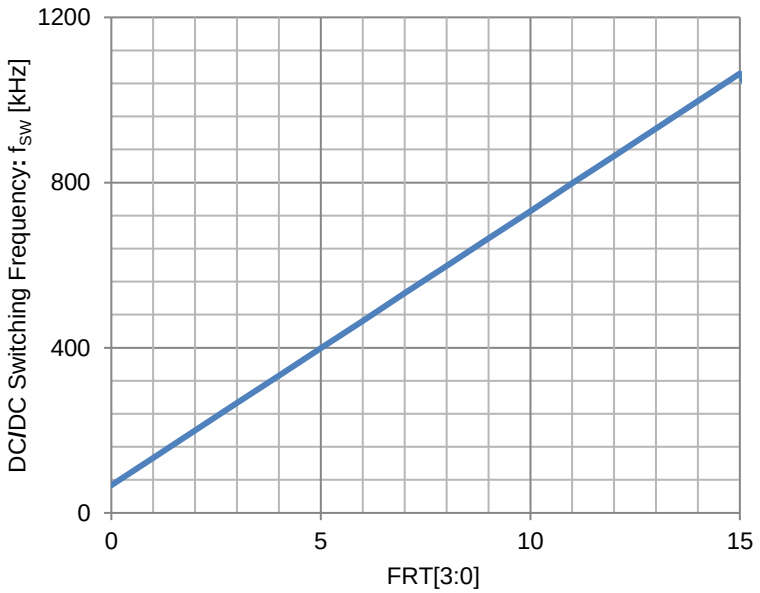


Figure 12. DC/DC Switching Frequency: f_{SW} vs FRT[3:0] (R_{RT} = 47 kΩ)

10 Switching Frequency Setting (OSC) – continued

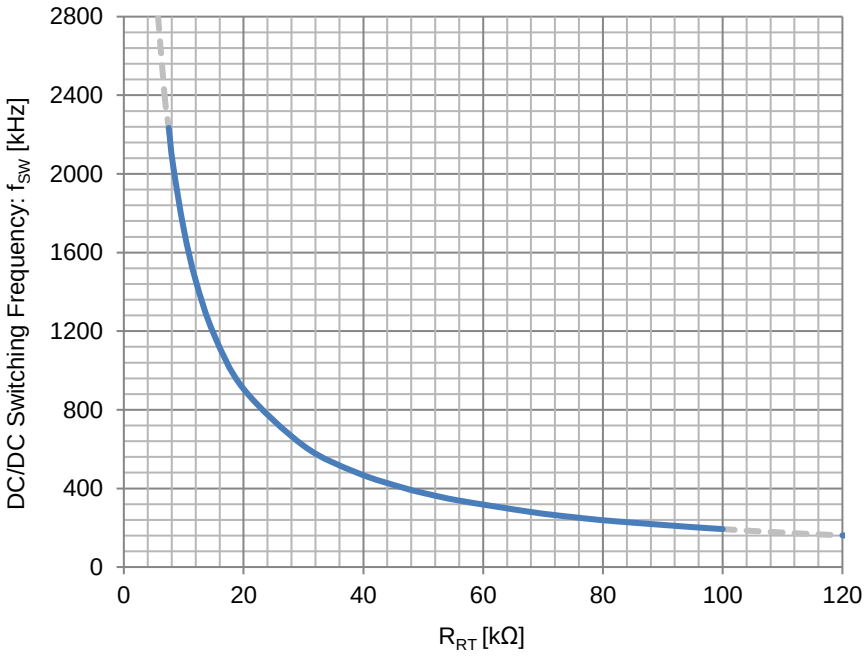


Figure 13. DC/DC Switching Frequency: f_{SW} vs R_{RT} (FRT[3:0] = 5)

Table 1. DC/DC Frequency Setting (R_{RT} = 47 kΩ)

FRT (Dec)	DC/DC Frequency [kHz]
0	68
1	133
2	200
3	261
4	336
5 (initial)	399
6	460
7	522
8	588
9	648
10	710
11	768
12	840
13	899
14	956
15	1014

10 Switching Frequency Setting (OSC) – continued

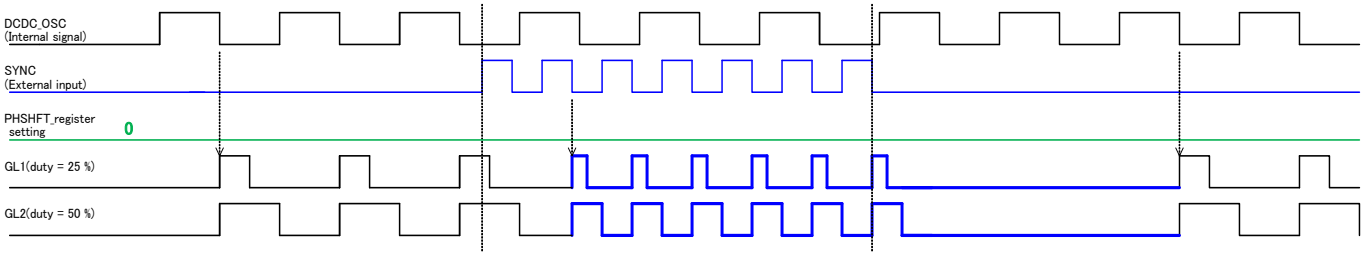


Figure 14. SYNC Operation Waveforms 1

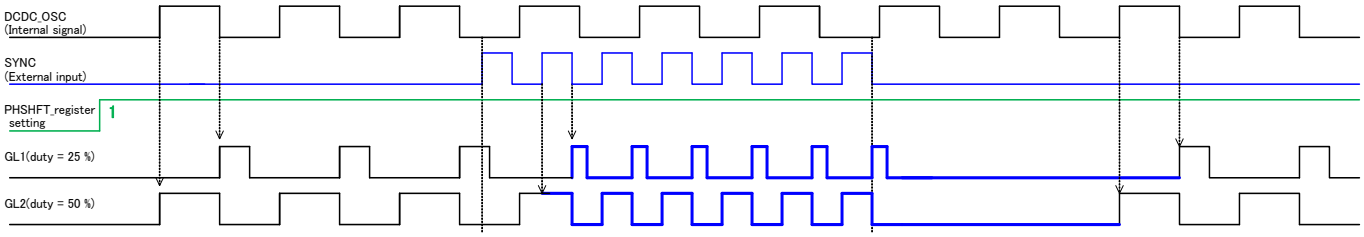


Figure 15. SYNC Operation Waveforms 2

Description of Blocks - continued

11 Spread Spectrum Frequency Modulation (SSFM)

The BD18354MUF-M has a built-in spread spectrum function and the modulation switching frequency is $\pm f_{SSFMW}$ % around the set frequency f_{SWx}. The spread spectrum modulation frequency and the modulation width f_{SSFMW} can be programmable by the register SSFM [2:0] and SSFMW [1:0]. When SSFM [2:0] is set to 0, spread spectrum modulation is not applicable. When enable the SSFM function, all channels operate at the same modulation frequency (f_{SSFM}).
During SYNC operation, this function is disabled, so set SSFM[2:0] = 0.

SSFM[2:0]	f_{SSFM} [Hz]
0	SSFM Not applicable
1	64
2	128
3	257
4 (initial)	506
5	1044
6	2204
7	3968

SSFMW[1:0]	f_{SSFMW} [%]
0	0
1 (initial)	5
2	10
3	15

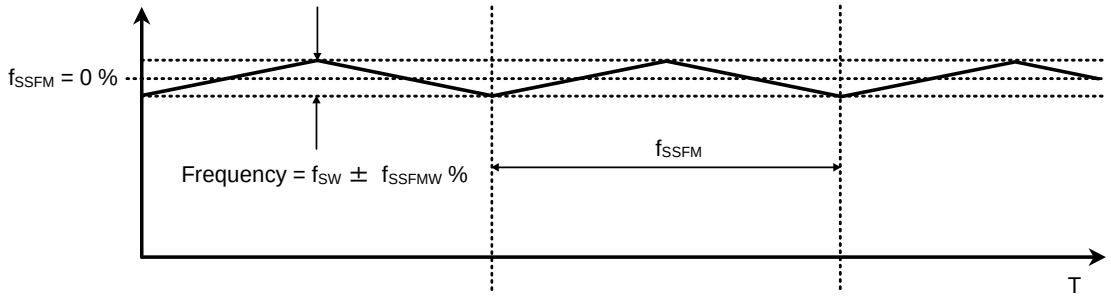


Figure 16. Spread Spectrum

Description of Blocks - continued

12 Protection Function

12.1 Power On Reset (POR)

The BD18354MUF-M has a POR circuit monitoring the input power supply V_{REG5}. When POR is detected, all internal circuits and logic registers will be initialized. The POR circuit's main purpose is internal logic initialized in POR condition by reset signal. Between the POR detection threshold and UVLO detection threshold by the VREG5 pin, internal register values will not be reset.

12.2 Under Voltage Lock Out (UVLO)

UVLO is a protection circuit that prevents IC malfunction at power-ON or power-OFF.
When the VIN pin voltage becomes V_{INUVD} or less, the VREG5 pin voltage becomes $V_{REG5UVD}$ or less, or the VDRV7 pin voltage becomes $V_{DRV7UVD}$ or less, the PDRVx pin outputs high level to turn off external P-ch MOSFET. DC/DC is stopped and GLx outputs low level.

12.3 Thermal Shutdown (TSD)

In case of a TSD as Tj > 175 °C (Typ), all the buck DC/DC converters will be disable immediately and all internal circuits and logic registers will be initialized. When TSD recovered at Tj < 150 °C (Typ), the DC/DC converters will be in the SPI state until start-up sequence trigger occurs.

12.4 Over Current Protection (OCP)

When the CSx pin voltage becomes V_{CSOCPx} or more, over current is detected and the GLx pin outputs low until the next switching cycle. Also, if OCP is detected 8 times under the condition that COMPx pin voltage exceeds V_{CSLOW} + slope compensation voltage, the device will be in hiccup mode (automatic recovery switching off). In the hiccup mode, the PDRVx pin outputs high level to turn off the external P-ch MOSFET. DC/DC stops and GLx outputs low level. FAULT_Bx outputs low level and outputs error detection. The device restart after hiccup time (t_{HICCUP}) elapses.
The OCP detection current (I_{OCPx}) is set by the following formula.

$$I_{OCPx} = \frac{V_{CSOCPx}}{R_{CSx}} \quad [A]$$

Where:
V_{CSOCPx} is the OCP detection voltage set by the OCPSETx[1:0] register.
R_{CSx} is a resistor connected to the CSx pin.

The OCP detection voltage (V_{CSOCPx}) is set by the following table.

OCPSETx[1:0]	V_{CSOCPx} [mV]
0	100
1 (initial)	150
2	200
3	300

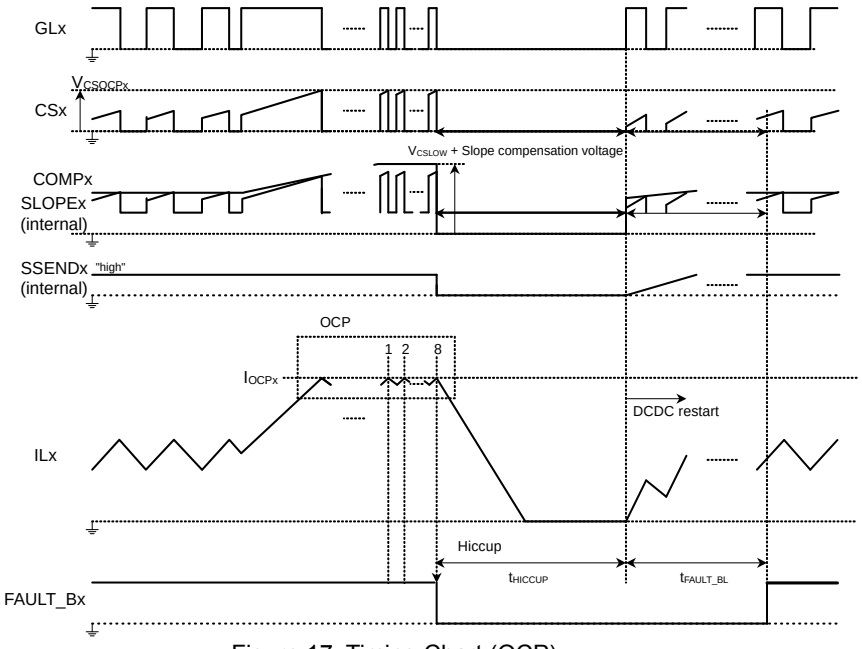


Figure 17. Timing Chart (OCP)

12 Protection Function - continued

12.5 Short Circuit Protection (SCP)

When the anode of the LED is shorted to GND, the voltage between the SNSPx pin and the SNSNx pin can be monitored and protected by SCP.
When the voltage between the SNSPx pin and the SNSNx pin become $V_{SNSxSCP}$ or more, SCP is detected after SCP delay time (t_{SCPDLY}). The detection voltage ($V_{SNSxSCP}$) is set 330 mV.

When SCP is detected, the PDRV pin outputs high level to turn off the external P-ch MOSFET. DC/DC stops and GL outputs low level. FAULT_B outputs low level and outputs error detection.
Restart after hiccup time (t_{HICCUP}) elapses. If the anode of the LED is shorted to GND, the SCP is detected again and the operation is repeated. FAULT_B holds low output until t_{FAULT_BL} after restart.

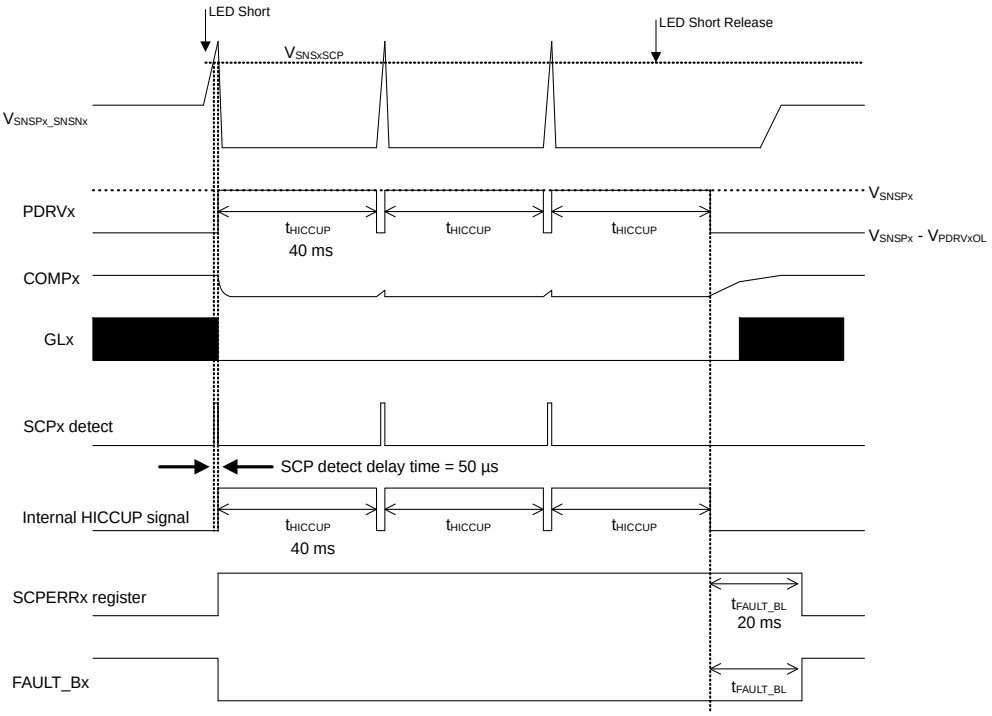


Figure 18. Timing Chart (SCP)

When the anode of the LED is shorted to GND, the voltage between the SNSP pin and the SNSN pin may exceed the absolute voltage. It is recommended to insert a PNP transistor as shown below figure and clamp the voltage.
Design to take full consideration of power dissipation of R_{SNSx} and P-ch MOSFET.

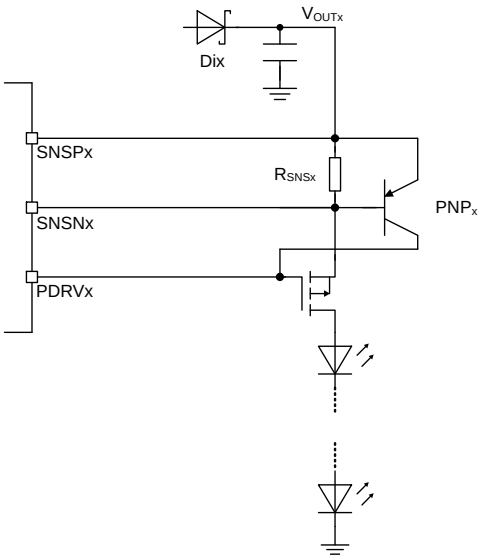


Figure 19. PNP Clamp Setting Circuit

12 Protection Function - continued

12.6 Over Voltage Protection (OVP)

OVP is detected when the SNSPx pin voltage becomes V_{OVPx} or more. The detection voltage (V_{OVPx}) is set by the following formula.

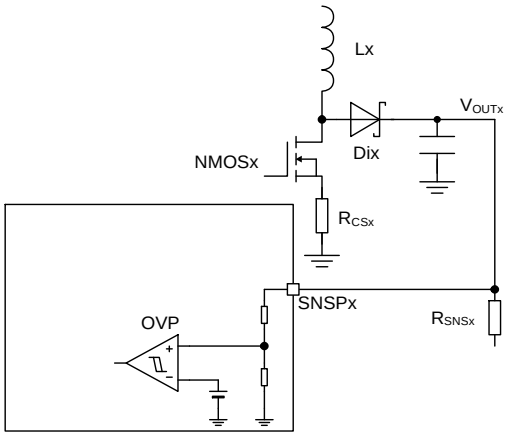


Figure 20. OVP Circuit

$$V_{OVPx} = OVPSET[3:0] \times 2.18 + 34.8\ [V]$$

OVPSETx[3:0]	V_{OVPx} [V]	OVPSETx[3:0]	V_{OVPx} [V]
0	34.80	8	52.24
1	36.98	9	54.42
2	39.16	10	56.60
3	41.34	11	58.78
4	43.52	12	60.96
5	45.70	13	63.14
6	47.88	14	65.32
7	50.06	15 (initial)	67.50

When OVP is detected, the PDRVx pin outputs high level to turn off the external P-ch MOSFET. DC/DC stops and GLx outputs low level. FAULT_Bx outputs low level and outputs error detection.
OVP has hysteresis ($V_{OVPxHYS}$ = 1.6 V typ), and when the SNSPx pin voltage becomes V_{OVPx} - $V_{OVPxHYS}$ or less, DC/DC restarts. When the LED is open, OVP is detected again and the OVP detection operation is repeated.
When OVP is released and the voltage between the SNSPx pin and the SNSNx pin becomes V_{SNSxSG} (LED Status Good Threshold Voltage) or more, FAULT_Bx outputs high level. FAULT_Bx holds low output until t_{FAULT_BL} elapses after OVP is released.

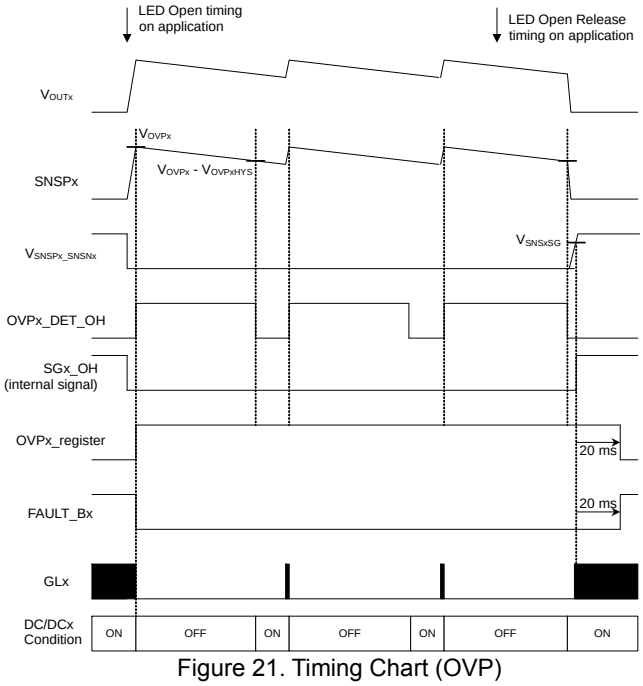


Figure 21. Timing Chart (OVP)

12 Protection Function - continued

12.7 External Over Voltage Protection (EOVP)

When EOVPx/SSUx = 0 (initial setting), OVP voltage can be set by dividing resistors R_{EOVPx1}, R_{EOVPx2} connected between DC/DC output and GND. LED open failure can also be detected by the OVP function.

The detection voltage V_{OUT_EOVPx} is set by the following formula.

$$V_{OUT\_EOVPx} = \frac{R_{EOVPx1} + R_{EOVPx2}}{R_{EOVPx2}} \times V_{EOVPx} \quad [V]$$

Where:

V_{EOVPx} is the external over voltage protection detect voltage = 2.50 V (Typ).

The timing chart for detection is the same as for OVP.

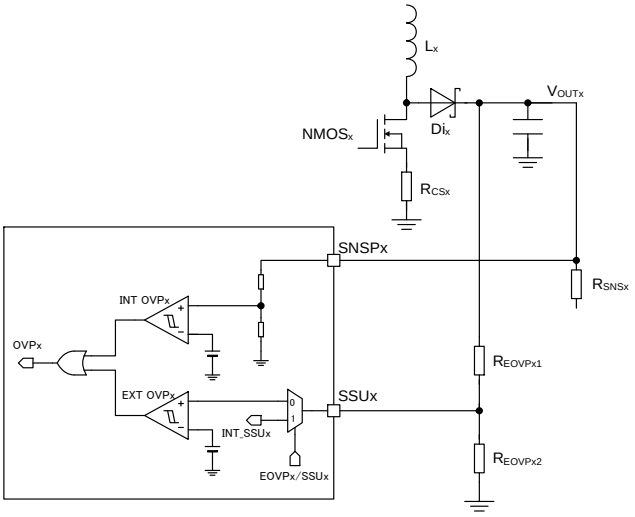


Figure 22. External OVP Setting Circuit

12.8 Under Voltage Detection (UVD)

When EOVPx/SSUx = 1 UVD is detected when the SNSNx pin voltage become V_{UVD} or less.

The UVD detection voltage V_{UVD} and the UVD release voltage V_{UVR} set by BTBx register. If BTBx is set to “0” in the BTBx register, the UVD detection voltage V_{UVDx1} = 0.6 V (Min). The UVD release voltage V_{UVRx1} = 2.2 V (Max). If BTBx is set to “1” in the BTBx register, the UVD detection voltage V_{UVDx2} = 13.6 V (Min). The UVD release voltage V_{UVRx2} = 15.2 V (Max).

UVD is monitored when the voltage between the SNSPx pin and the SNSNx pin becomes V_{SNSxSG} or more in the ON section of PWM dimming. After detection the internal counter starts. When the voltage between the SNSPx pin and the SNSNx pin becomes V_{SNSxSG} or more in the ON section of PWM dimming, it counts up. When the total time reaches t_{UVD}, the FAULT_Bx outputs becomes Low.

After UVLO, TSD, SCP, OVP is released or after EN = H input, until t_{UVD} has elapsed, UVD does not be detected.

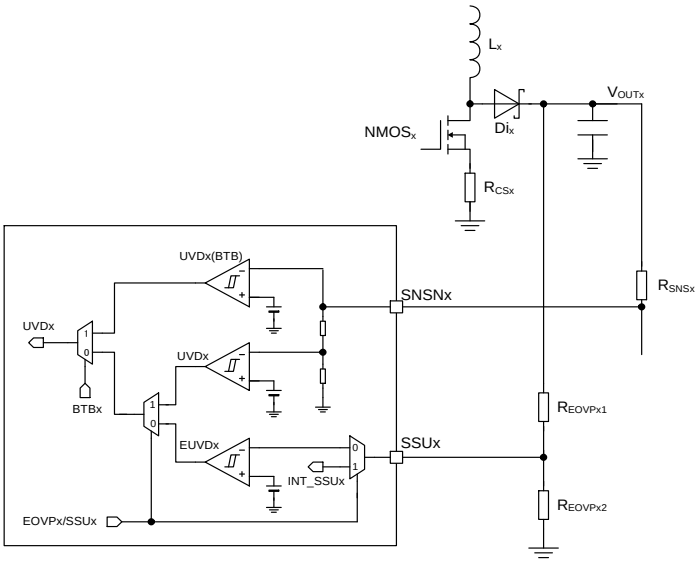


Figure 23. UVD Setting Circuit

12.8 Under Voltage Detection (UVD) - continued

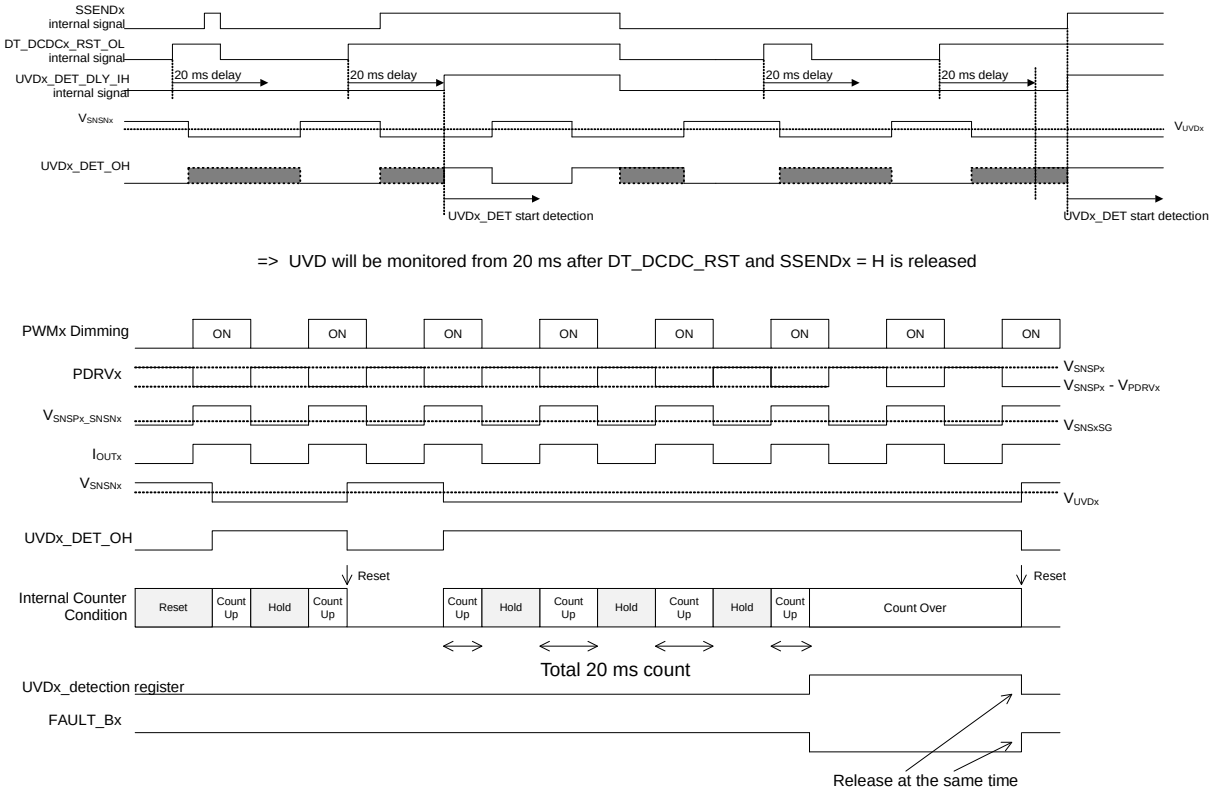


Figure 24. Timing Chart (UVD)

When the LED is short-circuited during lighting in the Buck-Boost topology, etc., SCP operates at first and hiccup operation occurs, and UVD may be detected 20 ms (Typ) after the SCP detection release condition. In this case, the FAULT_Bx signal will output FAULT_Bx = L when SCP is detected, FAULT_Bx = H when SCP is released, and FAULT_Bx = L again when UVD is detected 20 ms later or later. FAULT_Bx = L output is held until the UVD condition is released.

12.9 External Under Voltage Detection (EUVD)

When EOVPx/SSUx = 0 setting, EUVD is enabled instead of UVD.

EUVD voltage can be set by dividing resistors R_{EOVPx1}, R_{EOVPx2} connected between DC/DC output and GND. This function is effective when the SNSNx pin voltage = 7.1 V or less.

The detection voltage (V_{OUT_EUVDx}) is set by the following formula.

$$V_{OUT\_EUVDx} = \frac{R_{EOVPx1}+R_{EOVPx2}}{R_{EOVPx2}} \times V_{EUVDx} \quad [V]$$

Where:

V_{EUVDx} is the external under voltage detect voltage = 185 mV (Typ).

The settings and operation regarding BTBx and the timing chart for detection are the same as for UVD.

When the state is shifted to the STAND-ALONE state with the CSB pin = "L" input held, it is recognized as the BTB1 register "0" setting when the SCL pin < 0.6 V, the BTB1 register "1" setting when the SCL pin > 2.2 V, the BTB2 register "0" setting when the SDA pin < 0.6 V, the SDA pin > 2.2 V, the BTB2 register is set to "1".

State	The CSB Pin	The SCL Pin	The SDA Pin	BTB1	BTB2
STAND-ALONE	L	L	L	0	0
		L	H	0	1
		H	L	1	0
		H	H	1	1
	H	EEPROM operation	EEPROM operation	X	X
Others	X				

Description of Blocks - continued

13 Outputs Abnormal Status (FAULT_Bx)

The following table summarizes the device's behavior under fault condition.

Abnormal detection / protection function

In BD18354MUF-M, the OCP and SCP faults can be configured to be a non-latched fault in OCPLATx, and SCPLATx register. If a fault is configured as non-latched, upon occurrence of the fault, the associated channel turns off. The channel performs a soft-start after expiration of a configurable fault timer and when the fault is cleared. In latched fault condition, the associated channel is turned off and remains off until the channel enable-bits are reprogrammed in the EN register.

Detection / Protection Function	Detecting Condition (all the value is typical)		Description in Detecting			
	Detection	Release	DC/DC	Register	ADC	FAULT_Bx Output STAND-ALONE
VREG5 POR	V_{REG5} ≤ 2.7 V	V_{REG5} ≥ 2.9 V	GLx = L PDRVx = H COMPx discharged	All registers initialized	Not Available	Hiz
VIN UVLO	V_{IN} ≤ 4.1 V	V_{IN} ≥ 4.5 V	VREG5 off VDRV7 off CHONx = 0 GLx = L PDRVx = H COMPx discharged	UVLO bit is set in the status register	Not Available	Hiz
VDRV7 VREG5 UVLO	V_{DRV7} ≤ 4.1 V V_{REG5} ≤ 4.1 V	V_{DRV7} ≥ 4.5 V V_{REG5} ≥ 4.2 V	CHONx = 0 GLx = L PDRVx = H COMPx discharged	UVLO bit is set in the status register	Not Available	Hiz
Thermal Shutdown (TSD)	Tj > 175 °C	Tj < 150 °C	VREG5 off VDRV7 off GLx = L PDRVx = H COMPx discharged	All registers initialized	Not Available	L
Over Current Protection (OCP)	CHONx = 1 V_{CSx} ≥ 0.15 V	V_{CSx} < 0.15 V	GLx = L	-	Available	L
	CHONx = 1 V_{CSx} ≥ 0.15 V V_{COMPx} ≥ V_{CSHIGH} t_{CSOCP} = 8 SSENDx = H	V_{CSx} < 0.15 V	GLx = L PDRVx = H COMPx discharged with hiccup time (40 ms)	Corresponding the OCPERRx bit is set in the status register	Available	L
Short Circuit Protection (SCP)	CHONx = 1 V_{SNSx} ≥ $V_{SNSxSCP}$	V_{SNSx} < $V_{SNSxSCP}$	GLx = L PDRVx = H COMPx discharged with hiccup time (40 ms)	Corresponding the SCPERRx bit is set in the status register after 50 µs counts	Available	L
Over Voltage Detection (OVP)	CHONx = 1 V_{SNSNx} ≥ 7.4 V and V_{SNSPx} ≥ V_{OVPx} or V_{SSUx} ≥ 2.500 V (EOVPx/SSUx = 0)	CHONx = 1 PWMx = H and V_{SNSPx} ≤ V_{OVPx} - $V_{OVPxHYS}$ or V_{SSUx} ≤ 2.435 V (EOVPx/SSUx = 0)	GLx = L PDRVx = H	Corresponding the OVPERRx bit is set in the status register	Available	L

(Note) The setting becomes effective after UVLO is released. V_{CSHIGH} = V_{CSLOW} + slope compensation voltage.

13 Outputs Abnormal Status (FAULT_Bx) - continued

Detection / Protection Function	Detecting Condition (all the value is typical)		Description in Detecting			
	Detection	Release	DC/DC	Register	ADC	FAULT_Bx Output STAND-ALONE
Under Voltage Detection (UVD)	CHONx = 1 PWMx = H V_{SNSNx} ≤ 7.1 V and V_{SSUx} ≤ 0.185 V (EOVPx/SSUx = 0) or V_{SNSNx} ≤ V_{UVDx1} (BTBx = 0) (EOVPx/SSUx = 1) or V_{SNSNx} ≤ V_{UVDx2} (BTBx = 1)	CHONx = 1 PWMx = H and V_{SSUx} ≥ 0.250 V (EOVPx/SSUx = 0) or V_{SNSNx} ≥ V_{UVRx1} (BTBx = 0) (EOVPx/SSUx = 1) or V_{SNSNx} ≥ V_{UVRx2} (BTBx = 1)	-	Corresponding the UVDERRx bit is set in the status register after 20 ms counts	Available	L

(Note) The setting becomes effective after UVLO is released.

Protection setting table

Protection		Error Control Register			Error Control		
NAME	Symbol	Latch	Error Clear	FAULT_B Output Enable	System	Status Register	FAULT_Bx
Power On Reset	POR	-	-	-	Reset	-	Hiz
UVLO	UVLO	-	-	FLTBEN[0]	-	UVLO	L
Thermal Shutdown	TSD	-	-	-	Reset	-	L
CHx Over Current Protection	OCP	Selected by OCPLATx	FLTRSTx	FLTBEN[1]	-	OCPERRx	L
CHx Short Circuit Protection	SCP	Selected by SCPLATx	FLTRSTx	FLTBEN[2]	-	SCPERRx	L
CHx Over Voltage Protection	OVP	-	-	FLTBEN[3]	-	OVPERRx	L
CHx Under Voltage Detection	UVD	-	-	FLTBEN[4]	-	UVDERRx	L
CRC Error for SPI	SPICRCERR	Initial	FLTRSTx	-	-	SPICRCERR	L
Watch Dog Timer for SPI	WDTERR	Initial	FLTRSTx	-	-	WDTERR	L
CRC Error for I2C	I2CCRCERR	Initial	FLTRSTx	-	-	I2CCRCERR	L

"x" – x = 1,2 for channel.
"-" – This protection does not have this function.
"Status register" – If there are two registers, both registers are updated. This protection does not have effect on this output.

When POR or TSD is detected, it is not possible to detect other protection.

Description of Blocks - continued

14 A/D Monitor Channel Select

The following table is A/D monitor setting table.
The data in register is updated to the newest data immediately when the new data is written.
Do not set VMONSEL and read AD values at the same time.
Read AD values after VMONSEL setting is completed.

bit[3:0] VMONSEL[3:0]
VMON register is shared in for monitoring below node. This register should be programmed before reading VMON register when target node voltage is need.

Table 2. VMONSEL Status

VMONSEL	Monitor Node
0 (initial)	Thermal
1	V_{IN}
2	V_{SNSN1}
3	V_{ISNS1}
4	V_{SNSN2}
5	V_{ISNS2}
6	Not Used
7	Not Used
8	V_{BIN1}
9	V_{BIN2}
10	V_{NTC1}
11	V_{NTC2}
12	V_{MSEL}
13	V_{INDIM} (for VIN dimming)

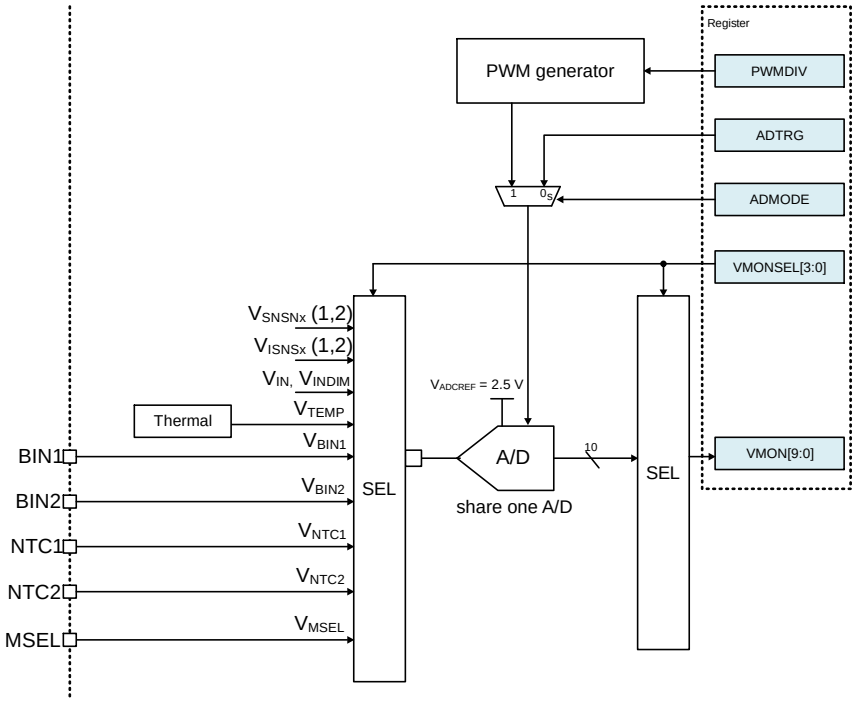


Figure 25. A/D System Structure

Description of Blocks - continued

15 State Machine

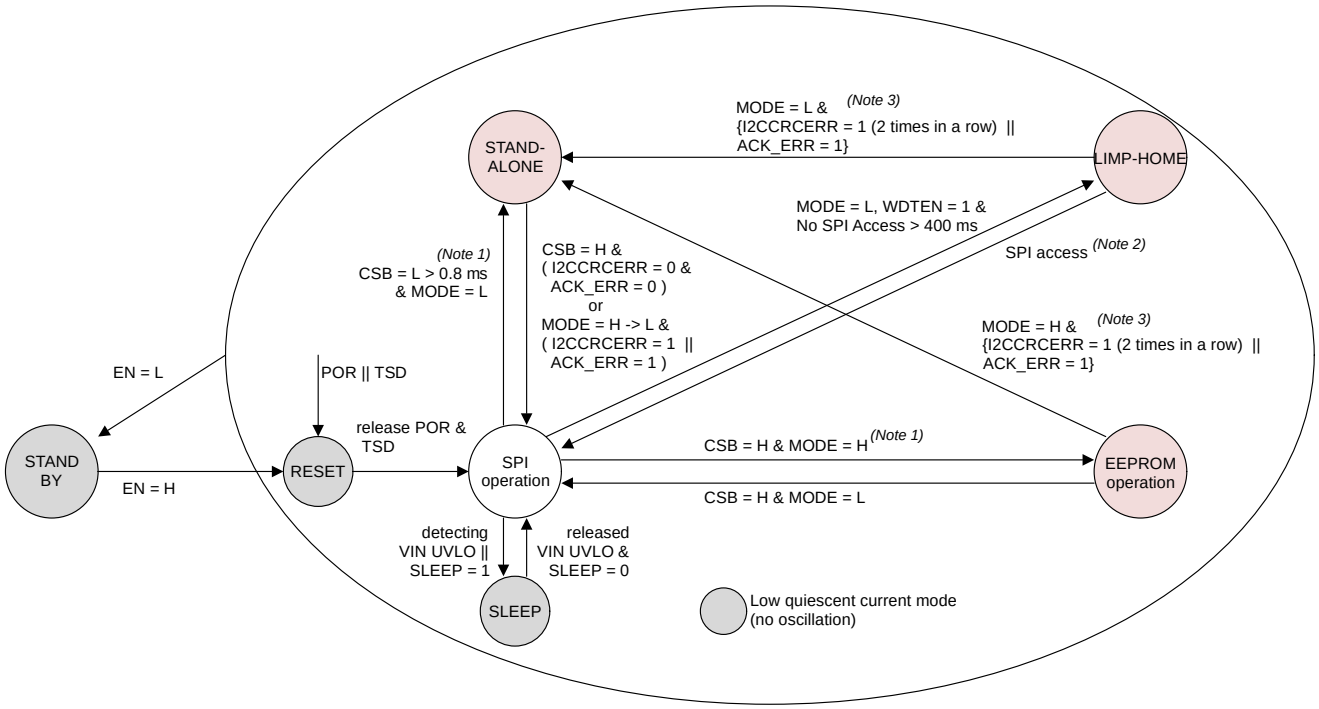


Figure 26. State Machine

(Note 1) To avoid SPI communication malfunction, be sure to apply CSB = H when SPI communication control is not performed.
(Note 2) During this SPI access, the state only transitions from the LIMP-HOME state to the SPI state. The register value is not updated.
(Note 3) ACK_ERR asserts high (ACK_ERR = 1) when follower address did not ACK during I2C EEPROM read operation. ACK_ERR is cleared when SWRST = 1 or FLTRSTx = 1.

Table 3. State Machine Description

State	Quiescent Current	LED Lighting	Description
STAND BY	Low	OFF	The internal regulators are turned off and all internal block is initialized
RESET	Low	OFF	All internal block is initialized
SPI Operation	Normal	Lighting (Programmed by SPI)	Dimming is programmed by the SPI setting. A/D conversion is available.
SLEEP	Low	OFF	Keep Low quiescent current until SLEEP = 0. All register value are kept (not initialized). Set to SLEEP mode with CHONx = 0.
EEPROM Operation	Normal	Lighting (Programmed by external EEPROM)	This IC loads data from EEPROM to register in this state. SPI is not accepted in this state. State is changed to “SPI operation” after setting CHONx = 0 when MODE = H -> L. If this IC detects CRC error two times with EEPROM, state is changed to “STAND-ALONE”.
LIMP-HOME	Normal	Lighting (Programmed by external EEPROM)	This IC loads data from EEPROM to register in this state. While loading data from the EEPROM, the IC performs CHONx = 0 control. State is changed to “SPI operation” when SPI access and CRC are OK. The SPI command when state returns is not reflected. If this IC detects CRC error two times with EEPROM, state is changed to “STAND-ALONE”.
STAND-ALONE	Normal	Lighting (Programmed by external resistor)	When MODE = L and CSB = L for 0.8 ms, this IC keeps lighting by external resistor setting. Protection can be checked by monitoring FAULT_B1/FAULT_B2 = L.

Description of Blocks - continued

16 SPI Protocol and AC Electrical Characteristics

This IC can be accessed via the SPI using the CSB, SCK, SI and SO pins as shown below.

CSB – Chip Select
SCK – Serial Clock
SI – Serial Data Input
SO – Serial Data Output

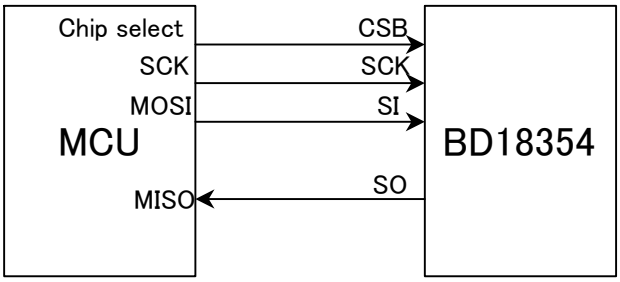


Figure 27. MCU Connection

Select the IC to be accessed by setting the CSB to low. Send the data based on the format as shown below figure. Data to be sent follow a MSB first 24-bit data format for write: 1-bit RW (read or write), 7-bit register address, 8-bit register data (to be written) and 8-bit CRC. The SPI can be accessed in daisy chain connection or parallel connection. There is no multiple bytes write/read feature. After each command, fix SI to low and CSB to high. SI data is output with 24 bits shift from SO. Pull up the CSB pin to H voltage when booting using the EEPROM or when not using the SPI communication function.

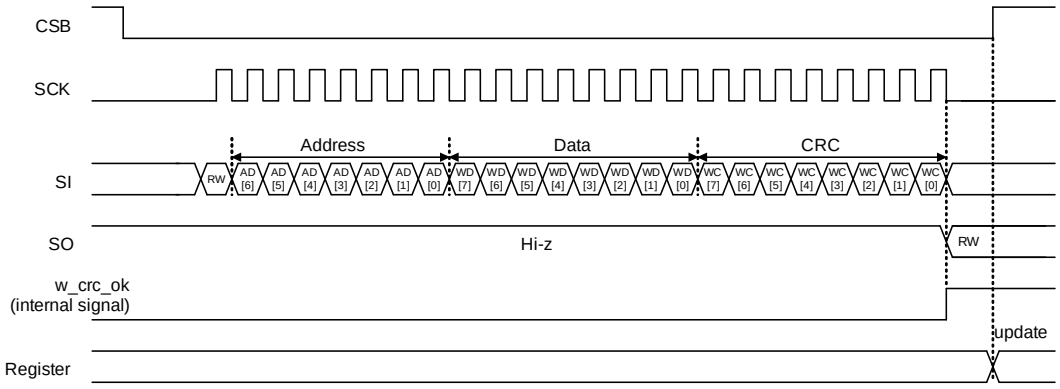


Figure 28. Data Format (Write)

16 SPI Protocol and AC Electrical Characteristics - continued

Read command data format is sent as follows: 1-bit RW, 7-bit register address, fixed 0xFF for register data and 8-bit CRC.
When CRC is OK (w_crc_ok = high) after the Read command as shown below, it is necessary to toggle CSB (low -> high -> low) to store the read data.
To output the data, it is necessary to send 24-bit High input data (Dummy Data).
MCU must calculate CRC using 0 as initial value.
For input data: use 16-bit data for calculation. 16-bit data = (RW, Address[6:0], Data[7:0])
For output data: use 15-bit data for calculation.
<RDMODE = 0> 15-bit data = (Address[6:0], Data[7:0]) Not including MSB.
<RDMODE = 1> 15-bit data = (5-bit (blank data), Data0[7:0], Data1[1:0]) Not including MSB.

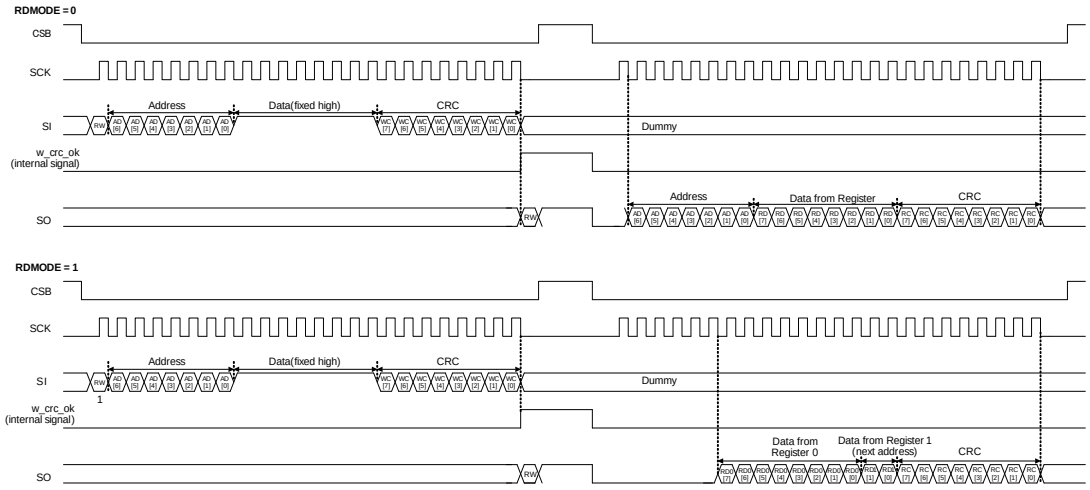


Figure 29. Data Format (Read)

16 SPI Protocol and AC Electrical Characteristics - continued

SPI AC Timing

SPI AC characteristics are as shown below.

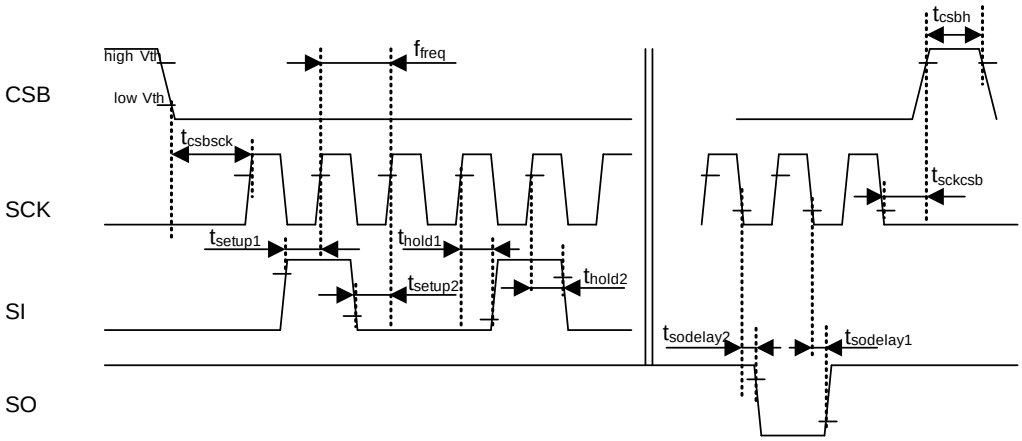


Figure 30. SPI AC Timing

Table 4. SPI AC Timing

Recommended Operation Condition

(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Item	Symbol	Unit	Min	Typ	Max
SPI Frequency	f_{freq}	MHz	0.1	-	2.0
CSB - SCK Timing	t_{csbSCK}	ns	1,000	-	-
SCK - CSB Timing	t_{SCKcsb}	ns	500	-	-
Setup Time1 (low -> high)	t_{setup1}	ns	200	-	-
Setup Time2 (high -> low)	t_{setup2}	ns	200	-	-
Hold Time1 (low -> high)	t_{hold1}	ns	200	-	-
Hold Time2 (high -> low)	t_{hold2}	ns	200	-	-
SO Delay (low -> high)	$t_{sodelay1}$	ns	-	-	200
SO Delay (high -> low)	$t_{sodelay2}$	ns	-	-	200
CSB High Pulse	t_{csbh}	ns	1,000	-	-

(Output load capacitance: 15 pF)

16 SPI Protocol and AC Electrical Characteristics - continued

SPI Protocol

Write/Read, Address

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RW	AD[6:0]						

Bit	Parameter	Function
AD[6:0]	Register Address	0x00 to 0x1A, 0x20

Note: There is no access to addresses that are not between the specified range.

Bit	Parameter	Function
RW	Read/Write	0: read access 1: write access

Data

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WD/RD[7:0]							

Bit	Parameter	Value
WD/RD [7:0]	Data of Write/Read	0x00 to 0xFF

CRC

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
WC/RC[7:0]							

Bit	Parameter	Value
WC/RC [7:0]	CRC Data of Write/Read	0x00 to 0xFF

This IC has a CRC (cyclic redundancy check) function for detecting errors in the SPI communication.
CRC for write command is calculated using RW bit, 6-bit register address and 8-bit register data and is calculated MSB first.
Read output is calculated the same.
CRC formula is" $x^8+x^5+x^4+1$" which is translated as the circuit as shown below. Initial value of CRC is 0x00.

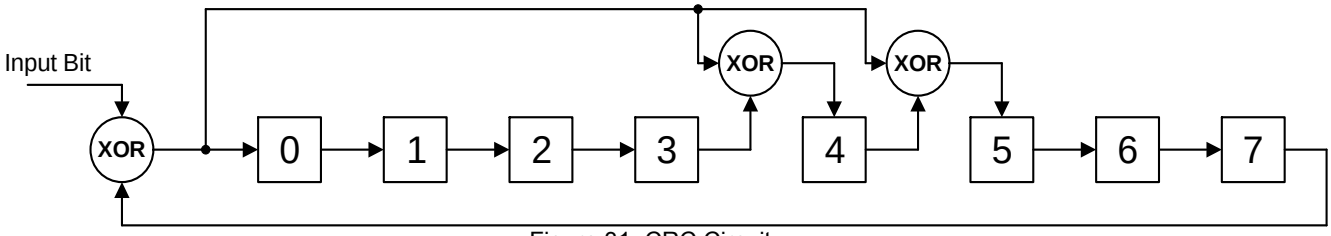


Figure 31. CRC Circuit

16 SPI Protocol and AC Electrical Characteristics - continued

NOTE (SPI Restrictions):
Command with the following input is not valid RW = 0, Address = 0x00, Data = 0x00, CRC = 0x00.
SPI will not execute the read command it is treated as dummy and will only shift the input by 24-bit.

Example 1)
Writing data
Address = 0x14 (ADTRG)
Data = 0x80
CRC = 0xB4

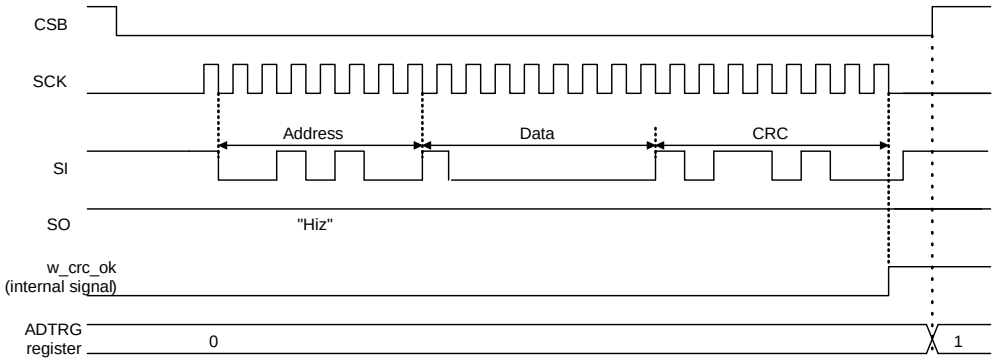


Figure 32. SPI Protocol of the 1 Byte Write

Example 2)
Reading data (RDMODE = 1)
Address = 0x1C (VMON)
Data = 0xFF(dummy)
CRC = 0x76 (MCU -> this device)

Read data = 0x05
CRC = 0xF5 (this device -> MCU)

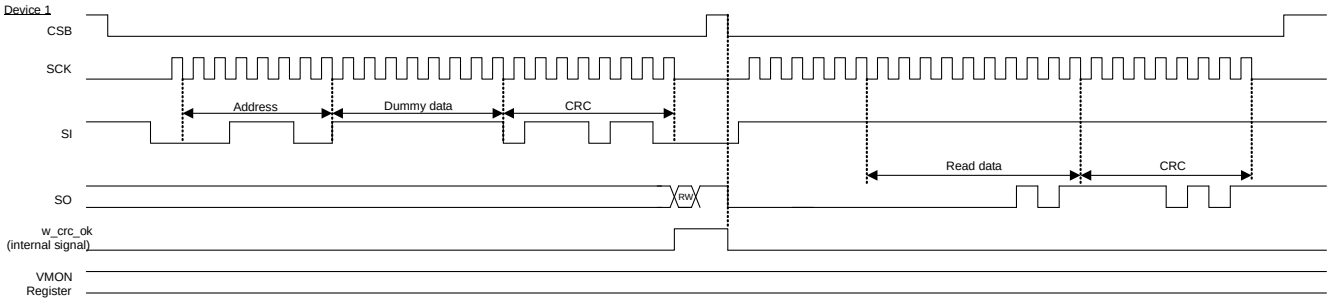


Figure 33. SPI Protocol of the 1 Byte Read

Description of Blocks – continued

17 EEPROM Operation

EEPROM can be used to store 8 sets of register setting using 4-kbit EEPROM size. MSEL pin voltage can be controlled to select which setting will be used by the device. EEPROM access is also available by setting the MODE pin. When MODE = H, EEPROM load is available after starting the device. When MODE = L, EEPROM load is available when WDT error is detected. Writing or updating EEPROM values is also available using the SPI Interface. EEPROM can be accessed using the SCL and SDA pins as show in the figure below. If EEPROM is not used, both the SDA pin and the SCL pin should be pulled up with 1 kΩ to the VREG5 pin.
SCL - Serial Clock for EEPROM Access
SDA - Serial Data for EEPROM Access

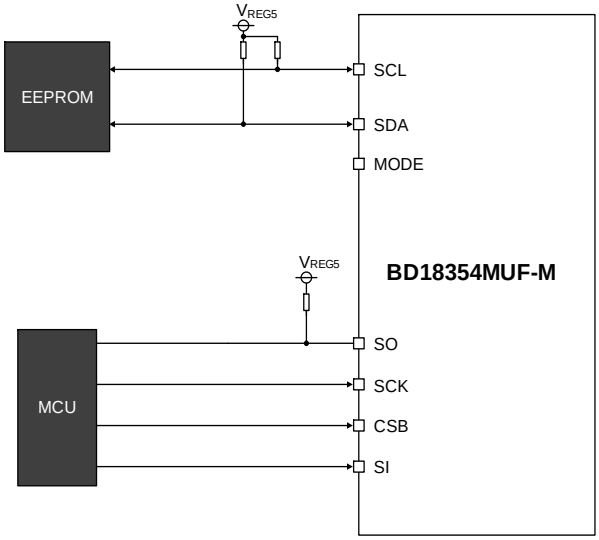


Figure 34. EEPROM and Device Connection

17.1 EEPROM Load (The MODE Pin)

The figure below shows the sequence on how to load data during EEPROM operation state.

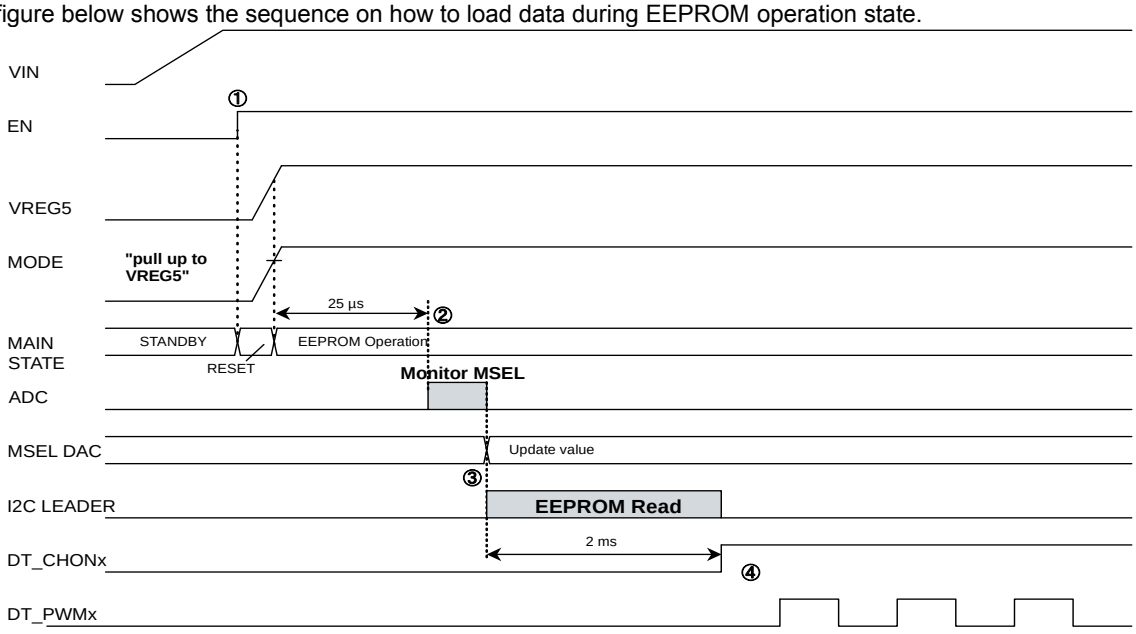


Figure 35. EEPROM Load Sequence

When you light the LED by EEPROM load access, follow the sequence below.
① Start the circuit with EN = H (To RESET state).
② When Reset is released, MSEL pin voltage is monitored by ADC after 25 µs to determine the EEPROM address setting.
③ EEPROM load will start and data from EEPROM is stored to internal register map of the device.
④ EEPROM load will finish after 2 ms and device will operate based on the loaded EEPROM data.

17.1 EEPROM Load (The MODE Pin) – continued

By monitoring the MSEL pin voltage, register setting number can be selected and load the data stored in the respective EEPROM address. For the data stored in each setting, alternate register address data and CRC data is stored. This is to make sure that correct data is loaded and stored to internal register map. When corresponding CRC data is NG and was detected twice, EEPROM load will stop and the state goes to STAND-ALONE.

Table 5. MSEL Pin Voltage Decoder for EEPROM Address Range

Register Setting #	MSEL Pin Voltage		EEPROM Address	
	Min (V)	Max (V)	Start	End
1	0.000	0.625	0x000	0x03F
2	0.626	1.250	0x040	0x07F
3	1.251	1.875	0x080	0x0BF
4	1.876	2.500	0x0C0	0x0FF
5	2.501	3.125	0x100	0x13F
6	3.126	3.750	0x140	0x17F
7	3.751	4.375	0x180	0x1BF
8	4.376	5.000	0x1C0	0x1FF

Setting #1 (MSEL = 0 V to 0.635 V)	
Address	Details
0x000	Data for Reg Address 0x00
0x001	CRC for Reg Address 0x00
0x002	Data for Reg Address 0x01
0x003	CRC for Reg Address 0x01
0x004	Data for Reg Address 0x02
0x005	CRC for Reg Address 0x02
…	…
0x03E	Data for Reg Address 0x1F
0x03F	CRC for Reg Address 0x1F

EEPROM load will start by sending a dummy byte (start bit, 9 SCL cycles high, stop bit). After that, follower address will be sent followed by a write bit. The next byte will be address byte which indicates the start address for EEPROM load. The follower address will be sent again but R/W bit is now HIGH indicating read command to EEPROM. The SDA line will now be controlled by EEPROM and data byte will be sent to the device one-by-one. The sequential read protocol is displayed in the figure below and this protocol is automatically sent by the device.

Bus Activity:

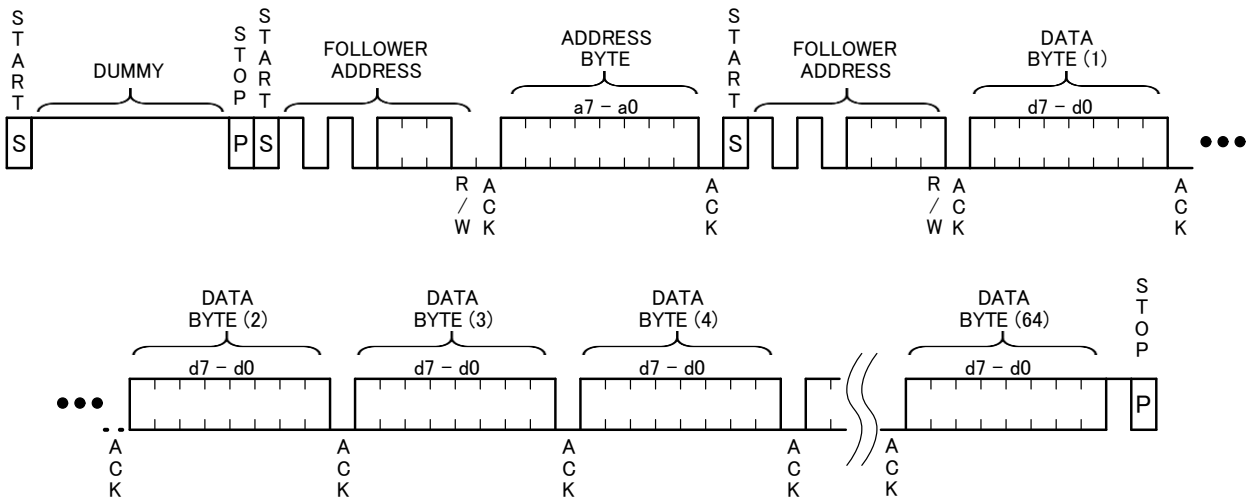


Figure 36. EEPROM Loading Protocol

17.1 EEPROM Load (The MODE pin) – continued

EEPROM Access Parameters

Follower Address

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Follower Address[6:0]							RW

bit	Parameter	Function
Follower Address[6:0]	EEPROM Follower Address	The follower address is a fixed address with the following data: 1_0_1_0_0_0_P Where P is the page address. If P = 0, register setting 1, 2, 3 and 4 can be loaded. If P = 1, register setting 5, 6, 7 and 8 can be loaded.
R/W	Read or Write Access	0: Write Access 1: Read Access

Address Byte

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Address Byte[7:0]							

bit	Parameter	Function
Address Byte[7:0]	Register Address Start for EEPROM Load	When P = 0: 8'h00 – Start address for register setting #1 8'h40 – Start address for register setting #2 8'h80 – Start address for register setting #3 8'hC0 – Start address for register setting #4 When P = 1: 8'h00 – Start address for register setting #5 8'h40 – Start address for register setting #6 8'h80 – Start address for register setting #7 8'hC0 – Start address for register setting #8

Data Byte

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Data Byte[7:0]							

bit	Parameter	Function
Data Byte[7:0]	Data Loaded form EEPROM	0x00 to 0xFF This data is the register data or CRC that will be stored in the internal register map.

17 EEPROM Operation – continued

17.2 EEPROM Load (SPI Signal)

EEPROM Data can be updated by using the SPI Interface. The figure below shows the sequence on how to write or update data.

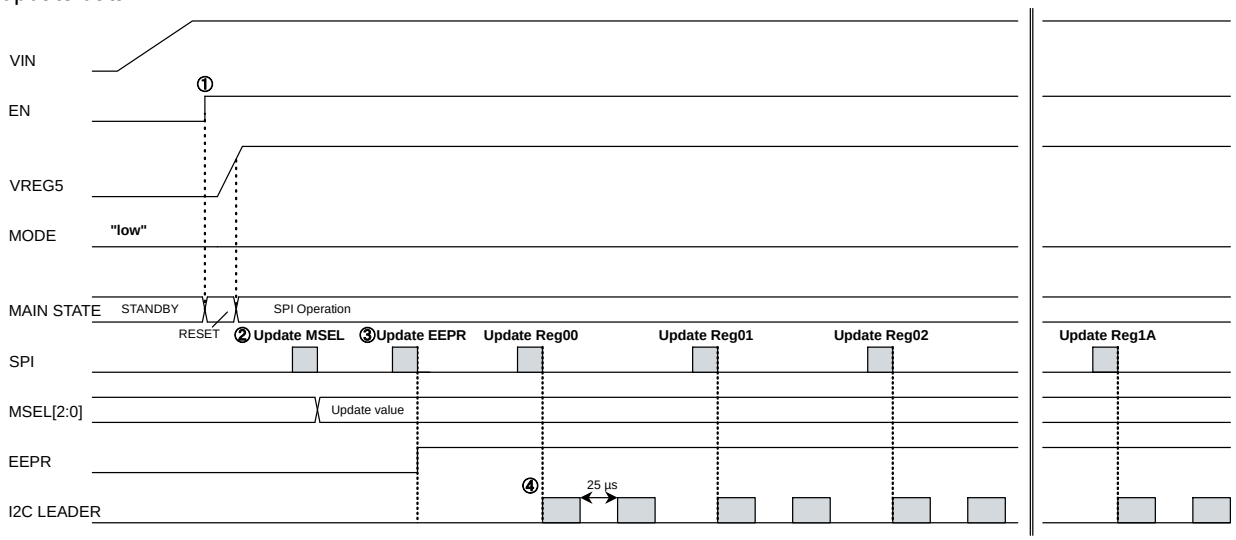


Figure 37. EEPROM Write Sequence

In writing or updating EEPROM values, follow the sequence below.

① Start the circuit with EN = H (To RESET state).

② When reset is released, state will go to the SPI operation. Update MSEL register to select which EEPROM address range will be updated.

③ Update EEPR register to H. This will enable write-protection to internal register map. Instead of storing the SPI write commands to register map, it will be automatically converted to I2C write command that will be sent to EEPROM.

④ EEPROM will be updated by the SPI Interface. The designated address is calculated automatically and the corresponding CRC data is also stored to the next address of the data.

The Write Protocol to update EEPROM values can be seen in the figure below. The device will start by sending the follower address followed by R/W = 0 bit to indicate write command. The address byte is the calculated address where the data will be stored. The data byte will be the same as the data sent through the SPI write command and the CRC for this data is automatically computed and will be written to the next EEPROM address after 25 µs.
Bus Activity:

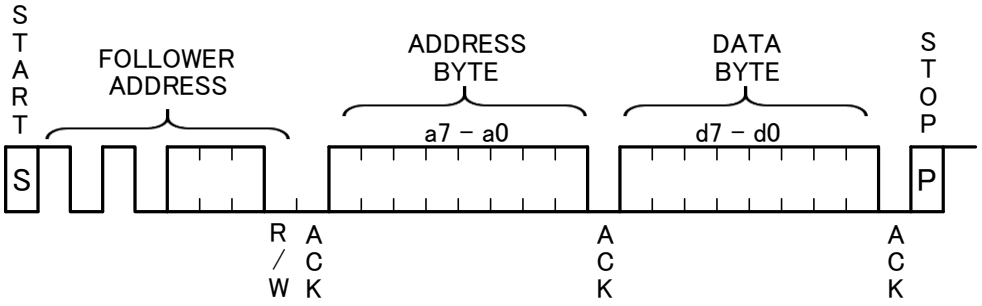


Figure 38. Byte Write Protocol

Description of Blocks – continued

18 Register

Register MAP(Address 0x00 to 0x20)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	Initial	Reset Condition	Comments
SYSSET	0x00	-	WLOCK	RDMODE	SLEEP	-	FLTBCNTEN	FLTBCNT	SWRST	R/W	0x00	POR/TSD/ SWRST	Software reset, Sleep setting, Register access control NOTE : POR/TSD for reset of SWRST
ERRSET1	0x01	-	WDTEN	-	FLTBEN[4:0]					R/W	0x5E	POR/TSD/ SWRST	FAULT_B output enable, WDT setting,
ERRSET2	0x02	OCP1MASK	SCP1MASK	OCPSET1[1:0]		OVPSET1[3:0]				R/W	0x1F	POR/TSD/ SWRST	Protection detection setting for CH1
ERRSET3	0x03	FLTRST1	SCPLAT1	OCPLAT1	EOVP1/SSU1	-	-	-	-	R/W	0x00	POR/TSD/ SWRST	EOVP/SSU setting, Protection status latch, Error reset for CH1
ERRSET4	0x04	OCP2MASK	SCP2MASK	OCPSET2[1:0]		OVPSET2[3:0]				R/W	0x1F	POR/TSD/ SWRST	Protection detection setting for CH2
ERRSET5	0x05	FLTRST2	SCPLAT2	OCPLAT2	EOVP2/SSU2	-	-	-	-	R/W	0x00	POR/TSD/ SWRST	EOVP/SSU setting, Protection status latch, Error reset for CH2
PHSET	0x06	PPSEN	PWMDIV[2:0]			-	-	-	-	R/W	0x10	POR/TSD/ SWRST	PWM frequency, Phase shift setting
ISET1H	0x07	ISET1[9:2]								R/W	0xE1	POR/TSD/ SWRST	Current/Voltage setting for CH1
ISET1L	0x08	CAL1[3:0]				-	-	ISET1[1:0]		R/W	0xF1	POR/TSD/ SWRST	Current/Voltage, Slope offset setting for CH1
ISET2H	0x09	ISET2[9:2]								R/W	0xE1	POR/TSD/ SWRST	Current/Voltage setting for CH2
ISET2L	0x0A	CAL2[3:0]				-	-	ISET2[1:0]		R/W	0xF1	POR/TSD/ SWRST	Current/Voltage, Slope offset setting for CH2
DPWM1H	0x0B	DPWM1[9:2]								R/W	0x00	POR/TSD/ SWRST	PWM ON duty for CH1
DPWM1L	0x0C	-	-	-	-	-	-	DPWM1[1:0]		R/W	0x00	POR/TSD/ SWRST	PWM ON duty for CH1
DPWM2H	0x0D	DPWM2[9:2]								R/W	0x00	POR/TSD/ SWRST	PWM ON duty for CH2
DPWM2L	0x0E	-	-	-	-	-	-	DPWM2[1:0]		R/W	0x00	POR/TSD/ SWRST	PWM ON duty for CH2
DCDCSET1	0x0F	MULTIP	PHSHFT	-	-	FRT[3:0]				R/W	0x45	POR/TSD/ SWRST	Switching frequency, Phase shift setting of DC/DC OSC, Multi phase setting
DCDCSET2	0x10	SSUSET2[1:0]		SSUSET1[1:0]		BTB2	BTB1	VMODE2	VMODE1	R/W	0x00	POR/TSD/ SWRST	Voltage mode, Boost mode and Slow start up setting for each CH
DCDCSET3	0x11	-	-	-	SSFMW[1:0]		SSFM[2:0]			R/W	0x0C	POR/TSD/ SWRST	SSCG setting for both CH
DCDCSET4	0x12	-	-	SSSET2[2:0]			SSSET1[2:0]			R/W	0x12	POR/TSD/ SWRST	Soft start setting for each CH
CHEN	0x13	-	-	PWMDIM2	PWMDIM1	-	-	CHON2	CHON1	R/W	0x00	POR/TSD/ SWRST	DC/DC enable, PWM dimming enable
ADSEL	0x14	ADTRG	-	-	ADMODE	VMONSEL[3:0]				R/W	0x10	POR/TSD/ SWRST	Thermal, VIN, VSNSN1, VISNS1, VSNSN2, VISNS2, VBIN1, VBIN2, VMSEL, VINDIM voltage monitor, Auto dimming mode, A/D converter trigger in manual mode
NTCVINGAIN1	0x15	VINDSET1[1:0]		VINDGAIN1[1:0]		BINSEL1[1:0]		NTCGAIN1[1:0]		R/W	0x6E	POR/TSD/ SWRST	VIN dimmg, BIN rank, and NTC gain setting CH1
NTCSET1	0x16	NTCSET1[7:0]								R/W	0x7F	POR/TSD/ SWRST	NTC start voltage CH1
NTCVINGAIN2	0x17	VINDSET2[1:0]		VINDGAIN2[1:0]		BINSEL2[1:0]		NTCGAIN2[1:0]		R/W	0x6E	POR/TSD/ SWRST	VIN dimmg, BIN rank, and NTC gain setting CH2
NTCSET2	0x18	NTCSET2[7:0]								R/W	0x7F	POR/TSD/ SWRST	NTC start voltage CH2
CURSET1	0x19	-	-	-	ISLP1[2:0]			-	-	R/W	0x10	POR/TSD/ SWRST	Slope tilt setting CH1
CURSET2	0x1A	-	CURLIMEN2	CURLIMEN1	ISLP2[2:0]			-	-	R/W	0x10	POR/TSD/ SWRST	Slope tilt setting CH2, Current limit enable
VMONH	0x1C	VMON[9:2]								RO	0x00	POR/TSD/ SWRST	Voltage monitor by A/D.
VMONL	0x1D	-	-	-	-	-	-	VMON[1:0]		RO	0x00	POR/TSD/ SWRST	Voltage monitor by A/D.
ERRSTALL	0x1E	WDTERR	SPICRCERR	I2CCRCERR	-	-	UVLO	ERRDET2	ERRDET1	RO	0x00	POR/TSD/ SWRST	Error status register
ERRST	0x1F	OCPERR2	SCPERR2	UVDERR2	OVPERR2	OCPERR1	SCPERR1	UVDERR1	OVPERR1	RO	0x00	POR/TSD/ SWRST	Error status register
EEPCTRL	0x20	EEPR	EEP_LOAD	WRSEL[1:0]		PAGEWREN	MSEL[2:0]			R/W	0x00	POR/TSD/ SWRST	EEPROM control registers

WO: Write Only, RO: Read Only, R/W: Read and Write
SWRST register reset condition is POR/TSD. All other registers reset condition is POR/TSD/SWRST.
When writing a register value to the EEPROM be sure to write 0 for the SWRST register value.

(Caution 1) SWRST, FLTRSTx and ADTRG are “write only”, and reset condition of SWRST is only “POR/TSD”.
(Caution 2) EEPR, SLEEP and SWRST can only be updated by SPI (not affected by EEPROM load).
(Caution 3) When writing a register value to the EEPROM be sure to write 0 for the SWRST register value.

18 Register - continued

Description of Registers

●Address 0x00: SYSSET System Setting [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	WLOCK	RDMODE	SLEEP	-	FLTBCNTEN	FLTBCNT	SWRST
Initial Value	-	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[0] SWRST
SWRST register return '0' automatically. Hence, this register is "Write only".
Set this register when you want to reset digital circuit.
When writing a register value to the EEPROM be sure to write 0 for the SWRST register value.
Writing 1 in the SWRST register will not work properly.

Table 6. SWRST Operation

SWRST	Reset
0	Normal
1	Reset for digital circuit (return '0' automatically)

bit[1] FLTBCNT
bit[2] FLTBCNTEN
These register controls FAULT_B output. If FLTBCNTEN = 0, FAULT_B is controlled by error detection. If FLTBCNTEN = 1, FAULT_B is Low when FLTBCNT = 0 and FAULT_B is Hiz when FLTBCNT = 1.

Table 7. FLTBCNTEN Operation

FLTBCNTEN	Operation
0	FAULT_B output is controlled by error detection.
1	FAULT_B = FLTBCNT FAULT_B output is controlled by FLTBCNT register.

bit[4] SLEEP
This IC has sleep mode which stops internal clock, so this IC is in low "quiescent current" condition. This IC keeps register value when SLEEP = 1.

Table 8. SLEEP Operation

SLEEP	Operation
0	Normal
1	Low "quiescent current" condition. Oscillator is stopped. DC/DC and current driver are off. Only internal regulator is available.

18 Register - continued

bit[5] RDMODE

This register controls read protocol. If RDMODE = 1, it outputs read data (target address 8-bit + next address bit[1:0]). The detail of protocol can be referred in "SPI Protocol" section.

Table 9. RDMODE Operation

RDMODE	Operation
0	Outputs target address data
1	Outputs target address data + next address data bit [1:0]

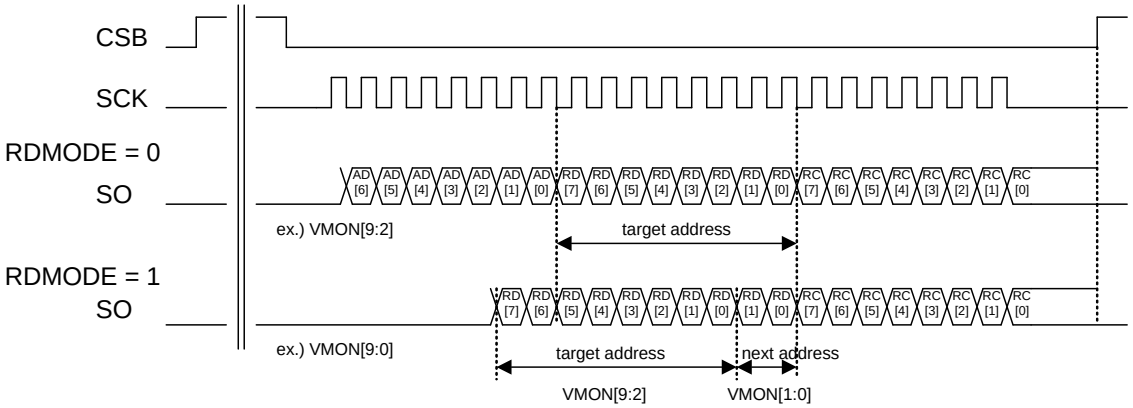


Figure 39. RDMODE Operation

bit[6] WLOCK

DPWMx, ISETx and VMON registers are split into two registers (higher and lower byte). Normally, whenever a byte (higher or lower) is written, it will immediately be reflected in PWM dimming control. If WLOCK function is used, PWM dimming control will not be updated until the two bytes (higher and lower) are written.
Note that it doesn't matter whether the higher or lower byte is written first.

Table 10. WLOCK Operation

WLOCK	Operation
0	Normal update
1	PWM dimming control is not updated until writing the other address. (0x07 to 0x0E)

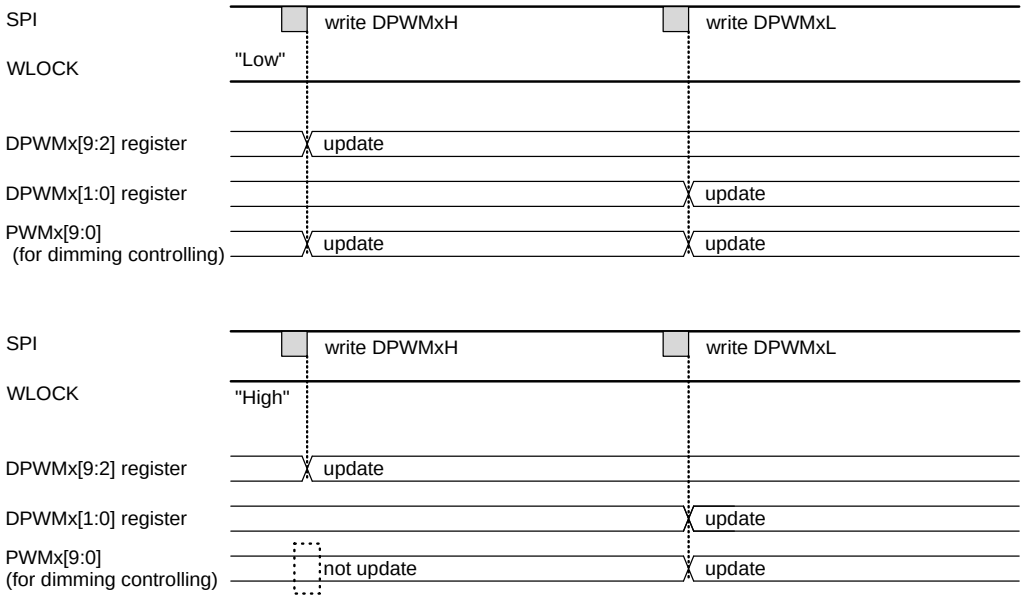


Figure 40. WLOCK Function Example

18 Register - continued

●Address 0x01: ERRSET1 Enable Setting [Read/Write] Initial Value 0x5E

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	WDTEN	-	FLTBEN[4:0]				
Initial Value	0	1	0	1	1	1	1	0

The data in register is updated to the newest data immediately when the new data is written.

bit[4:0] FLTBEN[4:0]
FAULT_B output enable setting

Table 11. FAULT_B Output Enable

FLTBEN[x]	Operation
0	Target protection is disabled in FAULT_B output. FAULT_B is fixed 'H' (with Pull-up resistor).
1	Normal operation.

Table 12. FLTBEN Assigned for Each Protection

FLTBEN[x]	FAULT_B Output Mask
Bit 0	UVLO
Bit 1	Over Current Protection
Bit 2	Short Circuit Protection
Bit 3	Over Voltage Protection
Bit 4	Under Voltage Detection

bit[6] WDTEN
This register is "Watch Dog Timer" function enable. If WDTEN = 1, LIMP-HOME function is available by "Watch Dog Timer error" when state is "SPI operation".
Changing the WDTEN register setting after "Watch Dog Timer error" detection is prohibited.

Table 13. "Watch Dog Timer" Enable

WDTEN	Enable
0	"Watch Dog Timer" is not available.
1	"Watch Dog Timer" is available.

●Address 0x02: ERRSET2 Protection Setting [Read/Write] Initial Value 0x1F

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	OCP1MASK	SCP1MASK	OCPSET1[1:0]		OVPSET1[3:0]			
Initial Value	0	0	0	1	1	1	1	1

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[3:0] OVPSET1[3:0]
This register controls the OVP voltage threshold for CH1. (See "Over Voltage Protection (OVP)".)

Table 14. OVP Voltage Setting

OVPSET1[3:0]	V_{OVP1} [V]	OVPSET1[3:0]	V_{OVP1} [V]
0	34.80	8	52.24
1	36.98	9	54.42
2	39.16	10	56.60
3	41.34	11	58.78
4	43.52	12	60.96
5	45.70	13	63.14
6	47.88	14	65.32
7	50.06	15 (initial)	67.50

18 Register - continued

bit[5:4] OCPSET1[1:0]
This register controls the OCP voltage threshold for CH1. (See "Over Current Protection (OCP)".)

Table 15. OCP Voltage Setting

OCPSET1[1:0]	V_{CSOCP1} [mV]
0	100
1 (initial)	150
2	200
3	300

bit[6] SCP1MASK
The SCP function of CH1 is programmed by this register. When SCP1MASK = '0', the SCP function of CH1 is enabled, when SCP1MASK = '1', the SCP function of CH1 is masked.

Table 16. SCP1MASK Function

SCP1MASK	Operation
0	the SCP function of CH1 is enabled.
1	the SCP function of CH1 is masked.

bit[7] OCP1MASK
The OCP function of CH1 is programmed by this register. When OCP1MASK = '0', the OCP function of CH1 is enabled, when OCP1MASK = '1', the OCP function of CH1 is masked.

Table 17. OCP1MASK Function

OCP1MASK	Operation
0	the OCP function of CH1 is enabled.
1	the OCP function of CH1 is masked.

●Address 0x03: ERRSET3 Protection Setting [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	FLTRST1	SCPLAT1	OCPLAT1	EOVP1/SSU1	-	-	-	-
Initial Value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[4] EOVP1/SSU1
When EOVP1/SSU1 = 0, the external OVP and UVD functions are enabled and the SSU function is disabled, when EOVP1/SSU1 = 1, the external OVP and UVD functions are disabled and the SSU function is enabled. (For details on "External Over Voltage Protection (EOVP)" and "Slow Startup".)

Table 18. EOVP1/SSU1 Function

EOVP1/SSU1	Operation
0	The external OVP and UVD functions are enabled.
1	The SSU function is enabled.

bit[5] OCPLAT1
The releasing function of over current protection is programmed by this register. If OCPLAT1 = '1', the OCPERR1 register doesn't become '0' until writing FLTRST1 = '1'. If OCPLAT1 = '0', The OCPERR1 becomes '0' by over current protection released.
Set OCPLAT1 when OCPERR1 = 0.

Table 19. Over Current Protection Latch Operation Setting

OCPLAT1	Operation
0	If this error condition is released, error status register and FAULT_B1 returns normal condition.
1	This IC keeps error condition until writing FLTRST1 = 1.

18 Register - continued

bit[6] SCPLAT1
The releasing function of short circuit protection is programmed by this register. If SCPLAT1 = '1', the SCPERR1 register doesn't become '0' until writing FLTRST1 = '1'. If SCPLAT1 = '0', the SCPERR1 becomes '0' by short circuit error protection released.
Set SCPLAT1 when SCPERR1 = 0.

Table 20. Short Circuit Protection Latch Operation Setting

SCPLAT1	Operation
0	If this error condition is released, error status register and FAULT_B1 returns normal condition.
1	This IC keeps error condition until writing FLTRST1 = 1.

bit[7] FLTRST1
The error status registers are initialized by this register. If each protection is latched, its condition is released. For WDTERR, SPICRCERR and I2CCRCERR, either FLTRST1 or FLTRST2 can clear the error.

Table 21. Error Status Reset

FLTRST1	Operation
0	Normal
1	Initialize error status for WDTERR, SPICRCERR, I2CCRCERR, OCPERR1 and SCPERR1.

OVPERR1 and UVDERR1 are not reset.

●Address 0x04: ERRSET4
This register is used to make setting of protection for CH2.
The setting procedure is the same as that for CH1 with Address set to 0x02.

●Address 0x05: ERRSET5
This register is used to make setting of protection for CH2.
The setting procedure is the same as that for CH1 with Address set to 0x03.

●Address 0x06: PHSET PWM Frequency Setting [Read/Write] Initial Value 0x10

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PPSEN	PWMDIV[2:0]			-	-	-	-
Initial Value	0	0	0	1	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[6:4] PWMDIV[2:0]
The PWM dimming frequency is programmed by this register.

Table 22. PWM Output Frequency Setting

PWMDIV[2:0]	PWM Output Frequency [Hz]
0	81.4
1 (initial)	203.0
2	244.0
3	305.0
4	407.0
5	488.0
6	610.0
7	814.0

bit[7] PPSEN
The PWM dimming phase is programmed by this register.

Table 23. PWM Phase Setting

PPSEN	Phase
0	No Phase shift
1	CH1: no shift CH2: 180 degrees

18 Register - continued

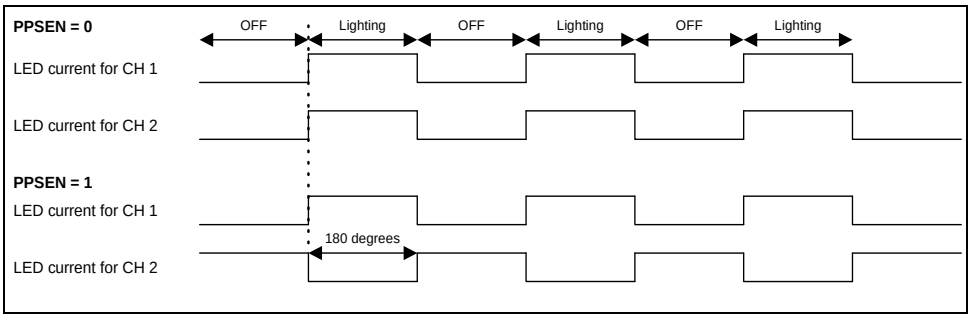


Figure 41. PWM Phase Shift Setting

●Address 0x07: ISET1H ISET Setting for CH1 [Read/Write] Initial Value 0xE1

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ISET1[9:2]							
Initial Value	1	1	1	0	0	0	0	1

●Address 0x08: ISET1L ISET Setting for CH1 [Read/Write] Initial Value 0xF1

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	CAL1[3:0]				-	-	ISET1[1:0]	
Initial Value	1	1	1	1	0	0	0	1

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting. If you want to change value during dimming, WLOCK function can be used.

ISET1H
bit[7:0]: ISET1[9:2]
ISET1L
bit[1:0]: ISET1[1:0]
LED average current is programmed by this register using the following formula.

Formula

$$I_{LED1AVE} = \frac{V_{SNS1}}{R_{SNS1}} = \frac{V_{DCDIM1} - 0.2\,V}{12 \times R_{SNS1}} = (\frac{ISET1[9:0]}{1024} \times V_{FSRADC} - 0.2\,V) \times \frac{1}{12 \times R_{SNS1}}$$

ISET1L
bit[7:4]: CAL1[3:0]
CAL1: Each channel has three calibration bits, which adds 2.75 mV of offset per bit (2.75 mV to 19.25 mV) to the slope low voltage.

Table 24. Slope Low Voltage Setting

CAL1[3:0]	SLOPE Offset [mV]	CAL1[3:0]	SLOPE Offset [mV]
0	+19.25	8	-19.25
1	+16.50	9	-16.50
2	+13.75	10	-13.75
3	+11.00	11	-11.00
4	+8.25	12	-8.25
5	+5.50	13	-5.50
6	+2.75	14	-2.75
7	0	15 (initial)	0

18 Register - continued

●Address 0x09 to 0x0A: ISET2H, ISET2L

This register is used to make setting of LED current for CH2. The setting procedure is the same as that for CH1 with address set to 0x07 and 0x08

●Address 0x0B: DPWM1H PWM Duty Setting for CH1 [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DPWM1[9:2]							
Initial Value	0	0	0	0	0	0	0	0

●Address 0x0C: DPWM1L PWM Duty Setting for CH1 [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	DPWM1[1:0]	
Initial Value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting. If you want to change value during dimming, WLOCK function can be used.

DPWM1H
bit[7:0]: DPWM1[9:2]
DPWM1L
bit[1:0]: DPWM1[1:0]
LED average current in PWM is programmed by this register. When DPWM = 10'h000, PWM output is fixed low. For DPWM > 10'h000, the dimming ratio is calculated by the following formula.

$$D_{PWMx} = \frac{DPWMx[9:0] + 1}{1024}$$

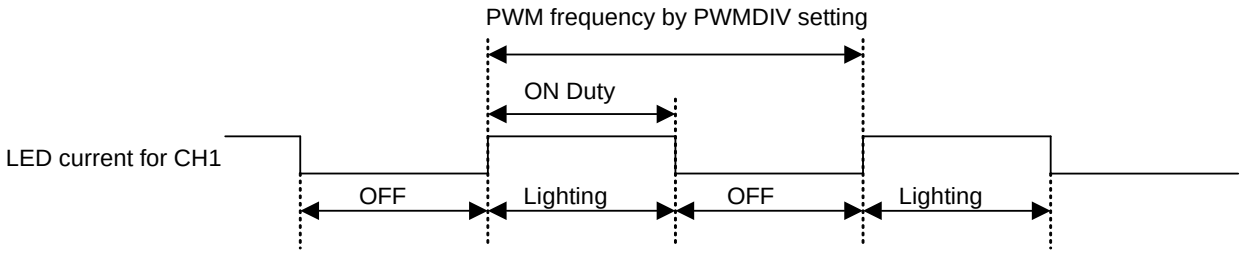


Figure 42. PWM Dimming

●Address 0x0D to 0x0E: DPWM2H, DPWM2L

This register is used to make setting of PWM for CH2. The setting procedure is the same as that for CH1 with address set to 0x0B and 0x0C.

●Address 0x0F: DCDCSET1 DC/DC Setting 1 [Read/Write] Initial Value 0x45

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	MULTIP	PHSHFT	-	-	FRT[3:0]			
Initial Value	0	1	0	0	0	1	0	1

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[3:0] FRT[3:0]
DC/DC frequency setting is programmed for by this register.
It is available to use DC/DC frequency setting under 2.50 MHz. (over 2.50 MHz setting is prohibited.)
See "Switching Frequency Setting (OSC)" in Description of Blocks for the details.

bit[6] PHSHFT
When PHSHFT = 0, the phases of the CH1 and CH2 oscillators operate in phase.
When PHSHFT = 1, the phase of the oscillator of CH2 is delayed by 180 degrees with respect to CH1.
Set PHSHT when CHONx = 0.

18 Register - continued

bit[7] MULTIP
Set MULTIP = 1 when using in multi-phase voltage mode.
Set MULTIP when CHONx = 0.

This mode is used for dual-phase CV output settings.
For dual-phase CV output settings, set the following registers.
MULTIP = 1, PHSHFT = 1, PWMDIMx = 0, VMODEx = 1, and CURLIMENx = 0.
ISLP1[2:0] and ISLP2[2:0] settings must be common. (ex)ISLP1[2:0] = ISLP2[2:0] = 4

The DC/DC operation with this setting is as follows.
The COMP1 and COMP2 pins are shorted by a resistor inside the IC, and the switching duty is returned by the COMP1 pin.
VOUT output voltage is set by ISET1[9:0].
ISET2[9:0] setting is invalid.
The startup setting is enabled when CHON2 = CHON1 = 1.

See "SPI operation (Multi phase Voltage output)" for application examples.

●Address 0x10: DCDCSET2 DC/DC Setting 2 [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	SSUSET2[1:0]		SSUSET1[1:0]		BTB2	BTB1	VMODE2	VMODE1
Initial Value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these registers in initial setting.

bit[1:0] VMODEx
"Voltage regulation mode" for DC/DC is programmed by this register.

Table 25. Voltage Regulation Mode Setting

VMODEx	Controlled Mode
0 (initial)	Current regulation mode for CHx (initial)
1	Voltage regulation mode for CHx

bit[3:2] BTBx
The internal UVD detection voltage of CHx is programmed by this register.

Table 26. The Internal UVD Detection Voltage Setting

BTBx	Controlled Mode
0 (initial)	The internal UVD detection voltage of CHx is set to V_{UVDx1}.
1	Internal UVD detection voltage of CHx is set to V_{UVDx2}.

bit[5:4] SSUSET1[1:0]
This register controls the division factor for slow startup function of CH1. See "Slow Startup" in description of blocks section for the details.

bit[7:6] SSUSET2[1:0]
This register controls the division factor for slow startup function of CH2. See "Slow Startup" in description of blocks section for the details.

18 Register - continued

●Address 0x11: DCDCSET3 DC/DC Setting 3 [Read/Write] Initial Value 0x0C

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	SSFMW[1:0]		SSFM[2:0]		
Initial Value	0	0	0	0	1	1	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[2:0] SSFM[2:0]
The modulation DC/DC switching frequency is programmed for all channel by this register.

Table 27. SSFM Modulation Setting

SSFM[2:0]	SSFM Modulation Ratio [Hz]
0	SSFM OFF (Fixed frequency of DC/DC)
1	64
2	128
3	257
4 (initial)	506
5	1044
6	2204
7	3968

bit[4:3] SSFMW[1:0]
The modulation DC/DC switching frequency deviation is programmed for all channel by this register.

Table 28. SSFM Modulation Width Setting

SSFMW[1:0]	f_{SSFMW} [%]
0	0
1 (initial)	5
2	10
3	15

●Address 0x12: DCDCSET4 DC/DC Setting 4 [Read/Write] Initial Value 0x12

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	SSSET2[2:0]			SSSET1[2:0]		
Initial Value	0	0	0	1	0	0	1	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[2:0] SSSET1[2:0]
This register controls the division factor for the switching frequency that will be used in soft start function of CH1. See “Soft Start” in the description of blocks section for the details.

bit[5:3] SSSET2[2:0]
This register controls the division factor for the switching frequency that will be used in soft start function of CH2. See “Soft Start” in the description of blocks section for the details.

18 Register - continued

●Address 0x13: CHEN Channel Enable and Dimming Enable [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	PWMDIM2	PWMDIM1	-	-	CHON2	CHON1
Initial Value	0	0	0	0	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[1:0] CHONx
Each channel starts-up by this register. If CHONx = 1, LED dimming is available for CHx. CHONx = 0, LED dimming is not available for CHx. Protection such as “Over Current Protection”, “Short Circuit Protection”, “Over Voltage Protection” and “Under Voltage Detection” in the target channel is not available when CHONx = 0.

Table 29. Channel Enable

CHONx	Enable
0 (initial)	CHx is disable.
1	CHx is enable.

bit[5:4] PWMDIMx
This register is used to turn the PWM dimming function ON/OFF.
When PWMDIMx = 1, PWM dimming can be performed using the internal PWM duty set by the DPWMx[9:0] register or the external PWM duty input to the PWMDx pin.
Internal PWM duty and external PWM duty are OR controlled (H signal has priority).
When PWMDIMx = 0, the internal PWM duty is set to 100 %.

Table 30. PWM Dimming Enable

PWMDIMx	Operation
0 (initial)	PWM Duty is 100 % fixed.
1	PWM Dimming enable. Dimming ratio is programmed by DPWMx[9:0] register or PWMDx pin input signal.

Table 31. How to Dim by PWM

CHONx	PWMDIMx	DPWMx[9:0]	PWMDx Pin Input	DC/DCx	PWM Dimming for CHx
0	x	x	x	OFF	OFF
1	0	x	x	ON	PWM duty 100 % dimming
1	1	0	x	ON	Programmed by PWMDx input duty
1	1	x	L	ON	Programmed by DPWMx[9:0] register
1	1	x	H	ON	PWM duty 100 % dimming

●Address 0x14: ADSEL A/D Monitor Channel Select [Read/Write] Initial Value 0x10

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ADTRG	-	-	ADMODE	VMONSEL[3:0]			
Initial Value	0	0	0	1	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
Set these register in initial setting.

bit[3:0] VMONSEL[3:0]
VMON register is shared in for monitoring below node. This register should be programmed before reading VMON register when target node voltage is need.

18 Register - continued

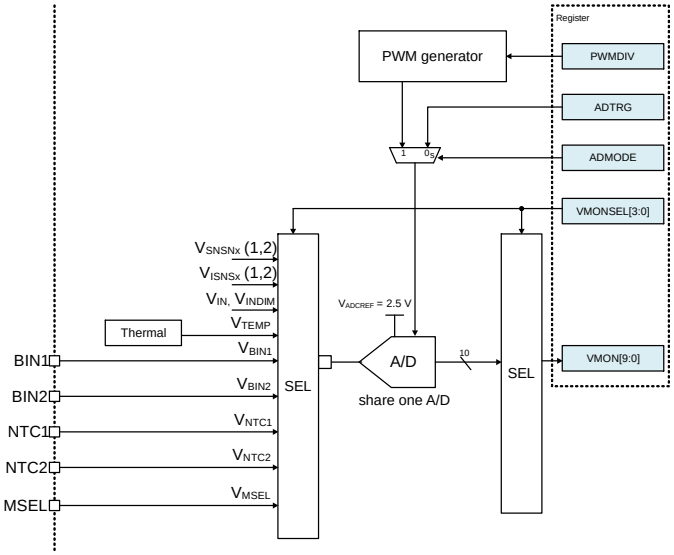


Figure 43. A/D System Structure

Table 32. VMONSEL Status

VMONSEL	Monitor Node
0 (initial)	Thermal
1	V_{IN}
2	V_{SNSN1}
3	V_{ISNS1}
4	V_{SNSN2}
5	V_{ISNSN2}
6	Not Used
7	Not Used
8	V_{BIN1}
9	V_{BIN2}
10	V_{NTC1}
11	V_{NTC2}
12	V_{MSEL}
13	V_{INDIM} (for VIN dimming)

bit[4] ADMODE

There are two A/D converting modes.

When ADMODE = 1, A/D converter is operated automatically. Conversion frequency is controlled by an internal counter that monitors the inputs used in dimming (VIN, BINx, NTCx) for voltage derating. 1 cycle = 128 µs.

When ADMODE = 0, A/D converter is operated manually by ADTRG. A/D converter becomes sleep condition (low current consumption) after 1 conversion.

Table 33. ADMODE Operation

ADMODE	Operation
0	A/D conversion for only target node by ADTRG register
1 (initial)	Repeat the A/D conversion of BINx/VIN/NTCx to automatically adjust the dimming of ISETDx[9:0]. This period is internally programmed and fixed at 128 µs.

bit[7] ADTRG

A/D starts to convert the data selected by VMONSEL register after writing ADTRG = 1 during ADMODE = 0. This register will return to '0' after writing '1'. Updated data is available less than 15 µs. Issue the ADTRG command after soft start of each channel is completed.

Table 34. ADTRG

ADTRG	Operation
0	No conversion
1	Starts to convert data in ADMODE = 0

18 Register - continued

●Address 0x15: NTCVINGAIN1 Voltage Derating Setting 1 for CH1 [Read/Write] Initial Value 0x6E

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	VINDSET1[1:0]		VINDGAIN1[1:0]		BINSEL1[1:0]		NTCGAIN1[1:0]	
Initial Value	0	1	1	0	1	1	1	0

The data in register is updated to the newest data immediately when the new data is written.
See "VIN Pin, NTCx Pin and BINx Pin Dimming Setting" for the details.

bit[1:0] NTCGAIN1[1:0]
The thermal derating gain is set by this register.

bit[3:2] BINSEL1[1:0]
The value from the BIN table is set by this register.

bit[5:4] VINDGAIN1[1:0]
The input voltage derating gain is set by this register.

bit[7:6] VINDSET1[1:0]
The input voltage derating start voltage is set by this register.

●Address 0x16: NTCSET1 Voltage Derating Setting 2 for CH1 [Read/Write] Initial Value 0x7F

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	NTCSET1[7:0]							
Initial Value	0	1	1	1	1	1	1	1

The data in register is updated to the newest data immediately when the new data is written.
See "VIN Pin, NTCx Pin and BINx Pin Dimming Setting" for the details.

bit[7:0] NTCSET1[7:0]
The NTC start voltage is set by this register.

●Address 0x17 to 0x18: NTCVINGAIN2 and NTCSET2
These registers are for voltage derating setting of CH2 and has same function as address 0x15 and 0x16.

●Address 0x19: CURSET1 Slope Compensation Current Setting 1 [Read/Write] Initial Value 0x10

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	ISLP1[2:0]			-	-
Initial Value	0	0	0	1	0	0	0	0

●Address 0x1A: CURSET2 Slope Compensation Current Setting 2 [Read/Write] Initial Value 0x10

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	CURLIMEN2	CURLIMEN1	ISLP2[2:0]			-	-
Initial Value	0	0	0	1	0	0	0	0

The data in register is updated to the newest data immediately when the new data is written.
For CURLIMENx see "Rush Current Limit Drive Circuit" for detail.

bit[4:2] ISLPx[2:0]
The slope compensation peak voltage is set by this register.

Table 35. CHx Slope Compensation Peak Voltage Setting

ISLPx	$V_{SLPx(PK)}$ [mV]
0	0
1	65
2	120
3	175
4 (initial)	235
5	290
6	345
7	400

18 Register - continued

bit[5] CURLIMEN1
bit[6] CURLIMEN2

Table 36. CURLIMENx

CURLIMENx	Operation
0	The Rush Current Limit Function OFF (initial)
1	The Rush Current Limit Function ON

●Address 0x1C: VMONH Common Voltage Monitor by A/D [Read] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	VMON[9:2]							
Initial Value	0	0	0	0	0	0	0	0

●Address 0x1D: VMONL Common Voltage Monitor by A/D [Read] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	VMON[1:0]	
Initial Value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data are updated by A/D converting.

VMONH
bit[7:0] VMON[9:2]
VMONL
bit[1:0]: VMON[1:0]
This register is used for monitoring Thermal, V_{IN}, V_{SNSNx}, V_{ISNSx}, V_{BINx}, V_{NTCx}, V_{MSEL} or V_{INDIM} node.
This operation is programmed by VMONSEL register.
This data is divided into two register address. If all of 10bit data is required during SPI read, RDMODE function is available.

Formula 1 for thermal sensor voltage

Thermal sensor voltage ADC read value = 418 @25 deg
Thermal sensor voltage ADC read value = 602 @150 deg

1.472 count/temp (1 degree)

Formula 2 for external input pin nodes

Monitor voltage 1 [V] = “X” x (VMON + 1) / 1024

V_{IN}: “X” = 77.5, V_{SNSNx}: “X” = 75, V_{ISNSx}/V_{NTCx}: “X” = 2.5, V_{BINx}/V_{MSEL}: “X” = 5.0, V_{INDIM}: “X” = 10.

●Address 0x1E: ERRSTALL All Error Status Each Protection [Read] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	WDTERR	SPICRCERR	I2CCRCERR	-	-	UVLO	ERRDET2	ERRDET1
Initial Value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data (one or more error) is detected.

bit[1:0] ERRDETx
This register is error status each channel.

Table 37. Error Status of Each Channel

ERRDETx	Status
0	Normal
1	Detects error UVDERRx || OCPERRx || SCPERRx || OVPERRx

18 Register - continued

bit[2] UVLO
This register is error status for UVLO.

Table 38. UVLO

UVLO	Status
0	Normal
1	Detects Under Voltage Error for V_{IN}/V_{DRV7}/V_{REG5}

bit[5] I2CCRCERR
This register is error status for I2C CRC. This error is detected when two times I2C CRC error is detected.

Table 39. “I2C CRC” Error Status

I2CCRCERR	Status
0	Normal
1	Detects I2C CRC Error

bit[6] SPICRCERR
This register is error status for the SPI CRC. If CRC error is detected, this register becomes 1. This register becomes 0 by FLTRSTx = 1. If CRC error occurred to the SPI command sent after to sending FLTRSTx, this will not be detected, for more details refer to error sequence for “SPI CRC error”.

Table 40. “SPI CRC” Error Status

SPICRCERR	Status
0	Normal
1	Detects SPI CRC Error

bit[7] WDTERR
This register is error status for “Watch Dog Timer”. If “Watch Dog Timer error” is detected, this register becomes 1. This register becomes 0 by FLTRSTx = 1.

Table 41. “Watch Dog Timer” Error Status

WDTERR	Status
0	Normal
1	Detects Watch Dog Timer Error

●Address 0x1F: ERRST Channel Error Status [Read] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	OCPERR2	SCPERR2	UVDERR2	OVPERR2	OCPERR1	SCPERR1	UVDERR1	OVPERR1
Initial Value	0	0	0	0	0	0	0	0

The register data is updated to the newest data immediately when the data (“Over Voltage Error”, “Under Voltage Error”, “Short Circuit Protection”, “Over Current Protection”) is detected.

bit[0] OVPERR1
bit[4] OVPERR2
This register is “Over Voltage error” status for CHx. OVPERRx becomes “1” and FAULT_Bx becomes “0” when “CHx Over Voltage” is detected. When detecting, this status register will detect immediately but during release, there is 20 ms internal counter where PWMx = H (when PWM dimming H control) and SGx = H (when $V_{SNSxAVE} > V_{SNSxSG}$) before OVPERRx returns to “0” and FAULT_Bx returns to normal “1”.

Table 42. “Over Voltage Protection” Error Status

OVPERRx	Status
0	Normal
1	Detects CHx Over Voltage Protection

bit[1] UVDERR1
bit[5] UVDERR2
This register is “Under Voltage Detection” status for CHx. UVDERRx becomes “1” and FAULT_Bx becomes “0” when “CHx Under Voltage” is detected. This protection is only possible to detect after 20 ms internal counter where CHONx = H, PWMx = H (when PWM dimming H control) and SGx = H (when $V_{SNSxAVE} > V_{SNSxSG}$) and soft start is already finished (SSENDx = H). During release, UVDERRx returns to “0” immediately at PWMx = H and FAULT_Bx returns to normal “1”.

18 Register - continued

Table 43. “Under Voltage Detection” Error Status

UVDERRx	Status
0	Normal
1	Detects CHx Under Voltage

bit[2] SCPERR1
bit[6] SCPERR2
This register is “Short Circuit Protection error” status for CHx. SCPERR1 becomes “1” and FAULT_Bx becomes “0” when “CHx Short Circuit” is detected. There is a 50 µs internal counter when detecting SCP. After SCP is detected, hiccup operation starts repeatedly every 40 ms. When there is no longer Short Circuit error, there is 20 ms release time before SCPERRx returns to “0” and FAULT_Bx returns to normal “1”.

Table 44. “Short Circuit Protection” Error Status

SCPERRx	Status
0	Normal
1	Detects CHx Short Circuit Protection

bit[3] OCPERR1
bit[7] OCPERR2
This register is “Over Current Protection” status for CHx. OCPERRx becomes “1” and FAULT_Bx becomes “0” when “CHx Over Current” is detected. This protection is detected when OCPx is detected eight times and the device enters hiccup operation.
After hiccup time elapses, there is 20 ms internal counter for release time before OCPERRx returns to “0” and FAULT_Bx returns to normal “1”.

Table 45. “Over Current Protection” Error Status

SCPERRx	Status
0	Normal
1	Detects CHx Over Current Protection

●Address 0x20: EEPCTRL EEPROM Control Registers [Read/Write] Initial Value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	EEPR	EEP_LOAD	WRSEL[1:0]		PAGEWREN	MSEL[2:0]		
Initial Value	0	0	0	0	0	0	0	0

The data in registers is updated to the newest data immediately when the new data is written.

bit[2:0] MSEL[2:0]
This register is use for selecting access to each EEPROM address range.

Table 46. MSEL Setting

MSEL[2:0]	Register Setting #	EEPROM Address	
		Start	End
0	Setting #1	0x000	0x03F
1	Setting #2	0x040	0x07F
2	Setting #3	0x080	0x0BF
3	Setting #4	0x0C0	0x0FF
4	Setting #5	0x100	0x13F
5	Setting #6	0x140	0x17F
6	Setting #7	0x180	0x1BF
7	Setting #8	0x1C0	0x1FF

bit[3] PAGEWREN
This register is used to enable EEPROM page write.

Table 47. PAGEWRITE Enable

PAGEWREN	Status
0	No writing
1	When EEPR =1, WRSEL[1:0] = 1 to 3, and EEP_LOAD = 0, data from register map is page written to EEPROM.

18 Register - continued

bit[5:4] WRSEL[1:0]
This register is used for the selection of EEPROM write options.

Table 48. EEPROM Write Mode Select

WRSEL[1:0]	Status
0	No writing
1	Byte write mode
2	8 bytes page write mode
3	16 bytes page write mode

bit[6] EEP_LOAD
This register is used to select EEPROM operation.

Table 49. EEPROM Load Status

EEP_LOAD	Status
0	EEPROM writing operation.
1	EEPROM loading operation. Loads the EEPROM data of the model set by the MSEL pin into the register map.

bit[7] EEPR
This register is used to enable access to EEPROM.

Table 50. EEPROM Access Mode Select

EEPR	Status
0	Unable to access EEPROM
1	Accessible to EEPROM

Table 51. EEPROM Control Registers

EEPR	EEP_LOAD	WRSEL[1:0]		PAGEWREN	REMARKS
Bit7	Bit6	Bit5	Bit4	Bit3	
0	*	*	*	*	Normal
1	0	0	0	0	EEPROM writing not yet started (CHON, Watch Dog Timer is masked)
1	0	0	1	*	Byte write
1	0	1	0	0	Page write (8 bytes): SPI write updates the register map
1	0	1	0	1	Page write (8 bytes): Data from register map is written in EEPROM
1	0	1	1	0	Page write (16 bytes): SPI write updates the register map
1	0	1	1	1	Page write (16 bytes): Data from register map is written in EEPROM
1	1	0	0	0	Load

Writing procedure
(ex.1) Write to model 2 with Byte write option.
Data to be written to EEPROM is written to register map.
0x20 = 91 (EEPR = 1, EEP_LOAD = 0, WRSEL = 1, PAGEWREN = 0, MSEL = 1): Byte write command.
0x20 = 00 (EEPR = 0, EEP_LOAD = 0, WRSEL = 0, PAGEWREN = 0, MSEL = 0): Return to the SPI control.

(ex.2) Write to model 3 with 16byte Page write option.
Data to be written to EEPROM is written to register map.
0x20 = B2 (EEPR = 1, EEP_LOAD = 0, WRSEL = 3, PAGEWREN = 0, MSEL = 2): Set write options and models.
0x20 = BA (EEPR = 1, EEP_LOAD = 0, WRSEL = 3, PAGEWREN = 1, MSEL = 2): Page write command.
0x20 = 00 (EEPR = 0, EEP_LOAD = 0, WRSEL = 0, PAGEWREN = 0, MSEL = 0): Return to the SPI control.

Loading procedure
0x20 = C0 (EEPR = 1, EEP_LOAD = 1, WRSEL = 0, PAGEWREN = 0, MSEL = 0): Data load command.
0x20 = 80 (EEPR = 1, EEP_LOAD = 0, WRSEL = 0, PAGEWREN = 0, MSEL = 0): Return to EEPR standby state.
0x20 = 00 (EEPR = 0, EEP_LOAD = 0, WRSEL = 0, PAGEWREN = 0, MSEL = 0): Return to the SPI control.

Operation Sequence

1 Start-up & Turn-off Sequence

1.1 Normal Start-up (No SPI Communication, EN Pin Control Start-up)

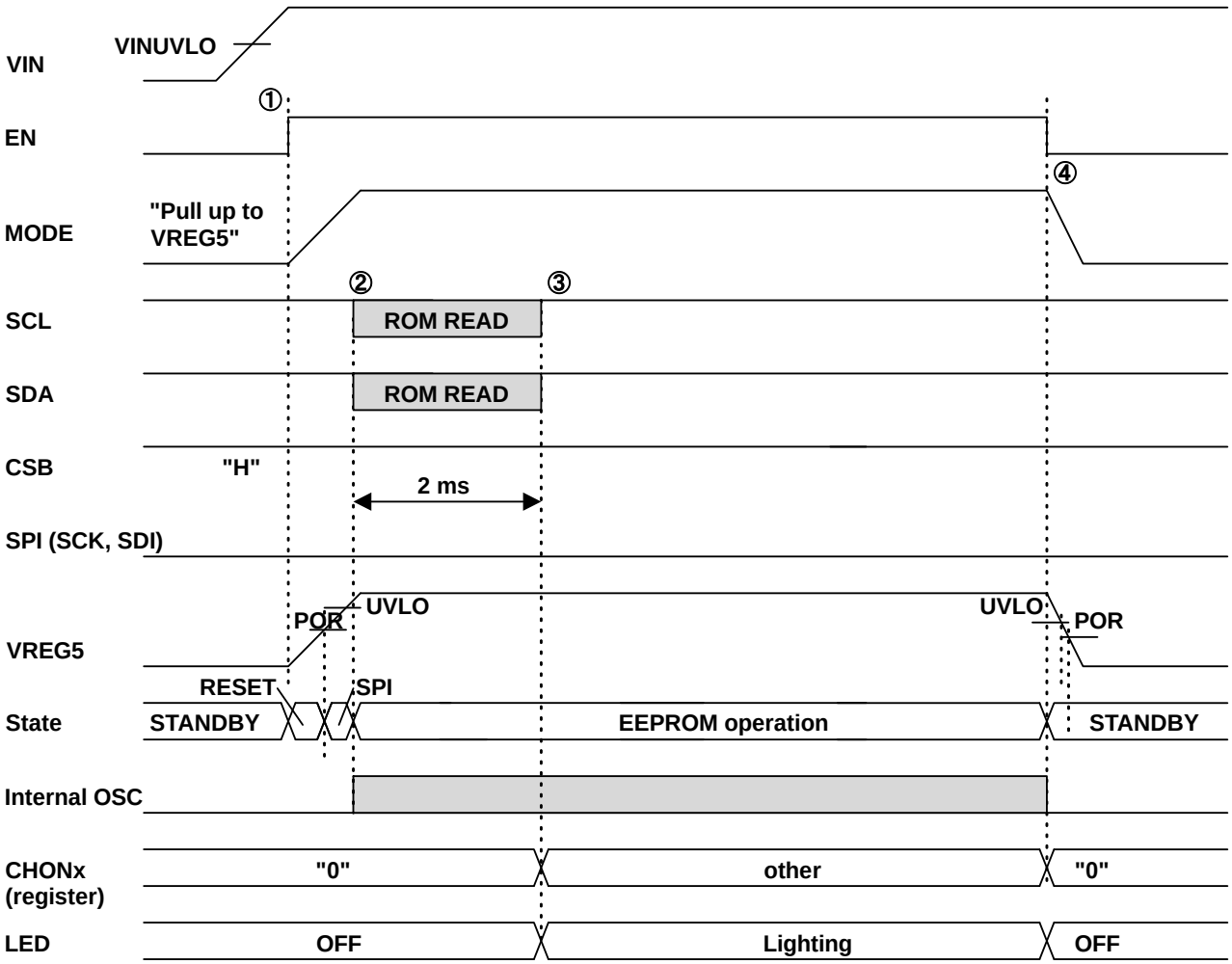


Figure 44. Start-up Sequence for EN Pin Control

When you light the LED by EN pin control, follow the sequence below.

① Start the circuit with EN = H (To RESET state).
② Data loading starts from EEPROM after VREG5 UVLO is released. (To EEPROM operation state).
③ After loading is completed, each channel starts operation by EEPROM setting.
④ After turning off VREG5 with EN = L, go to standby state (To STANDBY state).

1 Start-up & Turn-off Sequence – continued

1.2 Normal Start-up (No SPI Communication, VIN Start-up)

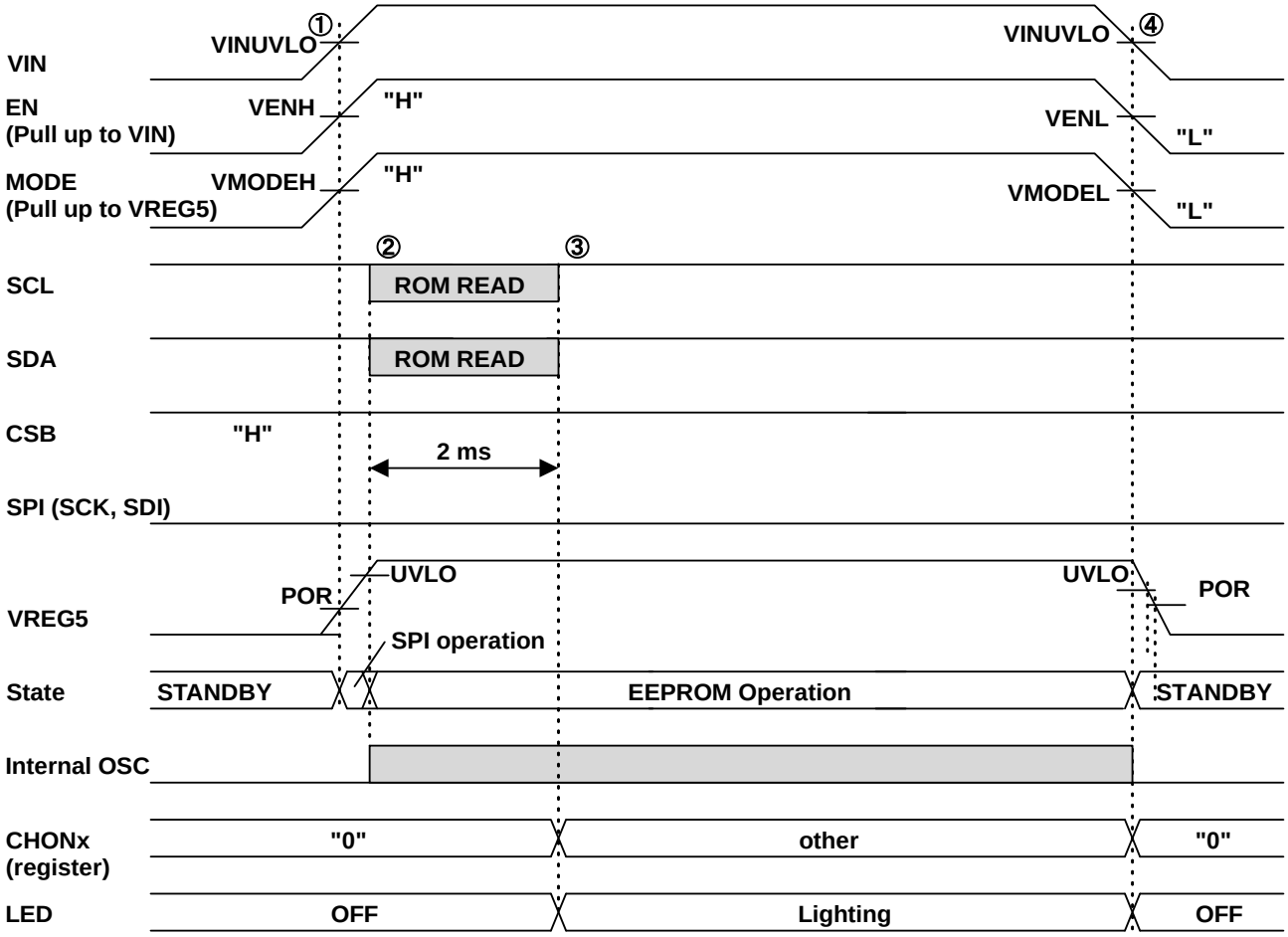


Figure 45. Start-up Sequence for VIN Pin Control

When you light the LED by VIN pin control, follow the sequence below.

① Circuit start after VIN UVLO is released (To SPI operation state).
② Data loading starts from EEPROM after VREG5 UVLO is released.
③ After loading is completed, each channel starts operation by EEPROM setting.
④ Enter standby state after VIN UVLO is detected (To STANDBY state).

1 Start-up & Turn-off Sequence – continued

1.3 STAND-ALONE Start-up (EN = H, MODE = L, CSB = L)

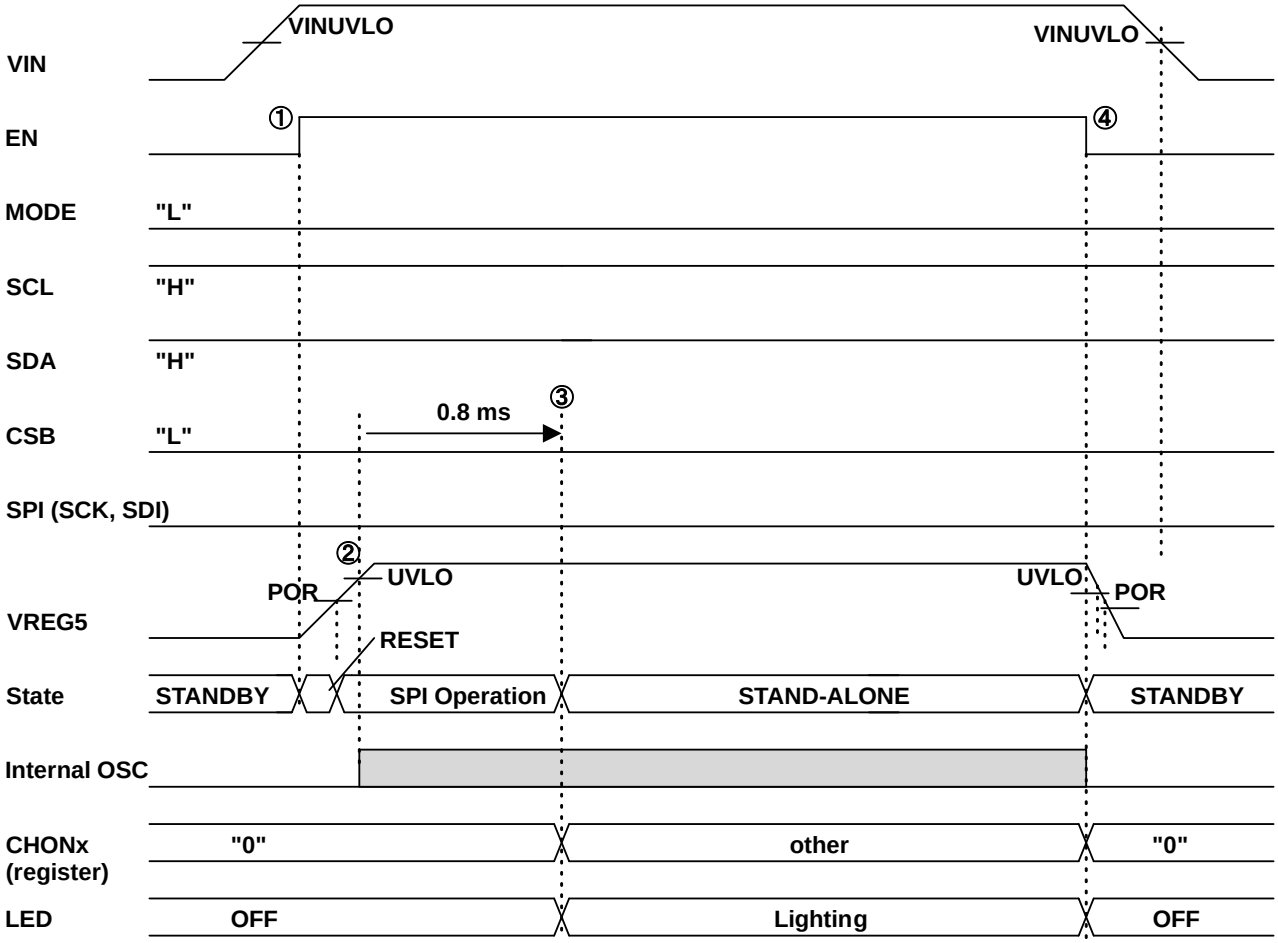


Figure 46. Start-up Sequence for STAND-ALONE

When you light the LED by STAND-ALONE, follow the sequence below.

① Start the circuit with EN = H (To RESET state)
② Start of 0.8 ms count since CSB = L, after VREG5 UVLO is released (To SPI operation state).
③ Start operation in STAND-ALONE mode after 0.8 ms (To STAND-ALONE state).
④ Enter standby state with EN = L (To STANDBY state).

1 Start-up & Turn-off Sequence – continued

1.4 Normal Start-up (SPI Operation)

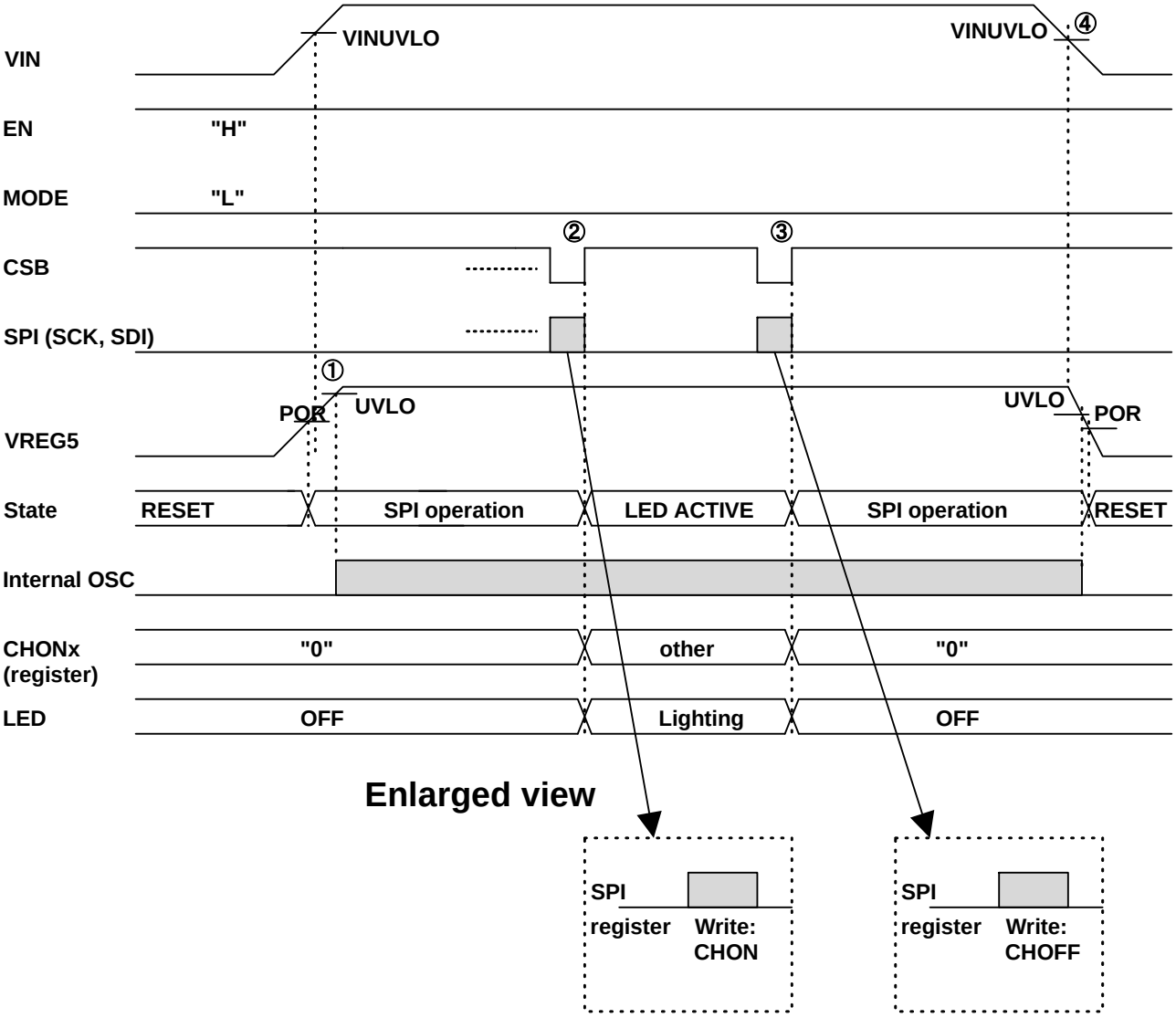


Figure 47. Start-up Sequence for Normal Operation

When you light the LED by general SPI control, follow the sequence below.

① VREG5 UVLO release.
② Turn on each channel by setting CHONx = 1.
③ Each channel is turned off by setting CHONx = 0.
④ Operation off with VIN UVLO detection.

1 Start-up & Turn-off Sequence – continued

1.5 Sleep Mode

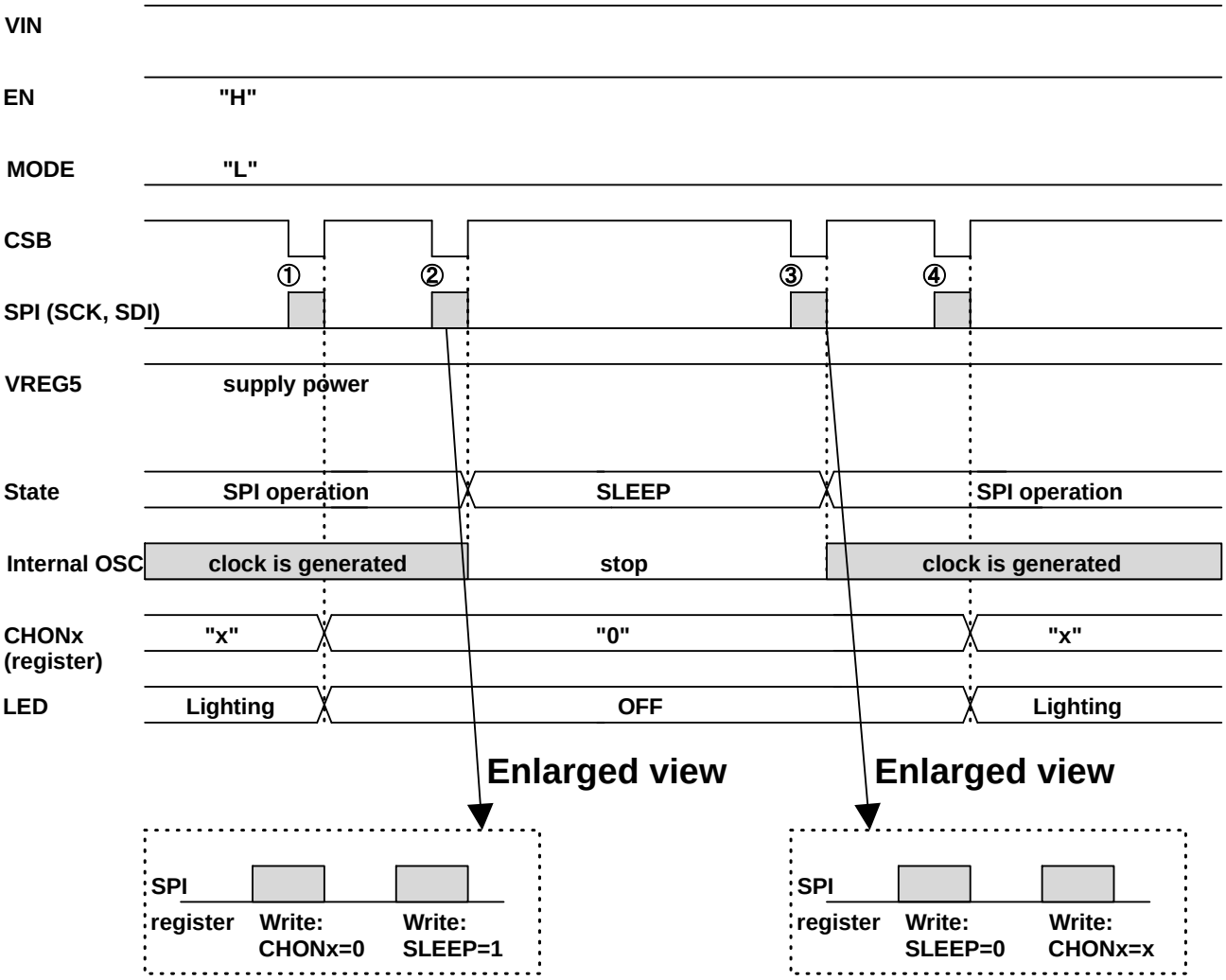


Figure 48. Sequence for SLEEP Mode

When you use SLEEP mode by the SPI control, follow the sequence below.

① CHONx = 0, this IC stop lighting and go “STANDBY“ state.
② SLEEP = 1, internal oscillator stops. (Low quiescent current by stopping internal clock)
③ SLEEP = 0, internal oscillator starts.
④ CHONx = x, this IC starts lighting and go “LED ACTIVE” state.

Operation Sequence – continued

2 Error Sequence

2.1 Error Sequence for “CRC Error”

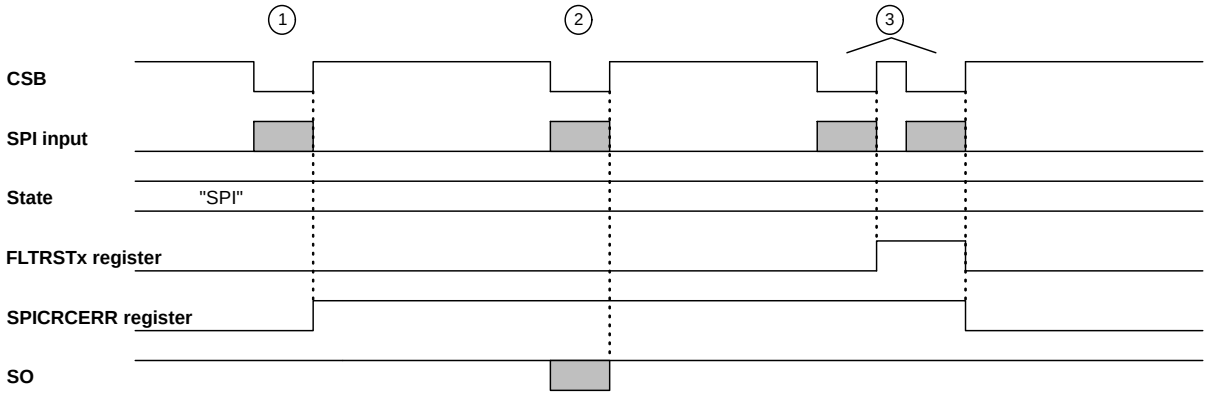


Figure 49. CRC Error Detection

① CRC error is detected when data sent does not match the CRC value in the SPI command. This mismatch can be caused by wrong data or noise in the SPI line. Write operation is not executed in the IC. Target register is not updated. In this case, CRC error status register is updated to H. Protection is latched automatically, sending the SPI command with correct CRC does not clear CRCERR status register.
② MCU sends read command to status registers to confirm CRC status register.
③ MCU sends FLTRSTx and dummy SPI (data 0x00) to release the status register.

2.2 Error Sequence for “WDT Error”

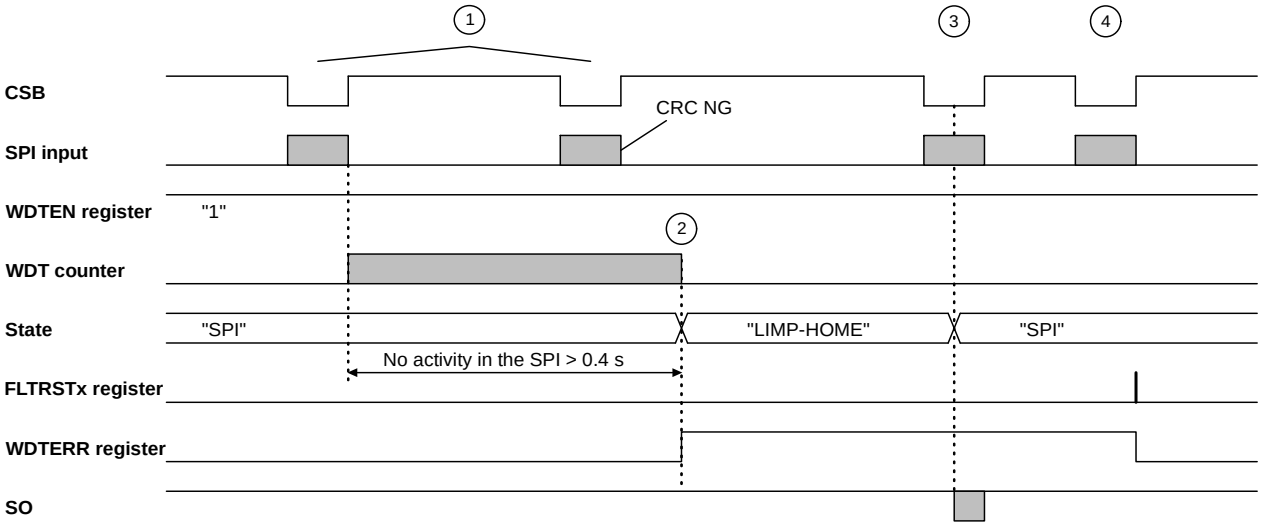


Figure 50. WDT Error Detection

① Watch Dog Timer starts to count at SPI state. When there is no "CRC OK" detected in more than 0.4 s, IC detects WDT error.
② WDT is detected, it sets the corresponding status register WDTERR to H and state changes from SPI to LIMP-HOME.
③ MCU sends read command to status register to confirm WDT status. This event releases LIMP-HOME mode.
④ WDT detection is latches automatically, MCU must send FLTRSTx to clear the WDTERR status register and FAULT_Bx output.

Operation Sequence – continued

3 A/D Control Sequence

This IC can control A/D monitoring mode by ADMODE register. When ADMODE is H, ADC is used for BINx, VIN and NTCx derating. When ADMODE is L, ADC can be operated manually.

3.1 ADMODE = 1 (Auto Mode)

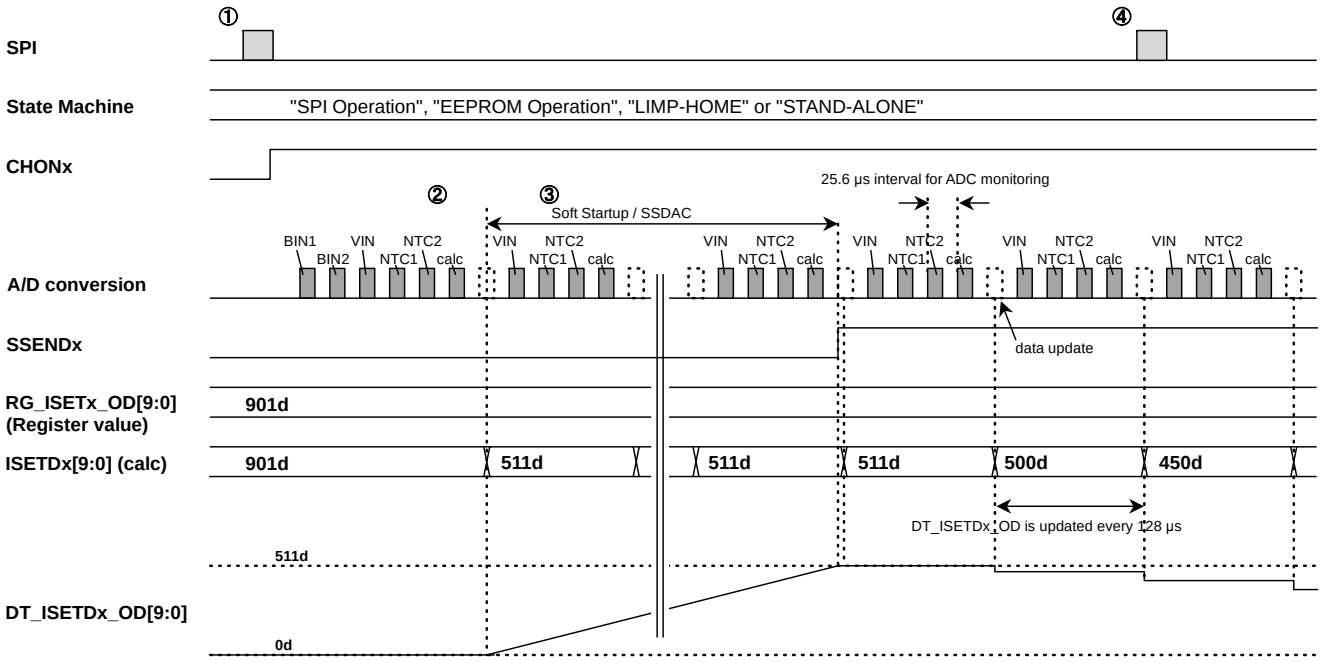


Figure 51. A/D Control (ADMODE = 1)

① Automatic ADC Monitoring only operates when CHON output of either channel is turned on at ADMODE = H. CHON is enabled by writing using SPI, update by EEPROM load or by going to “STAND-ALONE” state. Whenboth ADMODE and either CHON channel are H, voltage from the BINx, VIN and NTCx pins is read for one time. This will be used to compute for the first ISETDx value which will be the reference value for slow startup or SSDAC function.

② After the first calculation is finished, ISETDx is updated and either slow startup or SSDAC operates based on the initial status of SSUx pin. DT_ISETDx_OD increments by 1 until it reached the value of calculated ISETDx. The value is updated even during increment.

③ The automatic ADC monitoring continues but this time, only the VIN and NTCx pins will be monitored repeatedly. The interval between ADC monitoring is 25.6 µs while the interval of updating ISETDx output is 128 µs. When the pin voltage is changed, calculated ISETDx value will also change based on the derating formula and the result is reflected to DT_ISETDx_OD output.

④ Register settings for derating (VINDSETx, NTCSETx, VINDGAINx and NTCGAINx) can also be update if SPI access is available. New value of ISETDx is then calculated and reflected on next update timing. The output DT_ISETDx_OD is connected to DAC which is then connected to the LED driver to control the LED current.

3. A/D Control Sequence – continued

3.2 ADMODE = 0 (manual mode)

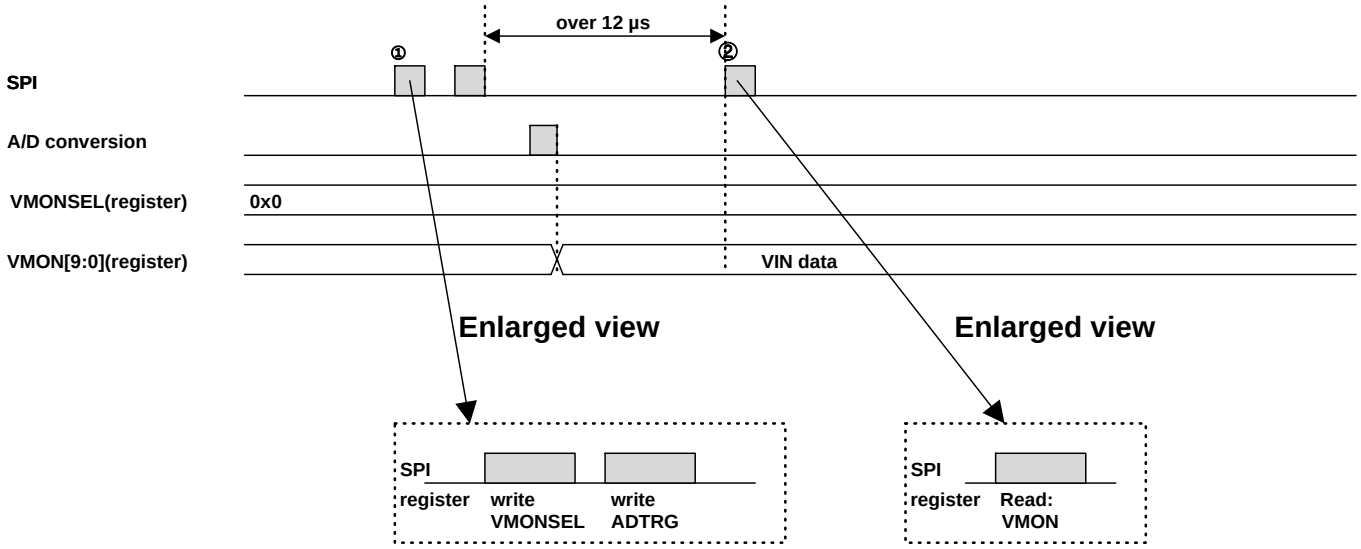


Figure 52. A/D Control (ADMODE = 0)

① In order to monitor the pin voltage by ADC, VMONSEL register should be updated by SPI. For example, for V_{IN} set VMONSEL to 4'h0 to enable monitoring at the VIN pin. A/D starts to convert by ADTRG = 1. The value is stored to VMON register which can be read by SPI.
② ADC converter takes around 11 µs to finish conversion. VMON register is available after 12 µs (include margin). SPI read is sent to confirm value of VMON register.

Typical Performance Curves
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

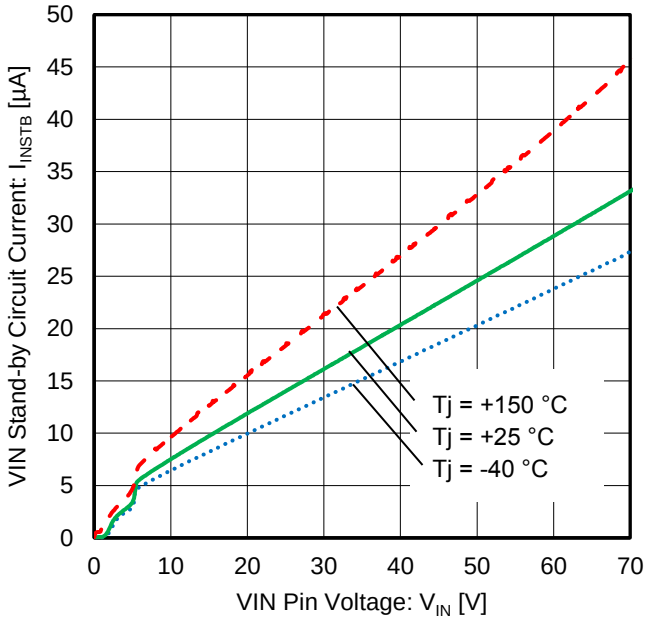


Figure 53. VIN Stand-by Circuit Current vs VIN Pin Voltage

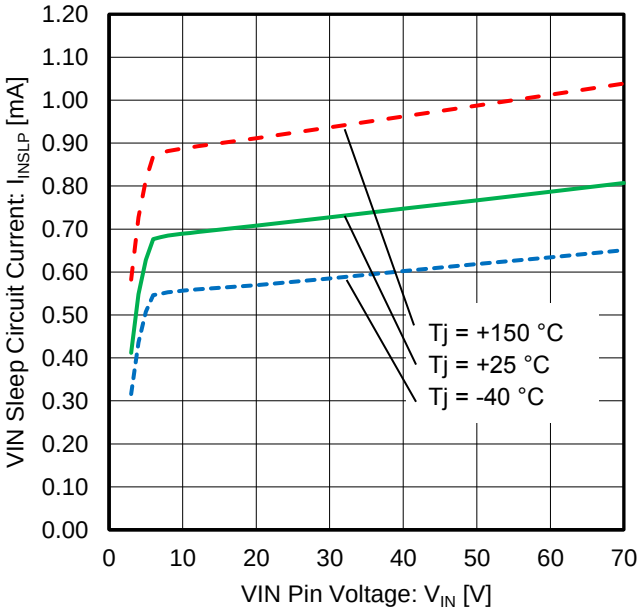


Figure 54. VIN Sleep Circuit Current vs VIN Pin Voltage

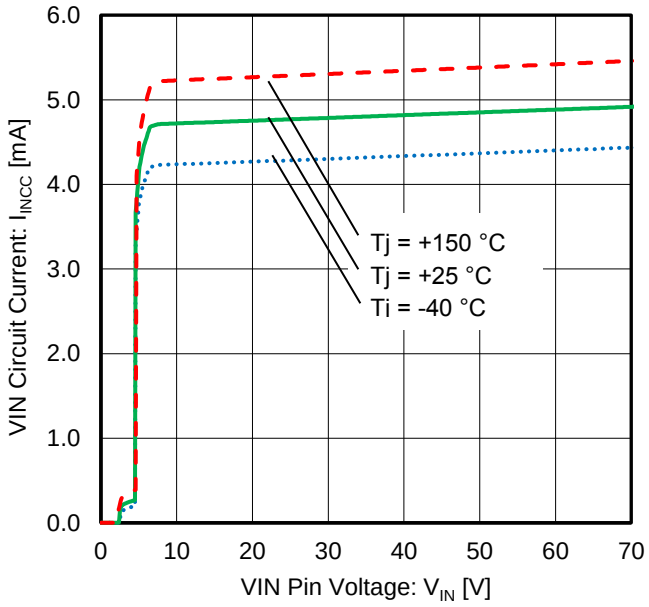


Figure 55. VIN Circuit Current vs VIN Pin Voltage

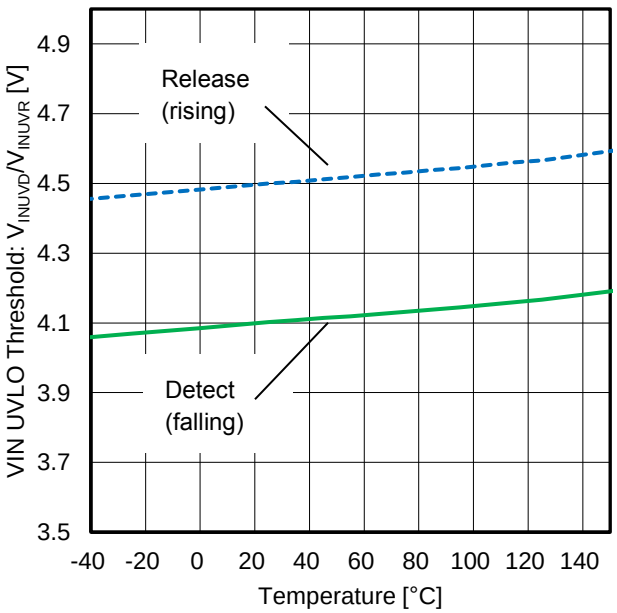


Figure 56. VIN UVLO Threshold Voltage vs Temperature

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

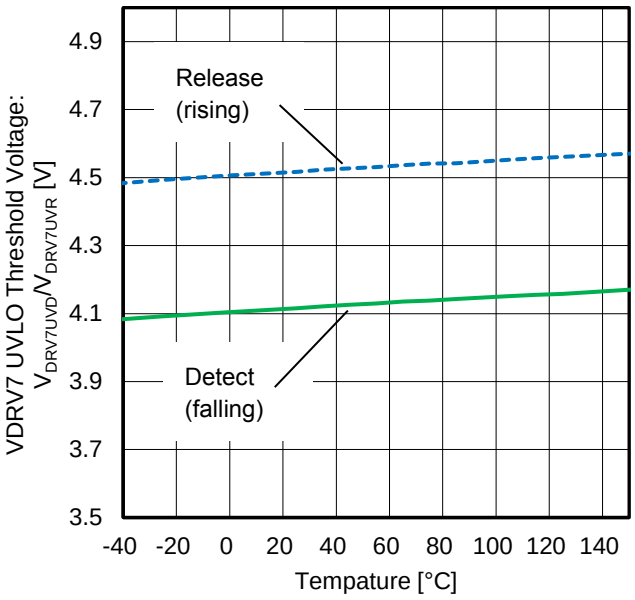


Figure 57. VDRV7 UVLO Threshold Voltage vs Temperature

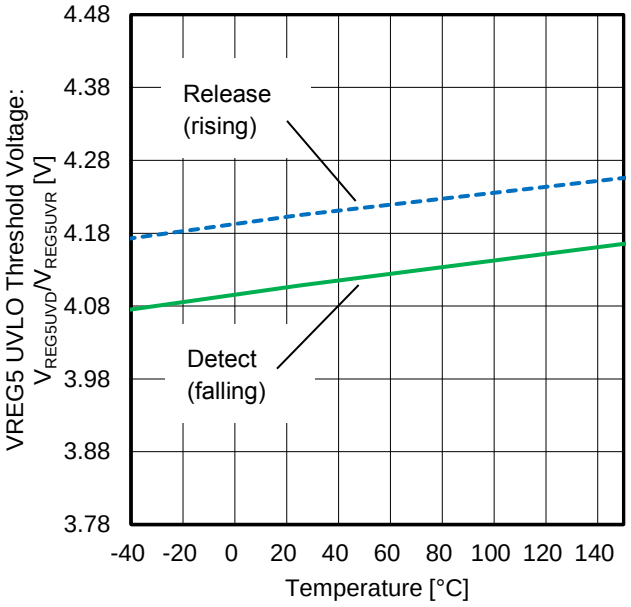


Figure 58. VREG5 UVLO Threshold Voltage vs Temperature

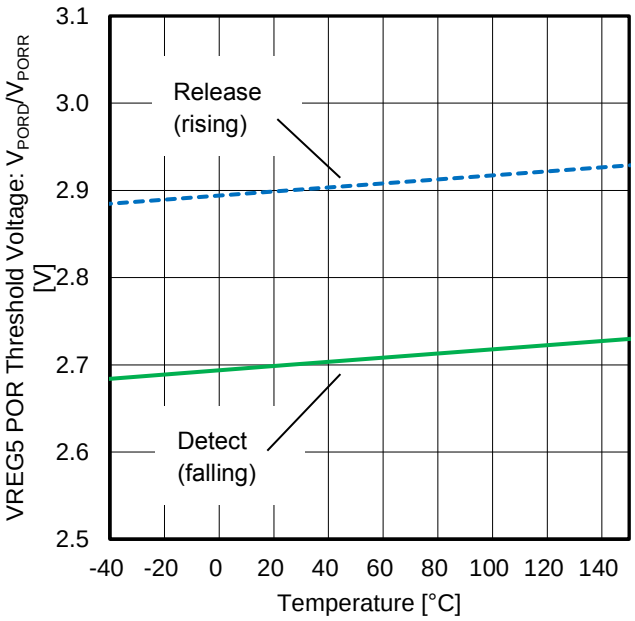


Figure 59. VREG5 POR Threshold Voltage vs Temperature

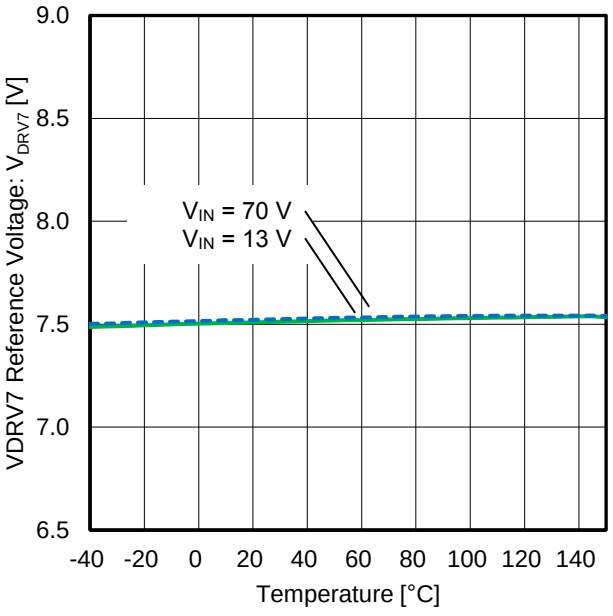


Figure 60. VDRV7 Reference Voltage vs Temperature
I_{VDRV7} = No load

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

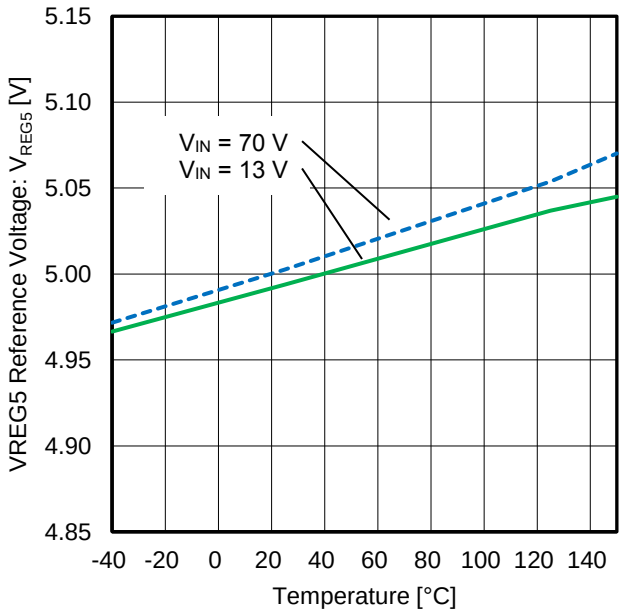


Figure 61. VREG5 Reference Voltage: vs Temperature
I_{VREG5} = No load

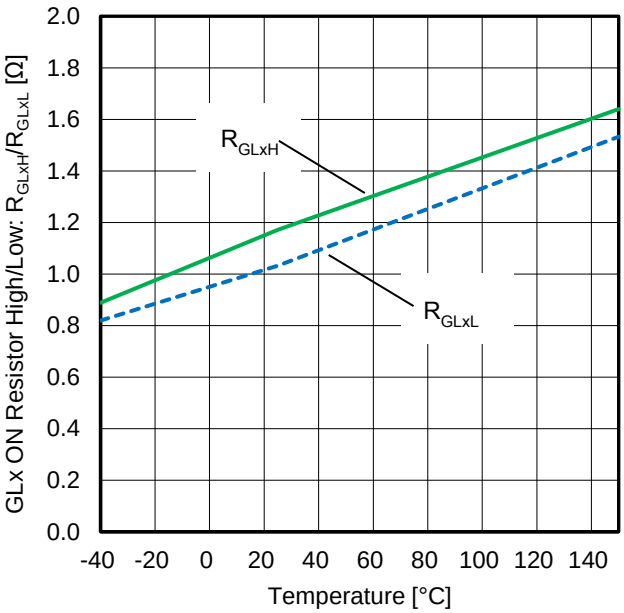


Figure 62. GLx ON Resistor High/Low vs Temperature
I_{GLx} = 10 mA load/input

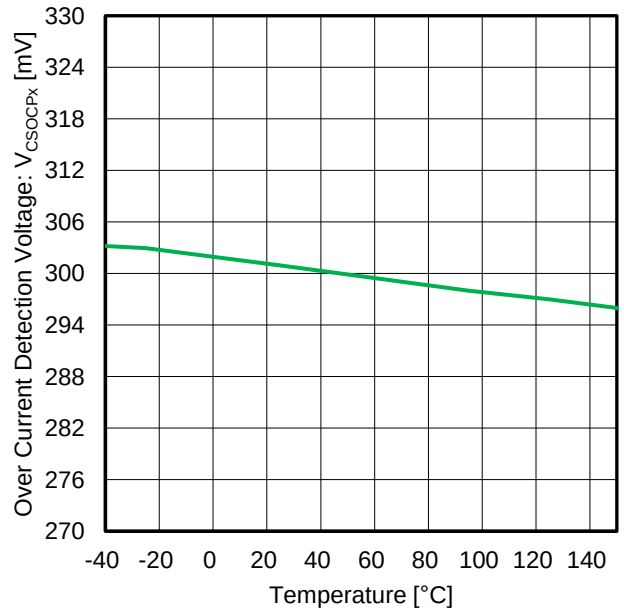


Figure 63. Over Current Detection Voltage vs Temperature
OCPSETx[1:0] = 3

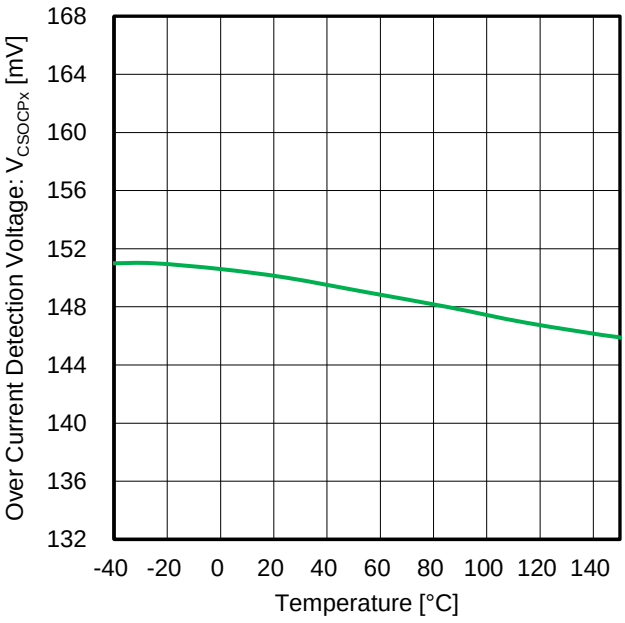


Figure 64. Over Current Detection Voltage vs Temperature
OCPSETx[1:0] = 1 (initial)

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

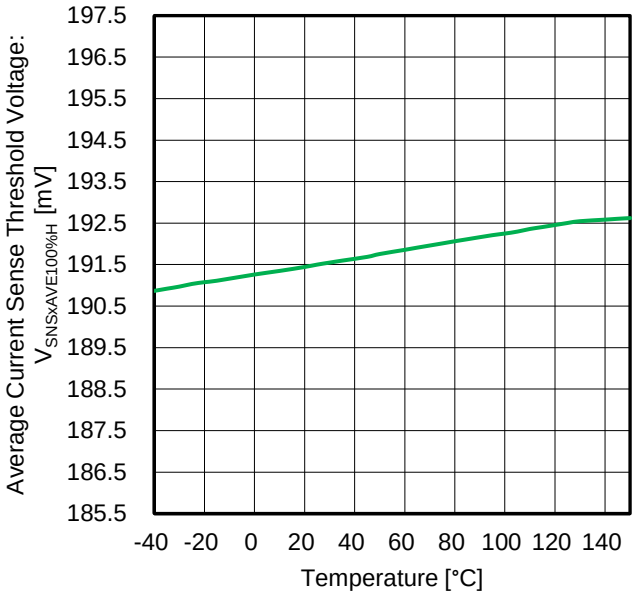


Figure 65. Average Current Sense Threshold Voltage vs Temperature
ISETx[9:0] = 1023

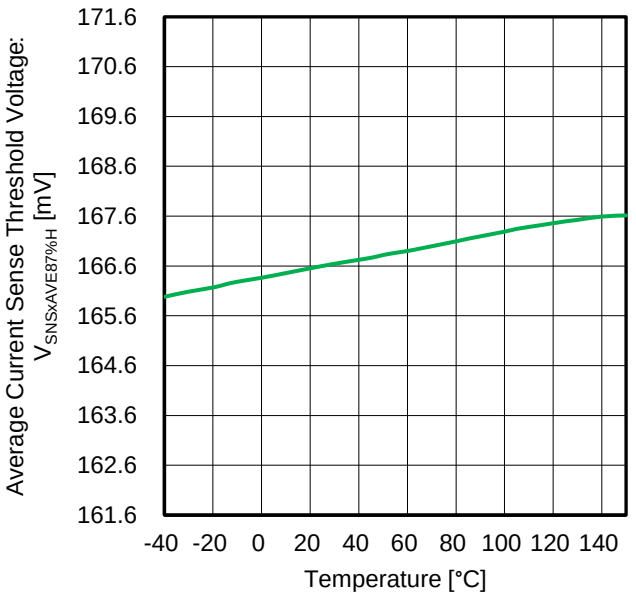


Figure 66. Average Current Sense Threshold Voltage vs Temperature
ISETx[9:0] = 901 (initial)

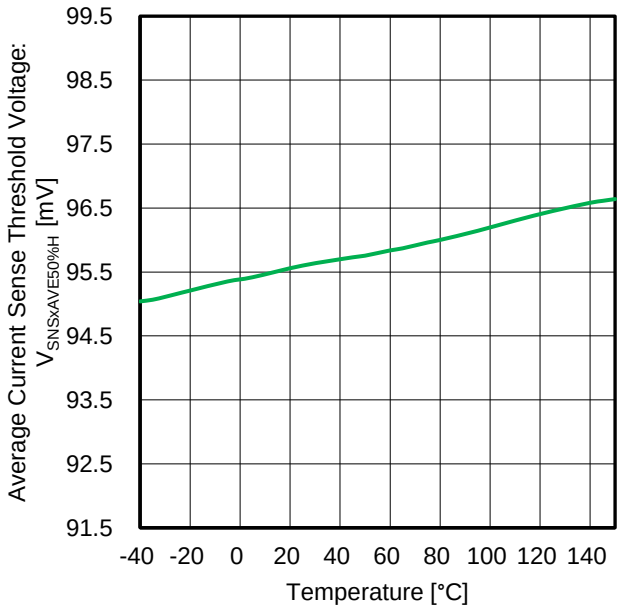


Figure 67. Average Current Sense Threshold Voltage vs Temperature
ISETx[9:0] = 552

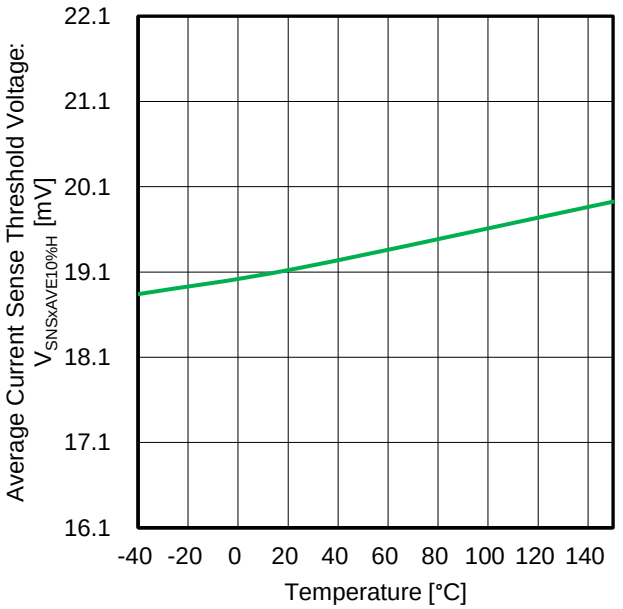


Figure 68. Average Current Sense Threshold Voltage vs Temperature
ISETx[9:0] = 176

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

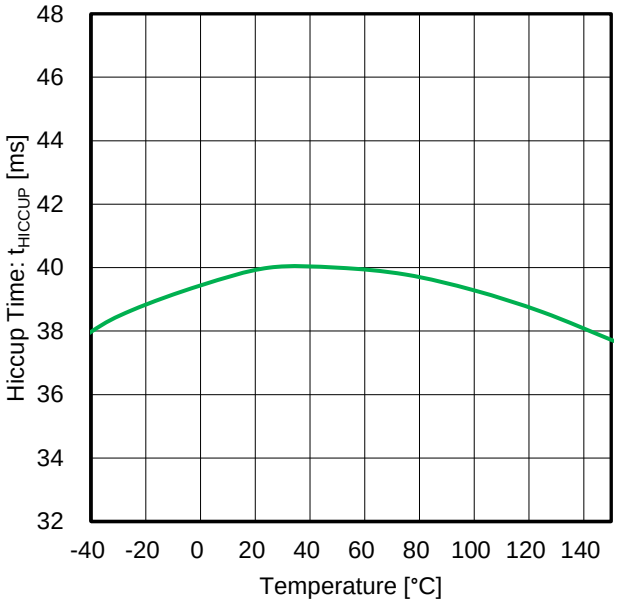


Figure 69. Hiccup Time vs Temperature

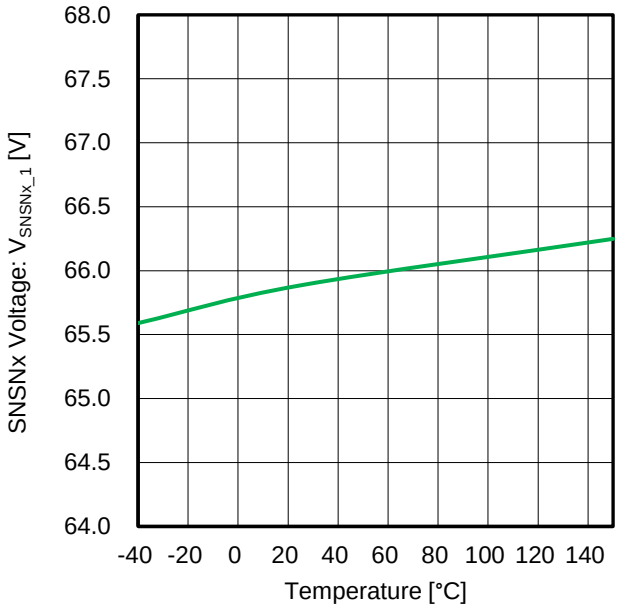


Figure 70. SNSNx Voltage vs Temperature
ISETx[9:0] = 901, VMODEx = 1

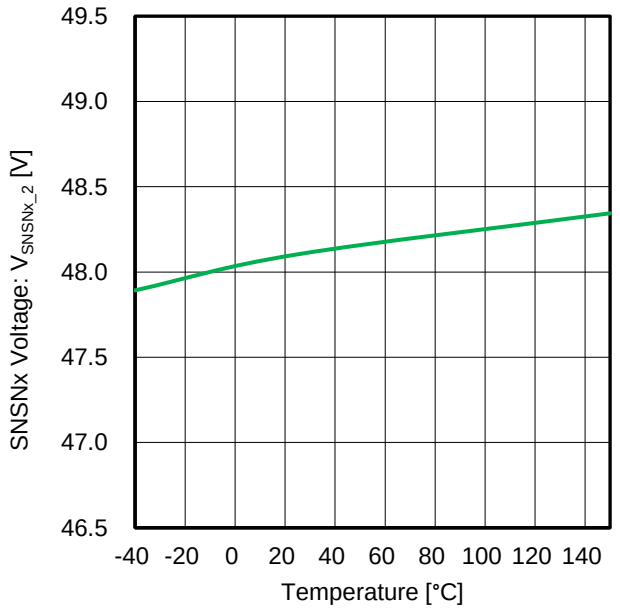


Figure 71. SNSNx Voltage vs Temperature
ISETx[9:0] = 655, VMODEx = 1

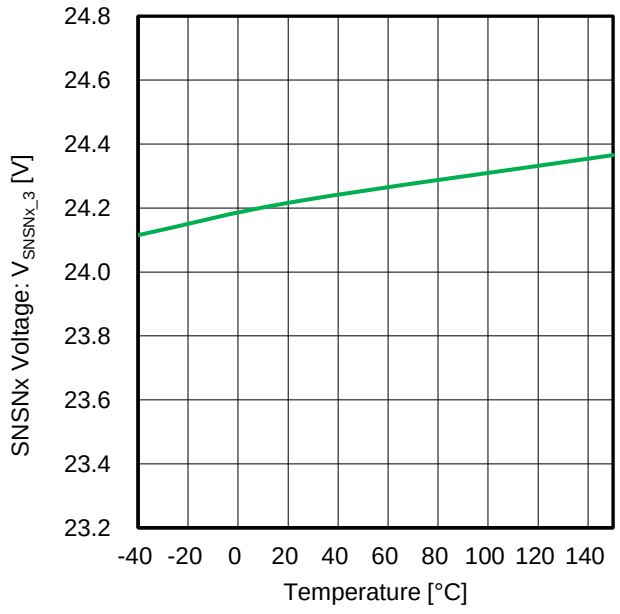


Figure 72. SNSNx Voltage vs Temperature
ISETx[9:0] = 328, VMODEx = 1

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

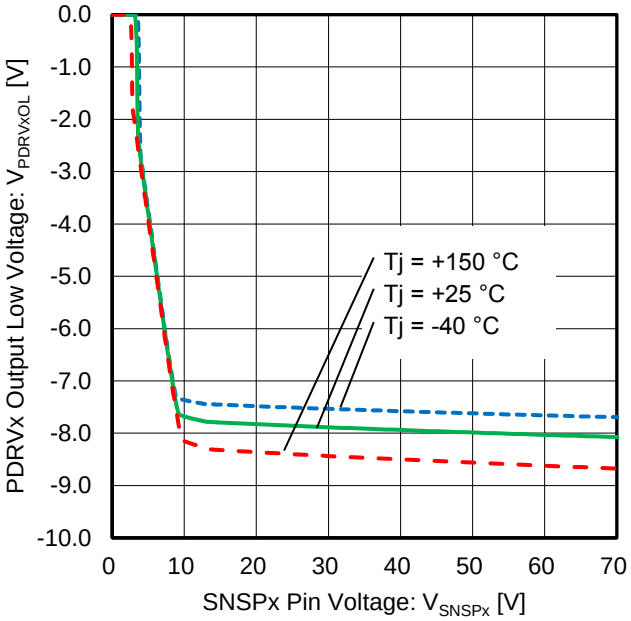


Figure 73. PDRVx Output Low Voltage vs SNSPx Pin Voltage

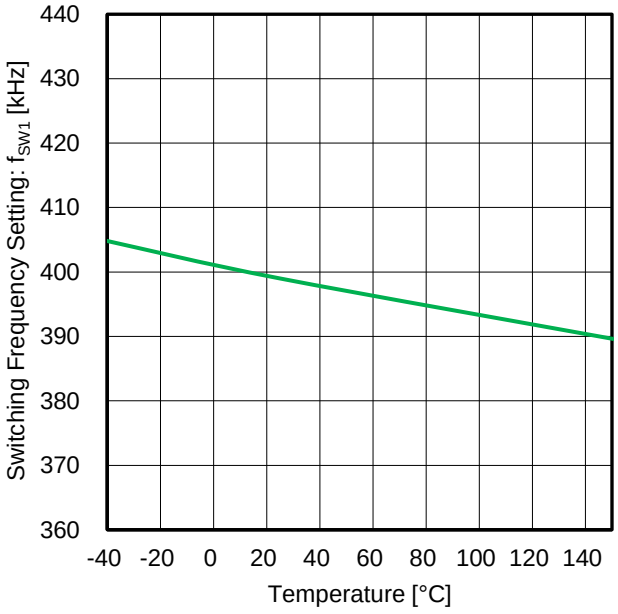


Figure 74. Switching Frequency Setting vs Temperature
R_{RT} = 47 kΩ, FRT[3:0] = 5 (initial)

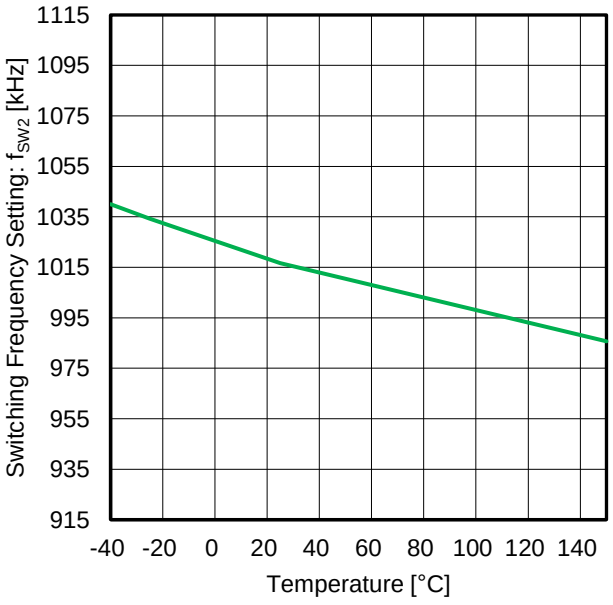


Figure 75. Switching Frequency Setting vs Temperature
R_{RT} = 47 kΩ, FRT[3:0] = 15

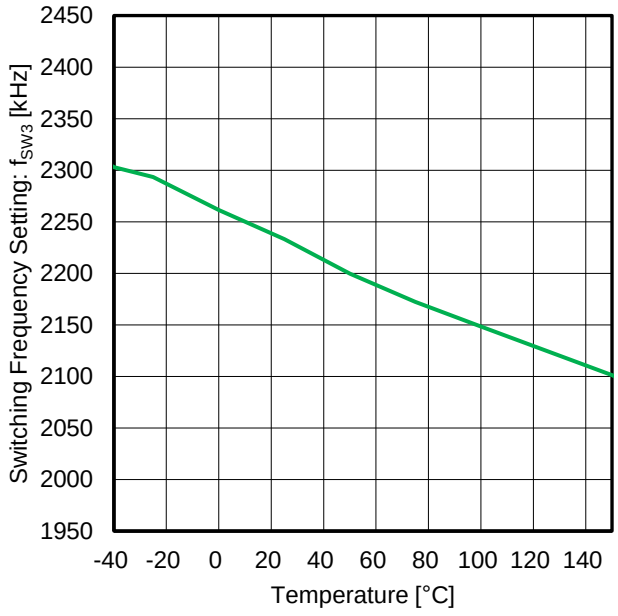


Figure 76. Switching Frequency Setting vs Temperature
R_{RT} = 7.5 kΩ, FRT[3:0] = 5 (initial)

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

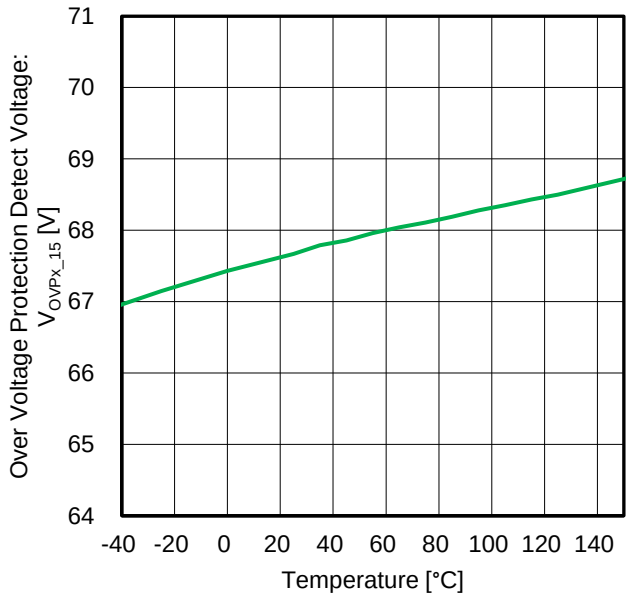


Figure 77. Over Voltage Protection Detect Voltage vs Temperature
V_{SNSPx} rising, OVPSETx[3:0] = 15 (initial)

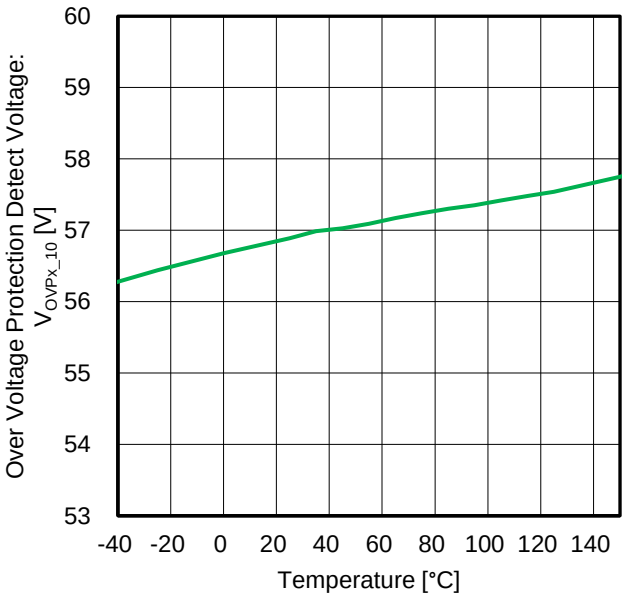


Figure 78. Over Voltage Protection Detect Voltage vs Temperature
V_{SNSPx} rising, OVPSETx[3:0] = 10

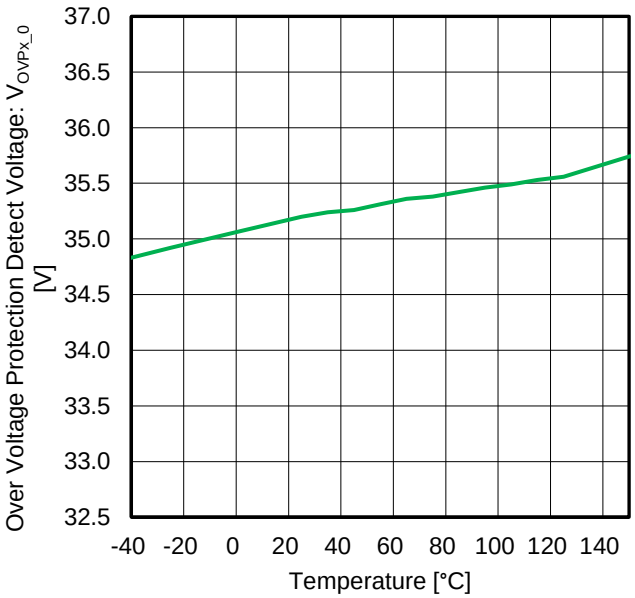


Figure 79. Over Voltage Protection Detect Voltage vs Temperature
V_{SNSPx} rising, OVPSETx[3:0] = 0

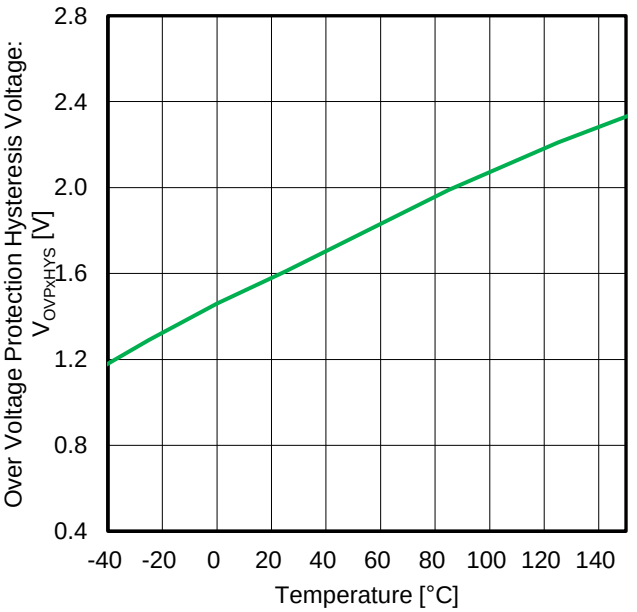


Figure 80. Over Voltage Protection Hysteresis Voltage vs Temperature
OVPSETx[3:0] = 15 (initial)

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

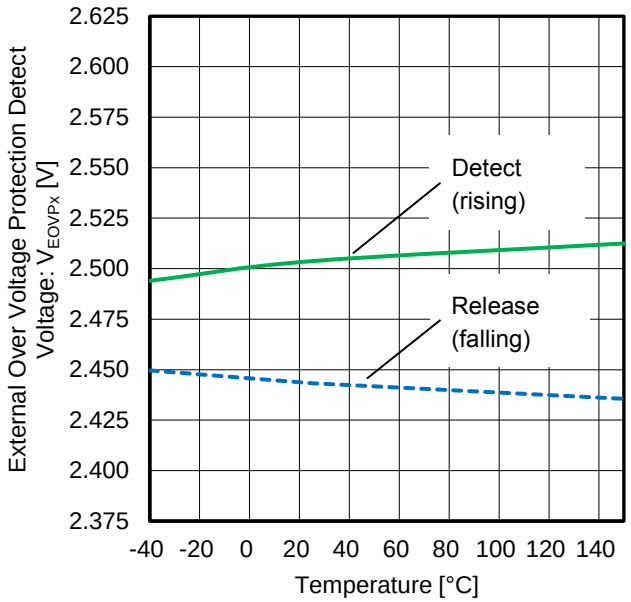


Figure 81. External Over Voltage Protection Detect Voltage vs Temperature
V_{SSUx} rising/falling

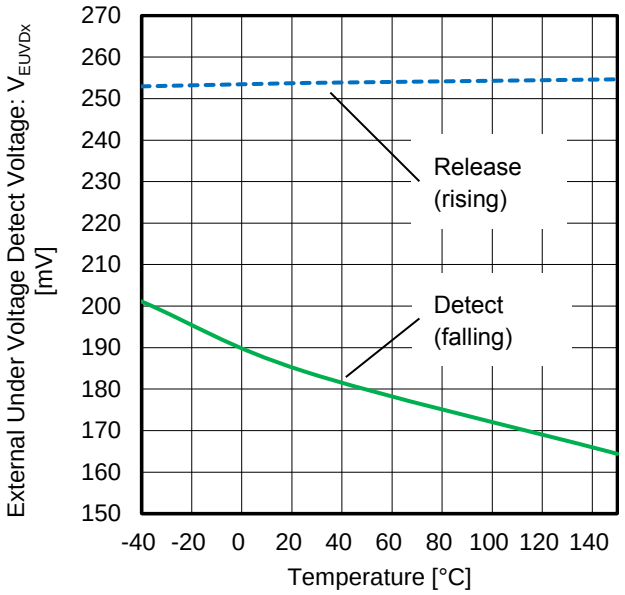


Figure 82. External Under Voltage Detect Voltage vs Temperature
V_{SSUx} rising/falling

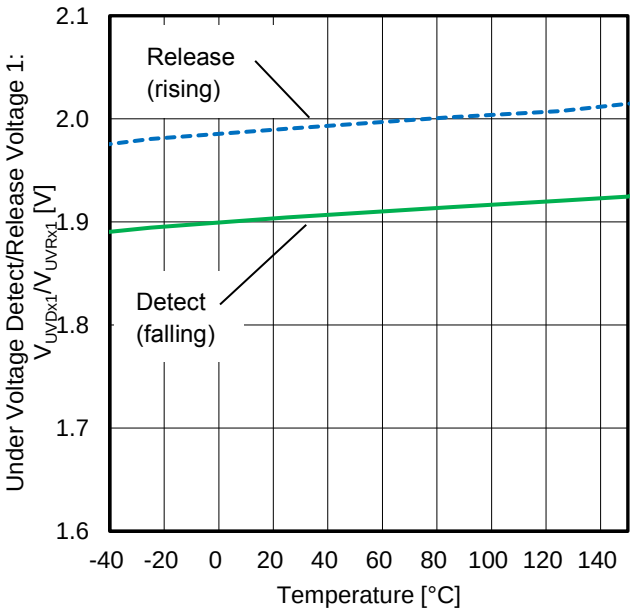


Figure 83. Under Voltage Detect/Release Voltage 1 vs Temperature
V_{SNSNx} rising/falling, BTBx = 0 (initial)

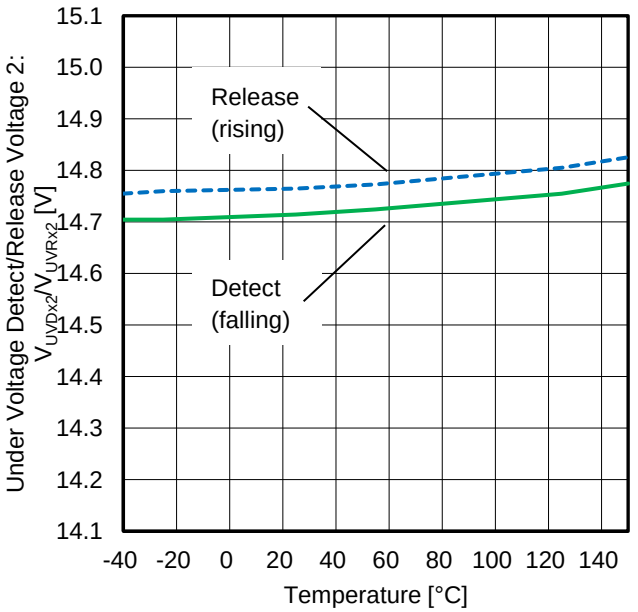


Figure 84. Under Voltage Detect/Release Voltage 2 vs Temperature
V_{SNSNx} falling/rising, BTBx = 1

Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = 25 °C)

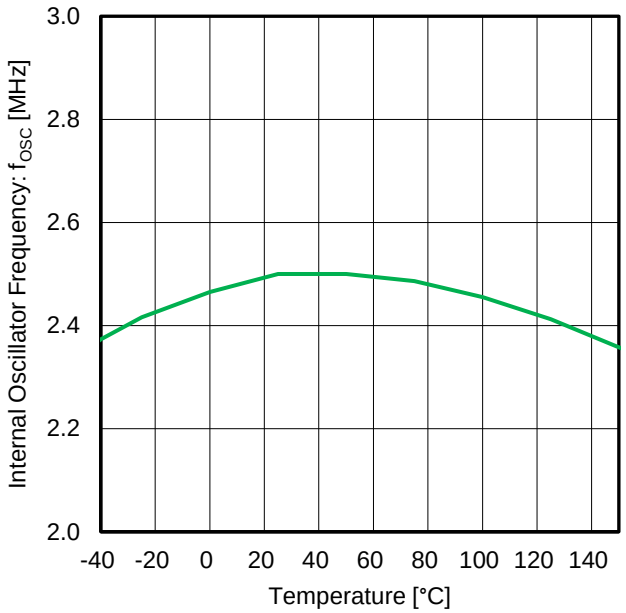


Figure 85. Internal Oscillator Frequency vs Temperature

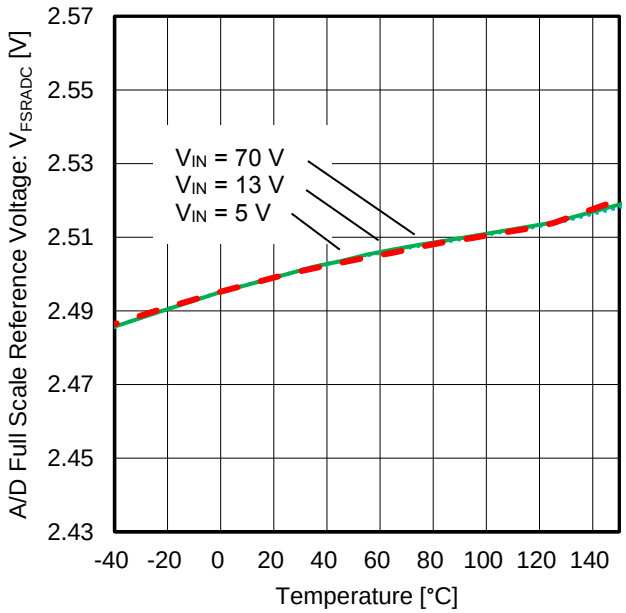


Figure 86. A/D Full Scale Reference Voltage vs Temperature

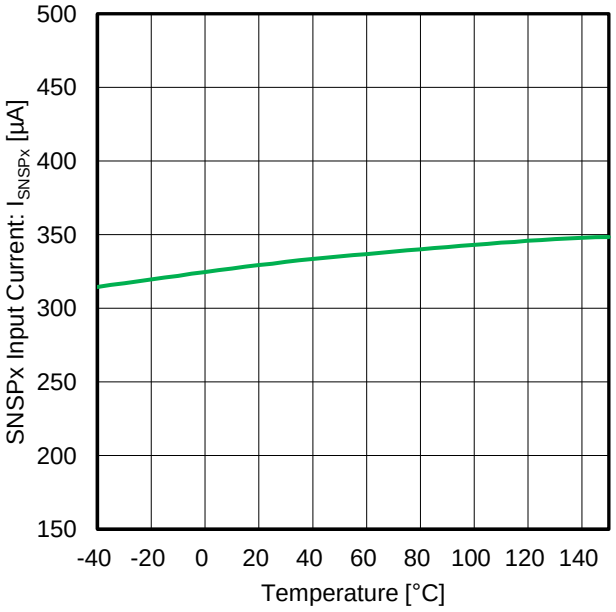


Figure 87. SNSPx Input Current vs Temperature

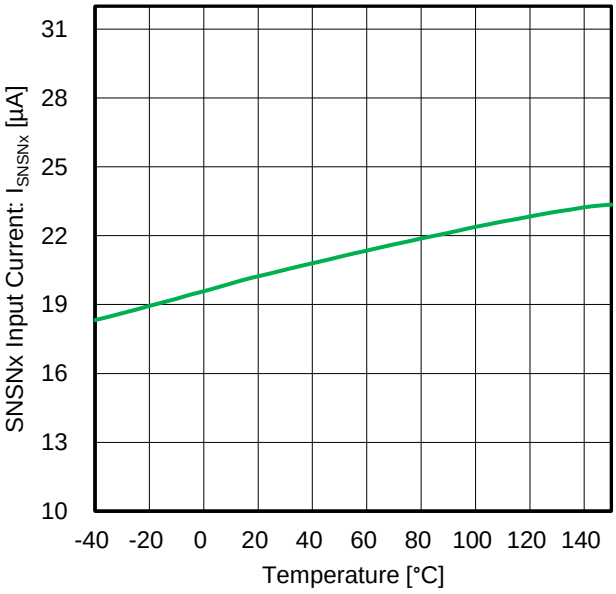


Figure 88. SNSNx Input Current vs Temperature

Application Typical Waveforms

(1 SPI Operation (CH1: Boost CH2: Boost Voltage Output))

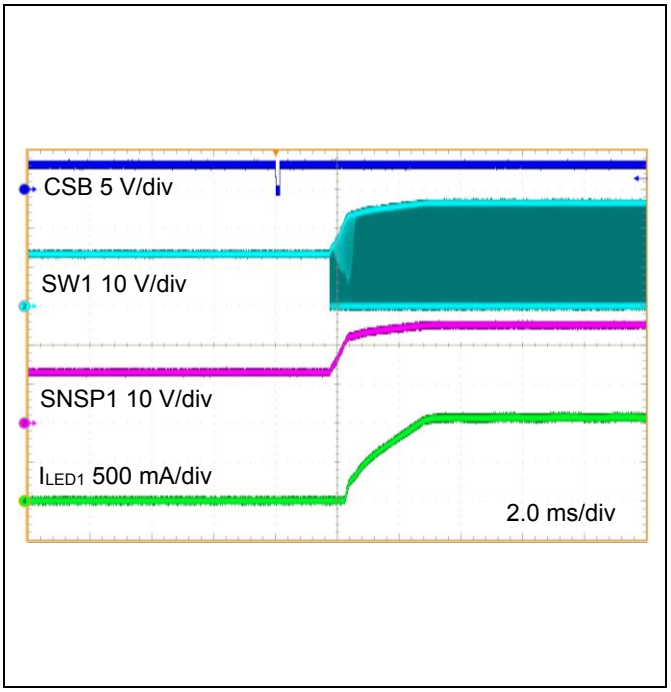


Figure 89. CH1 ON (Boost 8 LEDs Drive)
I_{LED1} = 1.04 A setting
The PWMD1 pin = H

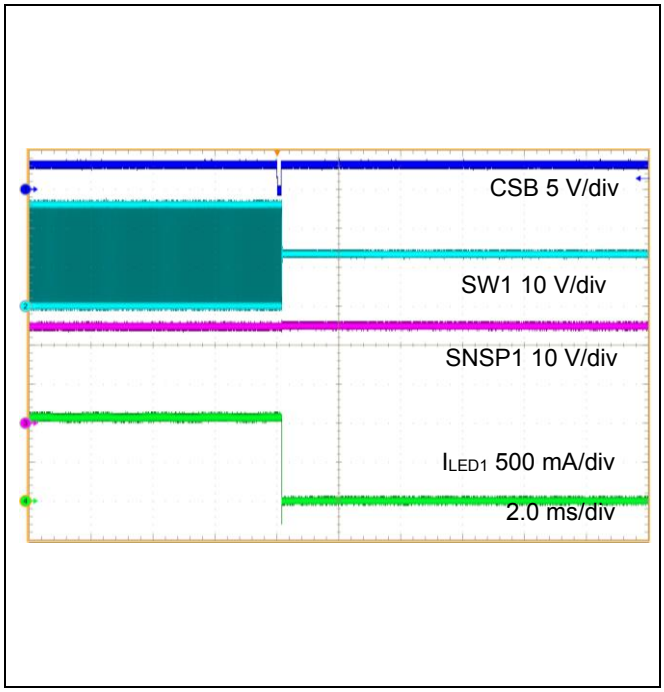


Figure 90. CH1 OFF (Boost 8 LEDs Drive)
I_{LED1} = 1.04 A setting
The PWMD1 pin = H

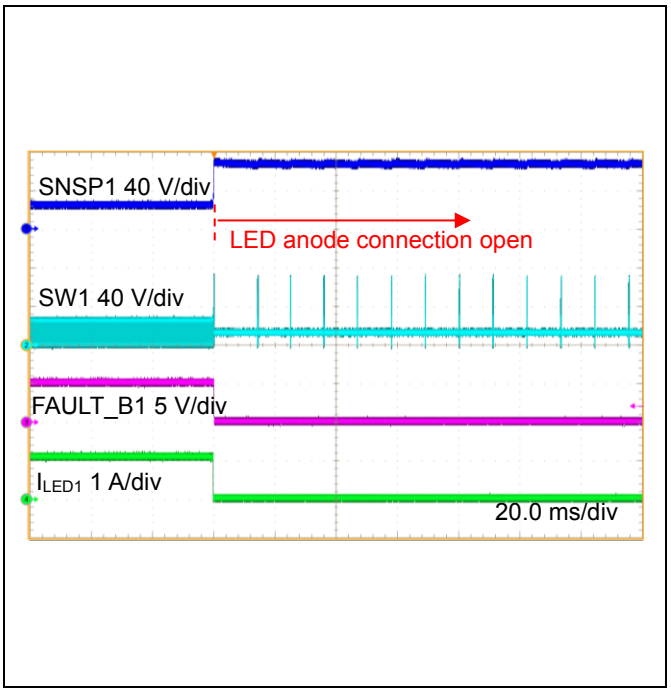


Figure 91. CH1 External Over Voltage Protection Detect
External OVP setting voltage = 55.6 V
LED anode connection open detect
The PWMD1 pin = H

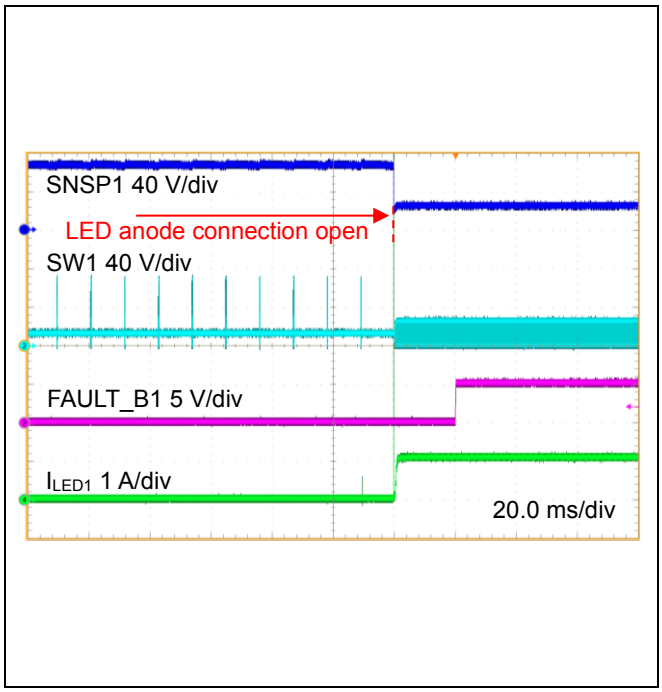


Figure 92. CH1 External Over Voltage Protection Release
External OVP setting voltage = 55.6 V
LED anode connection open release
The PWMD1 pin = H

Application Typical Waveforms - continued
(1 SPI Operation (CH1: Boost CH2: Boost Voltage Output))

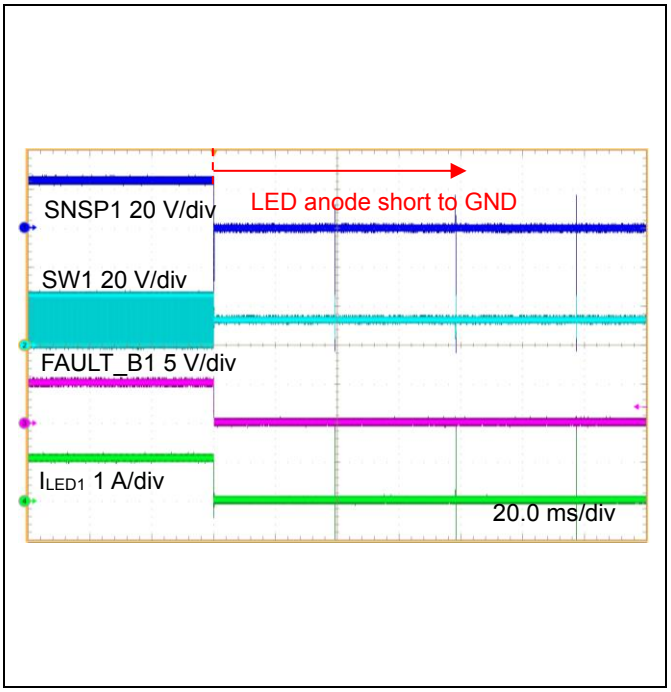


Figure 93. CH1 Short Circuit Protection Detect
LED anode short to GND detect
The PWMD1 pin = H

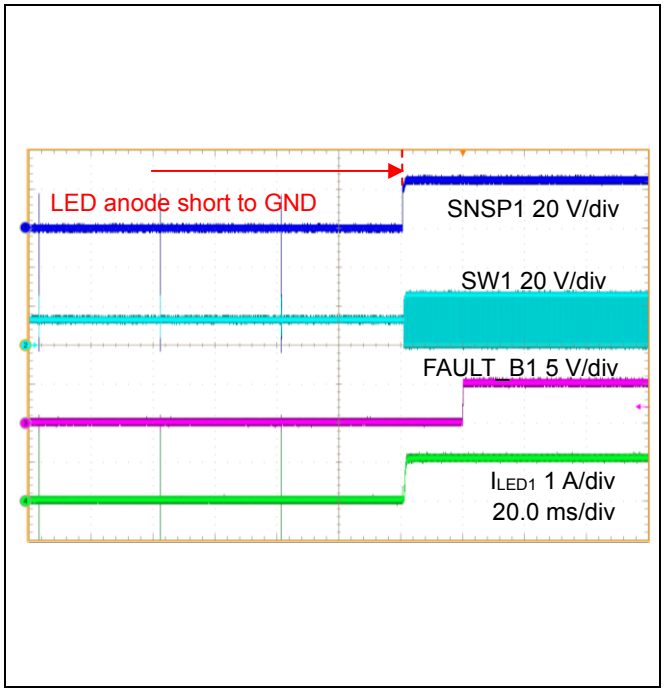


Figure 94. CH1 Short Circuit Protection Release
LED anode short to GND release
The PWMD1 pin = H

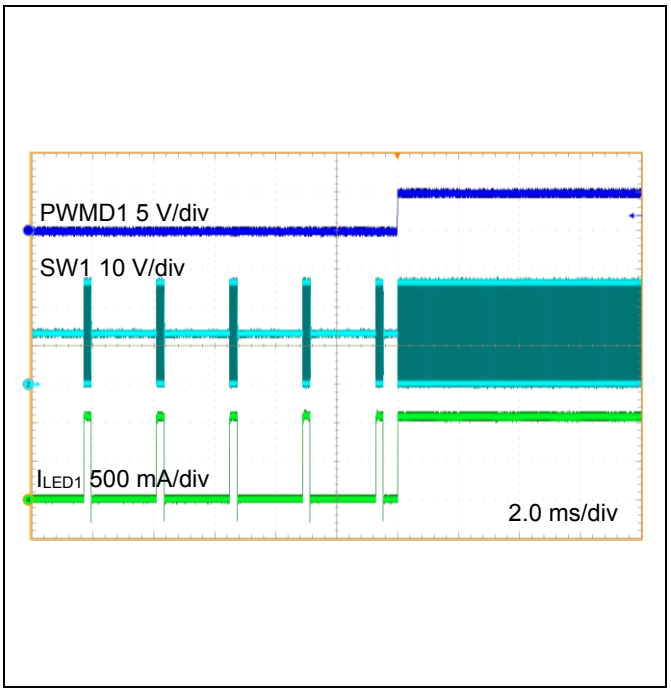


Figure 95. CH1 PWM Dimming Change 10 % to 100 %
The PWMD1 pin = L to H

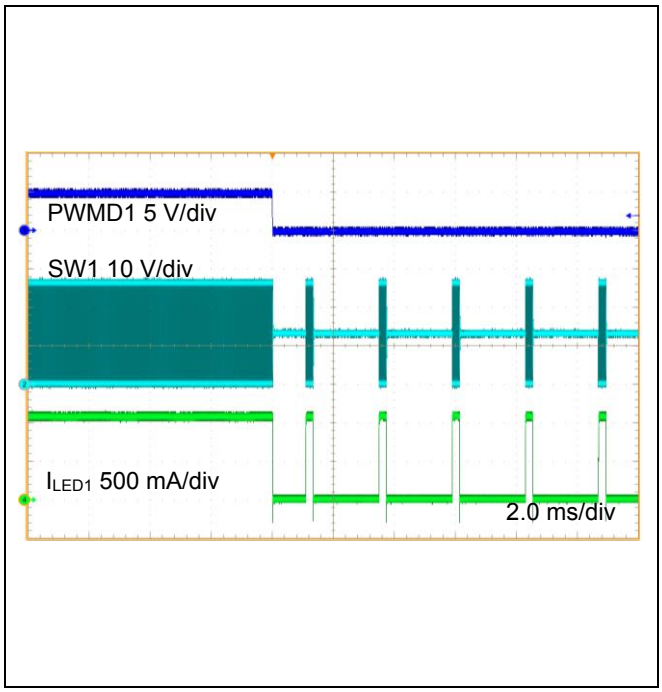


Figure 96. CH1 PWM Dimming Change 100 % to 10 %
The PWMD1 pin = H to L

Application Typical Waveforms - continued
(1 SPI Operation (CH1: Boost CH2: Boost Voltage Output))

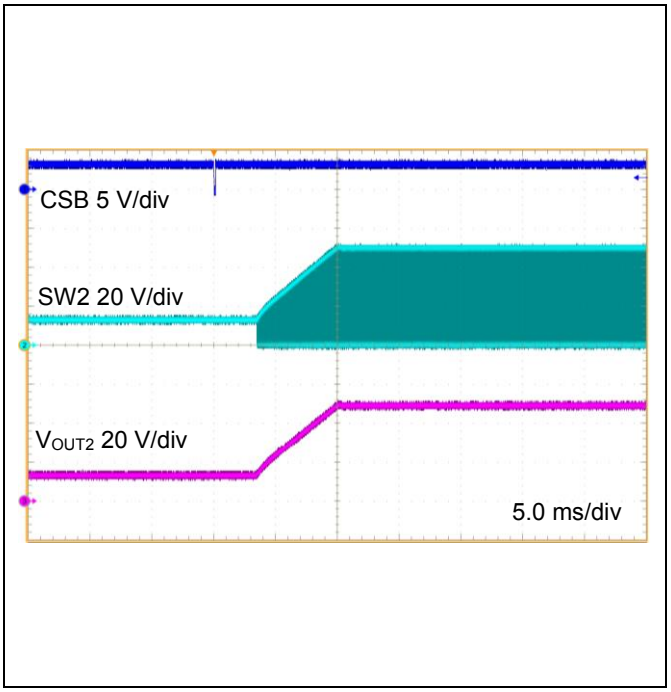


Figure 97. CH2 ON (Boost Voltage 48 V Output)
V_{OUT2} = 48 V setting (ISET2[9:0] = 655)

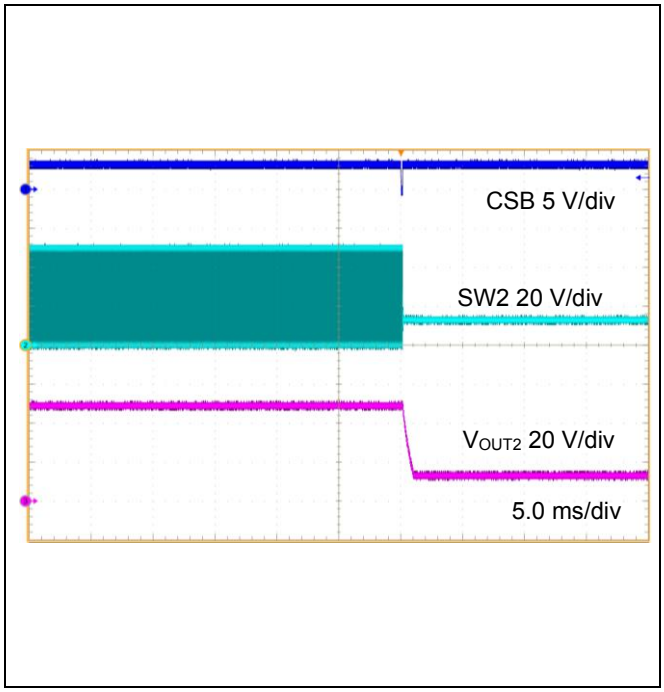


Figure 98. CH2 OFF (Boost Voltage 48 V Output)
V_{OUT2} = 48 V setting (ISET2[9:0] = 655)

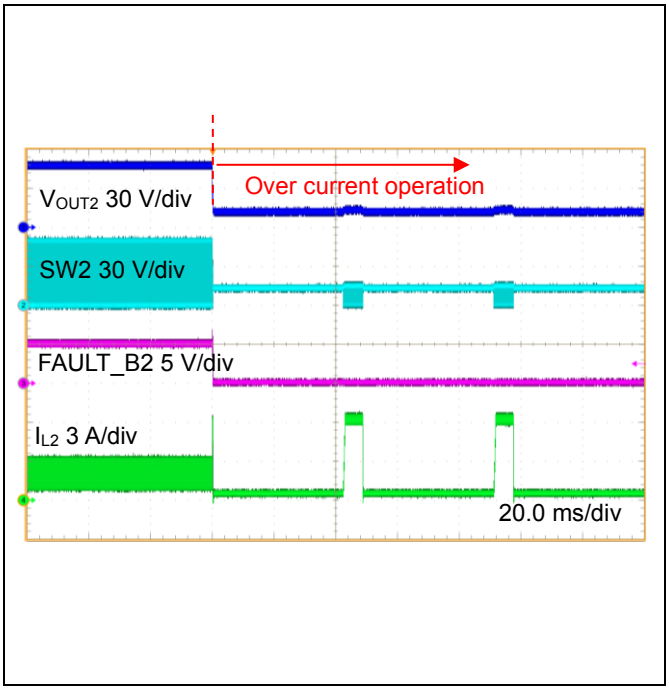


Figure 99. CH2 Over Current Protection Detect
I_{OCP2} = 6.25 A setting (OCPSET2[1:0] = 1)

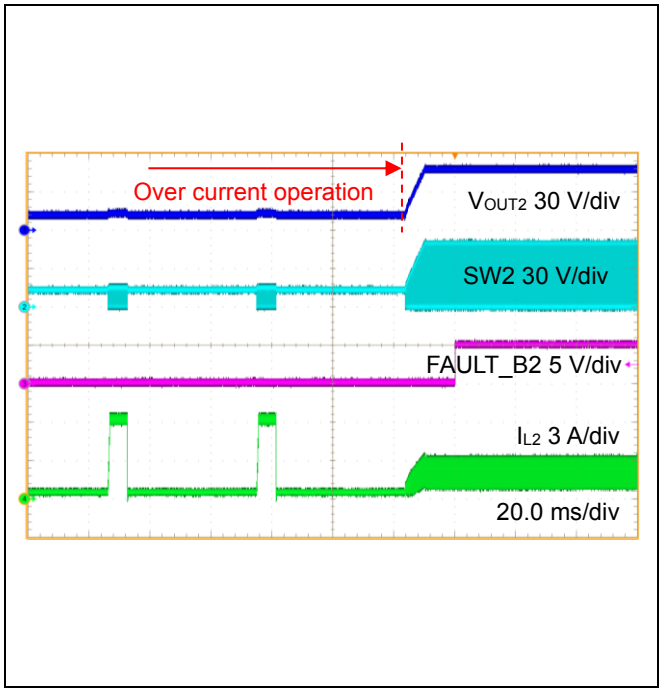


Figure 100. CH2 Over Current Protection Release
I_{OCP2} = 6.25 A setting (OCPSET2[1:0] = 1)

Application Typical Waveforms - continued
(2 STAND-ALONE Operation (CH1: SEPIC CH2: Boost to VIN))

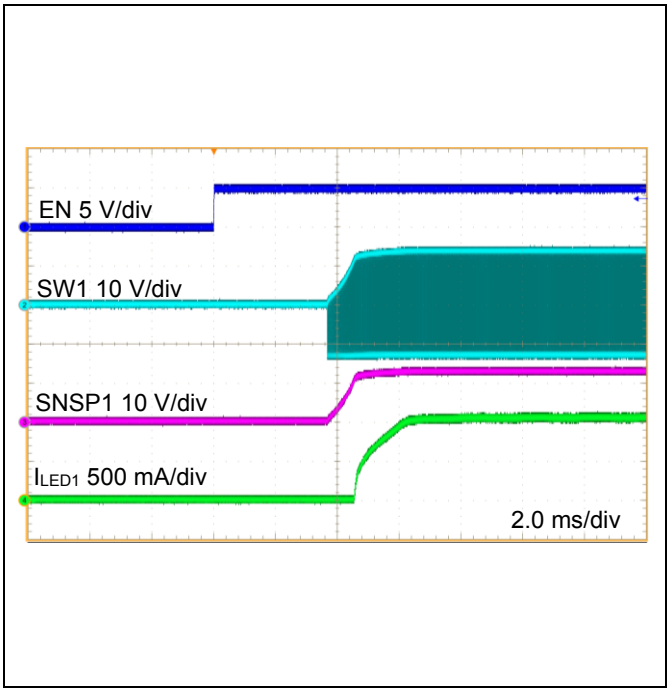


Figure 101. CH1 ON (SEPIC 4 LEDs Drive)
I_{LED1} = 1.06 A setting

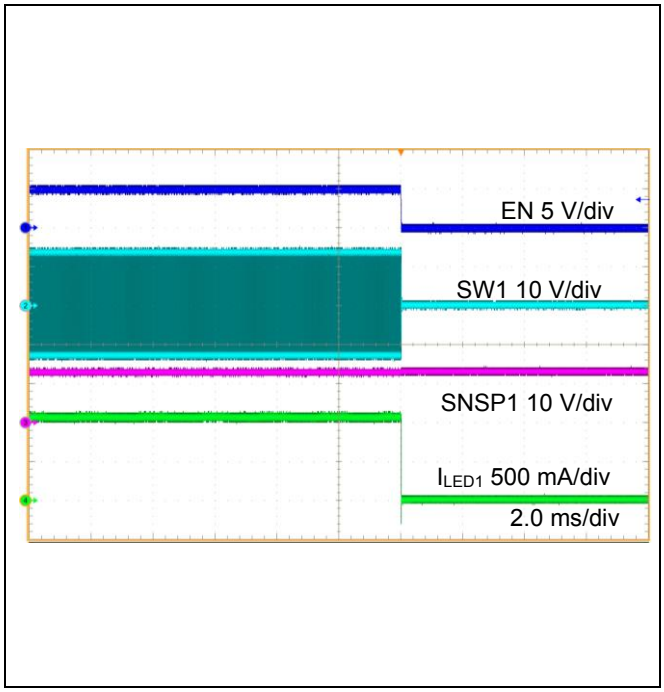


Figure 102. CH1 OFF (SEPIC 4 LEDs Drive)
I_{LED1} = 1.06 A setting

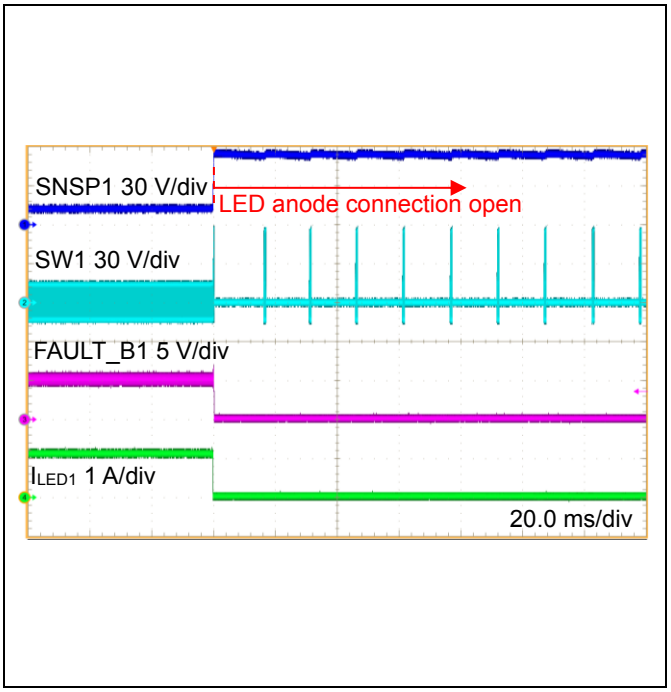


Figure 103. CH1 External Over Voltage Protection Detect
External OVP setting voltage = 55.6 V
LED anode connection open detect

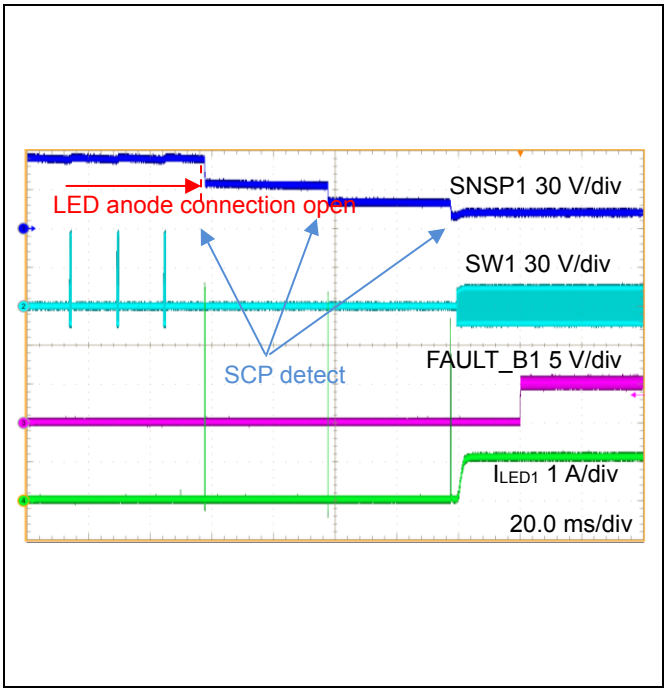


Figure 104. CH1 External Over Voltage Protection Release
External OVP setting voltage = 55.6 V
LED anode connection open release

Application Typical Waveforms - continued
(2 STAND-ALONE Operation (CH1: SEPIC CH2: Boost to VIN))

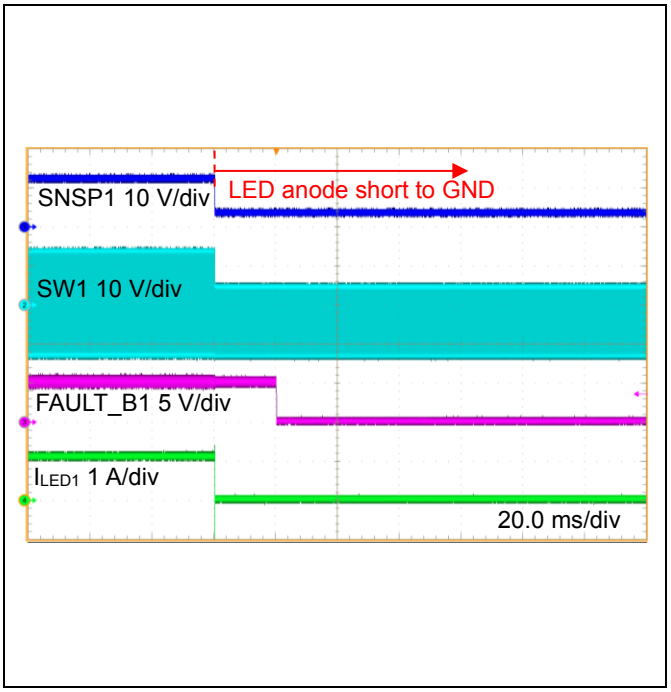


Figure 105. CH1 Under Voltage Detection Detect
LED anode short to GND detect

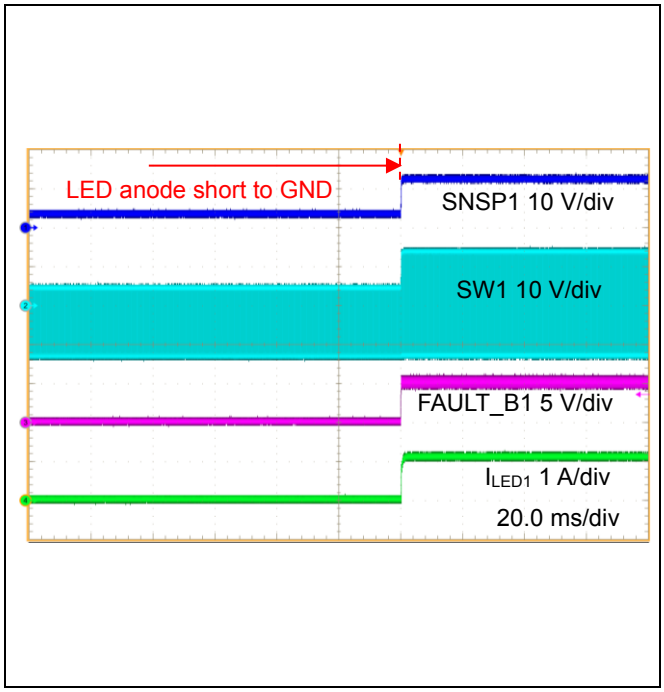


Figure 106. CH1 Under Voltage Detection Release
LED anode short to GND release

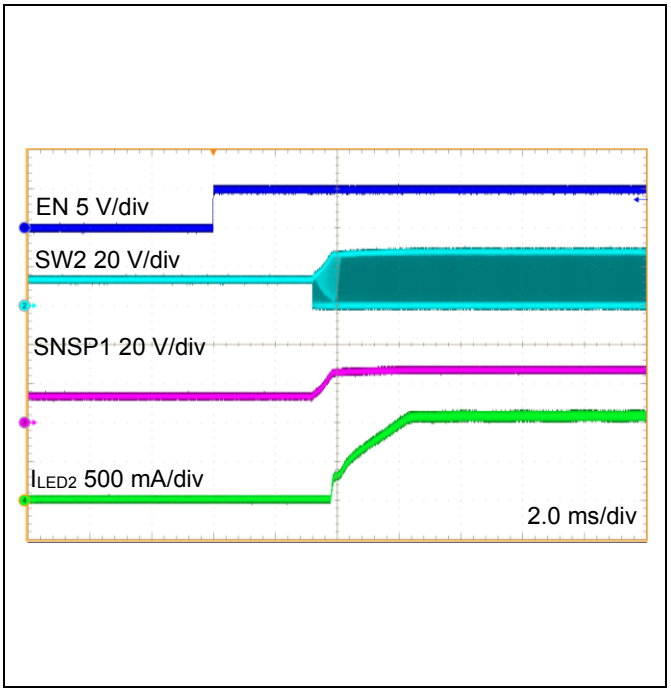


Figure 107. CH2 ON (Boost to VIN 4 LEDs Drive)
I_{LED2} = 1.06 A setting

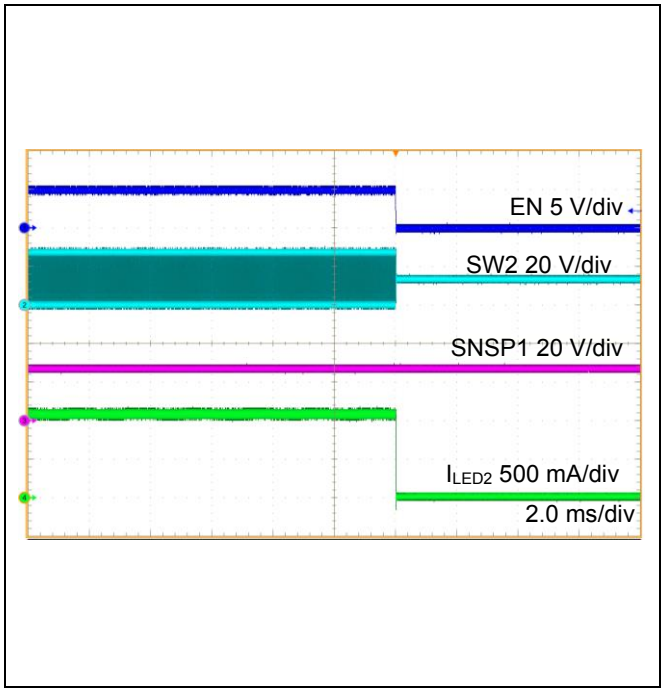


Figure 108. CH2 OFF (Boost to VIN 4 LEDs Drive)
I_{LED2} = 1.06 A setting

Application Typical Waveforms - continued
(2 STAND-ALONE Operation (CH1: SEPIC CH2: Boost to VIN))

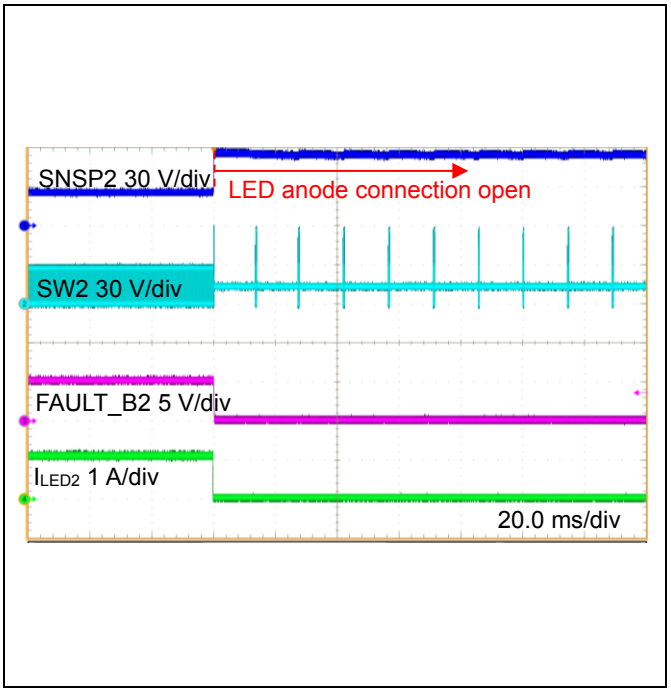


Figure 109. CH2 External Over Voltage Protection Detect
External OVP setting voltage = 55.6 V
LED anode connection open detect

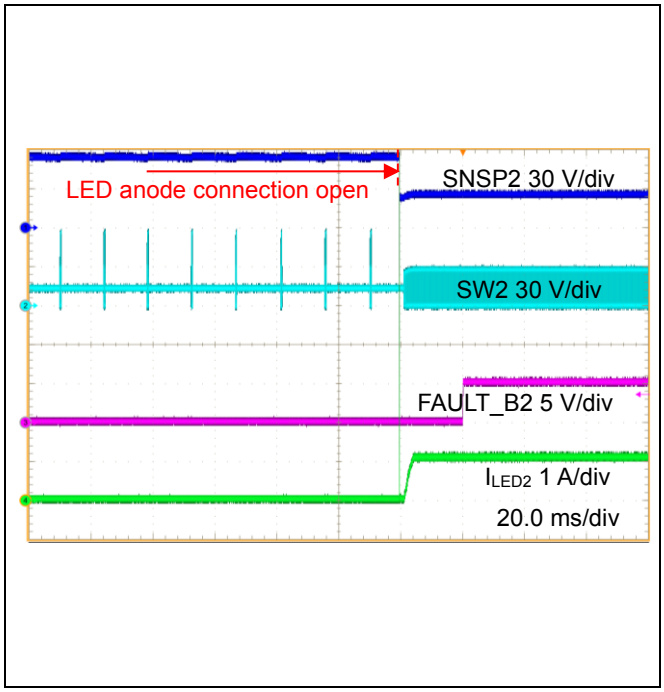


Figure 110. CH2 External Over Voltage Protection Detect
External OVP setting voltage = 55.6 V
LED anode connection open release

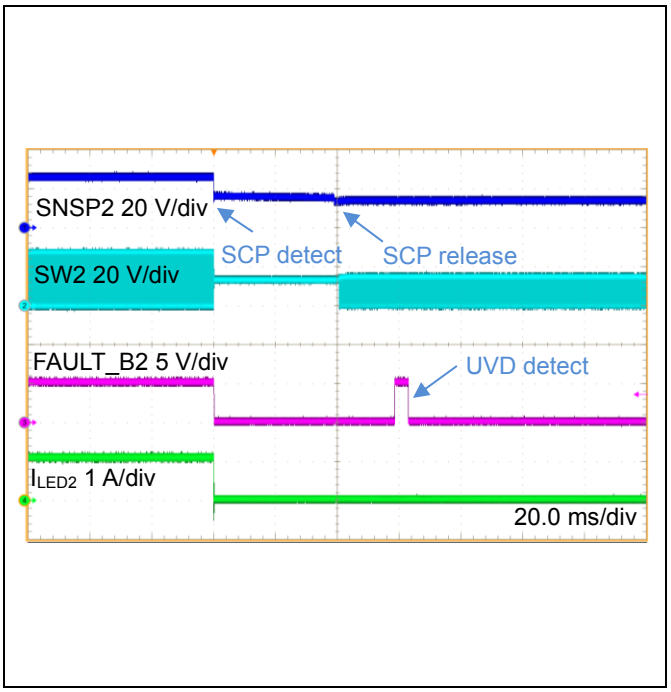


Figure 111. CH2 Under Voltage Detection Detect
LED anode short to VIN detect

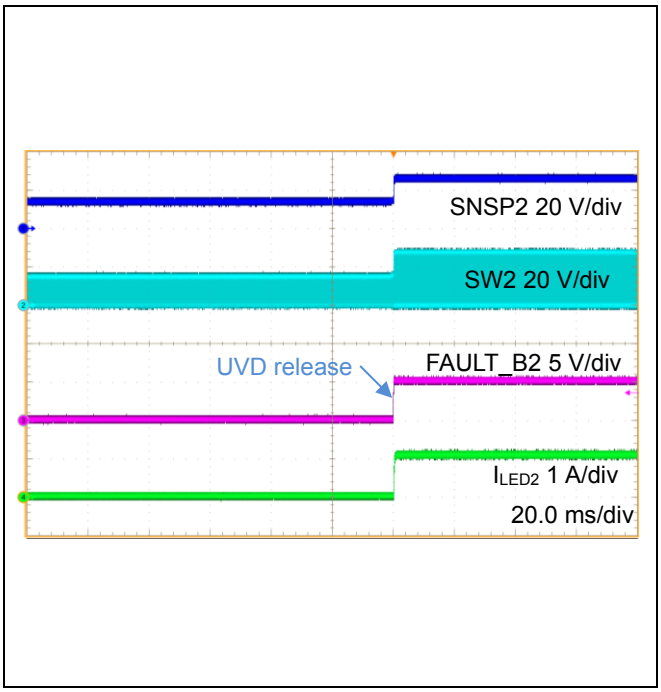


Figure 112. CH2 Under Voltage Detection Release
LED anode short to VIN release

Application Typical Waveforms - continued
(3 SPI Operation (Multi Phase Voltage Output))

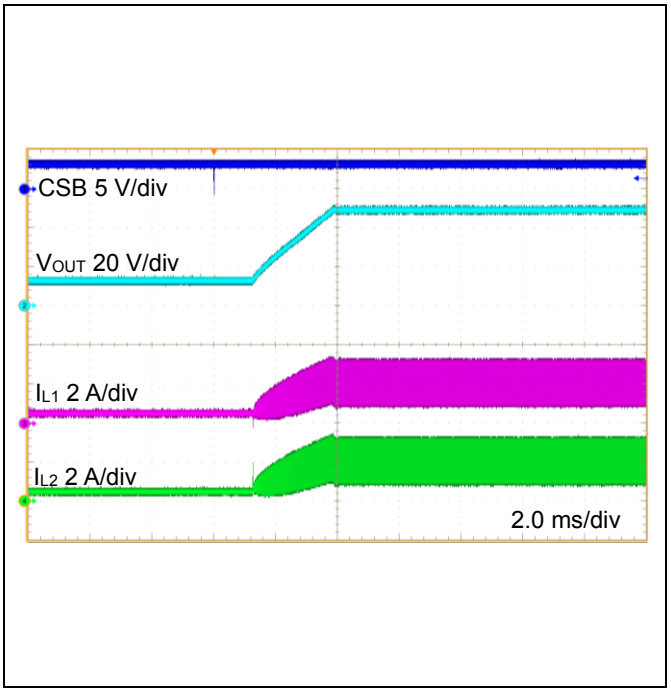


Figure 113. Multiphase Output ON
V_{OUT} = 48 V setting (ISET1[9:0] = 655)

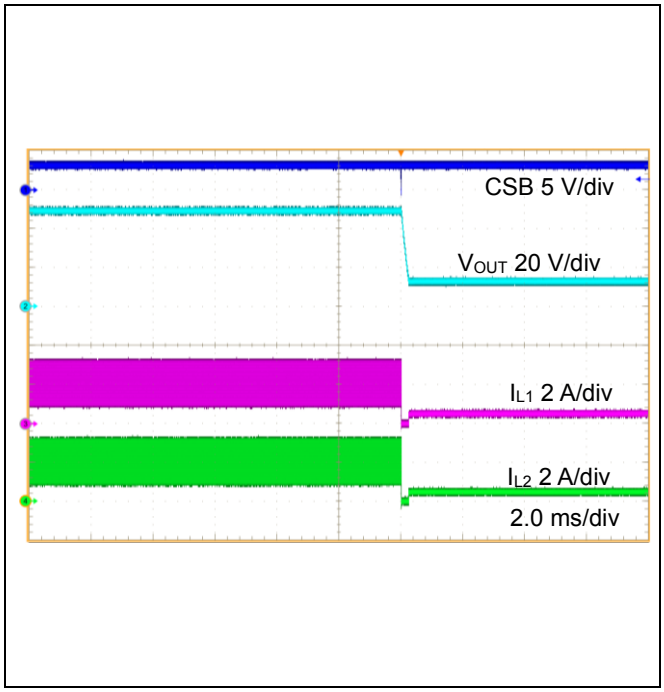


Figure 114. Multiphase Output OFF
V_{OUT} = 48 V setting (ISET1[9:0] = 655)

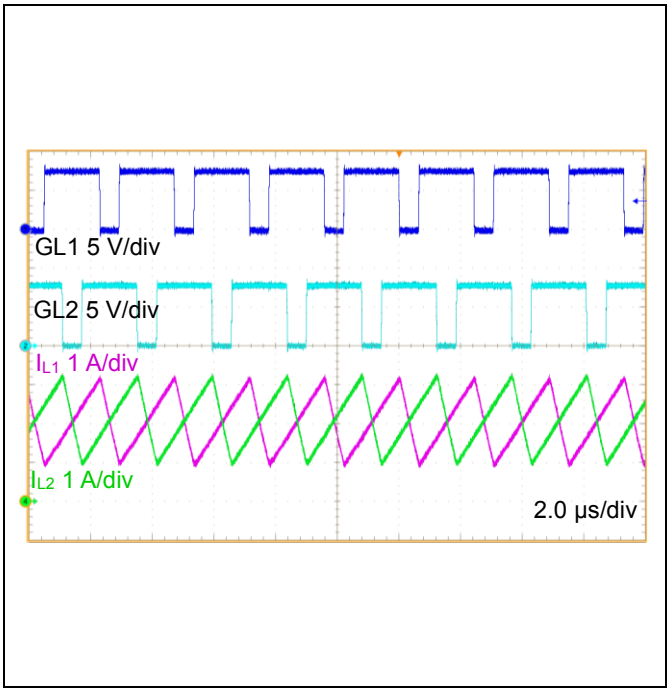


Figure 115. Inductor Ripple Current
V_{OUT} = 48 V setting (ISET1[9:0] = 655)

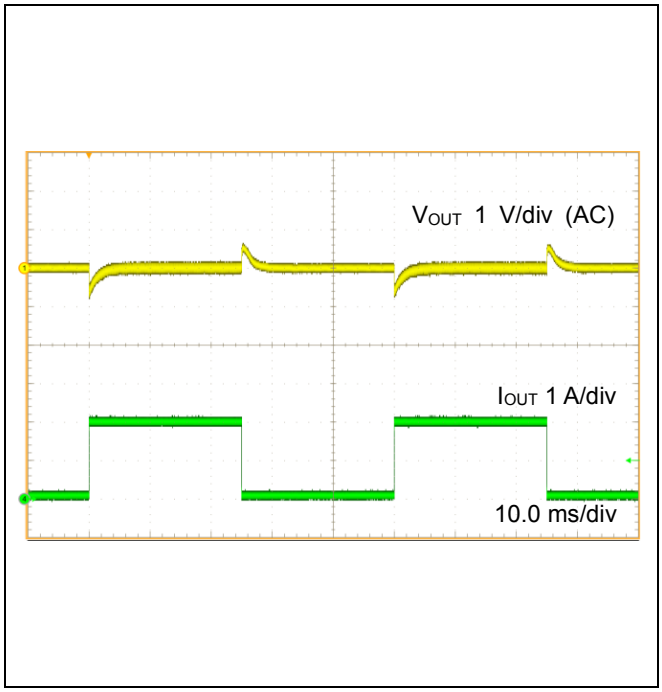


Figure 116. Multiphase Output
I_{OUT} = 0.1 A to 2.0 A transient

Application Typical Waveforms - continued
(4 STAND-ALONE Operation (Multi Phase Voltage Output))

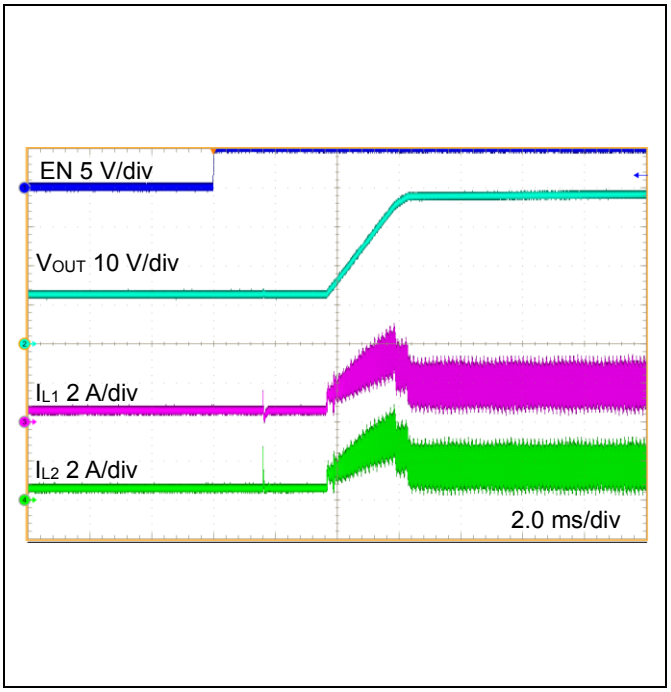


Figure 117. Multiphase Output ON
VOUT = 39.7 V setting

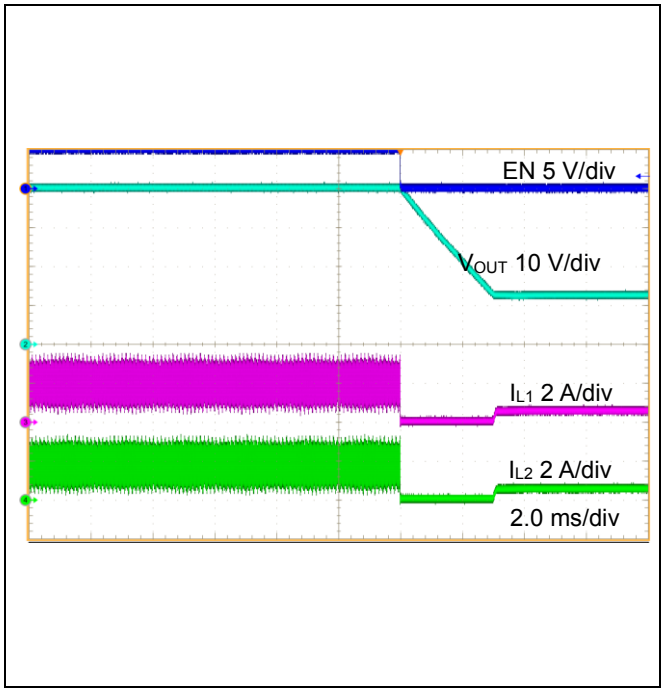


Figure 118. Multiphase Output OFF
VOUT = 39.7 V setting

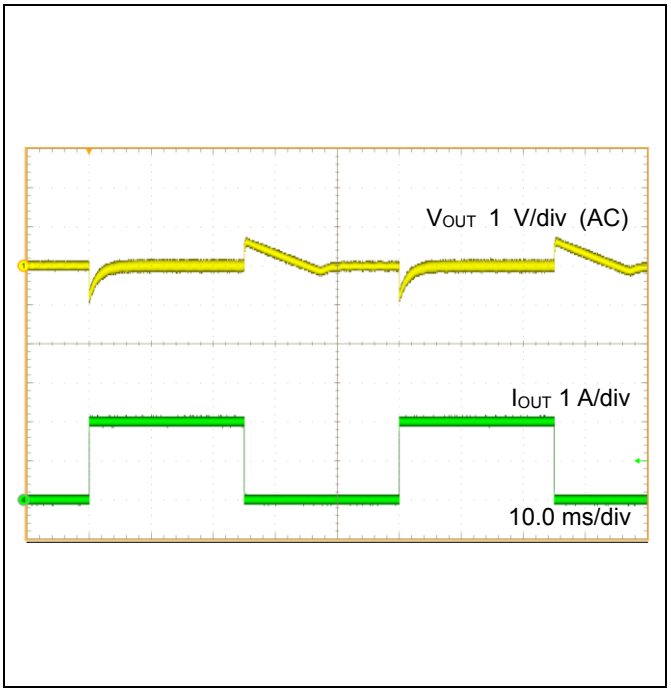


Figure 119. Multiphase Output
IOUT = 0 A to 2 A transient

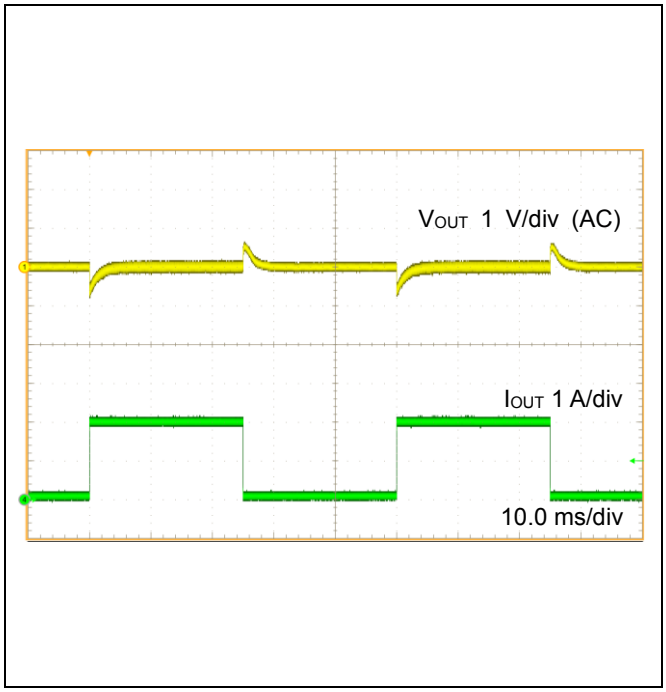


Figure 120. Multiphase Output
IOUT = 0.1 A to 2.0 A transient

Application Typical Waveforms - continued
(5 EEPROM Operation (CH1: Boost with PWM Dimming, CH2: Boost with Rush Current Limit Function))

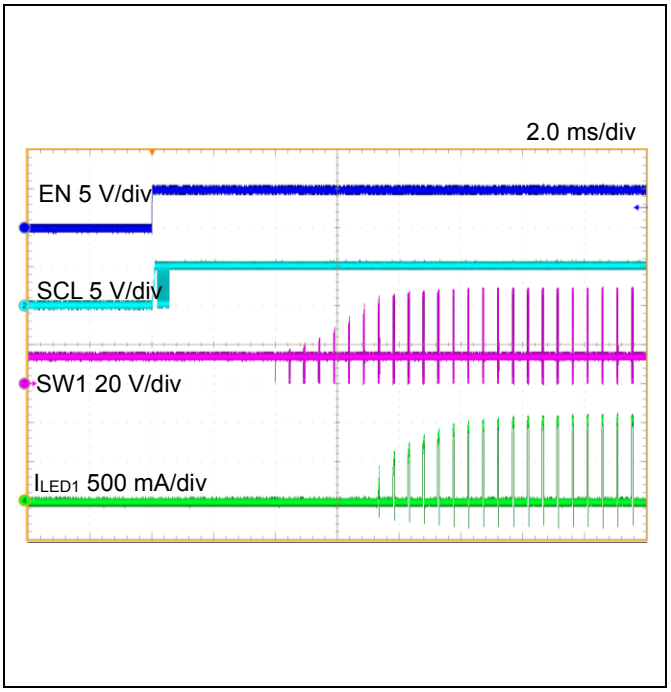


Figure 121. CH1 ON (Boost 16 LEDs Drive)
I_{LED1} = 1.04 A setting
10 % PWM dimming (DPWM1[9:0] = 102)

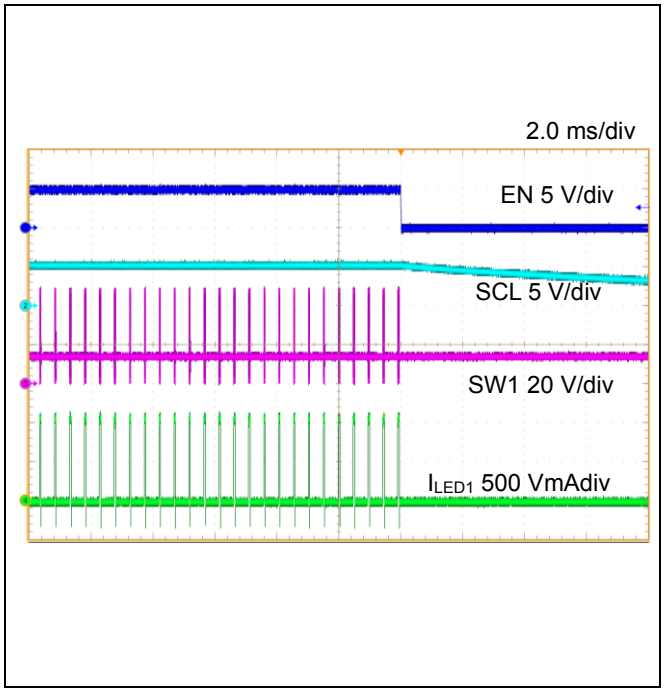


Figure 122. CH1 OFF (Boost 16 LEDs Drive)
I_{LED1} = 1.04 A setting
10 % PWM dimming (DPWM1[9:0] = 102)

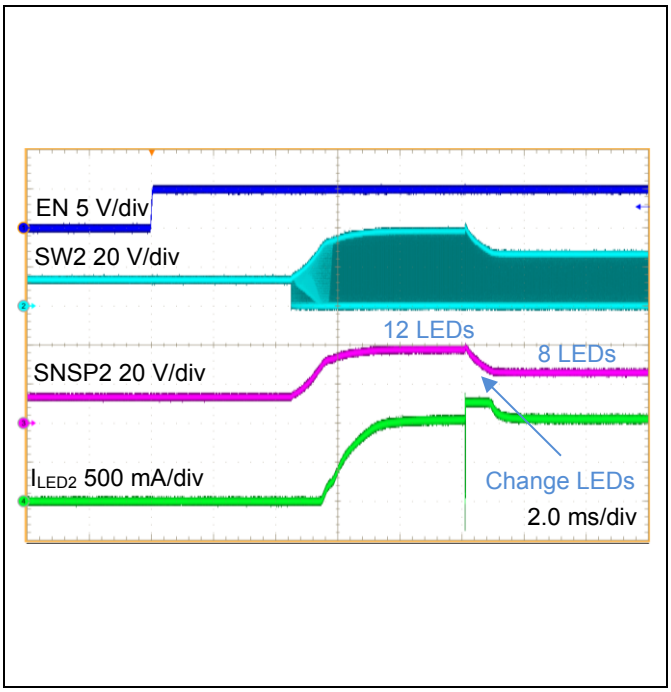


Figure 123. CH2 Rush Current Limit Function
I_{LED2} = 1.04 A setting
Rush Current Limit Function: ON (CURLIMEN2 = 1)
Change LED number 12 LEDs to 8 LEDs

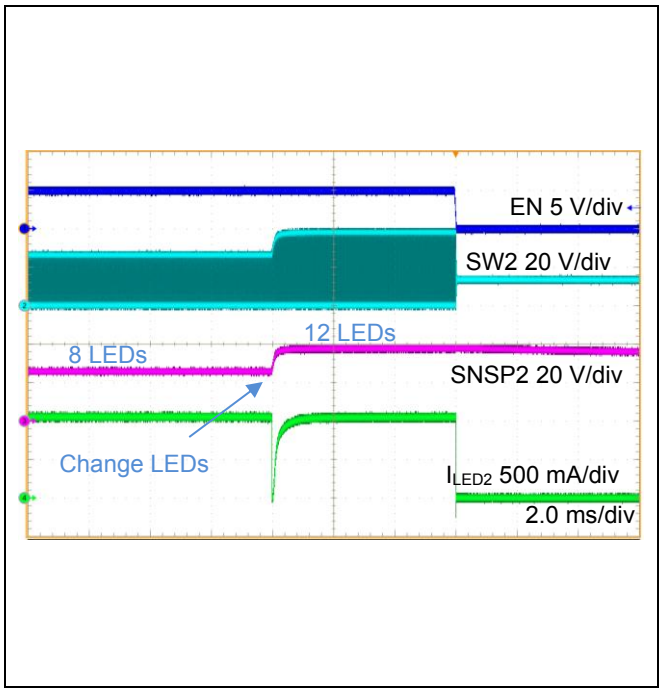


Figure 124. CH2 Rush Current Limit Function
I_{LED2} = 1.04 A setting
Rush Current Limit Function: ON (CURLIMEN2 = 1)
Change LED number 8 LEDs to 12 LEDs

Application Examples

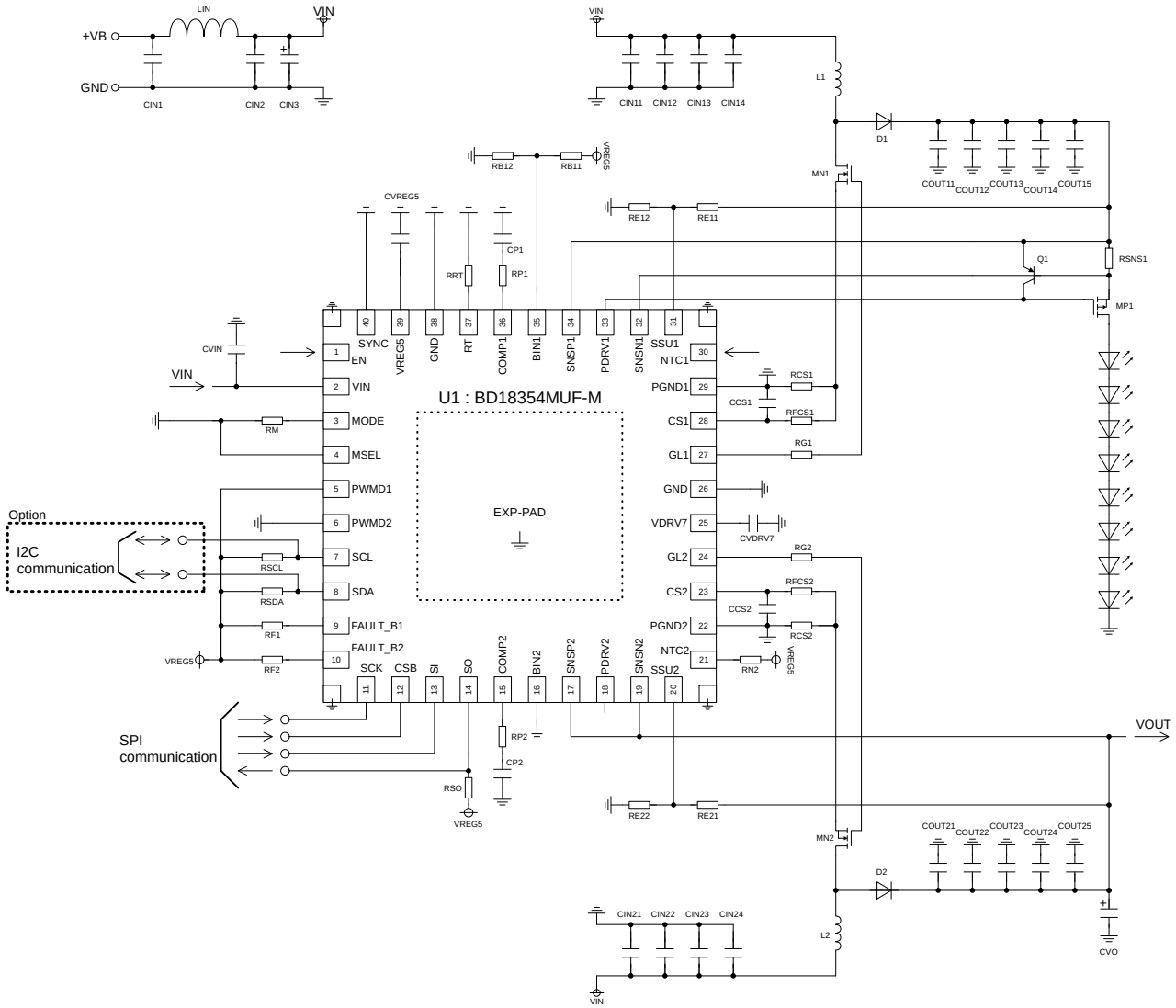
1 SPI Operation (CH1: Boost CH2: Boost Voltage Output)

VIN = 8 V to 18 V
DC/DC Switching Frequency = 399 kHz
I_{OCP} = 6.25 A
External OVP Setting Voltage = 55.6 V
ADMODE = 0

CH1: Current output
LED = 8 series, Vf = 3.0 V (Typ), 3.5 V (Max)
LED Current = 1.04 A (= 166.6 mV / 0.16 Ω), 10 % PWM dimming (DPWM1[9:0] = 102)
When PWMDIM1 = 1 and PWMD1 pin = H, 100 % PWM Dimming operation.
When PWMDIM1 = 1 and PWMD1 pin = L, 10 % PWM Dimming operation.

CH2: Voltage output (VMODE2 = 1)
V_{OUT} = 48 V (ISET2[9:0] = 655)

This is the basic circuit for SPI operation. CH1 is boost LED driver configuration and CH2 is boost voltage output configuration. Registers not mentioned are initial settings (register values can be changed). When a communication error occurs, the STAND-ALONE operation is performed, and the PWMD1 pin = "H" to turn on the LED for CH1, and the PWMD2 pin = "L" to stop the voltage output for CH2. By connecting an EEPROM as an option, the register settings at the time of a communication error can be road from the EEPROM.



1 SPI Operation (CH1: Boost CH2: Boost Voltage Output) - continued

Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18354MUF-M	-	-	ROHM
Resistor	R_{RT}	MCR03	47	kΩ	ROHM
	R_{P1}	MCR03	33	Ω	ROHM
	R_{P2}	MCR03	6.8	kΩ	ROHM
	R_{B11}	MCR03	15	kΩ	ROHM
	R_{B12}	MCR03	20	kΩ	ROHM
	R_{E11}, R_{E21}	MCR03	510	kΩ	ROHM
	R_{E12}, R_{E22}	MCR03	24	kΩ	ROHM
	R_{FCS1}, R_{FCS2}	MCR03	0	Ω	ROHM
	R_{G1}, R_{G2}	MCR03	4.7	Ω	ROHM
	R_{F1}, R_{F2}, R_{SO}, R_{M}, R_{N2}	MCR03	10	kΩ	ROHM
	R_{SDA}, R_{SCL}	MCR03	1	kΩ	ROHM
	R_{SNS1}	LTR18	0.16	Ω	ROHM
	R_{CS1}, R_{CS2}	LTR18	0.024	Ω	ROHM
Capacitor	C_{IN1}, C_{IN2}	GCM32EC71H106KA01	10	μF	murata
	C_{IN3}	UCM1H221MNL1GS	220	μF	Nichicon
	C_{VIN}	GCM21BR71H105KA01	1	μF	murata
	C_{IN11}, C_{IN12}, C_{IN13}, C_{IN21}, C_{IN22}, C_{IN23}	GCM32DC72A475KE02	4.7	μF	murata
	C_{IN14}, C_{IN24}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT11}, C_{OUT21}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT12}, C_{OUT13}, C_{OUT14}, C_{OUT15}, C_{OUT22}, C_{OUT23}, C_{OUT24}, C_{OUT25}	GCM32ER71H475KA55	4.7	μF	murata
	C_{VO}	80FVF100M+P	100	μF	SunCon
	C_{P1}	GCM21BR11E105KA42	1	μF	murata
	C_{P2}	GCM188R71C473KA01	0.047	μF	murata
	C_{VREG5}	GCM21BR71C475KA67	4.7	μF	murata
	C_{VDRV7}	GCM21BR71C475KA67	4.7	μF	murata
	C_{CS1}, C_{CS2}	-	open	-	-
Inductor	L_{IN}	SPM10065VT-2R2M-D	2.2	μH	TDK
	L1	ETQP5M100YFK	10	μH	Panasonic
	L2	SPM10065VT-100M-D	10	μH	TDK
Diode	D1, D2	RB048RSM10STF	-	-	ROHM
MOSFET	MN1, MN2	RD3P06BBKHRB	-	-	ROHM
	MP1	RQ3L120BJFRA	-	-	ROHM
Transistor	Q1	SSTA56HZG	-	-	ROHM

Application Examples - continued

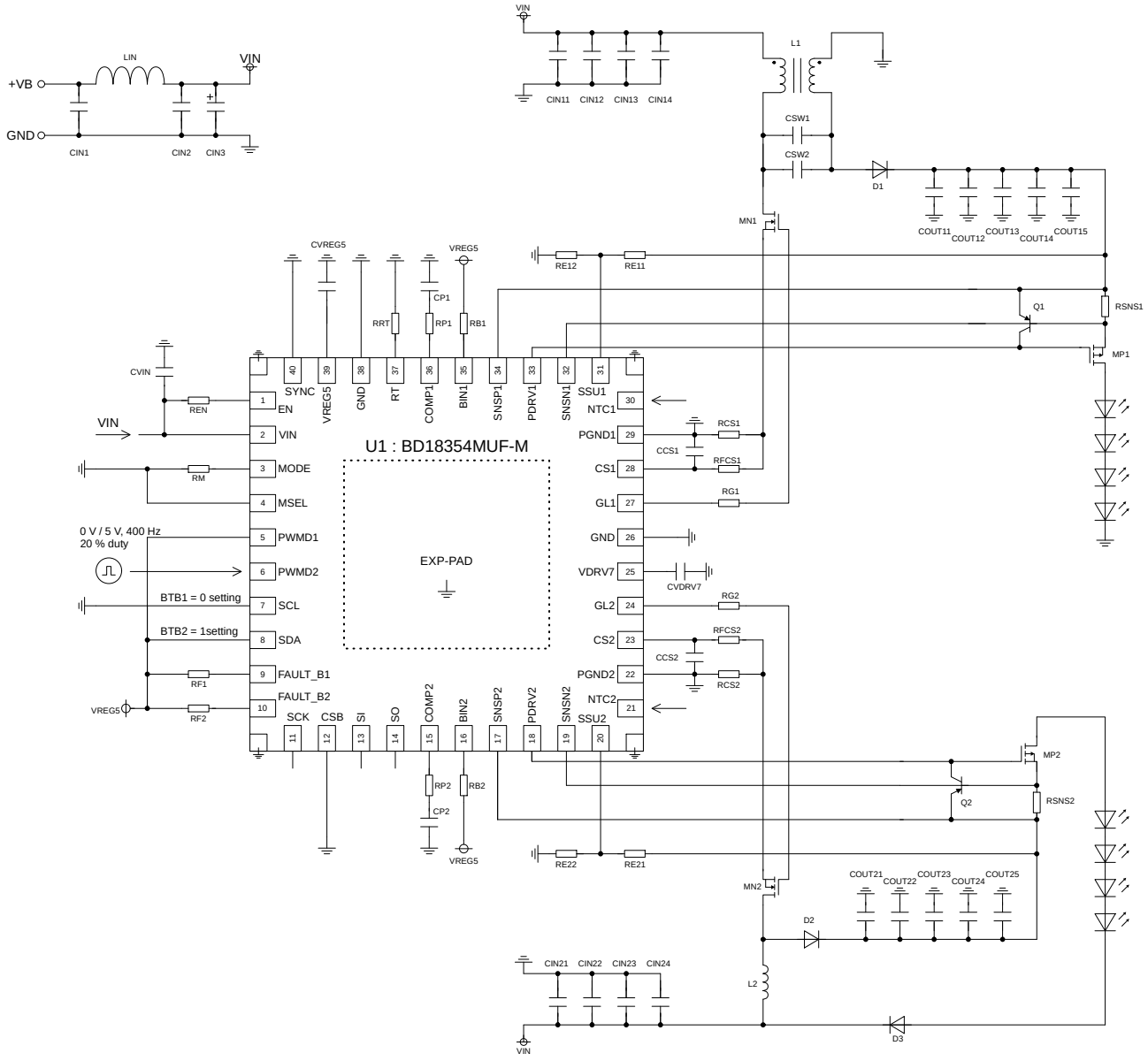
2 STAND-ALONE Operation (CH1: SEPIC CH2: Boost to VIN)

VIN = 8.5 V to 18 V
DC/DC Switching Frequency = 399 kHz
I_{OCP} = 6.25 A
External OVP Setting Voltage = 55.6 V
LED = 4 series, Vf = 3.0 V (Typ), 3.5 V (Max)

CH1: Current output
LED Current = 1.06 A (= 191.1 mV / 0.18 Ω)

CH2: Current output
LED Current = 1.06 A (= 191.1 mV / 0.18 Ω, PWM dimming 20 %)

This is a basic circuit for turning on LEDs under STAND-ALONE control, with CH1 in SEPIC configuration and CH2 in boost to VIN configuration. The registers are initial settings for STAND-ALONE control (The register values cannot be changed).



2 STAND-ALONE Operation (CH1: SEPIC CH2: Boost to VIN) - continued

Recommended Parts List

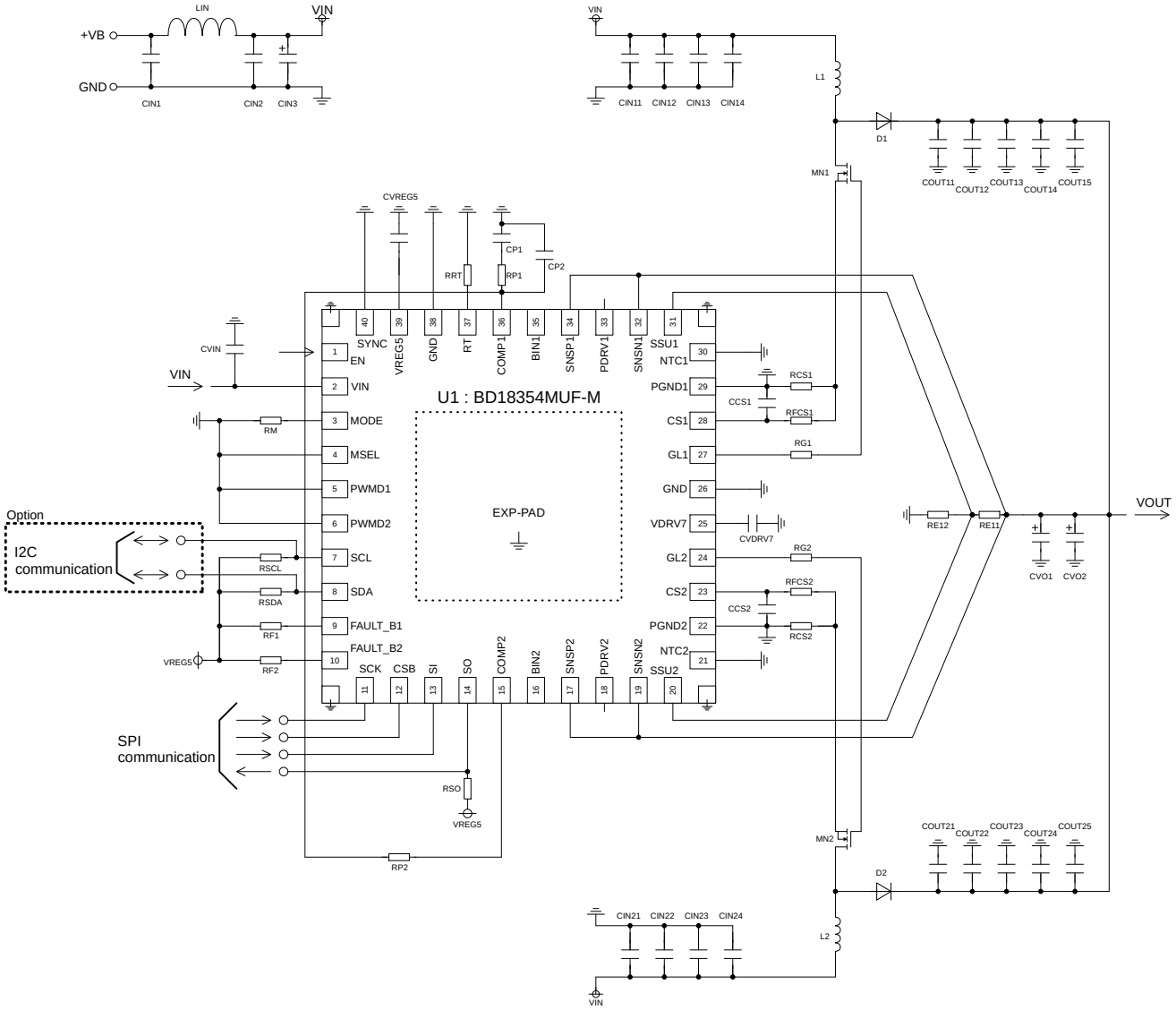
Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18354MUF-M	-	-	ROHM
Resistor	R_{RT}	MCR03	47	kΩ	ROHM
	R_{P1}, R_{P2}	MCR03	33	Ω	ROHM
	R_{B1}, R_{B2}	MCR03	10	kΩ	ROHM
	R_{E11}, R_{E21}	MCR03	510	kΩ	ROHM
	R_{E12}, R_{E22}	MCR03	24	kΩ	ROHM
	R_{FCS1}, R_{FCS2}	MCR03	0	Ω	ROHM
	R_{G1}, R_{G2}	MCR03	4.7	Ω	ROHM
	R_{EN}, R_M, R_{F1}, R_{F2}	MCR03	10	kΩ	ROHM
	R_{SNS1}, R_{SNS2}	LTR18	0.18	Ω	ROHM
	R_{CS1}, R_{CS2}	LTR18	0.024	Ω	ROHM
Capacitor	C_{IN1}, C_{IN2}	GCM32EC71H106KA01	10	µF	murata
	C_{IN3}	UCM1H221MNL1GS	220	µF	Nichicon
	C_{VIN}	GCM21BR71H105KA01	1	µF	murata
	C_{IN11}, C_{IN12}, C_{IN13}, C_{IN21}, C_{IN22}, C_{IN23}	GCM32DC72A475KE02	4.7	µF	murata
	C_{IN14}, C_{IN24}	GCJ188R72A104KA01	0.1	µF	murata
	C_{SW1}, C_{SW2}	GCM32ER71H475KA55	4.7	µF	murata
	C_{OUT11}, C_{OUT21}	GCJ188R72A104KA01	0.1	µF	murata
	C_{OUT12}, C_{OUT13}, C_{OUT14}, C_{OUT15}, C_{OUT22}, C_{OUT23}, C_{OUT24}, C_{OUT25}	GCM32ER71H475KA55	4.7	µF	murata
	C_{P1}, C_{P2}	GCM21BR11E105KA42	1	µF	murata
	C_{VREG5}	GCM21BR71C475KA67	4.7	µF	murata
	C_{VDRV7}	GCM21BR71C475KA67	4.7	µF	murata
	C_{CS1}, C_{CS2}	-	open	-	-
Inductor	L_{IN}	SPM10065VT-2R2M-D	2.2	µH	TDK
	L1	MSD1278T-103MLD	10	µH	Coil Craft
	L2	ETQP5M100YFK	10	µH	Panasonic
Diode	D1, D2	RB048RSM10STF	-	-	ROHM
	D3	RB068LAM100TF	-	-	ROHM
MOSFET	MN1, MN2	RD3P06BBKHRB	-	-	ROHM
	MP1, MP2	RQ3L120BJFRA	-	-	ROHM
Transistor	Q1, Q2	SSTA56HZG	-	-	ROHM

Application Examples - continued

3 SPI Operation (Multi Phase Voltage Output)

VIN = 8 V to 18 V
DC/DC Switching Frequency = 399 kHz
MULTIP = 1, VMODE1 = VMODE2 = 1, SCP1MASK = SCP2MASK = 1, CHON1 = CHON2 = 1
ADMODE = 0
V_{OUT} = 48 V (ISET1[9:0] = 655)
I_{OUT} = 1.0 A, I_{OCP} = 6.25 A
External OVP Setting Voltage = 55.6 V

This is a basic circuit for multiphase voltage output under SPI control. Registers not mentioned are initial settings. (Register values can be changed.)
When MULTIP = 1, COMP1 = COMP2 is shorted inside the IC.
The output voltage setting depends on the CH1 setting, but both CH1 and CH2 should be set the same.
The ISLP setting should be the same. CLIMEN function does not work.
Do not use PWM dimming.
When a communication error occurs, STAND-ALONE operation is performed and voltage output is stopped because the PWMDx pin = "L". By connecting EEPROM as an option, the register settings at the time of communication error can be read from EEPROM.



3 SPI Operation (Multi Phase Voltage Output) - continued

Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18354MUF-M	-	-	ROHM
Resistor	R_{RT}	MCR03	47	kΩ	ROHM
	R_{P1}	MCR03	30	kΩ	ROHM
	R_{P2}	MCR03	0	Ω	ROHM
	R_{E11}	MCR03	510	kΩ	ROHM
	R_{E12}	MCR03	24	kΩ	ROHM
	R_{FCS1}, R_{FCS2}	MCR03	0	Ω	ROHM
	R_{G1}, R_{G2}	MCR03	4.7	Ω	ROHM
	R_M, R_{F1}, R_{F2}, R_{SO}	MCR03	10	kΩ	ROHM
	R_{SDA}, R_{SCL}	MCR03	1	kΩ	ROHM
	R_{CS1}, R_{CS2}	LTR18	0.024	Ω	ROHM
Capacitor	C_{IN1}, C_{IN2}	GCM32EC71H106KA01	10	µF	murata
	C_{IN3}	UCM1H221MNL1GS	220	µF	Nichicon
	C_{VIN}	GCM21BR71H105KA01	1	µF	murata
	C_{IN11}, C_{IN12}, C_{IN13}, C_{IN21}, C_{IN22}, C_{IN23}	GCM32DC72A475KE02	4.7	µF	murata
	C_{IN14}, C_{IN24}	GCJ188R72A104KA01	0.1	µF	murata
	C_{OUT11}, C_{OUT21}	GCJ188R72A104KA01	0.1	µF	murata
	C_{OUT12}, C_{OUT13}, C_{OUT14}, C_{OUT15}, C_{OUT22}, C_{OUT23}, C_{OUT24}, C_{OUT25}	GCM32ER71H475KA55	4.7	µF	murata
	C_{VO1}, C_{VO2}	80FVF100M+P	100	µF	Suncon
	C_{P1}	GCM188R71C473KA01	0.047	µF	murata
	C_{P2}	GCM1882C2A681JA01	680	pF	murata
	C_{VREG5}	GCM21BR71C475KA67	4.7	µF	murata
	C_{VDRV7}	GCM21BR71C475KA67	4.7	µF	murata
	C_{CS1}, C_{CS2}	-	open	-	-
Inductor	L_{IN}	SPM10065VT-2R2M-D	2.2	µH	TDK
	L1	SPM10065VT-100M-D	10	µH	TDK
	L2	SPM10065VT-100M-D	10	µH	TDK
Diode	D1, D2	RB048RSM10STF	-	-	ROHM
MOSFET	MN1, MN2	RD3P06BBKHRB	-	-	ROHM

Application Examples - continued

4 STAND-ALONE Operation (Multi Phase Voltage Output)

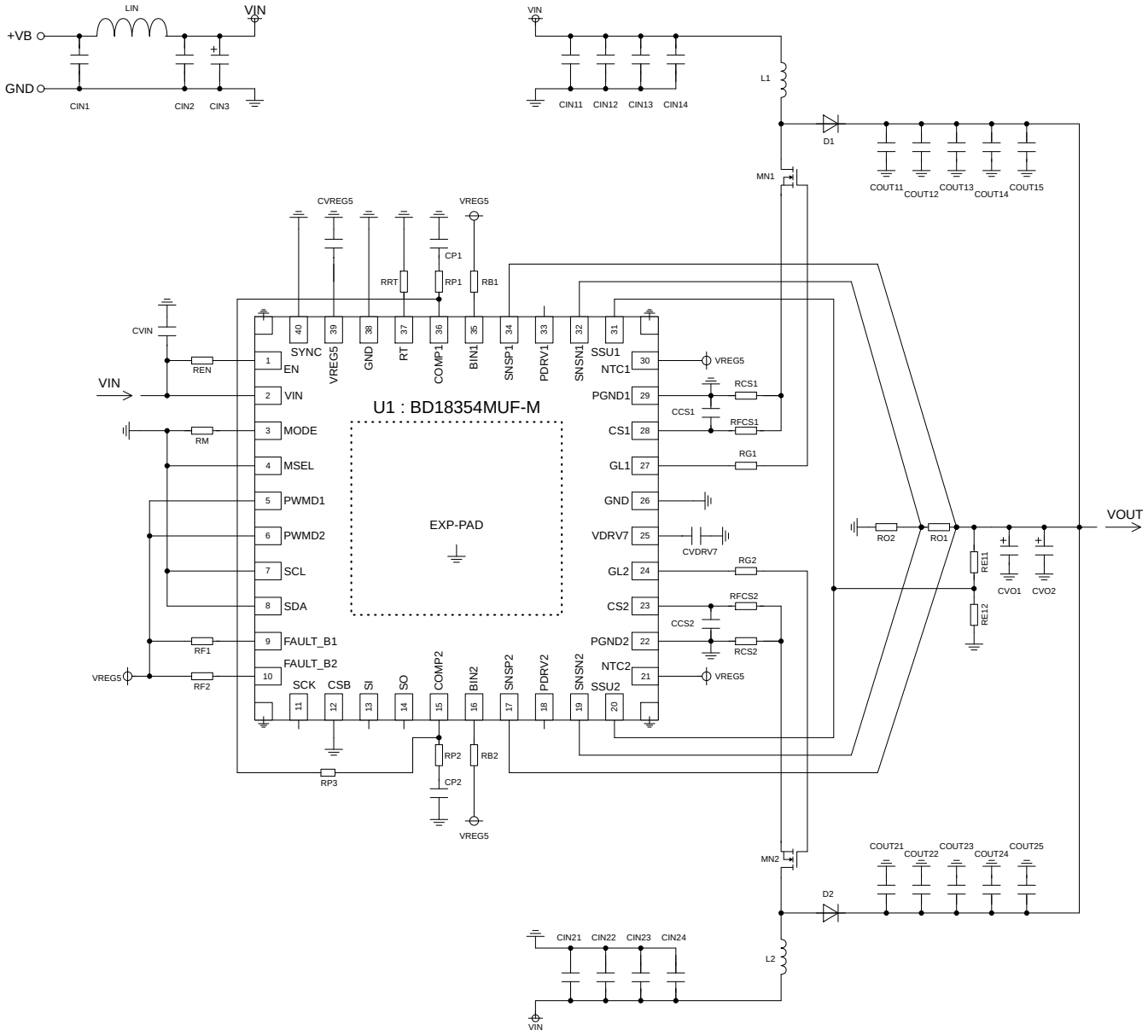
VIN = 8.5 V to 18 V
DC/DC Switching Frequency = 399 kHz
V_{OUT} = 39.7 V, I_{OUT} = 1.0 A, I_{OCP} = 6.25 A
External OVP Setting Voltage = 55.6 V

This is a basic circuit for multiphase boost voltage output with STAND-ALONE control. The registers are initial settings. (Register values cannot be changed.)
In this application, the power components generate more heat when the input voltage is low.
Final thermal design decisions should be made after careful consideration and evaluation at worst case by the customer.
The spread spectrum function operates at a frequency of ±5 % (Typ) of the set frequency f_{SW} in a STAND-ALONE setting.
Refer to the following for the VOUT calculation formula under CV mode and STAND-ALONE conditions.

$$V_{OUT} = \left(\frac{V_{SNS100\%}}{R_{O1}} - I_{SNSN\_HSS} \times 2\right) \times R_{O2} + V_{SNS99.8\%}$$

$$V_{SNS99.8\%} = 0.1911 \text{ [V]}$$

$$I_{SNSN\_HSS} = 1.1 \times V_{SNSN} + 14 \text{ [µA]}$$



4 STAND-ALONE Operation (Multi Phase Voltage Output) - continued

Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18354MUF-M	-	-	ROHM
Resistor	R_{RT}	MCR03	47	kΩ	ROHM
	R_{P1}, R_{P2}	MCR03	6.8	kΩ	ROHM
	R_{P3}	MCR03	0	Ω	ROHM
	R_{E11}	MCR03	510	kΩ	ROHM
	R_{E12}	MCR03	24	kΩ	ROHM
	R_{O1}	MCR03	100	Ω	ROHM
	R_{O2}	MCR03	22	kΩ	ROHM
	R_{FCS1}, R_{FCS2}	MCR03	0	Ω	ROHM
	R_{G1}, R_{G2}	MCR03	4.7	Ω	ROHM
	R_{EN}, R_M, R_{B1}, R_{B2}, R_{F1}, R_{F2}	MCR03	10	kΩ	ROHM
	R_{CS1}, R_{CS2}	LTR18	0.024	Ω	ROHM
Capacitor	C_{IN1}, C_{IN2}	GCM32EC71H106KA01	10	μF	murata
	C_{IN3}	UCM1H221MNL1GS	220	μF	Nichicon
	C_{VIN}	GCM21BR71H105KA01	1	μF	murata
	C_{IN11}, C_{IN12}, C_{IN13}, C_{IN21}, C_{IN22}, C_{IN23}	GCM32DC72A475KE02	4.7	μF	murata
	C_{IN14}, C_{IN24}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT11}, C_{OUT21}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT12}, C_{OUT13}, C_{OUT14}, C_{OUT15}, C_{OUT22}, C_{OUT23}, C_{OUT24}, C_{OUT25}	GCM32ER71H475KA55	4.7	μF	murata
	C_{VO1}, C_{VO2}	80FVF100M+P	100	μF	Suncon
	C_{P1}, C_{P2}	GCM188R71C473KA01	0.047	μF	murata
	C_{VREG5}	GCM21BR71C475KA67	4.7	μF	murata
	C_{VDRV7}	GCM21BR71C475KA67	4.7	μF	murata
	C_{CS1}, C_{CS2}	-	open	-	-
Inductor	L_{IN}	SPM10065VT-2R2M-D	2.2	μH	TDK
	L1	SPM10065VT-100M-D	10	μH	TDK
	L2	SPM10065VT-100M-D	10	μH	TDK
Diode	D1, D2	RB048RSM10STF	-	-	ROHM
MOSFET	MN1, MN2	RD3P06BBKHRB	-	-	ROHM

Application Examples - continued

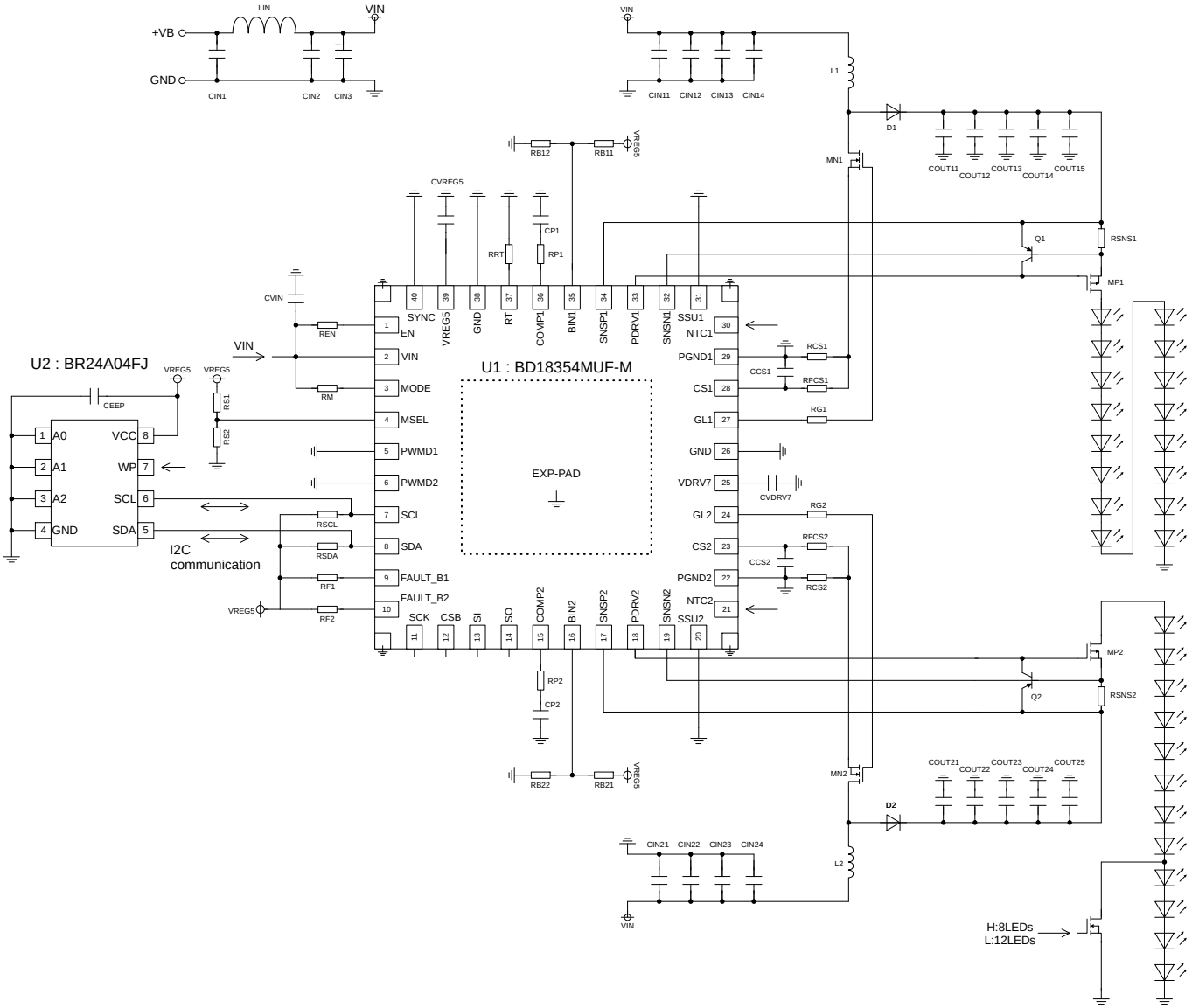
5 EEPROM Operation (CH1: Boost with PWM Dimming, CH2: Boost with Rush Current Limit Function)

VIN = 8 V to 18 V
DC/DC Switching Frequency = 399 kHz
I_{OCP} = 6.25 A
ADMODE = 0
Data load from EEPROM (Data set 2)

CH1: Boost Current Output
LED = 16 series, Vf = 3.0 V (Typ), 3.5 V (Max)
LED Current = 1.04 A (= 166.6 mV / 0.16 Ω), 10 % PWM dimming (DPWM1[9:0] = 102)
OVP detection voltage = 67.50 V (EOVP1/SSU1 = 1, OVPSET1[3:0] = 15)

CH2: Boost Current Output (Rush Current Limit Function: ON)
LED = 12/8 series, Vf = 3.0 V (Typ), 3.5 V (Max)
LED Current = 1.04 A (= 166.6 mV / 0.16 Ω), Rush Current Limit Function: ON (CURLIMEN2 = 1)
OVP detection voltage = 50.06 V (EOVP2/SSU2 = 1, OVPSET2[3:0] = 7)

This is a basic circuit to turn on LEDs with EEPROM operation; CH1 is boost configuration and CH2 is boost to VIN configuration. Registers not mentioned are initial settings. (Depends on the EEPROM data to be loaded)
Starts up by reading register settings from the address selected by the MSEL pin voltage. Lights off when a communication error occurs (because PWMD1 = PWMD2 = L). 8 different lighting conditions can be supported on the same board design by changing the MSEL pin voltage (limited to within the register setting range).



5 EEPROM Operation (CH1: Boost with PWM Dimming, CH2: Boost with Rush Current Limit Function) - continued

Recommended Parts List

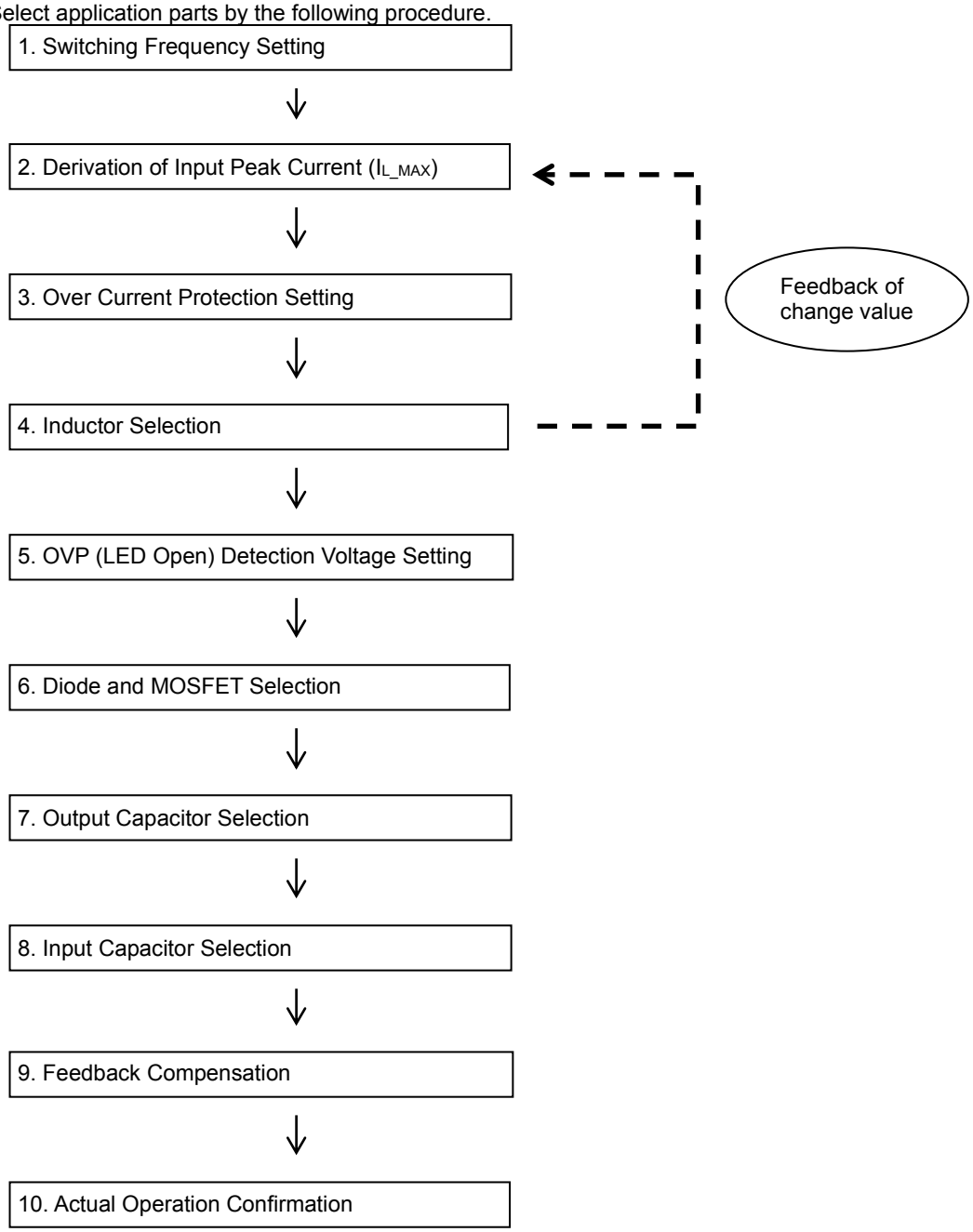
Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18354MUF-M	-	-	ROHM
	U2	BR24A04FJ	-	-	ROHM
Resistor	R_{RT}	MCR03	47	kΩ	ROHM
	R_{P1}, R_{P2}	MCR03	33	Ω	ROHM
	R_{B11}, R_{B21}	MCR03	15	kΩ	ROHM
	R_{B12}, R_{B22}	MCR03	20	kΩ	ROHM
	R_{FCS1}, R_{FCS2}	MCR03	0	Ω	ROHM
	R_{G1}, R_{G2}	MCR03	4.7	Ω	ROHM
	R_{EN}, R_M, R_{F1}, R_{F2}	MCR03	10	kΩ	ROHM
	R_{SDA}, R_{SCL}	MCR03	1	kΩ	ROHM
	R_{S1}	MCR03	47	kΩ	ROHM
	R_{S2}	MCR03	20	kΩ	ROHM
	R_{SNS1}, R_{SNS2}	LTR18	0.16	Ω	ROHM
	R_{CS1}, R_{CS2}	LTR18	0.024	Ω	ROHM
Capacitor	C_{IN1}, C_{IN2}	GCM32EC71H106KA01	10	μF	murata
	C_{IN3}	UCM1H221MNL1GS	220	μF	Nichicon
	C_{VIN}	GCM21BR71H105KA01	1	μF	murata
	C_{IN11}, C_{IN12}, C_{IN13}, C_{IN21}, C_{IN22}, C_{IN23}	GCM32DC72A475KE02	4.7	μF	murata
	C_{IN14}, C_{IN24}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT11}, C_{OUT21}	GCJ188R72A104KA01	0.1	μF	murata
	C_{OUT12}, C_{OUT13}, C_{OUT14}, C_{OUT15}, C_{OUT22}, C_{OUT23}, C_{OUT24}, C_{OUT25}	GCM32ER71H475KA55	4.7	μF	murata
	C_{P1}, C_{P2}	GCM21BR11E105KA42	1	μF	murata
	C_{VREG5}	GCM21BR71C475KA67	4.7	μF	murata
	C_{VDRV7}	GCM21BR71C475KA67	4.7	μF	murata
	C_{CS1}, C_{CS2}	-	open	-	-
	C_{EEP}	GCJ188R71C104KA01	0.1	μF	murata
Inductor	L_{IN}	SPM10065VT-2R2M-D	2.2	μH	TDK
	L1, L2	ETQP5M100YFK	10	μH	Panasonic
Diode	D1, D2	RB048RSM10STF	-	-	ROHM
MOSFET	MN1, MN2	RD3P06BBKHRB	-	-	ROHM
	MP1, MP2	RQ3L120BJFRA	-	-	ROHM
Transistor	Q1, Q2	SSTA56HZG	-	-	ROHM

Application Parts Selection Method (Boost Mode LED Driver Application)

Refer to Application Examples 1 SPI Operation (CH1: Boost Output).

A constant setting sheet is available. Contact ROHM directly.

Select application parts by the following procedure.



Application Parts Selection Method (Boost Mode LED Driver Application) - continued

1 Switching Frequency Setting

The switching frequency of the DC/DC can be set by the resistor R_{RT} connected to the RT pin and the register FRT[3:0].
Design value: Switching Frequency = 399 kHz (FRT[3:0] = 5)

$$f_{SW} \approx \frac{(FRT[3:0]+1)\times k}{R_{RT}} = \frac{(5+1)\times k}{47\ k\Omega} \approx 399 \qquad \text{[kHz]}$$

$$k = 3125 \times 10^6$$

2 Derivation of Input Peak Current I_{L_MAX} (ISETx[9:0] = 901)

2.1 Calculation of Output Voltage (V_{OUT})

BOOST Setting:

$$V_{OUT} = V_{f\_LED} \times N + V_{SNSxAVE87\%H} + R_{ON\_PWMFET} \times I_{LED}$$

$$= 3.0 \times 8 + 0.1666 + 0.2 \times 1 \approx 24.4 \qquad \text{[V]}$$

Where:

V_{f_LED}	is the Vf of LED (Typ: 3.0 V, Max: 3.5 V).
N	is the number of series LED.
R_{ON_PWMFET}	is the ON resistance of MOSFET for PWM dimming (MP1).
I_{LED}	is the output LED current.

2.2 Calculation of DC/DC Switching Duty (D_{SW})

$$D_{SW} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \frac{24\ V - 13\ V}{24\ V} \approx 0.458$$

2.3 Calculation of Output Current (I_{LED})

$$I_{LED} = \frac{V_{SNSxAVE87\%H}}{R_{SNS}} = \frac{0.1666}{0.16} \approx 1.04 \qquad \text{[A]}$$

2.4 Calculation of Input Peak Current (I_{L_MAX})

$$I_{L\_MAX} = I_{L\_AVE\_MAX} + \frac{1}{2}\Delta I_{L\_MAX} = 3.90 + 0.84 = 4.74 \qquad \text{[A]}$$

$$I_{L\_MIN} = I_{L\_AVE\_MIN} - \frac{1}{2}\Delta I_{L\_MAX} = 1.48 - 0.84 = 0.64 \qquad \text{[A]}$$

$$I_{L\_AVE\_MAX} = \frac{V_{OUT\_MAX} \times I_{LED}}{\eta \times V_{IN\_MIN}} = \frac{28\ V \times 1\ A}{0.9 \times 8} \approx 3.90 \qquad \text{[A]}$$

$$I_{L\_AVE\_MIN} = \frac{V_{OUT\_MIN} \times I_{LED}}{\eta \times V_{IN\_MAX}} = \frac{24\ V \times 1\ A}{0.9 \times 18} \approx 1.48 \qquad \text{[A]}$$

$$\Delta I_{L\_MAX} = \frac{V_{IN}}{L} \times \frac{(V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{1}{f_{SW\_MIN}}$$

$$= \frac{14\ V}{10\ \mu H} \times \frac{(28\ V - 14\ V)}{28\ V} \times \frac{1}{360\ kHz} \approx 1.68 \qquad \text{[A]}$$

Where:

I_{L_MAX}	is the maximum inductor current.
I_{L_MIN}	is the minimum inductor current.
I_{L_AVE}	is the mean inductor current.
$I_{L\_AVE\_MAX}$	is the maximum mean inductor current.
$I_{L\_AVE\_MIN}$	is the minimum mean inductor current.
ΔI_{L_MAX}	is the maximum inductor ripple current.
η	is the efficiency.
f_{SW_MIN}	is the minimum switching frequency FRT[3:0] = 5.

2.4 Calculation of Input Peak Current (I_{L_MAX}) - continued

- ●Assign minimum input voltage for calculation.
- ●BD18354MUF-M adopts current mode DC/DC converter control. When I_{L_MIN} is positive, it becomes to be in the consecutive modes, and it will be in the discontinuity mode when I_{L_MIN} is negative. Feedback characteristics are easy to become insufficient in the discontinuous mode, and responsiveness turns worse, and a switching waveform pattern becomes irregular, and stability is easy to turn worse. Therefore, it is sufficient validation of feedback characteristics are recommended.
- ●η (efficiency) is calculated as 90 %.

Application Parts Selection Method (Boost Mode LED Driver Application) - continued

3 Over Current Protection Setting

Select R_{CS} (resistance for over current detection) to realize below.
Design value: Over current detection = 6.25 A (OCPSETx[1:0] = 1)

$$I_{OCP\_MIN} = \frac{V_{CSOCP\_MIN}}{R_{CS\_MAX}} > I_{L\_MAX} \qquad [A]$$

$$I_{OCP\_MIN} = \frac{V_{CSOCP\_MIN}}{R_{CS\_MAX}} = \frac{0.132}{0.02424} \approx 5.45 > 4.74 \qquad [A]$$

Where:
I_{OCP_MIN} is the minimum over current detection current.
V_{CSOCP_MIN} is the minimum over current detection voltage (OCPSETx[1:0] = 1 = 150 mV).

Set a sufficient margin in consideration of the variation of the inductor.

4 Inductor Selection

For the purpose of stabilizing current mode DC/DC converter operation, adjustment of L value within the following condition is recommended.

$$L > \frac{(V_{OUT} - V_{IN}) \times R_{CS\_MAX}}{\Delta ISLP_{MIN} \times f_{SW\_MIN} \times 2}$$

$$L > \frac{(28 - 8) \times 24.24\ m\Omega}{200\ mV \times 360\ kHz \times 2} \approx 3.4 \qquad [\mu H]$$

Where:
$\Delta ISLP_{MIN}$ is the minimum slope compensation setting (ISLPx[1:0] = 4 = 235 mV).
f_{SW_MIN} is the minimum switching frequency (FRT[3:0] = 5 = 399 kHz).

Application Parts Selection Method (Boost Mode LED Driver Application) - continued

5 OVP (LED Open) Detection Voltage Setting

The LED open detection voltage setting can be made with OVPSETx[3:0] register or with the resistor value connected to the SSUx pin.
See "Description of Blocks 12.6 Over Voltage Protection (OVP)" for details on the OVPSETx[3:0] register setting. This section describes how to set OVP using external resistors. The LED open detection voltage needs higher voltage setting than overshoot of output voltage at start up to avoid start up failure. Further, output voltage at the time of LED open detection (V_{OUT_EOVP}) is calculable as shown below by setting R_{E11} and R_{E12}.
Design value: External over voltage detection = 55.6 V

$$V_{OUT\_EOVP} = \frac{R_{E11} + R_{E12}}{R_{E12}} \times V_{EOVP}$$

$$= \frac{510\ k\Omega + 24\ k\Omega}{24\ k\Omega} \times 2.5\ V \approx 55.6\ (Typ) \qquad [V]$$

Where:
V_{OUT_EOVP} is the OVP (LED open) detection voltage.

R_{E11}, R_{E12} resistor will be the current discharge path for the output capacitor when PWM = L.
Improperly the resistor value can increase VOUT ripple and cause the LED to flicker. Therefore, it is recommended to select R_{OPUD1} in the range of 500 kΩ to 1000 kΩ.
Sufficient verification for LED flickering is required with actual application as behavior differs by characteristic of output capacitor and LED. (V_{OUT} drop can be prevented by inserting bigger output capacitor or R_{E11} resistance.)

6 Diode and MOSFET Selection

Selection of MOSFET MN1
Select a MOSFET (M1) whose VDS rating is higher than the maximum voltage for OVP (LED open) detection.

$$MN1\ V_{DS} > V_{OUT\_EOVP\_MAX} = \frac{R_{E11} + R_{E12}}{R_{E12}} \times V_{EOVP\_MAX}$$

$$= \frac{510\ k\Omega + 24\ k\Omega}{24\ k\Omega} \times 2.625\ V \approx 58.4\ (Max) \qquad [V]$$

Where:
$MN1\ V_{DS}$ is the maximum rating voltage between drain and source of MN1.
$V_{OUT\_EOVP\_MAX}$ is the maximum external over voltage detection voltage.

The RMS current rating (I_{DS_RMS}) flowing between the drain - source of MN1 can be calculated as follows.

$$I_{DS\_RMS} = 1.3 \times \sqrt{(I_{L\_AVE})\text{^}2 \times D_{SW}}$$

Where:
I_{L_AVE} is the mean inductor current.
D_{SW} is the switching duty.

A loss of MN1 is calculated next. The loss of MN1 has switching loss P_{LOSS1} and MN1 ON resistance loss P_{LOSS2}. Switching loss P_{LOSS1} and MN1 ON resistance loss P_{LOSS2} can be calculated as follows.

$$P_{LOSS1} = \frac{(t_R + t_F)}{2} \times f_{SW} \times (V_{OUT} + V_{D1}) \times I_{L\_AVE}$$

$$P_{LOSS2} = {I_{L\_AVE}}^2 \times R_{ON} \times D_{SW}$$

Where:
t_R is the rise time of MN1 drain-source.
t_F is the fall time of MN1 drain-source.
V_{D1} is the forward voltage of D1.
R_{ON} is the ON resistance of MN1.

6 Diode and MOSFET Selection - continued

Selection of rectifier diode D1

For power consumption reduction, use a schottky barrier diode for rectification diode D1. The withstand voltage rating of the diode shall be higher than the OVP (LED Open) detection voltage. In addition, schottky barrier diode with low leakage current shall be selected if PWM dimming is used. Because the leakage current increases with higher temperature environment, the output capacitor can be discharged in PWM = L which may result that LED current will be unstable. The current limit of D1 can be calculated in the following formula.

$$I_{D1} = I_{L\_AVE} \times (1 - D_{SW})$$

Where:
I_{L_AVE} is the mean inductor current.
D_{SW} is the DC/DC switching duty.

Selection of MOSFET MP1

Consider margin and set the rated voltage rather higher than the actual usage condition for LED current and output voltage.

Selection of transistor Q1 for current clamp

It is recommended to insert Q1 to control the flow of excessive large current at the time of anode ground fault. By inserting Q1, the set current is clamped by the Vf of Q1, so the withstand current of MP1 can be suppressed.
For example, when Vf = 0.5 V, the current is clamped at about 3 times the set current. Select the V_{CE} of Q1 that satisfies the following formula.

$$V_{CE} > V_{OUT\_EOVP\_MAX}$$

Where:
V_{CE} is the withstand voltage between collector and emitter of Q1.

Also, select in consideration of hFE, speed and saturation voltage.

7 Output Capacitor Selection

Output capacitance includes two purposes. The first is to reduce output ripple. The second is to supply current to LED when MOSFET (MN1) is switched on. The output voltage ripple is influenced by both bulk capacitance and ESR. (When a ceramic capacitor is used, most of the ripple caused by bulk capacitance.) Bulk capacitance and the ESR can be calculated in lower formula.

$$C_{OUT} \geq I_{LED} \times \frac{D_{SW\_MAX}}{\Delta V_{COUT} \times f_{SW\_MIN}}$$

$$R_{ESR} < \frac{\Delta V_{ESR}}{I_{L\_MAX}}$$

Where:
ΔV_{COUT} is the influence with the capacitor among output ripple.
ΔV_{ESR} is the ripple which occurs in the ESR of the output capacitor.
f_{SW_MIN} is the minimum switching frequency.

The total output ripple permitted here can be expressed as product of LED current ripple and the equivalent resistance of the LED. This equivalent resistance is defined as "ΔV / ΔI of the LED current", and it is necessary to calculate from I-V properties in the data sheet of the selected LED. When the application condition is the number of the driven LED = 8 pcs (equivalent resistance 0.2 Ω / LED), LED current = 1 A (I_{L_MAX} = 4.74 A), switching duty = 72 % (V_{IN} = 8 V, V_{OUT} = 28 V), switching frequency = 400 kHz, LED current ripple = 5 %. Then the total output ripple can be calculated as follows.

$$V_{OUT\_RIPPLE} = 1\,A \times 5\,\% \times (0.2\,\Omega \times 8) = 80 \quad \text{[mV]}$$

Where:
V_{OUT_RIPPLE} is the V_{OUT} ripple voltage.

If bulk capacitance causes 95 % among total output ripple, the output capacitor is calculated as follows.

$$C_{OUT} \geq 1 \times \frac{0.72}{0.08 \times 0.95} \times \frac{1}{400\,kHz} \approx 23.7 \quad \text{[µF]}$$

$$R_{ESR} < \frac{V_{OUT\_RIPPLE}}{I_{L\_MAX}} = \frac{0.08}{4.74} \approx 16.9 \quad \text{[mΩ]}$$

7 Output Capacitor Selection - continued

However, the capacitance of output capacitor mentioned above is minimum capacitance. Therefore, select parts considering the tolerance of the capacitor and DC bias properties. Furthermore, because small external part connected to output may lead to bigger ripple on output voltage, which may result in LED flickering, sufficient verification of the actual application is required. Increase output capacitors if judged to be required from the verification. In addition, an acoustic noise may be produced by the piezoelectric effect of the ceramic capacitor during PWM dimming. Low ESR electrolytic capacitor used together with a ceramic capacitor may reduce this noise. But capacitance may largely decrease with a change of the voltage with the ceramic capacitor and may not accord with the numerical value calculated from theory.

8 Input Capacitor Selection

In DC/DC converter, since peak current flows between input and output, a capacitor is also required in the input side. Therefore, low ESR capacitors with capacitor of 10 µF or more and ESR component of 100 mΩ or less are recommended as input capacitors. If a capacitor out of the range is selected, an excessive ripple voltage may be superimposed on the input voltage and the LSI may malfunction.

$$C_{IN} \geq \frac{\Delta I_L}{8 \times V_{IN\_RIPPLE} \times f_{SW}}$$

Where:
V_{IN_RIPPLE} is the V_{IN} ripple voltage.

9 Feedback Compensation

- ●Concerning stability condition of application.
  Stability condition for system with negative feedback is as shown below.
  Phase-lag when gain is 1 (0 dB) is no more than 150° (namely, phase margin is 30° or more).
  Further, since DC/DC converter application is sampled by switching frequency, GBW of the entire system is set to be 1 / 10 or less of switching frequency. To wrap up, target characteristics of application are as shown below.
- ●Phase-lag when gain is 1 (0 dB) is 150° or less (namely, phase margin is 30° or more).
- ●GBW at the time (namely, frequency when gain is 0 dB) is 1/10 or less of switching frequency. Therefore, in order to raise responsiveness by limiting GBW, higher switching frequency is required.
- ●Phase margin: 60° or more
- ●GBW: 1/20 or less of switching frequency.

The knack for securing stability feedback compensation is to insert phase-lead f_{Z1} near GBW. GBW is determined by C_{OUT} and phase-lag f_P due to output impedance R_L (= V_{OUT} / I_{LED}).
They are shown in the following formula.

Phase-lead

$$f_{Z1} = \frac{1}{2 \pi \times C_{P1} \times R_{P1}}$$

Phase-lag

$$f_P = \frac{1}{2 \pi \times R_L \times C_{OUT}}$$

$$R_L = \frac{V_{OUT}}{I_{LED}}$$

As described above, secure phase margin. R_L value at maximum load should be inserted. In addition, with boost DC/DC, right half plane zero (RHP zero) is to be considered. This zero has a characteristic of zero as a gain and as the pole with phase. Because it causes an oscillation when this zero effects on a control loop, it is necessary to bring GBW just before RHP zero. RHP zero f_{Z2} can be calculated with an equation below and shows good characteristic by setting GBW to be lower than 1/10 of RHP zero or less.

$$f_{Z2} = \frac{R_L \times (\frac{V_{IN}}{V_{OUT}})^2}{2 \pi \times L}$$

9 Feedback Compensation - continued

Particularly when supply voltage rises and gets close to output voltage, the switching output becomes irregular and ripple of the output voltage increases. Ripple of the LED current may thereby get bigger.

Since this setting is obtained by simplified, not strict, calculation, adjustment by actual equipment may be required in some cases.
Further, since these characteristics will vary depending upon substrate layout, load condition, etc., confirm satisfactorily with actual equipment when planning mass production.

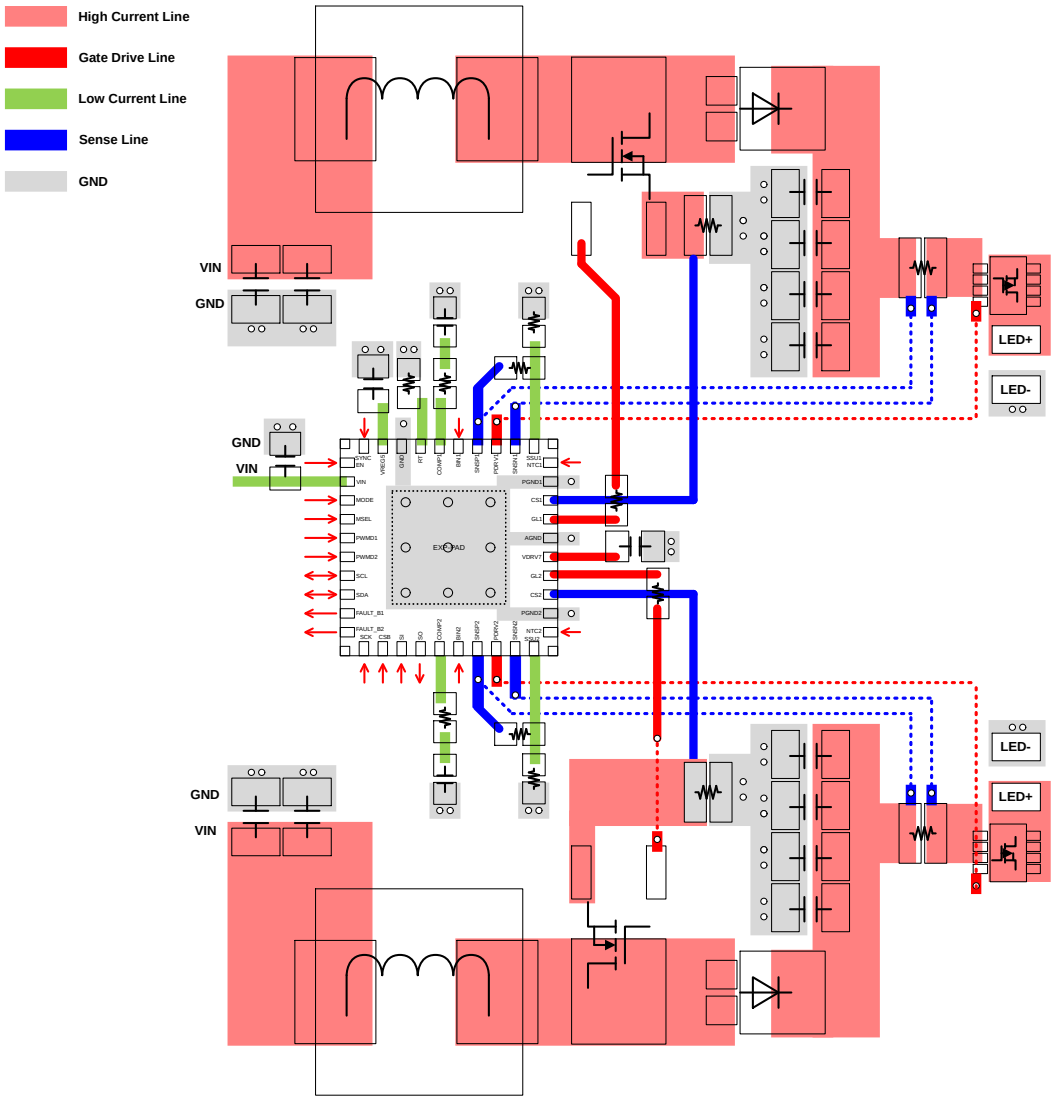
10 Actual Operation Confirmation

Select external parts based on verification with actual equipment since characteristics will vary depending on various factors such as load current, input voltage, output voltage, inductor value, load capacitance, switching frequency and mounting pattern.

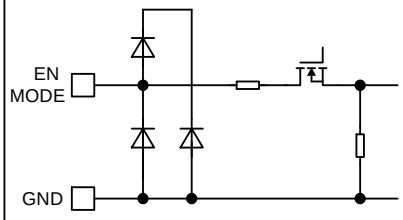
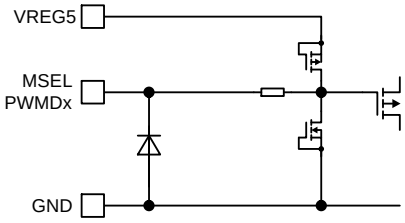
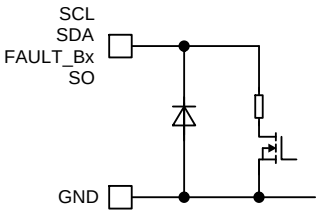
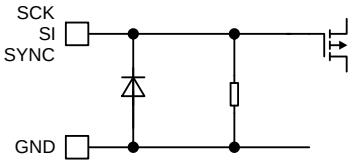
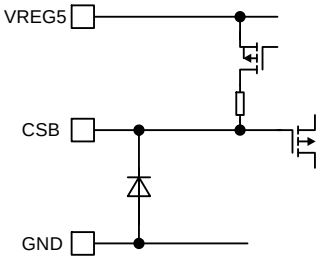
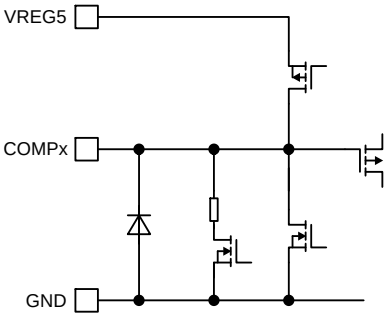
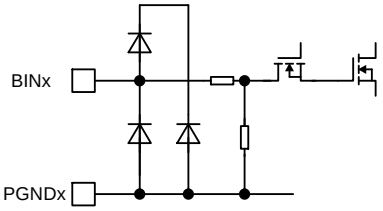
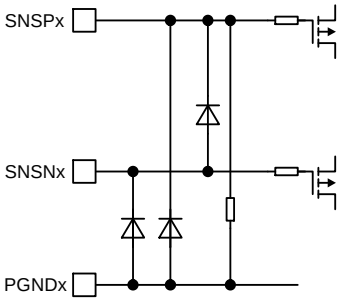
About the attention point at the time of the PCB layout

1. Locate the decoupling capacitor of C_{VIN}, C_{VREG5} and C_{VDRV7} close to the LSI pin as much as possible.
2. R_{RT} locates it close to the RT pin.
3. Because high current may flow in PGNDx, lower impedance.
4. Prevent noise to be applied to the EN, NTCx, COMPx, RT, PWMDx, SSUx, SNSPx and SNSNx pins.
5. As the GLx, CSx and PDRVx pins are switching, be careful not to affect the neighboring patterns.
6. There is EXP-PAD on the back side of the package.
7. For noise reduction, it is recommended that PGNDx of R_{CSx} and PGNDx of C_{OUTx} have common grounds. In addition, consider the PCB layout so that the current path of MNx → R_{CSx}, R_{CSx} → PGNDx and the current path of MNx → Dx → C_{OUT} → PGNDx are the shortest and with the lowest impedance on the same surface without vias etc.

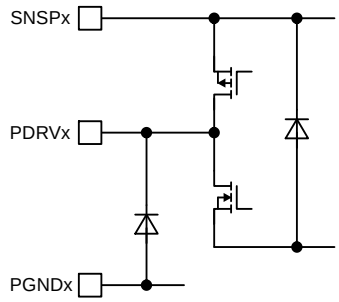
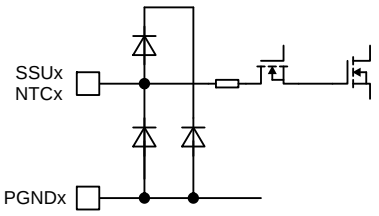
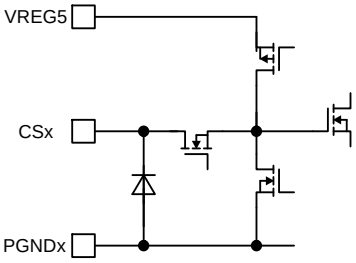
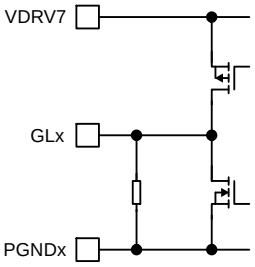
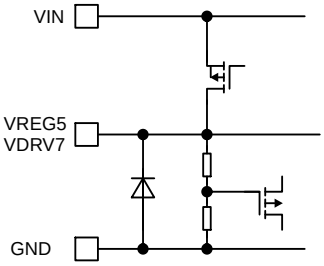
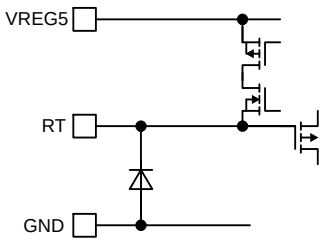
PCB Layout Example



I/O Equivalence Circuits

Pin No.	Pin Name	I/O Equivalence Circuit	Pin No.	Pin Name	I/O Equivalence Circuit
1 3	EN MODE		4 5 6	MSEL PWMD1 PWMD2	
7 8 9 10 14	SCL SDA FAULT_B1 FAULT_B2 SO		11 13 40	SCK SI SYNC	
12	CSB		15 36	COMP2 COMP1	
16 35	BIN2 BIN1		17 19 32 34	SNSP2 SNSN2 SNSN1 SNSP1	

I/O Equivalence Circuits- continued

Pin No.	Pin Name	I/O Equivalence Circuit	Pin No.	Pin Name	I/O Equivalence Circuit
18 33	PDRV2 PDRV1		20 21 30 31	SSU2 NTC2 NTC1 SSU1	
23 28	CS2 CS1		24 27	GL2 GL1	
25 39	VDRV7 VREG5		37	RT	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

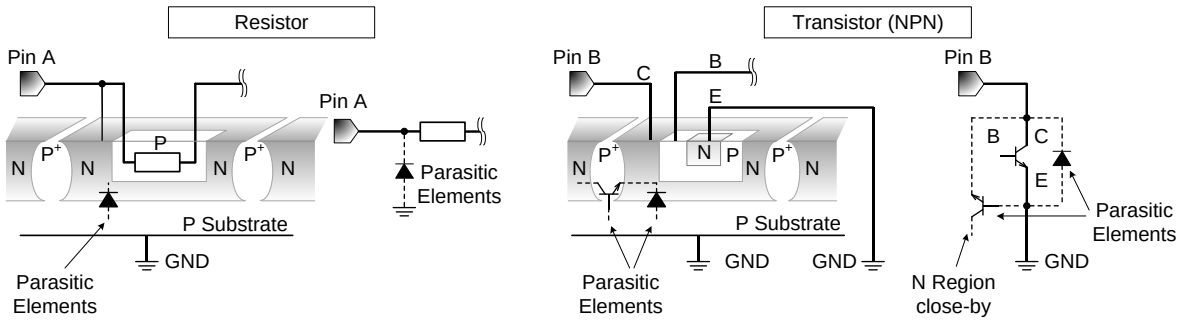


Figure 125. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

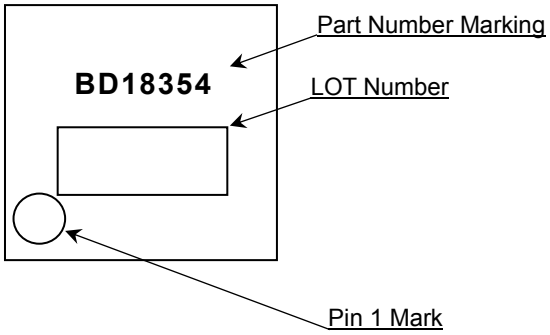
B	D	1	8	3	5	4	M	U	F	-	ME 2

Package
MUF: VQFN40FV6060

Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

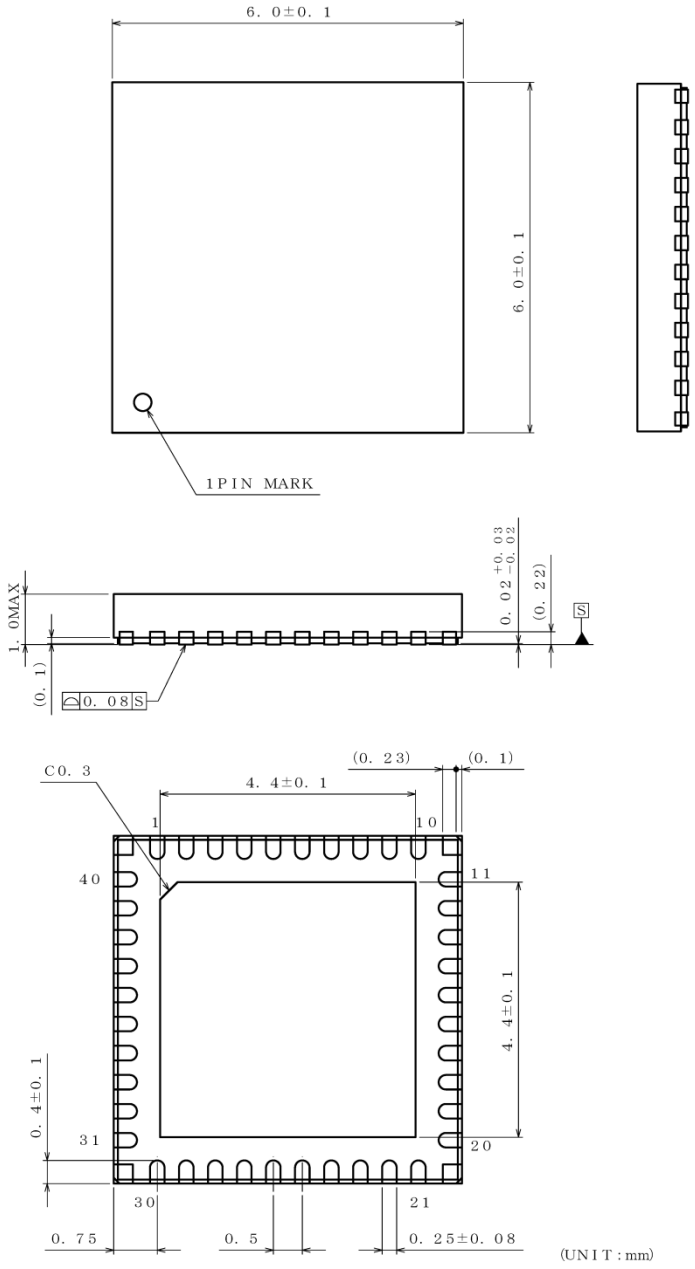
Marking Diagram

VQFN40FV6060 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN40FV6060

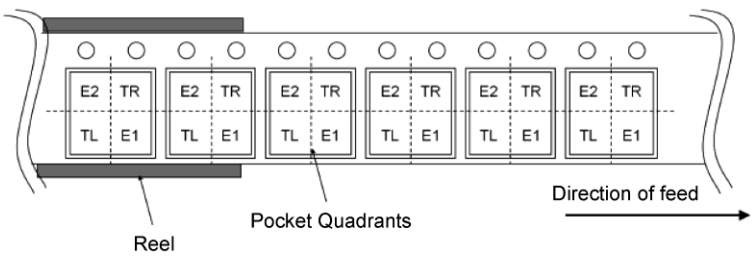


NOTE: Dimensions in ( ) for reference only.

PKG: VQFN40FV6060
Drawing No. EX406-5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
25.Jun.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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