Datasheet

Automotive LED Driver Series

64-channel Constant Current Drivers Embedded Backlight LED Driver for Automotive

BD83164MWF-M

General Description

BD83164MWF-M is embedded 64-channel constant current drivers with 16-bit PWM dimming. This device can set LED constant current value by setting external ISET Resistor. Communication via SPI is feasible.

Key Specifications

- Power Supply Voltage Range: 3.0 V to 5.5 V
- Maximum LEDn Pin Voltage (n = 1 to 64): 10 V
- LED Output Current Setting Range:10 mA to 45 mA
- Operating Temperature Range: -40 °C to +125 °C

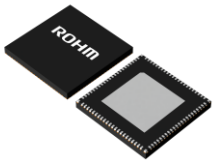
Features

- AEC-Q100 Qualified*(Note 1)*
- Integrated 64-channel LED Constant Current Drivers
- SPI Interface (Cascade Connection Feasible)
- 16-bit PWM Dimming (Min On Pulse 0.5 µs)
- 6-bit Global DC Dimming (50 % to 100 %)
- LED Constant Current Setting by ISET Resistor
- Phase Shift Function (16 bits)
- LED Open Detection and LED Short Detection
- Abnormal Output FAILB Pin

(Note 1) Grade 1

Package

Package	W (Typ) x D (Typ) x H (Max)
UQFN88FBV100	10.0 mm x 10.0 mm x 1.0 mm



UQFN88FBV100

Applications

- Cluster, Center Infotainment Display
- Other Automotive Backlights

Typical Application Circuit

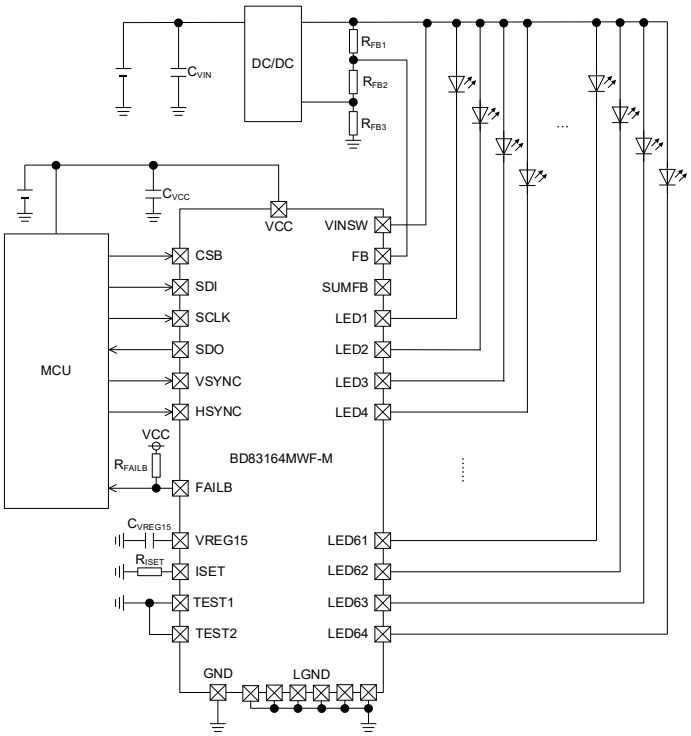


Figure 1. Typical Application Circuit

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Pin Configuration

UQFN88FBV100 (TOP VIEW)

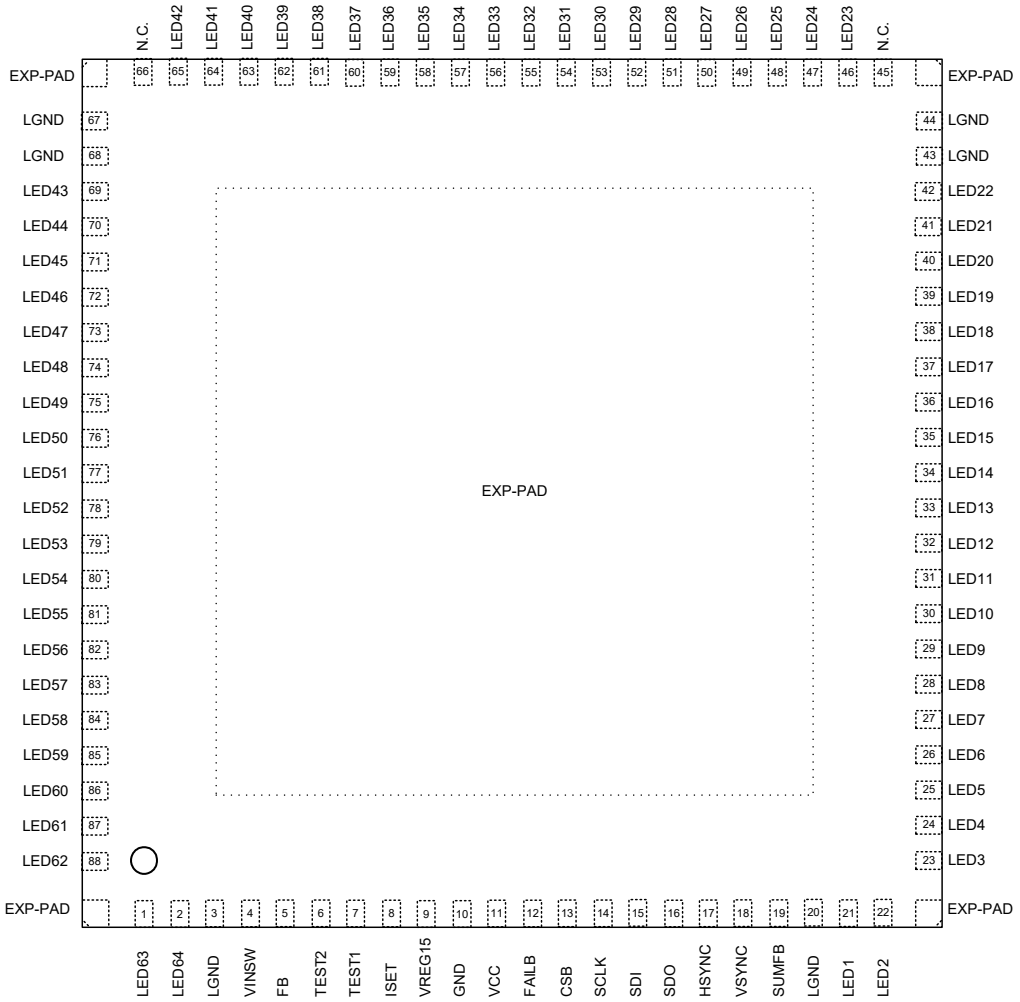


Figure 2. Pin Configuration

Pin Descriptions

Pin Number	Pin Name	Signal Type *(Note 1)*	Function
1	LED63	P	Output constant current channel 63
2	LED64	P	Output constant current channel 64
3	LGND	P	Analog GND for constant current driver block
4	VINSW	A	OVP detection pin for DC/DC voltage
5	FB	A	Control DC/DC voltage pin
6	TEST2	A	TEST2 pin (required: short to GND)
7	TEST1	A	TEST1 pin (required: short to GND)
8	ISET	A	LED constant current setting pin
9	VREG15	A	Output of 1.5 V voltage regulator (required: Not used as a pull-up power supply)
10	GND	A	Common GND
11	VCC	P	Power supply pin
12	FAILB	O	Abnormal operation detection output pin

(Note 1) **A:** Sensitive signal such as detect and reference, **O:** Output signal from IC, **P:** Large current signal susceptible to impedance, including transient current.

Pin Descriptions – continued

Pin Number	Pin Name	Signal Type *(Note 1)*	Function
13	CSB	I	SPI device select setting pin
14	SCLK	I	SPI CLK input pin
15	SDI	I	SPI data input pin
16	SDO	O	SPI data output pin
17	HSYNC	I	HSYNC signal input pin
18	VSYNC	I	VSYNC signal input pin
19	SUMFB	I/O	Control FB current pin
20	LGND	P	Analog GND for constant current driver block
21	LED1	P	Output constant current channel 1
22	LED2	P	Output constant current channel 2
23	LED3	P	Output constant current channel 3
24	LED4	P	Output constant current channel 4
25	LED5	P	Output constant current channel 5
26	LED6	P	Output constant current channel 6
27	LED7	P	Output constant current channel 7
28	LED8	P	Output constant current channel 8
29	LED9	P	Output constant current channel 9
30	LED10	P	Output constant current channel 10
31	LED11	P	Output constant current channel 11
32	LED12	P	Output constant current channel 12
33	LED13	P	Output constant current channel 13
34	LED14	P	Output constant current channel 14
35	LED15	P	Output constant current channel 15
36	LED16	P	Output constant current channel 16
37	LED17	P	Output constant current channel 17
38	LED18	P	Output constant current channel 18
39	LED19	P	Output constant current channel 19
40	LED20	P	Output constant current channel 20
41	LED21	P	Output constant current channel 21
42	LED22	P	Output constant current channel 22
43	LGND	P	Analog GND for constant current driver block
44	LGND	P	Analog GND for constant current driver block
45	N.C.	-	Not connected internally.
46	LED23	P	Output constant current channel 23
47	LED24	P	Output constant current channel 24
48	LED25	P	Output constant current channel 25
49	LED26	P	Output constant current channel 26
50	LED27	P	Output constant current channel 27
51	LED28	P	Output constant current channel 28

(Note 1) **I:** Input signal from other units, **O:** Output signal from IC, **P:** Large current signal susceptible to impedance, including transient current.

Pin Descriptions – continued

Pin Number	Pin Name	Signal Type *(Note 1)*	Function
52	LED29	P	Output constant current channel 29
53	LED30	P	Output constant current channel 30
54	LED31	P	Output constant current channel 31
55	LED32	P	Output constant current channel 32
56	LED33	P	Output constant current channel 33
57	LED34	P	Output constant current channel 34
58	LED35	P	Output constant current channel 35
59	LED36	P	Output constant current channel 36
60	LED37	P	Output constant current channel 37
61	LED38	P	Output constant current channel 38
62	LED39	P	Output constant current channel 39
63	LED40	P	Output constant current channel 40
64	LED41	P	Output constant current channel 41
65	LED42	P	Output constant current channel 42
66	N.C.	-	Not connected internally.
67	LGND	P	Analog GND for constant current driver block
68	LGND	P	Analog GND for constant current driver block
69	LED43	P	Output constant current channel 43
70	LED44	P	Output constant current channel 44
71	LED45	P	Output constant current channel 45
72	LED46	P	Output constant current channel 46
73	LED47	P	Output constant current channel 47
74	LED48	P	Output constant current channel 48
75	LED49	P	Output constant current channel 49
76	LED50	P	Output constant current channel 50
77	LED51	P	Output constant current channel 51
78	LED52	P	Output constant current channel 52
79	LED53	P	Output constant current channel 53
80	LED54	P	Output constant current channel 54
81	LED55	P	Output constant current channel 55
82	LED56	P	Output constant current channel 56
83	LED57	P	Output constant current channel 57
84	LED58	P	Output constant current channel 58
85	LED59	P	Output constant current channel 59
86	LED60	P	Output constant current channel 60
87	LED61	P	Output constant current channel 61
88	LED62	P	Output constant current channel 62
-	EXP-PAD	-	The EXP-PAD should be connected to the board ground. The center and corner EXP-PADs are shorted inside the package.

(Note 1) **P:** Large current signal susceptible to impedance, including transient current.

Block Diagram

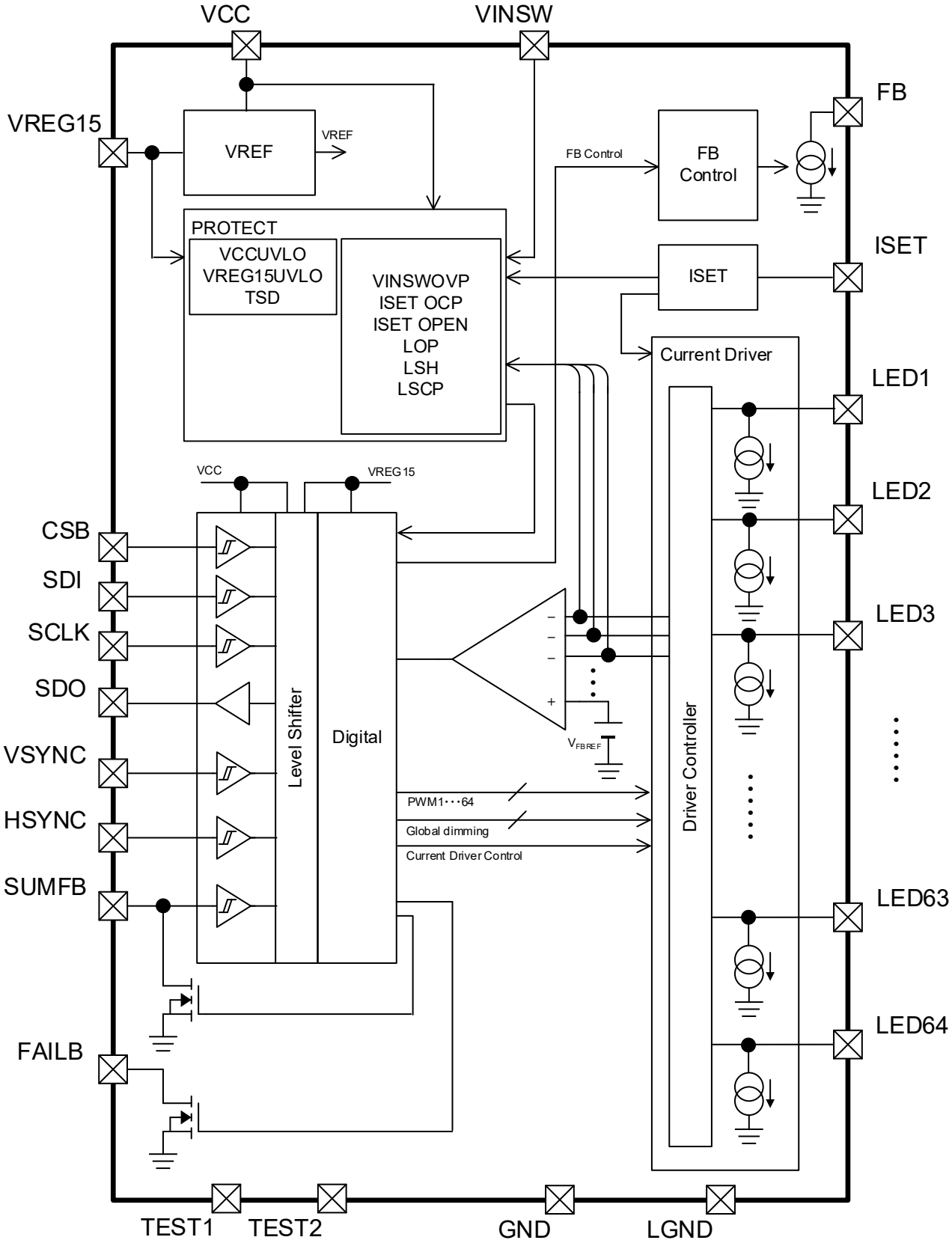


Figure 3. Internal Block Diagram

Description of Blocks

If there is no description, the mentioned values are typical value. The suffixes n represents the number of current driver (n = 1 to 64), respectively. For example, LEDn means LED1, LED2,,,LED64. This expression is applicable to the whole of this datasheet.

1 VREF

Internal reference voltage circuit. VREF block generates the reference voltage and outputs 1.5 V to the VREG15 pin. It cannot be used to supply power to external components from this IC. Connect a ceramic capacitor (C_{VREG15}) to the VREG15 pin for phase margin. C_{VREG15} range is 0.47 µF to 6.8 µF and recommended value is 2.2 µF. If the C_{VREG15} is not connected, unstable operation might occur e.g. oscillation.

2 Current Driver / ISET

Current driver circuit for lighting LED. This device has 64-channel constant current drivers. Maximum LED current level I_{LEDMAX} (≤ 45 mA) of all channels is set by the external res R_{ISET} of the ISET pin. The global dimming current I_{LEDn} (50 % to 100 %) is set by the register IREF[5:0]. And the PWM dimming is set by the register DTYCNTn[15:0].

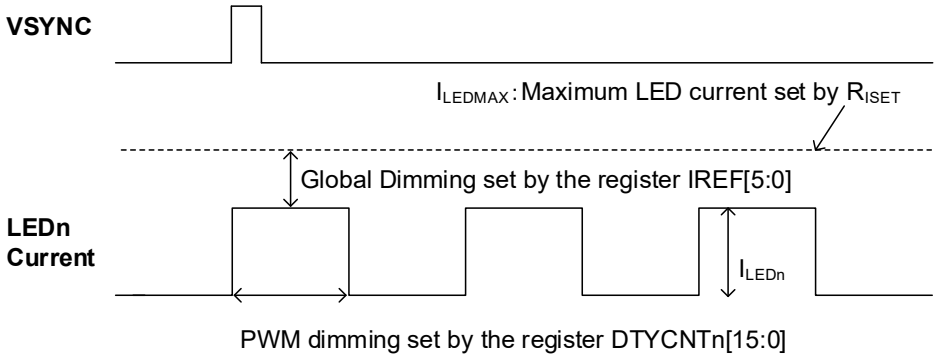


Figure 4. LED Current Setting Method for Dimming

2.1 Output Current Setting and Global DC Dimming

I_{LEDMAX} and I_{LEDn} can be calculated by the following equation.
Recommended I_{LEDMAX} setting range is from 10 mA to 45 mA.

$$I_{LEDMAX} = \frac{1200k}{R_{ISET}} \quad [\text{mA}]$$

$$I_{LEDn} = I_{LEDMAX} \times \frac{(IREF[5:0]+64)}{127} \quad [\text{mA}]$$

I_{LEDn} can be used from 10 mA to 45 mA. For example, I_{LEDMAX} = 20 mA (R_{ISET} = 60 kΩ), IREF[5:0] can set full range, but I_{LEDMAX} = 10 mA (R_{ISET} = 120 kΩ), IREF[5:0] should be set all High. It is possible to adjust the current using IREF[5:0] during operation.
Evaluate the actual operation sufficiently to change IREF[5:0] during feedback using DC/DC because unstable operation such as flickering may occur.

2 Current Driver / ISET - continued

2.2 Local PWM Dimming Control

PWM dimming frequency and pulse width are set by SPI commands. Constant current driver can be controlled synchronized to the internal signal PWMn for each channel set by SPI.
The minimum pulse width of constant current driver is limited to 0.5 μs.
The accurate average current of $I_{LEDAVEn}$ is expressed as follows, f_{HSYNC} = 65535 x f_{VSYNC}.

$$I_{LEDAVEn} = I_{LEDn} \times \{(DTYCNTn[15:0])/65535\} \quad [\text{mA}]$$

2.3 Delay Control (Phase Shift)

This IC integrates 16-bit local (each channel) delay function. The delay amount is set in DLY01[15:0] to DLY64[15:0]. The delay resolution is 1 HSYNC. In case VSYNC frequency is 240 Hz, HSYNC is 15728400 Hz, so the delay rate can be set by 64 ns steps.
If DLYn[15:0] is 0, LED current will occur 5 or 6 HSYNC clocks after VSYNC rises.
If the length of the local delay and duty is more than the VSYNC period, the remaining “ON” width is output at the next VSYNC period as shown in Figure 5.

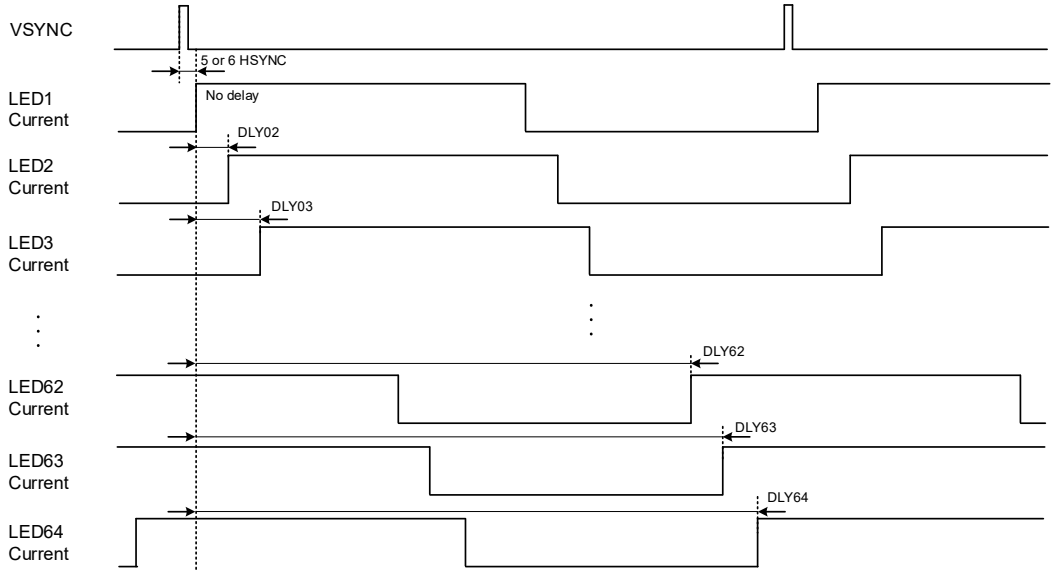


Figure 5. Delay Control

2.4 LEDn Pin Handling for Unused Channels

Set LEDEN[n-1] of unused CHs to 0 and open the pin. When the protection function is active, a high impedance state (unused CHs are OPEN) may result in false protection detection. Therefore, it is highly recommended that PRCEN is set to 1.

Description of Blocks – continued

3 FB Control

FB pin sink current controller. The DC/DC output voltage is controlled by the FB pin sink current. Each LED pin voltage is sampled at a timing determined by SMPTIM[2:0]. The FB pin sink current flows so that the minimum LED pin voltage is equal to the Feedback Reference Voltage (V_{FBREF}). The FB sink current is controlled by FBDAC. As shown in Figure 7, the FB pin sink current changes with FBDAC setting step every VSYNC rise. Considering the FB pin sink current (the maximum FB sink pin current is 200 µA), the resistors between this device and the DC/DC in Figure 6 must be determined. The FB pin voltage must be more than 0.6 V for the FB pin to function properly. Using DC/DC feedback, it is recommended to set the components to satisfy the following formula under typical conditions. Vripple depends on external components and register settings. If Vripple is large, LED current may be unstable, resulting in brightness degradation and flickering. Designing for mass production, make sure to check the actual device before setting. In addition, when all PWMDTYn have a minimum width such as 500 ns, the LED pin voltage drop is delayed by the parasitic capacitance of the LED elements and the capacitors mounted on the LED pins. As a result, the LED pin voltage cannot be sampled accurately and the constant current driver may not be able to control stably due to insufficient output voltage. Please check the actual device thoroughly or contact us regarding the setting.

$$V_{FBREF} + V_f = V_{DC/DC\ FB} \times \frac{R_{FB1} + R_{FB2} + R_{FB3}}{R_{FB3}} + R_{FB1} \times 100\ \mu A \qquad [V]$$

$$V_{FBREF} > R_{LEDn} \times I_{LEDMAX} + V_{ripple} \qquad [V]\ \textit{(Note 1)}$$

V_{FBREF}	: Feedback reference voltage of BD83164MWF-M
V_f	: Forward voltage of LED
$V_{DC/DC\ FB}$	: Feedback reference voltage of DC/DC IC
$R_{FB1}, R_{FB2}, R_{FB3}$	: Resistor to divide DC/DC VOUT
R_{LEDn}	: LEDn pin on resistance (Max = 10 Ω)
I_{LEDMAX}	: LED current determined by the resistor connected to the ISET pin
V_{ripple}	: DC/DC VOUT ripple due to DC/DC operation, PWM operation, FB pin sink current rate and sampling error

(Note 1) It is recommended to calculate V_{ripple} as 200 mV.

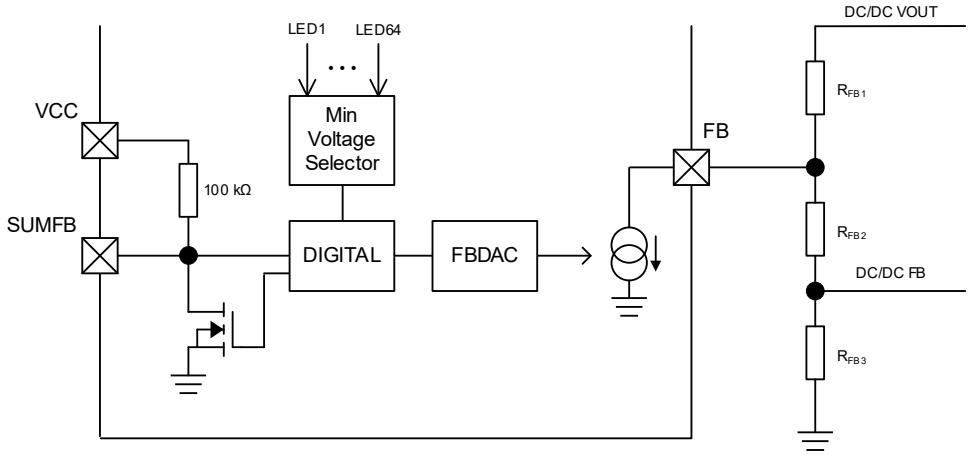


Figure 6. FB Control Block Diagram

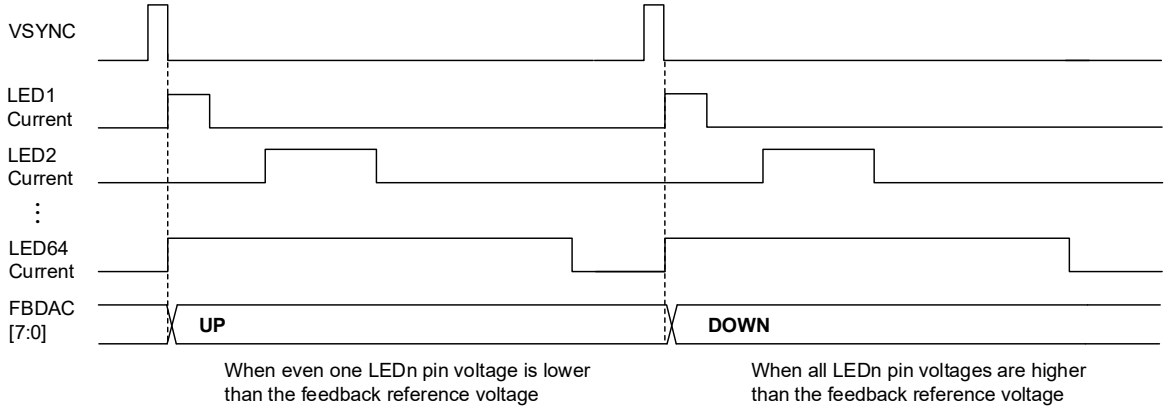


Figure 7. FB Control Timing

Description of Blocks – continued

4 PROTECT

Outputs the status of protective operation from the FAILB pin and the SDO pin. Since the FAILB pin is an open drain output, connect it to the VCC pin with a resistor. If the FAILB pin is not monitored, turn the FAILB pin to OPEN or connect to the GND pin.

4.1 VCC Under Voltage Lock Out (VCCUVLO)

This is VCC under voltage protection function.
When VCCUVLO is detected, FAILB goes Low and this IC returns to initial state.
The error condition is retained unless ERRCLR[0] is written to 1.

4.2 VREG15 Under Voltage Lock Out (VREG15UVLO)

This is VREG15 under voltage protection function.
When VREG15UVLO is detected, FAILB goes Low and this IC returns to initial state.
The error condition is retained unless ERRCLR[0] is written to 1.

4.3 Thermal Shutdown (TSD)

This is thermal shutdown function.
When TSD is detected, FAILB goes Low and this IC returns to initial state.
The error condition is retained unless ERRCLR[0] is written to 1.

4.4 VINSW Over Voltage Protection (VINSWOVP)

This is VINSW over voltage protection function.
When VINSWOVP is detected, FAILB goes Low and the status of Error register is updated.
The detection voltage of VINSWOVP can be changed by VINSWOVPREF[1:0].

4.5 ISET Over Current Protection (ISETOCP)

This is ISET over current protection function.
When ISETOCP is detected, FAILB goes Low and the status of Error register is updated.

4.6 ISET Open Protection (ISETOPEN)

This is ISET open protection function.
When ISETOPEN is detected, FAILB goes Low and the status of Error register is updated.

4.7 LED Open Protection (LOP)

This is LED open protection function.
When LOP is detected, FAILB goes Low and the status of Error register is updated.
This IC can detect LOP during PWMn = High. The error condition is retained during PWMn = Low.

Caution 1: *When LOP is detected on a CH, the feedback path of that CH is pulled up to VCC. So, when LOP is detected on all driving CHs, the FB sink current decreases every VSYNC rise regardless of the LED pin voltages.*

4.8 LED Short Protection (LSH)

This is LED short protection function.
When LSH is detected, FAILB goes Low and the status of Error register is updated.
This IC can detect LSH during PWMn = High. The error condition is retained during PWMn = Low.

Caution 1: *When capacitor is attached to the LEDn pin, it is necessary to set appropriate error mask time to prevent the false detection. (Error mask time can be set with the ERRMASK[7:0])*

4.9 LED Short Circuit Protection (LSCP)

This is LED short circuit protection function.
When LSCP is detected, FAILB goes Low and the status of Error register is updated.
This IC can detect LSCP during PWMn = Low. The error condition is retained during PWMn = High.
Using LSCP function, set PRCEN[0] to 1.

Description of Blocks – continued

5 DIGITAL

IC digital processing block. This IC uses Serial Peripheral Interface (SPI) with CSB, SCLK, SDI and SDO signals. The registers of this IC are controlled via SPI, and the functions of this IC can be flexibly changed by the registers. For a detailed description of each register, see pages 35 to 54.

5.1 VSYNC Function

The clock is related to the frame rate of image processing input pin. By initial setting, the frame rate is the same frequency as the VSYNC clock.

5.2 HSYNC Function

The clock that is the basis of digital signal processing input pin. By initial setting, HSYNC clock is recommend to a frequency 65535 times the VSYNC frequency.

5.3 SUMFB Function

Using DC/DC feedback and multiple LED drivers (Daisy Chain), Short each SUMFB pin. The SUMFB pin functions as both an open-drain output with 100 kΩ pull-up of internal IC and an input pin to control the LED pin voltages of ICs. The minimum of them is controlled to be equal to the Feedback Reference Voltage (V_{FBREF}). For a single IC, it is recommended the SUMFB pin to be OPEN.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage Range	V_{CC}	-0.3 to +7.0	V
VREG15, ISET Pin Voltage Range	V_{REG15}, V_{ISET}	-0.3 to +2.1	V
VINSW, FB, LEDn Pin Voltage Range	V_{INSW}, V_{FB}, V_{LEDn} *(Note 1)*	-0.3 to +10.0	V
TEST1, TEST2 Pin Voltage Range	V_{TEST1}, V_{TEST2}	-0.3 to +V_{CC}	V
FAILB, CSB, SCLK, SDI, SDO, VSYNC, HSYNC, SUMFB Pin Voltage Range	V_{FAILB}, V_{CSB}, V_{SCLK}, V_{SDI}, V_{SDO}, V_{VSYNC}, V_{HSYNC}, V_{SUMFB}	-0.3 to +V_{CC}	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum LEDn Output Current	I_{LEDn}	50 *(Note 2)(Note 3)*	mA

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) n = 1 to 64

(Note 2) Wide Vf variation of LED increases loss at the driver, which results in rise in package temperature. Therefore, the board needs to be designed with attention paid to heat radiation.

(Note 3) This current value is per 1ch. It needs be used within a range not exceeding Tjmax.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
UQFN88FBV100				
Junction to Ambient	θ_{JA}	57.1	21.0	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	6.0	3.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air). The BD83164MWF-M chip is used.

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	-	+125	°C
Power Supply Voltage 1	V_{CC}	3.0	5.0	5.5	V
Power Supply Voltage 2	V_{INSW}	-	-	10	V
HSYNC Frequency	f_{HSYNC}	-	-	20	MHz
HSYNC Duty	D_{HSYNC}	40	-	60	%
VSYNC Frequency	f_{VSYNC}	50	-	300	Hz
VSYNC Minimum On Pulse Width	$t_{VSYNCMIN}$	50	-	-	μs
PWM Minimum Pulse Width	t_{PWMMIN}	0.5	-	-	μs
LEDn Pin Output Current	I_{LEDn}	10	-	45	mA

Operating Conditions (External component value range)

Parameter	Symbol	Min	Typ	Max	Unit
VCC Pin Connection Capacitor	C_{VCC}	1.0*(Note 1)*	2.2	10.0	μF
VREG15 Pin Connection Capacitor	C_{VREG15}	0.47*(Note 1)*	2.20	6.80	μF
ISET Pin Resistor	R_{ISET}	26.7*(Note 1)*	-	120	kΩ
FAILB Pin Pull up Resistor	R_{FAILB}	9*(Note 1)*	-	110	kΩ

(Note 1) Set resistor and capacitor values so that it does not fall below the minimum value in consideration of variations in temperature characteristics, DC bias characteristics, etc.

Electrical Characteristics
(Unless otherwise specified V_{CC} = 3.0 V to 5.5 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Device Overview]						
Circuit Current 1	I_{CC1}	-	8.5	13.0	mA	V_{VSYNC} = V_{HSYNC} = V_{CSB} = V_{SCLK} = V_{SDI} = Low
Circuit Current 2	I_{CC2}	-	24	36	mA	f_{VSYNC} = 120 Hz f_{HSYNC} = 7,684,320 Hz V_{CSB} = V_{SCLK} = V_{SDI} = Low R_{ISET} = 40 kΩ LEDEN1601[15:0] = 0xFFFF LEDEN3217[15:0] = 0xFFFF LEDEN4833[15:0] = 0xFFFF LEDEN6449[15:0] = 0xFFFF
[VREG15 Block]						
VREG15 Pin Output Voltage	V_{REG15}	1.41	1.53	1.65	V	I_{VREG15} = 0 mA
[PROTECT LOGIC Block]						
VCCUVLO Detection Voltage	$V_{CCUVLO1}$	2.42	2.56	2.70	V	V_{CC} = Sweep Down
VCCUVLO Release Voltage	$V_{CCUVLO2}$	2.64	2.78	2.92	V	V_{CC} = Sweep Up
VCCUVLO Hysteresis Voltage	$V_{CCUVLOHYS}$	-	220	-	mV	
VREG15UVLO Detection Voltage	$V_{REG15UVLO}$	1.18	1.25	1.32	V	V_{REG15} = Sweep Down
LEDn Pin Open Detection Voltage *(Note 1)*	V_{LOP}	0.09	0.15	0.21	V	
LEDn Pin Short Detection Voltage 1 *(Note 1)*	V_{LSH1}	0.9	1.3	1.7	V	LEDSH[1:0] = 0x0
LEDn Pin Short Detection Voltage 2 *(Note 1)*	V_{LSH2}	2.2	2.6	3.0	V	LEDSH[1:0] = 0x1
LEDn Pin Short Detection Voltage 3 *(Note 1)*	V_{LSH3}	3.5	3.9	4.3	V	LEDSH[1:0] = 0x2
LEDn Pin Short Detection Voltage 4 *(Note 1)*	V_{LSH4}	4.8	5.2	5.6	V	LEDSH[1:0] = 0x3
ISET Pin Over Current Detection Resistor	$R_{ISETOCP}$	-	12	-	kΩ	IREF[5:0] = 0x3F
ISET Pin Open Detection Resistor	$R_{ISETOPEN}$	-	440	-	kΩ	IREF[5:0] = 0x3F
VINSW Pin Over Voltage Detection 1	$V_{INSWOVP1}$	5.5	6.0	6.5	V	VINSWOVPREF[1:0] = 0x0
VINSW Pin Over Voltage Detection 2	$V_{INSWOVP2}$	6.5	7.0	7.5	V	VINSWOVPREF[1:0] = 0x1
VINSW Pin Over Voltage Detection 3	$V_{INSWOVP3}$	7.5	8.0	8.5	V	VINSWOVPREF[1:0] = 0x2
VINSW Pin Over Voltage Detection 4	$V_{INSWOVP4}$	8.5	9.0	9.5	V	VINSWOVPREF[1:0] = 0x3
[LOGIC Input Block (CSB, SCLK, SDI, VSYNC, HSYNC)] *(Note 2)*						
Input High Voltage	V_{INH}	V_{CC} x 0.75	-	-	V	
Input Low Voltage	V_{INL}	-	-	V_{CC} x 0.2	V	
Input Current	I_{IN}	-0.8	0	+0.8	µA	V_{IN} = 0 V to V_{CC}
[SDO Output Block]						
Output High Voltage	V_{OUTH}	V_{CC} -0.2	-	V_{CC}	V	I_{SDO} = -1 mA
Output Low Voltage	V_{OUTL}	-	-	0.2	V	I_{SDO} = 1 mA

(Note 1) n = 1 to 64
(Note 2) V_{CSB}, V_{SCLK}, V_{SDI}, V_{VSYNC}, V_{HSYNC} are judged as High more than V_{CC} x 0.75 and as Low less than V_{CC} x 0.2.
Do not use this IC in the condition of V_{CSB}, V_{SCLK}, V_{SDI}, V_{VSYNC}, V_{HSYNC} between V_{CC} x 0.75 and V_{CC} x 0.2.

Electrical Characteristics – continued
(Unless otherwise specified V_{CC} = 3.0 V to 5.5 V, Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Constant Current Driver Block]						
ISET Pin Voltage	V_{ISET}	1.20	1.25	1.30	V	IREF[5:0] = 0x3F
LEDn Pin ON Resistance*(Note 1)*	R_{LEDn}	-	-	10	Ω	
LEDn Pin Current Absolute Error ((I_{LEDAVE} / I_{LEDMAX} - 1) x 100)*(Note 1)(Note 2)*	ΔI_{LEDnA}	-2	-	+2	%	Ta = +25 °C R_{ISET} = 40 kΩ PWMn = 100 % IREF[5:0] = 0x3F
		-3	-	+3	%	Ta= -40 °C to +125 °C R_{ISET} = 40 kΩ PWMn = 100 % IREF[5:0] = 0x3F
LEDn Pin Current Relative Error ((I_{LEDn} / I_{LEDAVE} - 1) x 100)*(Note 1)(Note 3)*	ΔI_{LEDnR}	-5	-	+5	%	Ta = +25 °C R_{ISET} = 40 kΩ PWMn = 100 % IREF[5:0] = 0x3F
		-8	-	+8	%	Ta= -40 °C to +125 °C R_{ISET} = 40 kΩ PWMn = 100 % IREF[5:0] = 0x3F
LEDn Pin Leak Current*(Note 1)*	$I_{LEDnLEAK}$	-	-	1	μA	V_{LEDn} = 9 V V_{INSW} = 9 V
LEDn Pin Pull-up Current*(Note 1)*	$I_{LEDnPRC}$	80	160	240	μA	V_{LEDn} = 1.5 V LEDEN1601[15:0] = 0x0000 LEDEN3217[15:0] = 0x0000 LEDEN4833[15:0] = 0x0000 LEDEN6449[15:0] = 0x0000 PRCEN[0] = 0x1
[Feedback Control Block]						
Feedback Reference Voltage 1	V_{FB1}	0.40	0.45	0.50	V	FBREF[2:0] = 0x0
Feedback Reference Voltage 2	V_{FB2}	0.45	0.50	0.55	V	FBREF[2:0] = 0x1
Feedback Reference Voltage 3	V_{FB3}	0.50	0.55	0.60	V	FBREF[2:0] = 0x2
Feedback Reference Voltage 4	V_{FB4}	0.55	0.60	0.65	V	FBREF[2:0] = 0x3
Feedback Reference Voltage 5	V_{FB5}	0.60	0.65	0.70	V	FBREF[2:0] = 0x4
Feedback Reference Voltage 6	V_{FB6}	0.65	0.70	0.75	V	FBREF[2:0] = 0x5
Feedback Reference Voltage 7	V_{FB7}	0.70	0.75	0.80	V	FBREF[2:0] = 0x6
Feedback Reference Voltage 8	V_{FB8}	0.75	0.80	0.85	V	FBREF[2:0] = 0x7
FB Pin Maximum Sink Current	I_{FBMAX}	170	200	230	μA	FBDAC[7:0] = 0xFF V_{FB} = 1 V
FB Pin ON Resistance	R_{FB}	-	-	3.0	kΩ	
SUMFB Pin ON Resistance	R_{SUMFBL}	10	120	250	Ω	I_{SUMFB} = 1 mA
SUMFB Pin Pull-up Resistance to VCC	R_{SUMFBH}	50	100	150	kΩ	
[FAILB Output Block]						
FAILB Pin ON Resistance	R_{FAILBL}	10	70	200	Ω	I_{FAILB} = 1 mA
FAILB Pin Leak Current	$I_{FAILBLEAK}$	-	0	1	μA	V_{FAILB} = 5 V

(Note 1) n = 1 to 64
(Note 2) ΔI_{LEDnA} = (I_{LEDAVE} / I_{LEDMAX} - 1) x 100
I_{LEDAVE} is the average current of LED1 to LED64.
I_{LEDMAX} is LED current determined by the resistor connected to the ISET pin.
(Note 3) ΔI_{LEDnR} = (I_{LEDn} / I_{LEDAVE} - 1) x 100

Typical Performance Curves

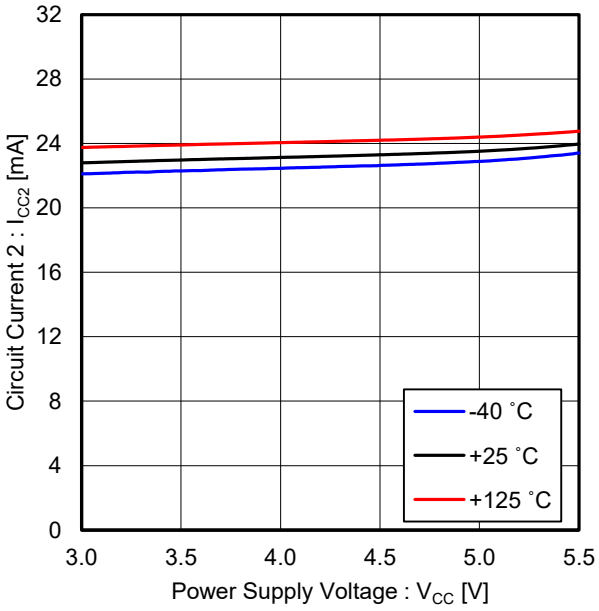


Figure 8. Circuit Current 2 vs Power Supply Voltage

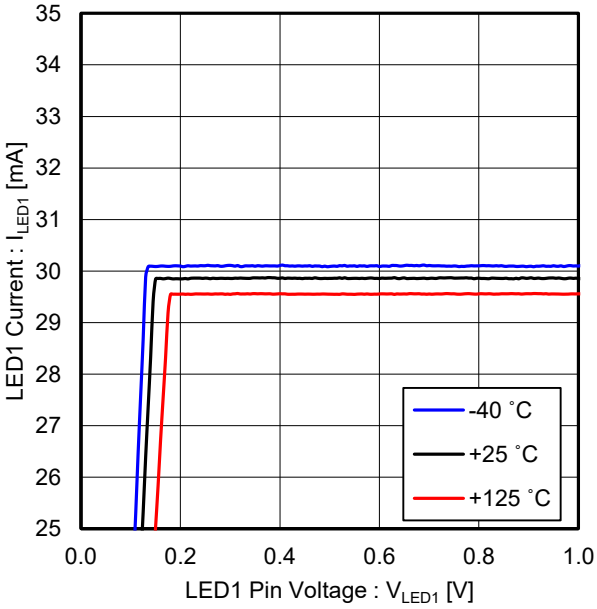


Figure 9. LED1 Current vs LED1 Pin Voltage (V_{CC} = 3.3 V)

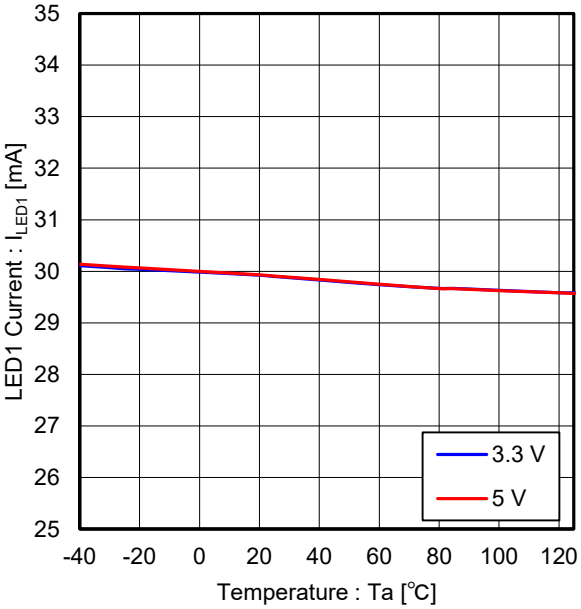


Figure 10. LED1 Current vs Temperature

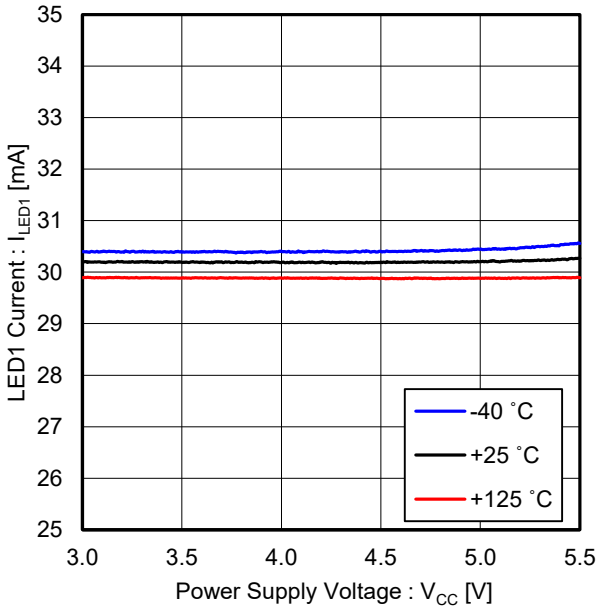


Figure 11. LED1 Current vs Power Supply Voltage

Typical Performance Curves – continued

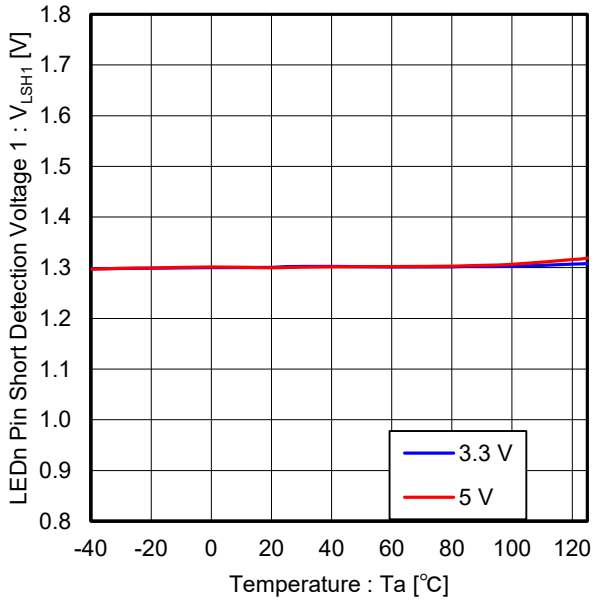


Figure 12. LEDn Pin Short Detection Voltage 1 vs Temperature

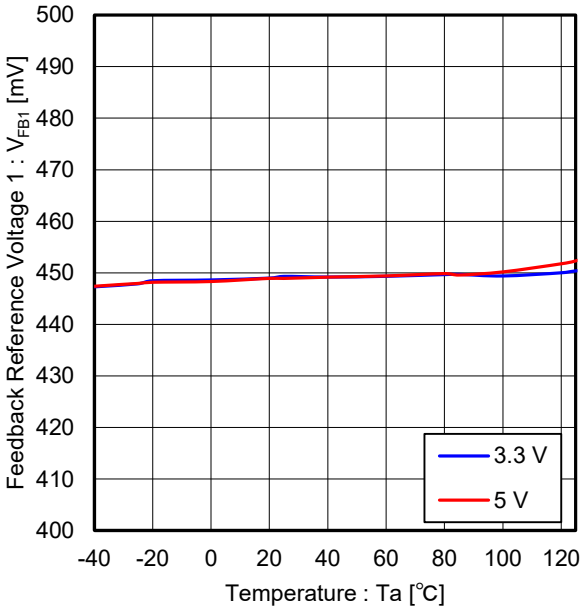


Figure 13. Feedback Reference Voltage 1 vs Temperature

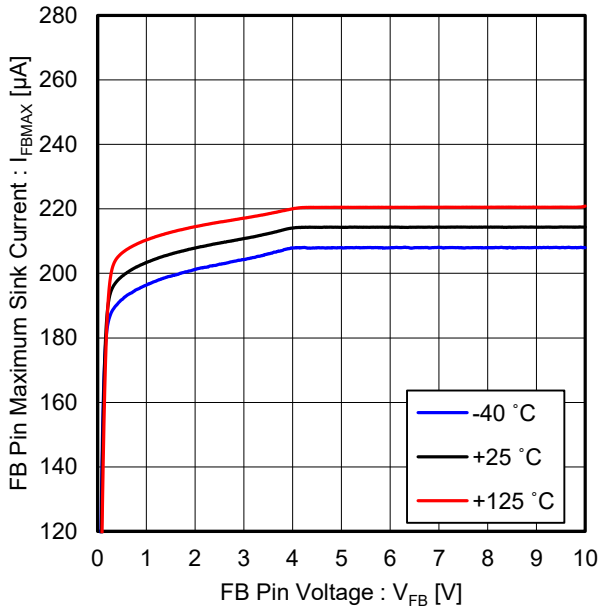


Figure 14. FB Pin Maximum Sink Current vs FB Pin Voltage (V_{CC} = 5 V)

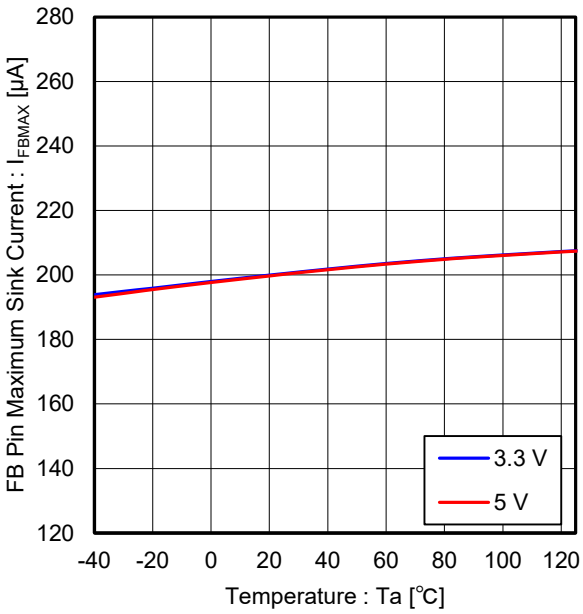


Figure 15. FB Pin Maximum Sink Current vs Temperature

Functions of Logic Block

1 Serial Interface and AC Electrical Characteristics

Serial Peripheral Interface (SPI) controls the IC with CSB, SCLK, SDI, and SDO signals.
Start the SPI communication with the initial value of CSB is High, and that of SCLK and SDI is Low.
Using multiple LED drivers, connect the SDO pin to the SDI pin of the next device to make cascade connection.
SDO signal outputs the SDI input after 16 SCLK pulses. Example of the N address write is shown in the following.
The initial value of SDO is Low until it is used to output the signal. SPI protocol is as Figure 16 and Figure 17.

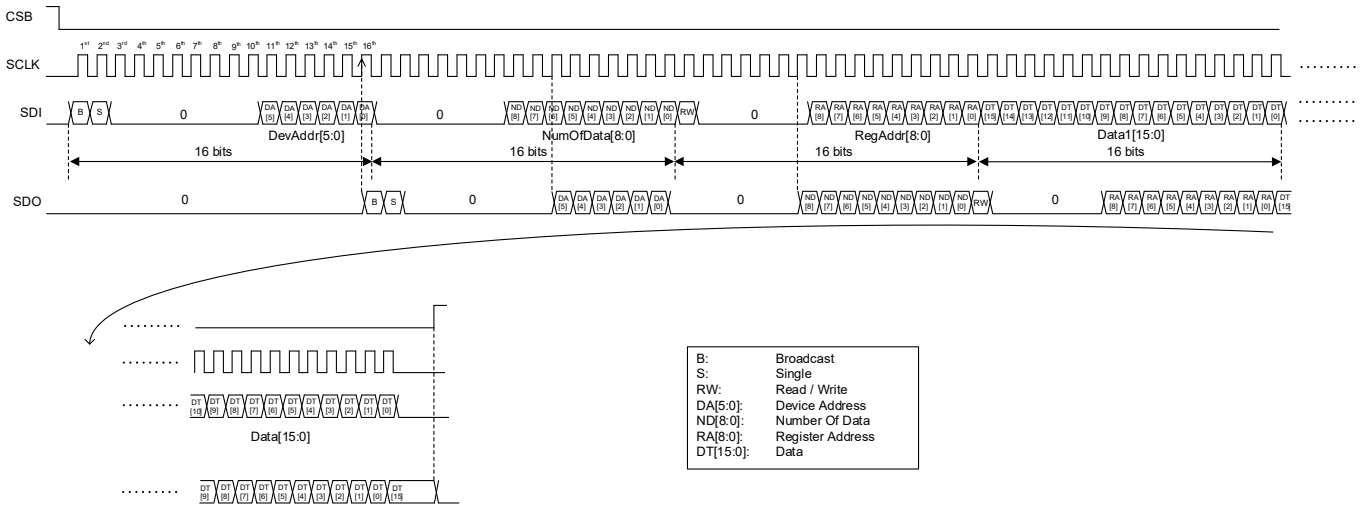


Figure 16. SPI Protocol (Write)

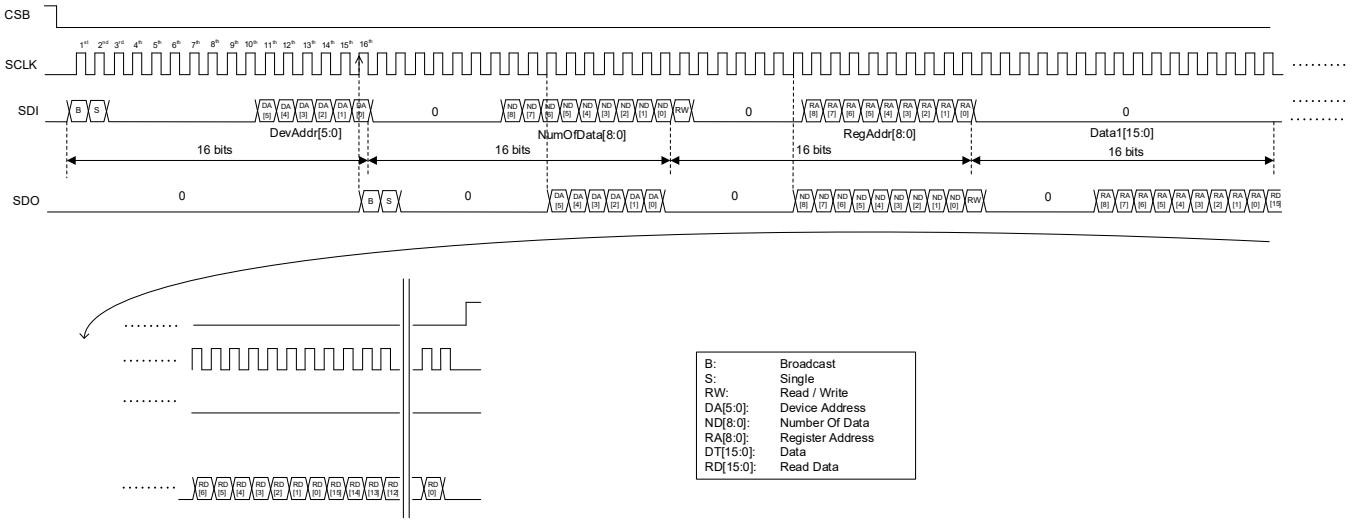


Figure 17. SPI Protocol (Read)

Functions of Logic Block – continued

2 SPI AC Timing

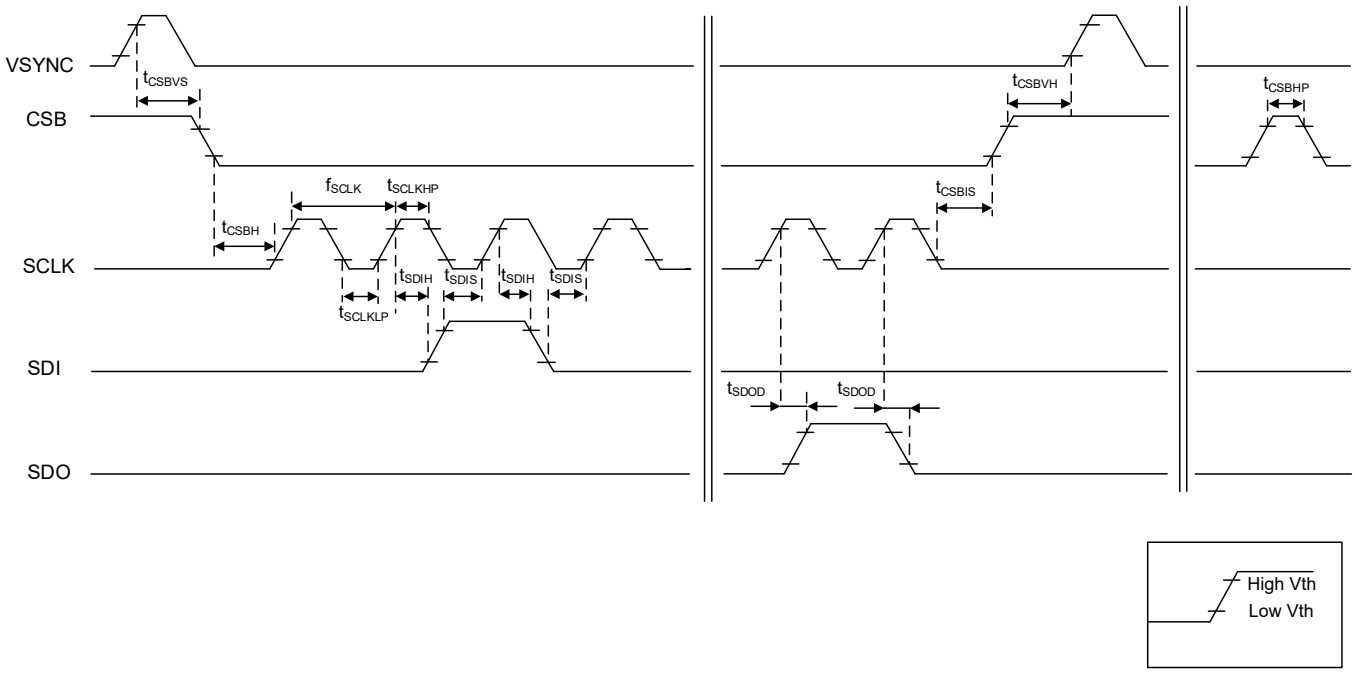


Figure 18. Timing Chart of Input Signal

SPI Recommended Operation Condition
(Unless Otherwise Specified Ta = -40 °C to +125 °C, V_{CC} = 3.0 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	0.1	-	20.0	MHz
SCLK High Pulse Width	t_{SCLKHP}	22.5	-	-	ns
SCLK Low Pulse Width	t_{SCLKLP}	22.5	-	-	ns
SDI Input Setup Time	t_{SDIS}	15	-	-	ns
SDI Input Hold Time	t_{SDIH}	15	-	-	ns
CSB Input Setup Time	t_{CSBIS}	25	-	-	ns
CSB Input Hold Time	t_{CSBH}	25	-	-	ns
SDO Output Delay Time	t_{SDOD}	-	-	30	ns
CSB High Pulse Width	t_{CSBHP}	1000	-	-	ns
CSB Setup Time for VSYNC	t_{CSBVS}	10	-	-	µs
CSB Hold Time for VSYNC	t_{CSBVH}	10	-	-	µs
Cascade Connection Number	$N_{CASCADE}$	-	-	16	pcs

Caution 1: *Do not input VSYNC rising edge during CSB = Low*

(Output load capacitance: 15 pF)

The maximum frequency of the HSYNC and VSYNC is described in the previous section “Recommended Operating Conditions”.
V_{CSB}, V_{SCLK}, V_{SDI}, V_{VSYNC}, V_{HSYNC} are judged as High more than V_{CC} x 0.75 and as Low less than V_{CC} x 0.2.
Do not use this IC in the condition of V_{CSB}, V_{SCLK}, V_{SDI}, V_{VSYNC}, V_{HSYNC} between V_{CC} x 0.75 and V_{CC} x 0.2.

Functions of Logic Block – continued

3 SPI Connection

3.1 Cascade Connection

Each device can be controlled by connecting the SCLK and CSB pins to all devices in parallel, and by connecting each SDO to the SDI of the next device in series. The maximum number of devices that can be cascaded is 16.

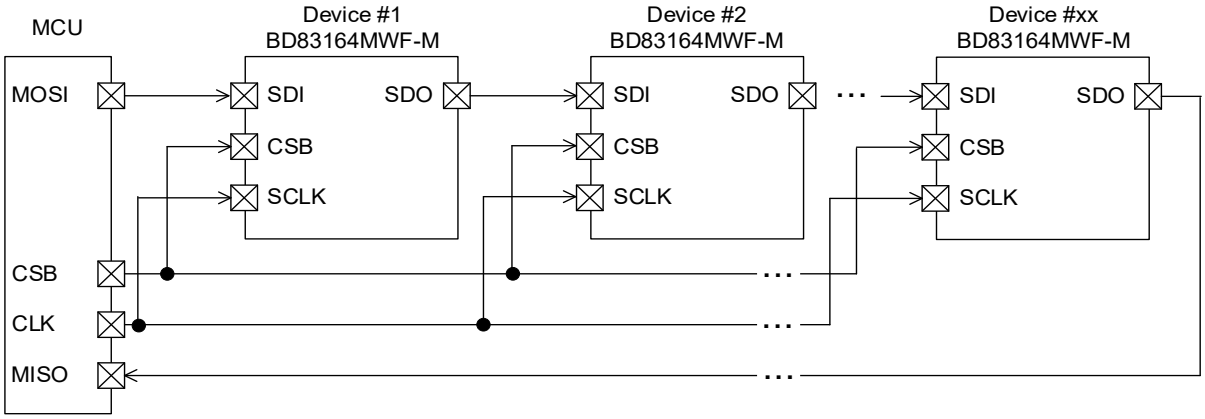


Figure 19. Image of Cascade Connection

3.2 Individual Connection

Each device can be controlled by connecting the SCLK and SDI pins to all devices in parallel, and by connecting each CSB.

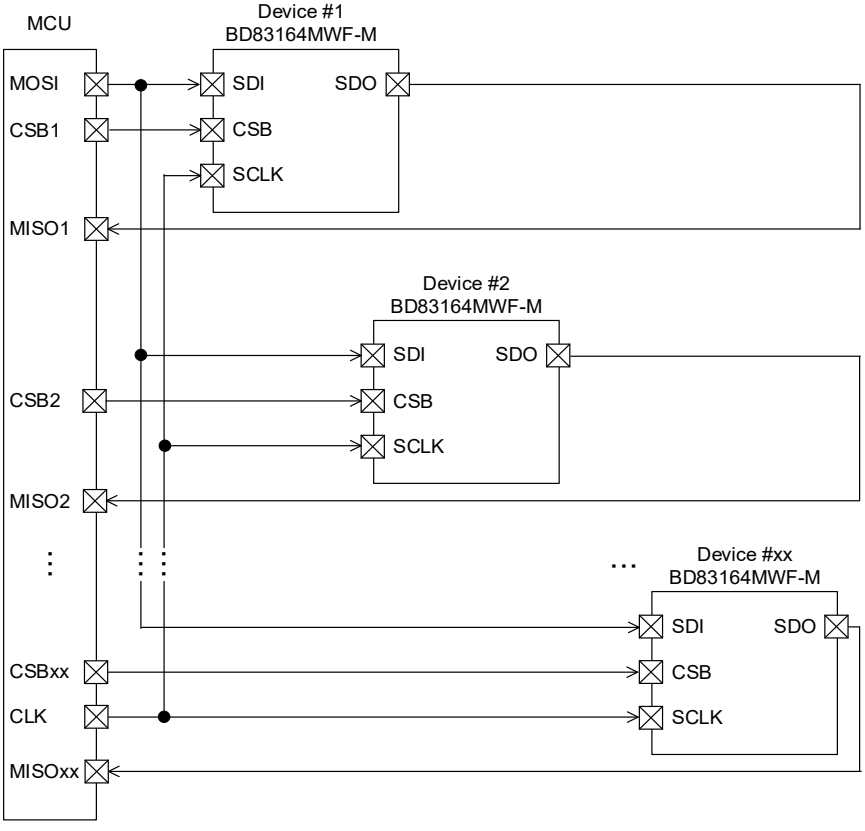


Figure 20. Image of Individual Connection

Functions of Logic Block – continued

4 SPI Data Flow

MCU Write and Read flow is shown as follow. This IC has 3 timing schemes for updating the analog control data.

Type 1 (immediately): Data is updated after SPI access.
Type 2 (VSYNC): Data is updated after SPI access and VSYNC rising edge.
Type 3 (PWM): Data is updated after SPI access and VSYNC rising edge and PWMn timing.

So, there is a lag between Read data and Control data.

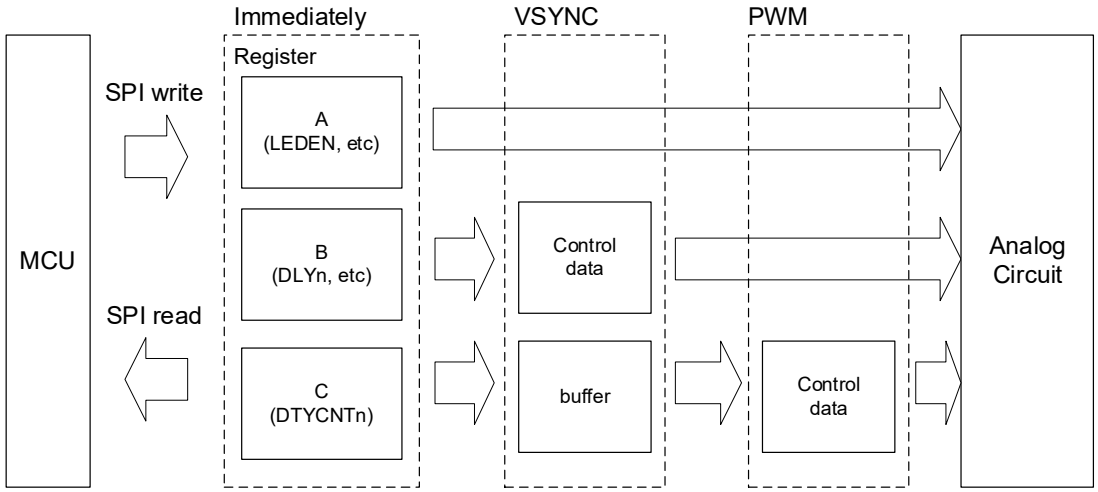


Figure 21. SPI Data Flow

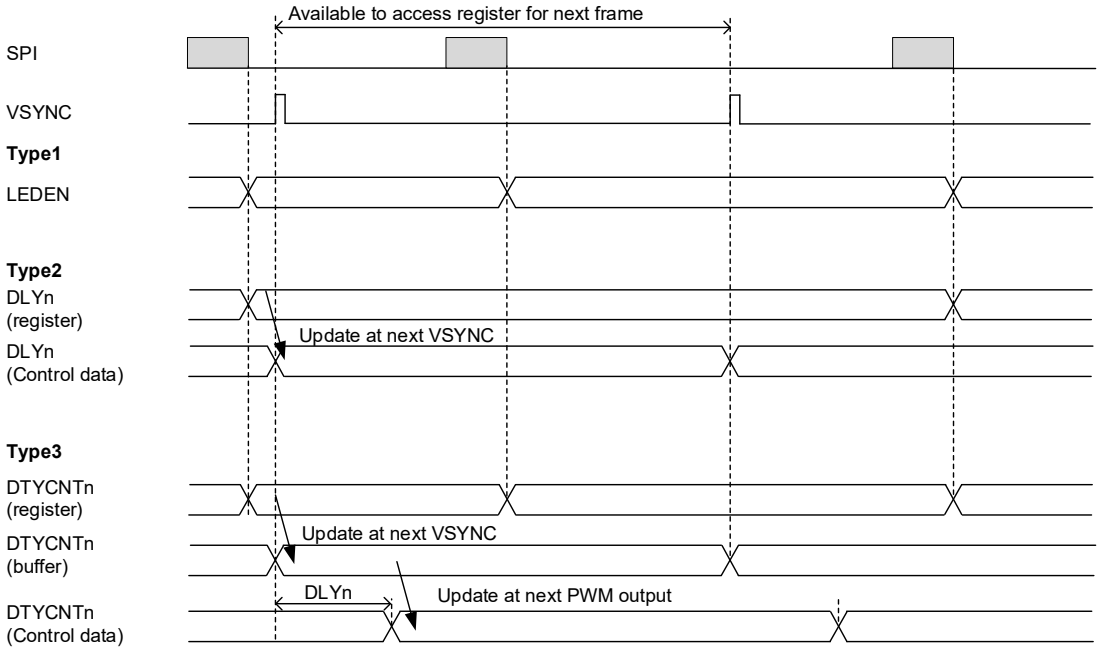


Figure 22. SPI Data Flow Timing

Functions of Logic Block – continued

5 SPI Protocol

5.1 Device Address

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B	S	0								DevAddr[5:0]					

Bit	Parameter	Value
B	Broadcast	B = 1: All devices receive the data (Write only / No Read) B = 0: Write/Read to the Device that assigned by DevAddr[5:0]
S	Single	S = 1: 1 address Write/Read mode S = 0: Block Write/Read mode
DevAddr[5:0]	Device Address	0x00: Write the same data to the same RegAddr[8:0] of all devices (provided, B = 1) 0x01 to 0x10: Device Address 0x3F: Write the different data to the same RegAddr[8:0] of all devices (provided, B = 1)

DevAddr[5:0] of each device is calculated by counting the number of byte of 0x0000 data after the falling edge of CSB. When the received DevAddr[5:0] matches with the calculated DevAddr[5:0] of the device, Write/Read function occurs. When the received DevAddr[5:0] does not match with the calculated DevAddr[5:0] of the device, the data is not received and is output to SDO. Refer to each protocol for the details.

5.2 Number of Transferred Byte When Block Write/Read

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0							NumOfData[8:0]								

Bit	Parameter	Value
NumOfData[8:0]	Number of transferred data	0x002 to 0x08F

Transferred byte number = NumOfData[8:0]

5.2 Number of Transferred Byte When Block Write/Read – continued

When S = 0 (Block Write/Read) of DevAddr[5:0], set the number of transferred byte (NumOfData) after DevAddr[5:0].
When S = 1, it skip this packet. (“Device Address” -> “Register Address” -> ….)
Access this IC using the settings as shown in Table 1 and Table 2.

Table 1. Access Table for Write (RW = 0)

SPI Setting				Access to Devices			Acceptable *(Note 1)*
B	S	DevAddr[5:0]	NumOfData[8:0]	For Single Device	For All Device		
					Same Data	Different Data	
0	0	0x00	0x002 to 0x08F	-	-	-	X
		0x01 to 0x10		O	-	-	O
		0x11 to 0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x10		O	-	-	O
				O	-	-	O
		0x11 to 0x3F		-	-	-	X
1	0	0x00	0x002 to 0x08F	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O
	1	0x00	Not sending this data	-	O	-	O
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	O	O

(Note 1) X: This setting is not acceptable. Do not set this condition.

Table 2. Access Table for Read (RW = 1)

SPI Setting				Access to Devices			Acceptable *(Note 1)*
B	S	DevAddr[5:0]	NumOfData[8:0]	For Single Device	For All Device		
					Same Data	Different Data	
0	0	0x00	0x002 to 0x0A0	-	-	-	X
		0x01 to 0x10		O	-	-	O
		0x11 to 0x3F		-	-	-	X
	1	0x00	Not sending this data	-	-	-	X
		0x01 to 0x10		O	-	-	O
				O	-	-	O
		0x11 to 0x3F		-	-	-	X
1	0 / 1	0x00	0x002 to 0x0A0	-	-	-	X
		0x01 to 0x3E		-	-	-	X
		0x3F		-	-	-	X

(Note 1) X: This setting is not acceptable. Do not set this condition.

5 SPI Protocol – continued

5.3 Register Address

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RW	0						RegAddr[8:0]								

Bit	Parameter	Value
RW	Read/Write	RW = 0: Write the registers RW = 1: Read the registers
RegAddr[8:0]	Register Address	0x000 to 0x09F

5.4 Data

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data[15:0]															

Bit	Parameter	Value
Data[15:0]	Data	0x0000 to 0xFFFF

5 SPI Protocol – continued

5.5 Single Device, 1 Address Write (Write to Device #1)

B =	0:	Target device receives the data
S =	1:	Single
DevAddr[5:0] =	0x01:	Target device address
NumOfData[8:0] =	-:	1 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 bytes.

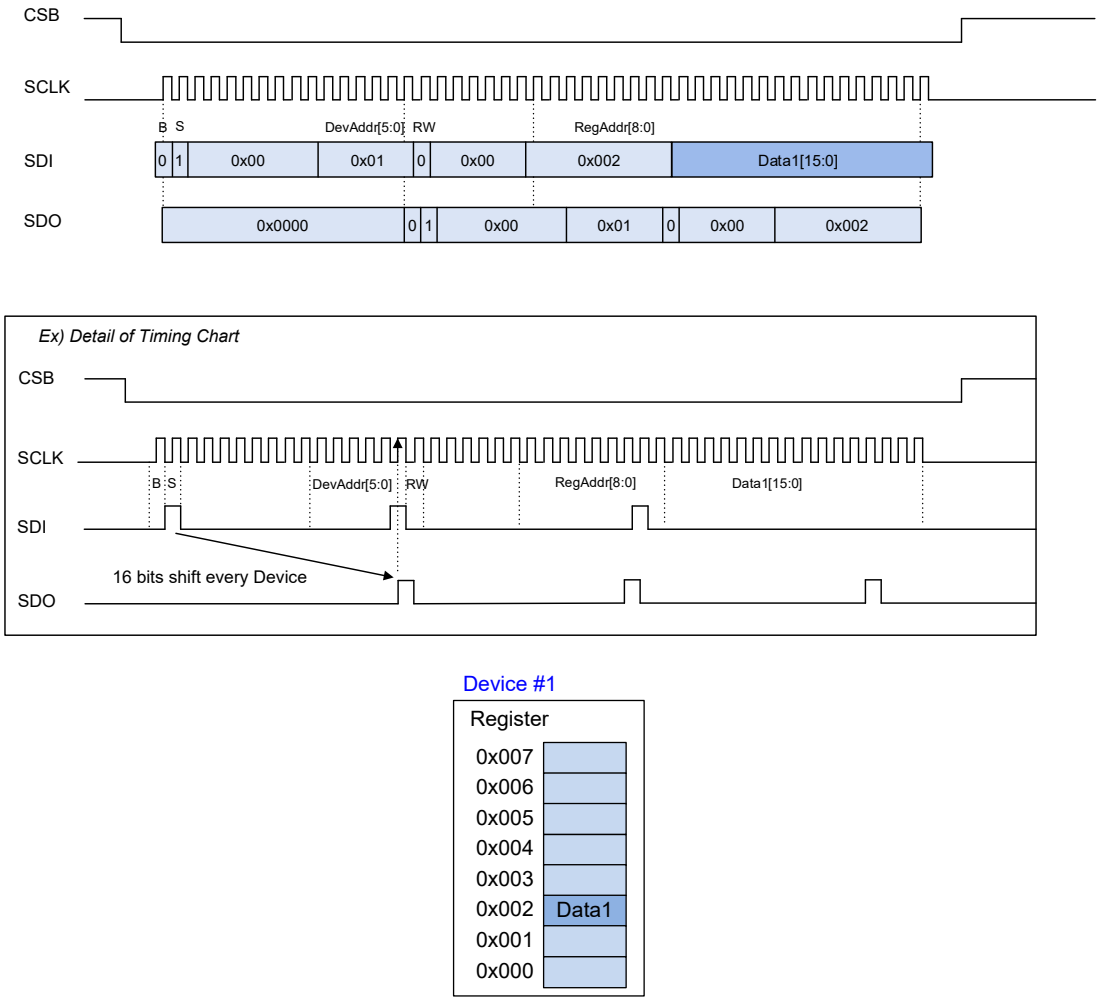


Figure 23. SPI Protocol for 1 Address Write to Device #1

5 SPI Protocol – continued

5.6 Single Device, 1 Address Write (Write to Device #3)

B =	0:	Target device receives the data
S =	1:	Single
DevAddr[5:0] =	0x03:	Target device address
NumOfData[8:0] =	-:	1 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

DevAddr[5:0] of each device is calculated by counting the number of bytes of 0x0000 data after the falling edge of CSB.
DevAddr[5:0] = (Number of byte of 0x0000 data) + 1

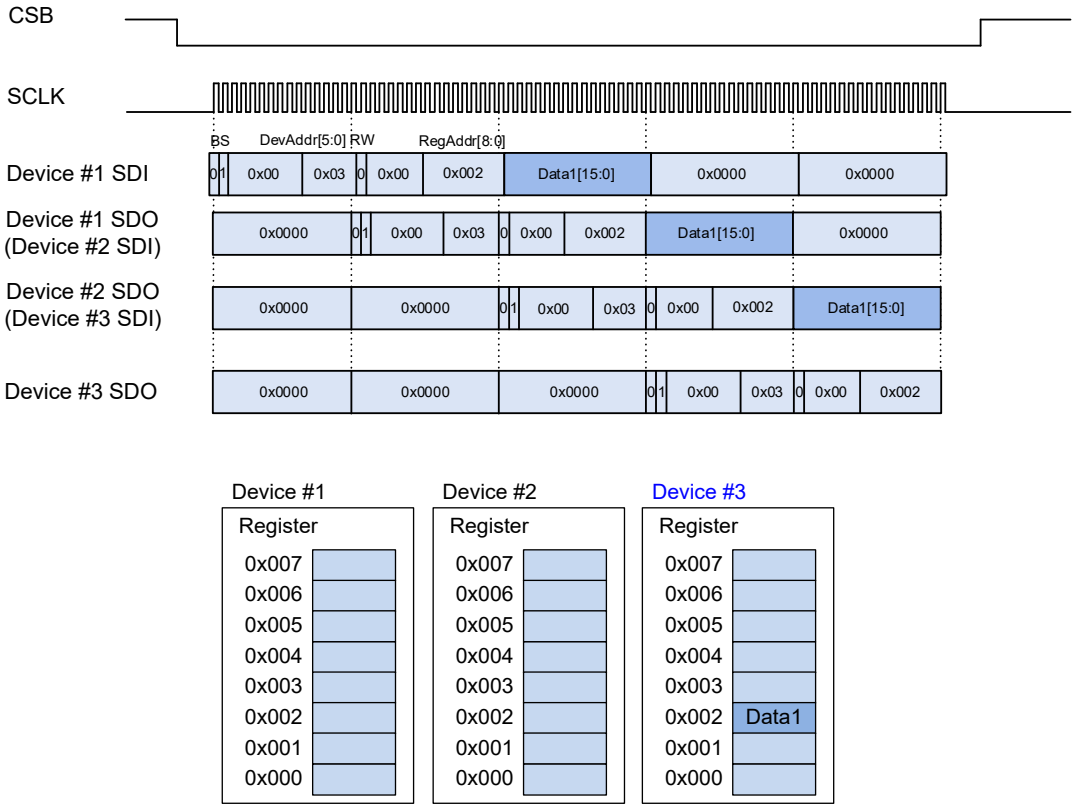


Figure 24. SPI Protocol for 1 Address Write to Device #3

5 SPI Protocol – continued

5.7 Single Device, N Address Write (Write to the consecutive register of Device #1)

B =	0:	Target device receives the data
S =	0:	Multi
DevAddr[5:0] =	0x01:	Target device address
NumOfData[8:0] =	0x003:	3 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

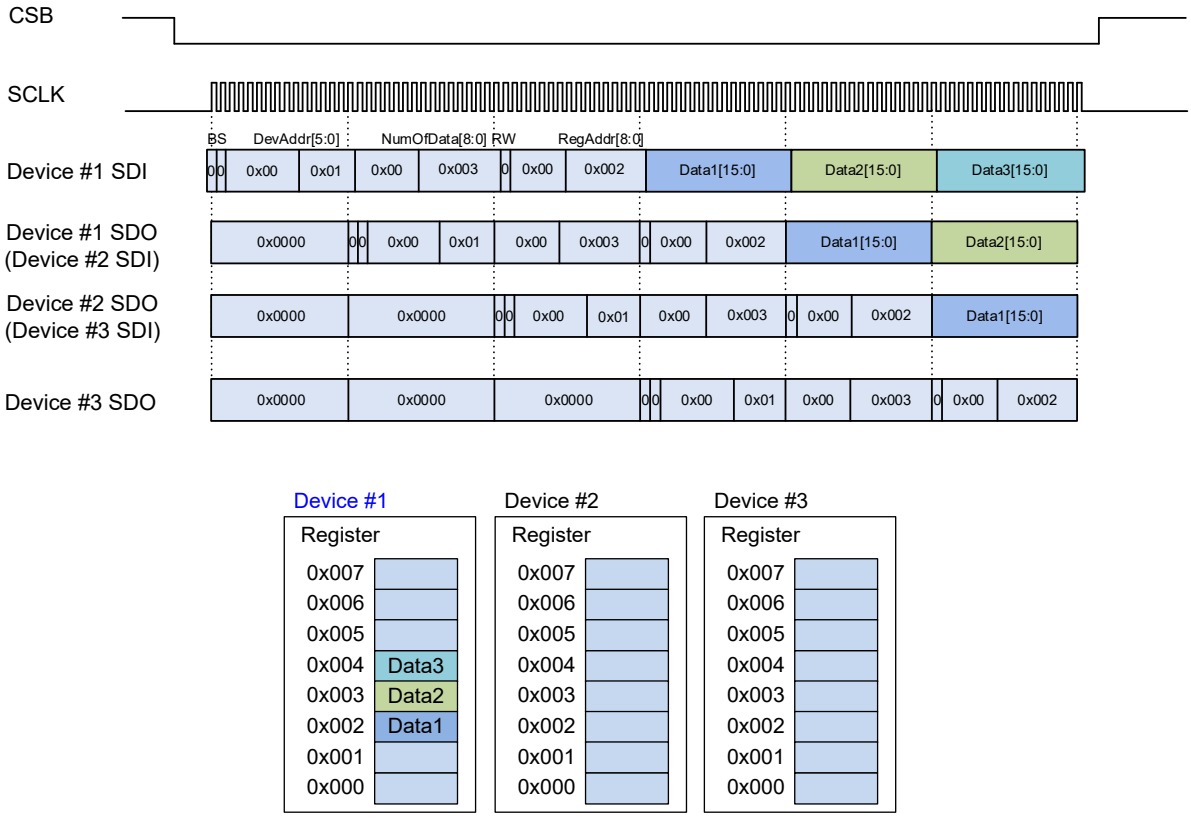


Figure 25. SPI Protocol for N Address Write to Device #1

5 SPI Protocol – continued

5.8 All Devices, Same 1 Address Write (Write the different 2 byte data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	1:	Single
DevAddr[5:0] =	0x3F:	All devices receive different data
NumOfData[8:0] =	-:	1 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

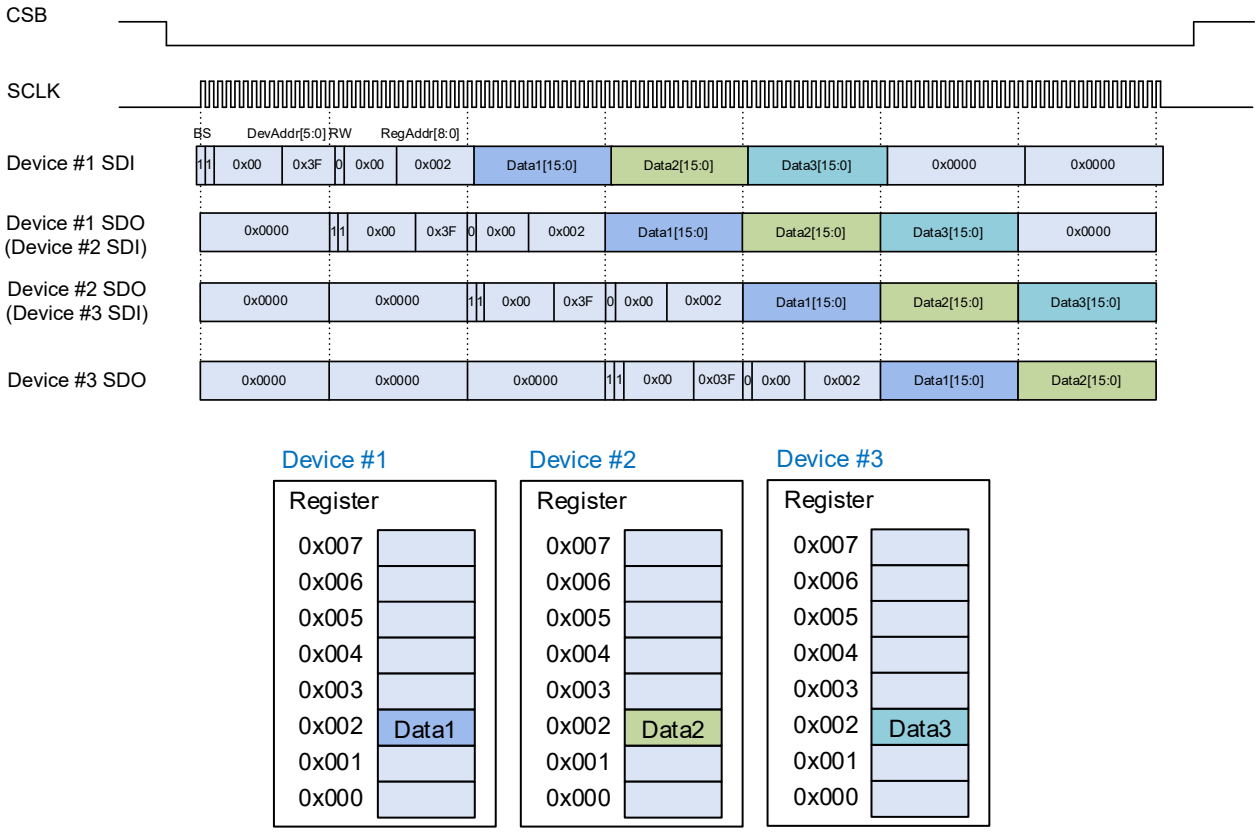


Figure 26. SPI Protocol for 1 Address Different Data Write to All Devices

5 SPI Protocol – continued

5.9 All Devices, Same 1 Address Write (Write the same 2 byte data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	1:	Single
DevAddr[5:0] =	0x00:	All devices receive the same data
RW =	0:	Write
NumOfData[8:0] =	-:	1 address access
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

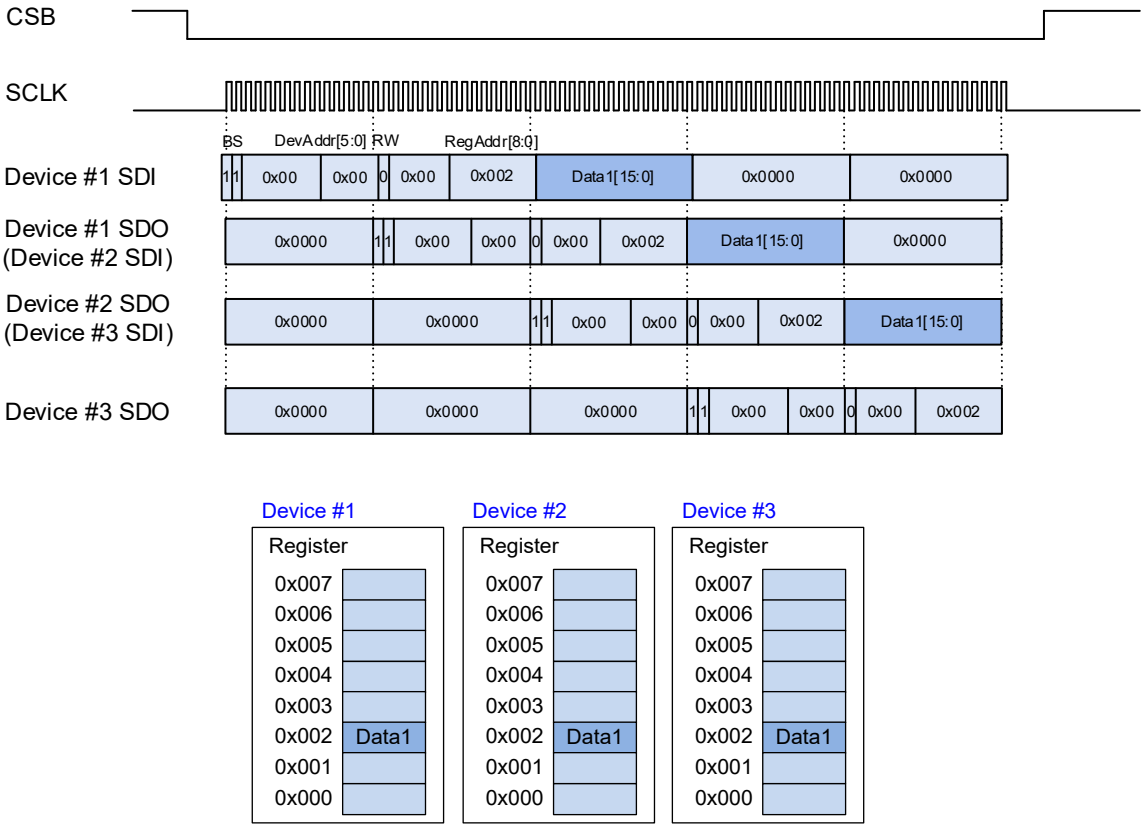


Figure 27. SPI Protocol for 1 Address Same Data Write to All Devices

5 SPI Protocol – continued

5.10 All Devices, Same N Address Write (Write the different N x 2 byte data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	0:	Multi
DevAddr[5:0] =	0x3F:	All devices receive different data
NumOfData[8:0] =	0x002:	2 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

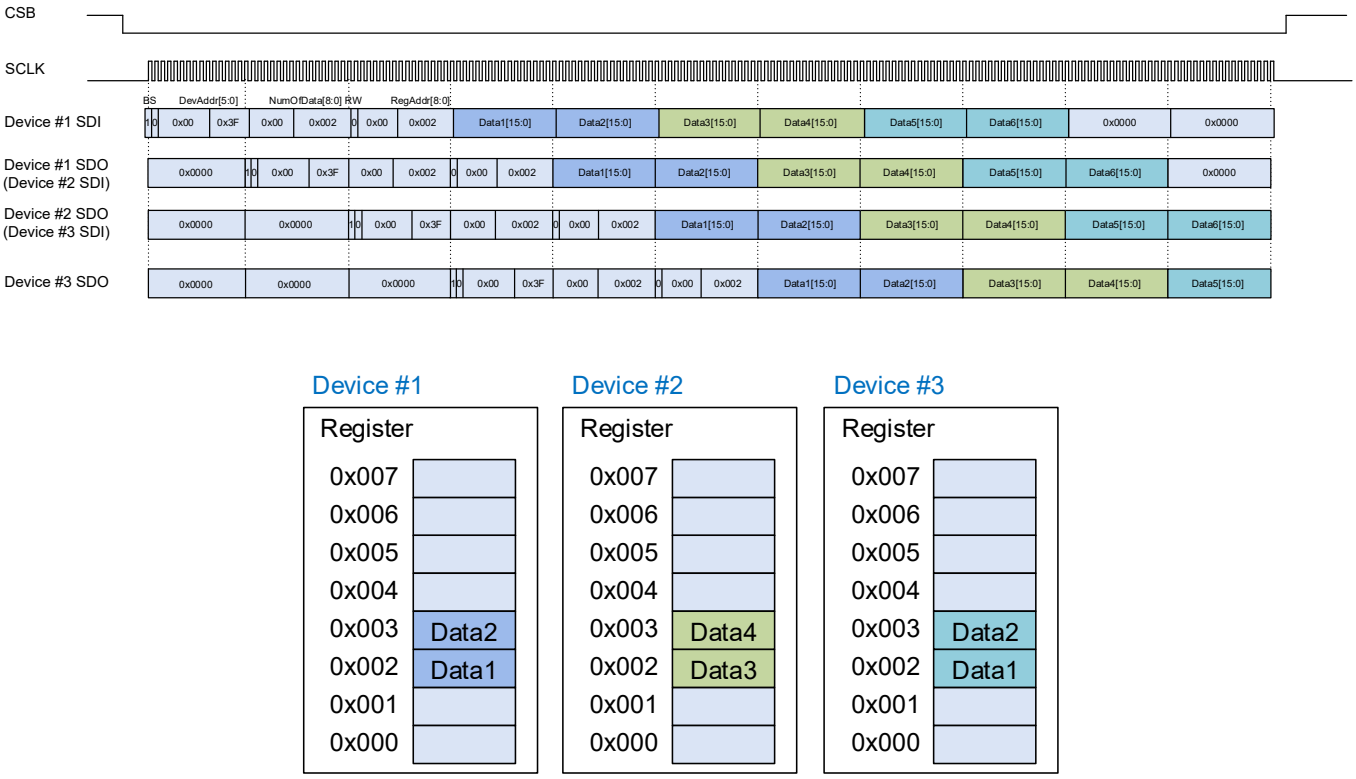


Figure 28. SPI Protocol for N Address Different Data Write to All Devices

5 SPI Protocol – continued

5.11 All Devices, Same N Address Write (Write the same N x 2 byte data to the same RegAddr[8:0] of all devices)

B =	1:	All devices receive data
S =	0:	Multi
DevAddr[5:0] =	0x00:	All devices receive the same data
NumOfData[8:0] =	0x003:	3 address access
RW =	0:	Write
RegAddr[8:0] =	0x002:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], RegAddr[8:0], and Data[15:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

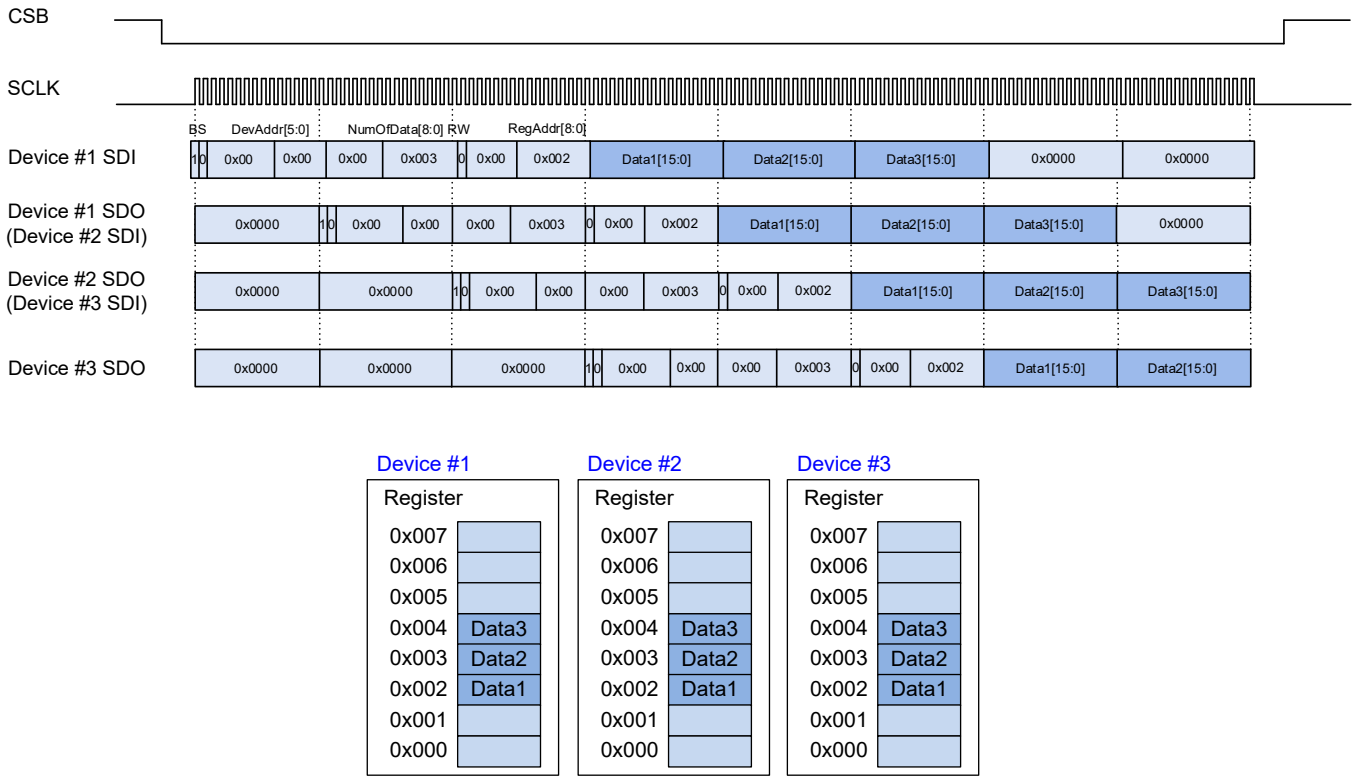


Figure 29. SPI Protocol for N Address Same Data Write to All Devices

5 SPI Protocol – continued

5.12 Single Device, 1 Address Read (Read the 2 byte data from Device #2)

B =	0:	Target device receive the data
S =	1:	Single
DevAddr[5:0] =	0x02:	Target device address
NumOfData[8:0] =	-:	1 address access
RW =	1:	Read
RegAddr[8:0] =	0x003:	Address

SDI: Transfer in the order of DevAddr[5:0] and RegAddr[8:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

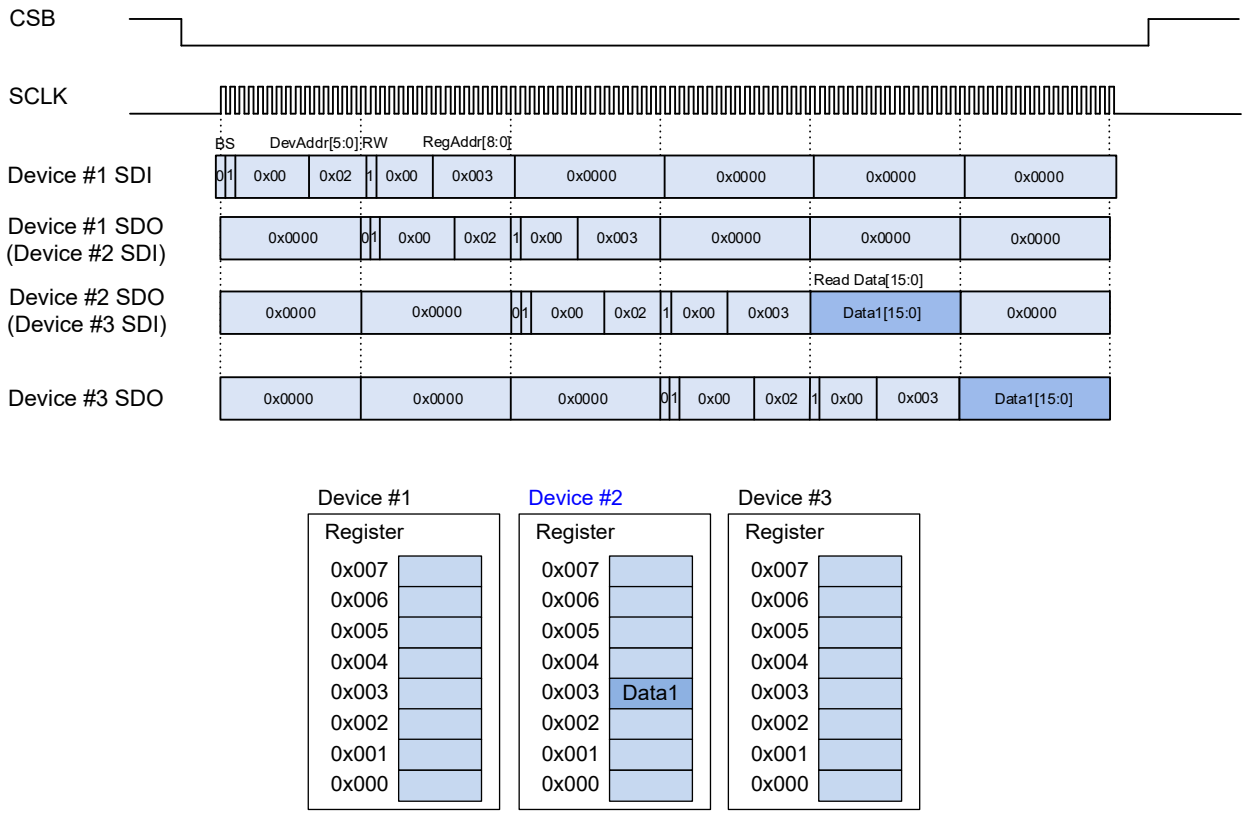


Figure 30. SPI Protocol for 1 Address Read from Device #2

5 SPI Protocol – continued

5.13 Single Device, N Address Read (Read the N x 2 byte data from Device #2)

B =	0:	Target device receives the data
S =	0:	Multi
DevAddr[5:0] =	0x02:	Target device address
NumOfData[8:0] =	0x002:	2 address access
RW =	1:	Read
RegAddr[8:0] =	0x003:	Address

SDI: Transfer in the order of DevAddr[5:0], NumOfData[8:0], and RegAddr[8:0].
SDO: Output the transferred data to the next device after SDI input by 2 byte.

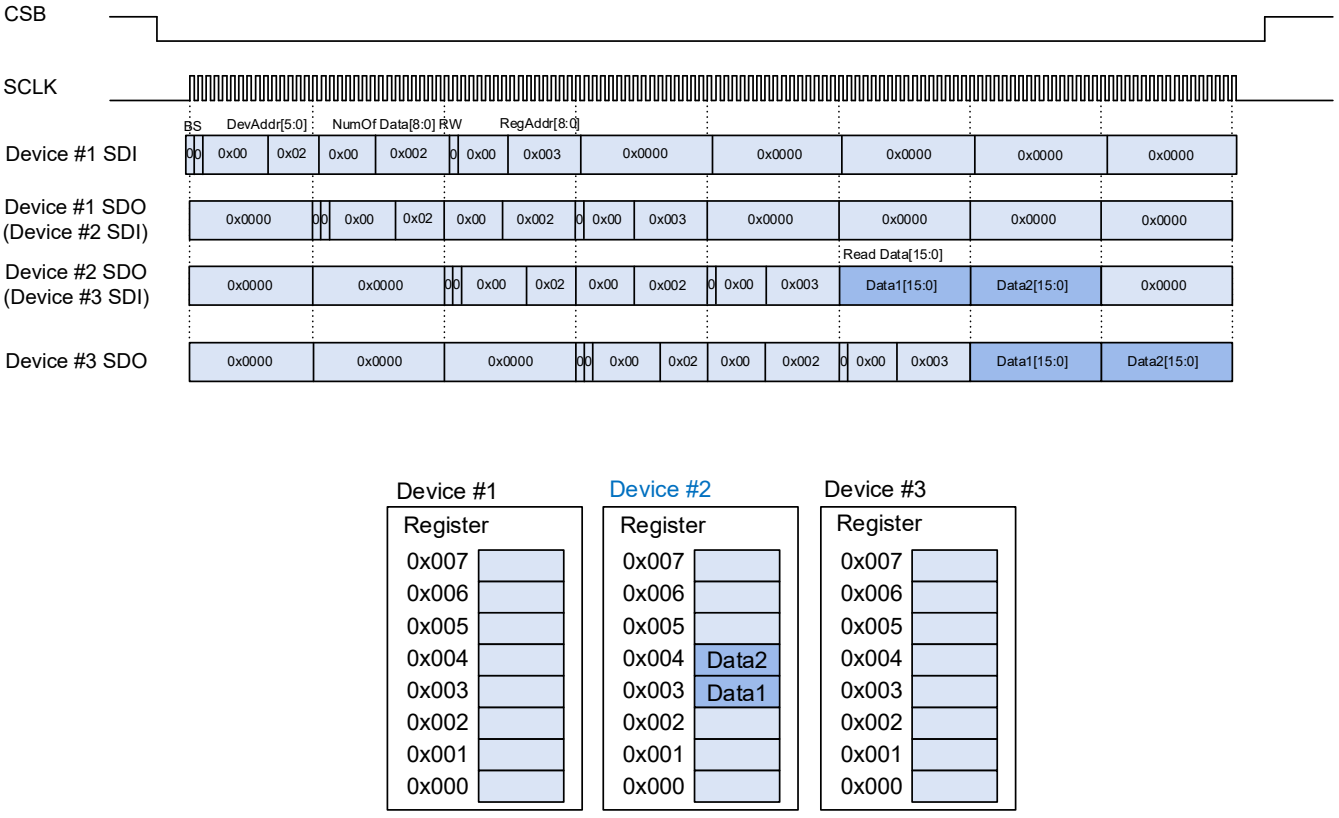


Figure 31. SPI Protocol for N Address Read from Device #2

5 SPI Protocol – continued

5.14 Example (Write the data to N Devices)

Example of byte transfer for the duty setting of N devices in Cascade Connection.

Table 3. Byte Transfer

Transfer setting	B, S, DevAddr[5:0]	2 byte
	RW, NumOfData[8:0]	2 byte
	RegAddr[8:0]	2 byte
Data	Data for the duty setting	(2 byte x 64 channel) x N device = 128 x N byte
Dummy byte	for multi device transfer	2 x (N-1) byte
SUM		4 + 130 x N byte

The details of when N is 2 are described below.

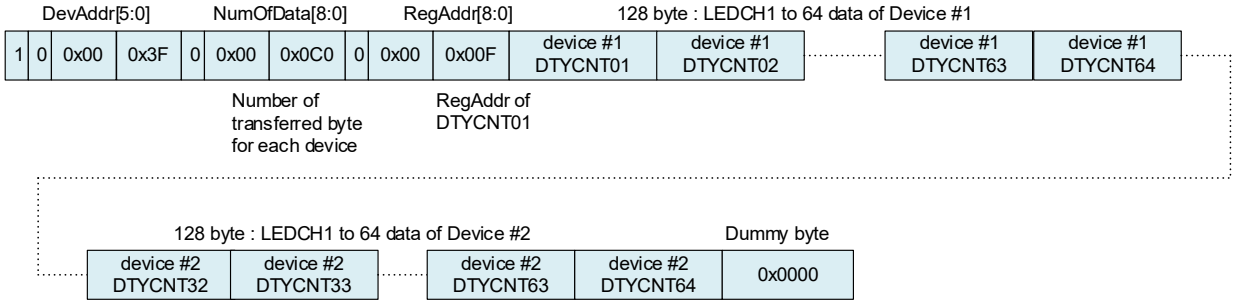


Figure 32. Transfer Byte Number for Multi Access

Functions of Logic Block – continued

6 Register Map

Address	Register Name	Description	Section
0x000	SRSST	Software reset and Soft Start time	Here
0x001	TURNONWAIT	Wait time after turning on	Here
0x002	SSMASK	Soft Start mask time	Here
0x003	ERRMASK	Error output mask time	Here
0x006	SYSCONFIG1	System config 1	Here
0x007	SYSCONFIG2	System config 2	Here
0x008	SYSCONFIG3	System config 3	Here
0x009	LEDEN1601	Enable of LED1 to LED16	Here
0x00A	LEDEN3217	Enable of LED17 to LED32	Here
0x00B	LEDEN4833	Enable of LED33 to LED48	Here
0x00C	LEDEN6449	Enable of LED49 to LED64	Here
0x00D	IREF	Global DC Dimming	Here
0x00F	DTYCNT01	PWM duty setting of LED1	Here
0x010 to 0x04E	DTYCNT02 to DTYCNT64	PWM duty setting of LED2 to PWM duty setting of LED64	Here
0x04F	DLY01	Delay setting of LED1	Here
0x050 to 0x08E	DLY02 to DLY64	Delay setting of LED2 to Delay setting of LED64	Here
0x08F	ERLSH1601	Error status of LED1 to LED16 short detection	Here
0x090	ERLSH3217	Error status of LED17 to LED32 short detection	Here
0x091	ERLSH4833	Error status of LED33 to LED48 short detection	Here
0x092	ERLSH6449	Error status of LED49 to LED64 short detection	Here
0x093	ERLOP1601	Error status of LED1 to LED16 open detection	Here
0x094	ERLOP3217	Error status of LED17 to LED32 open detection	Here
0x095	ERLOP4833	Error status of LED33 to LED48 open detection	Here
0x096	ERLOP6449	Error status of LED49 to LED64 open detection	Here
0x097	ERLSCP1601	Error status of LED1 to LED16 SCP detection	Here
0x098	ERLSCP3217	Error status of LED17 to LED32 SCP detection	Here
0x099	ERLSCP4833	Error status of LED33 to LED48 SCP detection	Here
0x09A	ERLSCP6449	Error status of LED49 to LED64 SCP detection	Here
0x09F	EROTHER	Other error status	Here

As for the register update timing, there are 3 kinds of timing.
For more information on the above, see page 21.

Functions of Logic Block – continued

7 Description of Registers

The writing register annotated “-” is not valid.

Address 0x000: SRSST

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	SSEN	SSTIM[2:0]			-	-	-	SWRST
Initial value	0	0	1	1	0	0	0	0

[Read/Write] Initial value: 0x0030 Update: Immediately

The register data is updated immediately when the new data is written. SWRST is Write-only register.
This register firstly should be set.

Bit[7] SSEN

This register enables/disables Soft Start function.
When SSEN = 1 is updated, IC (FB pin sink current) starts to operate.

Table 4. Enable Setting for Soft Start

SSEN	Enable Setting
0	Soft Start is not available
1	Soft Start is available

Bit[6:4] SSTIM

SSTIM[2:0] is the register for setting the Soft Start time. It sets how the FBDAC[7:0] code changes with HSYNC.
The Initial setting of SSTIM register is 3, so the FB pin sink current is changed every 1024 counts by HSYNC.

Table 5. Soft Start Time / 1 Count

SSTIM[2:0]	Count Up Time
0	@128 HSYNC
1	@256 HSYNC
2	@512 HSYNC
3	@1024 HSYNC
4	@2048 HSYNC
5	@4096 HSYNC
6	@6144 HSYNC
7	@8192 HSYNC

Bit[0] SWRST

This register can reset other registers.
This register is available when HSYNC is input.
SPI is not available for 1.5 ms after SWRST = 1 is written.

Table 6. Software Reset

SWRST	Software Reset
0	Normal
1	Reset (return to “0” automatically)

7 Description of Registers – continued

Address 0x001: TURNONWAIT

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	TURNONWAIT[7:0]							
Initial value	0	0	0	0	0	1	0	0

[Read/Write] Initial value: 0x0004 Update: VSYNC

The register data is updated at the next VSYNC falling edge after the data is written.
This register firstly should be set.

The mask time of PWM output and FB pin sink current is set by counting the number of VSYNC pulses.
This register is updated at the 3rd VSYNC pulse after reset is released (UVLO, SWRST).
If this register needs to be updated, update this register before the 3rd VSYNC pulse.
This register can't be set lower than 0x04.

$$t_{TURNONWAIT} = TURNONWAIT[7:0]/f_{VSYNC} \quad [s]$$ (Except for waiting time until 1st VSYNC pulse)

Table 7. Maximum Turn on Wait Time

f_{VSYNC} [Hz]	60	120	240
Maximum TURNONWAIT Time [ms]	4,250	2,125	1,062.5

7 Description of Registers – continued

Address 0x002: SSMASK

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	SSMASK[7:0]							
Initial value	0	0	1	1	1	1	0	0

[Read/Write] Initial value: 0x003C Update: VSYNC

The register data is updated at the next VSYNC signal rising edge after the data is written. Set the value higher than 0x02. This register firstly should be set.

The mask time of ERROR detection only during start-up is set by counting the number of VSYNC pulses and after VSYNC rising edge including first PWM = High.

$$t_{SSMASK} = (SSMASK[7:0] + 1)/f_{VSYNC} \quad [s]$$

Table 8. Maximum Soft Start Mask Time

f_{VSYNC} [Hz]	60	120	240
Maximum SSMASK Time [ms]	4,267	2,133	1,067

Address 0x003: ERRMASK

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERRMASK[7:0]							
Initial value	0	0	1	0	1	0	0	1

[Read/Write] Initial value: 0x0029 Update: VSYNC

The register data is updated at the next VSYNC signal rising edge up after the data is written.

Range: 0x03 or more (Set for 0x00 to 0x02 also lead to 0x03, register value = writing value)
ERROR mask time is set by counting the number of HSYNC pulses.

$$t_{ERRMASK} = ERRMASK[7:0]/f_{HSYNC} \quad [s]$$

This register is effective for LOP, LSH and LSCP.
If the capacitor of the LEDn pin C_{LED} is connected, the transient response is affected.
Set the value considering the time margin of LOP, LSH and LSCP.
(For example, in the case of LOP) If ERRMASK = 3, the error signal is masked by 3 HSYNC cycles.
ERRMASK counter resets when the detection conditions for each protection function are not met.
The ERRMASK time can be expressed in relation to the HSYNC frequency.

Table 9. Maximum Error Mask Time

f_{HSYNC} [Hz]	3,932,160	7,864,320	15,728,640
Maximum ERRMASK Time [µs]	64.8	32.4	16.2

7 Description of Registers – continued

Address 0x006: SYSCONFIG1

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	PWMFREQ[1:0]		-	FBREF[2:0]			PRCEN	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	LSCPEN	-	-	LOPEN	LSHEN	LEDSH[1:0]	
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the new data is written.
This register should be set before PWM dimming. Do not change this register value during dimming.

Bit[15:14] PWMFREQ (Update this register until the 4th VSYNC pulse from RESET release.)
The register PWMFREQ defines the number of times PWM turns on during a VSYNC pulse. So, the proper HSYNC pulse number is almost proportional to the PWMFREQ.

$$f_{HSYNC} = f_{VSYNC} \times 65535 \times 2^{(PWMFREQ[1:0])} \quad \text{[Hz]}$$

The example of HSYNC pulse number is shown as VSYNC is 60 Hz, 120 Hz, 240 Hz, 480 Hz.
The maximum HSYNC frequency is 20 MHz. (Refer to frequency range of electric characteristics)

Table 10. HSYNC Frequency and PWM Frequency (Example)*(Note 1)*

PWMFREQ [1:0]	VSYNC Frequency [Hz]			
	60	120	240	480
0	60	120	240	480
	3,932,100	7,864,200	15,728,400	-
1	120	240	480	960
	7,864,200	15,728,400	-	-
2	240	480	960	1,920
	15,728,400	-	-	-

(Note 1) "-" is not acceptable to set this value in PWMFREQ register

Bit[12:10] FBREF
Feedback reference voltage of FB control block.

Table 11. Reference of FB Control Block

FBREF[2:0]	Feedback Reference Voltage
0x0	0.45 V
0x1	0.50 V
0x2	0.55 V
0x3	0.60 V
0x4	0.65 V
0x5	0.70 V
0x6	0.75 V
0x7	0.80 V

Bit[9] PRCEN
This register enables/disables LED Pull-up Current. It is highly recommended that PRCEN is set to 1.

Table 12. Enable Setting for LED Pull-up Current

PRCEN	Enable Setting
0	LED Pull-up Current is not available
1	LED Pull-up Current during PWMn = Low is available

Address 0x006: SYSCONFIG1 – continued

Bit[6] LSCPEN
This register enables/disables LED SCP Error detection.

Table 13. Enable Setting for LED SCP Error Detection

LSCPEN	Enable Setting
0	LED SCP Error detection is not available
1	LED SCP Error detection is available

Bit[3] LOPEN
This register enables/disables LED Open Error detection.

Table 14. Enable Setting for LED Open Error Detection

LOPEN	Enable Setting
0	LED Open Error detection is not available
1	LED Open Error detection is available

Bit[2] LSHEN
This register enables/disables LED Short Error detection.

Table 15. Enable Setting for LED Short Error Detection

LSHEN	Enable Setting
0	LED Short Error detection is not available
1	LED Short Error detection is available

Bit[1:0] LEDSH
This register controls the detection voltage for LED Short Error.

Table 16. LED Short Error Detection Voltage Setting

LEDSH[1:0]	Detection Voltage [V]
0	1.3 V
1	2.6 V
2	3.9 V
3	5.2 V

7 Description of Registers – continued

Address 0x007: SYSCONFIG2

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	FBHOLD	SMPTIM[2:0]			SUMFBL	VINSW OVPEN	VINSWOVPREF[1:0]	
Initial value	0	0	1	1	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	SMPTIM AFMONI	FAILB TEST	FAILB CNT	ISET OPENEN	AUTOCLR	AUTOOFF	ERRCLR	ERRLAT
Initial value	0	0	0	1	0	0	0	0

[Read/Write] Initial value: 0x3010 Update: Immediately

The register data is updated immediately when the new data is written.
This register should be set before PWM dimming except FBHOLD. Do not change this register value during dimming except FBHOLD.

The data in registers (ERRLAT) are updated at the next VSYNC signal rising edge after the data is written.
AUTOCLR and ERRCLR are Write-only registers.

Bit[15] FBHOLD

This register enables/disables to keep FB pin sink current setting.

Table 17. FBHOLD Condition

FBHOLD	Enable Setting
0	FB pin sink current DAC controlled by LEDn pin voltage
1	FB pin sink current DAC keeps

When FBHOLD = 0, FB pin sink current DAC is controlled by LEDn pin voltage.
When FBHOLD = 1, FB pin sink current DAC is kept with its previous setting and LEDn pin voltage is ignored.

Address 0x007: SYSCONFIG2 – continued

Bit[14:12] SMPTIM

This register determines the sampling timing of the LEDn pin voltage. The LEDn pin voltage is sampled at the timing of counting the number of HSYNC pulses set in this register. The FB sink current is adjusted according to the LED pin voltages. The sampling timing must be set within PWM Duty. Otherwise, it will not be sampled, and the FB sink current will decrease.

$$5 \times 10^{-7} \leq 1/f_{HSYNC} \times SMPTIM[2:0] \leq 1/f_{HSYNC} \times DTYCNTn[15:0] \quad [s]$$

Table 18. Sampling Time

SMPTIM[2:0]	LED Channel Voltage Sampling Time
0x0	1 HSYNC
0x1	2 HSYNC
0x2	4 HSYNC
0x3	8 HSYNC
0x4	16 HSYNC
0x5	32 HSYNC
0x6	64 HSYNC
0x7	128 HSYNC

Good case

SMPTIM = 0x4

DTYCNTn = 0x0015 (21 HSYNC)

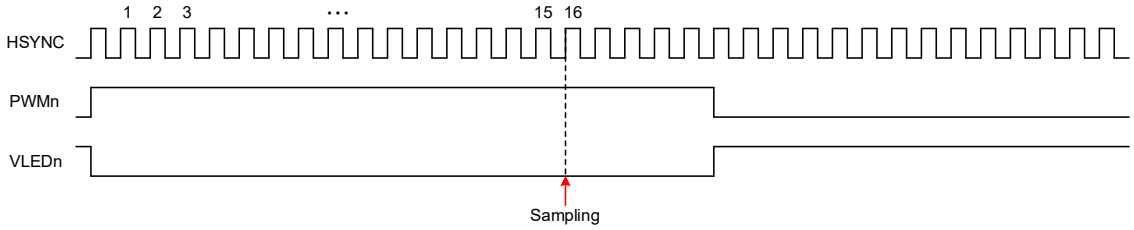


Figure 33. Appropriate Sampling Timing

Bad case

SMPTIM = 0x5

DTYCNTn = 0x0015 (21 HSYNC)

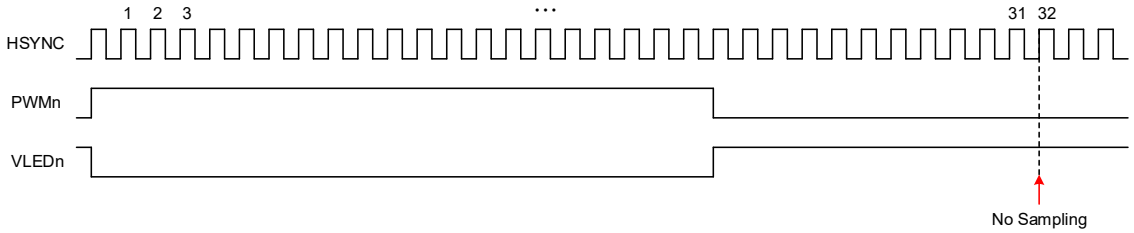


Figure 34. Inappropriate Sampling Timing

Bit[11] SUMFBL

This register enables/disables that SUMFB pin is forced Low.

Table 19. Enable Setting for SUMFBL

SUMFBL	Enable Setting
0	Normal status
1	SUMFB is forced Low

When SUMFBL = 0, SUMFB pin voltage is High when all LEDn pin voltages are above feedback reference voltage. SUMFB pin voltage is Low when at least one of LEDn pin voltage is below feedback reference voltage. When SUMFBL = 1, SUMFB pin voltage is Low.

Address 0x007: SYSCONFIG2 – continued

Bit[10] VINSWOVPEN
This register enables/disables over voltage detection of the VINSW pin.

Table 20. Enable Setting for Over Voltage Detection of the VINSW Pin

VINSWOVPEN	Enable Setting
0	VINSW Over Voltage detection is not available
1	VINSW Over Voltage detection is available

Bit[9:8] VINSWOVPREF
Detection voltage for over voltage of the VINSW pin.

Table 21. Detection Voltage Setting of the VINSW Pin

VINSWOVPREF[1:0]	Detection Voltage [V]
0	6.0 V
1	7.0 V
2	8.0 V
3	9.0 V

Bit[7] SMPTIMAFMONI
This register enables/disables to change sampling timing.

Table 22. Enable Setting for SMPTIMAFMONI

SMPTIMAFMONI	Enable Setting
0	Sampling is performed at the timing set by SMPTIM[2:0]
1	Sampling is performed after the timing set by SMPTIM[2:0] until PWMn goes Low. Sampling is performed at every rising edge of HSYNC in the above interval.

When SMPTIMAFMONI = 0, the LEDn pin voltage is sampled at the timing set by SMPTIM[2:0], and the FB sink current is adjusted according to the LED pin voltages.
When SMPTIMAFMONI = 1, the LEDn pin voltage is sampled every HSYNC during PWMn is High after the timing set by the SMPTIM[2:0].

SMPTIMAFMONI = 0
SMPTIM = 0x4
DTYCNTn = 0x0015 (21 HSYNC)

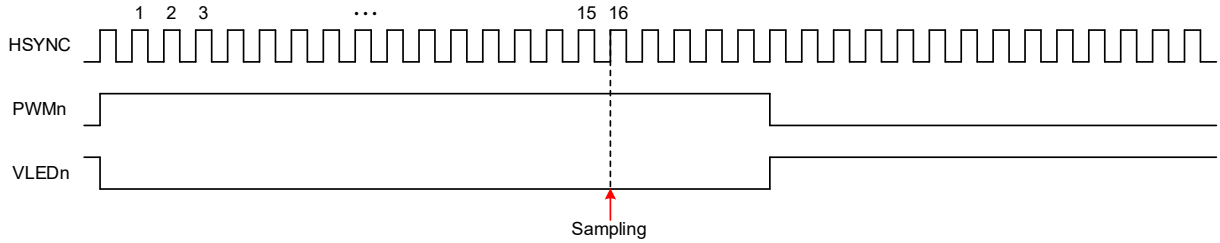


Figure 35. Sampling Timing When SMPTIMAFMONI = 0

SMPTIMAFMONI = 1
SMPTIM = 0x4
DTYCNTn = 0x0015 (21 HSYNC)

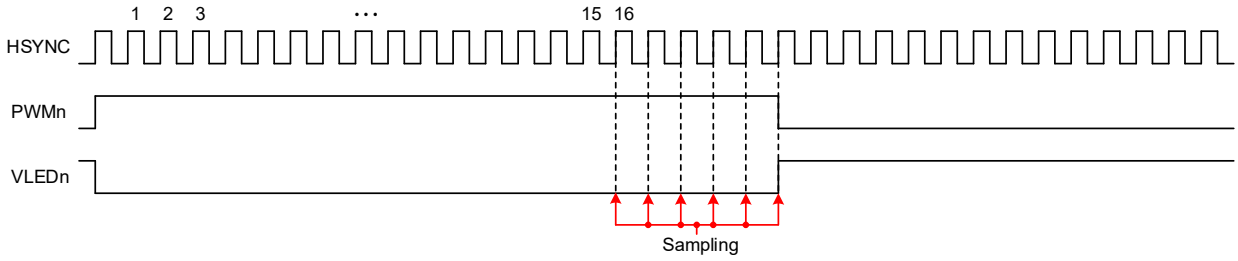


Figure 36. Sampling Timing When SMPTIMAFMONI = 1

Address 0x007: SYSCONFIG2 – continued

Bit[6] FAILBTEST
This register enables/disables the FAILB pin output by the FAILBCNT register.

Table 23. Enable Setting for FAILBTEST

FAILBTEST	Enable Setting
0	Normal operation
1	FAILB controlled by FAILBCNT is available

Bit[5] FAILBCNT
This register enables/disables FAILB output voltage when FAILBTEST = 1.

Table 24. Enable Setting for FAILBCNT

FAILBCNT	Enable Setting
0	The FAILB pin output Low when FAILBTEST = 1
1	The FAILB pin output High when FAILBTEST = 1

Bit[4] ISETOPENEN
This register enables/disables ISET Open Error detection.

Table 25. Enable Setting for ISET Open Error Detection

ISETOPENEN	Enable Setting
0	ISET Open Error detection is not available
1	ISET Open Error detection is available

Bit[3] AUTOCLR
AUTOCLR is available in AUTOOFF = 1 setting.

Table 26. AUTOOFF Condition

AUTOCLR	AUTOOFF Condition
0	No Operation
1	AUTOOFF condition in LEDn output is released (return to “0” automatically)

Bit[2] AUTOOFF
Control ON/OFF condition in LEDn output. AUTOOFF condition is latched until released by UVLO or AUTOCLR.

Table 27. ON/OFF Condition of LEDn Output

AUTOOFF	ON/OFF Condition
0	LEDn does not turn OFF automatically after error is detected
1	LEDn turns OFF automatically after error is detected

Bit[1] ERRCLR
This register enables/disables to clear errors in error registers.

Table 28. Clear Error Register

ERRCLR	Clear Error Register
0	No Operation
1	Clear error in error register (returns to “0” automatically)

Bit[0] ERRLAT
Control error register and FAILB output when error is detected.

Table 29. Error Detection Function

ERRLAT	Error Detection Function
0	Error register and FAILB output return to initial condition when error is released
1	Error register and FAILB output are retained until ERRCLR = 1 is written

7 Description of Registers – continued

Address 0x008: SYSCONFIG3

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	DACUP[2:0]			DACDN[1:0]		-	MSMODE
Initial value	0	0	0	1	0	0	0	0

[Read/Write] Initial value: 0x0010 Update: Immediately

The register data is updated immediately when the new data is written.
This register firstly should be set.

Bit[6:4] DACUP
DACUP is register for setting the FBDAC's count up step after Soft Start.

Table 30. FBDAC Code Count Up Step

DACUP[2:0]	FBDAC Code Count Up Step
0	+1
1	+2
2	+3
3	+4
4	+5
5	+6
6	+7
7	+8

Bit[3:2] DACDN
DACDN is register for setting the FBDAC's count down step after Soft Start.

Table 31. FBDAC Code Count Down Step

DACDN[1:0]	FBDAC Code Count Down Step
0	-1
1	-2
2	-3
3	-4

Bit[0] MSMODE
MSMODE is register for setting of FBDAC’s main mode or sub mode.

Table 32. FBDAC Mode Setting

MSMODE	FBDAC Mode Setting
0	Main mode (DC/DC feedback device)
1	Sub mode (No DC/DC feedback device)

7 Description of Registers – continued

Address 0x009: LEDEN1601

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	LEDEN[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: Immediately

Address 0x00A: LEDEN3217

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	LEDEN[31:24]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: Immediately

Address 0x00B: LEDEN4833

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	LEDEN[47:40]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[39:32]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: Immediately

Address 0x00C: LEDEN6449

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	LEDEN[63:56]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	LEDEN[55:48]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the new data is written.

These registers (from 0x009 to 0x00C) enable or disable each LEDn. If “0” is set in LEDEN[n-1], LEDn current is turned off.

Table 33. LEDn Enable Setting

LEDEN[n-1]	LEDn Current Control
0	Disable
1	Enable

7 Description of Registers – continued

Address 0x00D: IREF

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	-	-	IREF[5:0]					
Initial value	0	0	1	1	1	1	1	1

[Read/Write] Initial value: 0x003F Update: Immediately

The register data is updated immediately when the new data is written.

This register is used with Global DC Dimming.
This register can change value during dimming. Evaluate the actual operation sufficiently to change this register during feedback using DC/DC because unstable operation such as flickering may occur.

Table 34. IREF Setting

IREF[5:0]	LEDn Current
0x0000	64/127 x I_{LEDMAX}
0x0001	65/127 x I_{LEDMAX}
0x0002	66/127 x I_{LEDMAX}
0x0003	67/127 x I_{LEDMAX}
0x0004	68/127 x I_{LEDMAX}
to	to
0x003D	125/127 x I_{LEDMAX}
0x003E	126/127 x I_{LEDMAX}
0x003F	127/127 x I_{LEDMAX}

I_{LEDMAX} is set by R_{ISET}.

7 Description of Registers – continued

Address 0x00F: DTYCNT01

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	DTYCNT01[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DTYCNT01[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: PWM

The register data is updated at the next PWM signal rising edge after the data is written.

This register is used to set the PWM pulse width for LED1. The PWM minimum pulse width is limited to 0.5 μs or over.

Table 35. PWM Duty Setting

DTYCNT01[15:0]	LED Pulse Width
0x0000	0 clock width@HSYNC
0x0001	1 clock width@HSYNC
0x0002	2 clock width@HSYNC
0x0003	3 clock width@HSYNC
0x0004	4 clock width@HSYNC
to	to
0xFFFC	65,532 clock width@HSYNC
0xFFFD	65,533 clock width@HSYNC
0xFFFE	65,534 clock width@HSYNC
0xFFFF	65,535 clock width@HSYNC

Address 0x010 to 0x04E: DTYCNTn (n = 02 to 64)

These registers are used to set the PWM pulse width for LED2 to LED64. The setting procedure is the same as that for LED1 with Address set to 0x00F. The PWM minimum pulse width is limited to 0.5 μs or over.

7 Description of Registers – continued

Address 0x04F: DLY01

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	DLY01[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	DLY01[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read/Write] Initial value: 0x0000 Update: VSYNC

The register data is updated at the next VSYNC timing after the data is written.

This register is used to set the delay width of PWM for LED1.

Table 36. Delay Setting of PWM Output

DLY01[15:0]	DLY01 Total Clock Number (clock width @HSYNC)
0x0000	Delay 5 to 6 HSYNC from rising edge of VSYNC pulse (*1)
0x0001	(*1) + 1
0x0002	(*1) + 2
0x0003	(*1) + 3
to	to
0xFFFC	(*1) + 65,532
0xFFFD	(*1) + 65,533
0xFFFE	(*1) + 65,534
0xFFFF	(not used)

Address 0x050 to 08E: DLYn (n = 02 to 64)
These registers are used to set the delay width of PWM for LED2 to LED64. The setting procedure is the same as that for LED1 with address set to 0x04F.

7 Description of Registers – continued

Address 0x08F: ERLSH1601

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSH[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x090: ERLSH3217

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSH[31:24]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x091: ERLSH4833

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSH[47:40]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[39:32]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x092: ERLSH6449

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSH[63:56]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSH[55:48]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x08F to 0x092) correspond to the status of LED Short Detection of LED1 to LED64.

Table 37. Status of LED Short Detection

ERLSH[n-1]	Status
0	Normal
1	Detected LED Short Error*(Note 2)*

(Note 2) ERRLAT = 0: ERLSH[n-1] turns 0, if LED Short Error is released or LEDEN[n-1] = 0 is set or LSHEN = 0 is set.
ERRLAT = 1: ERLSH[n-1] turns 0, if ERRCLR = 1 is set.

7 Description of Registers – continued

Address 0x093: ERLOP1601

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLOP[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x094: ERLOP3217

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLOP[31:24]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x095: ERLOP4833

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLOP[47:40]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[39:32]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x096: ERLOP6449

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLOP[63:56]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLOP[55:48]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x093 to 0x096) correspond to the status of LED Open Detection of LED1 to LED64.

Table 38. Status of LED Open Detection

ERLOP[n-1]	Status
0	Normal
1	Detected LED Open Error*(Note 3)*

(Note 3) ERRLAT = 0: ERLOP[n-1] turns 0, if LED Open Error is released or LEDEN[n-1] = 0 is set or LOPEN = 0 is set.
ERRLAT = 1: ERLOP[n-1] turns 0, if ERRCLR = 1 is set.

7 Description of Registers – continued

Address 0x097: ERLSCP1601

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSCP[15:8]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSCP[7:0]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x098: ERLSCP3217

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSCP[31:24]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSCP[23:16]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x099: ERLSCP4833

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSCP[47:40]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSCP[39:32]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

Address 0x09A: ERLSCP6449

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	ERLSCP[63:56]							
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	ERLSCP[55:48]							
Initial value	0	0	0	0	0	0	0	0

[Read] Initial value: 0x0000 Update: Immediately

The register data is updated immediately when the data is written.
These registers (0x097 to 0x09A) correspond to the status of LED SCP Detection of LED1 to LED64.

Table 39. Status of LED SCP Detection

ERLSCP[n-1]	Status
0	Normal
1	Detected LED SCP Error*(Note 4)*

(Note 4) ERRLAT = 0: ERLSCP[n-1] turns 0, if LED SCP Error is released or LSCPEN = 0 is set.
ERRLAT = 1: ERLSCP[n-1] turns 0, if ERRCLR = 1 is set.

7 Description of Registers – continued

Address 0x09F: EROTHER

Bit No.	Bit[15]	Bit[14]	Bit[13]	Bit[12]	Bit[11]	Bit[10]	Bit[9]	Bit[8]
Name	-	-	-	-	-	-	-	-
Initial value	0	0	0	0	0	0	0	0

Bit No.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Name	EROTP	-	-	ERISET OPEN	ERISET OCP	ERTSD UVLO	-	ERVINSW OVP
Initial value	0	0	0	0	0	1	0	0

[Read] Initial value: 0x0004 Update: Immediately

The register data is updated immediately when the new data is written.

Bit[7] EROTP

EROTP register corresponds to the status of OTP.

Table 40. Status of OTP

EROTP	Status
0	Normal
1	Detected OTP Error

Bit[4] ERISETOPEN

ERISETOPEN register corresponds to the status of ISET Open Detection.

Table 41. Status of ISET Open Detection

ERISETOPEN	Status
0	Normal
1	Detected ISET Open Error*(Note 5)*

Bit[3] ERISETOCP

ERISETOCP register corresponds to the status of ISET Over Current Detection.

Table 42. Status of ISET Over Current Detection

ERISETOCP	Status
0	Normal
1	Detected ISET Over Current Error*(Note 5)*

(Note 5) ERRLAT = 0: ERISETOPEN and ERISETOCP turn 0, if error condition is released.
ERRLAT = 1: ERISETOPEN and ERISETOCP turn 0, if ERRCLR = 1 is set.

Address 0x09F: EROTHER – continued

Bit[2] ERTSDUVLO
ERTSDUVLO register corresponds to the status of TSD or UVLO Detection.

Table 43. Status of TSD or UVLO Detection

ERTSDUVLO	Status
0	Normal
1	Detected TSD or UVLO Error*(Note 6)*

Bit[0] ERVINSWOVP
ERVINSWOVP register corresponds to the status of VINSW Over Voltage Detection.

Table 44. Status of VINSW Over Voltage Detection

ERVINSWOVP	Status
0	Normal
1	Detected VINSW Over Voltage Error*(Note 7)*

(Note 6) Initial value is 1, so it is recommended to write ERRCLR = 1 after startup in normal sequence.
(Note 7) ERRLAT = 0: ERVINSWOVP turn 0, if error condition is released.
ERRLAT = 1: ERVINSWOVP turn 0, if ERRCLR = 1 is set.

Application Example

The multiple BD83164MWF-M usage (the common SPI and the common DC/DC)

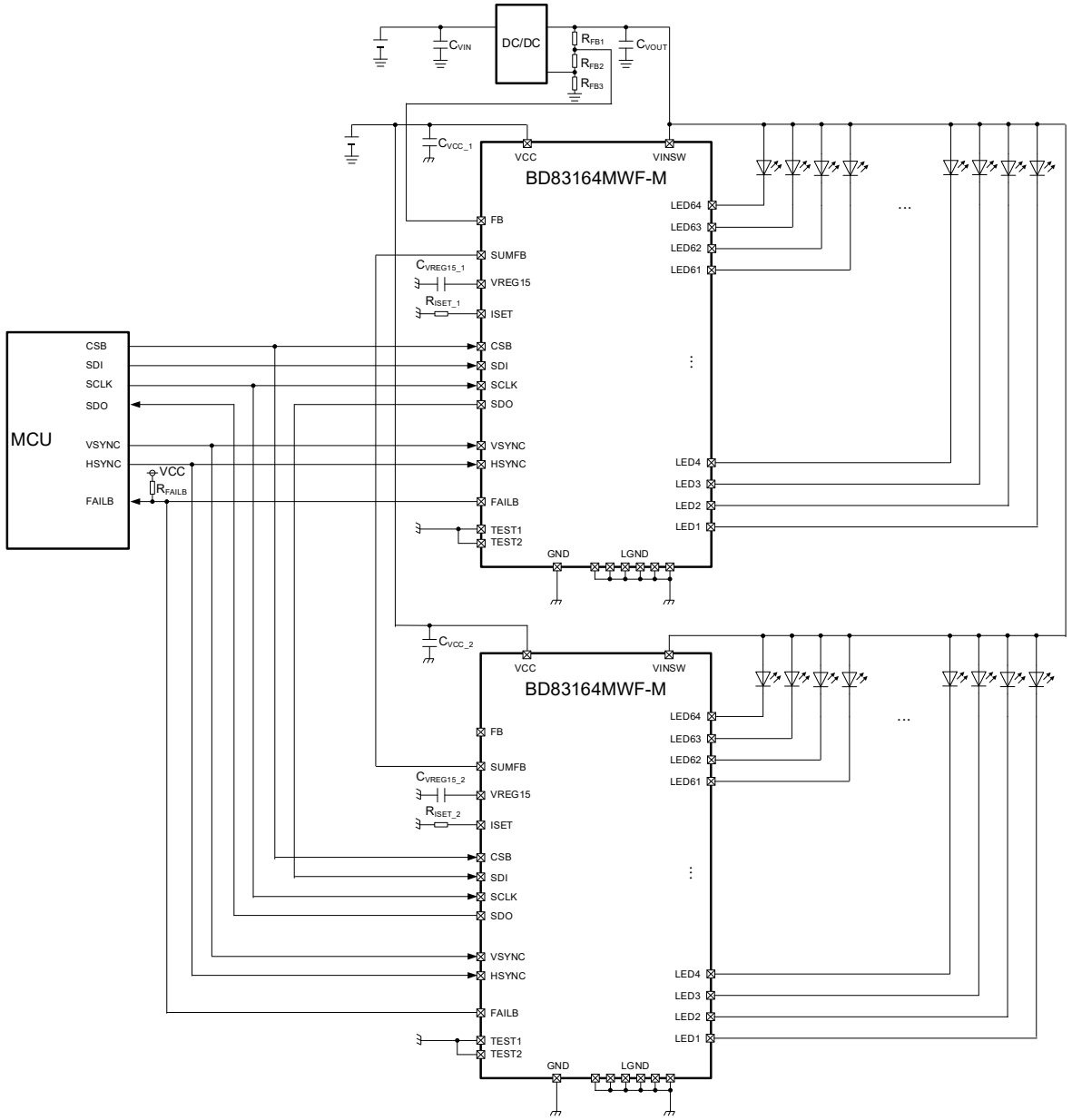


Figure 37. Device Connection Schematic Using DC/DC Converter

Timing Chart

1 Boot Sequence

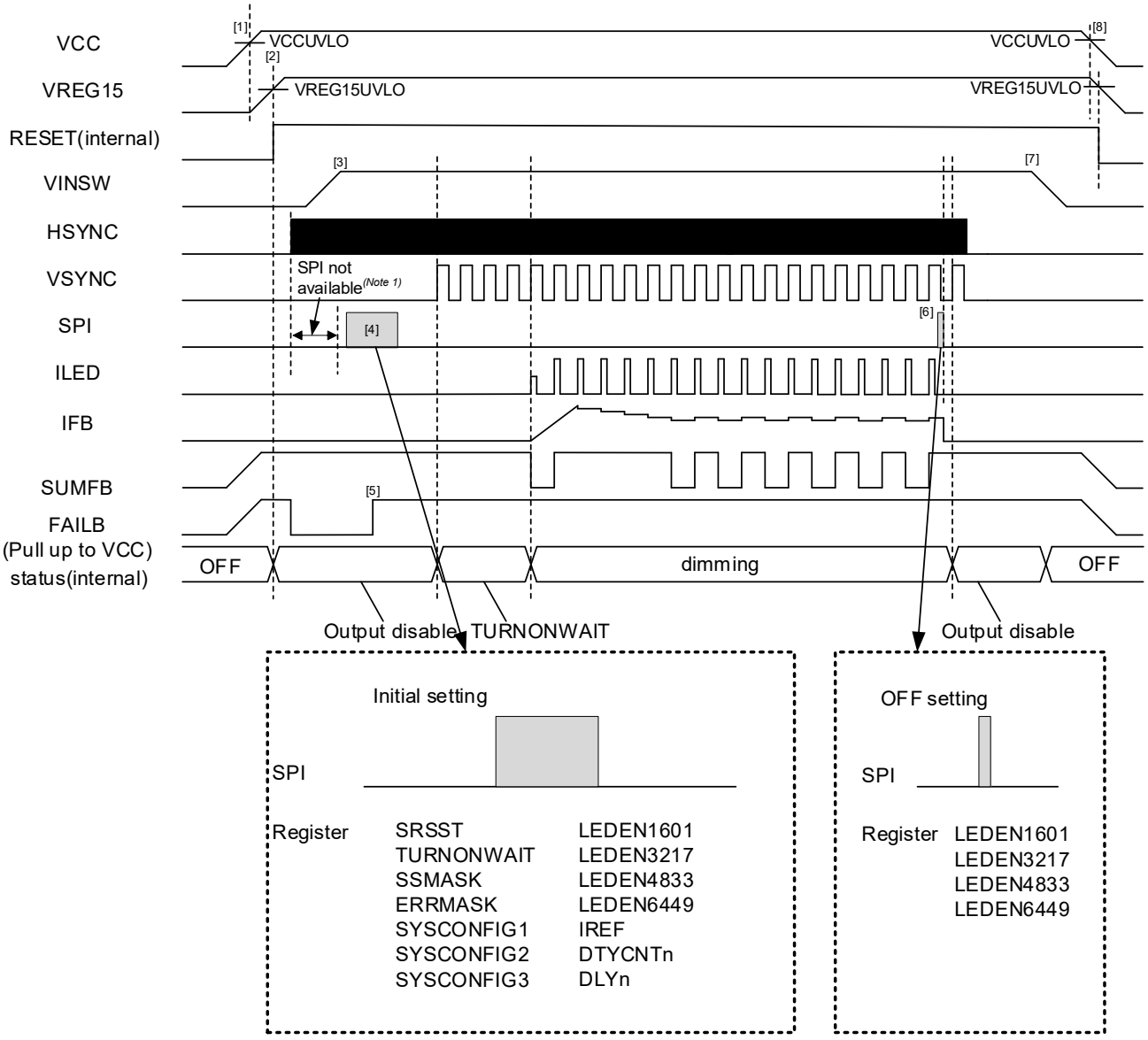


Figure 38. The Boot Sequence

Turn ON Sequence

[1] Power on VCC and VCCUVLO is released.
[2] VREG15UVLO and RESET is released. (RESET = VCCULVO or VREG15UVLO or SWRST[0])
[3] Power on VINSW.
[4] Set initial registers before 4th VSYNC period starts after SPI becomes available.
[5] ERTSDUVLO[0] is cleared by ERRCLR[0].

Turn OFF Sequence

[6] Set the register LEDEN1601, LEDEN3217, LEDEN4833 and LEDEN6449 to 0.
[7] Power off VINSW.
[8] Power off VCC.

(Note 1) SPI is not available for 1.5 ms after RESET and HSYNC input.

Timing Chart – continued

2 PWM Behavior When HSYNC Is Not Ideal

In this section, PWM dimming behavior is shown if HSYNC is not equal to ideal frequency.
The ideal frequency of HSYNC is 65535 times of VSYNC. Below are examples.

2.1 HSYNC Frequency Less than Ideal Frequency

Example: Delay = 0, Duty = 75 %, PWMFREQ[1:0] = 0

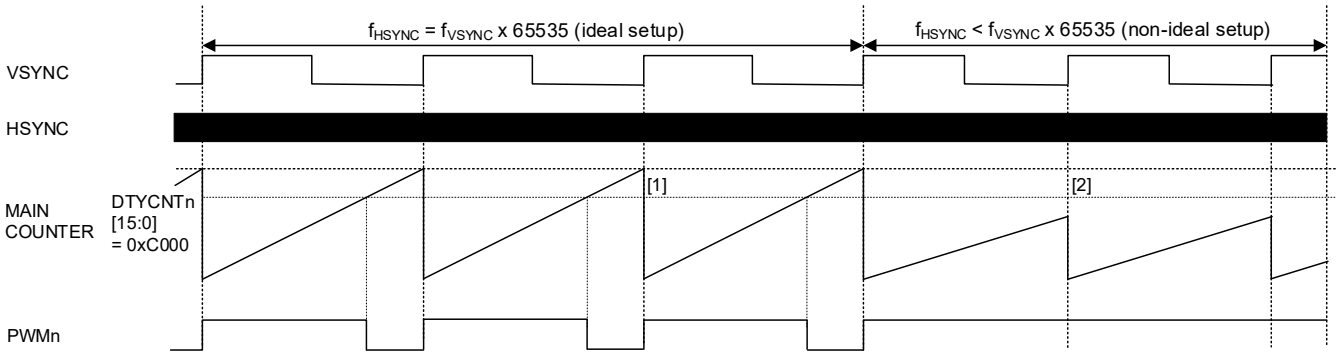


Figure 39. HSYNC Frequency Less than Ideal Frequency

The main counter is reset at the rising edge of VSYNC. The main counter starts counting up by HSYNC.
[1] As HSYNC frequency is equal to the ideal one, the main counter reaches the full value 65535. The ON width of PWMn is proper.
[2] As HSYNC frequency is smaller than the ideal one, the main counter does not reach the full value. The ON width of PWMn is long.

2.2 HSYNC Frequency More than Ideal Frequency

Example: Delay = 0, Duty = 75 %, PWMFREQ[1:0] = 0

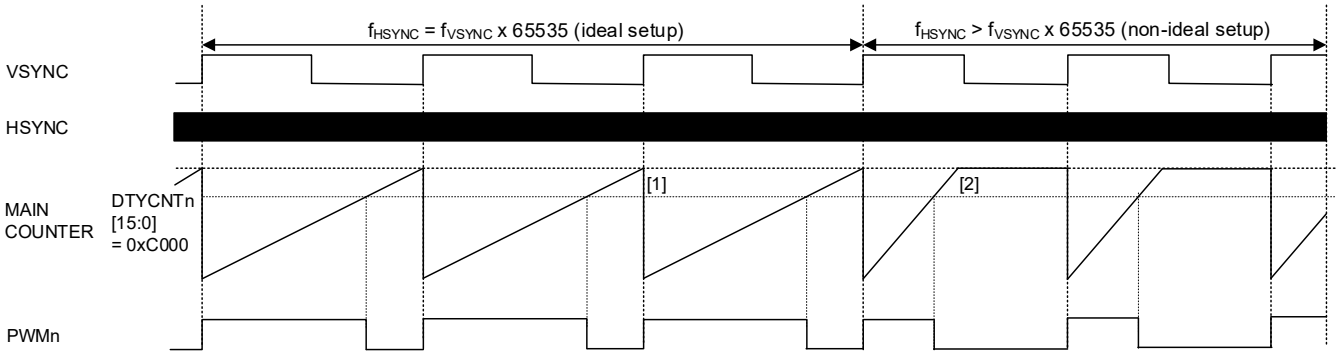


Figure 40. HSYNC Frequency More than Ideal Frequency

The main counter is reset at the rising edge of VSYNC. The main counter starts counting up by HSYNC.
[1] As HSYNC frequency is equal to the ideal one, the main counter reaches the full value 65535. The ON width of PWMn is proper.
[2] As HSYNC frequency is more than the ideal one, the main counter continues the full value 65535 without reset. The ON width of PWMn is short.

Timing Chart – continued

3 PWMFREQ Register Function

In this section, PWMFREQ Register Function is shown. When PWMFREQ[1:0] = 0, the main counter is only reset on the rising edge of VSYNC. In that case, the f_{PWM} and f_{VSYNC} will be the same. By setting PWMFREQ[1:0] to 1 or 2, the main counter will reset a specific number of times when it reaches 65535. By using this, the f_{PWM} can be multiplied by the f_{VSYNC}. The waveforms when f_{HSYNC} is 300000 times f_{VSYNC} are shown below. For the actual frequency settings, refer to Address 0x006: SYSCONFIG1.

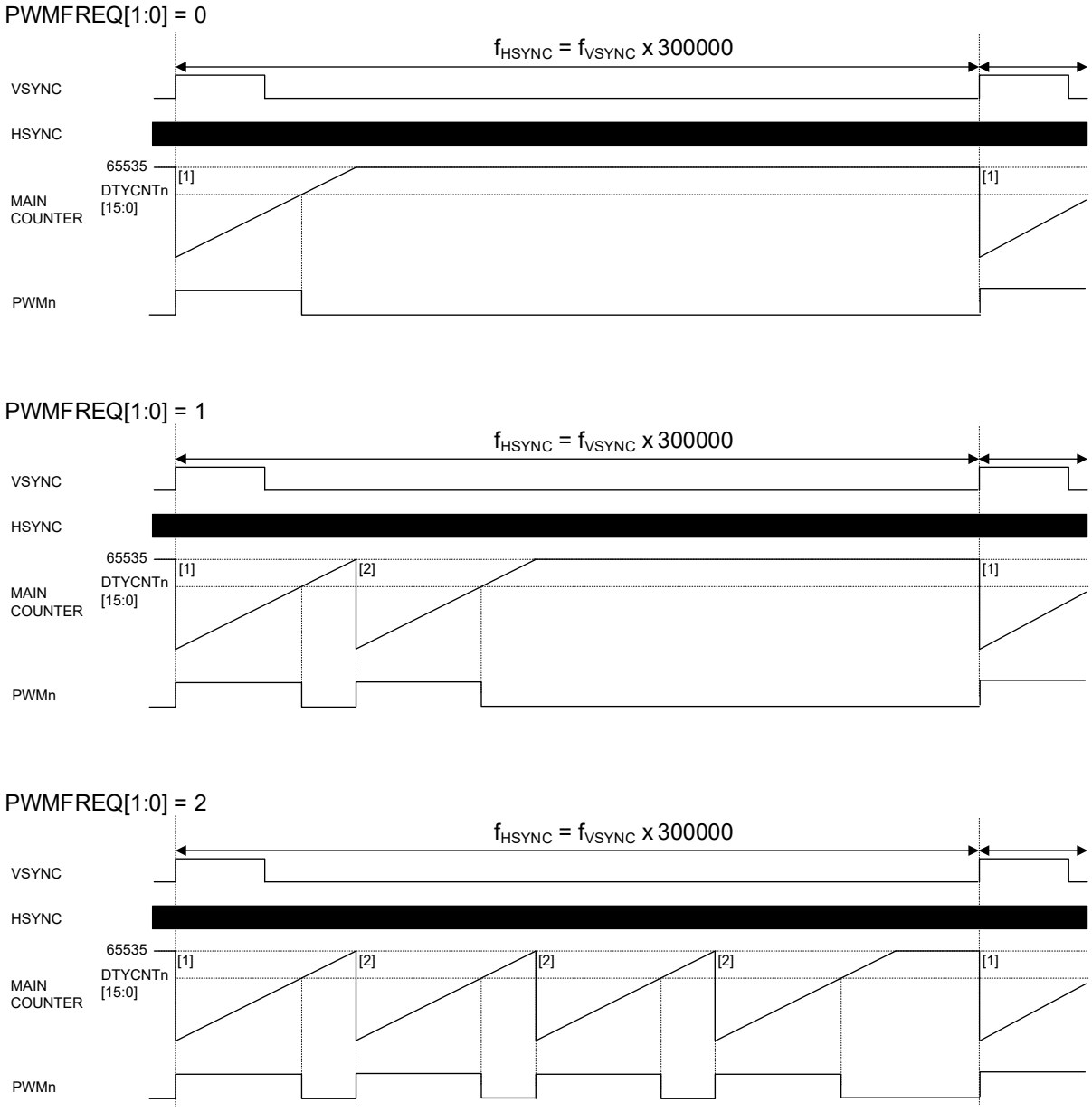


Figure 41. PWMFREQ[1:0] Function (f_{HSYNC} = f_{VSYNC} x 300000)

When PWMFREQ[1:0] is 1 or 2, the main counter resets when it reaches 65535. During one VSYNC, when PWMFREQ[1:0] = 1, it is reset once, and when PWMFREQ[1:0] = 2, it is reset three times.
[1] Main counter resets by the rising edge of VSYNC.
[2] Main counter resets by the reaching 65535.

Timing Chart – continued

4 ERROR Detection and Release

The following are the internal signals on the timing chart. This timing chart does not include analog delays.

XXXX_IL : Error detection signal (High: normal, Low: error)
RESET : Reset signal (High: normal, Low: reset)
SSEND : SSMASK signal (High: normal, Low: mask)
ERRMASK CNT : Counter for ERRMASK
SSMASK CNT : Counter for SSMASK

4.1 VCC Under Voltage Lock Out (VCCUVLO)

VCCUVLO can always be detected. When VCCUVLO is detected, the IC resets and the registers are set to initial values.

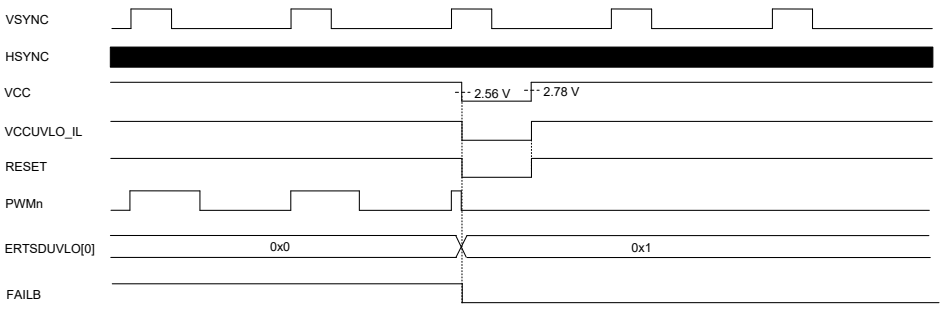


Figure 42. VCCUVLO Detection and Release

4.2 VREG15 Under Voltage Lock Out (VREG15UVLO)

VREG15UVLO can always be detected. When VREG15UVLO is detected, the IC resets and the registers are set to initial values.

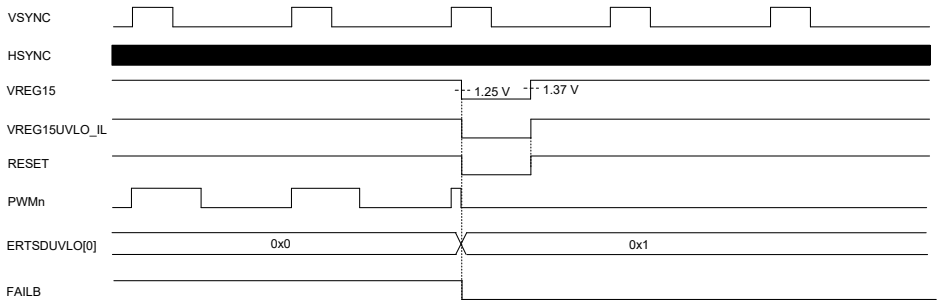


Figure 43. VREG15UVLO Detection and Release

4.3 Thermal Shutdown (TSD)

TSD can always be detected. When TSD is detected, the IC resets and the registers are set to initial values.

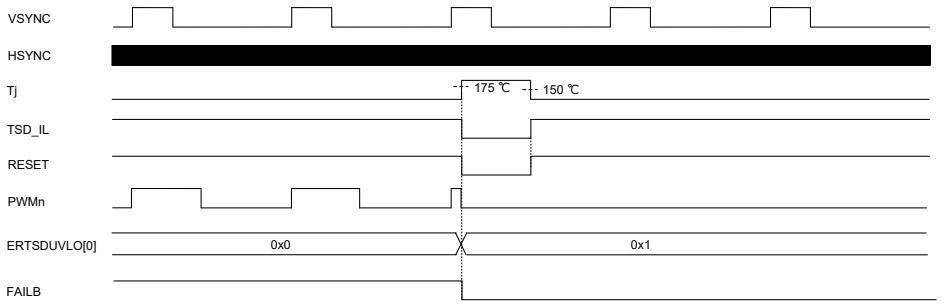


Figure 44. TSD Detection and Release

4 ERROR Detection and Release - continued

4.4 VINSW Over Voltage Protection (VINSWOVP)

VINSWOVP is detected after SSEND, and VINSWOVP is released as shown in Figure 45.

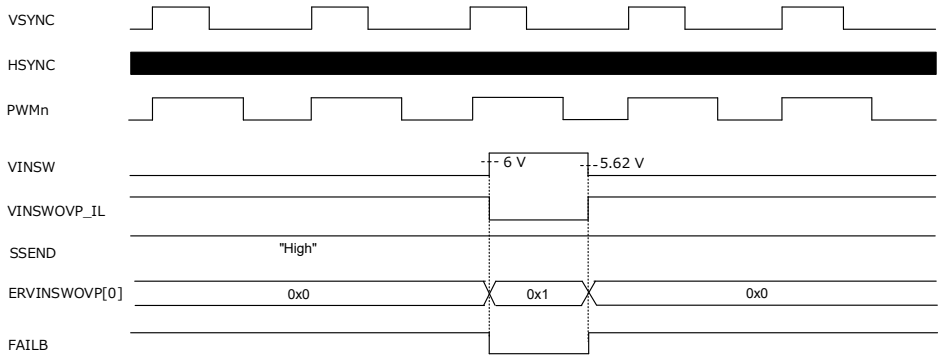


Figure 45. VINSWOVP Detection and Release
(VINSWOVPREF[1:0] = 0)

4.5 ISET Over Current Protection (ISETOCP)

ISETOCP is detected after SSEND, and ISETOCP is released as shown in Figure 46.
LEDn output is turned off by ISETOCP.

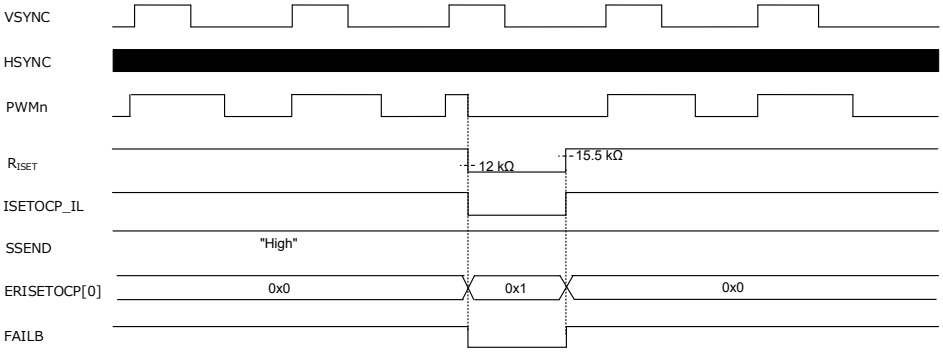


Figure 46. ISETOCP Detection and Release
(IREF[5:0] = 0x3F)

4.6 ISET Open Protection (ISETOPEN)

ISETOPEN is detected after SSEND, and ISETOPEN is released as shown in Figure 47.

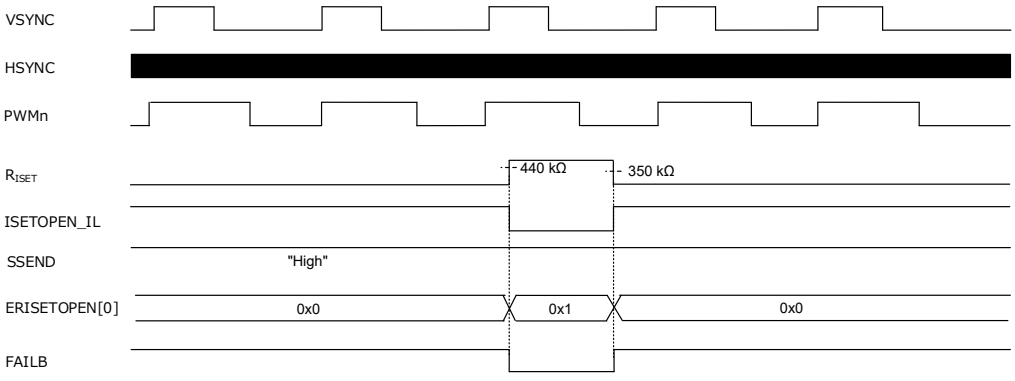


Figure 47. ISETOPEN Detection and Release
(IREF[5:0] = 0x3F)

4 ERROR Detection and Release - continued

4.7 LED Open Protection (LOP)

[Case1: LED Open Error signal is long width]
LOP detection and release are performed after $t_{ERRMASK}$ as shown in Figure 48.
If High of PWMn is shorter than $t_{ERRMASK}$, LOP is not detected and not released.

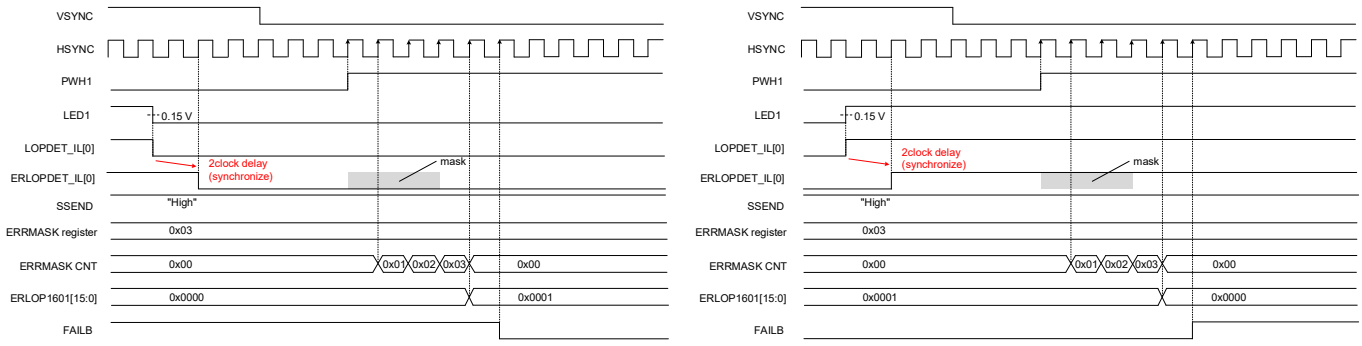


Figure 48. LOP Detection and Release
(ERRMASK[7:0] = 0x03)

[Case2: LED Open Error signal is short width]
While PWM1 = High and LOPDET_IL[0] = Low with SSEND = High (Soft Start end), if ERRMASK CNT does not count up until the ERRMASK[7:0], FAILB remains High.
In the same condition, if ERRMASK CNT counts up until ERRMASK[7:0], FAILB goes Low.

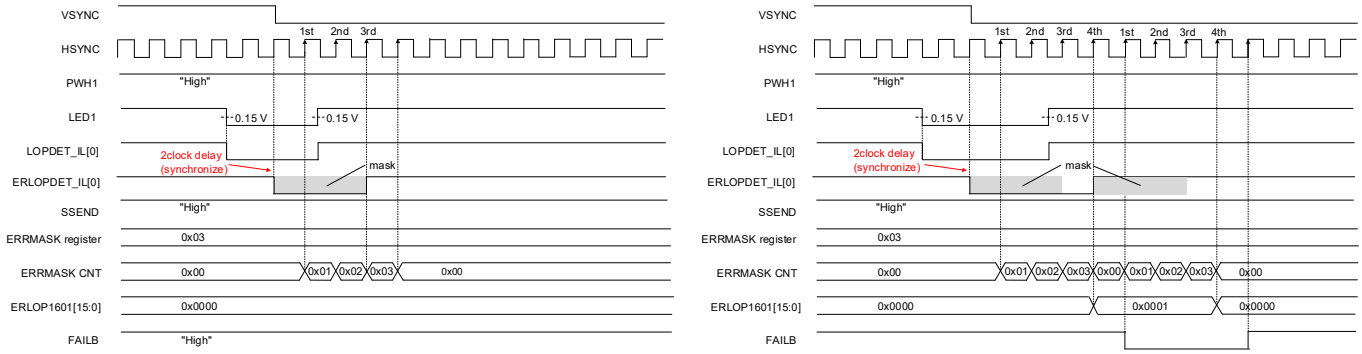


Figure 49. LOP Detection and Release
(ERRMASK[7:0] = 0x03)

4.8 LED Short Protection (LSH)

LSH detection and release are performed after $t_{ERRMASK}$ as shown in Figure 50.
If the capacitor of LEDn pin C_{LED} is connected, the transient response is affected. Set $t_{ERRMASK}$ considering the time margin of LSH.
If High of PWMn is shorter than $t_{ERRMASK}$, LSH is not detected and not released.

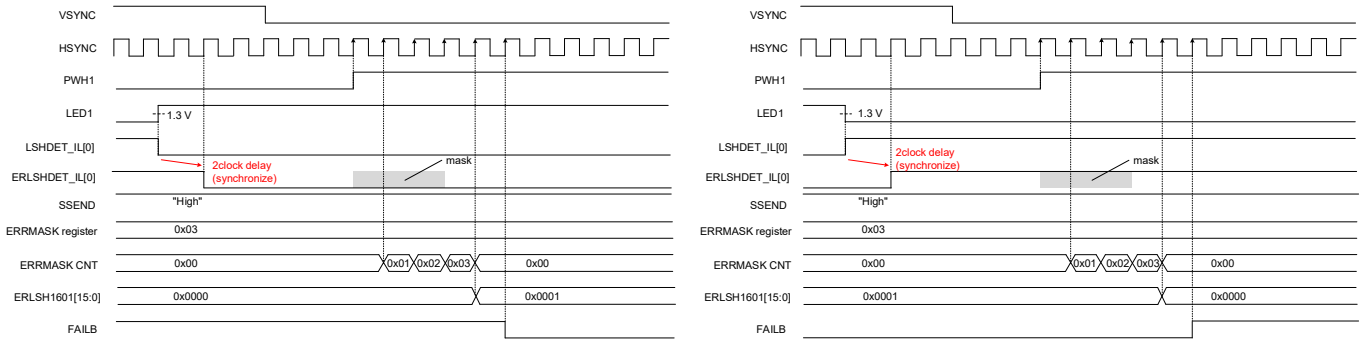


Figure 50. LSH Detection and Release
(ERRMASK[7:0] = 0x03, LEDSH[1:0] = 0)

4 ERROR Detection and Release - continued

4.9 LED Short Circuit Protection (LSCP)

LSCP is detected after ERRMASK, and LSCP is released as shown in Figure 51.
If Low of PWMn is shorter than $t_{ERRMASK}$, LSCP is not detected and not released.

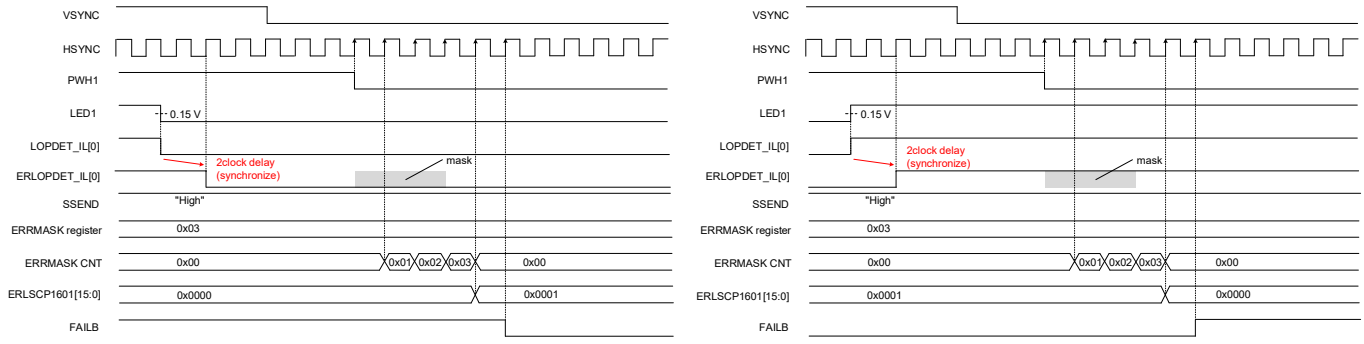


Figure 51. LSCP Detection and Release
(ERRMASK[7:0] = 0x03)

4.10 Soft Start Masking Function

Some protections cannot be detected during Soft Start (SSEND = Low). SSMASK counter counting starts on the first PWM rising edge. SSMASK counter counts up every VSYNC period until the SSMASK setting (SSEND = High) as shown Figure 52 below. For example, LOP can be detected when SSEND = High. It is also the same as for ISETOCP, ISETOPEN, LSH and LSCP.

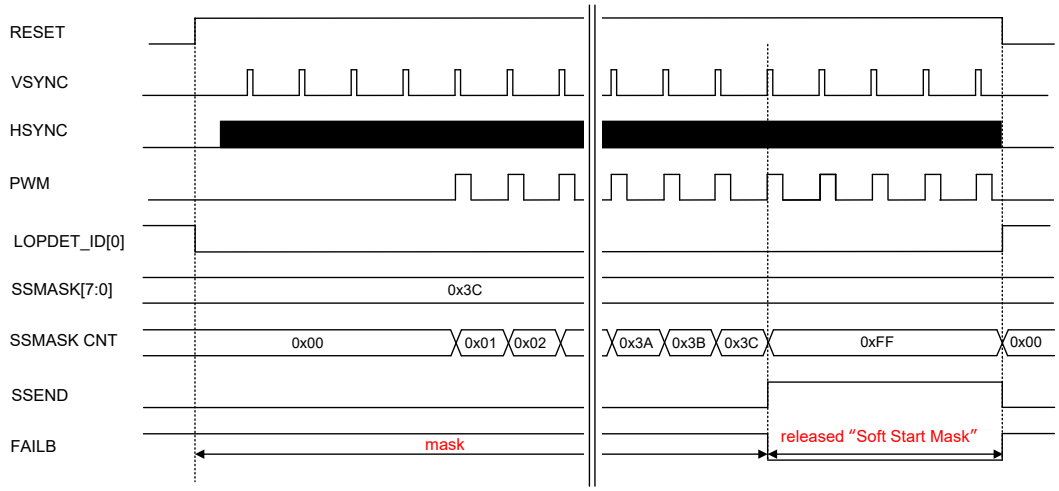


Figure 52. Setting for Soft Start Mask
(SSMASK[7:0] = 0x3C)

4 ERROR Detection and Release - continued

4.11 Error Sequence for the Register AUTOOFF

AUTOOFF set the abnormal LED = off automatically.
(Case) the register ERRLAT[0] = 0 and AUTOOFF[0] = 1

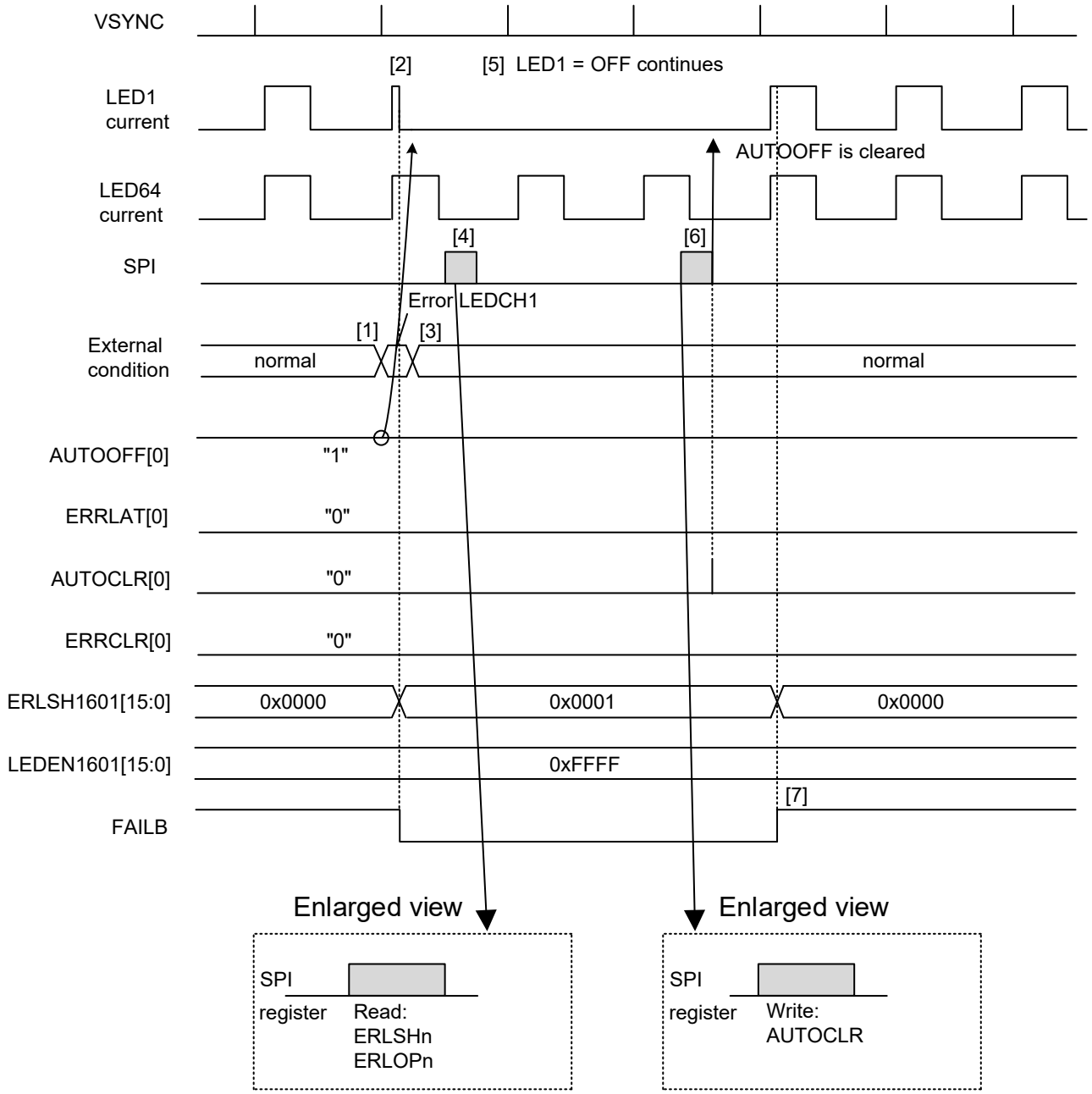


Figure 53. Error Sequence for the Register AUTOOFF = 1

[1] The external condition turns to LED Short Error.
[2] LED Short Error is detected, FAILB goes Low and, LEDCH1 output is turned off automatically. (PWM1 is Low)
[3] The external condition turns to normal. AUTOOFF = 1 so, the PWM1 = Low continues.
Since PWM1 is Low, IC does not judge the LED Short Error status. The FAILB keeps Low .
[4] By reading the register ERLSHn, ERLOPn, the abnormal LED component can be distinguished.
[5] LEDCH1 continues to turn off.
[6] The register AUTOCLR = 1 is written, the automatical off status is cleared.
[7] PWM1 is High, so IC judges LED Short Error. As the external condition is normal, LED turns on and ERLSH = All '0' and FAILB = High.

4 ERROR Detection and Release - continued

4.12 Error Sequence for the Register ERRLAT

ERRLAT keeps the abnormal state as latch state, even if that is released.
(Case) the register ERRLAT = 1 and AUTOOFF = 0

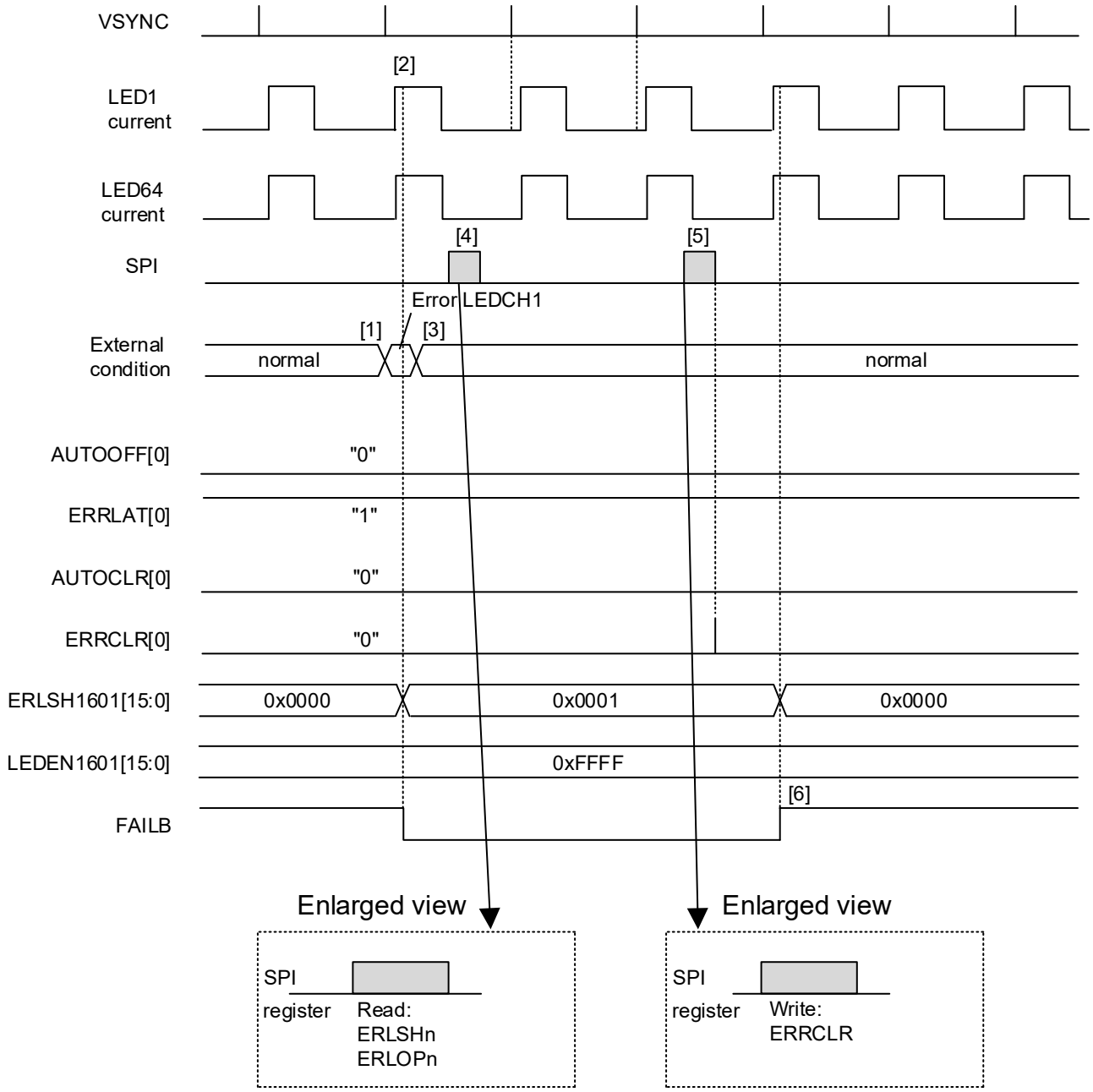


Figure 54. Error Sequence for the Register ERRLAT = 1

[1] The external condition turns to LED Short Error.
[2] LED Short Error is detected, FAILB goes Low.
[3] The external condition turns to normal. The register ERLSH keeps 0x0001 and FAILB asserts Low.
[4] By reading the register ERLSHn, ERLOPn, the abnormal LED component can be distinguished.
[5] The register ERRCLR = 1 is written, the register ERLSH is cleared.
[6] IC judges LED Short Error, the register ERLSH is cleared to All '0' and FAILB asserts High.

Condition for Protections

Table 45. Protection Table 1

		VCCUVLO	VREG15UVLO
Protection	Pin	VCC	VREG15
	Detection Condition	V_{CC} ≤ 2.56 V	V_{REG15} ≤ 1.25 V
	Release Condition	V_{CC} > 2.78 V	V_{REG15} > 1.37 V
Error Setting	Error Enable	-	-
	SSMASK	-	-
	ERRMASK	-	-
	ERRLAT	-	-
	AUTOOFF	-	-
Error Flag	Error Register	ERTSDUVLO*(Note 1)*	ERTSDUVLO*(Note 1)*
	FAILB	Low	Low

'O': It has the function. '-': It does not have the function.

(Note 1) Unless ERRCLR = 1 is written, ERTSDUVLO = 1 is retained.

Table 46. Protection Table 2

		TSD	VINSWOVP
Protection	Pin	-	VINSW
	Detection Condition	Tj ≥ 175 °C	$V_{INSW} \geq V_{INSWOVP}$
	Release Condition	Tj < 150 °C	$V_{INSW} < V_{INSWOVP} \times 0.936$
Error Setting	Error Enable	-	VINSWOVPEN
	SSMASK	-	O
	ERRMASK	-	-
	ERRLAT	-	O
	AUTOOFF	-	-
Error Flag	Error Register	ERTSDUVLO*(Note 1)*	ERVINSWOVP*(Note 2)*
	FAILB	Low	Low

'O': It has the function. '-': It does not have the function.

(Note 1) Unless ERRCLR = 1 is written, ERTSDUVLO = 1 is retained
(Note 2) When the IC detects VCCUVLO or VREG15UVLO or TSD, it cannot detect other protection.

Table 47. Protection Table 3

		ISETOCP	ISETOPEN
Protection	Pin	ISET	
	Detection Condition	$R_{ISETOCP} \leq 12$ kΩ	$R_{ISETOPEN} \geq 440$ kΩ
	Release Condition	$R_{ISETOCP} > 15.5$ kΩ	$R_{ISETOPEN} < 350$ kΩ
Error Setting	Error Enable	-	O
	SSMASK	O	O
	ERRMASK	-	-
	ERRLAT	O	O
	AUTOOFF	-	-
Error Flag	Error Register	ERISETOCP*(Note 1)(Note 2)*	ERISETOPEN*(Note 1)*
	FAILB	Low	Low

'O': It has the function. '-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD, it cannot detect other protection.
(Note 2) When ISETOCP is detected, the PWM of all CHs goes Low.

Condition for Protections – continued

Table 48. Protection Table 4

		LOP	LSH
Protection	Pin	LEDn	
	Detection Condition	LEDEN[n-1] = 1 and PWMn = 1 and $V_{LEDn} \leq 0.15$ V	LEDEN[n-1] = 1 and PWMn = 1 and $V_{LEDn} \geq V_{LSH}$
	Release Condition	LEDEN[n-1] = 0 or PWMn = 1 and $V_{LEDn} > 0.15$ V	LEDEN[n-1] = 0 or PWMn = 1 and $V_{LEDn} < V_{LSH}$
Error Setting	Error Enable	LOPEN	LSHEN
	SSMASK	O	O
	ERRMASK	O	O
	ERRLAT	O	O
	AUTOOFF	O	O
Error Flag	Error Register	ERLOP[n-1]*(Note 1)(Note 2)*	ERLSH[n-1]*(Note 1)*
	FAILB	Low	Low

'O': It has the function. '-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD, it cannot detect other protection.
(Note 2) LEDn pin voltage that detects LOP is automatically judged to be higher than V_{FBREF}.

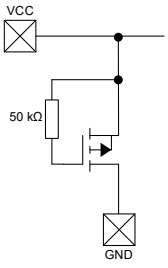
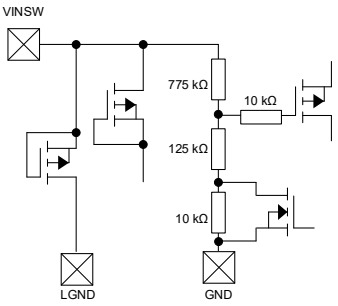
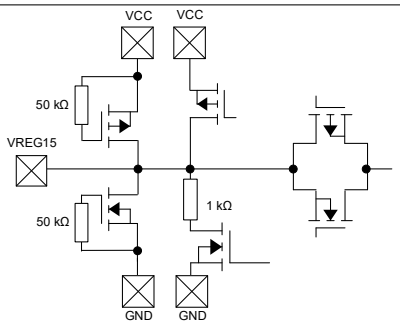
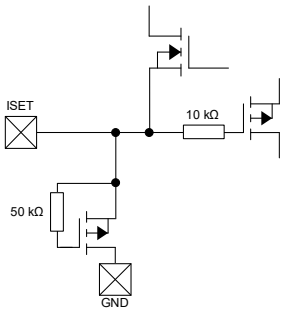
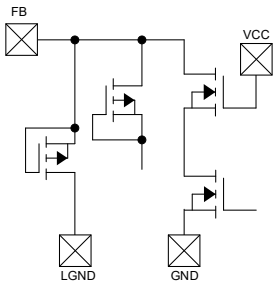
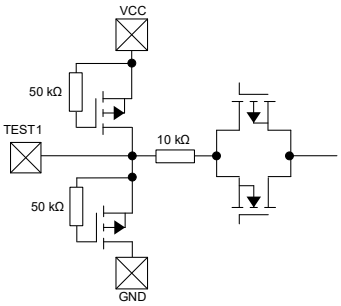
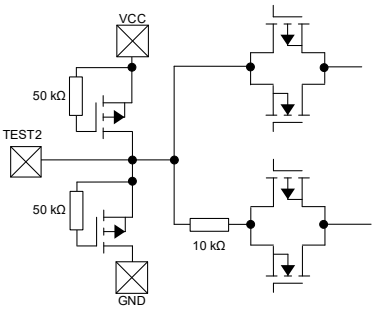
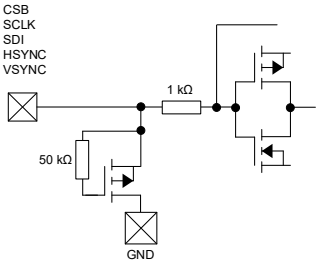
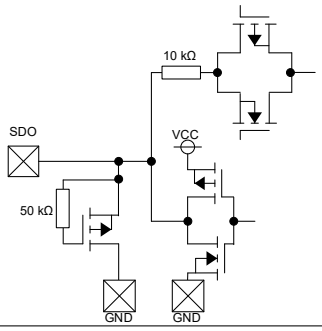
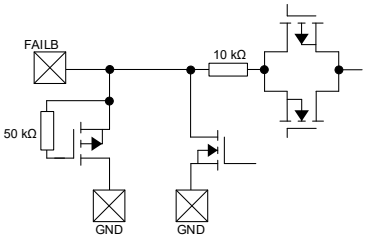
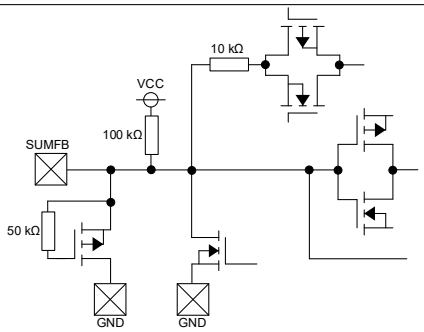
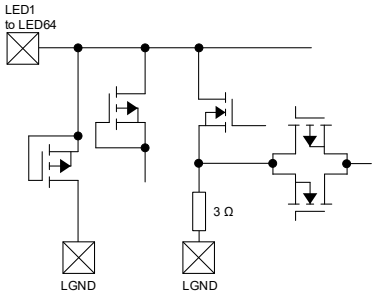
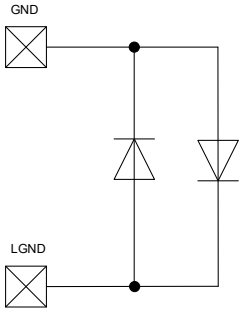
Table 49. Protection Table 5

		LSCP
Protection	Pin	LEDn
	Detection Condition	(LEDEN[n-1] = 0 or PWMn = 0) and $V_{LEDn} \leq 0.15$ V
	Release Condition	(LEDEN[n-1] = 0 or PWMn = 0) and $V_{LEDn} > 0.15$ V
Error Setting	Error Enable	LSCPEN
	SSMASK	O
	ERRMASK	O
	ERRLAT	O
	AUTOOFF	O
Error Flag	Error Register	ERLSCP[n-1]*(Note 1)*
	FAILB	Low

'O': It has the function. '-': It does not have the function.

(Note 1) When the IC detects VCCUVLO or VREG15UVLO or TSD, it cannot detect other protection.

I/O Equivalence Circuit

VCC	VINSW	VREG15
		
ISET	**FB**	**TEST1**
		
TEST2	**CSB, SCLK, SDI, HSYNC, VSYNC**	**SDO**
		
FAILB	**SUMFB**	**LED1 to LED64**
		
GND, LGND		
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So, unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

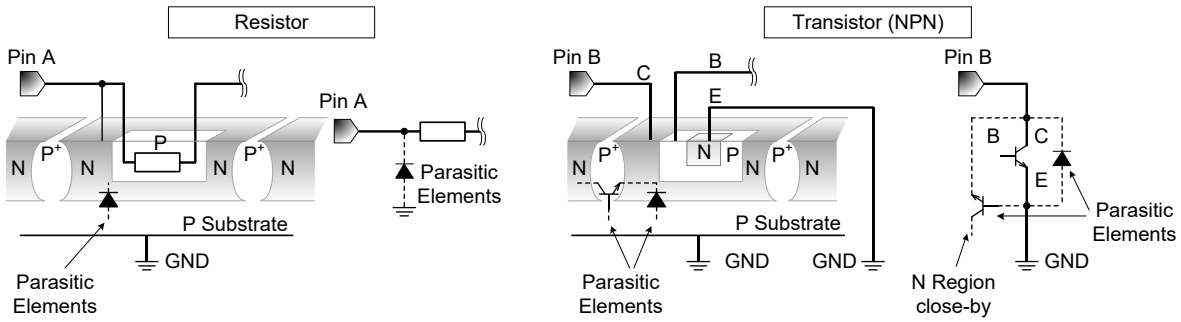


Figure 55 Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

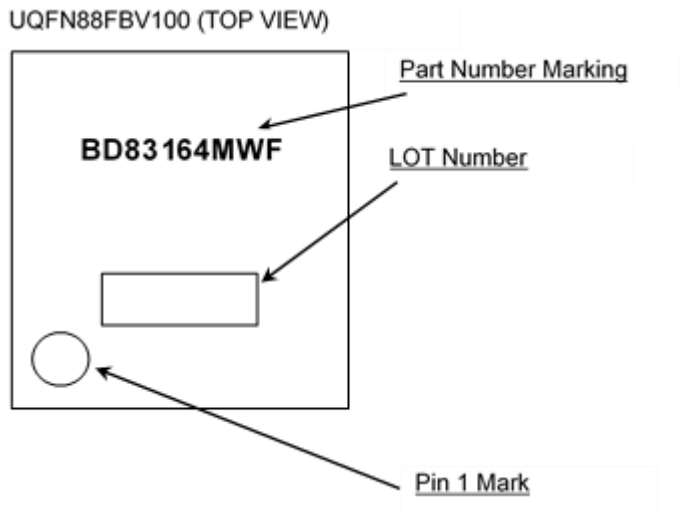
Ordering Information

B	D	8	3	1	6	4	M	W	F	-	M E 2

Package
MWF: UQFN88FBV100

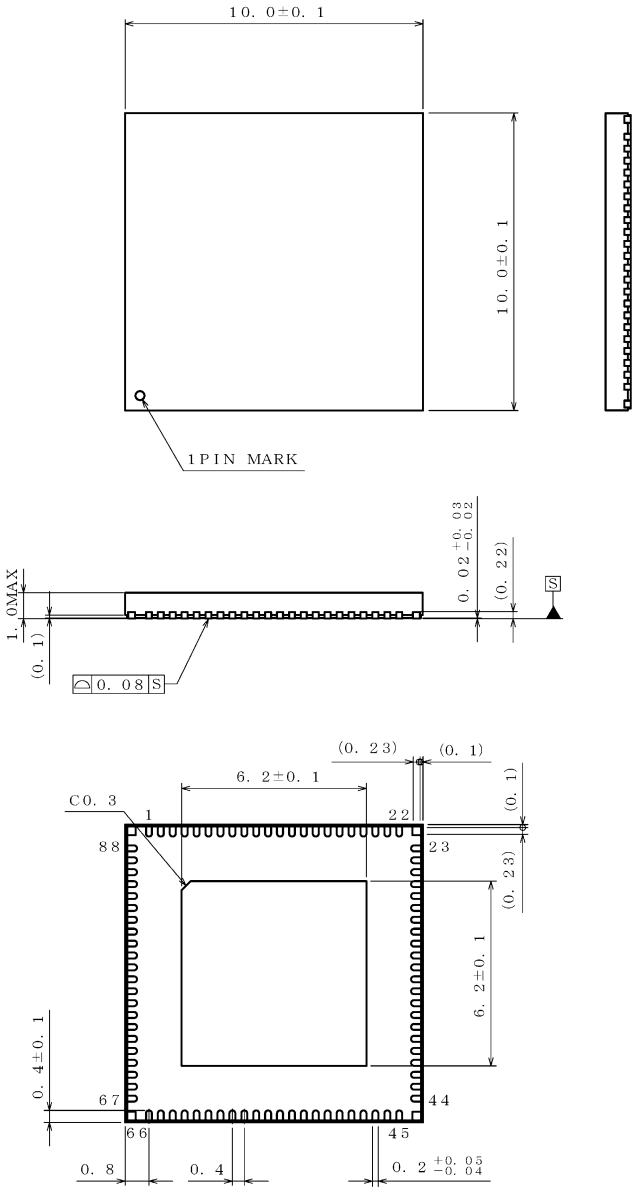
Product rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	UQFN88FBV100



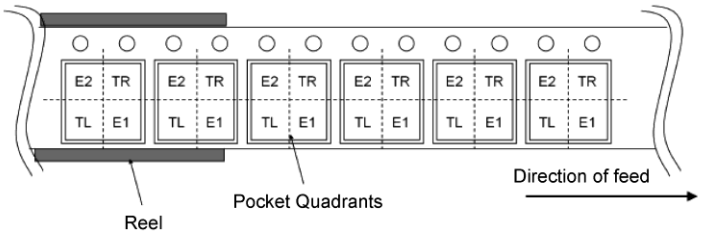
(UNIT : mm)

PKG : UQFN88FBV100
Drawing No. EX441−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Data	Revision	Changes
01.Mar.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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General Precaution

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