

1.2V to $V_{CC}-1V$, 0.55A 1ch

Ultra Low Dropout Linear Regulator

BD3507HFV

General Description

BD3507HFV is an ultra-low dropout linear regulator, which operates at a low input supply. The output voltage can be set by the VREF terminal and can be synchronized with other power supplies. BD3507HFV can make up a highly efficient system due to the implementation of an ultra-low dropout N-channel MOSFET with $R_{ON}=300m\Omega$ (Typ). This IC utilizes a power package with radiation fins, making it useable for regulation with a load of up to 550mA. BD3507HFV is suitable as power supply for chipset bus but it can also be used as a high side switch ($R_{ON} = 300m\Omega/I_{OUT} = 550mA$) of a low-voltage power supply line. External ceramic capacitors can be used as output capacitors for compact applications.

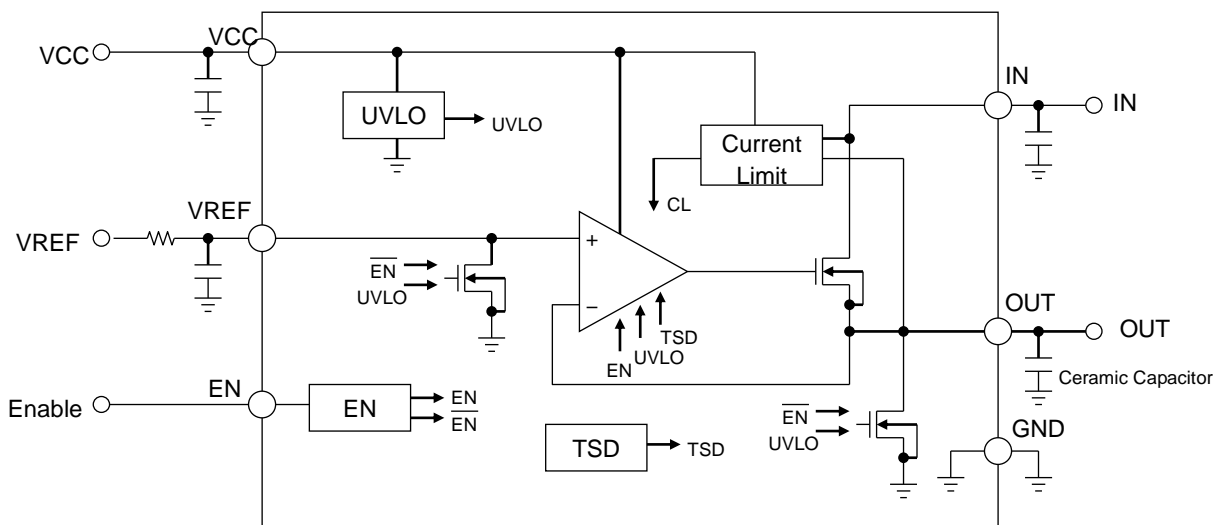
Features

- High-accuracy buffer circuit (adjustable from 0.65V to 2.7V)
- Thermal Shutdown Protection Circuit
- Enable function
- Over-Current Protection
- Undervoltage Lockout Protection
- Output Ceramic Capacitors

Applications

Notebook PC, desktop PC, digital camera, digital home appliances

Typical Application Circuit and Block Diagram

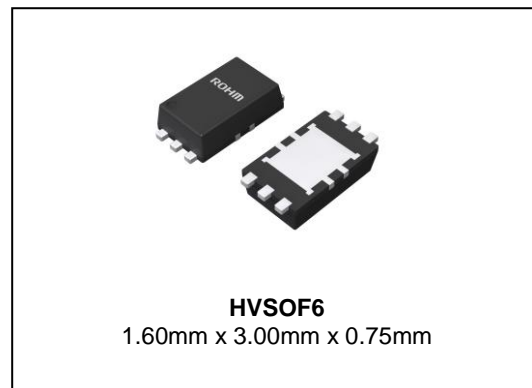


Key Specifications

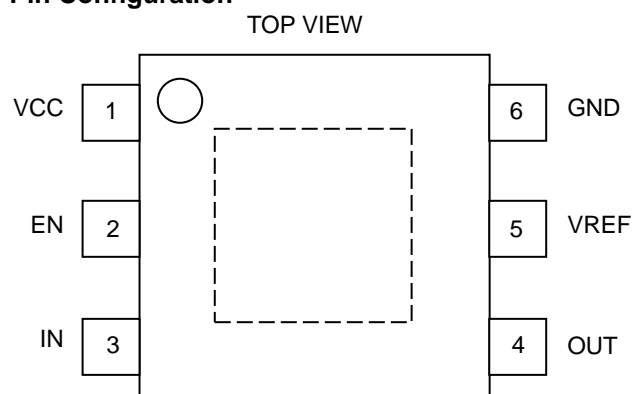
■ Input Voltage Range:	1.2V to $V_{CC}-1V$
■ Supply Voltage Range:	4.5V to 5.5V
■ Output Current:	550mA (Max)
■ ON-Resistance:	300mΩ(Typ)
■ Standby Current:	0μA (Typ)
■ Operating Temperature Range:	-10°C to +100°C

Package

W(Typ) x D(Typ) x H(Max)



Pin Configuration



Pin Descriptions

Pin No.	Pin Name	PIN Function
1	VCC	VCC pin
2	EN	Enable input pin
3	IN	Input voltage pin
4	OUT	Output pin
5	VREF	Reference voltage input pin
6	GND	Ground pin
reverse	FIN	Heat sink

Description of Blocks

- AMP**
 AMP is an error amplifier that compares the reference voltage (VREF) with OUT and drives the output N-Channel FET. The frequency characteristics are optimized so that ceramic capacitors can be used as output capacitors and high-speed transient response can be achieved. The input voltage range of the AMP section is GND-2.7V and the output voltage range of the AMP section is GND-VCC. When the regulator is OFF or UVLO, the output is brought to LOW level and the output of the N-Channel FET is turned OFF.
- EN**
 EN is a logic input pin which controls the regulator ON or OFF. When the regulator is OFF, the circuit current is maintained to 0μA to reduce the standby current of the device. In addition, EN turns ON the FET that discharges VREF and OUT to remove excess electric charge, and prevent malfunction of the IC at the output side. Since the EN pin has no electrical connection to the VCC terminal (as in the case where there is and ESD diode), it does not depend on the input sequence.
- UVLO**
 UVLO turns OFF the output to prevent output voltage from malfunctioning at the time when VCC voltage drops. Same with EN, UVLO discharges VREF and OUT. When the voltage exceeds the threshold voltage (3.8V, Typ), UVLO turns the output ON.
- Current Limit**
 When the output is ON and the output current exceeds the set current limit threshold (0.6A or more), the output voltage is attenuated to protect the IC on the load side. When current decreases, the output voltage is restored to the allowable value.
- Soft Start**
 Adding external resistor and capacitor to VREF pin can achieve soft-start. The output rises in synchronism with VREF pin until the time constant that is determined by C and R. Overshoot of output voltage or inrush current can be prevented.
- VREF**
 VREF is a reference voltage input pin and sets the output voltage. Since there is no electrical connection to the VCC terminal (as in the case where there is and ESD diode), it does not depend on the input sequence.
- TSD (Thermal Shut down)**
 In order to prevent thermal breakdown and thermal runaway of the IC, the output is turned OFF when chip temperature exceeds the threshold temperature. When the temperature decreases below the threshold temperature, the output is restored. While the TSD circuit is designed to protect the IC in the occurrence of extreme heat, thermal design should consider not to exceed Tj(max).
- IN**
 The IN line acts as the major current supply line, and is connected to the output N-Channel FET drain. Since there is no electrical connection with the VCC terminal, as in the case when an ESD diode is connected, so its operation does not depend on the input sequence. However, because of the body diode of the output N-Channel FET, there is electrical connection (diode connection) between IN and OUT. Consequently, when the output is turned ON and OFF by IN, reverse current flows, in which case care must be taken.

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Input Voltage1	V _{CC}	6.0 (Note1)	V
Input Voltage2	V _{IN}	6.0 (Note1)	V
Enable Input Voltage	V _{EN}	6.0 (Note1)	V
Power Dissipation1	Pd1	0.85 (Note 2)	W
Power Dissipation2	Pd2	1.40 (Note 3)	W
Operating Temperature Range	Topr	-10 to +100	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Provided Pd is not exceeded.

(Note 2) When mounted on a 70mm x 70mm x 1.6mm glass epoxy substrate (copper foil area: 2%). Derate by 6.8 mW/°C in the case of Ta≥25°C.

(Note 3) When mounted on a 70mm x 70mm x 1.6mm glass epoxy substrate (copper foil area: 18%). Derate by 11.2 mW/°C in the case of Ta≥25°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Rating		Unit
		Min	Max	
Input Voltage1	V _{CC}	4.5	5.5	V
Input Voltage2	V _{IN}	1.2	V _{CC} -1	V
VREF Setup Voltage	V _{REF}	0.65	2.7	V
EN Input Voltage	V _{EN}	-0.3	+5.5	V
Output Current	I _{OUT}	0	550	mA

Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V_{CC}=5V, V_{IN}=1.8V, V_{VREF}=1.2V, V_{EN}=3V)

Parameter	Symbol	Standard Value			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I _{CC}	-	0.4	0.7	mA	
Standby Current1	I _{STB}	-	0	10	μA	V _{EN} =0V
Standby Current2	I _{INSTB}	-	0	10	μA	V _{EN} =0V
Output Voltage1	V _{OUT1}	1.188	1.200	1.212	V	I _{OUT} =0mA
Output Voltage2	V _{OUT2}	1.188	1.200	1.212	V	I _{OUT} =300mA
Output Voltage3	V _{OUT3}	1.176	1.200	1.224	V	I _{OUT} =0mA to 550mA V _{CC} =4.5V to 5.5V Ta=-10°C to +100°C (Note 4)
Output Voltage4	V _{OUT4}	2.475	2.500	2.525	V	V _{IN} =3.3V, V _{VREF} =2.5V I _{OUT} =0mA
Output Voltage5	V _{OUT5}	2.475	2.500	2.525	V	V _{IN} =3.3V, V _{VREF} =2.5V I _{OUT} =300mA
Output Voltage6	V _{OUT6}	2.450	2.500	2.550	V	V _{IN} =3.3V, V _{VREF} =2.5V I _{OUT} =0mA to 550mA V _{CC} =4.5V to 5.5V Ta=-10°C to +100°C (Note 4)
Over-Current Protect	I _{CL}	600	-	-	mA	
Output ON-Resistance	R _{ON}	-	300	550	mΩ	
High Level Enable Input Voltage	V _{ENHIGH}	2.0	-	-	V	EN: Sweep-up
Low Level Enable Input Voltage	V _{ENLOW}	-0.2	-	+0.8	V	EN: Sweep-down
Enable Pin Input Current	I _{EN}	-	7	10	μA	V _{EN} =3V
UVLO OFF Voltage	V _{UVLO}	3.5	3.8	4.1	V	V _{CC} : Sweep-up
UVLO Hysteresis Voltage	V _{HYS}	100	160	220	mV	V _{CC} : Sweep-down
VREF Pin Bias Current	I _{VREF}	-0.1	-	+0.1	μA	V _{VREF} =0V to 2.7 V (Note 4)
VREF Discharge ON-Resistance	R _{ONREF}	-	1.0	2.0	kΩ	
Output Discharge ON-Resistance	R _{ONDIS}	-	0.1	0.3	kΩ	

(Note 4) Not 100% tested

Typical Performance Curves

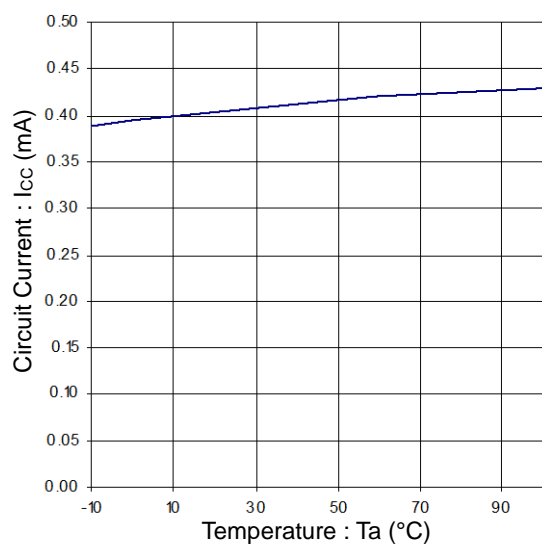
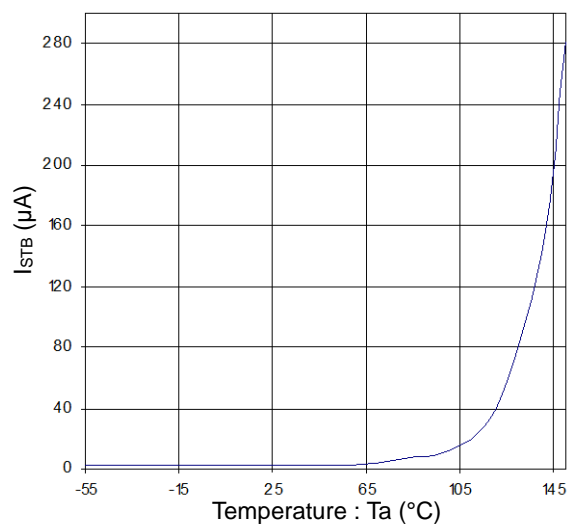
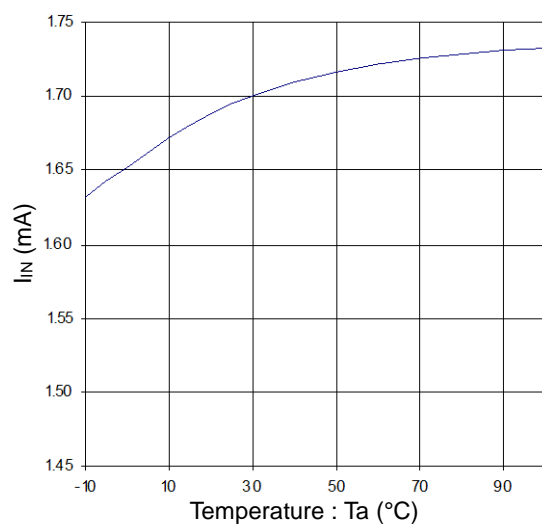
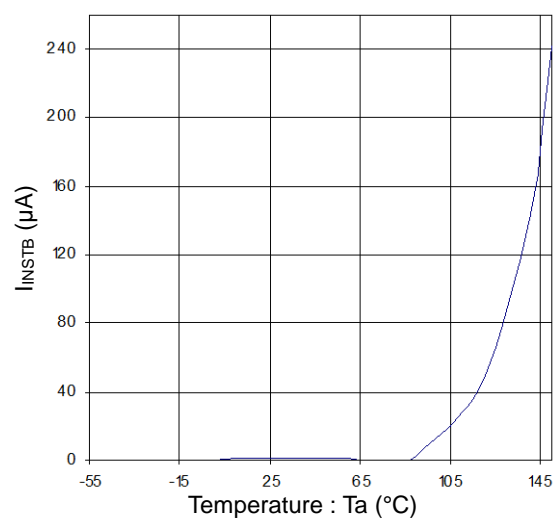


Figure 1. Circuit Current vs Temperature

Figure 2. I_{STB} vs TemperatureFigure 3. I_{IN} vs TemperatureFigure 4. I_{INSTB} vs Temperature

Typical Performance Curves – continued

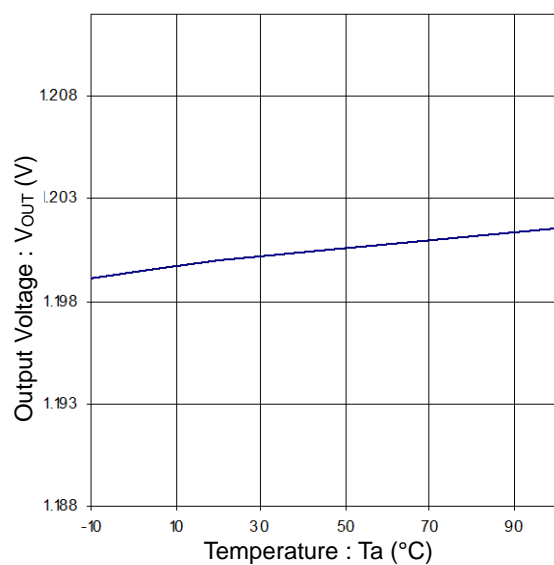


Figure 5. Output Voltage vs Temperature

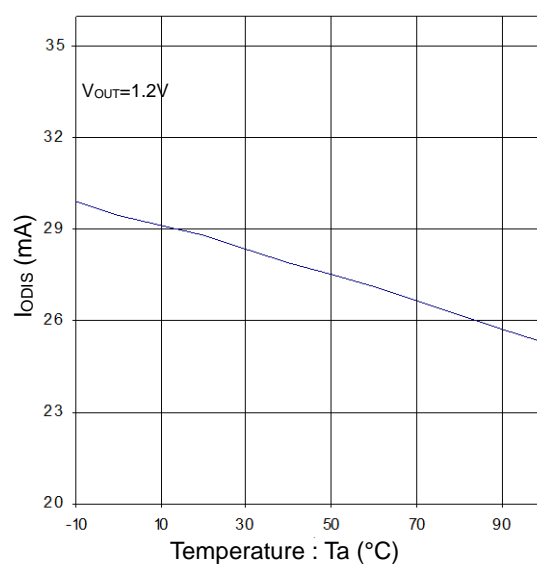
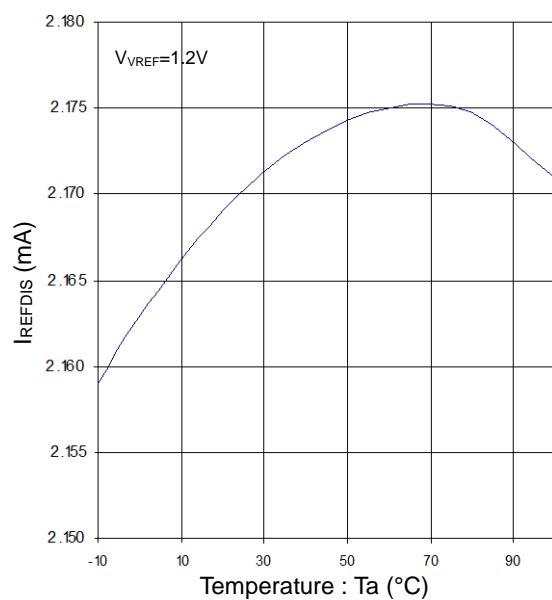
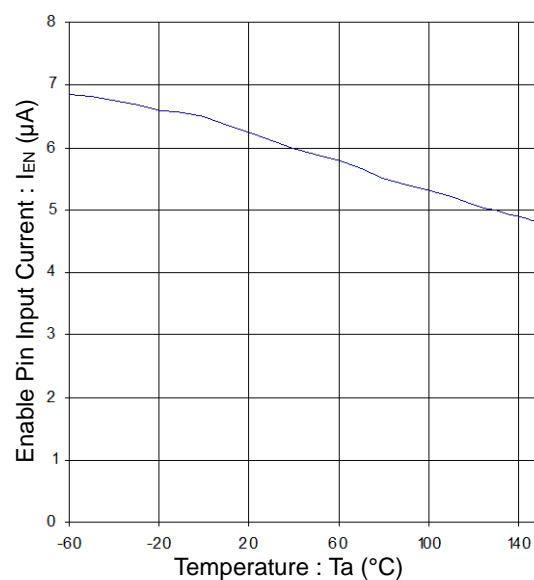
Figure 6. Output Discharge Current (I_{ODIS}) vs TemperatureFigure 7. VREF Discharge Current (I_{REFDIS}) vs Temperature

Figure 8. Enable Pin Input Current vs Temperature

Typical Performance Curves – continued

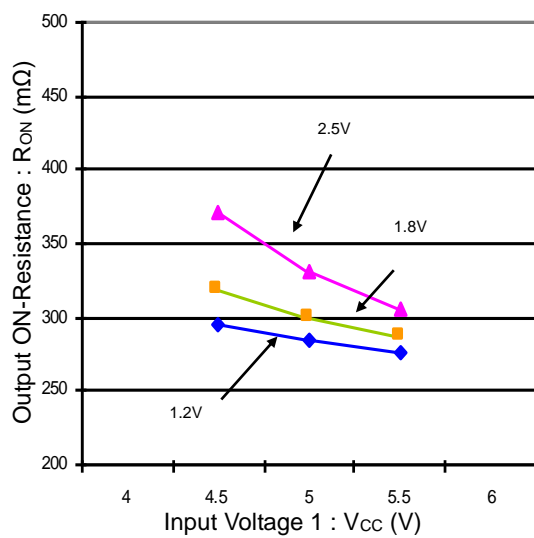


Figure 9. Output ON-Resistance vs Input Voltage 1

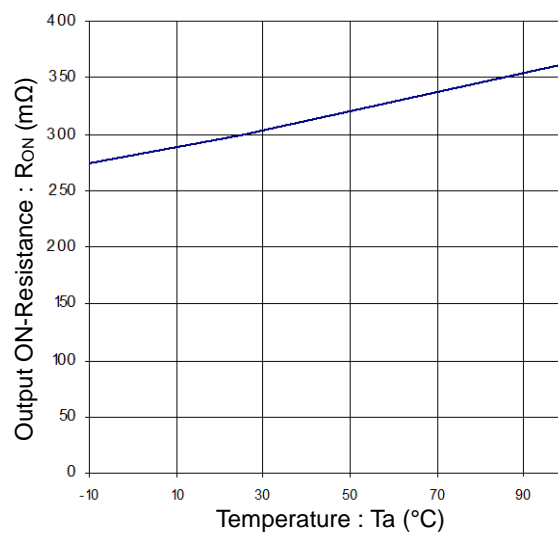


Figure 10. Output ON-Resistance vs Temperature

Typical Waveforms

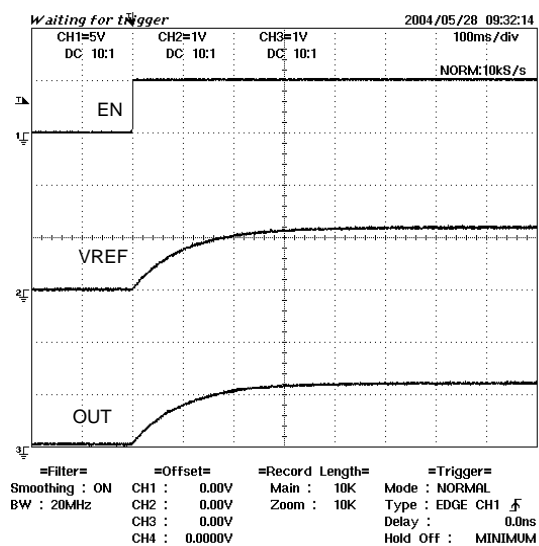


Figure 11. Startup Waveform

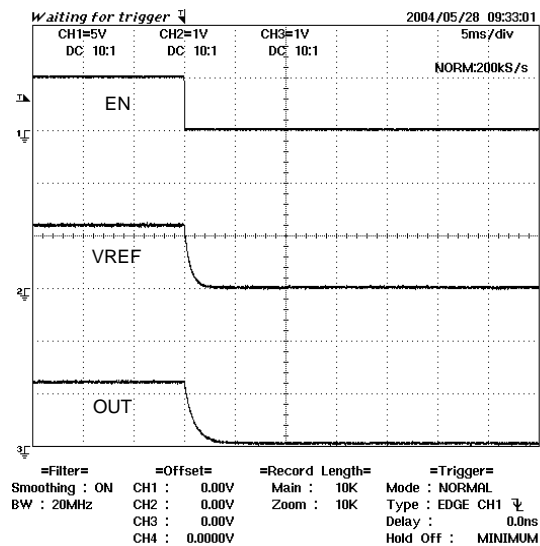


Figure 12. Shutdown Waveform

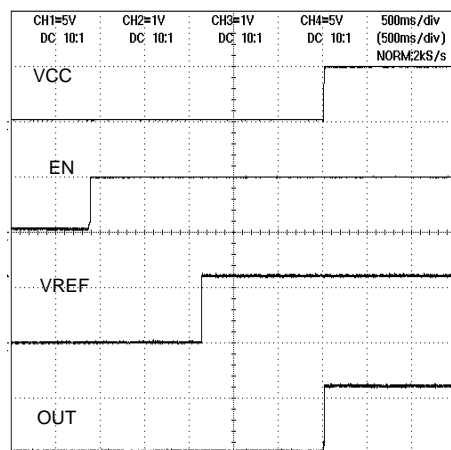


Figure 13. Input Sequence 1

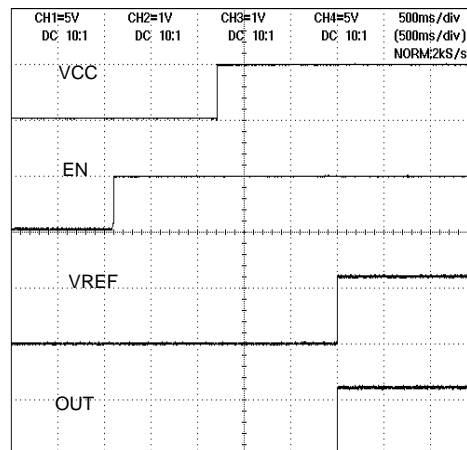


Figure 14. Input Sequence 2

Typical Waveforms – continued

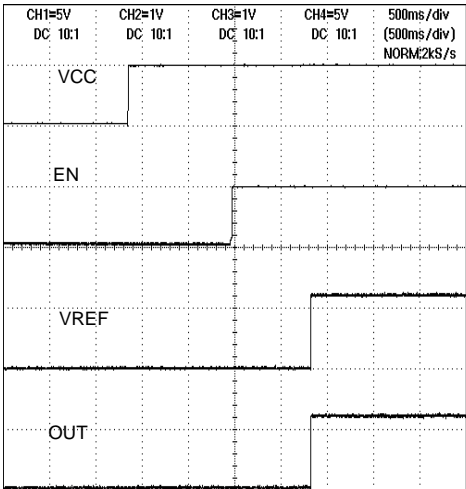


Figure 15. Input Sequence 3

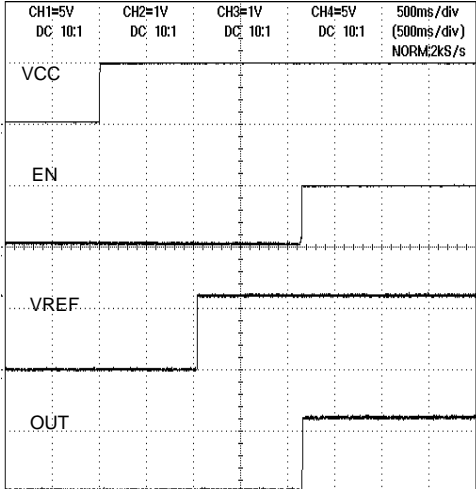


Figure 16. Input Sequence 4

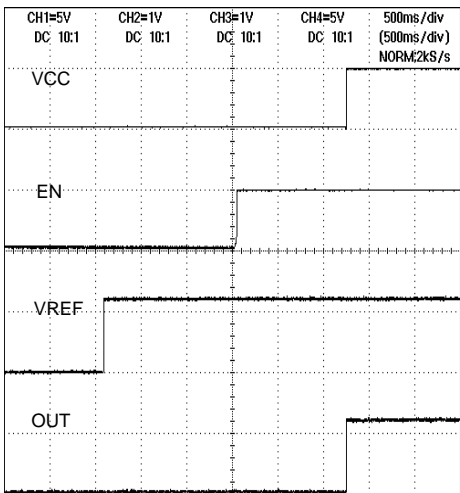


Figure 17. Input Sequence 5

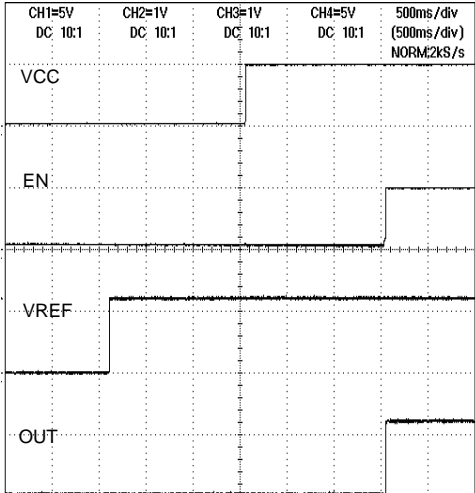


Figure 18. Input Sequence 6

Typical Waveforms – continued

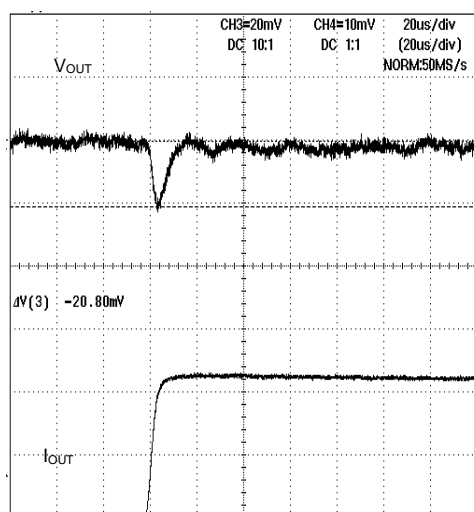


Figure 19. Transient Response
(0mA to 550mA/μs)

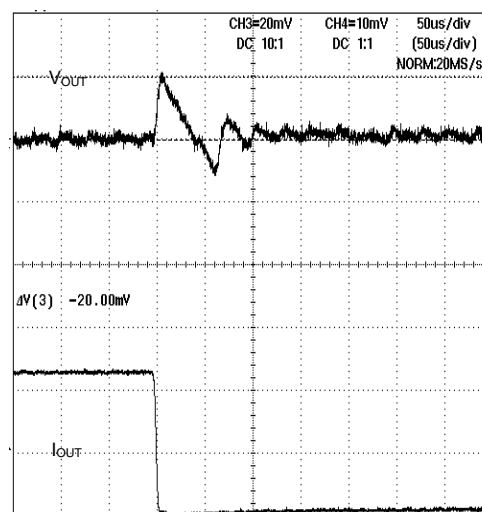
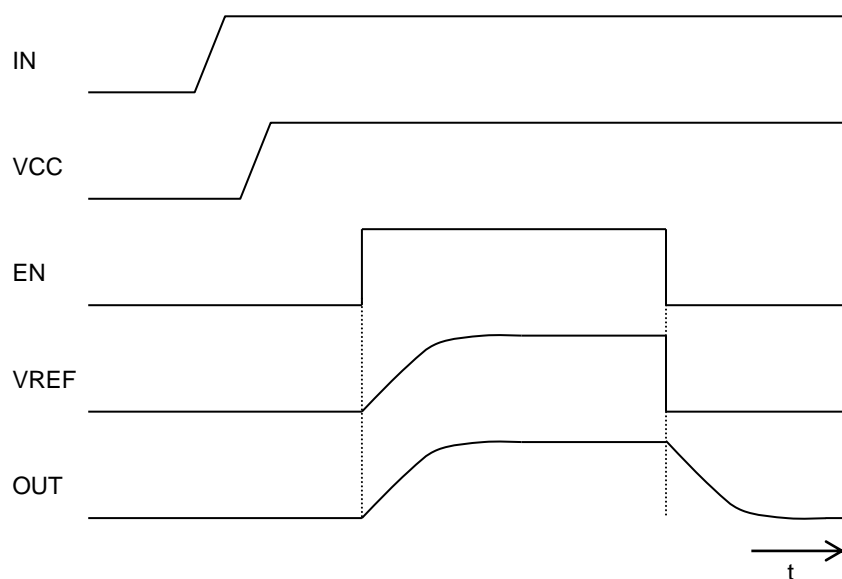


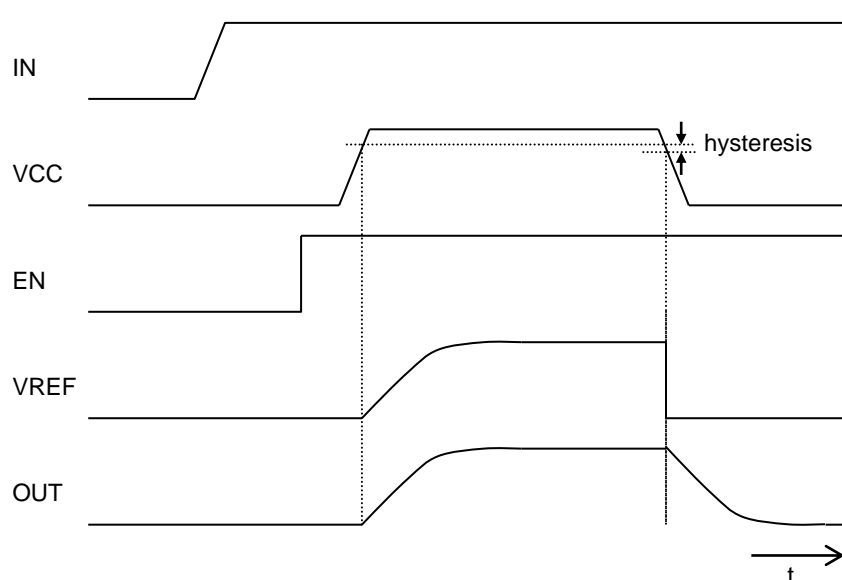
Figure 20. Transient Response
(550mA to 0mA/μs)

Timing Chart

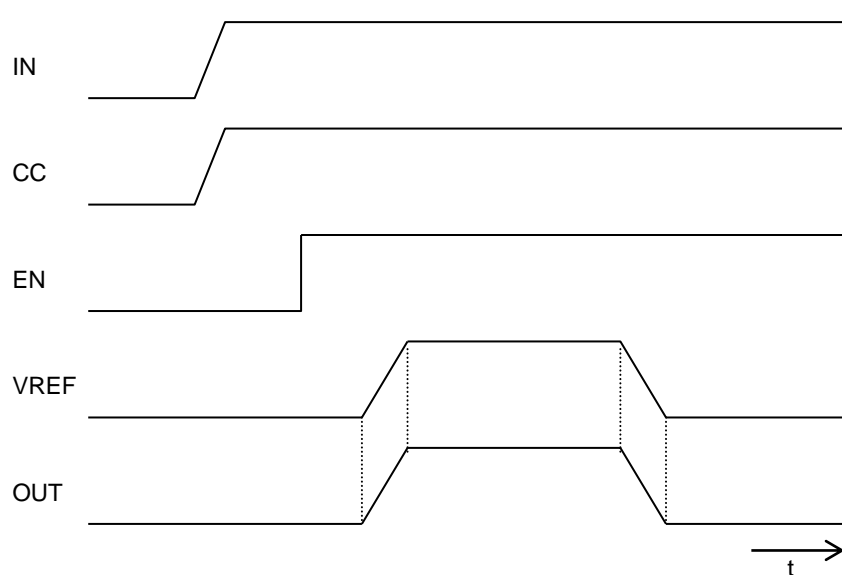
EN ON/OFF



VCC ON/OFF

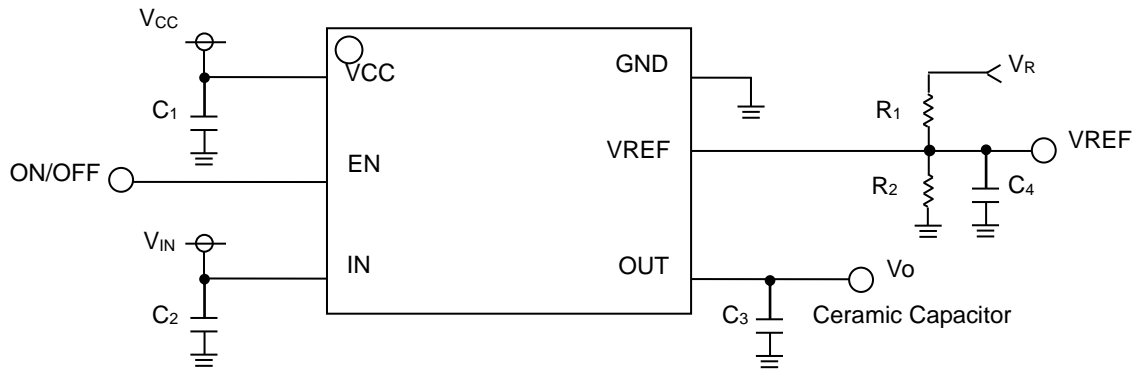


VREF Synchronous Action



Application Information

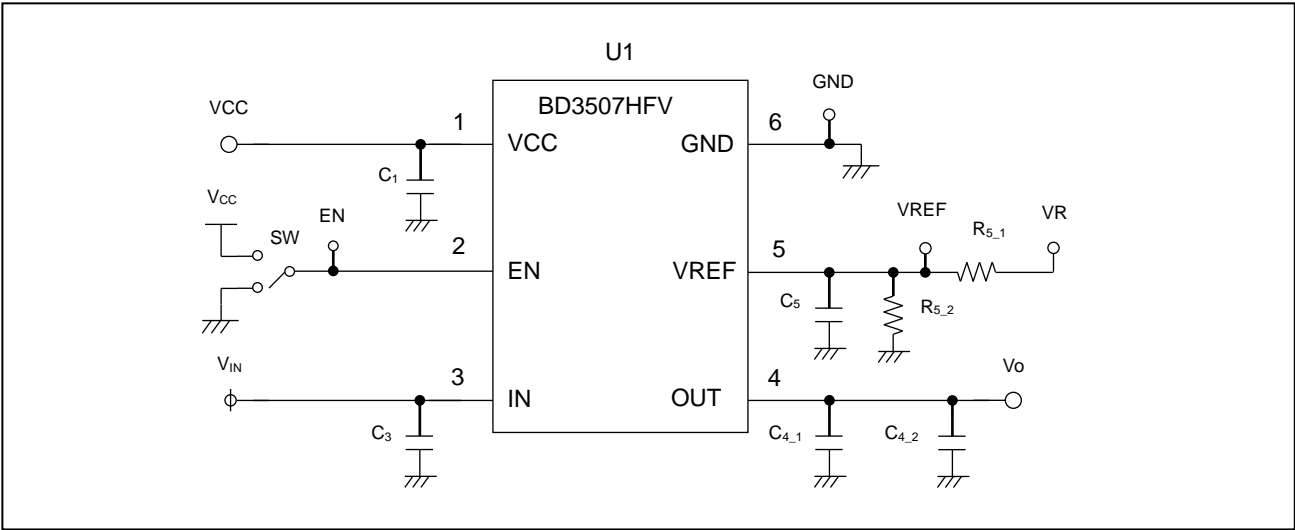
1. Application Setting Method



Part No	Value	Notes for Use
R ₁ /R ₂	22k/11k	The output voltage can be set by external reference voltage (V _R) and value of output voltage setting resistors (R ₁ , R ₂). Output voltage can be computed by $V_R \times R_2 / (R_1 + R_2)$ but it is recommended to use at the resistance value (total: about 10 kΩ) which is not susceptible to V _{REF} bias current (±100nA).
C ₃	22μF	Connect the output capacitor between OUT terminal and GND terminal without fail in order to stabilize output voltage. The output capacitor has a role to compensate for the phase of loop gain and to reduce output voltage fluctuation when load is rapidly changed. When there is an insufficient capacitor value, there is a possibility to cause oscillation, and when the equivalent serial resistance (ESR) of the capacitors is large, output voltage fluctuation is increased when load is rapidly changed. About 22μF ceramic capacitors are recommended but output capacitor greatly depends on temperature and load conditions. In addition, when various capacitors are connected in series, the total phase allowance of loop gain becomes insufficient, and oscillation may result. Thorough confirmation at application temperature and under load range conditions is requested.
C ₁	1μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (VCC). When output impedance of this power supply increases, the input voltages (V _{CC}) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 1μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended. But since the input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thorough confirmation under the application temperature and load range, is requested.
C ₂	10μF	The input capacitor plays a part to lower output impedance of a power supply connected to input terminals (IN). When output impedance of this power supply increases, the input voltages (V _{IN}) become unstable and there is a possibility of giving rise to oscillation and degraded ripple rejection characteristics. The use of capacitors of about 10μF with low ESR, which provide less capacity value changes caused by temperature changes, is recommended. But since input capacitor greatly depends on characteristics of the power supply used for input, substrate wiring pattern, thorough confirmation under the application temperature and load range, is requested.
C ₄	1μF	In this IC, the output voltage startup time can be set by VREF terminal capacitor (C ₄) and R ₁ and R ₂ values. When EN terminal is "High" or UVLO is reset, the desired output voltage is reached by the time constant determined by C ₄ , R ₁ , and R ₂ . It is recommended to use capacitors (B special) with small capacitance variations caused by temperature change for C ₄ .

2. Directions for Pattern Layout of PCB

BD3507HFV Evaluation Board Circuit

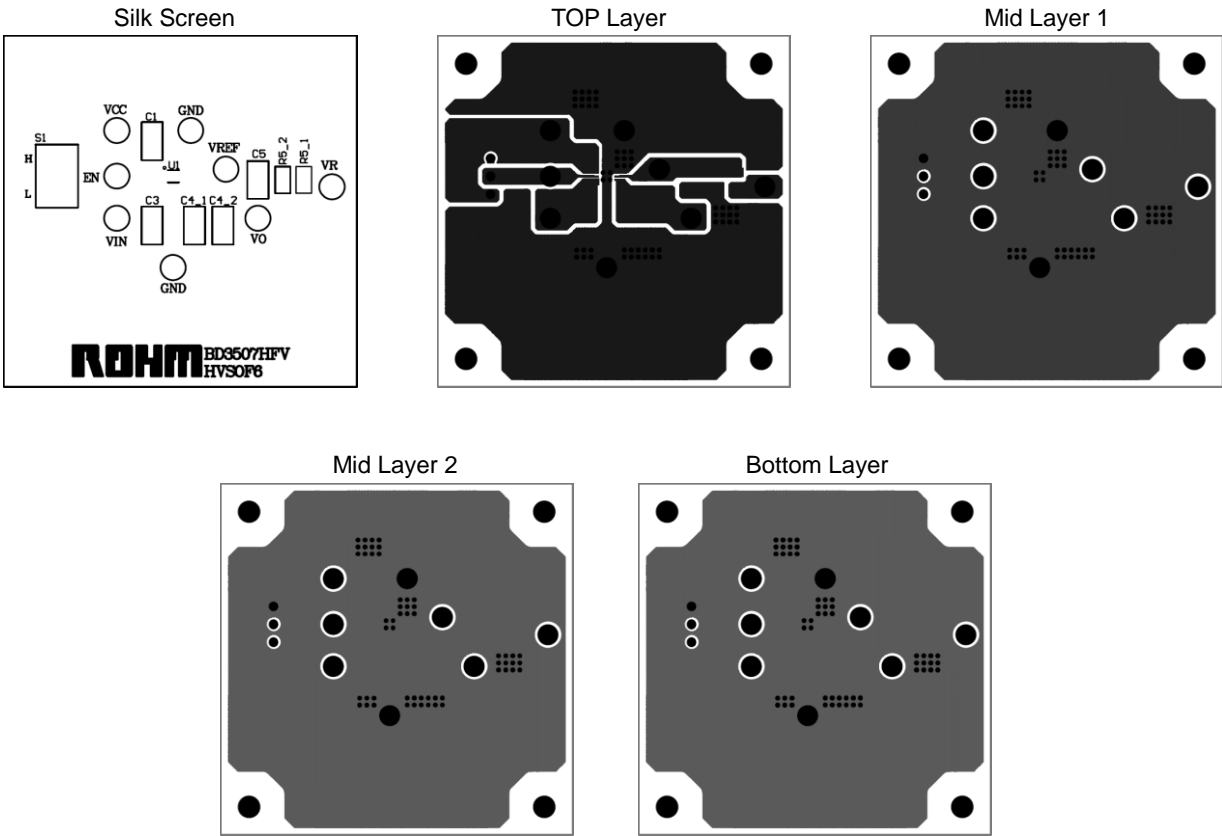


BD3507HFV Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3507HFV
R5_1	22k	ROHM	MCR03 Series
R5_2	11k	ROHM	MCR03 Series

Part No	Value	Company	Parts Name
C1	1μF	MURATA	GRM18 Series
C3	10μF	MURATA	GRM21 Series
C4_1	22μF	MURATA	GRM31 Series
C4_2			
C5	1μF	MURATA	GRM18 Series

BD3507HFV Evaluation Board Layout



3. Heat Loss

In thermal design, consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

- (1) Ambient temperature T_a shall be not more than 100°C.
- (2) Chip junction temperature T_j shall be not more than 150°C.

Chip junction temperature T_j can be considered as follows:

- ① Chip junction temperature T_j is found from IC surface temperature T_c under actual application conditions:

$$T_j = T_c + \theta_j - c \times W$$

<Reference value>

θ_j -c: HVSO6 30°C/W

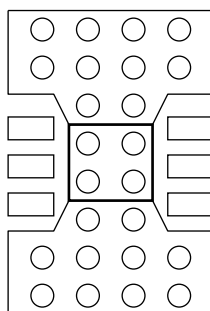
- ② Chip junction temperature T_j is found from ambient temperature T_a :

$$T_j = T_a + \theta_j - a \times W$$

<Reference value>

θ_j -a: HVSO6	147.1°C/W	Single-layer substrate (substrate surface copper foil area:2%)
	89.3°C/W	Single-layer substrate (substrate surface copper foil area:18%)
	73.5°C/W	Single-layer substrate (substrate surface copper foil area:51%) Substrate size 70 x 70 x 1.6mm ³

It is recommended to layout multiple VIAs, for heat radiation, in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multi-layer substrate). This package is so small (size: 1.0 mm x 1.6 mm) to layout the VIA at the bottom of IC. Spreading the pattern and increasing the number of VIA, as shown in the figure below, can achieve the most heat radiation characteristics. It is recommended that the size and number of VIA are designed suitable for the actual application (see figure below).



Most of heat loss in BD3507HFV occurs at the output N-Channel FET. Power loss is determined by multiplying the voltage between V_{IN} and V_{OUT} by the output current. Be sure to confirm the IN and OUT voltages used and output current conditions, and check with the thermal derating characteristics. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

$$\text{Power dissipation (W)} = \{\text{Input voltage (V}_{IN}\text{)} - \text{Output voltage (V}_{OUT} \approx V_{REF})\} \times I_{OUT} \text{ (average)}$$

Ex.) If $V_{IN} = 1.8\text{V}$, $V_{OUT} = 1.2\text{V}$, and $I_{OUT} \text{ (average)} = 0.5\text{ A}$, the power dissipation is given by the following:

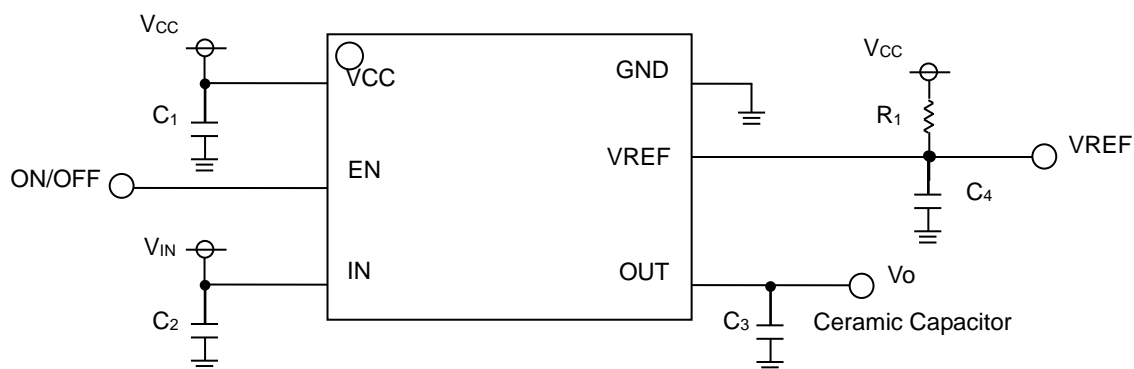
$$\begin{aligned} \text{Power dissipation (W)} &= (1.8\text{V} - 1.2\text{V}) \times 0.5\text{ (A)} \\ &= 0.3\text{W} \end{aligned}$$

4. Example of Application Circuit

Specifications: High side switch of low-voltage power supply line (1.2V - 2.5V)

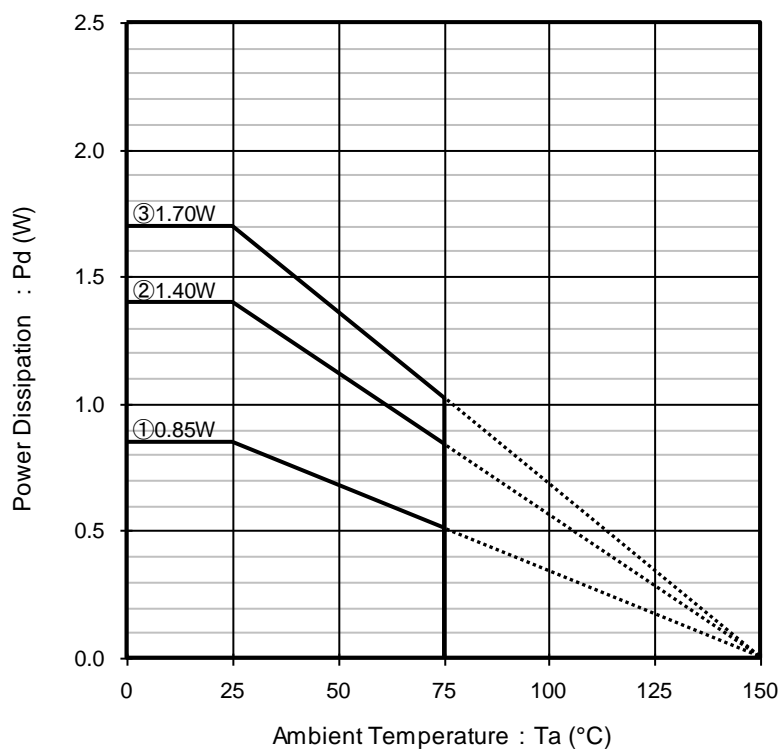
Characteristics: $R_{ON} = 300\text{ m}\Omega$, $I_{OUT(max)} = 550\text{ mA}$, with soft start function and overheat protection circuit equipped.

Example Circuit



Power Dissipation

HVSOF 6



① :PCB 1st layer (Cu-area : 2%)
 $\theta_{ja} = 147.1^{\circ}\text{C/W}$

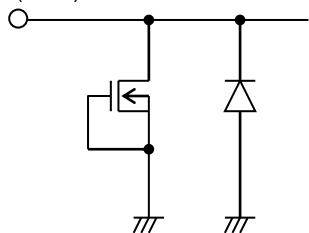
②:PCB 1st layer (Cu-area : 18%)
 $\theta_{ja} = 89.3^{\circ}\text{C/W}$

③:PCB 1st layer (Cu-area : 51%)
 $\theta_{ja} = 73.5^{\circ}\text{C/W}$

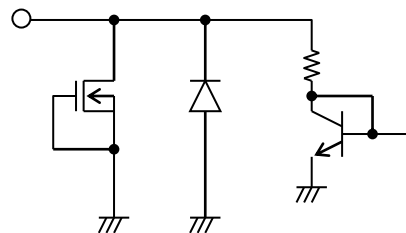
PCB size : 70mm x 70mm x 1.6mm

I/O Equivalent Circuits

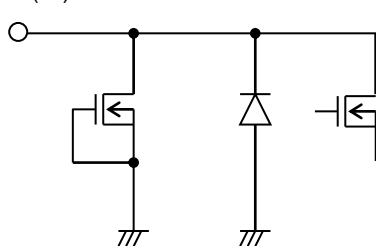
Pin 1 (VCC)



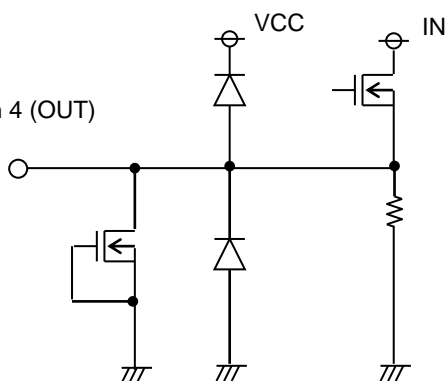
Pin 2 (EN)



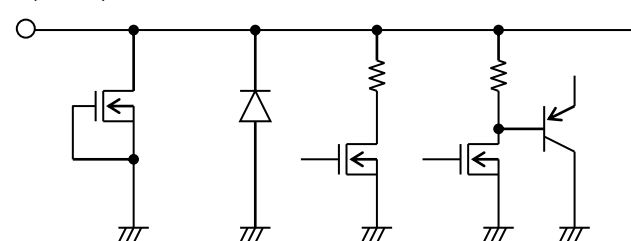
Pin 3 (IN)



Pin 4 (OUT)



Pin 5 (VREF)



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

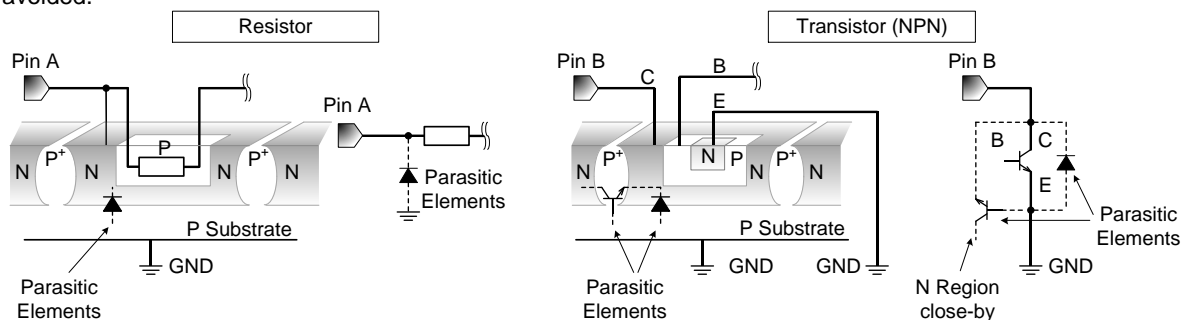


Figure 21. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF all output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

	TSD on Temperature [°C] (typ)	Hysteresis Temperature [°C] (typ)
BD3507HFV	175	-15

14. Capacitor across output and GND

In the event a large capacitor is connected across output and GND, when VCC and IN are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000 μ F between output and GND.

15. Input terminals (VCC,IN,EN,VREF)

In the present IC, EN terminal, IN terminal, VCC terminal, and VREF terminal have an independent construction. In addition, in order to prevent malfunction at the time of low input, the UVLO function is equipped with the VCC terminal. They begin to start output voltage when all the terminals reach threshold voltage without depending on the input order of input terminals.

16. Heat sink

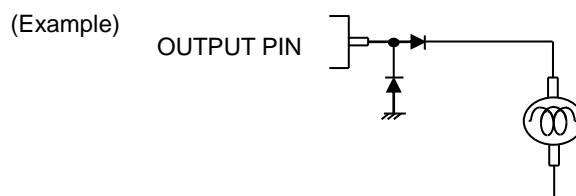
Heatsink is connected to SUB, which should be short-circuited to GND. Solder the heatsink to a pc board properly, which offers lower thermal resistance.

17. Operating range

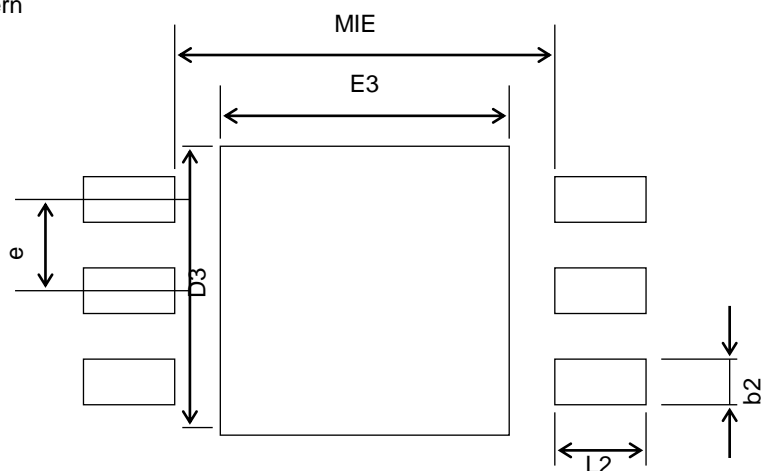
Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

Operational Notes – continued

18. For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.
19. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.



HVSOF6 land pattern



Unit: mm

Land Pitch e	Land Space MIE	Land Length L2	Land Width b2
0.50	2.20	0.55	0.25

Pad Length D3	Pad Width E3
1.60	1.60

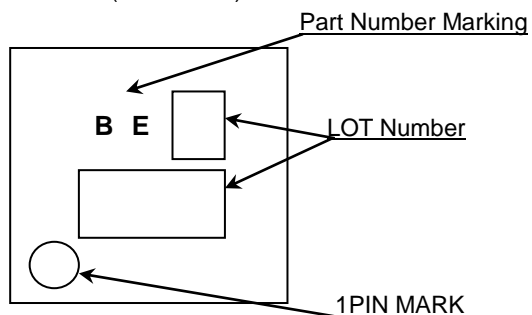
In actually designing, optimize in accordance with the condition.

Ordering Information

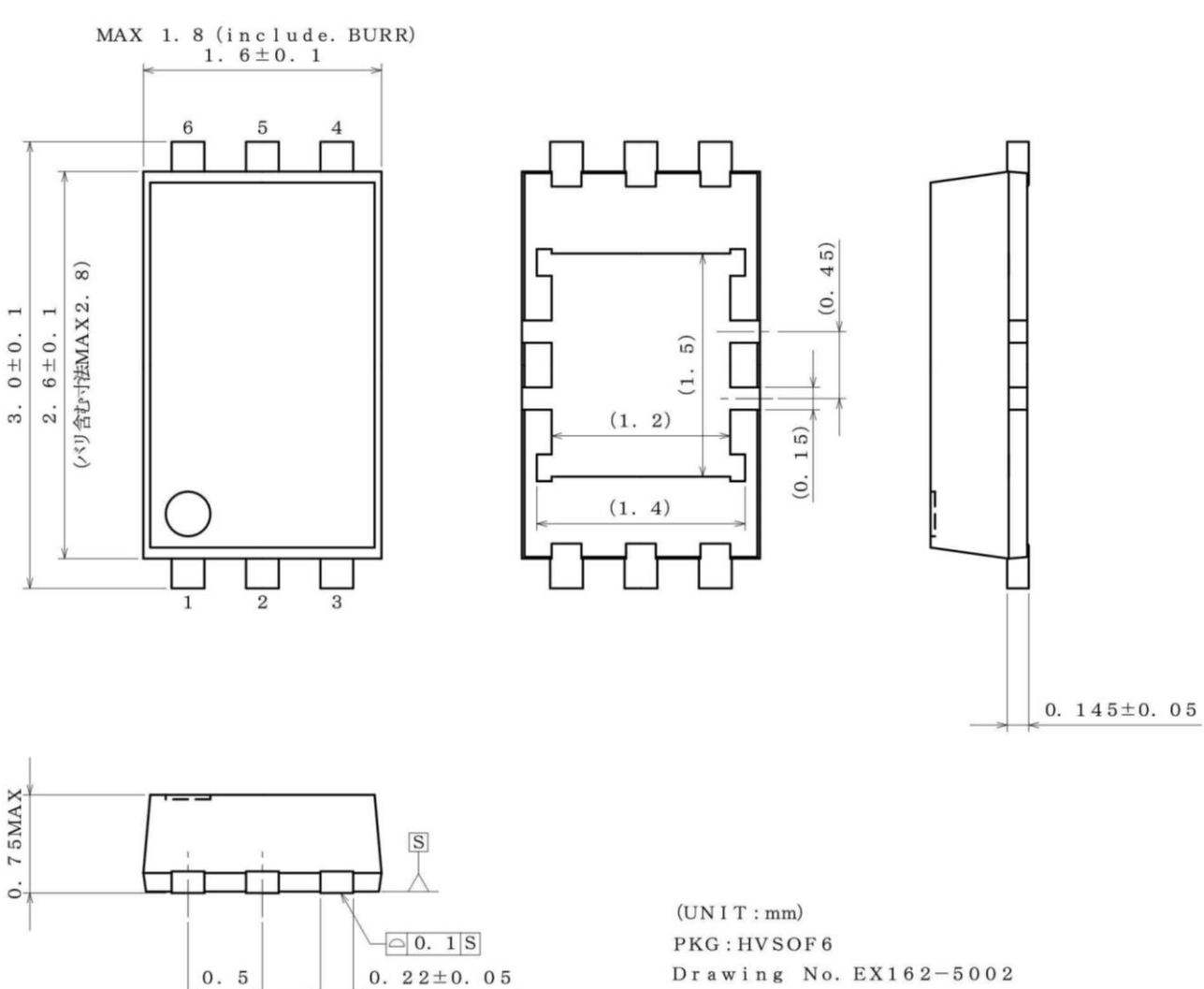
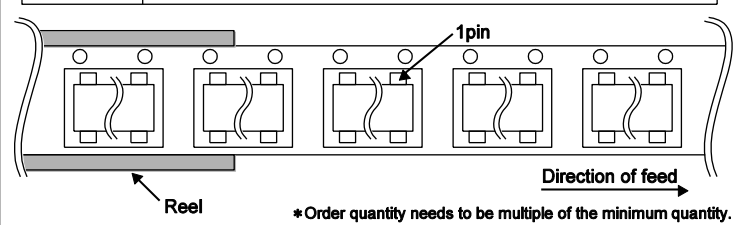
B D 3 5 0 7 H F V										-	T R		
Part Number										Package HFV: HVSO6			
Packaging and forming specification TR: Embossed tape and reel													

Marking Diagram

HVSO6 (TOP VIEW)



Physical Dimension, Tape and Reel Information

Package Name	HVSOF6						
 <p>(UNIT : mm) PKG : HVSOF6 Drawing No. EX162-5002</p>							
<p><Tape and Reel information></p> <table border="1"> <tr> <td>Tape</td><td>Embossed carrier tape</td></tr> <tr> <td>Quantity</td><td>3000pcs</td></tr> <tr> <td>Direction of feed</td><td>TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)</td></tr> </table>  <p>* Order quantity needs to be multiple of the minimum quantity.</p>		Tape	Embossed carrier tape	Quantity	3000pcs	Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)
Tape	Embossed carrier tape						
Quantity	3000pcs						
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)						

Revision History

Date	Revision	Changes
02.Nov.2015	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

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