

500-mA 3.3-V or 5.0-V Output LDO Regulators



BD4xxM5-C Series

General Description

The BD4xxM5 series are low quiescent regulators featuring 45 V absolute maximum voltage, and output voltage accuracy of $\pm 2\%$ (3.3 V or 5 V: Typ.), 500 mA output current and 38 μA (Typ.) current consumption. These regulators are therefore ideal for applications requiring a direct connection to the battery and a low current consumption. A logical "HIGH" at the CTL enables the device and "LOW" at the CTL disables the device. (Only W: Includes Enable Input). Ceramic capacitors can be used for compensation of the output capacitor phase. Furthermore, these ICs also feature overcurrent protection to protect the device from damage caused by short-circuiting and an integrated thermal shutdown to protect the device from overheating at overload conditions.

Features

- Qualified for Automotive Applications
- Wide Temperature Range (Tj): $-40\text{ }^{\circ}\text{C}$ to $+150\text{ }^{\circ}\text{C}$
- Wide Operating Input Range: 3.0 V to 42 V
- Low Quiescent Current: 38 μA (Typ.)
- Output Current: 500 mA
- High Output Voltage Accuracy: $\pm 2\%$
- Output Voltage: 3.3 V or 5.0 V (Typ.)
- Enable Input (Only W)
- Overload Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- AEC-Q100 Qualified (Note1)

(Note1: Grade1)

Package

W (Typ.) × D (Typ.) × H (Max.)

- FPJ: TO252-J5^(Note2) 6.60 mm × 10.10 mm × 2.38 mm



(Note2: TO252-J5 & TO252-J5F)

- FP: TO252-3 6.50 mm × 9.50 mm × 2.50 mm



- FP2: TO263-5^(Note3) 10.16 mm × 15.10 mm × 4.70 mm



(Note3: TO263-5 & TO263-5F)

- FP2: TO263-3^(Note4) 10.16 mm × 15.10 mm × 4.70 mm



(Note4: TO263-3 & TO263-3F)

Figure 1. Package Outlook

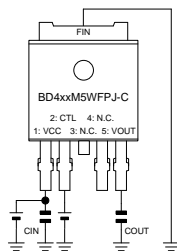
Applications

- Automotive (body, audio system, navigation system, etc.)

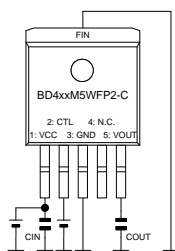
Typical Application Circuits

- Components Externally Connected: $0.1\text{ }\mu\text{F} \leq \text{CIN}$, $10\text{ }\mu\text{F} \leq \text{COUT}$ (Typ.)

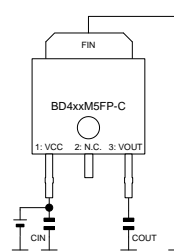
* Electrolytic, tantalum and ceramic capacitors can be used.



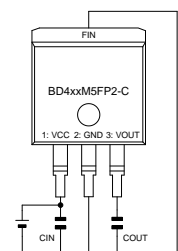
BD433 / 450M5WFPJ-C



BD433 / 450M5WFP2-C



BD433 / 450M5FP-C



BD433 / 450M5FP2-C

Figure 2. Typical Application Circuits

○Product structure: Silicon Monolithic Integrated Circuit ○This product is not designed protection against radioactive rays.

●Ordering Information

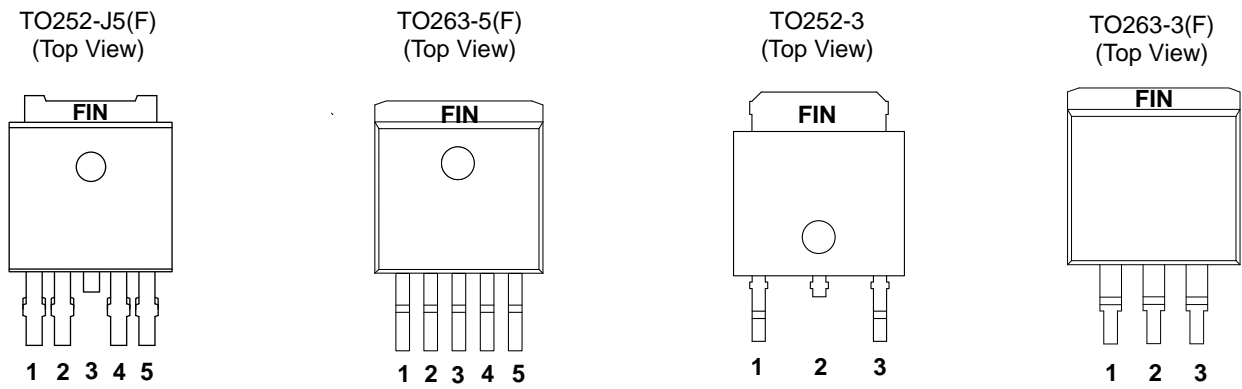
B D 4 x x M 5 W F P J										—	C Z E 2
Part Number		Output Voltage		Output Current		Enable Input		Package		Packaging and Forming Specification	
		33: 3.3 V 50: 5.0 V		5: 500 mA		W: Includes Enable Input		FPJ: TO252-J5(F) FP : TO252-3 FP2: TO263-5(F) TO263-3(F)		Z: Manufacturing Code E2: Embossed Tape and Reel	

●Lineup

Output Current Ability	Output Voltage (Typ.)	Enable Input ⁽¹⁾	Package Type	Orderable Part Number
500 mA	3.3 V	○	TO252-J5(F)	BD433M5WFPJ-CZE2
			TO263-5(F)	BD433M5WFP2-CZE2
		—	TO252-3	BD433M5FP-CE2
			TO263-3(F)	BD433M5FP2-CZE2
	5.0 V	○	TO252-J5(F)	BD450M5WFPJ-CZE2
			TO263-5(F)	BD450M5WFP2-CZE2
		—	TO252-3	BD450M5FP-CE2
			TO263-3(F)	BD450M5FP2-CZE2

(1) ○: Includes Enable Input
— : Not includes Enable Input

●Pin Configurations



●Pin Descriptions

■ BD433 / 450M5WFPJ-C

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	CTL	Output Control Pin
3	GND	Ground Pin
4	N.C.	Not Connected
5	VOUT	Output Pin
6 (FIN)	GND	Ground Pin

■BD433 / 450M5WFP2-C

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	CTL	Output Control Pin
3	GND	Ground Pin
4	N.C.	Not Connected
5	VOUT	Output Pin
6 (FIN)	GND	Ground Pin

■ BD433 / 450M5FP-C

Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	N.C.	Not Connected
3	VOUT	Output Pin
4 (FIN)	GND	Ground Pin

■BD433 / 450M5FP2-C

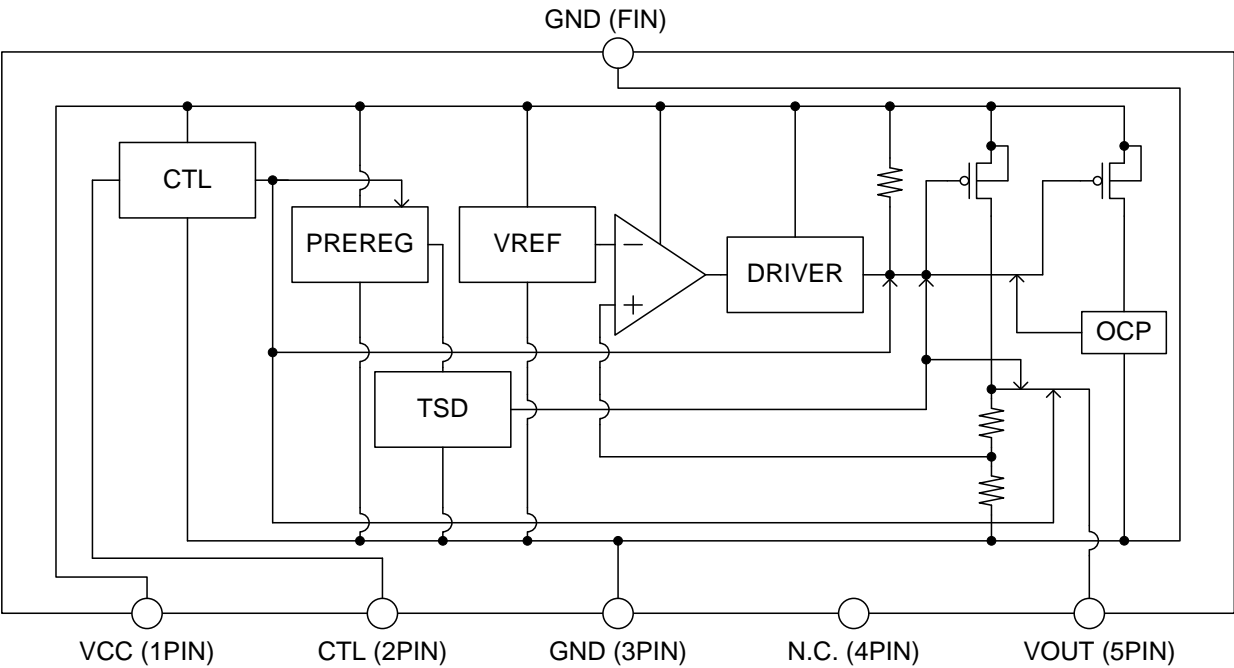
Pin No.	Pin Name	Function
1	VCC	Supply Voltage Input Pin
2	GND	Ground Pin
3	VOUT	Output Pin
4 (FIN)	GND	Ground Pin

* N.C. Pin is recommended to short with GND.

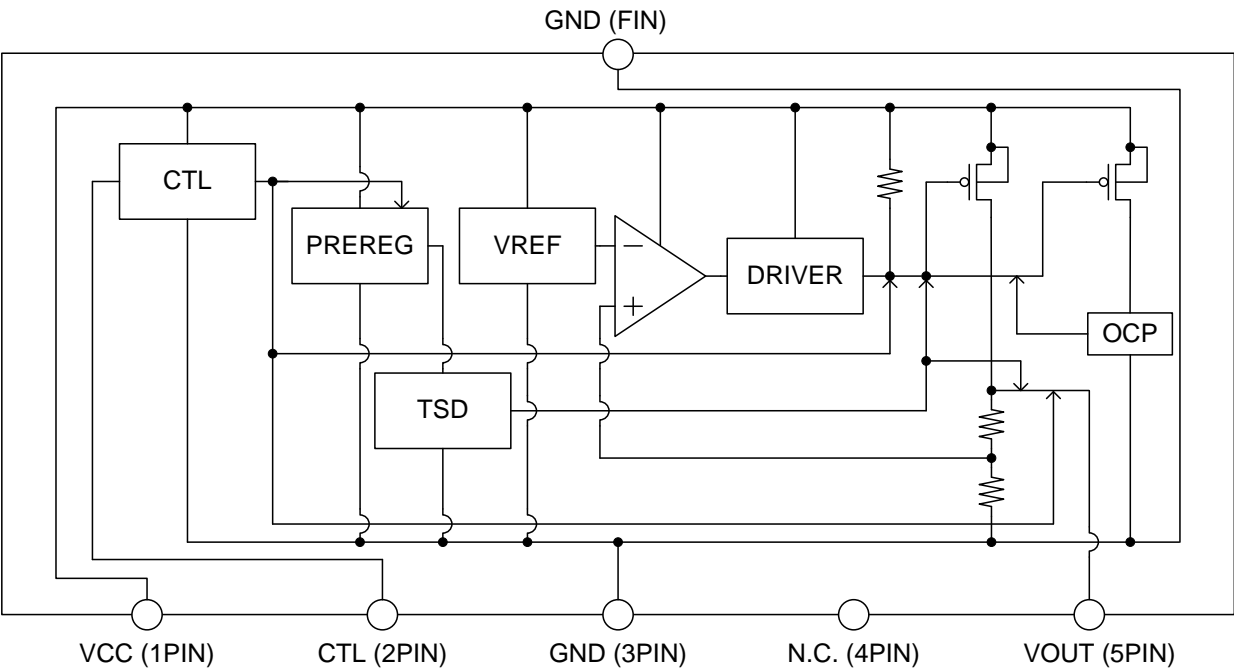
* N.C. Pin can be open because it isn't connected it inside of IC.

●Block Diagrams

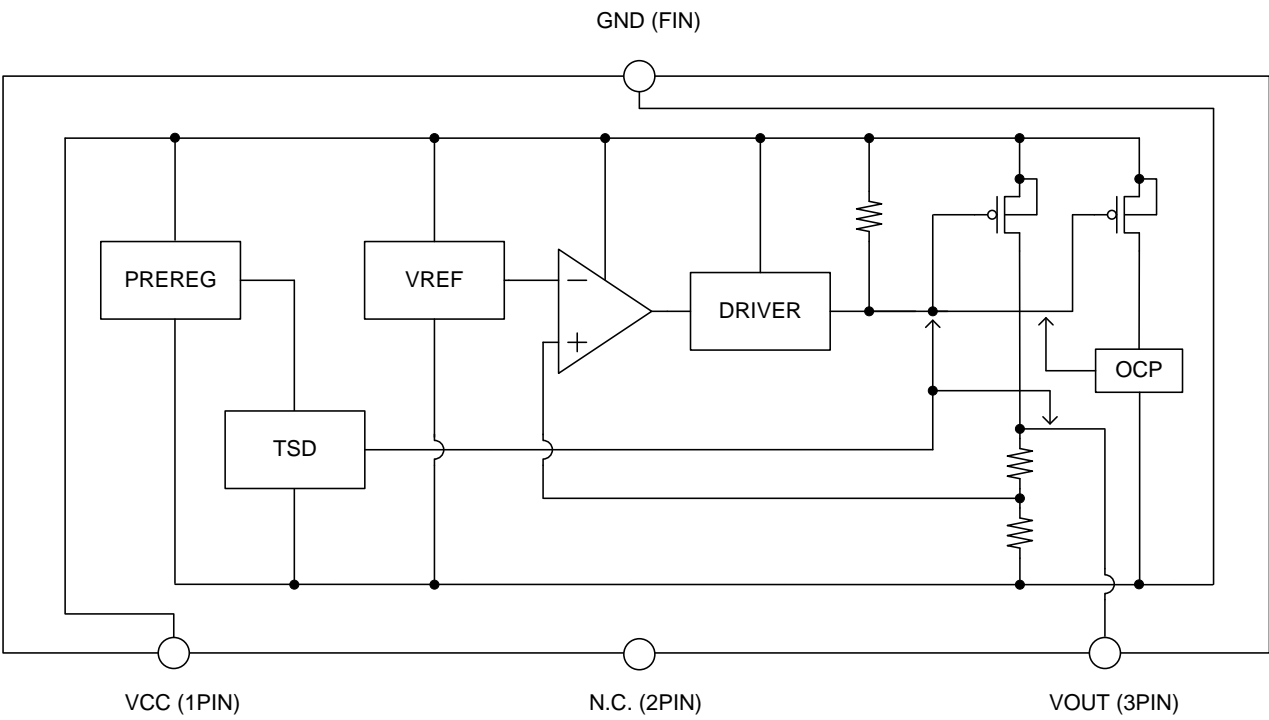
■ BD433 / 450M5WFPJ-C



■ BD433 / 450M5WFP2-C



■ BD433 / 450M5FP-C



■ BD433 / 450M5FP2-C

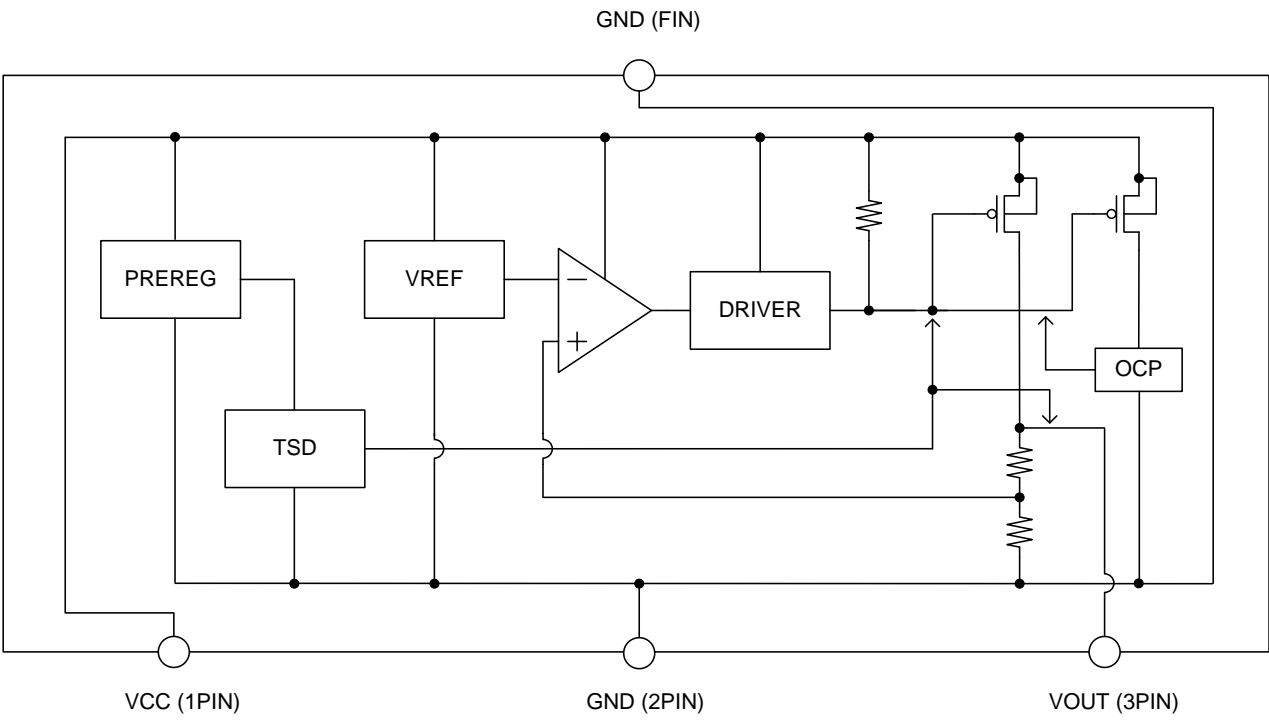


Figure 4. Block Diagrams

●Description of Blocks

Block Name	Function	Description of Blocks
CTL ⁽¹⁾	Control Output Voltage ON/OFF	A logical "HIGH" ($\geq 2.8\text{ V}$) at the CTL enables the device and "LOW" ($\leq 0.8\text{ V}$) at the CTL disable the device.
PREREG	Internal Power Supply	Power Supply for Internal Circuit
TSD	Thermal Shutdown Protection	To protect the device from overheating. If the chip temperature (T_j) reaches ca. $175\text{ }^{\circ}\text{C}$ (Typ.), the output is turned off.
VREF	Reference Voltage	Generate the Reference Voltage
DRIVER	Output MOS FET Driver	Drive the Output MOS FET
OCP	Over Current Protection	To protect the device from damage caused by over current. If the output current reaches ca. 900 mA (Typ.), the output is turned off.

(1) Applicable for product with Enable Input.

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage ⁽¹⁾	VCC	-0.3 to +45.0	V
Output Control Voltage ⁽²⁾	CTL	-0.3 to +45.0	V
Output Voltage	VOUT	-0.3 to +8.0	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
ESD withstand Voltage (HBM) ⁽³⁾	V _{ESD, HBM}	±2000	V

(1) Do not exceed Pd.

(2) Applicable for product with Enable Input.
The start-up orders of power supply (VCC) and the CTL do not influence if the voltage is within the operation power supply voltage range.

(3) ESD susceptibility Human Body Model "HBM".

●Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage (IOUT ≤ 500 mA) ⁽¹⁾	VCC	5.9	42.0	V
Supply Voltage (IOUT ≤ 250 mA) ⁽¹⁾	VCC	5.5	42.0	V
Supply Voltage (IOUT ≤ 500 mA) ⁽²⁾	VCC	4.6	42.0	V
Supply Voltage (IOUT ≤ 250 mA) ⁽²⁾	VCC	4.0	42.0	V
Output Control Voltage ⁽³⁾	CTL	0	42.0	V
Start-Up Voltage ⁽⁴⁾	VCC	3.0	–	V
Output Current	IOUT	0	500	mA
Junction Temperature Range	Tj	-40	+150	°C

(1) BD450M5WFPJ-C / BD450M5WFP2-C / BD450M5FP-C / BD450M5FP2-C

(2) BD433M5WFPJ-C / BD433M5WFP2-C / BD433M5FP-C / BD433M5FP2-C

(3) Applicable for Product with Enable Input.

(4) When IOUT = 0 mA

Notice: Please consider that the output voltage would be dropped (Dropout voltage) according to the output current.

● Thermal Impedance ⁽¹⁾

Parameter	Symbol	Typ.	Unit	Conditions
TO252-J5(F) / TO252-3				
Junction to Ambient	θ_{JA}	136	°C / W	1s ⁽²⁾
		23	°C / W	2s2p ⁽³⁾
Junction to Top Center of Case ⁽⁴⁾	Ψ_{JT}	17	°C / W	1s ⁽²⁾
		3	°C / W	2s2p ⁽³⁾
TO263-5(F) / TO263-3(F)				
Junction to Ambient	θ_{JA}	81	°C / W	1s ⁽²⁾
		21	°C / W	2s2p ⁽³⁾
Junction to Top Center of Case ⁽⁴⁾	Ψ_{JT}	8	°C / W	1s ⁽²⁾
		2	°C / W	2s2p ⁽³⁾

(1) The thermal impedance is based on JESD51 - 2A (Still-Air) standard.

(2) JESD51 - 3 standard FR4 114.3 mm × 76.2 mm × 1.57 mm 1-layer (1s)

(Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.)

(3) JESD51 -5 / -7 standard FR4 114.3 mm × 76.2 mm × 1.60 mm 4-layer (2s2p)

(Top copper foil: ROHM recommended footprint + wiring to measure / 2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, copper (top & reverse side / inner layers) 2oz. / 1oz.)

(4) T_T : Top center of case's (mold) temperature

●Electrical Characteristics

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$
 The typical value is defined at $T_j = 25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Shut Down Current	Ishut ⁽¹⁾	–	2.0	5.0	μA	$CTL = 0\text{ V}$ $T_j \leq 125\text{ }^{\circ}\text{C}$
Circuit Current	Icc	–	38	95	μA	$I_{OUT} = 0\text{ mA}$ $T_j \leq 125\text{ }^{\circ}\text{C}$
		–	38	175	μA	$I_{OUT} \leq 500\text{ mA}$ $T_j \leq 150\text{ }^{\circ}\text{C}$
Output Voltage	VOUT ⁽²⁾	4.90	5.00	5.10	V	$6\text{ V} \leq V_{CC} \leq 42\text{ V}$, $0\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$
		4.80	5.00	5.10	V	$6\text{ V} \leq V_{CC} \leq 42\text{ V}$ $0\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$
	VOUT ⁽³⁾	3.23	3.30	3.37	V	$6\text{ V} \leq V_{CC} \leq 42\text{ V}$ $0\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$
		3.20	3.30	3.37	V	$6\text{ V} \leq V_{CC} \leq 42\text{ V}$ $0\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$
Dropout Voltage	ΔV_d ⁽²⁾	–	0.20	0.50	V	$V_{CC} = V_{OUT} \times 0.95$ (Typ. 4.75 V) $I_{OUT} = 300\text{ mA}$
	ΔV_d ⁽³⁾	–	0.25	0.75	V	$V_{CC} = V_{OUT} \times 0.95$ (Typ. 3.135 V) $I_{OUT} = 300\text{ mA}$
Ripple Rejection	R.R.	55	60	–	dB	$f = 120\text{ Hz}$, $e_{in} = 1\text{ V}_{rms}$ $I_{OUT} = 100\text{ mA}$
Line Regulation	Reg.I	–	10	30	mV	$8\text{ V} \leq V_{CC} \leq 16\text{ V}$
Load Regulation	Reg.L	–	10	30	mV	$10\text{ mA} \leq I_{OUT} \leq 400\text{ mA}$
Thermal Shut Down	TSD	–	175	–	$^{\circ}\text{C}$	T_j at TSD ON

(1) Applicable for Product with Enable Input.

(2) For BD450M5WFPJ-C / BD450M5WFP2-C / BD450M5FP-C / BD450M5FP2-C

(3) For BD433M5WFPJ-C / BD433M5WFP2-C / BD433M5FP-C / BD433M5FP2-C

●Electrical Characteristics (Enable function * Applicable for product with Enable Input.)

Unless otherwise specified, $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$. The typical value is defined at $T_j = 25\text{ }^{\circ}\text{C}$.

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
CTL ON Mode Voltage	VthH	2.8	–	–	V	Active Mode
CTL OFF Mode Voltage	VthL	–	–	0.8	V	Off Mode
CTL Bias Current	ICTL	–	15	30	μA	$CTL = 5\text{ V}$

Typical Performance Curves

■BD433M5WFPJ-C / BD433M5WFP2-C / BD433M5FP-C / BD433M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$.

(1) Applicable for Product with Enable Input.

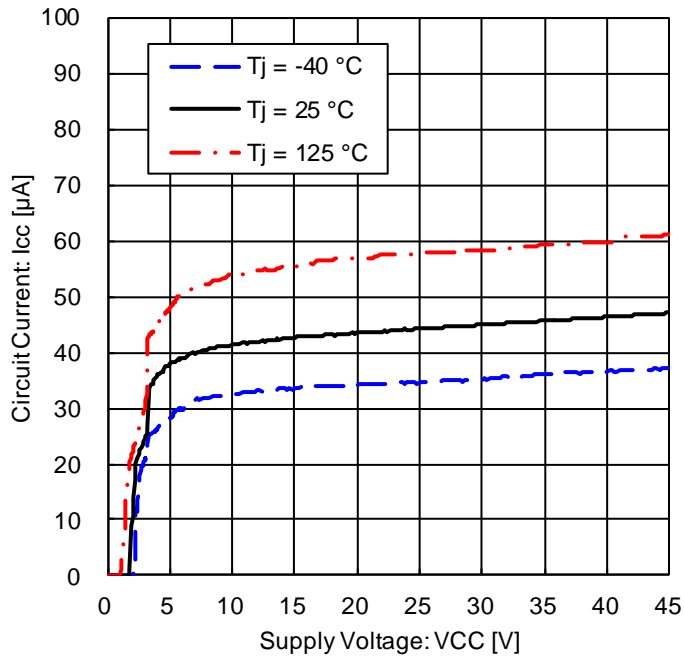


Figure 5. Circuit Current vs. Power Supply Voltage

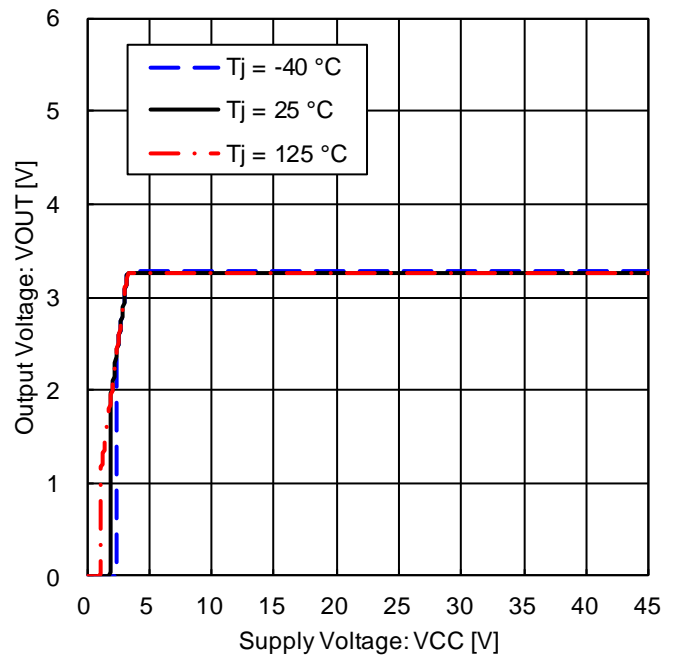


Figure 6. Output Voltage vs. Power Supply Voltage ($I_{OUT} = 0\text{ mA}$)

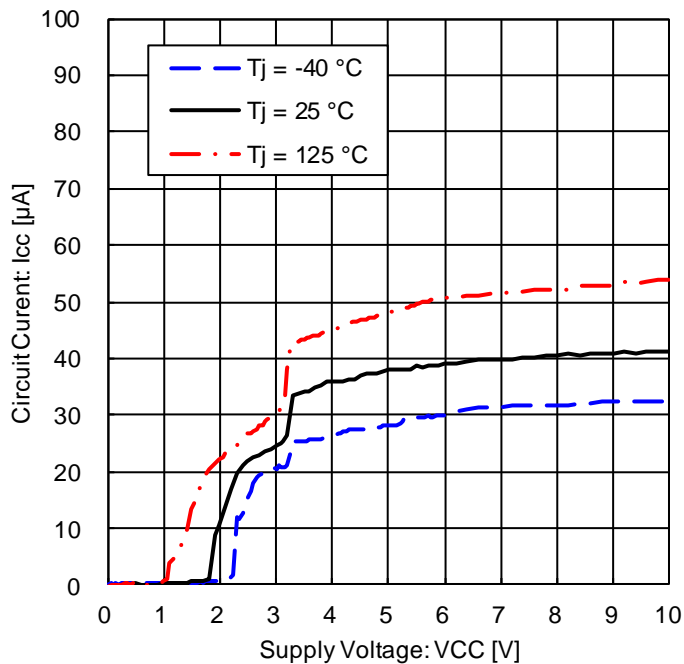


Figure 7. Circuit Current vs. Power Supply Voltage
*Magnified Figure 5. at low supply voltage

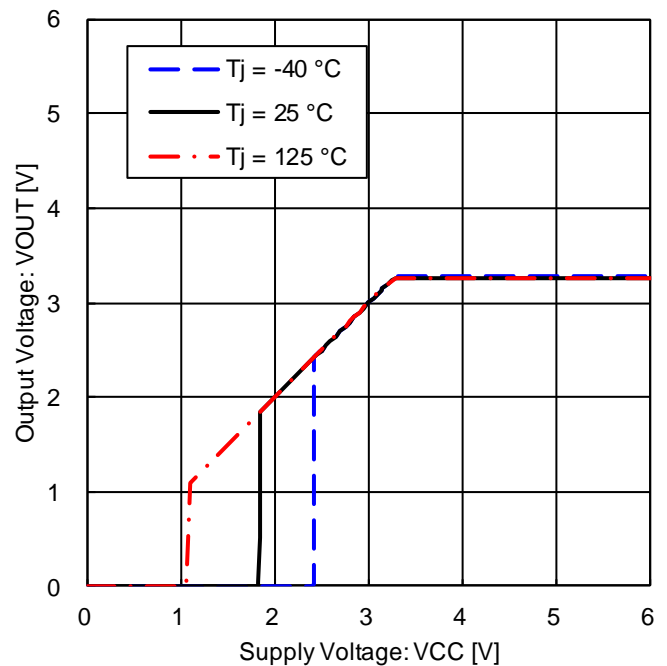


Figure 8. Output voltage vs. Power Supply Voltage ($I_{OUT} = 0\text{ mA}$)
* Magnified Figure 6. at Low Supply Voltage

Typical Performance Curves

■ BD433M5WFPJ-C / BD433M5WFP2-C / BD433M5FP-C / BD433M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$.

(1) Applicable for Product with Enable Input.

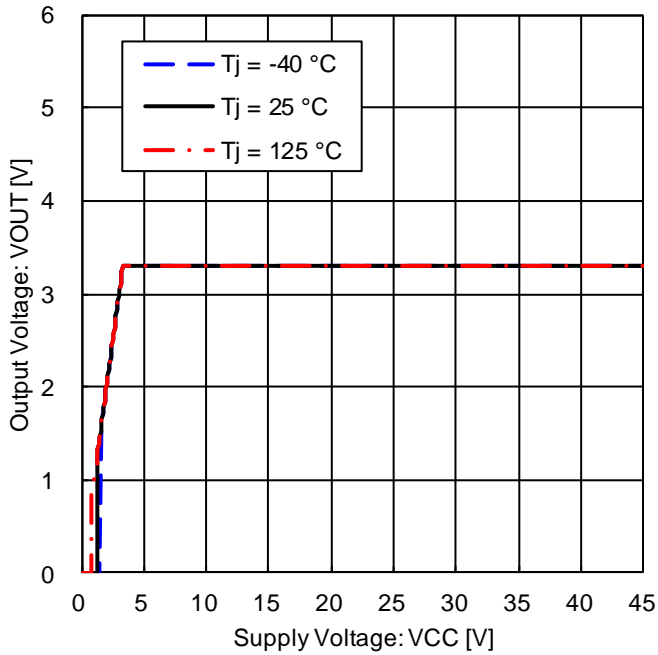


Figure 9. Output Voltage vs. Power Supply Voltage ($I_{OUT} = 10\text{ mA}$)

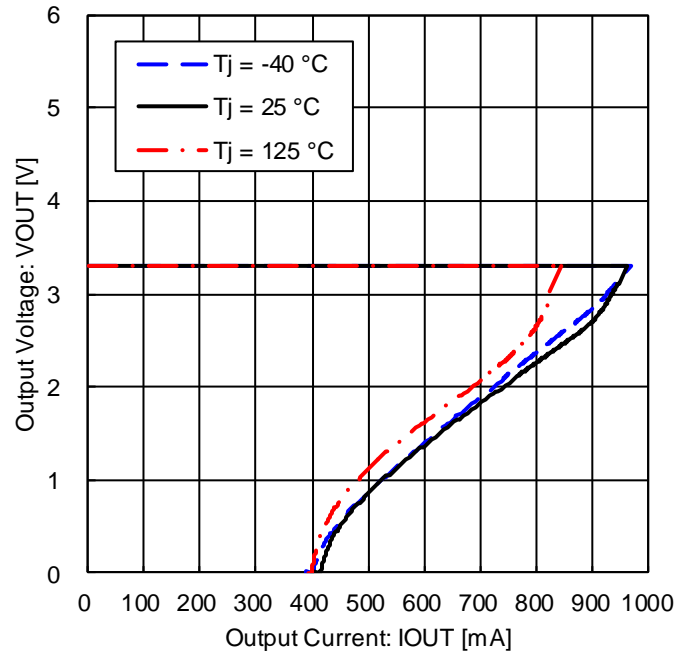


Figure 10. Output Voltage vs. Load (Over Current Protection)

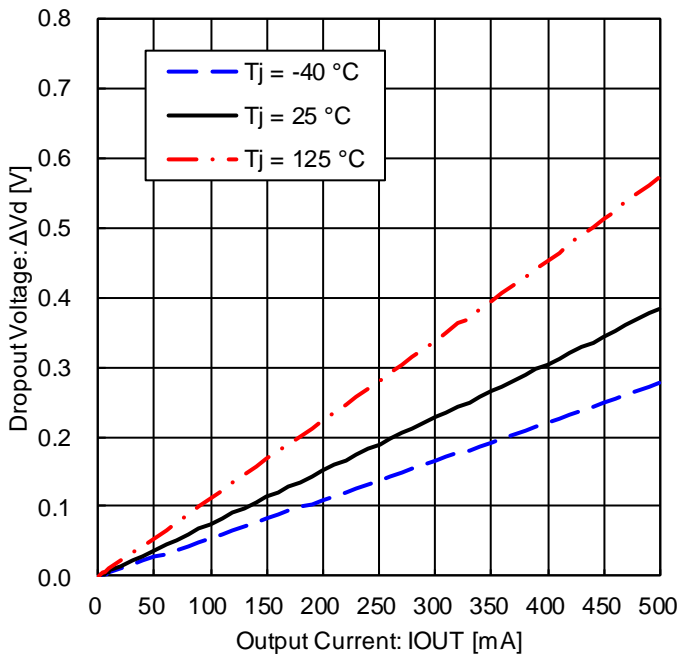


Figure 11. Dropout Voltage ($V_{CC} = 3.135\text{ V}$)

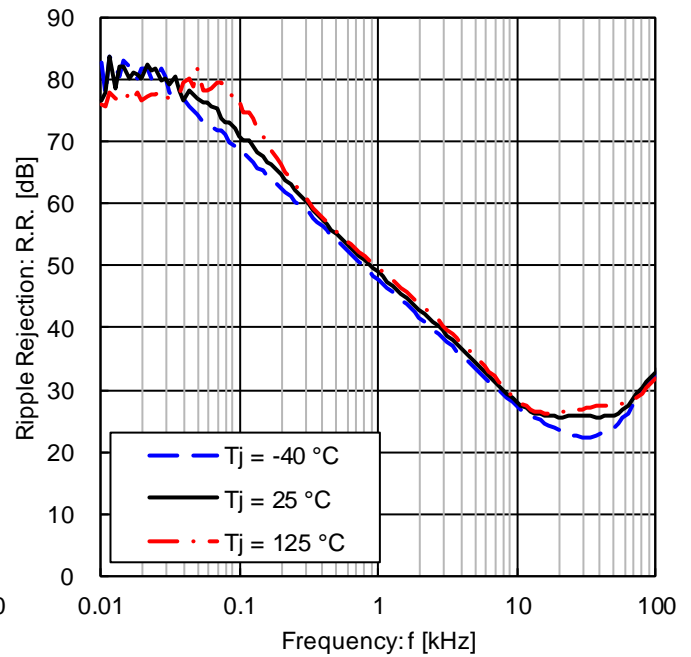


Figure 12. Ripple Rejection ($e_{in} = 1\text{ V}_{rms}$, $I_{OUT} = 100\text{ mA}$)

● Typical Performance Curves

■ BD433M5WFPJ-C / BD433M5WFP2-C / BD433M5FP-C / BD433M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$.

(1) Applicable for Product with Enable Input.

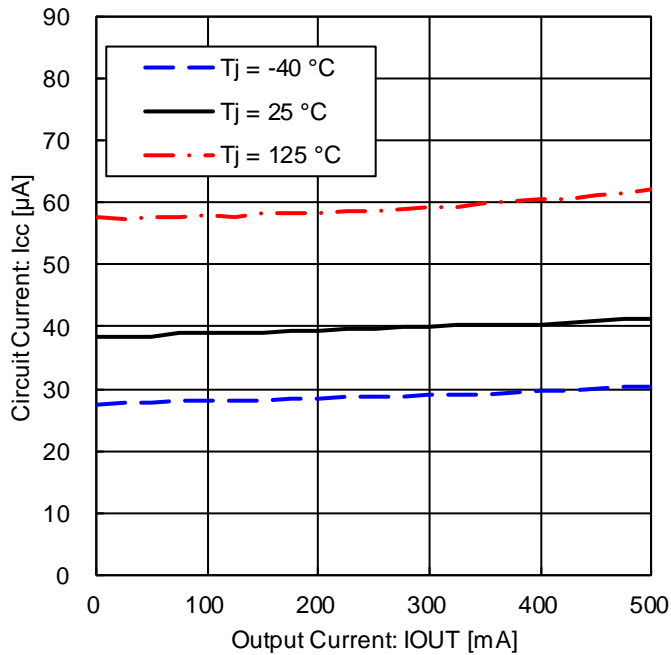


Figure 13. Circuit Current vs. Output Current

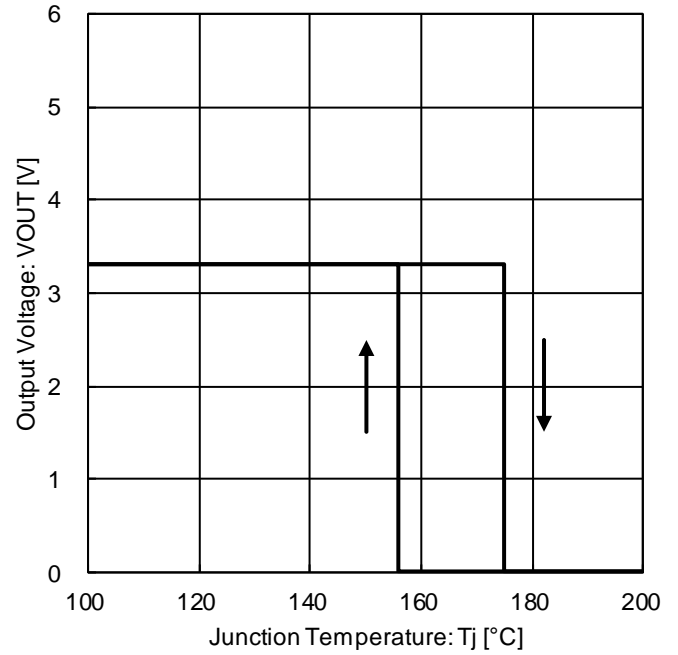


Figure 14. Output Voltage vs. Temperature (Thermal Shut Down)

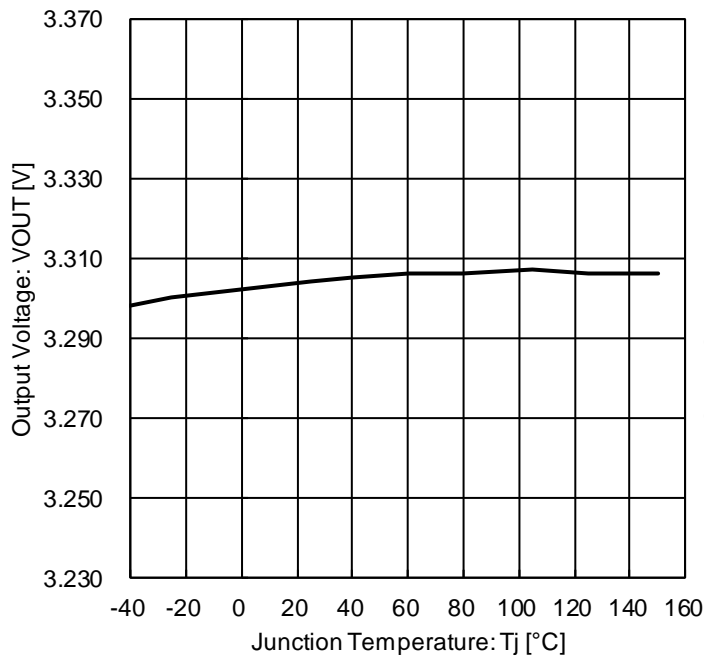


Figure 15. Output Voltage vs. Temperature

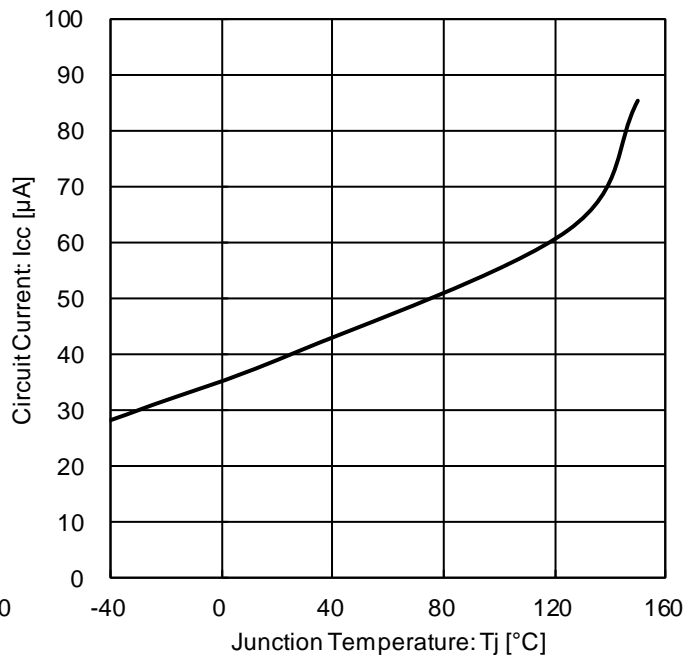


Figure 16. Circuit Current vs. Temperature

Typical Performance Curves

■BD433M5WFPJ-C / BD433M5WFP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$

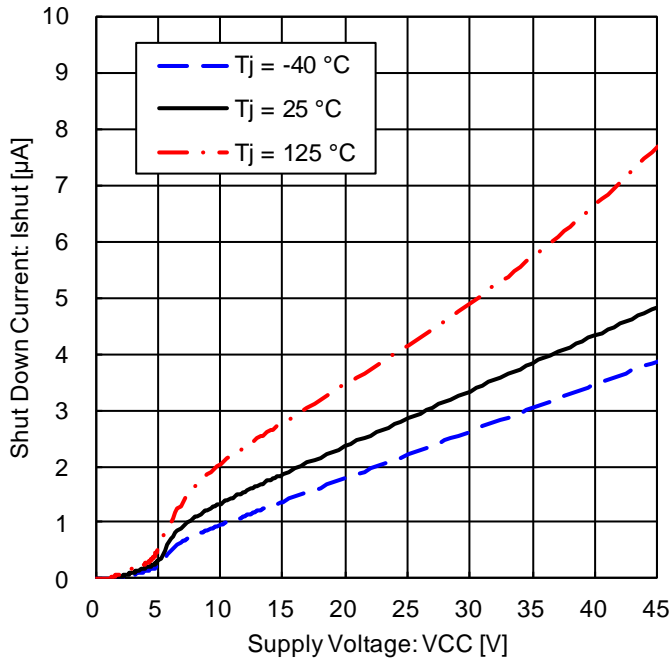


Figure 17. Shut Down Current vs. Power Supply Voltage (CTL = 0 V)

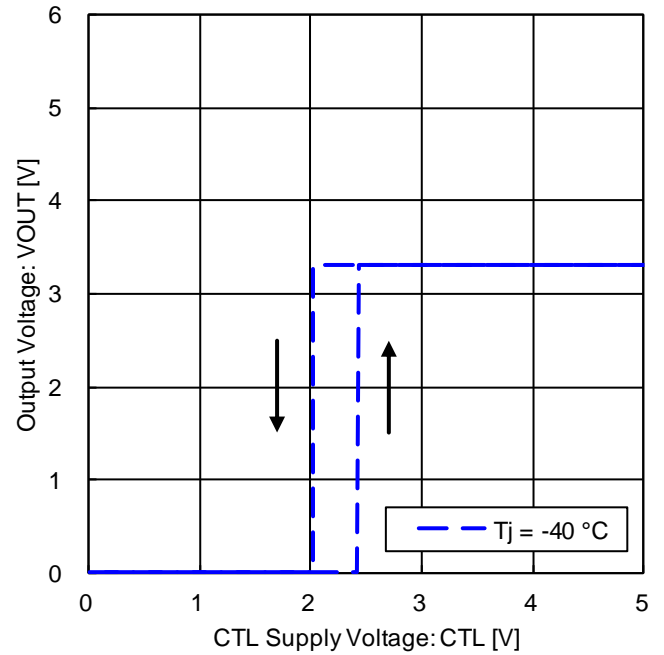


Figure 18. CTL ON / OFF Mode Voltage ($T_j = -40\text{ }^{\circ}\text{C}$)

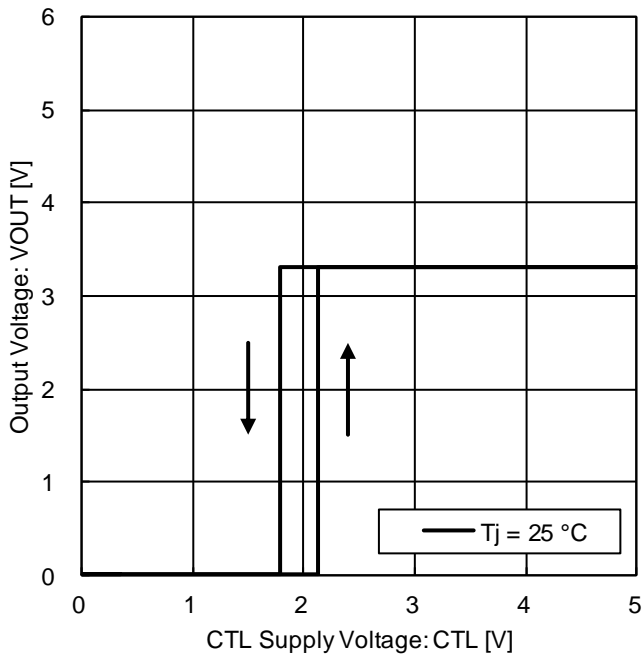


Figure 19. CTL ON / OFF Mode Voltage ($T_j = 25\text{ }^{\circ}\text{C}$)

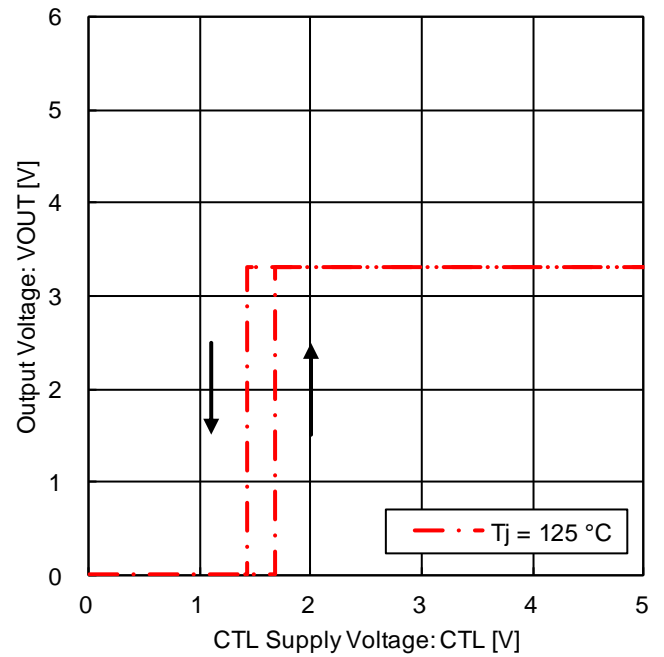


Figure 20. CTL ON / OFF Mode Voltage ($T_j = 125\text{ }^{\circ}\text{C}$)

●Typical Performance Curves

■BD433M5WFPJ-C / BD433M5WFP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$

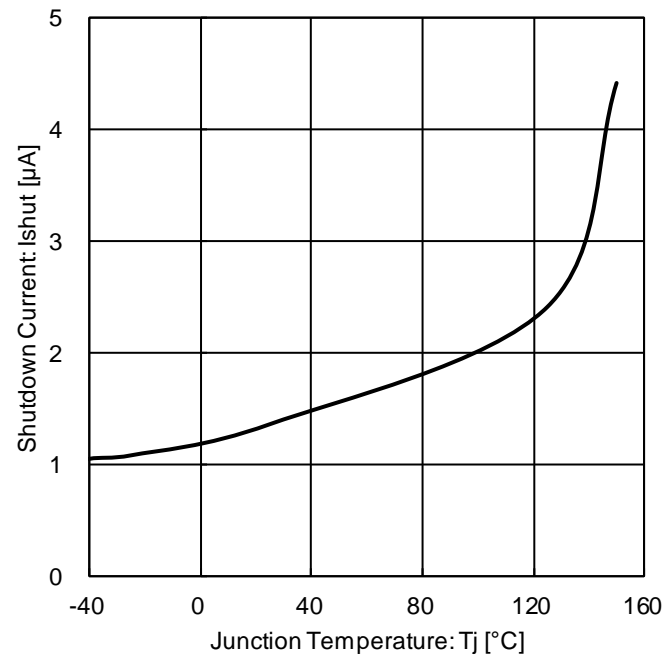


Figure 21. Shut Down Current
(CTL = 0 V)

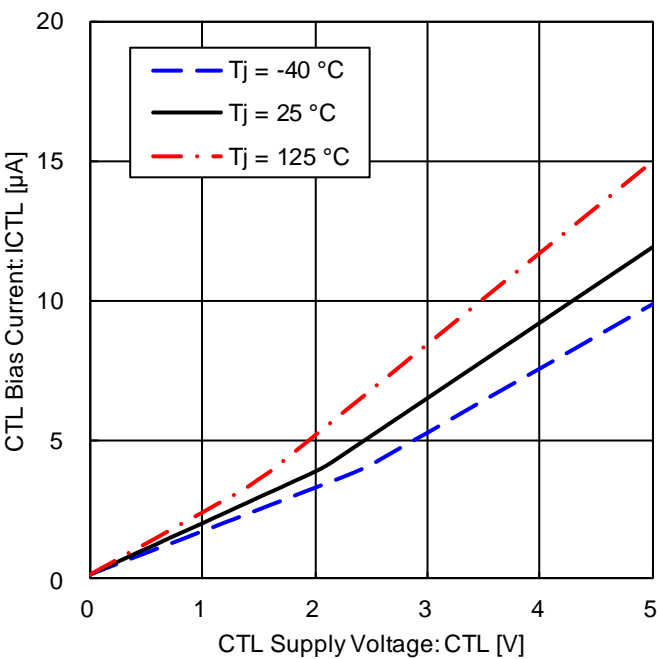


Figure 22. CTL Bias Current vs. CTL Supply Voltage

Typical Performance Curves

■BD450M5WFPJ-C / BD450M5WFP2-C / BD450M5FP-C/BD450M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$

(1) Applicable for Product with Enable Input.

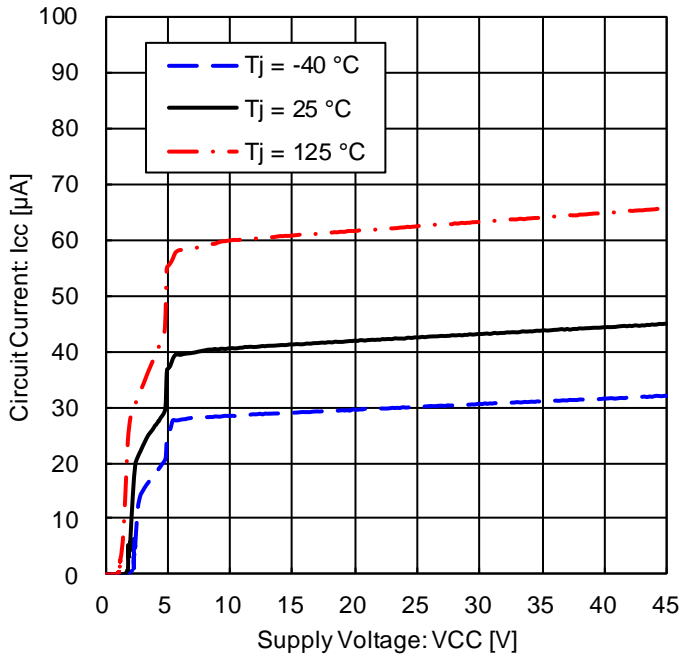


Figure 23. Circuit Current vs. Power Supply Voltage

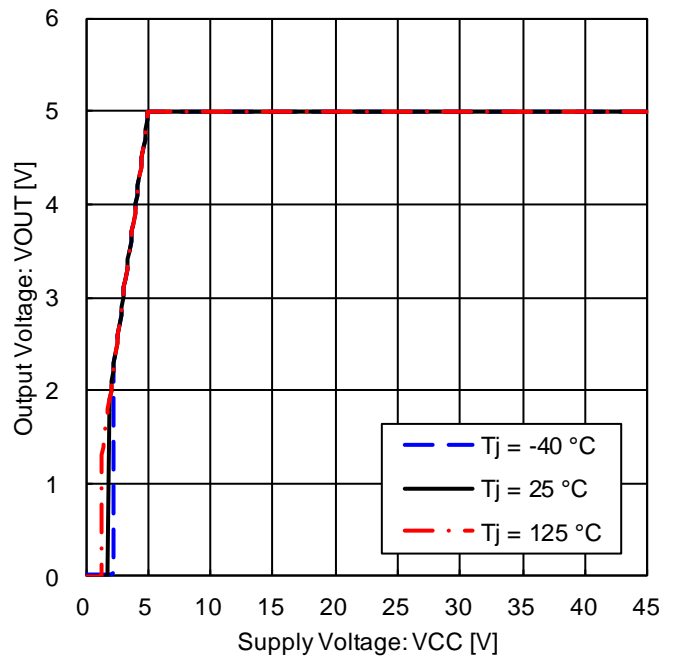


Figure 24. Output Voltage vs. Power Supply Voltage
($I_{OUT} = 0\text{ mA}$)

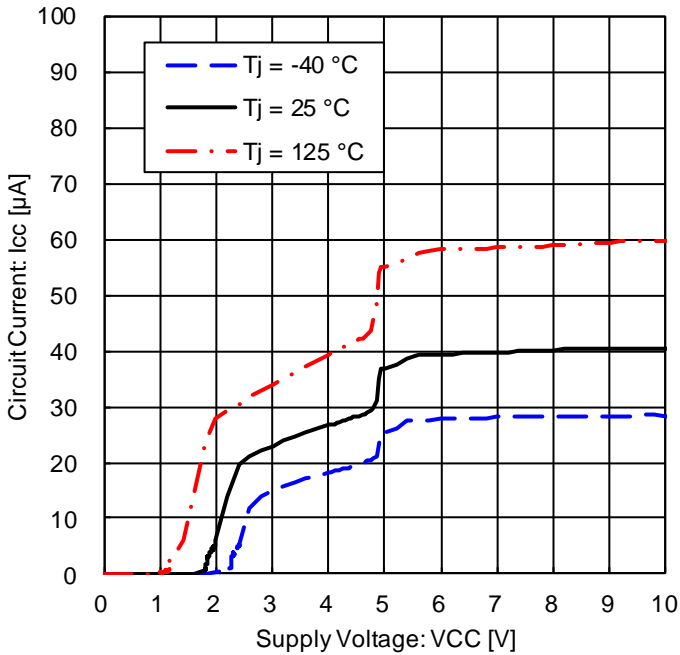


Figure 25. Circuit Current vs. Power Supply Voltage
*Magnified Figure 23. at low supply voltage

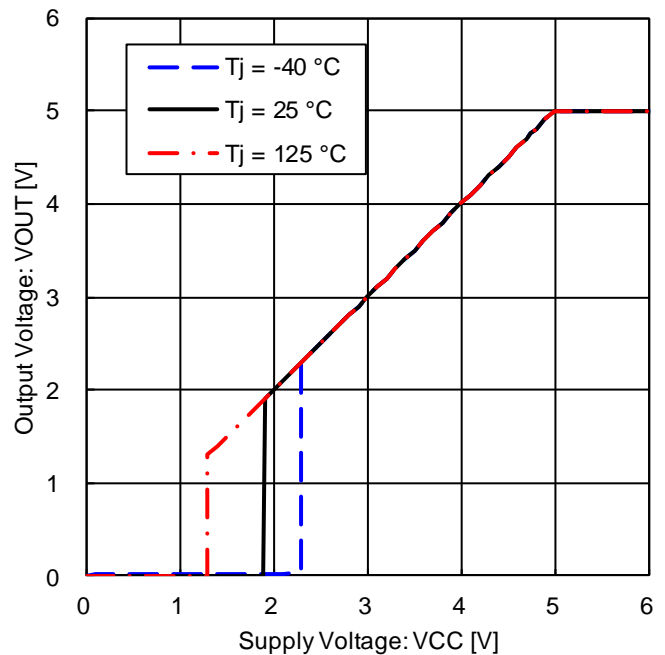


Figure 26. Output Voltage vs. Power Supply Voltage
($I_{OUT} = 0\text{ mA}$)
*Magnified Figure 24. at low supply voltage

Typical Performance Curves

■ BD450M5WFPJ-C / BD450M5WFP2-C / BD450M5FP-C / BD450M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$

(1) Applicable for Product with Enable Switch.

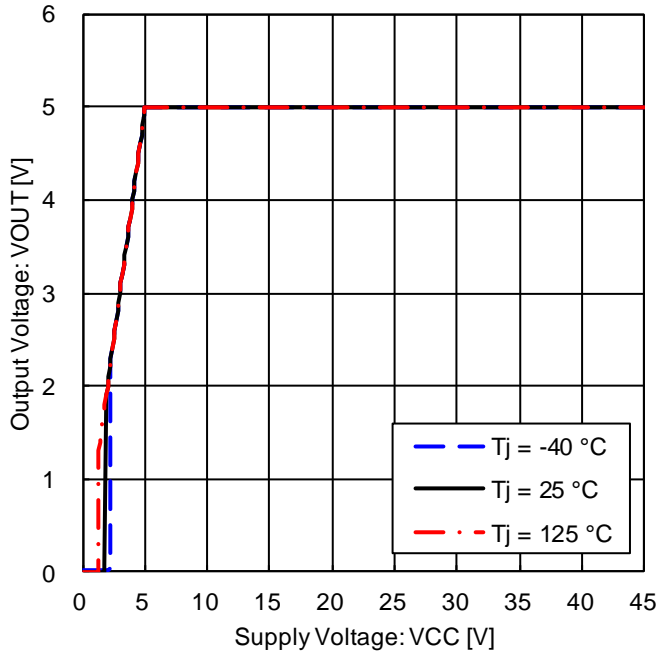


Figure 27. Output Voltage vs. Power Supply Voltage ($I_{OUT} = 10\text{ mA}$)

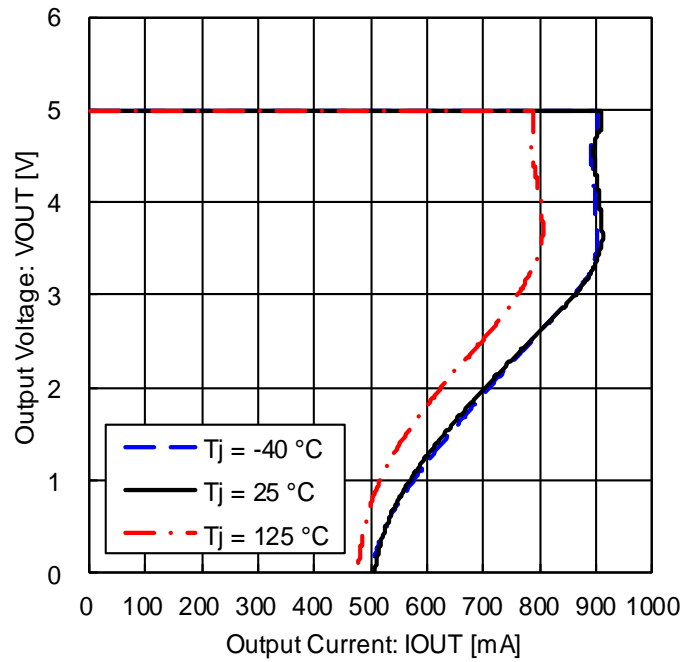


Figure 28. Output Voltage vs. Output Current (Over Current Protection)

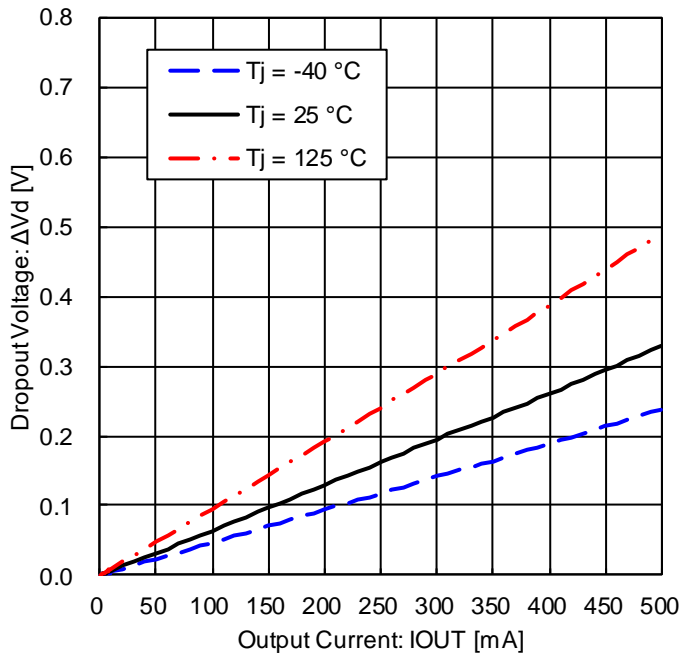


Figure 29. Dropout Voltage ($V_{CC}=4.75\text{ V}$)

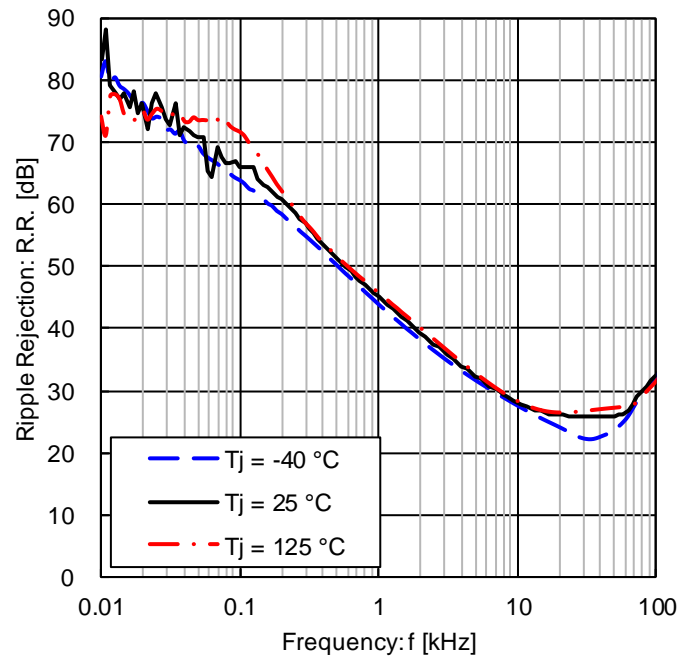


Figure 30. Ripple Rejection ($e_{in} = 1\text{ Vrms}$, $I_{OUT} = 100\text{ mA}$)

● Typical Performance Curves

■ BD450M5WFPJ-C / BD450M5WFP2-C / BD450M5WFP2-C / BD450M5FP-C / BD450M5FP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $CTL = 5\text{ V}^{(1)}$, $I_{OUT} = 0\text{ mA}$

(1) Applicable for Product with Enable Input.

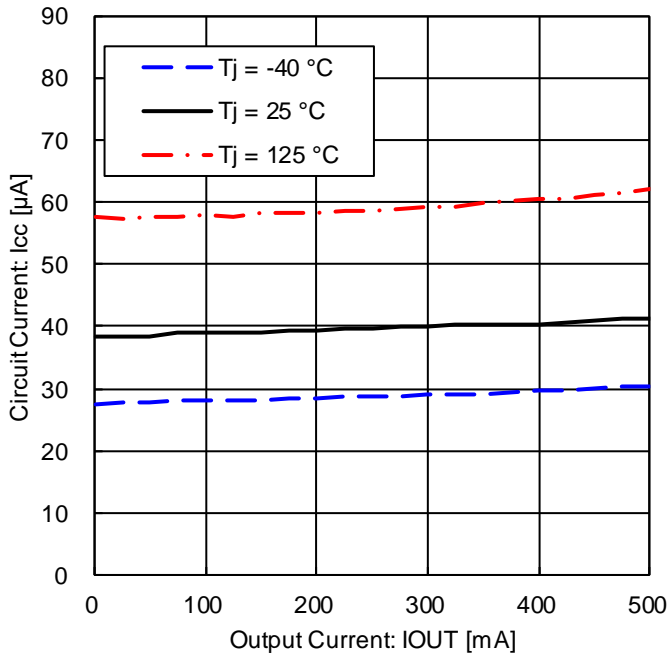


Figure 31. Circuit Current vs. Output Current

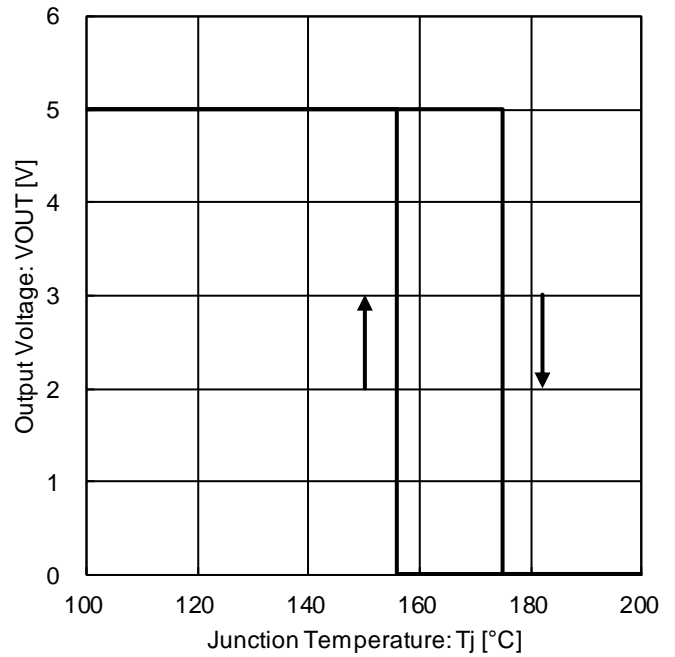


Figure 32. Output Voltage vs. Temperature (Thermal Shut Down)

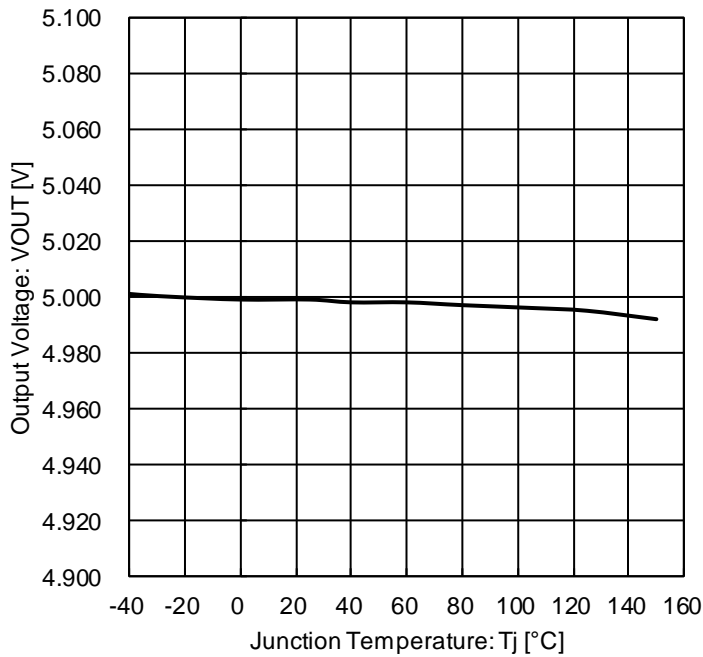


Figure 33. Output Voltage vs. Temperature

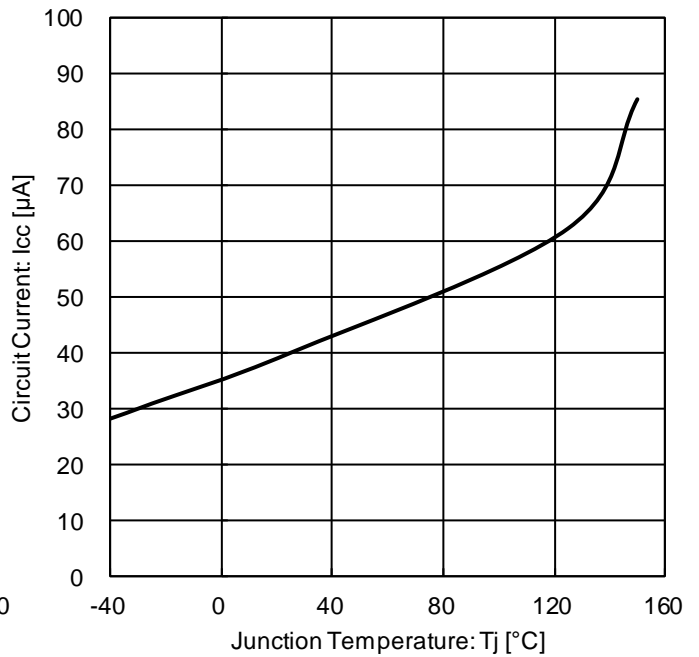


Figure 34. Circuit Current vs. Temperature

Typical Performance Curves

■BD450M5WFPJ-C / BD450M5WFP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$

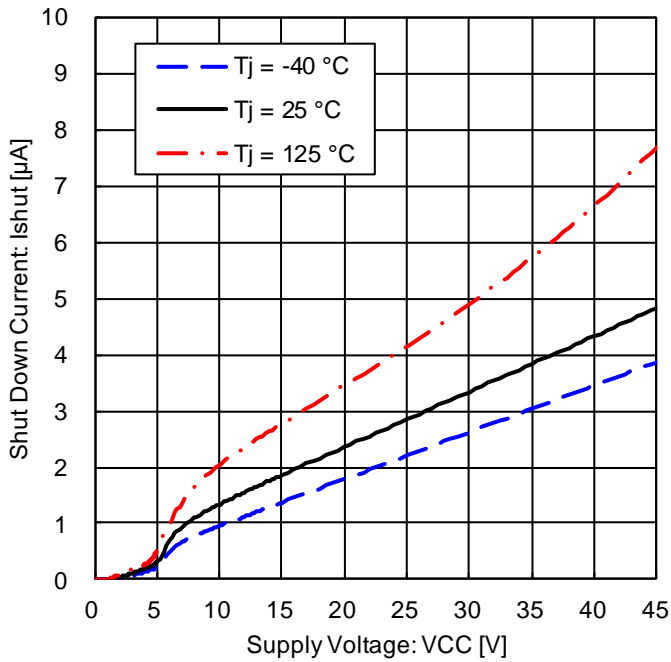


Figure 35. Shut Down Current vs. Power Supply Voltage
(CTL = 0 V)

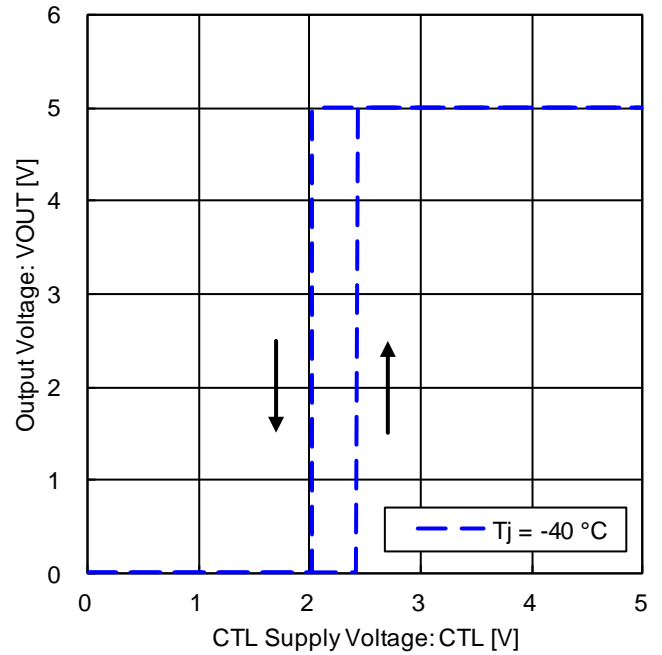


Figure 36. CTL ON / OFF Mode Voltage
($T_j = -40\text{ }^{\circ}\text{C}$)

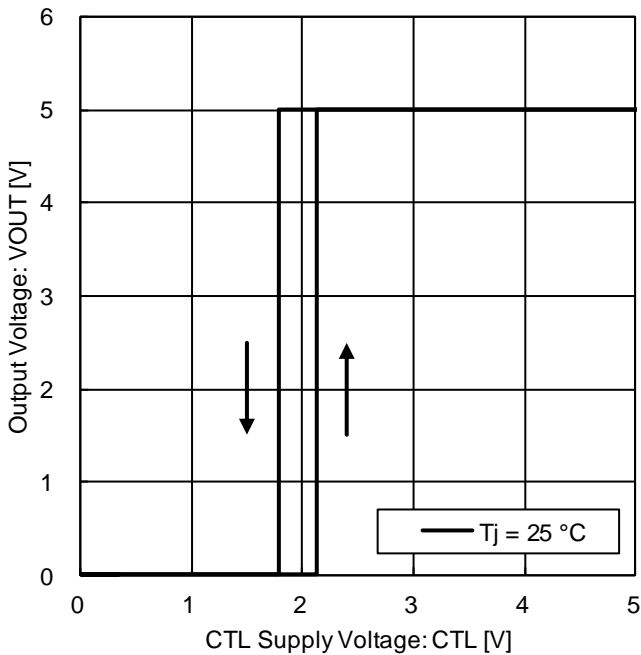


Figure 37. CTL ON / OFF Mode Voltage
($T_j = 25\text{ }^{\circ}\text{C}$)

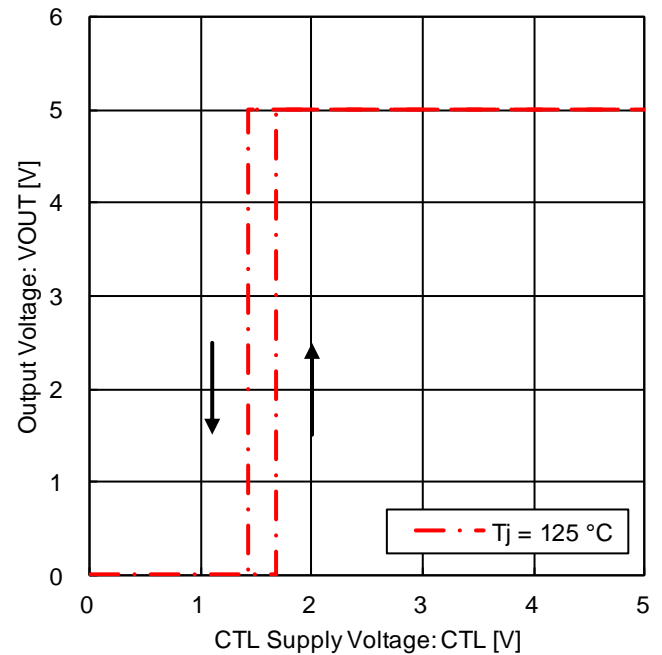


Figure 38. CTL ON / OFF Mode Voltage
($T_j = 125\text{ }^{\circ}\text{C}$)

●Typical Performance Curves
■BD450M5WFPJ-C / BD450M5WFP2-C Reference Data

Unless otherwise specified: $-40\text{ }^{\circ}\text{C} \leq T_j \leq +150\text{ }^{\circ}\text{C}$, $V_{CC} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$

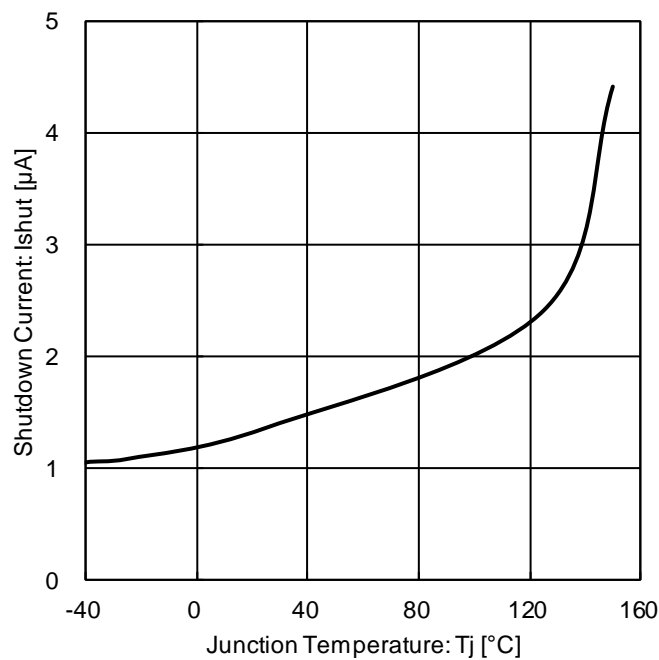


Figure 39. Shut Down Current vs. Temperature
(CTL = 0 V)

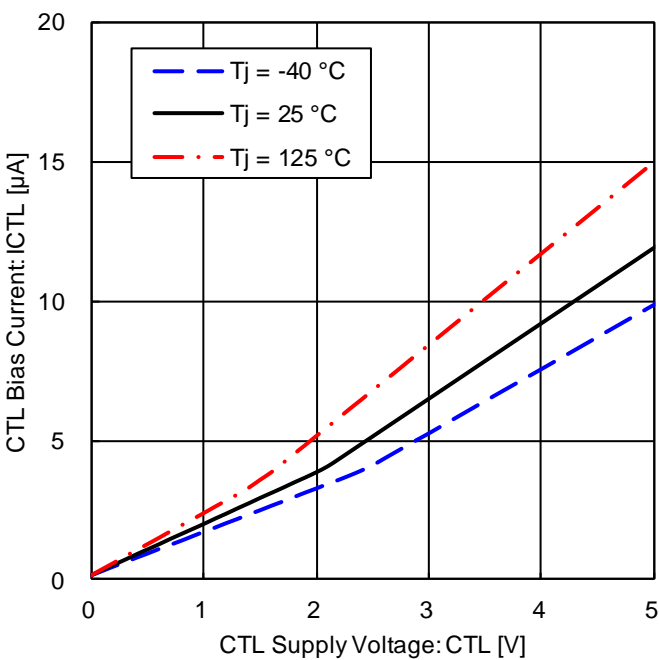
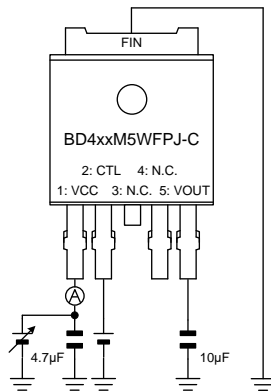
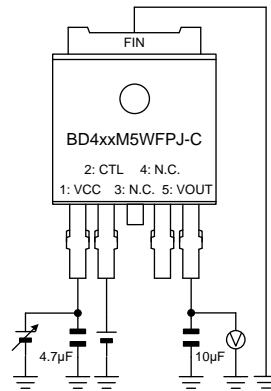


Figure 40. CTL Bias Current vs. CTL Supply Voltage

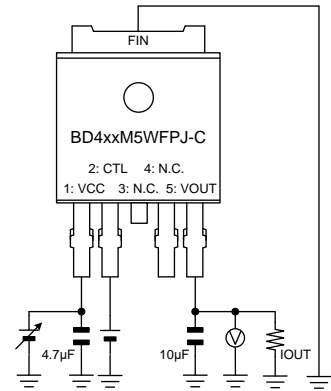
● Measurement Circuit for Typical Performance Curves (BD433 / 450M5WFPJ-C)



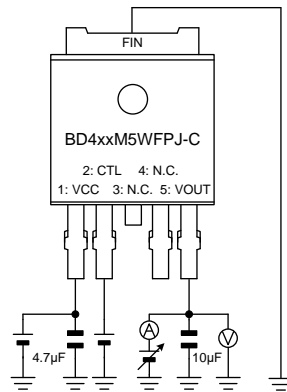
Measurement Setup for
Figure 5, 7, 16, 17, 21,
Figure 23, 25, 34, 35, 39



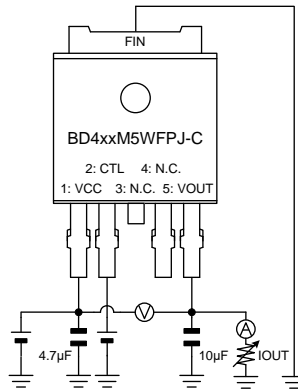
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



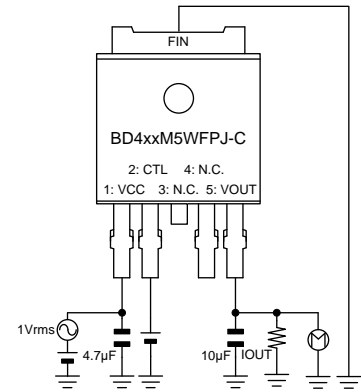
Measurement Setup for
Figure 9, 27



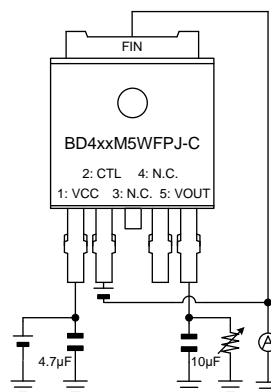
Measurement Setup for
Figure 10, 28



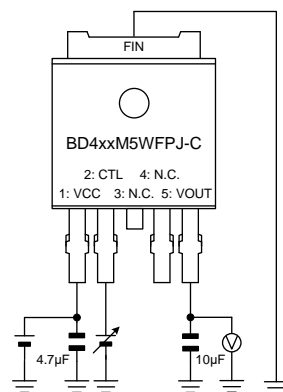
Measurement Setup for
Figure 11, 29



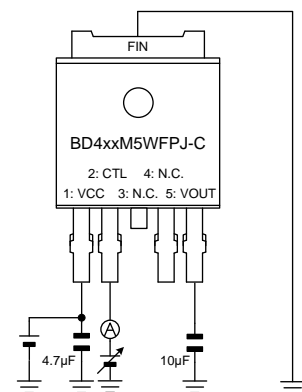
Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

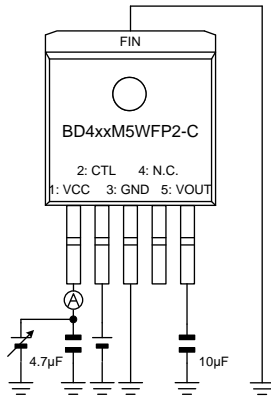


Measurement Setup for
Figure 18, 19, 20,
Figure 36, 37, 38

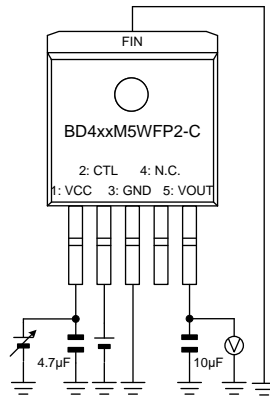


Measurement Setup for
Figure 22, 40

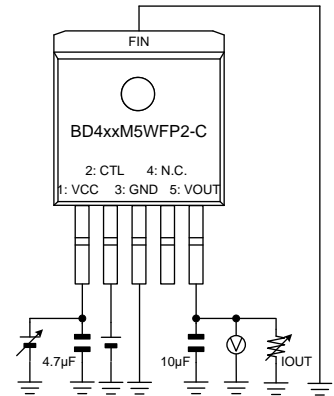
● Measurement Circuit for Typical Performance Curves (BD433 / 450M5WFP2-C)



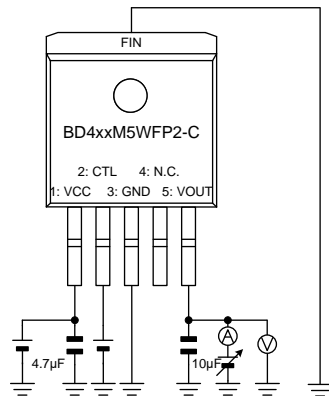
Measurement Setup for
Figure 5, 7, 16, 17, 21,
Figure 23, 25, 34, 35, 39



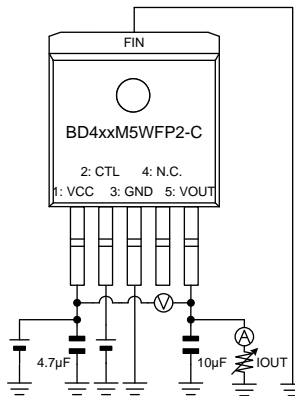
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



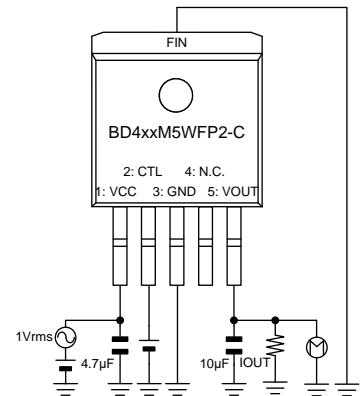
Measurement Setup for
Figure 9, 27



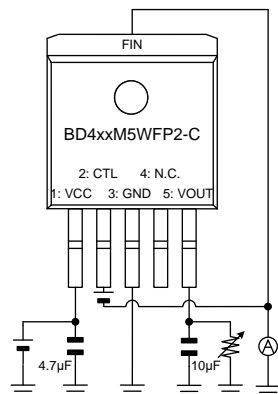
Measurement Setup for
Figure 10, 28



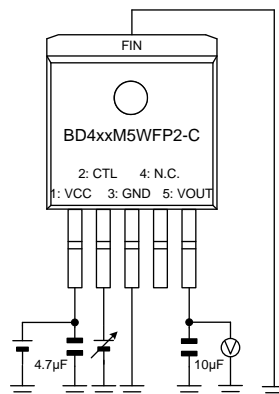
Measurement Setup for
Figure 11, 29



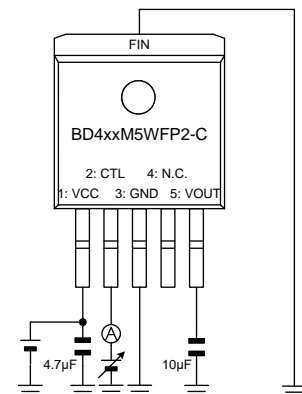
Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

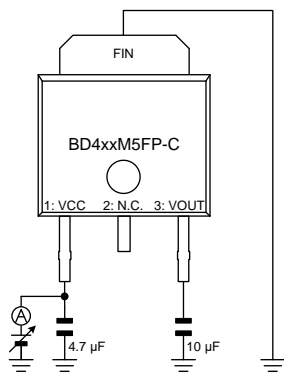


Measurement Setup for
Figure 18, 19, 20,
Figure 36, 37, 38

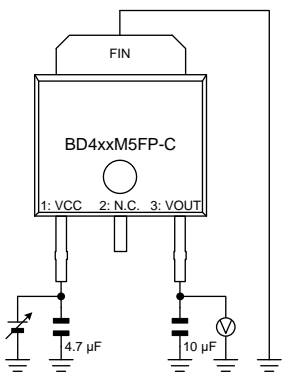


Measurement Setup for
Figure 22, 40

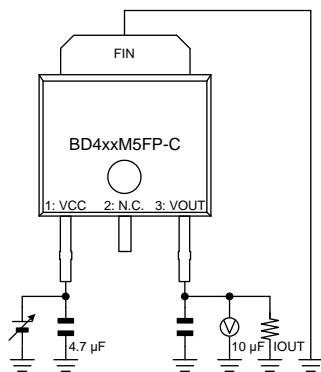
●Measurement Circuit for Typical Performance Curves (BD433 / 450M5FP-C)



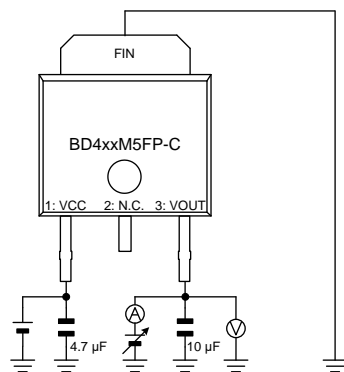
Measurement Setup for
Figure 5, 7, 16,
Figure 23, 25, 34



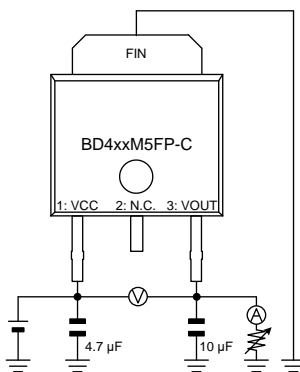
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



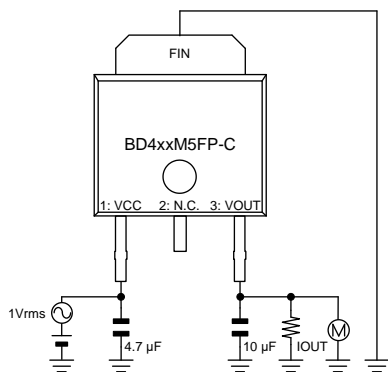
Measurement Setup for
Figure 9, 27



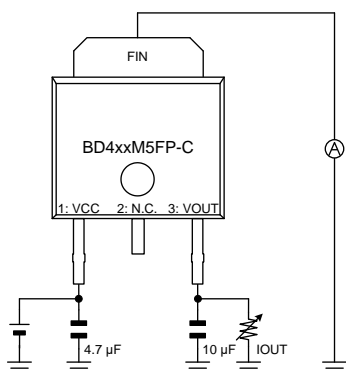
Measurement Setup for
Figure 10, 28



Measurement Setup for
Figure 11, 29

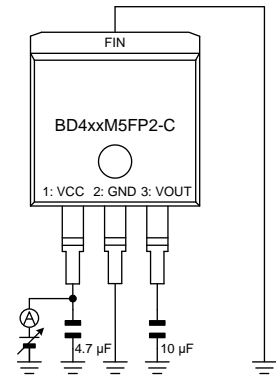


Measurement Setup for
Figure 12, 30

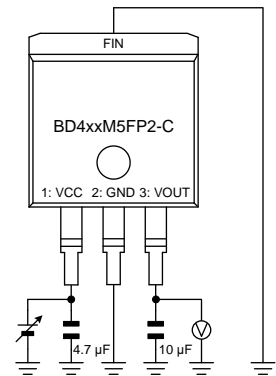


Measurement Setup for
Figure 13, 31

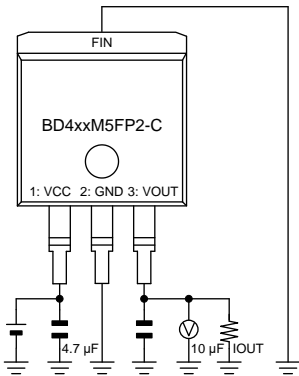
●Measurement Circuit for Typical Performance Curves (BD433 / 450M5FP2-C)



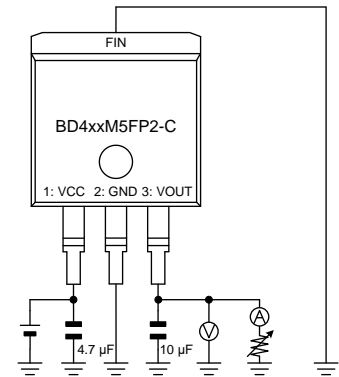
Measurement Setup for
Figure 5, 7, 16,
Figure 23, 25, 34



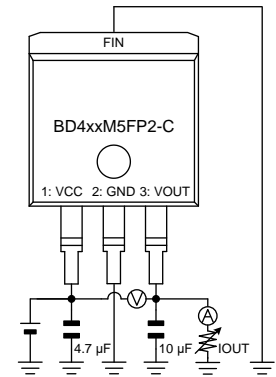
Measurement Setup for
Figure 6, 8, 14, 15,
Figure 24, 26, 32, 33



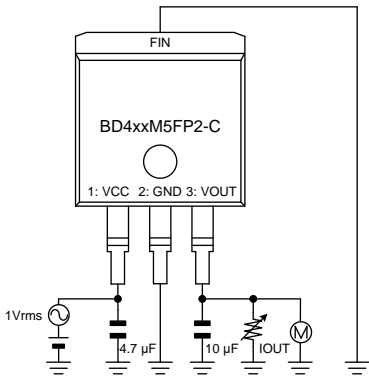
Measurement Setup for
Figure 9, 27



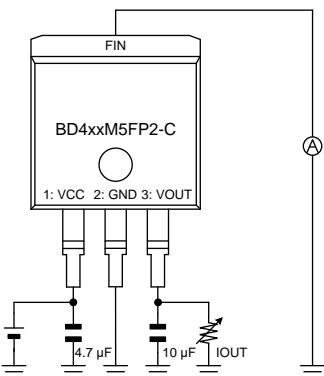
Measurement Setup for
Figure 10, 28



Measurement Setup for
Figure 11, 29



Measurement Setup for
Figure 12, 30



Measurement Setup for
Figure 13, 31

● Selection of Components Externally Connected

• VCC

Insert capacitors with a capacitance of 0.1 μF or higher between the VCC and the GND. Choose the capacitance according to the line between the power smoothing circuit and the VCC. Selection of the capacitance also depends on the application. Verify the application and allow sufficient margins in the design. We recommend using a capacitor with excellent voltage and temperature characteristics.

• Output Pin Capacitor

In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND. We recommend using a capacitor with a capacitance of 10 μF (Typ.) or higher. Electrolytic, tantalum and ceramic capacitors can be used. When selecting the capacitor ensure that the capacitance of 6 μF or higher is maintained at the intended applied voltage and temperature range. Due to changes in temperature the capacitor's capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor refer to the data of Figure 41.

The stable operation range given in the data of Figure 41 and Figure 42 is based on the standalone IC and resistive load. For actual applications the stable operating range is influenced by the PCB impedance, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

When selecting a ceramic type capacitor, we recommend using X5R, X7R or better with excellent temperature and DC-biasing characteristics and high voltage tolerance.

Also, in case of rapidly fluctuation of input voltage and load current, select the capacitance in accordance with verifying that the actual application meets with the required specification. Mount the capacitor as much as possible near connected pin.

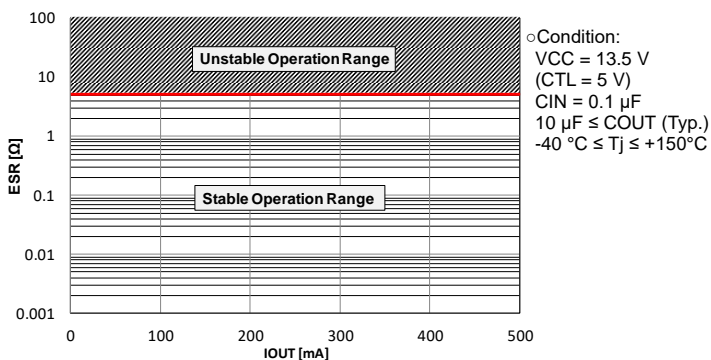


Figure 41. ESR vs. IOUT

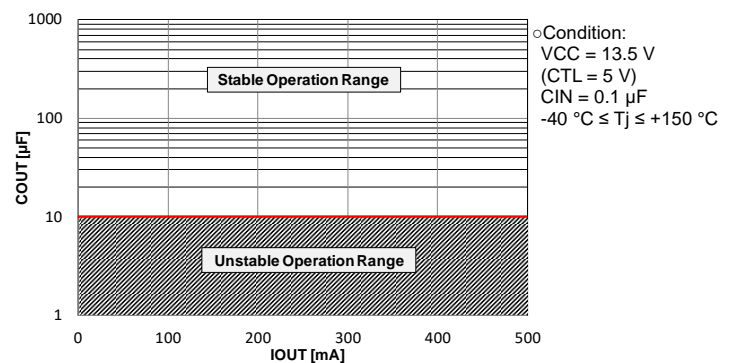
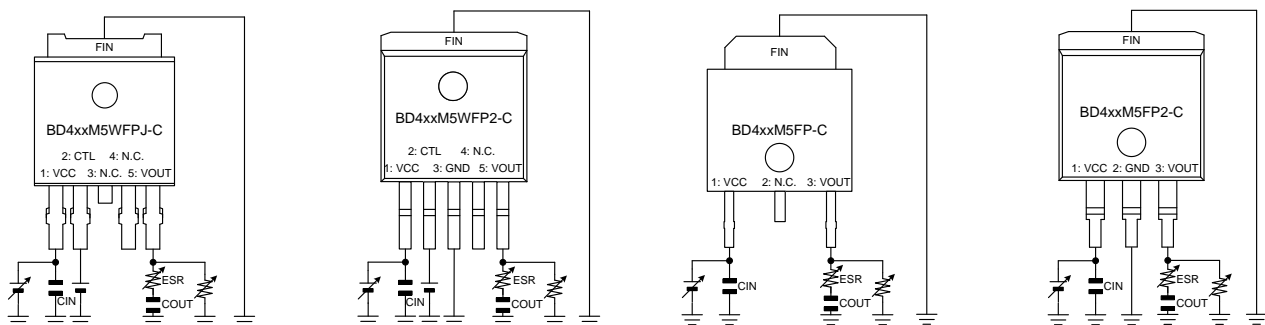


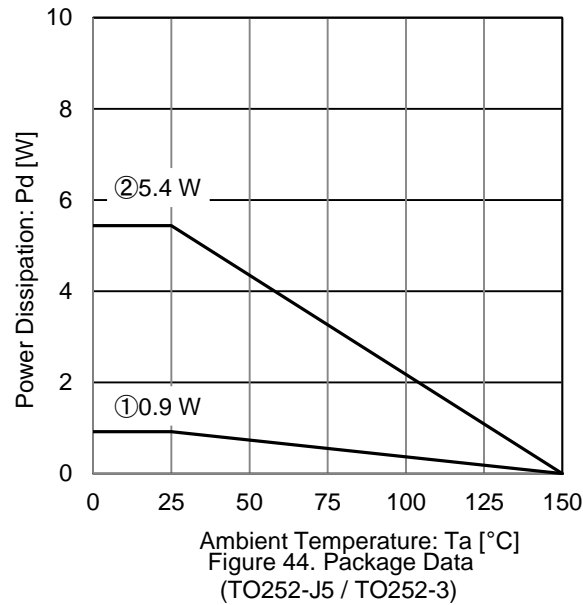
Figure 42. COUT (Typ.) vs. IOUT

● Measurement setup

Figure 43. Measurement Setups for ESR Reference Data
(about Output Pin Capacitor)

● Power Dissipation

■ TO252-J5(F) / TO252-3



IC mounted on ROHM standard board based on JEDEC.

①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)

Board material: FR4

Board size: 114.3mm × 76.2mm × 1.57 mm

Mount condition: PCB and exposed pad are soldered.

Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②: 4-layer PCB (Copper foil area on the reverse side of PCB: 74.2mm × 74.2mm)

Board material: FR4

Board size: 114.3mm × 76.2mm × 1.60 mm

Mount condition: PCB and exposed pad are soldered.

Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

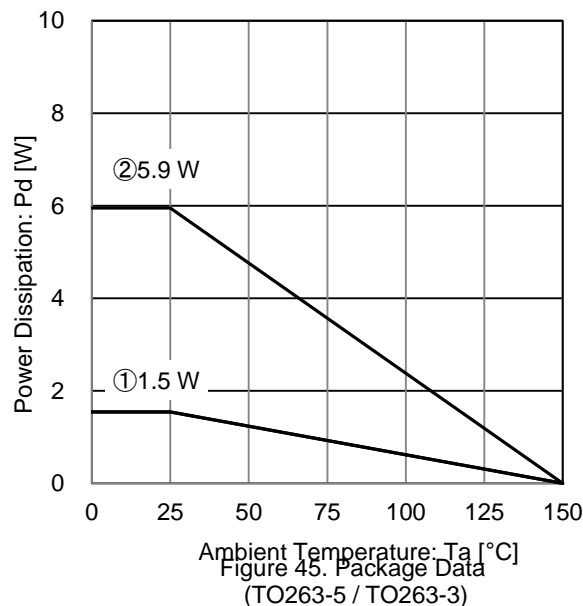
2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.

Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: $\theta_{JA} = 136 \text{ }^{\circ}\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 17 \text{ }^{\circ}\text{C/W}$

Condition②: $\theta_{JA} = 23 \text{ }^{\circ}\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 3 \text{ }^{\circ}\text{C/W}$

■ TO263-5(F) / TO263-3(F)



IC mounted on ROHM standard board based on JEDEC.

①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)

Board material: FR4

Board size: 114.3mm × 76.2mm × 1.57 mm

Mount condition: PCB and exposed pad are soldered.

Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

②: 4-layer PCB (Copper foil area on the reverse side of PCB: 74.2mm × 74.2mm)

Board material: FR4

Board size: 114.3mm × 76.2mm × 1.60 mm

Mount condition: PCB and exposed pad are soldered.

Top copper foil: ROHM recommended footprint + wiring to measure, 2 oz. copper.

2 inner layers copper foil area of PCB: 74.2 mm × 74.2 mm, 1 oz. copper.

Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm, 2 oz. copper.

Condition①: $\theta_{JA} = 81 \text{ }^{\circ}\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 8 \text{ }^{\circ}\text{C/W}$

Condition②: $\theta_{JA} = 21 \text{ }^{\circ}\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 2 \text{ }^{\circ}\text{C/W}$

● Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement.

Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 44, 45 when using the IC in an environment of $T_a \geq 25^\circ\text{C}$. Even if the ambient temperature T_a is at 25°C , depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be $T_j \leq T_{j\max} = 150^\circ\text{C}$ in all possible operating temperature range.

Should by any condition the maximum junction temperature $T_{j\max} = 150^\circ\text{C}$ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_j .

T_j can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature T_j .

$$T_j = T_a + P_C \times \theta_{JA}$$

T_j	: Junction Temperature
T_a	: Ambient Temperature
P_C	: Power Consumption
θ_{JA}	: Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature T_j .

$$T_j = T_T + P_C \times \Psi_{JT}$$

T_j	: Junction Temperature
T_T	: Top Center of Case's (mold) Temperature
P_C	: Power consumption
Ψ_{JT}	: Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption P_C (W).

$$P_C = (V_{CC} - V_{OUT}) \times I_{OUT} + V_{CC} \times I_{CC}$$

P_C	: Power Consumption
V_{CC}	: Input Voltage
V_{OUT}	: Output Voltage
I_{OUT}	: Load Current
I_{CC}	: Circuit Current

• Calculation Example(TO252-J5(F) / TO252-3)

If VCC = 13.5 V, VOUT = 5.0 V, IOU = 200 mA, Icc = 38 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (VCC - VOUT) \times IOU + VCC \times I_{cc} \\ &= (13.5 \text{ V} - 5.0 \text{ V}) \times 200 \text{ mA} + 13.5 \text{ V} \times 38 \mu\text{A} \\ &= 1.7 \text{ W} \end{aligned}$$

At the ambient temperature Tamax = 85°C, the thermal Impedance (Junction to Ambient) $\theta_{JA} = 23 \text{ }^{\circ}\text{C} / \text{W}$ (4-layer PCB),

$$\begin{aligned} T_j &= T_{\text{amax}} + P_C \times \theta_{JA} \\ &= 85 \text{ }^{\circ}\text{C} + 1.7 \text{ W} \times 23 \text{ }^{\circ}\text{C} / \text{W} \\ &= 124.1 \text{ }^{\circ}\text{C} \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature $T_T = 100^{\circ}\text{C}$ 、 $\Psi_{JT} = 17 \text{ }^{\circ}\text{C} / \text{W}$ (1-layer PCB),

$$\begin{aligned} T_j &= T_T + P_C \times \Psi_{JT} \\ &= 100 \text{ }^{\circ}\text{C} + 1.7 \text{ W} \times 17 \text{ }^{\circ}\text{C} / \text{W} \\ &= 128.9 \text{ }^{\circ}\text{C} \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

• Calculation Example (TO263-5(F) / TO263-3(F))

If VCC = 13.5 V, VOUT = 5.0 V, IOU = 200 mA, Icc = 38 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (VCC - VOUT) \times IOU + VCC \times I_{cc} \\ &= (13.5 \text{ V} - 5.0 \text{ V}) \times 200 \text{ mA} + 13.5 \text{ V} \times 38 \mu\text{A} \\ &= 1.7 \text{ W} \end{aligned}$$

At the ambient temperature Tamax = 85°C, the thermal impedance (Junction to Ambient) $\theta_{JA} = 21 \text{ }^{\circ}\text{C} / \text{W}$ (4-layer PCB),

$$\begin{aligned} T_j &= T_{\text{amax}} + P_C \times \theta_{JA} \\ &= 85 \text{ }^{\circ}\text{C} + 1.7 \text{ W} \times 21 \text{ }^{\circ}\text{C} / \text{W} \\ &= 120.7 \text{ }^{\circ}\text{C} \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature $T_T = 100^{\circ}\text{C}$ 、 $\Psi_{JT} = 8 \text{ }^{\circ}\text{C} / \text{W}$ (1-layer PCB),

$$\begin{aligned} T_j &= T_T + P_C \times \Psi_{JT} \\ &= 100 \text{ }^{\circ}\text{C} + 1.7 \text{ W} \times 8 \text{ }^{\circ}\text{C} / \text{W} \\ &= 113.6 \text{ }^{\circ}\text{C} \end{aligned}$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

● Application Examples

- Applying positive surge to the VCC

If the possibility exists that surges higher than 45 V will be applied to the VCC, a Zener Diode should be placed between the VCC and the GND as shown in the figure below.

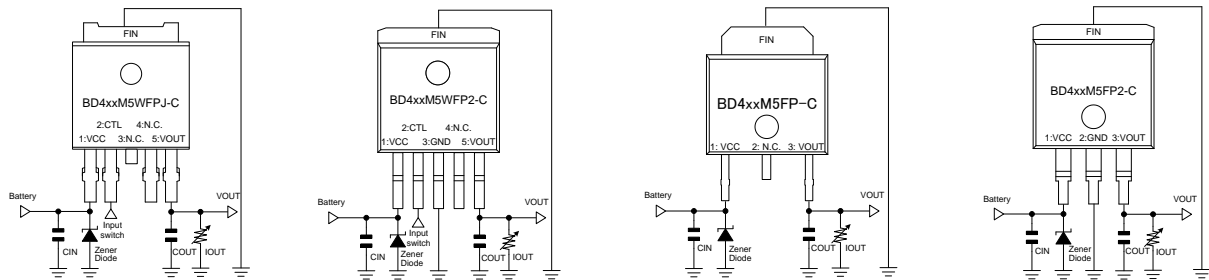


Figure 46. Sample Application Circuit 1

- Applying negative surge to the VCC

If the possibility exists that negative surges lower than the GND are applied to the VCC, a Schottky Diode should be placed between the VCC and the pin as shown in the figure below.

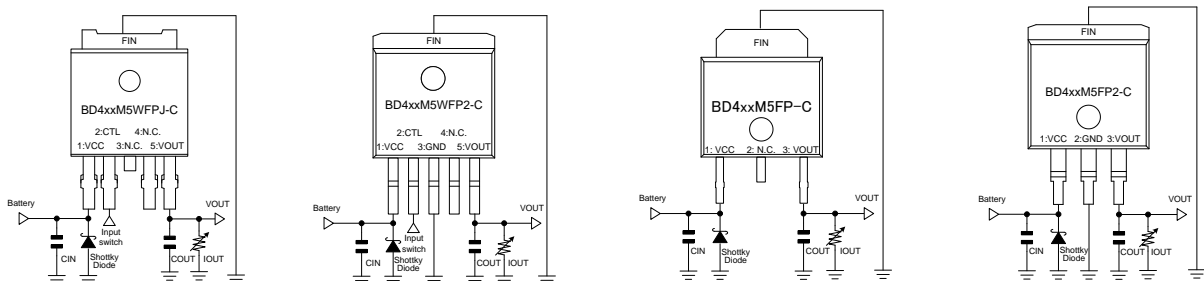


Figure 47. Sample Application Circuit 2

- Implementing a Protection Diode

If the possibility exists that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and shutdown, a protection diode should be placed as shown in the figure below.

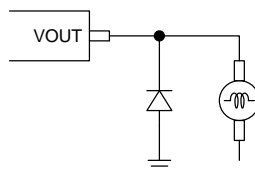


Figure 48. Sample Application Circuit 3

● I/O Equivalence Circuit

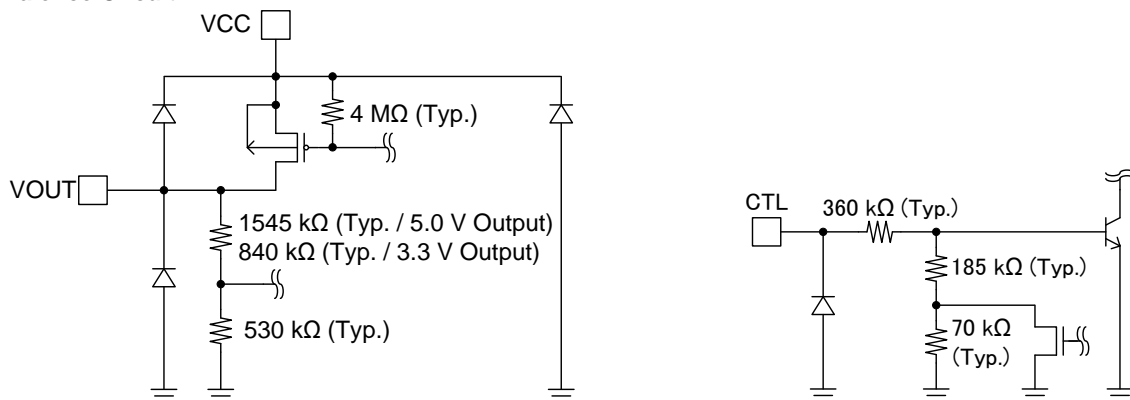


Figure 49. Input / Output Equivalence Circuit

●Operational Notes

- 1) Absolute Maximum Ratings
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters can result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.
- 2) The electrical characteristics given in this specification may be influenced by conditions such as temperature, supply voltage and external components. Transient characteristics should be sufficiently verified.
- 3) GND Electric Potential
Keep the GND potential at the lowest (minimum) level under any operating condition. Furthermore, ensure that, including the transient, none of the pin's voltage is less than the GND voltage.
- 4) GND Wiring Pattern
When both a small-signal GND and a high current GND are present, single-point grounding (at the set standard point) is recommended. This in order to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal GND. Similarly, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.
- 5) CTL
Do not make voltage level of chip enable keep floating level, or in between V_{thH} and V_{thL} . Otherwise, the output voltage would be unstable or indefinite.
- 6) Inter-pin Shorting and Mounting Errors
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Also, shorts caused by dust entering between the output, input and the GND may result in damaging the IC.
- 7) Inspection Using the Set Board
The IC needs to be discharged after each inspection process as, while using the set board for inspection, connecting a capacitor to a low-impedance pin may cause stress to the IC. As a protection from static electricity, ensure that the assembly setup is grounded and take sufficient caution with transportation and storage. Also, make sure to turn off the power supply when connecting and disconnecting the inspection equipment.
- 8) Thermal Design
The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed for in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. Use both the front and reverse side of the PCB to increase the heat dissipation pattern as far as possible. The amount of heat generated depends on the voltage difference across the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating.
Should by any condition the maximum junction temperature $T_{jmax} = 150^{\circ}\text{C}$ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design.
- 9) Overcurrent Protection Circuit
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.
- 10) Thermal Shut Down (TSD)
This IC incorporates an integrated thermal shutdown circuit to prevent heat damage to the IC. Normal operation should be within the power dissipation rating, if however the rating is exceeded for a continued period, the junction temperature (T_j) will rise and the TSD circuit will be activated and turn all output pins OFF. After the T_j falls below the TSD threshold the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

- 11) In some applications, the VCC and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VCC when the VCC shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 1000 μF . Also by inserting a reverse polarity diode in series to the VCC, it can prevent reverse current from reverse battery connection or the case. When the point A is short-circuited GND, if there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VCC and the VOUT.

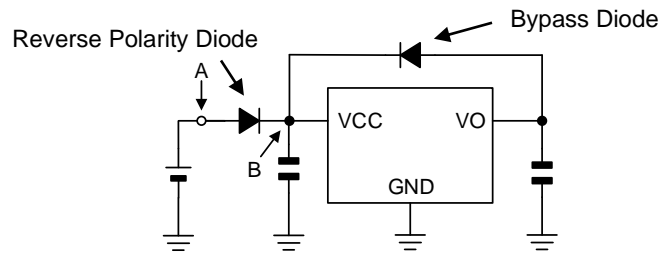


Figure 50. Recommend Example of Using Diodes

- 12) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.

For example, in case a resistor and a transistor are connected to the pins as shown in the figure below then:

- The P/N junction functions as a parasitic diode when the GND > pin A for the resistor, or the GND > pin B for the transistor.

- Also, when the GND > pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of the other adjacent elements to operate as a parasitic NPN transistor.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.

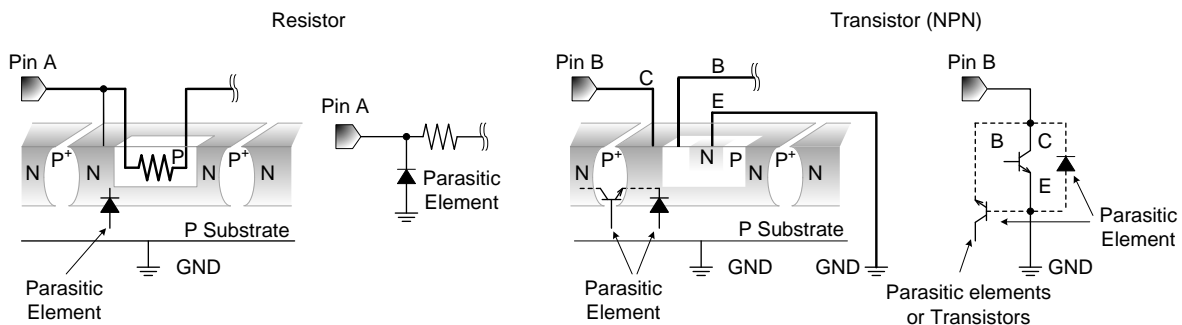
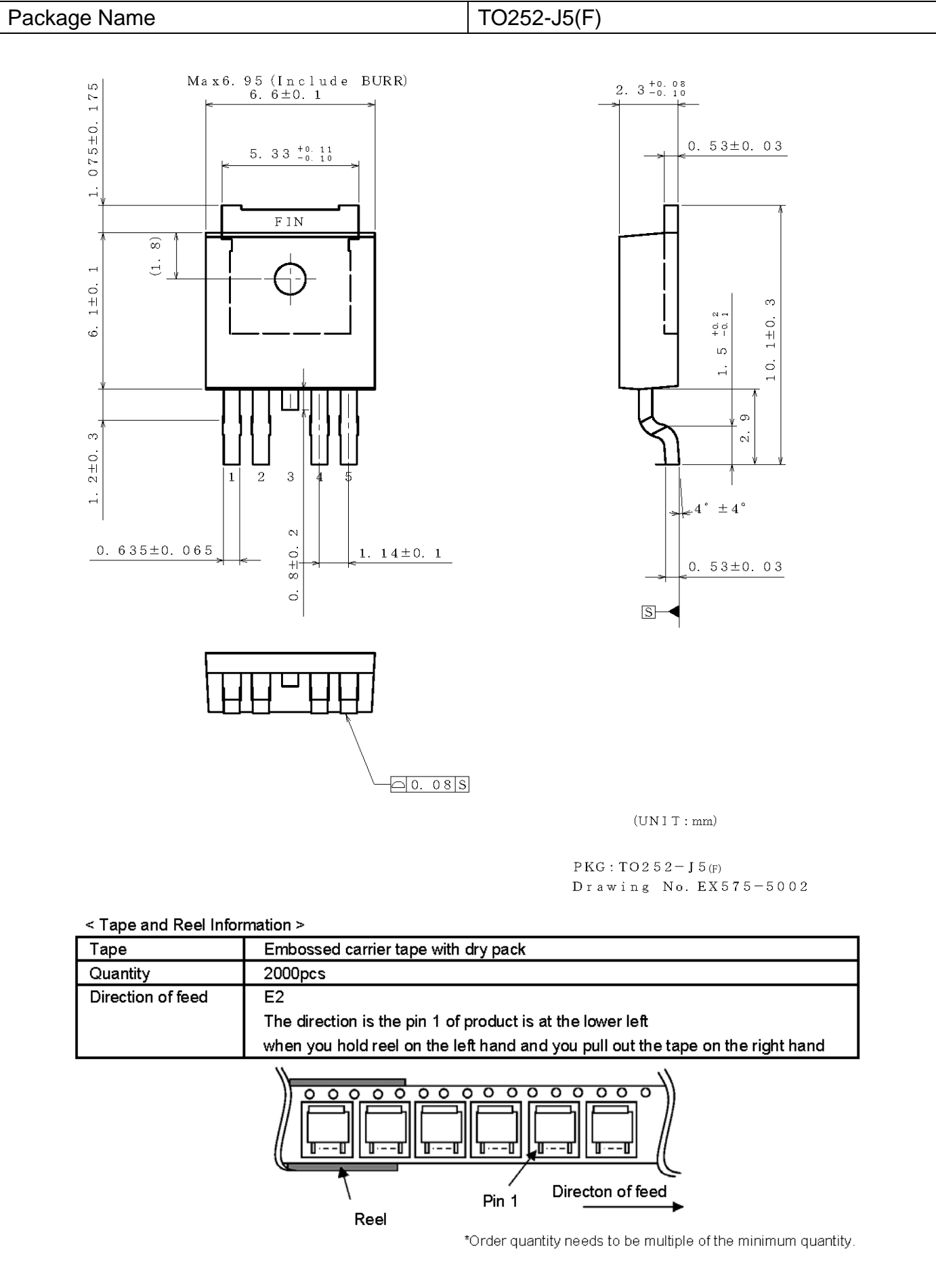
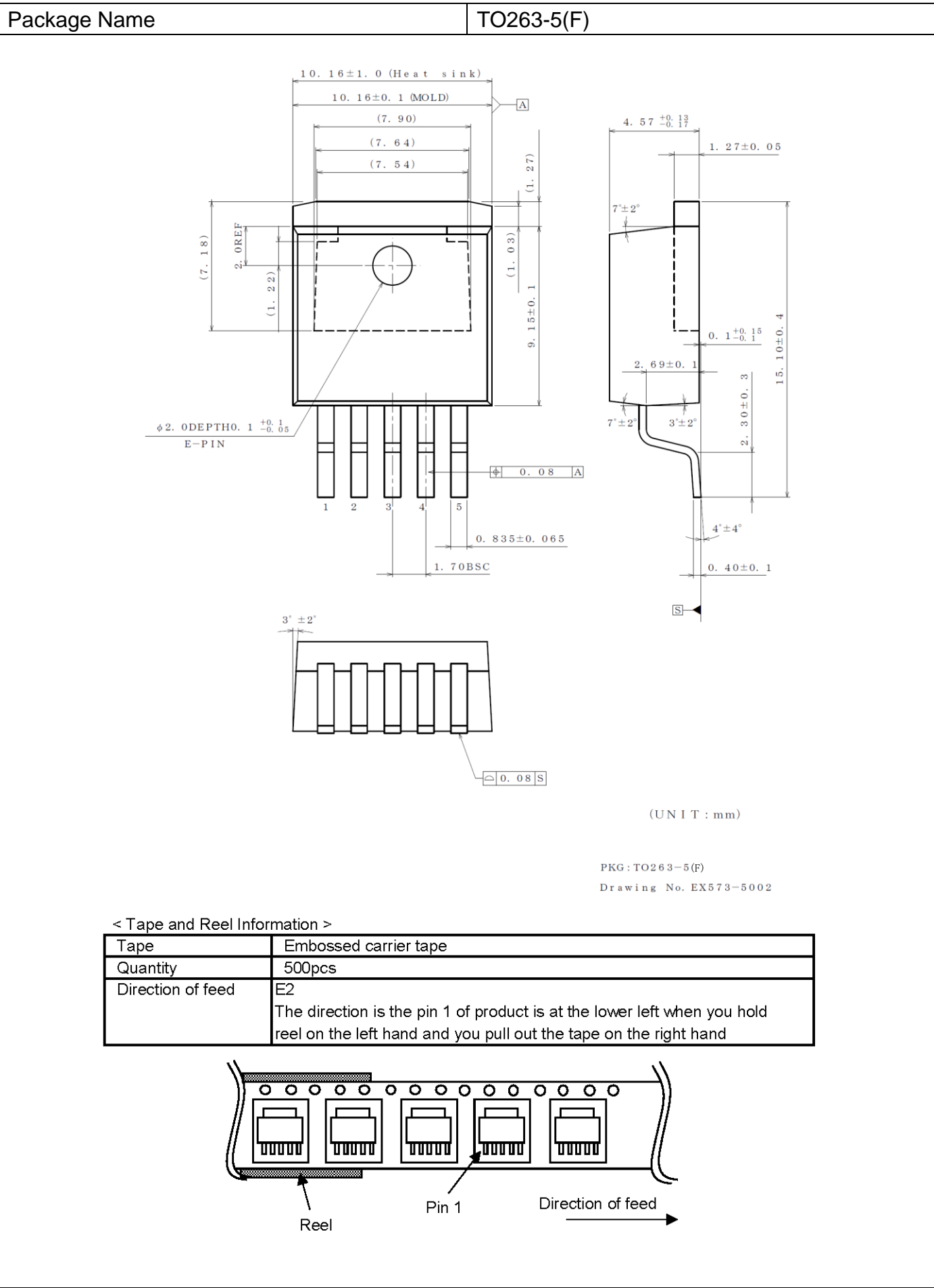
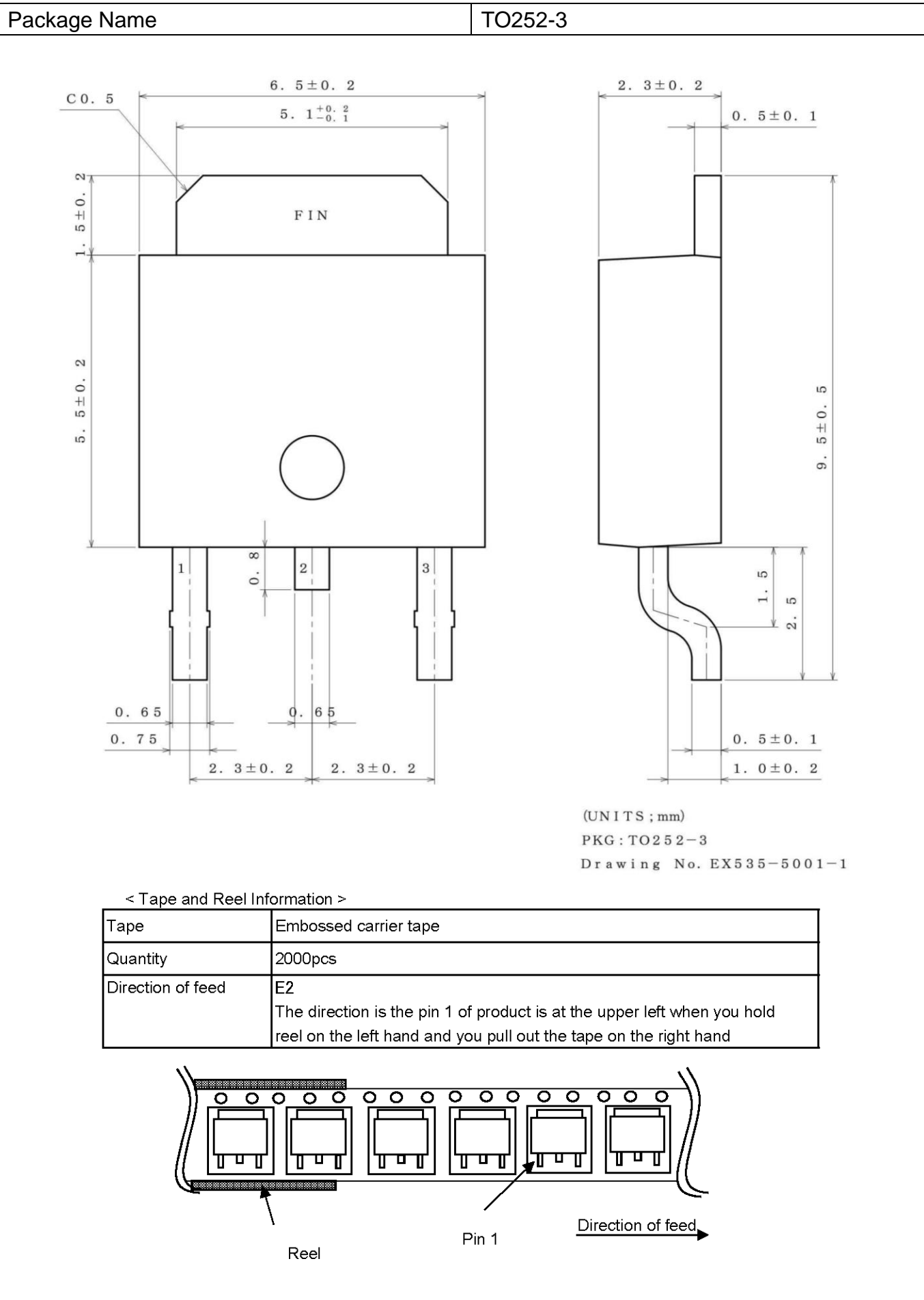


Figure 51. Example of parasitic element device

●Physical Dimension, Tape and Reel Information

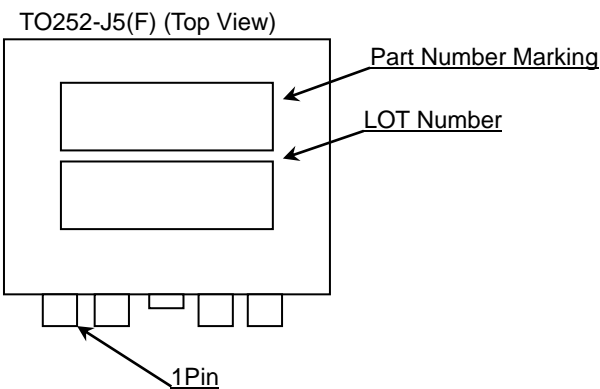






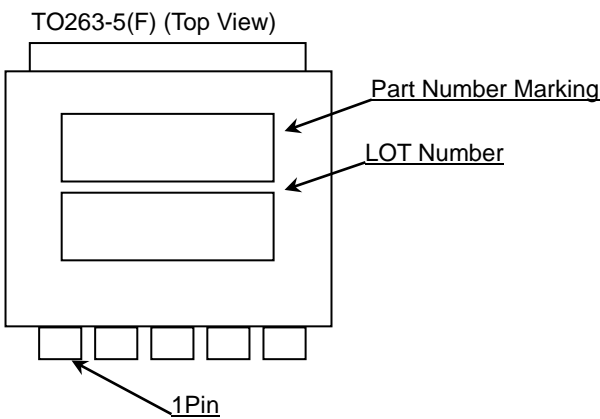
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 TSZ22111-15-001

●Marking Diagrams (Top View)



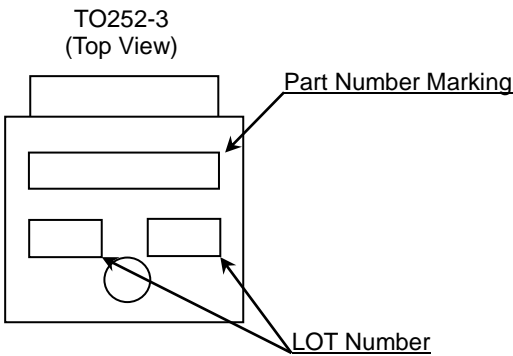
Part Number Marking	Output Voltage [V]	Enable Input ⁽¹⁾
433M5W	3.3	○
450M5W	5.0	○

(1) ○: Includes Enable Input
—: Not includes Enable Input



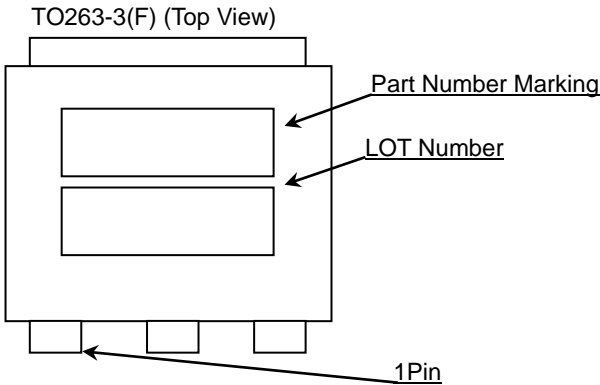
Part Number Marking	Output Voltage [V]	Enable Input ⁽¹⁾
433M5W	3.3	○
450M5W	5.0	○

(1) ○: Includes Enable Input
—: Not includes Enable Input



Part Number Marking	Output Voltage [V]	Enable Input ⁽¹⁾
433M5	3.3	—
450M5	5.0	—

(1) ○: Includes Enable Input
—: Not includes Enable Input



Part Number Marking	Output Voltage [V]	Enable Input ⁽¹⁾
433M5	3.3	—
450M5	5.0	—

(1) ○: Includes Enable Input
—: Not includes Enable Input

●Revision History

Date	Revision	Changes
5.Apr.2013	001	New Release
18.Oct.2013	002	General description and key specifications revised. Figure 1. FP2: TO263-5F H (Max.) revised. Pin No. Fin of BD433 / 450M5WFPJ-C and BD433 / 450M5WFP2-C revised. Figure 4. Block Diagrams (BD433 / 450M5WFPJ-C, BD433 / 450M5WFP2-C, BD433 / 450M5FP-C, BD433 / 450M5FP2-C) revised. Physical Dimension(TO252-J5F), Tape and Reel Information (TO263-5F, TO263-3F) revised.
01.Oct.2014	003	Key specifications is revised to Features. Calculation Example Figure No. of output current max. about TO252-3, TO263-5F, TO263-3F revised. Tape and Reel Information (TO263-5F, TO263-3F) revised.
04.Feb.2015	004	Names of PKG revised. Description of Thermal impedance (TO252-J5, TO252-3, TO263-5, TO263-3) revised.
23.May.2016	005	Names of Ordering Information revised. Title of Figure 45 revised. Copper foil area on the reverse side of PCB revised. AEC-Q100 (Note1:Grade1) appended.
22.Feb.2017	006	Names of Ordering Information revised. Improve the description, TO252-J5 to To252-J5(F), TO263-5 to TO263-5(F), TO263-3 to TO263-3(F). Measurement Figure revised. TO252-J5(F), TO263-5(F), TO263-3(F)'s PKG information revised.
22.May.2025	007	P.24 Improved the title of Figure 42.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [h] Use of the Products in places subject to dew condensation
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5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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