

Technical Note

CMOS LDO Regulators for Portable Equipments 1ch 150mA CMOS LDO Regulators

Pb Free RoHS Directive Compliance

No.11020EBT04

BHDDNB1WHFV series

Description

The BH INB1WHFV series is a line of 150 mA output, high-performance CMOS regulators that deliver a high ripple rejection ratio of 80 dB (Typ., 1 kHz). They are ideal for use in high-performance, analog applications and offer improved line regulation, load regulation, and noise characteristics. Using the ultra-small HVSOF5 package, which features a built-in heat sink, contributes to space-saving application designs.

Features

- 1) High accuracy output voltage: ± 1%
- 2) High ripple rejection ratio: 80 dB (Typ., 1 kHz)
- 3) Stable with ceramic capacitors
- 4) Low bias current: 60 μA
- 5) Output voltage on/off control
- 6) Built-in overcurrent and thermal shutdown circuits
- 7) Ultra-small HVSOF5 power package

Applications

Battery-driven portable devices, etc.

Product line

■150 mA BH□□NB1WHFV Series

Product name	2.5	2.8	2.85	2.9	3.0	3.1	3.3	Package
BHDDNB1WHFV	\checkmark	HVSOF5						

Model name: BH

b

Symbol	Description							
	Output voltage specification							
		□□ Output voltage (V) □□ Output						
	25	2.5 V (Typ.)	30	3.0 V (Typ.)				
а	28	2.8 V (Typ.)	31	3.1 V (Typ.)				
	2J	2.85 V (Typ.)	33	3.3 V (Typ.)				
	29	2.9 V (Typ.)						
b	Package HFV: HVSOF5							

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit		
Applied power supply voltage	VMAX	-0.3 to +6.0	V		
Power dissipation	Pd	410 ^{*1}	mW		
Operating temperature range	Topr	-40 to +85	°C		
Storage temperature range	Tstg	−55 to +125	°C		
*1: Reduce by 4.1 m/W/° over 25°C, when mounted on a class enory PCB (70 mm \times 70 mm \times 1.6 mm)					

*1: Reduce by 4.1 mW/°C over 25°C, when mounted on a glass epoxy PCB (70 mm \times 70 mm \times 1.6 mm).

Recommended operating ranges (not to exceed Pd)

Parameter	Symbol	Ratings	Unit
Power supply voltage	Vin	2.5 to 5.5	V
Output current	Ιουτ	0 to 150	mA

Recommended operating conditions

Parameter	Symbol	Ratings			Unit	Conditions
Falameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Input capacitor	CIN	0.1 ^{*2}	—	—	μF	The use of ceramic capacitors is recommended.
Output capacitor	Со	2.2 ^{*2}	—	—	μF	The use of ceramic capacitors is recommended.

*2 Make sure that the output capacitor value is not kept lower than this specified level across a variety of temperature, DC bias characteristic. And also make sure that the capacitor value cannot change as time progresses.

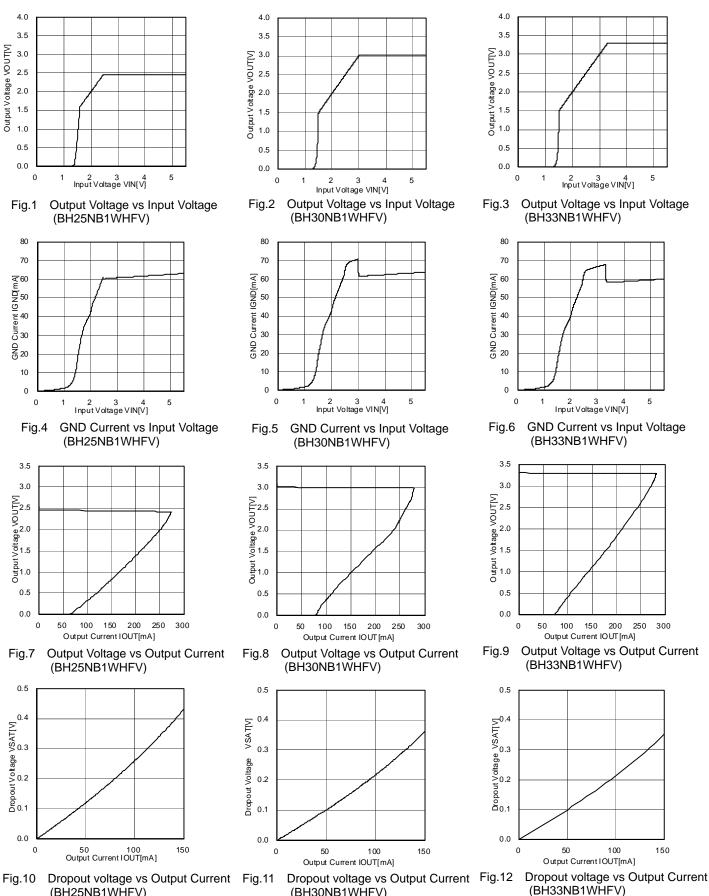
•Electrical characteristics

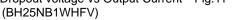
(Unless otherwise specified, Ta = 25°C, VIN = VOUT + 1.0 V, STBY = 1.5 V, CIN = 0.1 μ F, Co = 2.2 μ F)

Devenueter		Current al	Limits			Conditions	
Parameter		Symbol	Min.	Тур.	Max.	Unit	Conditions
Output voltage		Vout	Vout×0.99	Vout	Vout×1.01	V	Iout = 1 mA
Circuit current		IGND	—	60	100	μA	IOUT = 50 mA
Circuit current (STBY)		ISTBY	_	_	1.0	μA	STBY = 0 V
Ripple rejection ratio		RR	_	80	_	dB	VRR = -20 dBv, fRR = 1 kz, IOUT = 10 mA
Load response 1		LTV1	—	25		mV	IOUT = 1 mA to 30 mA
Load response 2		LTV2	_	25		mV	IOUT = 30 mA to 1 mA
Dropout voltage 1		VSAT1	_	80	150	mV	$VIN = 0.98 \times VOUT,$ IOUT = 30 mA
Dropout voltage 2		VSAT2	—	250	450	mV	VIN = 0.98 × VOUT, IOUT = 100 mA
Line regulation		VDL1	—	1	20	mV	VIN = VOUT + 0.5 V to 5.5 V, IOUT = 50 mA
Load regulation 1		VDLO1	_	6	30	mV	IOUT = 1 mA to 100 mA
Load regulation 2		VDLO2	—	9	90	mV	IOUT = 1 mA to 150 mA
Overcurrent protection limit current		ILMAX	—	250	_	mA	$Vo = Vout \times 0.98$
Short current		ISHORT	—	50	—	mA	Vo = 0 V
STBY pull-down resista	ance	RSTB	275	550	1100	kΩ	
STRV control voltage	ON	VSTBH	1.5	_	Vin	V	
STBY control voltage	OFF	VSTBL	-0.3		0.3	V	

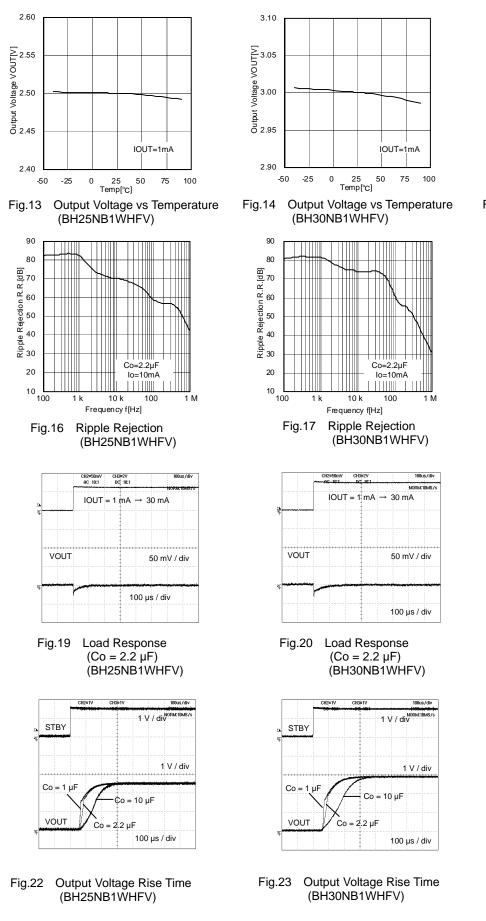
* This IC is not designed to be radiation-resistant.

Reference data





(BH30NB1WHFV)



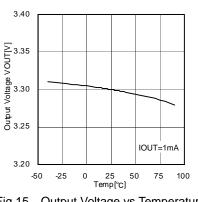
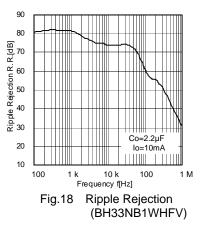


Fig.15 Output Voltage vs Temperature (BH33NB1WHFV)



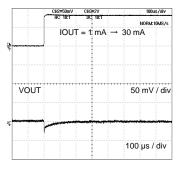


Fig.21 Load Response (Co = 2.2 µF) (BH33NB1WHFV)

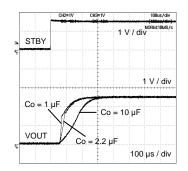
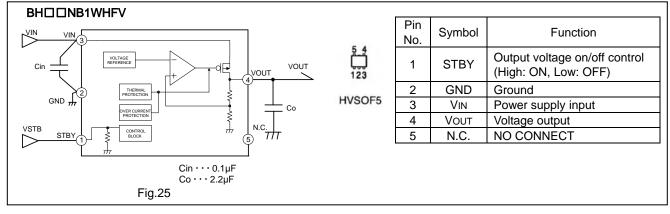


Fig.24 Output Voltage Rise Time (BH33NB1WHFV)

Block diagram, recommended circuit diagram, and pin assignment diagram



Power dissipation (Pd)

1. Power dissipation (Pd)

Power dissipation calculations include estimates of power dissipation characteristics and internal IC power consumption, and should be treated as guidelines. In the event that the IC is used in an environment where this power dissipation is exceeded, the attendant rise in the junction temperature will trigger the thermal shutdown circuit, reducing the current capacity and otherwise degrading the IC's design performance. Allow for sufficient margins so that this power dissipation is not exceeded during IC operation.



$$PMAX = (VIN - VOUT) \times IOUT (MAX.)$$

VIN : Input voltage Vo∪⊤ : Output voltage _ Io∪⊤ (MAX): Max. output current

2. Power dissipation/power dissipation reduction (Pd)

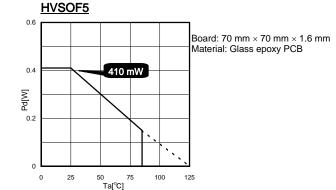


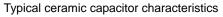
Fig. 26 HVSOF5 Power Dissipation/Power Dissipation Reduction (Example)

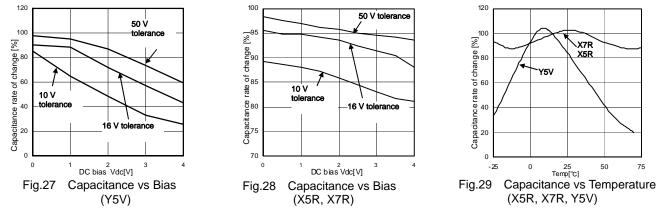
*Circuit design should allow a sufficient margin for the temperature range so that PMAX < Pd.

Input Output capacitors

It is recommended to insert bypass capacitors between input and GND pins, positioning them as close to the pins as possible. These capacitors will be used when the power supply impedance increases or when long wiring paths are used, so they should be checked once the IC has been mounted.

Ceramic capacitors generally have temperature and DC bias characteristics. When selecting ceramic capacitors, use X5R or X7R, or better models that offer good temperature and DC bias characteristics and high tolerant voltages.





Output capacitors

Mounting input capacitor between input pin and GND(as close to pin as possible), and also output capacitor between output pin and GND(as close to pin as possible) is recommended. The input capacitor reduces the output impedance of the voltage supply source connected to the VCC. The higher value the output capacitor goes, the more stable the whole operation becomes. This leads to high load transient response. Please confirm the whole operation on actual application board. Generally, ceramic capacitor has wide range of tolerance, temperature coefficient, and DC bias characteristic. And also its value goes lower as time progresses. Please choose ceramic capacitors after obtaining more detailed data by asking capacitor makers.

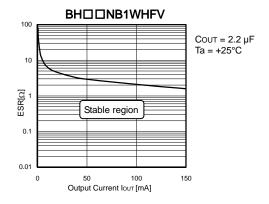


Fig.30 Stable Operation Region (Example)

Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

3. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

4. Thermal shutdown circuit (TSD)

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

5. Overcurrent protection circuit

The IC incorporates a built-in overcurrent protection circuit that operates according to the output current capacity. This circuit serves to protect the IC from damage when the load is shorted. The protection circuit is designed to limit current flow by not latching in the event of a large and instantaneous current flow originating from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capability has negative characteristics to temperatures.

6. Action in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

7. Ground wiring pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

8. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

9. Back Current

In applications where the IC may be exposed to back current flow, it is recommended to create a path to dissipate this current by inserting a bypass diode between the VIN and VOUT pins.

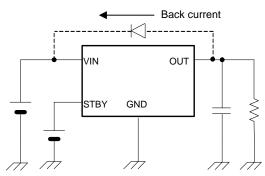


Fig. 31 Example Bypass Diode Connection

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

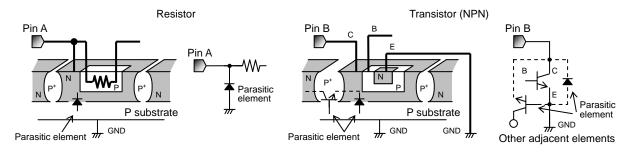
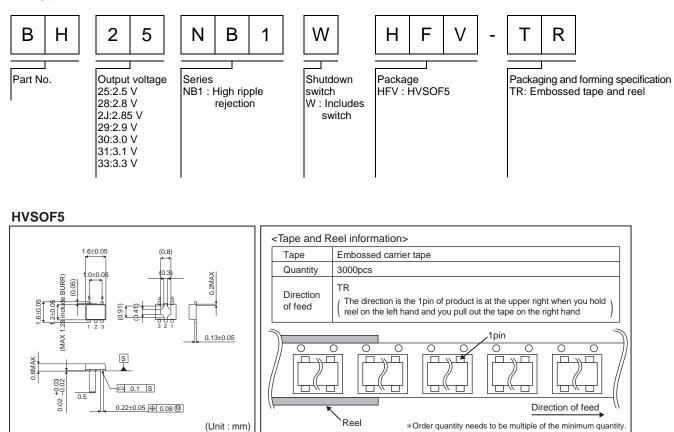


Fig.32 Example of IC structure

Ordering part number



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 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [C] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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