Hot Swap Controller and Digital Power and Energy Monitor with PMBus Interface

BD12780AMUV-LB

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

The BD12780AMUV-LB is a hot swap controller with PMBus Interface. It has load current, input voltage, output voltage, external N-channel FET power and temperature monitors via integrated 12-bit ADC. The BD12780AMUV-LB senses the voltage across the external sense resistor from the HSP and HSN pins, amplifies the voltage with an internal current sense amplifier, and measures the load current to limit the current.

The BD12780AMUV-LB controls the gate voltage of the external N-channel FET so that the load current is maintained around the current limit level. When the load current reaches the current limit threshold, the timer operates to limit the load current with the FET ON for the time determined by the capacitor connected to the TIMER pin. In addition, a constant power foldback scheme is used to control MOSFET power consumption in the event of a power-on or failure. This power limit keeps the FET within the safe operating area. When a short-circuit event occurs, the fast internal overcurrent detector responds within 320 ns and shuts down the gate of the external FET.

The BD12780AMUV-LB has under voltage and over voltage detection of the input voltage at UV and OV pins, and the detection voltage levels can be programmed with external resistor divider. The output voltage is also monitored at PWGIN pin with external resistor divider and the PWRGD signal is the indicator if the input and output voltages are within normal range.

Features

- ±0.7 % Accurate, 12-bit ADC for I_{OUT}, V_{IN}, V_{OUT}, and Temperature
- 320 ns Response Time to Short Circuit
- Shutdown upon FET Health Fault Detection
- Constant Power Foldback for Tighter FET SOA Protection
- Remote Temperature Sensing with Programmable Warning and Shutdown Thresholds
- Resistor-programmable 5 mV to 25 mV V_{SENSE} Current Limit
- Programmable Start-up Current Limit
- 1 % Accurate UV, OV, and PWRGD Thresholds
- Split Hot Swap and Power Monitor Inputs to Allow Additional External ADC Filtering
- Reports Power and Energy Consumption over Time
- Peak Detect Registers for Current, Voltage, and Power
- PROCHOT Power Throttling Capability
- PMBus 1.3 Compliant Interface

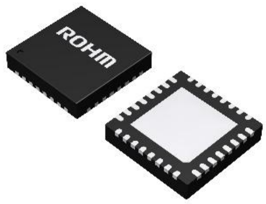
Applications

- Industrial Equipment
- Server and Datacenter
- Network Router and Switches
- Power Distribution Systems

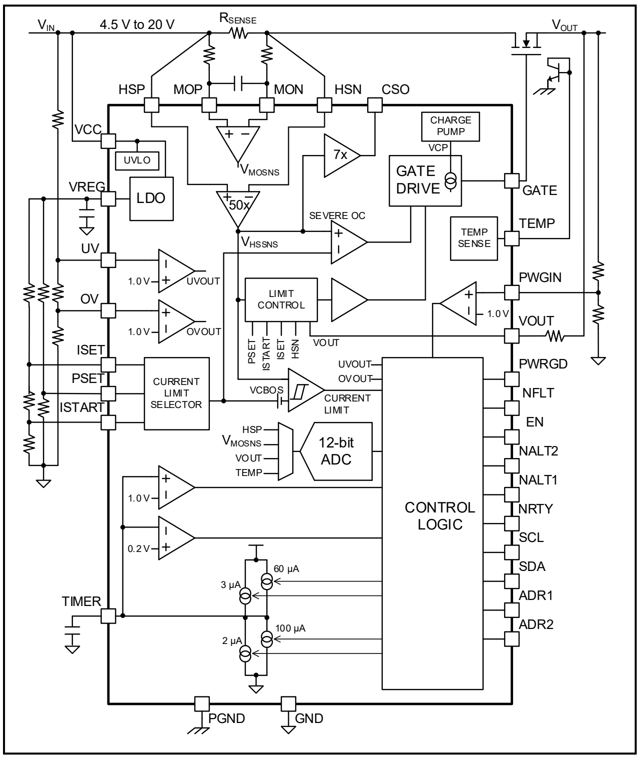
Key Specifications

- VCC Voltage Range: 4.5 V to 20 V (Absolute Max 30 V)
- Operating Temperature Range: -40 °C to +85 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN032V5050	5.0 mm x 5.0 mm x 1.0 mm



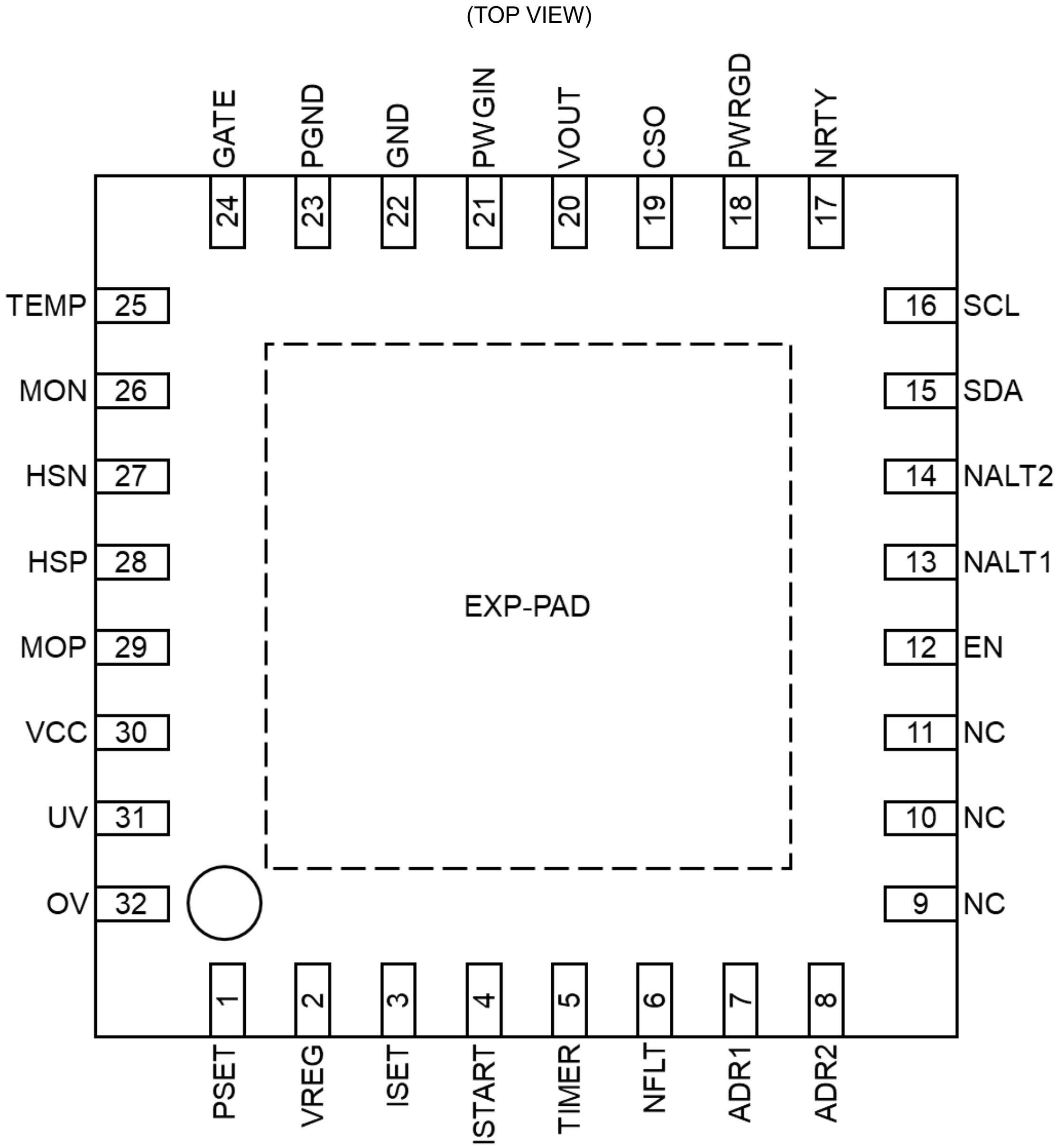
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

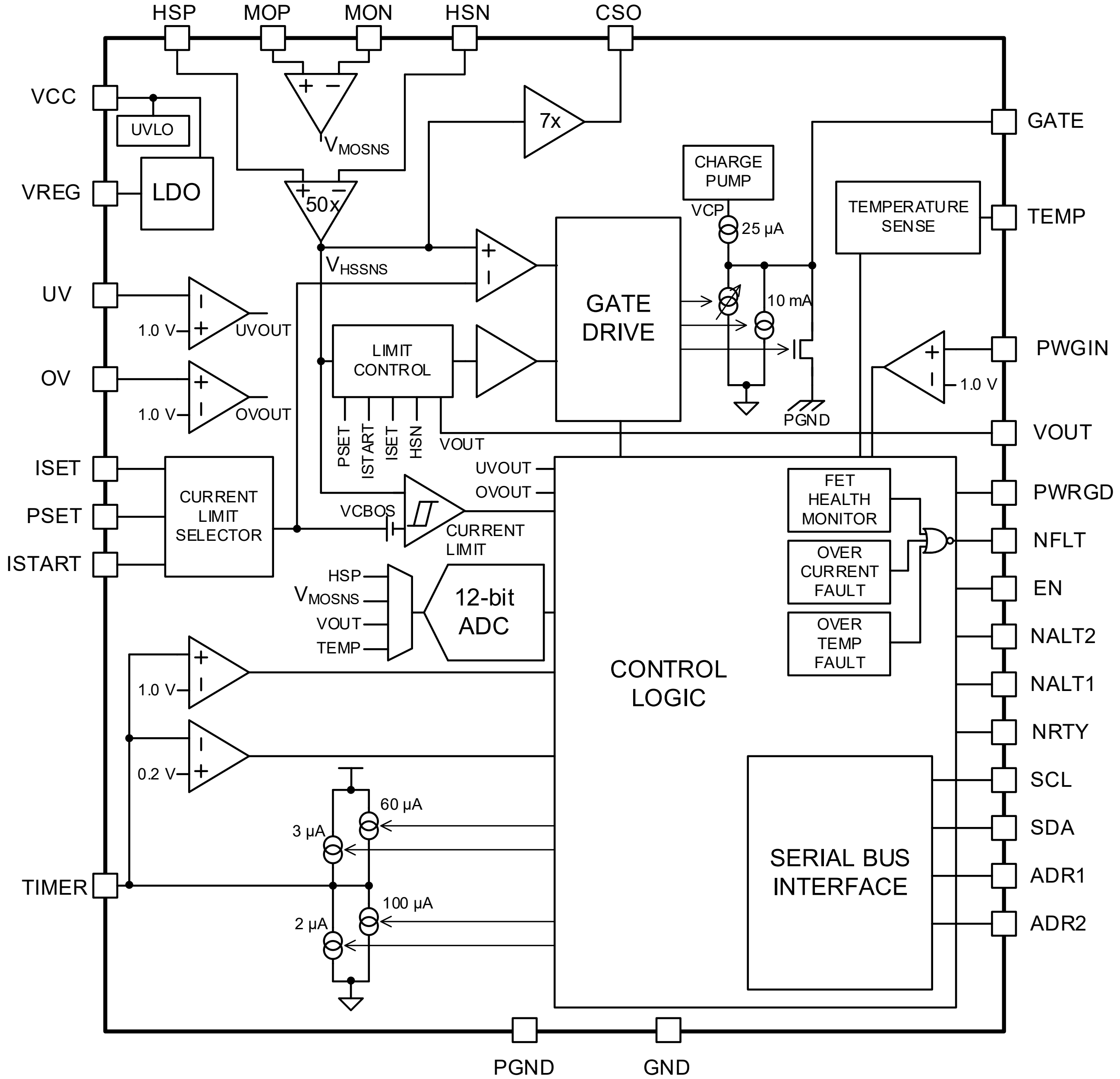
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	PSET	Power limit setting input
2	VREG	Internal regulator supply
3	ISET	Current limit setting input
4	ISTART	Start current limit setting input
5	TIMER	Timer with external capacitor
6	NFLT	Fault output
7	ADR1	PMBus device address 1
8	ADR2	PMBus device address 2
9	NC	Non Connection
10	NC	Non Connection
11	NC	Non Connection
12	EN	Device Enable
13	NALT1	SMB alert output 1 / Conversion (CONV)
14	NALT2	SMB alert output 2
15	SDA	PMBus data input / output
16	SCL	PMBus clock input
17	NRTY	Fault retry input
18	PWRGD	Power good output
19	CSO	Current sense amp output
20	VOUT	Output voltage feedback
21	PWGIN	Power good feedback
22	GND	Ground
23	PGND	Power ground
24	GATE	Gate driver output
25	TEMP	Temperature sense input
26	MON	Current monitor negative input
27	HSN	Current sense negative input
28	HSP	Current sense positive input
29	MOP	Current monitor positive input
30	VCC	Supply voltage input
31	UV	Under voltage input
32	OV	Over voltage input
−	EXP-PAD	Connect EXP-PAD to ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
VCC Power Supply Voltage	V_{CC}	−0.3 to +30	V
GATE Voltage	V_{GATE}	−0.3 to +42	V
VREG Voltage	V_{REG}	−0.3 to +4.5	V
PSET, ISET, ISTART, TIMER, ADR1, ADR2, NRTY, PWGIN, TEMP, OV, UV Voltages	V_{I1}	−0.3 to +4.5	V
SDA, SCL Voltages	V_{I2}	−0.3 to +7.0	V
MON, MOP, HSN, HSP, EN, VOUT Voltages	V_{I3}	−0.3 to +30	V
NFLT, NALT1, NALT2, PWRGD, CSO Voltages	V_O	−0.3 to +30	V
Maximum Junction Temperature	Tjmax	125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*
Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	11	5	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VCC Power Supply Voltage	V_{CC}	4.5	12	20	V
MOP, HSP Input Voltages	V_{IN}	2	12	20	V
Operating Temperature	Topr	−40	+25	+85	°C

Electrical Characteristics

(V_{CC} = 4.5 V to 20 V, $V_{CC} \geq V_{HSP}$ and V_{MOP}, V_{HSP} = 2 V to 20 V, V_{SENSE_HS} = ($V_{HSP} - V_{HSN}$) = 0 V, V_{SENSE_MO} = ($V_{MOP} - V_{MON}$) = 0 V, Ta = −40 °C to +85 °C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General (VCC, VREG)						
Undervoltage Lockout	V_{THUVLO}	3.0	3.2	3.4	V	VCC rising
Undervoltage Hysteresis	$V_{HYSTUVLO}$	0.5	0.7	0.9	V	
VREG Voltage	V_{REG}	2.68	2.70	2.72	V	0 μA ≤ I_{VREG} ≤ 100 μA; C_{VREG} = 1 μF
Quiescent Current	I_{CC}	−	−	5.5	mA	GATE on and power monitor running
Voltage Sense (UV, OV, PWGIN)						
Voltage Sense Input Current	I_{VSIN}	−	−	50	nA	Per individual pin, UV, OV, PWGIN ≤ 2.7 V
Voltage Sense Threshold	V_{THS}	0.99	1.00	1.01	V	UV falling, and OV rising
Voltage Sense Threshold Hysteresis	V_{HYST1}	45	60	75	mV	UV and OV
	V_{HYST2}	50	60	70	mV	PWGIN
UV Glitch Filter	GF_{UV}	2.0	3.8	7.0	μs	50 mV overdrive
OV Glitch Filter	GF_{OV}	1.5	2.8	3.5	μs	50 mV overdrive
PWGIN Glitch Filter	GF_{PWGIN}	−	1	−	μs	Asserting and deasserting of PWRGD pin
UV Propagation Delay	PD_{UV}	−	5	8	μs	UV low to GATE pull-down active
OV Propagation Delay	PD_{OV}	−	3	5	μs	OV high to GATE pull-down active
Gate Driver (GATE)						
GATE Drive Voltage ($\Delta V_{GATE} = V_{GATE} - V_{OUT}$)	ΔV_{GATE1}	10.0	11.5	14.0	V	20 V ≥ V_{CC} ≥ 8 V, I_{GATE} ≤ 5 μA
	ΔV_{GATE2}	8.0	11.5	14.0	V	V_{HSP} = V_{CC} = 5 V, I_{GATE} ≤ 5 μA
	ΔV_{GATE3}	7	10	14	V	V_{HSP} = V_{CC} = 4.5 V, I_{GATE} ≤ 1 μA
GATE Pull-Up Current	I_{GATEUP}	−30	−25	−20	μA	V_{GATE} = 0 V
GATE Pull-Down Regulation Current	I_{GATEDN_REG}	45	60	75	μA	V_{GATE} ≥ 2 V, V_{ISET} = 1.0 V, $V_{HSP} - V_{HSN}$ = 30 mV
GATE Pull-Down Slow Current	I_{GATEDN_SLOW}	5	10	15	mA	V_{GATE} ≥ 2 V
GATE Pull-Down Fast Current	I_{GATEDN_FAST}	750	1500	2250	mA	V_{GATE} ≥ 12 V, V_{CC} ≥ 12 V
Timer (TIMER)						
TIMER Pull-Up Current at POR	$I_{TIMERUPPOR}$	−2	−3	−4	μA	V_{TIMER} = 0.5 V
TIMER Pull-Up Current at Over Current Fault	$I_{TIMERUPFLT}$	−64	−60	−56	μA	0.2 V ≤ V_{TIMER} ≤ 1 V
TIMER Pull-Down Current at Fault Retry	$I_{TIMERDNRT}$	1.7	2.0	2.3	μA	V_{TIMER} = 0.5 V
TIMER Pull-Down Current for Hold	$I_{TIMERDNHOLD}$	−	100	−	μA	V_{TIMER} = 0.5 V
TIMER High Threshold	V_{TIMERH}	0.98	1.00	1.02	V	
TIMER Low Threshold	V_{TIMERL}	0.18	0.20	0.22	V	
TIMER Glitch Filter	GF_{TIMER}	−	10	−	μs	
Minimum POR Duration	t_{POR}	−	27	−	ms	Minimum initial insertion delays regardless of C_{TIMER} value

Electrical Characteristics - continued

(V_{CC} = 4.5 V to 20 V, V_{CC} ≥ V_{HSP} and V_{MOP}, V_{HSP} = 2 V to 20 V, V_{SENSE_HS} = (V_{HSP} − V_{HSN}) = 0 V, V_{SENSE_MO} = (V_{MOP} − V_{MON}) = 0 V, Ta = −40 °C to +85 °C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current Sense (HSP, HSN, CSO)						
Hot Swap Pin Input Current	I_{SNSP}, I_{SNSN}	−	−	150	µA	Per individual pin, V_{HSP}, V_{HSN} = 20 V
Input Current Imbalance	ΔI_{SNS}	−	−	5	µA	ΔI_{SNS} = I_{SNSP} − I_{SNSN}
Hot Swap Sense Current Limit Voltage	$V_{SENSECL0}$	19.75	20.00	20.25	mV	V_{ISET} > 1.65 V, V_{GATE} = V_{HSP} + 3 V, I_{GATE} = 0 µA
ISET Constant Power Inactive Voltage *(Note 6)*	$V_{SENSECL1}$	24.75	25.00	25.25	mV	V_{ISET} = 1.25 V, V_{DS} < 2 V
	$V_{SENSECL2}$	19.75	20.00	20.25	mV	V_{ISET} = 1.00 V, V_{DS} < 2 V
	$V_{SENSECL3}$	14.75	15.00	15.25	mV	V_{ISET} = 0.75 V, V_{DS} < 2 V
PSET Constant Power Active Voltage *(Note 7)*	$V_{SNSPOC1}$	9.25	10.00	10.75	mV	V_{ISET} > 1.65 V, V_{PSET} = 0.25 V, V_{DS} = 4 V
	$V_{SNSPOC2}$	4.65	5.00	5.35	mV	V_{ISET} > 1.65 V, V_{PSET} = 0.25 V, V_{DS} = 8 V
	$V_{SNSPOC3}$	1.70	2.00	2.30	mV	V_{ISET} > 1.65 V, V_{PSET} = 0.25 V, V_{DS} = 20 V
ISTART Current Limit Voltage	V_{ISTOC1}	4.7	5.0	5.3	mV	STRT_UP_IOUT_LIM = 3, V_{ISET} > 1.65 V
	V_{ISTOC2}	3.7	4.0	4.3	mV	V_{ISTART} = 0.2 V
ISTART Over Current Limit Clamp Voltage	V_{ISTOC_CLMP}	1.6	2.0	2.4	mV	V_{ISTART} = 0 V or STRT_UP_IOUT_LIM = 0
Circuit Breaker Offset	V_{CBOS}	0.60	0.88	1.12	mV	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}
Severe Over Current Limit Voltage Threshold	$V_{SNSSOC1}$	23	25	27	mV	V_{ISET} > 1.65 V, V_{PSET} > 1.1 V, optional select PMBus (125 %)
	$V_{SNSSOC2}$	28	30	32	mV	V_{ISET} > 1.65 V, V_{PSET} > 1.1 V, optional select PMBus (150 %)
	$V_{SNSSOC3}$	38	40	42	mV	V_{ISET} > 1.65 V, V_{PSET} > 1.1 V, optional select PMBus (200 %)
	$V_{SNSSOC4}$	43	45	47	mV	V_{ISET} > 1.65 V, V_{PSET} > 1.1 V, default at power-up (225 %)
Severe Over Current Short Glitch Filter Duration	$SOCS_{GF}$	100	160	220	ns	V_{SENSE_HS} step = 18 mV to (2 mV above V_{SNSOC_MAX})
Severe Over Current Long Glitch Filter Duration (Default)	$SOCL_{GF}$	530	715	900	ns	V_{SENSE_HS} step = 18 mV to (2 mV above V_{SNSOC_MAX})
Severe Over Current Response Time with Short Glitch Filter	$SOCS_{RT}$	200	260	320	ns	V_{SENSE_HS} step = 18 mV to (2 mV above V_{SNSOC_MAX})
Severe Over Current Response Timer with Long Glitch Filter	$SOCL_{RT}$	630	815	1000	ns	V_{SENSE_HS} step = 18 mV to (2 mV above V_{SNSOC_MAX})
CSO Gain	A_{CSO}	−	350	−	V/V	CSO = V_{SENSE_HS} x 350, V_{CC} > CSO + 2 V
CSO Total Output Error	CSO_{ERR1}	−1.6	0	+1.6	%	V_{SENSE_HS} = 20 mV, I_{CSO} ≤ 1 mA, C_{CSO} = 1 nF
	CSO_{ERR2}	−3.0	0	+3.0	%	V_{SENSE_HS} = 10 mV, I_{CSO} ≤ 1 mA, C_{CSO} = 1 nF
CSO Low Voltage	CSO_{VL}	−	40	−	mV	
CSO Current Limiting	CSO_{CL}	−	5	−	mA	CSO short-circuit current

(Note 6) $V_{SENSECL}$ = V_{ISET} / 50, V_{GATE} = V_{HSP} + 3 V, I_{GATE} = 0 µA, V_{DS} = V_{HSN} – V_{OUT}

(Note 7) FET power limit = (V_{PSET} x 8) / (50 x R_S), constant power active when V_{DS} > (V_{PSET} x 8) / I_{SET}

Electrical Characteristics - continued

(V_{CC} = 4.5 V to 20 V, $V_{CC} \geq V_{HSP}$ and V_{MOP}, V_{HSP} = 2 V to 20 V, $V_{SENSE\_HS} = (V_{HSP} - V_{HSN})$ = 0 V, $V_{SENSE\_MO} = (V_{MOP} - V_{MON})$ = 0 V, Ta = −40 °C to +85 °C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Over Current Setting (ISET, ISTART, PSET)						
ISET Reference Select Threshold	V_{ISETTH}	1.35	1.50	1.65	V	If $V_{ISET} > V_{ISETTH}$, V_{CLREF} is used
Over Current Limit Internal Reference Voltage	V_{CLREF}	−	1	−	V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	A_{CSAMP}	−	50	−	V/V	Accuracies included in total sense voltage accuracies
ISET Recommended Input Range	V_{ISET}	0.25	−	1.25	V	5 mV to 25 mV V_{SENSE} *(Note 8)* over current
ISTART Input Range	V_{ISTART}	0.10	−	1.25	V	Tie ISTART to VREG to disable start-up over current
PSET Reference Select Threshold	V_{PSETTH}	1.35	1.50	1.65	V	If $V_{PSET} > V_{PSETTH}$, constant power over current is disabled
Input Current	I_{INCL}	−	−	100	nA	Per individual pin, V_{ISET}, V_{ISTART}, $V_{PSET} \leq$ 2 V
Remote Diode Temperature Sensor (TEMP, External Transistor is 2N3904)						
Operating Range	T_{TEMP}	−55	−	+150	°C	Limited by external diode
Accuracy	T_{ACCU}	−	±1	±10	°C	Ta = T_{DIODE} = −40 °C to +85 °C
Resolution	T_{RESO}	−	0.25	−	°C	LSB size
Output Current Source	I_{TEMPL}	−	5	−	µA	Low Level
	I_{TEMPM}	−	32	−	µA	Medium Level
	I_{TEMPH}	−	140	−	µA	High Level
Maximum Series Resistance for External Diode	R_{SERI}	−	−	100	Ω	For < ±0.5 °C additional error, C_{PARA} = 0 F
Maximum Parallel Capacitance for External Diode	C_{PARA}	−	−	1	nF	R_{SERI} = 0 Ω
Power Monitoring (MOP, MON, HSP, VOUT)						
Monitor Pin Input Current	I_{MO}	−	−	25	nA	Per individual pin, MOP, MON, V_{MOP}, V_{MON} = 20 V
VOUT Input Current	I_{VOUT}	−	−	40	µA	V_{OUT} = 20 V
Current Monitor ADC Continuous Mode Conversion Time	t_{ICCONV}	−	144	165	µs	One sample of V_{MOP} - V_{MON}; from continuous conversion started to valid data in register
Voltage (V_{HSP}) Monitor ADC Continuous Mode Conversion Time	t_{VICONV}	−	64	73	µs	One sample of V_{HSP}; from continuous conversion started to valid data in register
Voltage (V_{OUT}) Monitor ADC Continuous Mode Conversion Time	t_{VICONV}	−	64	73	µs	One sample of V_{OUT}; from continuous conversion started to valid data in register
Current Monitor Absolute Error *(Note 9)*	$I_{MONERR1}$	−0.7	−	+0.7	%	V_{SENSE_MO} = 25 mV
	$I_{MONERR2}$	−0.7	−	+0.7	%	V_{SENSE_MO} = 20 mV
	$I_{MONERR3}$	−1.0	−	+1.0	%	V_{SENSE_MO} = 20 mV, 16-sample averaging
	$I_{MONERR4}$	−2.8	−	+2.8	%	V_{SENSE_MO} = 20 mV, no averaging
	$I_{MONERR5}$	−0.8	−	+0.8	%	V_{SENSE_MO} = 15 mV
	$I_{MONERR6}$	−1.1	−	+1.1	%	V_{SENSE_MO} = 10 mV
	$I_{MONERR7}$	−2.0	−	+2.0	%	V_{SENSE_MO} = 5 mV
	$I_{MONERR8}$	−4.3	−	+4.3	%	V_{SENSE_MO} = 2.5 mV
Voltage Monitor Absolute Error	V_{MONERR}	−1.0	−	+1.0	%	V_{HSP}, V_{OUT} = 5 V to 20 V
Power Monitor Absolute Error	P_{MONERR}	−1.7	−	+1.7	%	V_{SENSE_MO} = 20 mV, V_{HSP} = 12 V

(Note 8) V_{SENSE} is the potential difference of R_{SENSE}. R_{SENSE} is external current sense resistor.

(Note 9) V_{CC} = 4.5 V to 15 V, V_{MOP} = 2 V to 15 V, 128-sample averaging unless otherwise noted

Electrical Characteristics - continued

(V_{CC} = 4.5 V to 20 V, V_{CC} ≥ V_{HSP} and V_{MOP}, V_{HSP} = 2 V to 20 V, V_{SENSE_HS} = (V_{HSP} − V_{HSN}) = 0 V, V_{SENSE_MO} = (V_{MOP} − V_{MON}) = 0 V, Ta = −40 °C to +85 °C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Logic I/O (EN, NRTY, NFLT, PWRGD, NALT1, NALT2)						
Input Logic-high Threshold	V_{IH}	1.1	−	−	V	Per individual pin, EN, NRTY, NALT1
Input Logic-low Threshold	V_{IL}	−	−	0.8	V	Per individual pin, EN, NRTY, NALT1
Input Glitch Filter	GF_I	−	1	−	μs	Per individual pin, EN, NRTY, NALT1
NRTY Internal Pull-Up Current	I_{NRTY}	−	8	−	μA	
Open-drain Output Low Voltage	V_{OD1}	−	−	0.4	V	Per individual pin, NFLT, PWRGD, NALT1, NALT2, I_{OD1} = 1 mA
	V_{OD2}	−	−	1.5	V	Per individual pin, NFLT, PWRGD, NALT1, NALT2, I_{OD2} = 5 mA
Open-drain Leakage Current	I_{OD1}	−	−	100	nA	Per individual pin, NFLT, PWRGD, NALT1, NALT2, V_{OD1} ≤ 2 V, Output high-Z
	I_{OD2}	−	−	1	μA	Per individual pin, NFLT, PWRGD, NALT1, NALT2, V_{OD2} = 20 V, Output high-Z
VCC That Guarantees Valid PWRGD Output	$V_{PWRGDMIN}$	1.2	−	−	V	PWRGD Sink Current = 100 μA, PWRGD Threshold Voltage = 0.4 V
Quad Level Device Address Input (ADR1, ADR2)						
Address Set to 00	V_{ADRI00}	−	−	0.8	V	Connect to GND
Input Current for Address Set to 00	I_{ADRI00}	−40	−22	−	μA	V_{ADRx} = 0 V to 0.8 V (x = 0,1)
Address Set to 01	R_{ADRI01}	135	150	165	kΩ	Resistor to GND
Address Set to 10	I_{ADRI10}	−1	0	+1	μA	No connect state, maximum leakage current allowed
Address Set to 11	V_{ADRI11}	2	−	−	V	Connect to VREG
Input Current for Address Set to 11	I_{ADR11}	−	3	10	μA	V_{ADRx} = 2.0 V to V_{REG} (x = 0,1), must not exceed the maximum allowable current draw from V_{REG}
Serial Bus Digital Interface (SCL, SDA)						
Input High Voltage	V_{SBIH}	1.1	−	−	V	
Input Low Voltage	V_{SBIL}	−	−	0.8	V	
Output Low Voltage	V_{SBOL}	−	−	0.4	V	I_{OL} = 20 mA
Input Leakage Current	I_{SBLK1}	−10	−	+10	μA	
	I_{SBLK2}	−5	−	+5	μA	Device is not powered
Nominal Bus Voltage	V_{DD}	2.7	−	5.5	V	3 V to 5 V ± 10 %
Pin Capacitance	C_{SB}	−	5	−	pF	
Input Glitch Filter	t_{SB}	0	−	50	ns	

Typical Performance Curves

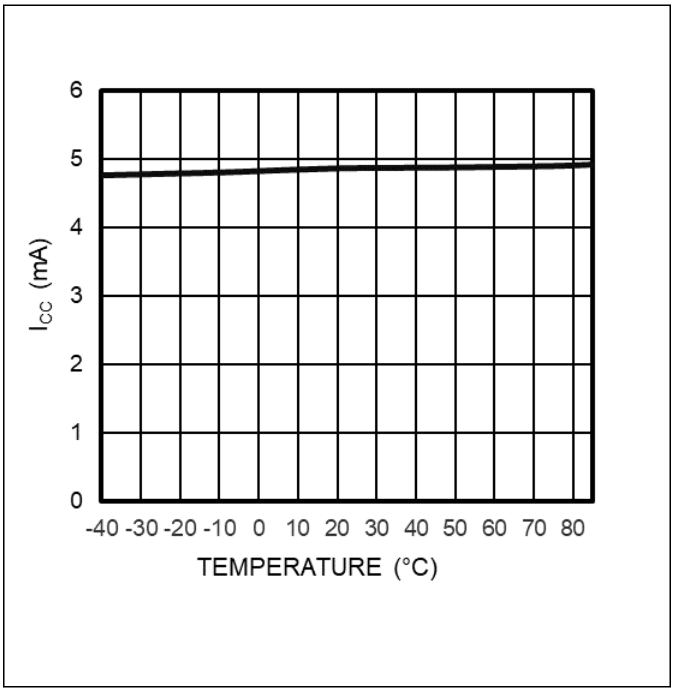


Figure 1. Supply Current (I_{CC}) vs Temperature
(V_{CC} = 12 V)

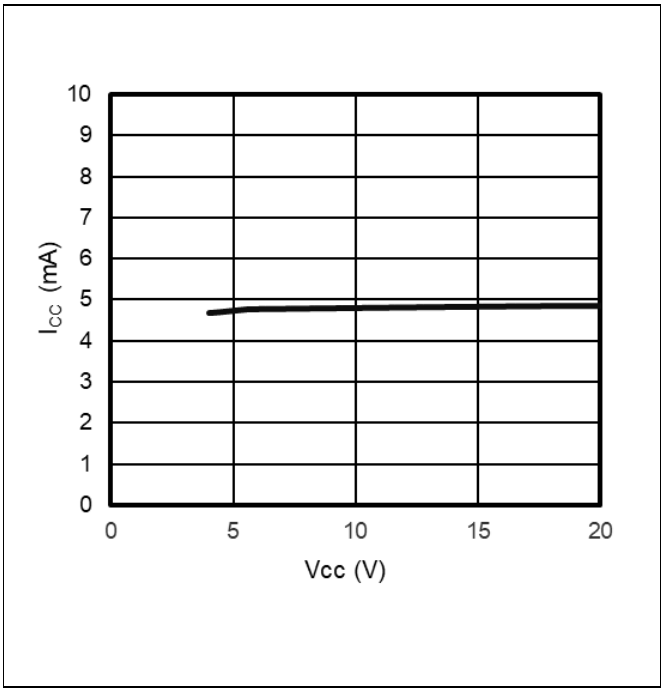


Figure 2. Supply Current (I_{CC}) vs V_{CC}
(Temperature = 25 °C)

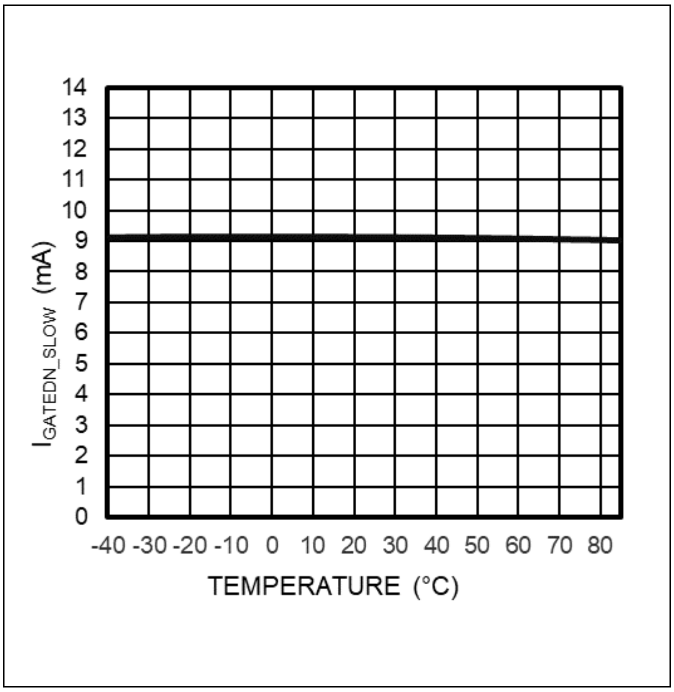


Figure 3. GATE Pull-Down Slow Current (I_{GATEDN_SLOW}) vs
Temperature (V_{CC} = 12 V)

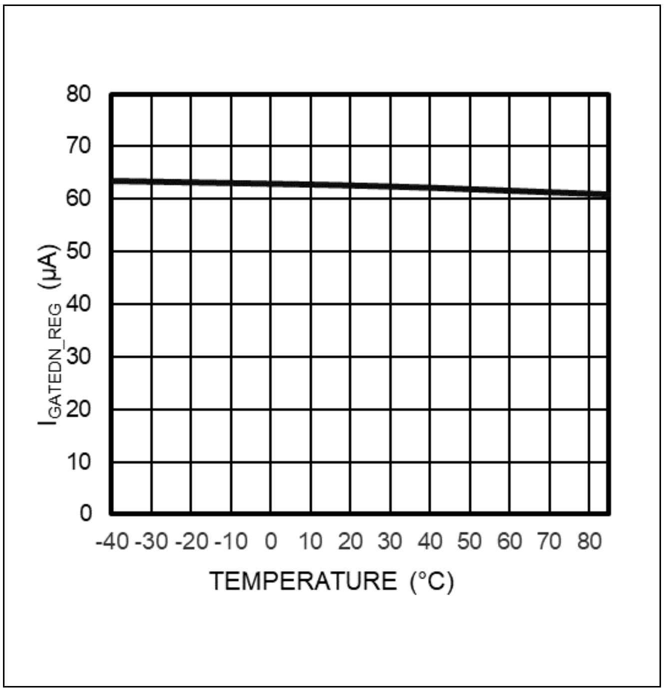


Figure 4. GATE Pull-Down Regulation Current (I_{GATEDN_REG})
vs Temperature (V_{CC} = 12 V)

Typical Performance Curves - continued

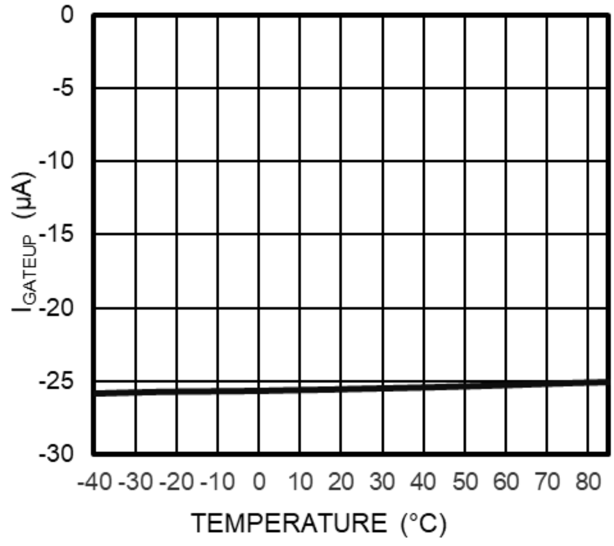


Figure 5. GATE Pull-Up Current (I_{GATEUP}) vs Temperature (V_{CC} = 12 V)

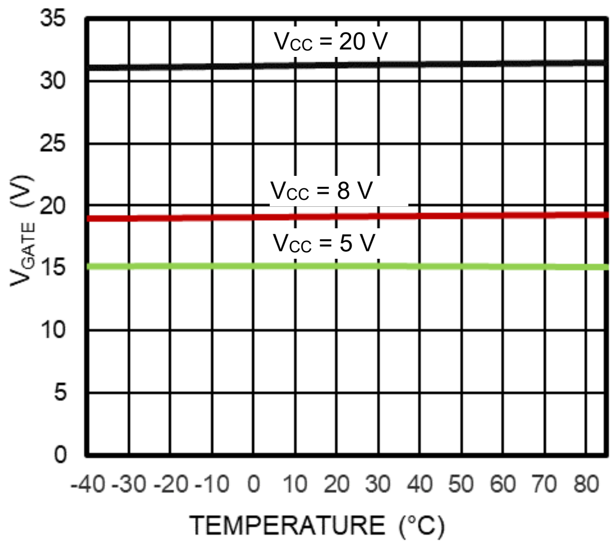


Figure 6. V_{GATE} (5 µA Load) vs Temperature

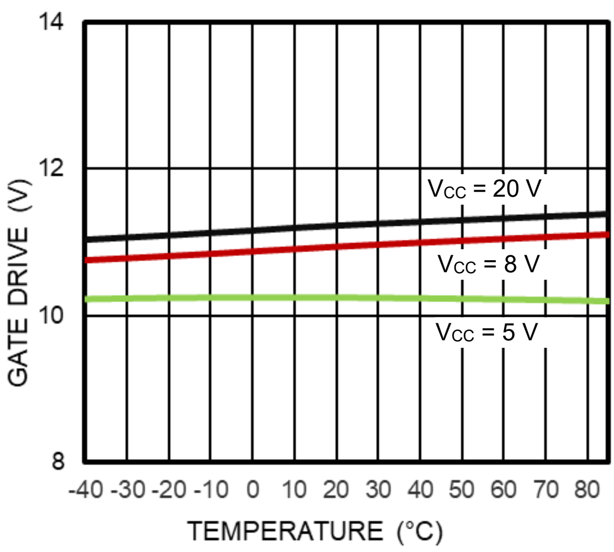


Figure 7. GATE Drive (5 µA Load) vs Temperature

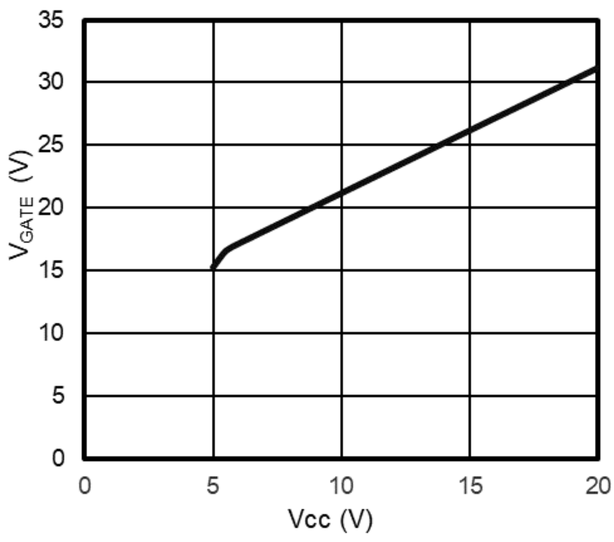


Figure 8. V_{GATE} (5 µA Load) vs V_{CC} (Temperature = 25 °C)

Typical Performance Curves - continued

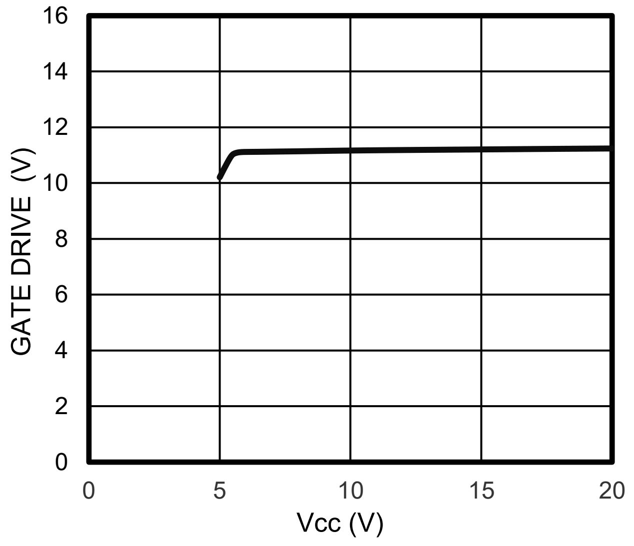


Figure 9. GATE Drive vs V_{CC}
(Temperature = 25 °C)

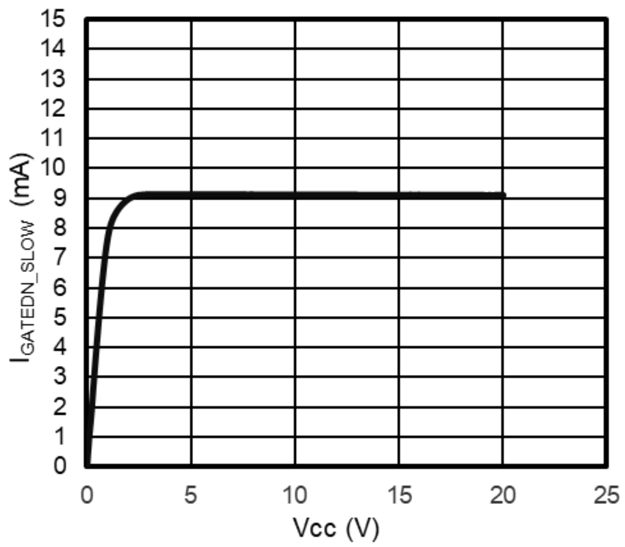


Figure 10. I_{GATEDN_SLOW} vs V_{CC}
(Temperature = 25 °C)

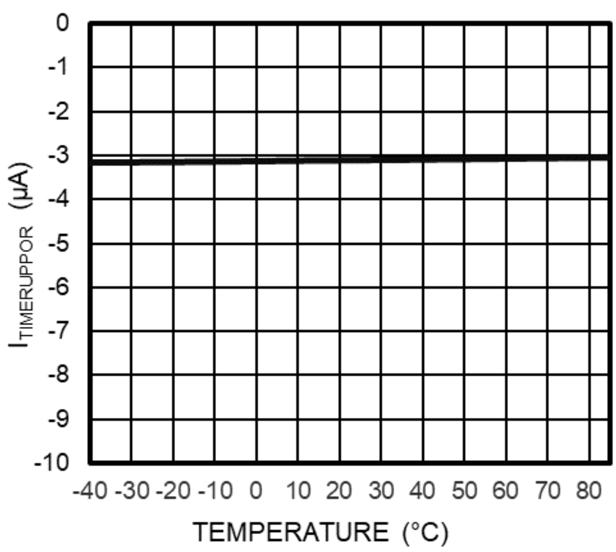


Figure 11. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$)
vs Temperature (Temperature = 25 °C)

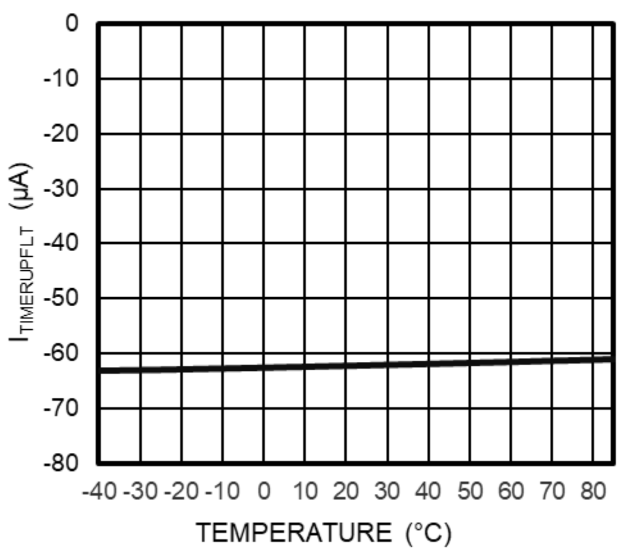


Figure 12. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$)
vs Temperature (V_{CC} = 12 V)

Typical Performance Curves - continued

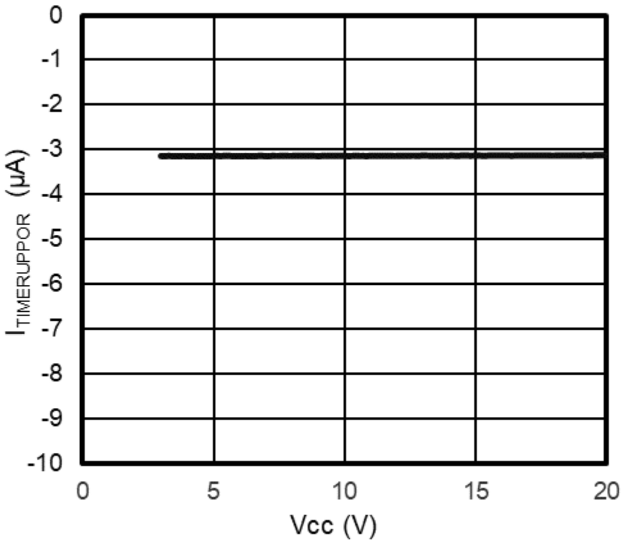


Figure 13. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs V_{CC} (Temperature = 25 °C)

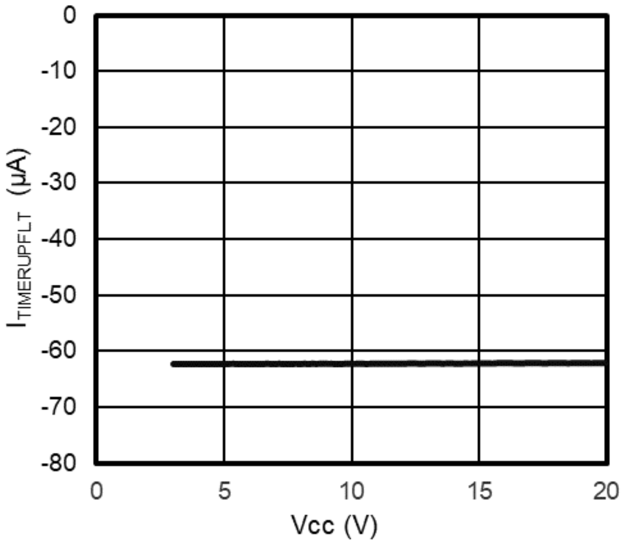


Figure 14. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs V_{CC} (Temperature = 25 °C)

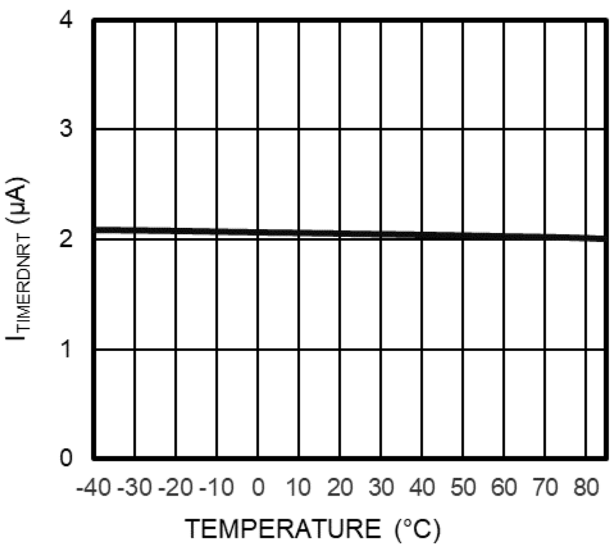


Figure 15. TIMER Pull-Down Current Retry ($I_{TIMERDNRT}$) vs Temperature (V_{CC} = 12 V)

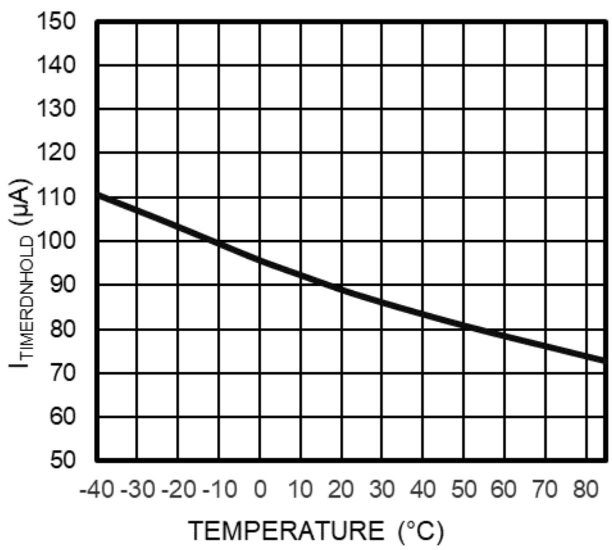


Figure 16. TIMER Pull-Down Current Hold ($I_{TIMERDNHOLD}$) vs Temperature (V_{CC} = 12 V)

Typical Performance Curves - continued

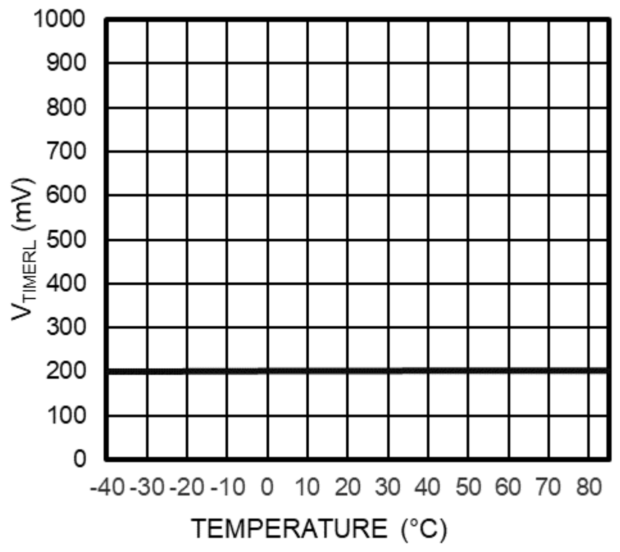


Figure 17. TIMER Low Threshold (V_{TIMERL}) vs Temperature (V_{CC} = 12 V)

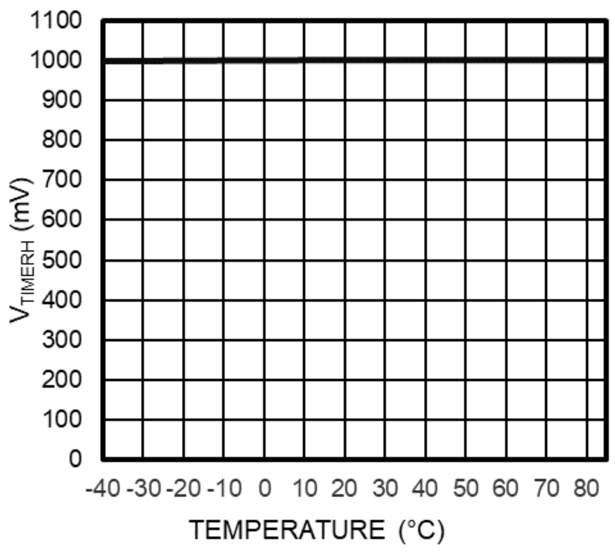


Figure 18. TIMER High Threshold (V_{TIMERH}) vs Temperature (V_{CC} = 12 V)

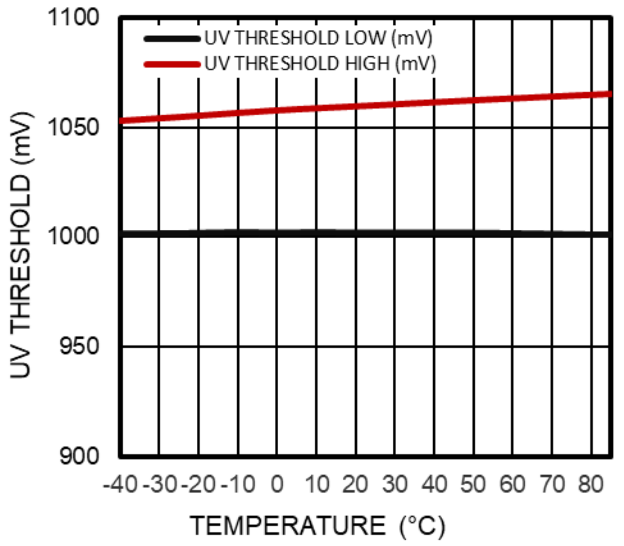


Figure 19. UV Threshold vs Temperature (V_{CC} = 12 V)

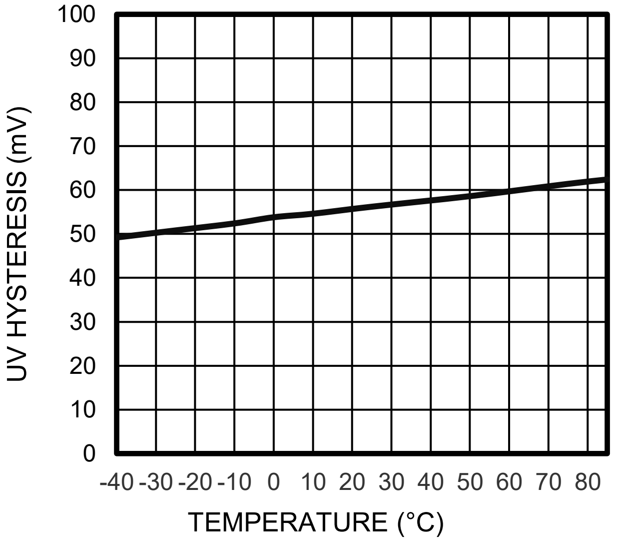


Figure 20. UV Hysteresis vs Temperature (V_{CC} = 12 V)

Typical Performance Curves - continued

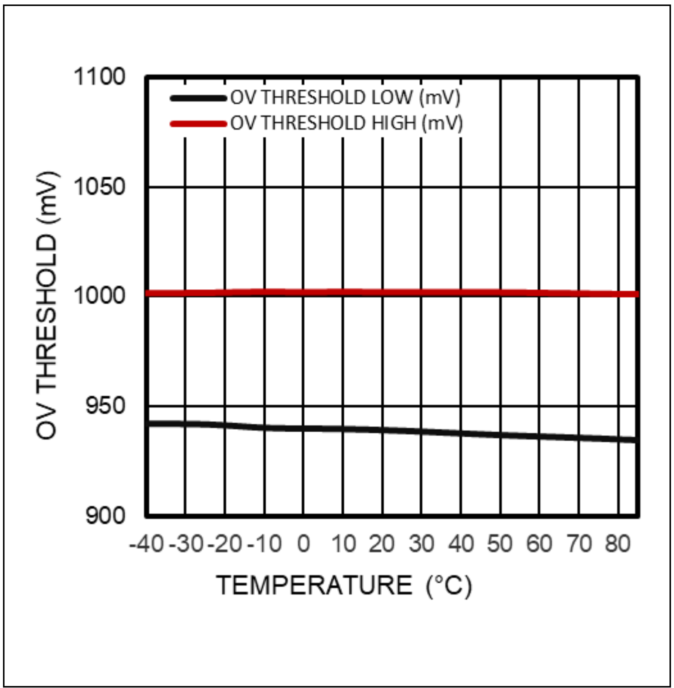


Figure 21. OV Threshold vs Temperature
(V_{CC} = 12 V)

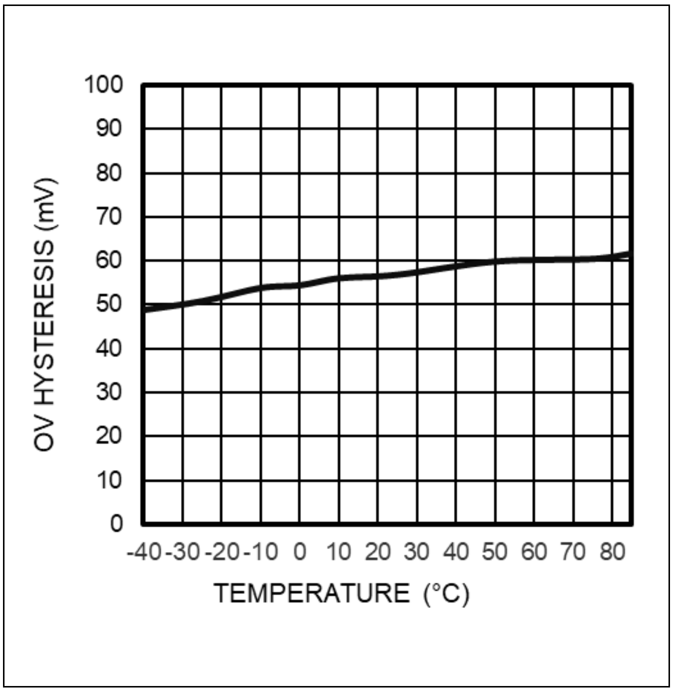


Figure 22. OV Hysteresis vs Temperature
(V_{CC} = 12 V)

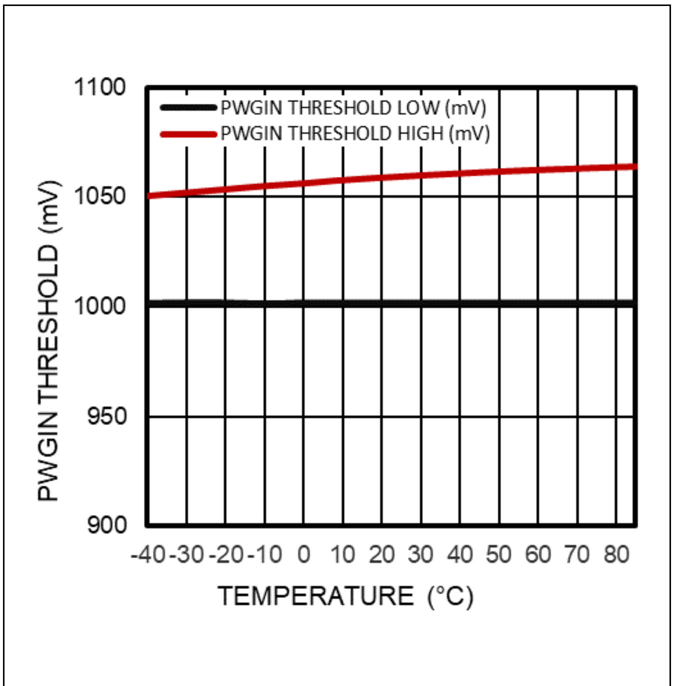


Figure 23. PWGIN Threshold vs Temperature
(V_{CC} = 12 V)

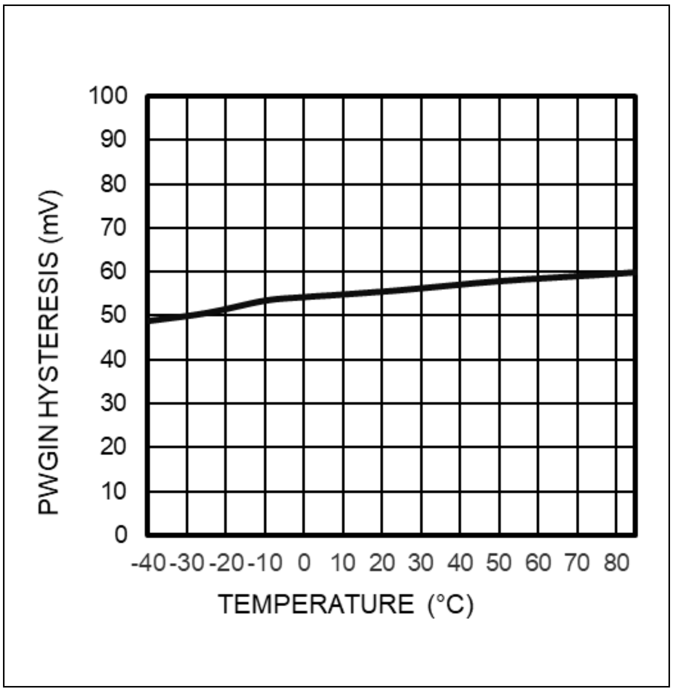


Figure 24. PWGIN Hysteresis vs Temperature
(V_{CC} = 12 V)

Typical Performance Curves - continued

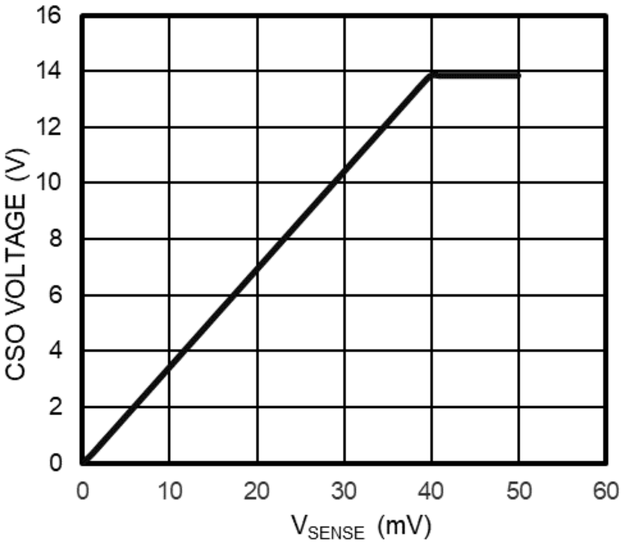


Figure 25. CSO Voltage vs V_{SENSE}
(V_{CC} = 16 V)

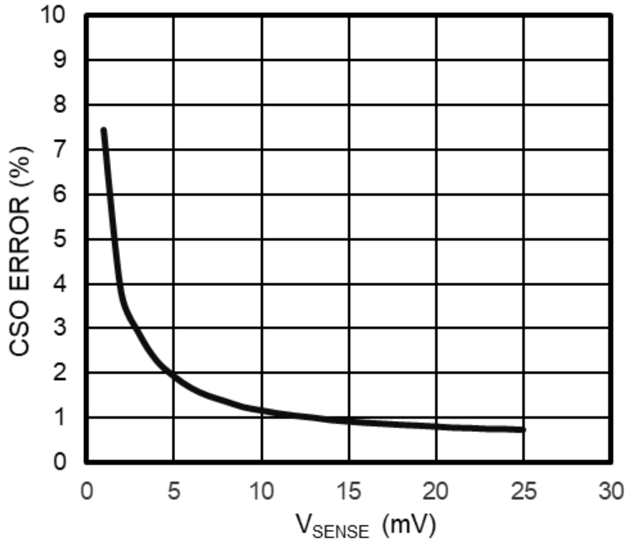


Figure 26. CSO Error vs V_{SENSE}
(V_{CC} = 12 V)

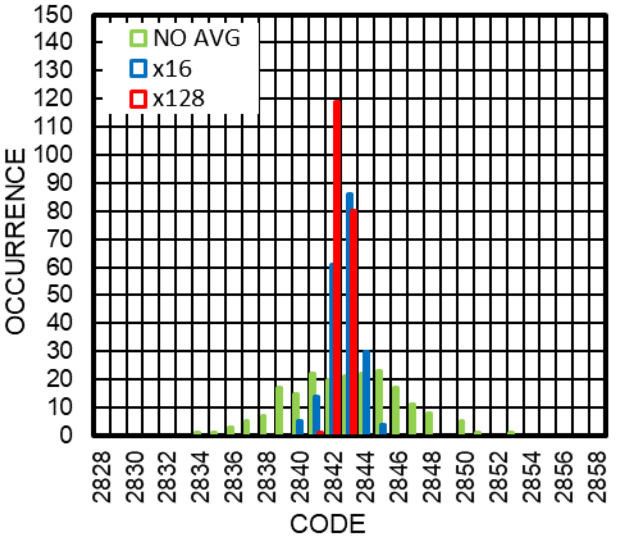


Figure 27. ADC Code Histogram (V_{SENSE} = 10 mV,
200 Measurements, V_{CC} = 12 V)

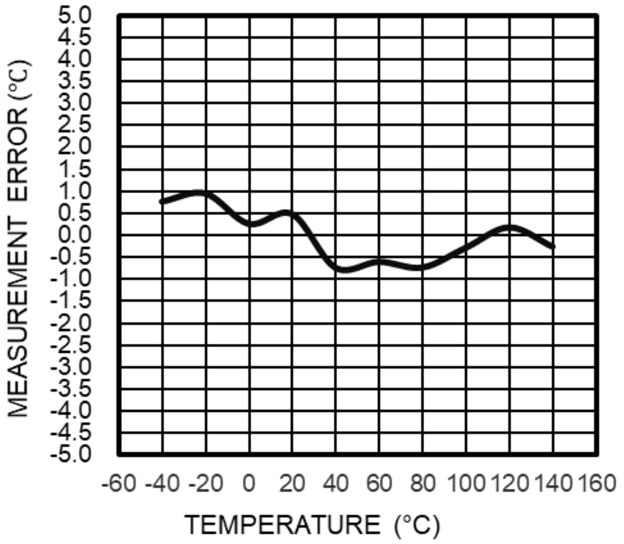


Figure 28. Measurement Error vs External Transistor
Temperature (V_{CC} = 12 V)

Typical Performance Curves - continued

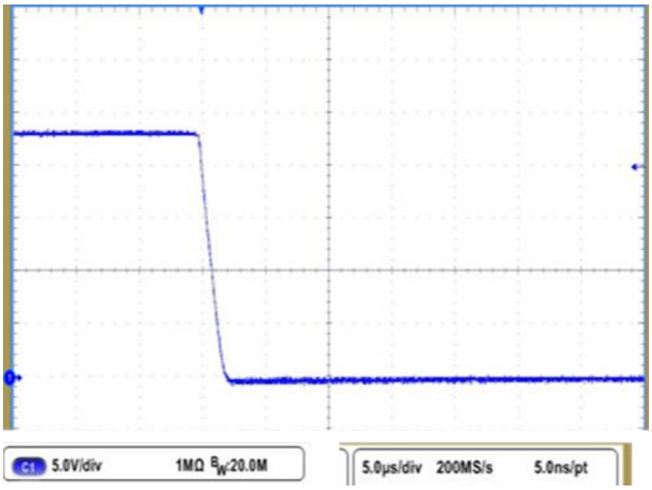


Figure 29. V_{GATE} Response to Severe Overcurrent Event
(V_{CC} = 12 V)

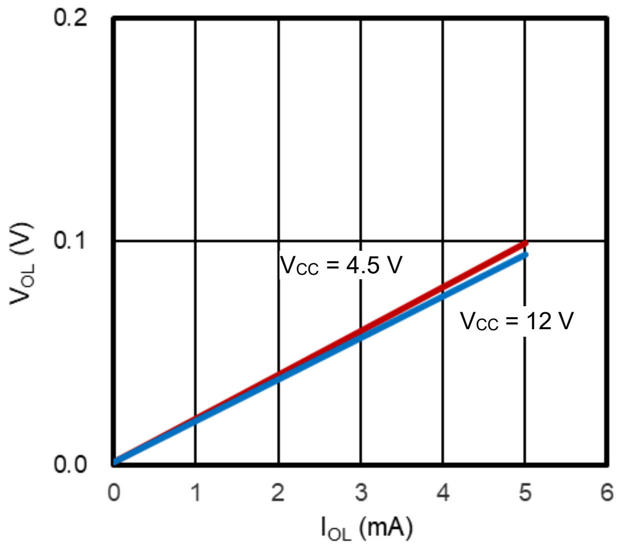


Figure 30. PWRGD Pin, V_{OL} vs I_{OL}

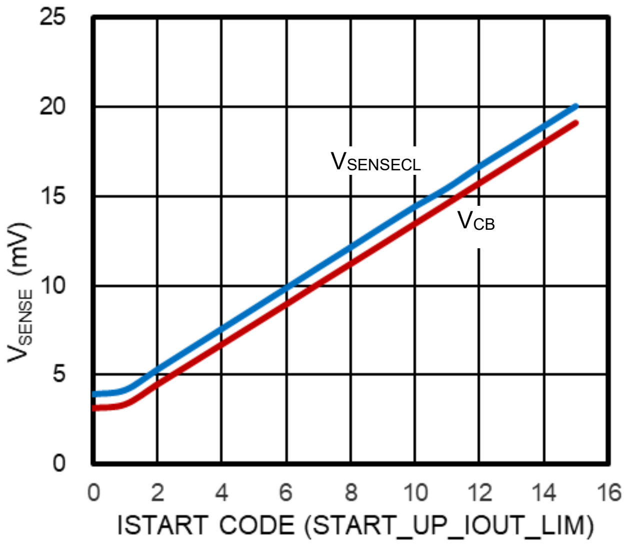


Figure 31. V_{SENSE} vs ISTART Code (STRT_UP_IOUT_LIM)
(V_{CC} = 12 V)

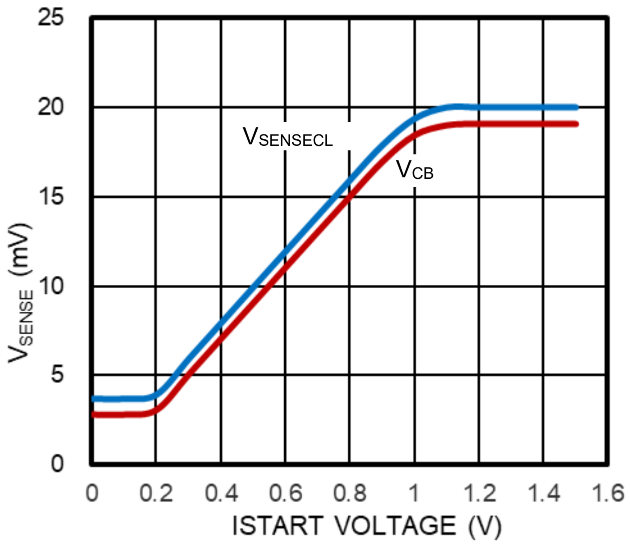


Figure 32. V_{SENSE} vs ISTART Voltage
(V_{CC} = 12 V)

Typical Performance Curves - continued

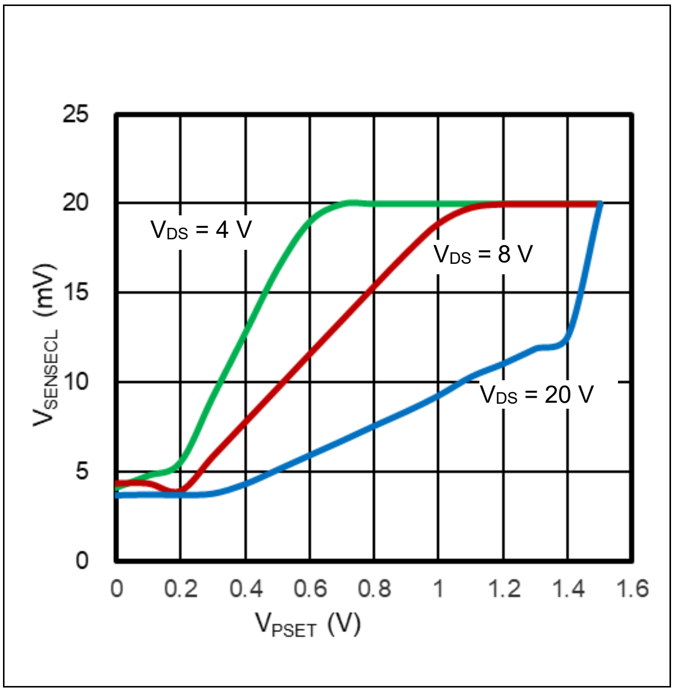


Figure 33. $V_{SENSECL}$ vs V_{PSET}
(V_{CC} = 12 V)

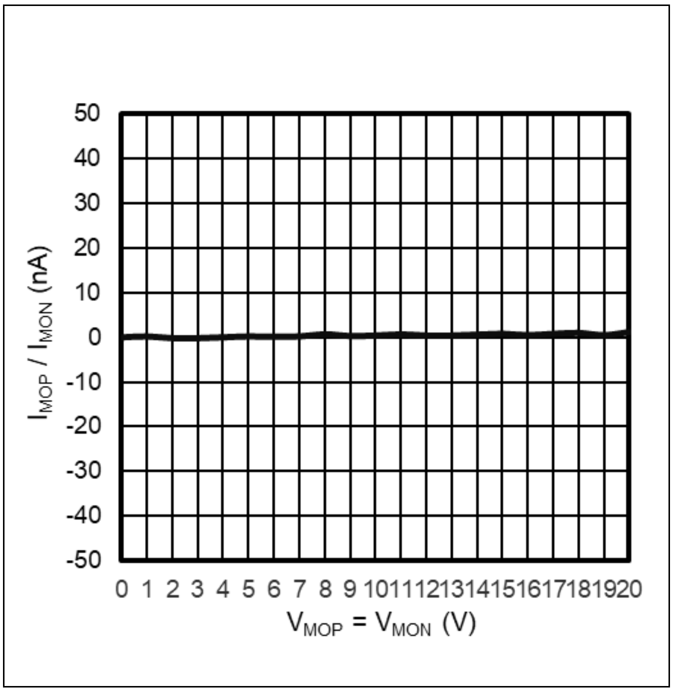


Figure 34. I_{MOP} / I_{MON} vs V_{MOP} / V_{MON} with V_{CC} = 20 V

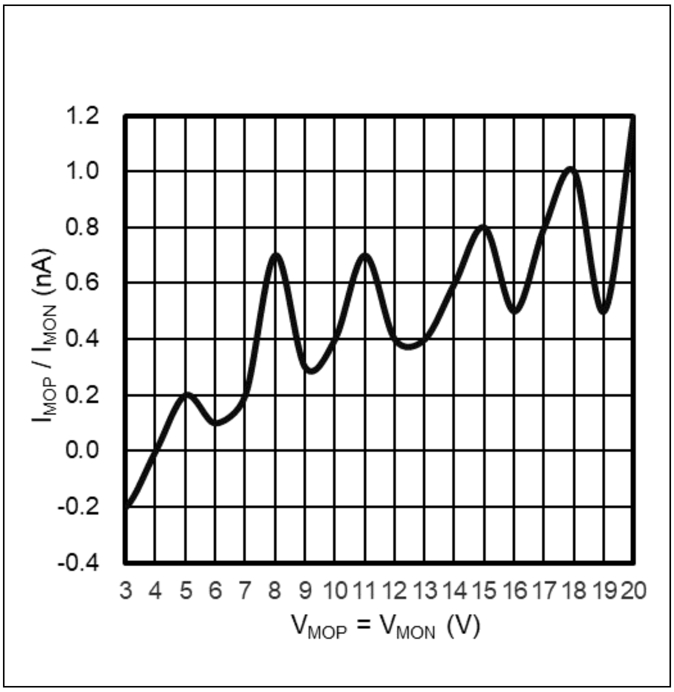


Figure 35. I_{MOP} / I_{MON} vs V_{MOP} / V_{MON} with V_{CC} = V_{MOP} = V_{MON}

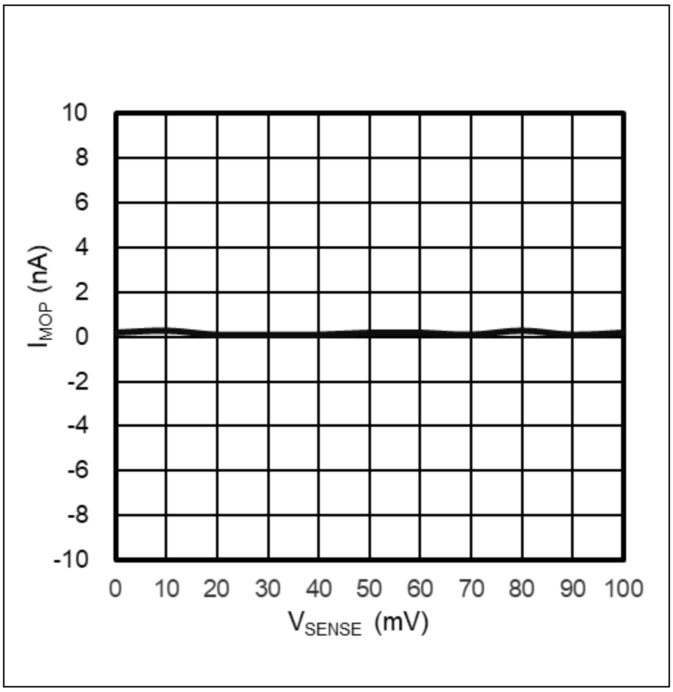


Figure 36. I_{MOP} vs V_{SENSE} with V_{CC} = V_{MOP} = 20 V

Typical Performance Curves - continued

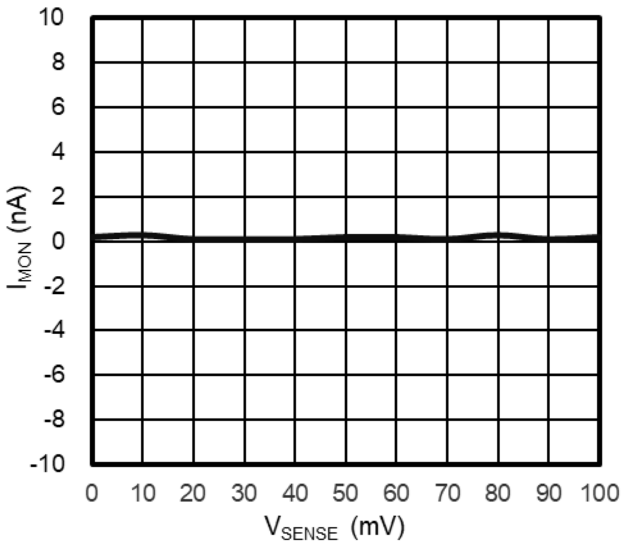


Figure 37. I_{MON} vs V_{SENSE} with V_{CC} = V_{MOP} = 20 V

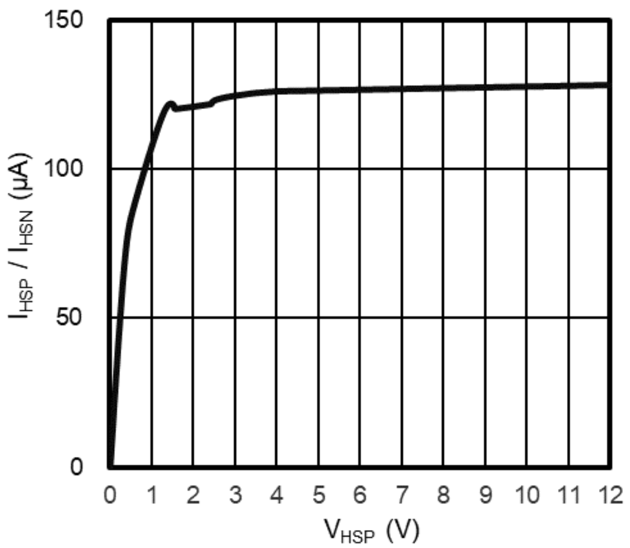


Figure 38. I_{HSP} / I_{HSN} vs V_{HSP}
(V_{CC} = 12 V)

Timing Chart

Serial Bus Timing Requirement

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{SCL}	10	–	1000	kHz
Bus Free Time	t_{BUF}	0.5	–	–	µs
Start Hold Time	t_{HD_STA}	0.26	–	–	µs
Start Setup Time	t_{SU_STA}	0.26	–	–	µs
Stop Setup Time	t_{SU_STO}	0.26	–	–	µs
Clock High Time	t_{HIGH}	0.26	–	50	µs
Clock Low Time	t_{LOW}	0.5	–	–	µs
Data Hold Time	t_{HD_SDA}	300	–	900	ns
Data Setup Time	t_{SU_SDA}	50	–	–	ns
Clock or Data Rise Time	t_R	20	–	120	ns
Clock or Data Fall Time	t_F	20	–	120	ns

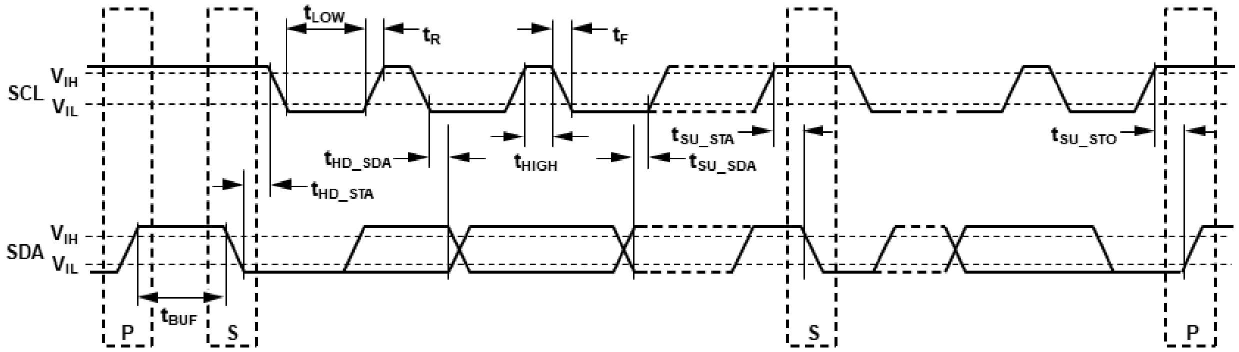


Figure 39. Serial Bus Timing Diagram

Description of Functions

The BD12780AMUV-LB controls inrush current upon hot plugging a circuit board to prevent backplane supply voltage sag and minimize impact on other circuits in the system by preventing unexpected resets.
The BD12780AMUV-LB has a current limit function programmable by an external voltage. It also has a programmable power limit function that controls the external power N-FET so that it can always be used within the Safe Operation Area. As the action after overcurrent detection, latch off or retry repeatedly can be selected based on the NRTY pin setting. If a downstream power rail is shorted, the severe overcurrent circuit quickly turns off the GATE pin within 320 ns after the short event. This prevents catastrophic damage to the system.
The BD12780AMUV-LB has precise monitors for system current, voltage, power, and remote temperature by 12-bit ADC, and the data can be read back through the PMBus.
The BD12780AMUV-LB has overvoltage and undervoltage protections and that are programmable by the external resistor dividers at UV pin and OV pin respectively. Also VOUT voltage level can be detected at PWGIN pin through the external resistor divider, and PWRGD signal is output when VOUT is valid level.

Power-up Sequence

When VCC exceeds UVLO voltage and VREG starts, then the reset of internal control logic is released, and the controller is ready to operate. The constant current driver starts 3 µA charging into external capacitor at TIMER pin after VCC exceeds the UV voltage level. The TIMER voltage reaches 1 V and the internal logic counter 27 ms is expired, the constant current driver at TIMER pin switches into 100 µA discharge current. The TIMER voltage crosses the 0.2 V voltage level, then the gate driver is ready to charge the GATE voltage. The time duration T_{INIT} is determined by the following equation.

$$T_{INIT} = (C_{TIMER} \times 1\ V / 3\ \mu A) + (C_{TIMER} \times 0.8\ V / 100\ \mu A)$$

The controller performs FET Health check in T_{INIT} duration. The GATE charging starts if the FET Health check is not failed. Once the GATE voltage exceeds HSN + 4 V, the VOUT is ready and PWRGD indicates high.

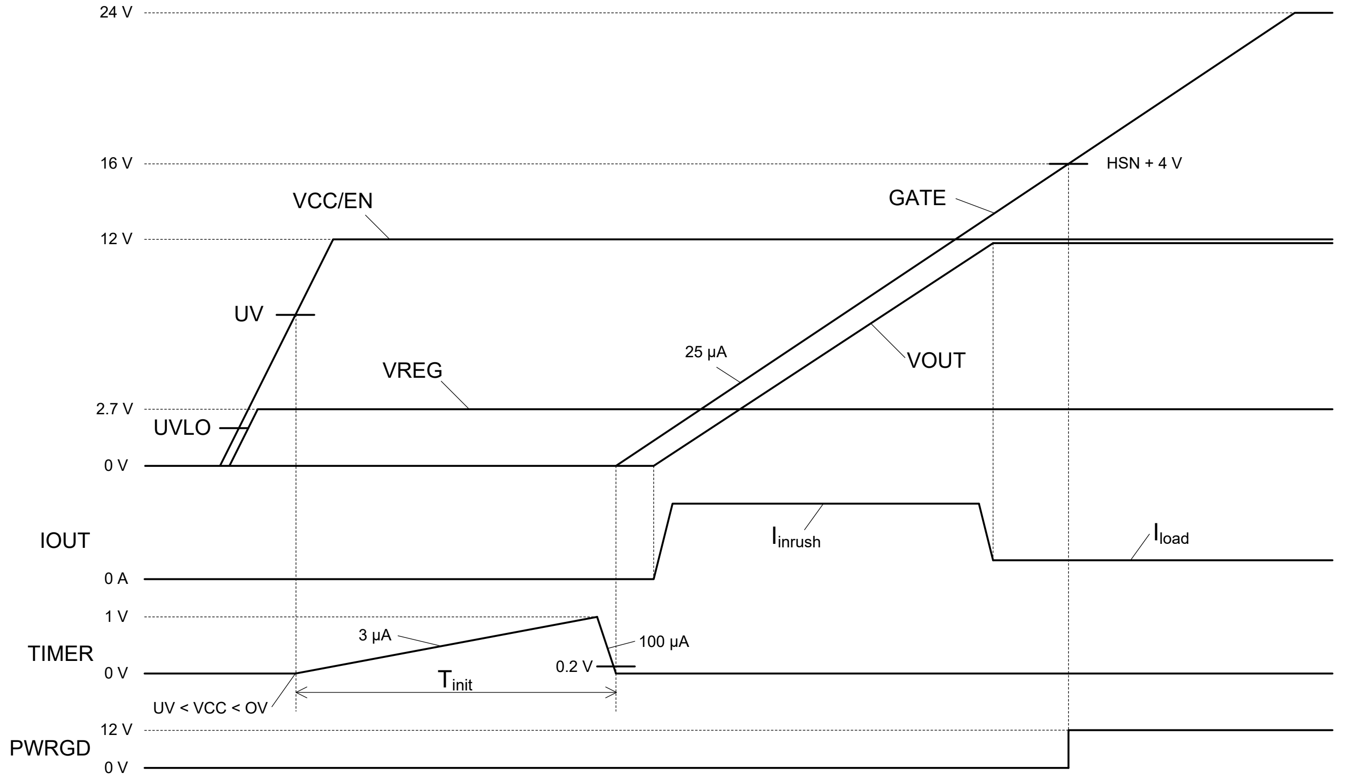


Figure 40. Power On Timing Chart

Power Good

The BD12780AMUV-LB has a comparator to detect VOUT voltage level and the comparator compares the PWGIN voltage with the internal 1 V reference voltage. The PWRGD pin is the indicator for the device ready, and it outputs PWRGD high once the following status are met.

- PWGIN > 1 V
- EN = High
- UV > 1 V
- OV < 1 V
- NFLT = High
- GATE > HSN + 4 V

In case that the GATE voltage drops below HSN + 4 V level from the PWRGD high state, the PWRGD pin is asserted low after 100 ms delay.

A/D Converter and Signal Monitor
Integrated 12-bit ADC can convert the following 4 analog signals into 12-bit digital code.

- Input Voltage V_{IN}
- Output Current I_{OUT}
- Output Voltage V_{OUT}
- Remote Temperature

HSP pin voltage and VOUT pin voltage are monitored as V_{IN} and V_{OUT} respectively. The monitor voltage is converted into 12-bit code using the following equation, and the results can be read with the 0x88 READ_VIN and 0x8B READ_VOUT commands, respectively.

READ_VIN [11:0] = 195.99 x V_{IN}
READ_VOUT [11:0] = 195.99 x V_{OUT}

where V_{IN} is HSP pin voltage [V] and V_{OUT} is VOUT pin voltage [V].

The difference voltage between MOP and MON is amplified by 39x gain with the internal current sense amplifier, and the output voltage of the amplifier is converted by ADC into 12-bit code as I_{OUT}. The code is calculated by the following equation and can be read with the 0x8C READ_IOUT command.

READ_IOUT [11:0] = 80 x R_{SENSE} x I_{OUT} + 2047.5

where R_{SENSE} is external current sense resistor [mΩ], and I_{OUT} is output current [A].

12-bit ADC converts the external NPN or PNP collector voltage connected to the TEMP pin into temperature data as the remote temperature. Multiple AD conversions are required to calculate the temperature data, and it takes 4 ms to obtain one temperature data. The remote temperature is converted into 12-bit code by the following equation and can be read by 0x8D READ_TEMPERATURE_1 command.

READ_TEMPERATURE_1 [11:0] = 4.2 x T + 3188

where T is remote temperature [°C].

In addition to the above, the BD12780AMUV-LB can provide input power data by calculating from V_{IN} and V_{OUT} data. The P_{IN} is represented by the following equation and can be read with the 0x97 READ_PIN command. The P_{IN} is 24-bit data, the upper 16-bit can be read with the READ_PIN command, and the READ_PIN_EXT command of 0xDB can be used to obtain all 24-bit data.

READ_PIN [15:0] = 61.23 x R_{SENSE} x P_{IN}

where P_{IN} is input power [W].

The calculated P_{IN} data is accumulated in the energy accumulator register as 24-bit ENERGY_EXT data, of which the upper 16-bit is output as ENERGY_COUNT. Each time the ENERGY_EXT digit overflows, rollover counter is incremented, of which the lower 8-bit is output as rollover counter. SAMPLE_COUNT is the data representing the number of times the P_{IN} has been accumulated. 0x86 READ_EIN command allows to read SAMPLE_COUNT, ROLLOVER_COUNT, ENERGY_COUNT, 0xDC READ_EIN_EXT command is required to access the full version data that is not truncated.
The A/D conversion sequence has 2 modes – Continuous Mode and Single Shot Mode. It can be selected at the PMON_MODE bit at 0xD4 PMON_CONFIG. In Single Shot mode, Single Conversion can be done by writing the CONVERT bit in 0xD3 PMON_CONTROL or applying the NALT1 pin logic from 0 to 1.
V_{IN}, V_{OUT}, and Temperature each have an enable bit in 0xD4 PMON_CONFIG, and it can be selected enable/disable. ADC results can be averaged up to 128 averages, and it can be selected with PWR_AVG and VI_AVG registers in 0xD4 PMON_CONFIG.
The ADC controller stores the peak values of I_{OUT}, V_{IN}, V_{OUT}, Temperature and P_{IN}. These data can be read by commands 0xD0 PEAK_IOUT, 0xD1 PEAK_VIN, 0xD2 PEAK_VOUT, 0xD7 PEAK_TEMPERATURE, 0xDA PEAK_PIN respectively.

Fault and Warning

Fault items and their actions are shown below.

Table 1. Fault Table

Fault Name	Pin	Control/Setting Bit	Status Bit	NFLT	PWRGD	NALTx	GATE	Comment
Disable	EN	ON	N/A	No Action	**Low**	No Action	**Slow Discharge (10 mA)**	
VIN Under Voltage	UV	VIN_UV_FAULT_ENx*	VIN_UV_FAULT (latched) UV_CMP_OUT	No Action	**Low**	**Low*** **	**Slow Discharge (10 mA)**	
VIN Over Voltage	OV	VIN_OV_FAULT_ENx*	VIN_OV_FAULT (latched) OV_CMP_OUT	No Action	**Low**	**Low*** **	**Slow Discharge (10 mA)**	
Over Current	HSP, HSN	IOUT_OC_FAULT_ENx*	IOUT_OC_FAULT (latched)	**Low**	**Low**	**Low*** **	**Regulation until Timer is expired Slow Discharge (10 mA) after Timer is expired**	NRTY pin to select Autoretry or Latch-off. NRTY=L: Autoretry after 10 sec NRTY=H or Open: Latch-off
Circuit Breaker	HSP, HSN	HS_INLIM_ENx*	HS_INLIM_FAULT (latched)	No Action	No Action	**Low*** **	No Action	
Severe Over Current	HSP, HSN	OC_TRIP_SELECT[1:0] OC_FILT_SELECT OC_RETRY_DIS	SEVERE_OC_FAULT (latched)	No Action	**Low**	No Action	**Fast Discharge (1500 mA)**	
Over Temperature Fault	TEMP (ADC)	OT_FAULT_LIMIT[11:0] OT_FAULT_ENx*	OT_FAULT (latched)	**Low**	**Low**	**Low*** **	**Slow Discharge (10 mA)**	
FET Health Fault	GATE	FHDIS FET_HEALTH_FAULT_ENx*	FET_HEALH_FAULT (latched)	**Low**	**Low after 100 ms**	**Low*** **	**Slow Discharge (10 mA)**	GATE - HSN < 4 V detection during the operation. V_{DS} short detection at start-up.
VOUT Under Voltage	PWGIN	N/A	PGB_STATUS	No Action	**Low**	No Action	No Action	
VOUT Over Voltage Warning	PWGIN (ADC)	VOUT_OV_WARN_LIMIT[11:0] VOUT_OV_WARN_ENx*	VOUT_OV_WARN (latched)	No Action	No Action	**Low** **	No Action	
VOUT Under Voltage Warning	PWGIN (ADC)	VOUT_UV_WARN_LIMIT[11:0] VOUT_UV_WARN_ENx*	VOUT_UV_WARN (latched)	No Action	No Action	**Low** **	No Action	
Power Warning	N/A (ADC)	PIN_OP_WARN_LIMIT[14:0] PIN_OP_WARN_ENx*	PIN_OP_WARN (latched)	No Action	No Action	**Low** **	No Action	
I2C Error	SCL, SDA	CML_ERROR_ENx*	CML_FAULT (latched)	No Action	No Action	**Low*** **	No Action	
VIN Under Voltage Warning	HSP (ADC)	VIN_UV_WARN_LIMIT[11:0] VIN_UV_WARN_ENx*	VIN_UV_WARN (latched)	No Action	No Action	**Low** **	No Action	
VIN Over Voltage Warning	HSP (ADC)	VIN_OV_WARN_LIMIT[11:0] VIN_OV_WARN_ENx*	VIN_OV_WARN (latched)	No Action	No Action	**Low** **	No Action	
Over Current Warning	MOP, MON (ADC)	IOUT_OC_WARN_LIMIT[11:0] IOUT_OC_WARN_ENx*	IOUT_OC_WARN (latched)	No Action	No Action	**Low** **	No Action	
Over Temperature Warning	TEMP (ADC)	OT_WARN_LIMIT[11:0] OT_WARN_ENx*	OT_WARNING (latched)	No Action	No Action	**Low** **	No Action	
Hysteretic Warning (IOUT)	MOP, MON (ADC)	PWR_HYST_EN HYSTERETIC_ENx* HYSTERESIS_HIGH[15:0] HYSTERESIS_LOW[15:0]	HYST_STATE HYST_GT_HIGH HYST_LT_LOW	No Action	No Action	**Low*** **	No Action	PWR_HYST_EN = 0
Hysteretic Warning (Power)	N/A (ADC)							PWR_HYST_EN = 1

* SMB Alert enable bit

** Need to set SMB Alert enable bit, otherwise "No Action". The Alert is latched in SMB Alert mode. The Alert is live signal in Digital Comparator mode.

*** Need to set SMB Alert enable bit, otherwise "No Action". The Alert is latched in SMB Alert mode. There is no Digital Comparator mode.

Enable / Disable

The BD12780AMUV-LB ON/OFF can be controlled by the EN pin or the ON bit at Address 0x01/bit7. When EN pin is input low, the BD12780AMUV-LB is OFF, PWRGD pin is low, and GATE pin is discharged by 10 mA.

V_{IN} Undervoltage and Overvoltage Detection

A comparator for undervoltage detection is built in and compares the UV pin voltage with the internal 1 V reference voltage. When the undervoltage is detected, the PWRGD pin is pulled low, and GATE pin is discharged by 10 mA. A detection comparator for overvoltage is also built in and compares the OV pin voltage with the internal 1 V reference voltage. When the overvoltage is detected, the same actions as UV fault are taken.
V_{IN} can also be monitored through an ADC and the thresholds can be set for OV and UV warnings with the VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT bits respectively. If this threshold is exceeded, VIN_OV_WARN and VIN_UV_WARN are set and latched.
When V_{IN} Undervoltage is detected prior to Severe Overcurrent Detection (Severe OC), Severe OC event will be masked.
To ensure proper detection of Severe OC in conditions such as the output short, an external capacitor of 40 nF (the effective capacitance) or more should be added between UV pin and GND as a filter.
Please use a capacitor 40 nF or more if resistor between VIN-GND (for UV setting) is around 100 kΩ.
In the case of changing resistance value, please confirm there are no problems with application usage considering the timing of Severe OC and UV.

Overcurrent Limit (CL) and Circuit Breaker (CB) Detection

The BD12780AMUV-LB has 3 types of current limit settings – ISET, PSET and ISTART. ISET is the current limit during normal operation, and the current limit is set according to the voltage at the ISET pin.

$$\text{ISET Limit} = (V_{HSP} - V_{HSN}) \times 50 / R_{SENSE}$$

If the ISET pin is set above 1.5 V, the internal 1 V reference voltage is selected as the setting voltage and the current limit is the default setting.
The setting in ISTART is valid at startup until PWRGD goes high. The same functionality can be set with the register STRT_UP_IOUT_LIM [3:0]. The respective equations are

$$\text{ISTART Limit} = (V_{HSP} - V_{HSN}) \times 50 / R_{SENSE}$$
$$\text{ISTART Limit} = V_{ISET} \times (\text{STRT\_UP\_IOUT\_LIM} + 1) / 16 / R_{SENSE}$$

The PSET setting works for limiting the external FET power and it is represented by the following equation.

$$\text{PSET Limit} = (V_{PSET} \times 8) / (50 \times R_{SENSE}).$$

The lowest one of these three current limit settings takes precedence.

Here is the description how the current limit operates with the circuit braker function. When the load becomes high and reaches the CB level, TIMER starts charging with 60 µA, and HS_INLIM_FAULT is set. When the load reaches the CL level, Driver starts GATE regulation. This regulation state continues until the load level drops below CB again. When TIMER voltage reaches 1 V, GATE is shut down and TIMER starts discharging 2 µA. The external FET can be turned ON again when the TIMER voltage drops below 0.2 V. Both NFLT and PWRGD pins go low when the overcurrent shutdown occurs. Auto retry or latch off after OC event can be selected by NRTY pin. NRTY has an internal pull-up and latch off is selected when NRTY is floated. When NRTY is set to low, waits 10 s after OC shutdown and starts auto retrying.

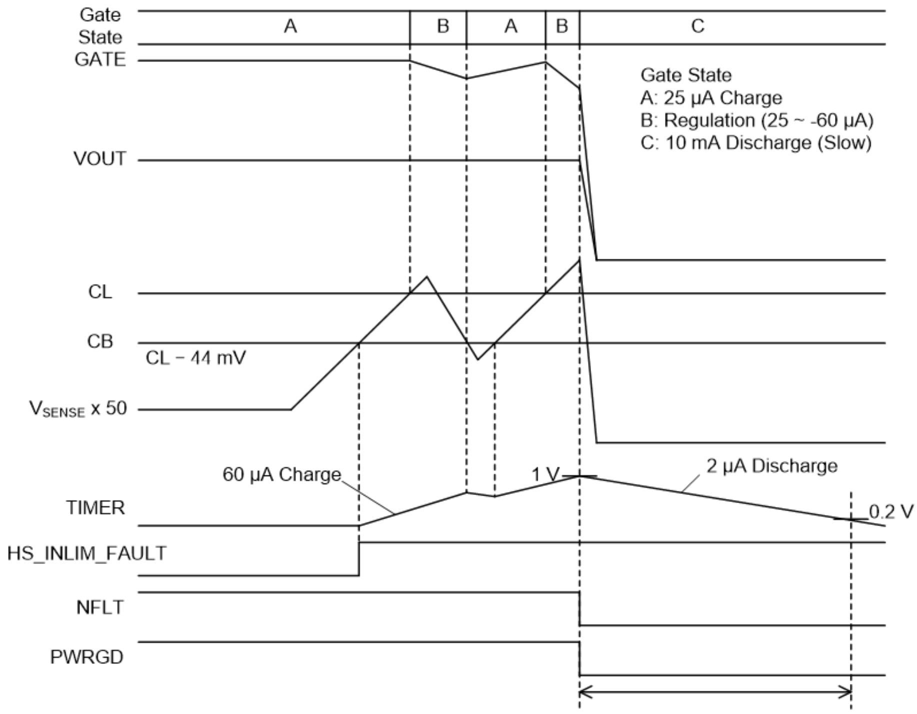


Figure 41. Current Limit Timing Chart

Severe Overcurrent Detection

Severe overcurrent threshold can be set in case of severe errors in system such as load short circuits. It can be selected from 125 % / 150 % / 200 % / 225 % of OC and can be set by OC_TRIP_SELECT [1:0] bits. GATE is strongly discharged immediately once Severe OC is detected. Auto retry is enabled by default and can be disabled by setting OC_RETRY_DIS bit. The filter of Severe OC can be selected from 2 values, and the default is 900 ns. 220 ns fast response can be selected by setting OC_FILT_SELECT to 0.

Over Temperature Detection

Temperature can be monitored using an external NPN or PNP. The monitored temperature can be read out through PMBus, and the Warning and Fault thresholds can be set at the registers in 0x4F and 0x51 respectively. If the fault threshold is exceeded, the status bit OT_FAULT is set, the controller sets NFLT low and discharges the GATE at 10 mA. In case of warning, the status bit OT_WARNING is set. These status bits are latched bits, and live information can be checked with TEMP_FAULT bit.

FET Health

External FETs are monitored for faults. Short-circuit faults between the Gate, Source, and Drain terminals of the FET can be detected. If FET Health fault is detected, the controller sets FET_HEALTH_FAULT status bit, NFLT low, and discharges the GATE at 10 mA.

V_{OUT} Fault and Warning Detection

VOUT is connected to the PWGIN pin through an external resistance voltage divider, and the PWGIN comparator detects undervoltage by comparing the internal 1 V reference voltage and the PWGIN voltage. When the undervoltage is detected, the PWRGD pin is asserted low, and the PGB_STATUS bit indicates whether the V_{OUT} is good or bad state.
V_{OUT} can be monitored through ADC, and the warning threshold for OV and UV can be set with VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT respectively. If the thresholds are exceeded, VOUT_OV_WARN and VOUT_UV_WARN status bits are set and latched.

Power Warning Detection

Power is calculated by multiplying the results of monitoring V_{IN} and I_{OUT} in ADC. The warning threshold of the power can be set with PIN_OP_WARN_LIMIT. If this threshold is exceeded, PIN_OP_WARN status bit is set and latched.

Hysteretic Warning Detection

The threshold of hysteresis detection can be set with HYSTERESIS_HIGH and HYSTERESIS_LOW. ADC code of I_{OUT} and P_{IN} can be compared to the thresholds, and either I_{OUT} or P_{IN} can be selected with PWR_HYST_EN bit.

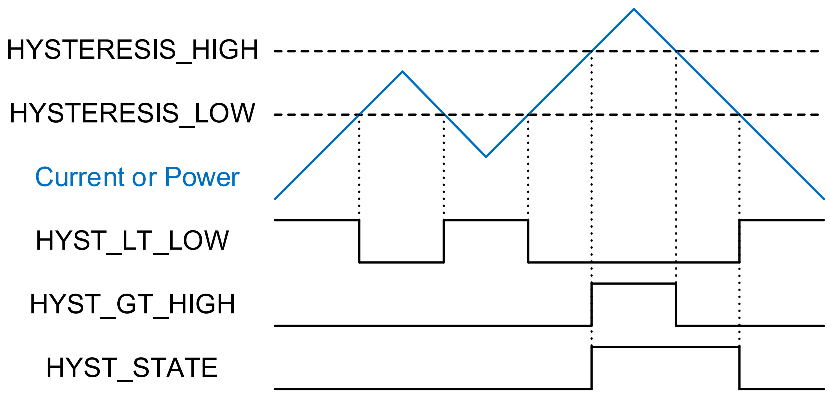


Figure 42. Hysteresis Function

I²C Error

When Packet Error Check (PEC) is used, the BD12780AMUV-LB compares the written data with the PEC data. The command is ignored and the CML_FAULT status bit is set if the data is incorrect.

Alert

The following three modes can be selected with the GPOx_MODE bit of the 0xD8 DEVICE_CONFIG command.

- SMBAlert
- GPO
- Digital Comparator

SMBAlert
The BD12780AMUV-LB can tell the alert directly from NALT1 or NALT2 pin to the host. These pins are open-drain outputs and are HiZ (OFF) at power-on. The alert signal can be selected and programmed at address 0xD5 ALERT1_CONFIG and 0xD6 ALERT2_CONFIG, and any fault or warning events enabled at ALERTx_CONFIG register assert NALT1 or NALT2 low. After the alert, issuing the CLEAR_FAULTS command clears the status bits and releases the NALT1 and NALT2 pins. At that time, if any faults or warnings continue to occur, the status bits are set again, and the NALT1 and NALT2 pins are not reasserted low. Only when any faults or warnings newly occurs, then the NALT1 and NALT2 pins are asserted low. However, in case Power Monitor (ADC) warning, the NALT1 and NALT2 pins are reasserted low if it is in warning state at the timing of the next ADC result update.

Alert Respond Address (ARA)
The host issues 0x0C command, and the devices with active SMBAlert return the device address. When SMBAlert occurs on multiple devices, the device with the lower device address number gets the right to communicate. The device that successfully responds to the device address releases the NALT1 and NALT2 pins at the timing of no acknowledge bit, however, it does not clear the status bit.

GPO
GPOx_INVERT bit is directly output from NALTx pin.

Digital Comparator
SMBAlert is latched signal, however, this is live signal.

Current Sense Output
The voltage across Rs, that is, the difference between HSP and HSN, is amplified by 350x and output from the CSO pin with a response time of 10 µs. By using this CSO, the system can detect overpower besides the protection functions in BD12780AMUV-LB.

Power Cycle Command
By sending the Power Cycle Command assigned to 0xD9, the BD12780AMUV-LB can be turned off once and turned on again. This power cycle interval can be selected from four values of 5/10/20/30/60/120/180/240 s using the PCYC_INTVL [2:0] bits provided in 0xDD. The default is 5 s.

PMBus Interface
It can communicate in I2C format through the SCL and SDA pins. The following table is the timing requirements for the interface.

DEVICE ADDRESSING
7-bit device address can be set by ADR1 and ADR2 pins. ADR2 and ADR1 are 4-value logic, and total of 16 values can be set according to the table below.

Table 2. Device Address Setting Table

ADR2	ADR1	Device Address
L	L	0x10
L	PD	0x11
L	HiZ	0x12
L	H	0x13
PD	L	0x40
PD	PD	0x41
PD	HiZ	0x42
PD	H	0x43
HiZ	L	0x44
HiZ	PD	0x45
HiZ	HiZ	0x46
HiZ	H	0x47
H	L	0x50
H	PD	0x51
H	HiZ	0x52
H	H	0x53

L: Connect to GND
H: Connect to VREG
HiZ: No connection
PD: Pull-down to GND by 150 kΩ resistor

Packet Error Check
Packet Error Check (PEC) can be used as an option in BD12780AMUV-LB communication. PEC can be sent from the controller side or the target side, and the BD12780AMUV-LB compares the written data with the PEC data, ignores the command if it is determined to be incorrect, and sets the CML_FAULT status bit.

Communication Format
Communication format has the following 4 types.

- Send Command
- Read / Write Byte
- Read / Write Word
- Block Read

The group command can be used to access multiple devices at once.

S: Start condition
Sr: Repeated start condition
P: Stop condition
R: Read bit
Wb: Write bit
A: Acknowledge bit (0)
Ab: Acknowledge bit (1)

Controller to Target

Target to Controller

S	Device Address	Wb	A	Data Byte	A	P		
S	Device Address	Wb	A	Data Byte	A	PEC	A	P

Figure 43. Send Byte and Send Byte with PEC

S	Device Address	Wb	A	Command Code	A	Data Byte	A	P		
S	Device Address	Wb	A	Command Code	A	Data Byte	A	PEC	A	P

Figure 44. Write Byte and Write Byte with PEC

S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Data Byte	Ab	P		
S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Data Byte	A	PEC	Ab	P

Figure 45. Read Byte and Read Byte with PEC

S	Device Address	Wb	A	Command Code	A	Low Data Byte	A	High Data Byte	A	P		
S	Device Address	Wb	A	Command Code	A	Low Data Byte	A	High Data Byte	A	PEC	A	P

Figure 46. Write Word and Write Word with PEC

S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Low Data Byte	A	…
High Data Byte	Ab	P										

S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Low Data Byte	A	…
High Data Byte	A	PEC	Ab	P								

Figure 47. Read Word and Read Word with PEC

S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Byte Count = N	A	…
Data Byte 1	A	Data Byte 2	A	…	Data Byte N	Ab	P					

S	Device Address	Wb	A	Command Code	A	Sr	Device Address	R	A	Byte Count = N	A	…
Data Byte 1	A	Data Byte 2	A	…	Data Byte N	A	PEC	Ab	P			

Figure 48. Block Read and Block Read with PEC

Register Maps

Table 3. PMBus Command Table

Command Code	Command Name	Access	Number of Data Bytes	Default Value
0x01	OPERATION	Read/Write Byte	1	0x80
0x03	CLEAR_FAULTS	Send Byte	0	Not applicable
0x19	CAPABILITY	Read Byte	1	0xB0
0x42	VOUT_OV_WARN_LIMIT	Read/Write Word	2	0x0FFF
0x43	VOUT_UV_WARN_LIMIT	Read/Write Word	2	0x0000
0x4A	IOUT_OC_WARN_LIMIT	Read/Write Word	2	0x0FFF
0x4F	OT_FAULT_LIMIT	Read/Write Word	2	0x0FFF
0x51	OT_WARN_LIMIT	Read/Write Word	2	0x0FFF
0x57	VIN_OV_WARN_LIMIT	Read/Write Word	2	0x0FFF
0x58	VIN_UV_WARN_LIMIT	Read/Write Word	2	0x0000
0x6B	PIN_OP_WARN_LIMIT	Read/Write Word	2	0x0FFF
0x78	STATUS_BYTE	Read Byte	1	0x00
0x79	STATUS_WORD	Read Word	2	0x0000
0x7A	STATUS_VOUT	Read Byte	1	0x00
0x7B	STATUS_IOUT	Read Byte	1	0x00
0x7C	STATUS_INPUT	Read Byte	1	0x00
0x7D	STATUS_TEMPERATURE	Read Byte	1	0x00
0x80	STATUS_MFR_SPECIFIC	Read Byte	1	0x00
0x86	READ_EIN	Block Read	6	0x000000000000
0x88	READ_VIN	Read Word	2	0x0000
0x8B	READ_VOUT	Read Word	2	0x0000
0x8C	READ_IOUT	Read Word	2	0x0000
0x8D	READ_TEMPERATURE_1	Read Word	2	0x0000
0x97	READ_PIN	Read Word	2	0x0000
0x98	PMBUS_REVISION	Read Byte	1	0x33
0x99	MFR_ID	Block Read	4	ROHM (ASCII Code)
0x9A	MFR_MODEL	Block Read	7	BD12780 (ASCII Code)
0x9B	MFR_REVISION	Block Read	2	0x3033
0xD0	PEAK_IOUT	Read/Write Word	2	0x0000
0xD1	PEAK_VIN	Read/Write Word	2	0x0000
0xD2	PEAK_VOUT	Read/Write Word	2	0x0000
0xD3	PMON_CONTROL	Read/Write Byte	1	0x01
0xD4	PMON_CONFIG	Read/Write Word	2	0x0714
0xD5	ALERT1_CONFIG	Read/Write Word	2	0x0000
0xD6	ALERT2_CONFIG	Read/Write Word	2	0x0000
0xD7	PEAK_TEMPERATURE	Read/Write Word	2	0x0000
0xD8	DEVICE_CONFIG	Read/Write Word	2	0x000D
0xD9	POWER_CYCLE	Send Byte	0	Not applicable
0xDA	PEAK_PIN	Read/Write Word	2	0x0000
0xDB	READ_PIN_EXT	Block Read	3	0x000000
0xDC	READ_EIN_EXT	Block Read	8	0x0000000000000000
0xDD	POWER_CYCLE_INTERVAL	Read/Write Byte	1	0x00
0xF2	HYSTERESIS_LOW	Read/Write Word	2	0x0000
0xF3	HYSTERESIS_HIGH	Read/Write Word	2	0xFFFF
0xF4	STATUS_HYSTERESIS	Read Byte	1	0x00
0xF6	STRT_UP_IOUT_LIM	Read/Write Word	2	0x000F

Register Definitions

OPERATION REGISTER (0x01)

The OPERATION command controls the hot swap enable and disable. This command is used to re-enable the hot swap after shutdown by fault event. Writing the enable command after the disabled command clears all fault and warning status which are not active.

Table 4. Bit Descriptions for OPERATION

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	ON	 0 1	Hot swap enable. Hot swap output disabled. Hot swap output enabled.	0x1	RW
[6:0]	RESERVED		Always reads as 0000000.	0x00	RESERVED

CLEAR_FAULTS REGISTER (0x03)

The CLEAR_FAULTS command resets all fault and warning status which are not active. This address doesn't have any registers to store data.

CAPABILITY REGISTER (0x19)

The CAPABILITY command requests the device to return the PMBus information supported by BD12780AMUV-LB.

Table 5. Bit Descriptions for CAPABILITY

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	PEC_SUPPORT	 1	Packet error check (PEC) support. Always reads as 1. PEC is supported.	0x1	R
[6:5]	MAX_BUS_SPEED	 10	Maximum bus interface speed. Always reads as 10. Maximum supported bus speed is 1 MHz.	0x2	R
4	SMBALERT_SUPPORT	 1	SMBAlert support. Always reads as 1. Device supports SMBAlert and ARA.	0x1	R
[3:0]	RESERVED		Always reads as 0000.	0x0	RESERVED

VOUT_OV_WARN_LIMIT REGISTER (0x42)

The VOUT_OV_WARN_LIMIT command sets the overvoltage warning threshold for V_{OUT} measured by ADC. The limit data is readable.

Table 6. Bit Descriptions for VOUT_OV_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_OV_WARN_LIMIT		Overvoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0xFFF	RW

VOUT_UV_WARN_LIMIT REGISTER (0x43)

The VOUT_UV_WARN_LIMIT command sets the undervoltage warning threshold for V_{OUT} measured by ADC. The limit data is readable.

Table 7. Bit Descriptions for VOUT_UV_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_UV_WARN_LIMIT		Undervoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0x000	RW

IOUT_OC_WARN_LIMIT REGISTER (0x4A)

The IOUT_OC_WARN_LIMIT command sets the overcurrent warning threshold for I_{OUT} measured between MOP and MON by ADC. The limit data is readable.

Table 8. Bit Descriptions for IOUT_OC_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	IOUT_OC_WARN_LIMIT		Overcurrent warning threshold for the I_{OUT} measurement, expressed in direct format.	0xFFF	RW

OT_FAULT_LIMIT REGISTER (0x4F)

The OT_FAULT_LIMIT command sets the overtemperature fault threshold for remote diode temperature measured on TEMP by ADC. The limit data is readable.

Table 9. Bit Descriptions for OT_FAULT_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_FAULT_LIMIT		Overtemperature fault threshold for the TEMP pin measurement, expressed in direct format.	0xFFF	RW

OT_WARN_LIMIT REGISTER (0x51)
The OT_WARN_LIMIT command sets the overtemperature warning threshold for remote diode temperature measured on TEMP by ADC. The limit data is readable.

Table 10. Bit Descriptions for OT_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_WARN_LIMIT		Overtemperature warning threshold for the TEMP pin measurement, expressed in direct format.	0xFFF	RW

VIN_OV_WARN_LIMIT REGISTER (0x57)
The VIN_OV_WARN_LIMIT command sets the overvoltage warning threshold for V_{IN} measured on HSP by ADC. The limit data is readable.

Table 11. Bit Descriptions for VIN_OV_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_OV_WARN_LIMIT		Overvoltage warning threshold for the HSP pin measurement, expressed in direct format.	0xFFF	RW

VIN_UV_WARN_LIMIT REGISTER (0x58)
The VIN_UV_WARN_LIMIT command sets the undervoltage warning threshold for V_{IN} measured on HSP by ADC. The limit data is readable.

Table 12. Bit Descriptions for VIN_UV_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_UV_WARN_LIMIT		Undervoltage warning threshold for the HSP pin measurement, expressed in direct format.	0x000	RW

PIN_OP_WARN_LIMIT REGISTER (0x6B)
The PIN_OP_WARN_LIMIT command sets the overpower warning threshold for the power calculated V_{IN} x I_{OUT} measured by ADC. The limit data is readable.

Table 13. Bit Descriptions for PIN_OP_WARN_LIMIT

Bits	Bit Name	Data	Descriptions	Defaut	Access
15	RESERVED		Always reads as 0.	0x0	RESERVED
[14:0]	PIN_OP_WARN_LIMIT		Overpower warning threshold for the V_{IN} x I_{OUT} power calculation, expressed in direct format.	0x7FFF	RW

STATUS_BYTE REGISTER (0x78)
The STATUS_BYTE command requests the device to return the status flags.

Table 14. Bit Descriptions for STATUS_BYTE

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	HOTSWAP_OFF	 0 1	Hot swap gate is off. This bit is live. The hot swap gate drive output is enabled. The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, an undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off.	0x0	R
5	RESERVED		Always reads as 0.	0x0	RESERVED
4	IOUT_OC_FAULT	 0 1	I_{OUT} overcurrent fault. This bit is latched. No overcurrent output fault detected. The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down.	0x0	R
3	VIN_UV_FAULT	 0 1	V_{IN} fault. This bit is latched. No undervoltage input fault detected on the UV pin. An undervoltage input fault was detected on the UV pin.	0x0	R
2	TEMP_FAULT	 0 1	Temperature fault or warning. This bit is live. There are no active status bits to be read by STATUS_TEMPERATURE. There are one or more active status bits to be read by STATUS_TEMPERATURE.	0x0	R
1	CML_FAULT	 0 1	CML fault. This bit is latched. No communications error detected on the I^2C/PMBus interface. An error was detected on the I^2C/PMBus interface. Errors detected include an unsupported command, invalid PEC byte, and incorrectly structured message.	0x0	R
0	NONEABOVE_STATUS	 0 1	None of the above. This bit is live. No other active status bit reported by any other status command. Active status bits are waiting to be read by one or more status commands.	0x0	R

STATUS_WORD REGISTER (0x79)
The STATUS_WORD command requests the device to return the status flags.

Table 15. Bit Descriptions for STATUS_WORD

Bits	Bit Name	Data	Descriptions	Defaut	Access
15	VOUT_STATUS	 0 1	V_{OUT} warning. This bit is live. There are no active status bits to be read by the STATUS_VOUT register. There are one or more active status bits to be read by STATUS_VOUT.	0x0	R
14	IOUT_STATUS	 0 1	I_{OUT} fault or warning. This bit is live. There are no active status bits to be read by the STATUS_IOUT register. There are one or more active status bits to be read by the STATUS_IOUT register.	0x0	R
13	INPUT_STATUS	 0 1	Input warning. This bit is live. There are no active status bits to be read by the STATUS_INPUT register. There are one or more active status bits to be read by STATUS_INPUT.	0x0	R
12	MFR_STATUS	 0 1	Manufacture specific fault or warning. This bit is live. There are no active status bits to be read by the STATUS_MFR_SPECIFIC register. There are one or more active status bits to be read by STATUS_MFR_SPECIFIC register.	0x0	R
11	PGB_STATUS	 0 1	Power is not good. This bit is live. Output power is good. The voltage on the PWGIN pin is above the threshold. Output power is bad. The voltage on the PWGIN pin is below the threshold.	0x0	R
[10:9]	RESERVED		Always set to 0.	0x0	RESERVED
8	FET_HEALTH_FAULT	 0 1	FET health fault. This bit is latched. No FET faults have been detected. A fault condition has been detected on the FET.	0x0	R
7	RESERVED		Always set to 0.	0x0	RESERVED
6	HOTSWAP_OFF		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
5	RESERVED		Always set to 0.	0x0	RESERVED
4	IOUT_OC_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
3	VIN_UV_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
2	TEMP_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
1	CML_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
0	NONEABOVE_STATUS		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R

STATUS_VOUT REGISTER (0x7A)
The STATUS_VOUT command requests the device to return the status flags related to V_{OUT} warnings.

Table 16. Bit Descriptions for STATUS_VOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	VOUT_OV_WARN	 0 1	V_{OUT} Overvoltage Warning. No overvoltage condition on the output supply detected by the power monitor. An overvoltage condition on the output supply was detected by the power monitor. This bit is latched.	0x0	R
5	VOUT_UV_WARN	 0 1	V_{OUT} Undervoltage warning. No undervoltage condition on the output supply detected by the power monitor. An undervoltage condition on the output supply was detected by the power monitor. This bit is latched.	0x0	R
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

STATUS_IOUT REGISTER (0x7B)
The STATUS_IOUT command requests the device to return the status flags related to IOUT faults and warnings.

Table 17. Bit Descriptions for STATUS_IOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	IOUT_OC_FAULT	 0 1	I_{OUT} overcurrent fault. No overcurrent output fault detected. The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. This bit is latched.	0x0	R
6	RESERVED		Always reads as 0.	0x0	RESERVED
5	IOUT_OC_WARN	 0 1	I_{OUT} overcurrent warning. No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command. An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command. This bit is latched.	0x0	R
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

STATUS_INPUT REGISTER (0x7C)

The STATUS_INPUT command requests the device to return the status flags related to V_{IN} and P_{IN} faults and warnings.

Table 18. Bit Descriptions for STATUS_INPUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	VIN_OV_FAULT	 0 1	V_{IN} overvoltage fault. No overvoltage detected on the OV pin. An overvoltage was detected on the OV pin. This bit is latched.	0x0	R
6	VIN_OV_WARN	 0 1	V_{IN} overvoltage warning fault. No overvoltage condition on the input supply detected by the power monitor. An overvoltage condition on the input supply was detected by the power monitor. This bit is latched.	0x0	R
5	VIN_UV_WARN	 0 1	V_{IN} undervoltage warning. No undervoltage condition on the input supply detected by the power monitor. An undervoltage condition on the input supply was detected by the power monitor. This bit is latched.	0x0	R
4	VIN_UV_FAULT	 0 1	V_{IN} undervoltage fault. No undervoltage detected on the UV pin. An undervoltage was detected on the UV pin. This bit is latched.	0x0	R
[3:1]	RESERVED		Always reads as 000.	0x0	RESERVED
0	PIN_OP_WARN	 0 1	P_{IN} overpower warning. No overpower condition on the input supply detected by the power monitor. An overpower condition on the input supply was detected by the power monitor. This bit is latched.	0x0	R

STATUS_TEMPERATURE REGISTER (0x7D)

The STATUS_TEMPERATURE command requests the device to return the status flags related to temperature faults and warnings.

Table 19. Bit Descriptions for STATUS_TEMPERATURE

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	OT_FAULT	 0 1	Overtemperature fault. No overtemperature fault detected by the ADC. An overtemperature fault was detected by the ADC. This bit is latched.	0x0	R
6	OT_WARNING	 0 1	Overtemperature warning. No overtemperature warning detected by the ADC. An overtemperature warning was detected by the ADC. This bit is latched.	0x0	R
[5:0]	RESERVED		Always reads as 000000.	0x0	RESERVED

STATUS_MFR_SPECIFIC REGISTER (0x80)

The STATUS_MFR_SPECIFIC command requests the device to return the status flags related to manufacturer specific faults and warnings.

Table 20. Bit Descriptions for STATUS_MFR_SPECIFIC

Bits	Bit Name	Data	Descriptions	Defaut	Access
7	FET_HEALTH_FAULT	 0 1	FET health fault. No FET health problems have been detected. An FET health fault has been detected. This bit is latched.	0x0	R
6	UV_CMP_OUT	 0 1	UV input comparator fault output. Input voltage to UV pin is above threshold. Input voltage to UV pin is below threshold. This bit is live.	0x0	R
5	OV_CMP_OUT	 0 1	OV input comparator fault output. Input voltage to OV pin is below threshold. Input voltage to OV pin is above threshold. This bit is live.	0x0	R
4	SEVERE_OC_FAULT	 0 1	Severe overcurrent fault. A severe overcurrent has not been detected by the hot swap. A severe overcurrent has been detected by the hot swap. This bit is latched.	0x0	R
3	HS_INLIM_FAULT	 0 1	Hot swap in limit fault. The hot swap has not actively limited the current into the load. The hot swap has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM_FAULT bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the time limit set by the capacitor on the TIMER pin elapses. This bit is latched.	0x0	R
[2:0]	HS_SHUTDOWN_CAUSE	 000 001 010 011 100 110	Cause of last hot swap shutdown. This bit is latched until the status registers are cleared. The hot swap is either enabled and working correctly, or has been shut down using the OPERATION command. An OT_FAULT condition occurred that caused the hot swap to shut down. An IOUT_OC_FAULT condition occurred that caused the hot swap to shut down. An FET_HEALTH_FAULT condition occurred that caused the hot swap to shut down. A VIN_UV_FAULT condition occurred that caused the hot swap to shut down. A VIN_OV_FAULT condition occurred that caused the hot swap to shut down.	0x0	R

READ_EIN REGISTER (0x86)
The READ_EIN command requests the device to return the accumulated energy values and data.

Table 21. Bit Descriptions for READ_EIN

Bits	Bit Name	Data	Descriptions	Defaut	Access
[47:24]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 5 is the high byte, Byte 4 is the middle byte, and Byte 3 is the low byte.	0x000000	R
[23:16]	ROLLOVER_COUNT		Number of times that the energy count has rolled over from 0x7FFF to 0x0000. This is an unsigned 8-bit binary value.	0x00	R
[15:0]	ENERGY_COUNT		Energy accumulator value in PMBus direct format. Byte 1 is the high byte, and Byte 0 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command. Use the READ_EIN_EXT register to access the nontruncated version.	0x0000	R

READ_VIN REGISTER (0x88)
The READ_VIN command requests the device to return the V_{IN} value.

Table 22. Bit Descriptions for READ_VIN

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VIN		Input voltage from the HSP pin measurement after averaging, expressed in direct format.	0x000	R

READ_VOUT REGISTER (0x8B)
The READ_VOUT command requests the device to return the V_{OUT} value.

Table 23. Bit Descriptions for READ_VOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VOUT		Input voltage from the VOUT pin measurement after averaging, expressed in direct format.	0x000	R

READ_IOUT REGISTER (0x8C)
The READ_IOUT command requests the device to return the I_{OUT} value.

Table 24. Bit Descriptions for READ_IOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_IOUT		Output current derived from MOP/MON sense pin voltage measurement after averaging, expressed in direct format.	0x000	R

READ_TEMPERATURE_1 REGISTER (0x8D)
The READ_TEMPERATURE_1 command requests the device to return the remote diode temperature value.

Table 25. Bit Descriptions for READ_TEMPERATURE_1

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_TEMPERATURE_1		Temperature from the TEMP pin measurement after averaging, expressed in direct format.	0x000	R

READ_PIN REGISTER (0x97)
The READ_PIN command requests the device to return the P_{IN} value.

Table 26. Bit Descriptions for READ_PIN

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:0]	READ_PIN		Input power calculation, using $V_{IN} \times I_{OUT}$, after averaging, expressed in PMBus direct format. P_{IN} values are calculated for each $V_{IN} \times I_{OUT}$ sample, all P_{IN} values are then averaged before the value is returned to the READ_PIN register.	0x0000	R

PMBUS_REVISION REGISTER (0x98)
The PMBUS_REVISION command requests the device to return the PMBus revision supported by BD12780AMUV-LB.

Table 27. Bit Descriptions for PMBUS_REVISION

Bits	Bit Name	Data	Descriptions	Defaut	Access
[7:4]	PMBUS_P1_REVISION	11	PMBus Part I Support. Revision 1.3.	0x3	R
[3:0]	PMBUS_P2_REVISION	11	PMBus Part II Support. Revision 1.3.	0x3	R

MFR_ID REGISTER (0x99)
The MFR_ID command requests the device to return the manufacturer ID.

Table 28. Bit Descriptions for MFR_ID

Bits	Bit Name	Data	Descriptions	Defaut	Access
[31:0]	MFR_ID		String identifying manufacturer as ROHM.	0x4D484F52	R

MFR_MODEL REGISTER (0x9A)
The MFR_MODEL command requests the device to return the IC part number.

Table 29. Bit Descriptions for MFR_MODEL

Bits	Bit Name	Data	Descriptions	Defaut	Access
[55:0]	MFR_MODEL		String identifying the part number of the chip - BD12780.	0x30383732314442	R

MFR_REVISION REGISTER (0x9B)
The MFR_REVISION command requests the device to return the IC part number.

Table 30. Bit Descriptions for MFR_REVISION

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:0]	MFR_REVISION		String identifying hardware revision.	0x3033	R

PEAK_IOUT REGISTER (0xD0)

The PEAK_IOUT command requests the device to report the peak I_{OUT} value. Writing 0x0000 resets the registers.

Table 31. Bit Descriptions for PEAK_IOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_IOUT		Peak output current measurement, I_{OUT}, expressed in direct format.	0x000	RW

PEAK_VIN REGISTER (0xD1)

The PEAK_VIN command requests the device to report the peak V_{IN} value. Writing 0x0000 resets the registers.

Table 32. Bit Descriptions for PEAK_VIN

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VIN		Peak input voltage measurement, V_{IN}, expressed in direct format.	0x000	RW

PEAK_VOUT REGISTER (0xD2)

The PEAK_VOUT command requests the device to report the peak V_{OUT} value. Writing 0x0000 resets the registers.

Table 33. Bit Descriptions for PEAK_VOUT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VOUT		Peak output voltage measurement, V_{OUT}, expressed in direct format.	0x000	RW

PMON_CONTROL REGISTER (0xD3)

The PMON_CONTROL command starts and stops the power monitor by 12-bit ADC.

Table 34. Bit Descriptions for PMON_CONTROL

Bits	Bit Name	Data	Descriptions	Defaut	Access
[7:1]	RESERVED		Always reads as 0000000.	0x00	RESERVED
0	CONVERT		Conversion enable.	0x1	RW
		0	Power monitor is not running.		
		1	Power monitor is sampling. Default. In single shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling. A rising edge on the conversion (CONV function of Pin 13) or writing "1" to CONVERT bit sets this bit to 1. During sampling, additional conversion edges are ignored.		

PMON_CONFIG REGISTER (0xD4)

The PMON_CONFIG command configures the power monitor. The data in this address are readable.

Table 35. Bit Descriptions for PMON_CONFIG

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:14]	RESERVED		Always reads as 00.	0x0	RESERVED
[13:11]	PWR_AVG		P_{IN} averaging.	0x0	RW
		000	Disables sample averaging for power.		
		001	Sets sample averaging for power to two samples.		
		010	Sets sample averaging for power to four samples.		
		011	Sets sample averaging for power to eight samples.		
		100	Sets sample averaging for power to 16 samples.		
		101	Sets sample averaging for power to 32 samples.		
		110	Sets sample averaging for power to 64 samples.		
		111	Sets sample averaging for power to 128 samples.		
[10:8]	VI_AVG		V_{IN} / V_{OUT} / I_{OUT} averaging.	0x7	RW
		000	Disables sample averaging for current and voltage.		
		001	Sets sample averaging for current and voltage to two samples.		
		010	Sets sample averaging for current and voltage to four samples.		
		011	Sets sample averaging for current and voltage to eight samples.		
		100	Sets sample averaging for current and voltage to 16 samples.		
		101	Sets sample averaging for current and voltage to 32 samples.		
		110	Sets sample averaging for current and voltage to 64 samples.		
		111	Sets sample averaging for current and voltage to 128 samples.		
[7:5]	RESERVED		Always reads as 000.	0x0	RESERVED
4	PMON_MODE		Conversion mode.	0x1	RW
		0	Single shot sampling.		
		1	Continuous sampling.		
3	TEMP1_EN		Enable temperature sampling.	0x0	RW
		0	Temperature sampling disabled.		
		1	Temperature sampling enabled.		
2	VIN_EN		Enable V_{IN} sampling.	0x1	RW
		0	V_{IN} sampling disabled.		
		1	V_{IN} sampling enabled.		
1	VOUT_EN		Enable V_{OUT} sampling.	0x0	RW
		0	V_{OUT} sampling disabled.		
		1	V_{OUT} sampling enabled.		
0	RESERVED		Always reads as 0.	0x0	RESERVED

ALERT1_CONFIG REGISTER (0xD5)
The ALERT1_CONFIG command configures the faults and warnings as the alert output on NALT1 pin. The data in this address are readable.

Table 36. Bit Descriptions for ALERT1_CONFIG

Bits	Bit Name	Data	Descriptions	Defaut	Access
15	FET_HEALTH_FAULT_EN1		FET health fault enable.	0x0	RW
14	IOUT_OC_FAULT_EN1		I_{OUT} overcurrent fault enable.	0x0	RW
13	VIN_OV_FAULT_EN1		V_{IN} overvoltage fault enable.	0x0	RW
12	VIN_UV_FAULT_EN1		V_{IN} undervoltage fault enable.	0x0	RW
11	CML_ERROR_EN1		Communications error enable.	0x0	RW
10	IOUT_OC_WARN_EN1		I_{OUT} overcurrent warning enable.	0x0	RW
9	HYSTERETIC_EN1		Hysteretic output enable.	0x0	RW
8	VIN_OV_WARN_EN1		V_{IN} overvoltage warning enable.	0x0	RW
7	VIN_UV_WARN_EN1		V_{IN} undervoltage warning enable.	0x0	RW
6	VOUT_OV_WARN_EN1		V_{OUT} overvoltage warning enable.	0x0	RW
5	VOUT_UV_WARN_EN1		V_{OUT} undervoltage warning enable.	0x0	RW
4	HS_INLIM_EN1		Hot swap in-limit enable.	0x0	RW
3	PIN_OP_WARN_EN1		P_{IN} overpower warning enable.	0x0	RW
2	OT_FAULT_EN1		Overtemperature fault enable.	0x0	RW
1	OT_WARN_EN1		Overtemperature warning enable.	0x0	RW
0	RESERVED		Always reads as 0.	0x0	RESERVED

ALERT2_CONFIG REGISTER (0xD6)
The ALERT2_CONFIG command configures the faults and warnings as the alert output on NALT2 pin. The data in this address are readable.

Table 37. Bit Descriptions for ALERT2_CONFIG

Bits	Bit Name	Data	Descriptions	Defaut	Access
15	FET_HEALTH_FAULT_EN2		FET health fault enable.	0x0	RW
14	IOUT_OC_FAULT_EN2		I_{OUT} overcurrent fault enable.	0x0	RW
13	VIN_OV_FAULT_EN2		V_{IN} overvoltage fault enable.	0x0	RW
12	VIN_UV_FAULT_EN2		V_{IN} undervoltage fault enable.	0x0	RW
11	CML_ERROR_EN2		Communications error enable.	0x0	RW
10	IOUT_OC_WARN_EN2		I_{OUT} overcurrent warning enable.	0x0	RW
9	HYSTERETIC_EN2		Hysteretic output enable.	0x0	RW
8	VIN_OV_WARN_EN2		V_{IN} overvoltage warning enable.	0x0	RW
7	VIN_UV_WARN_EN2		V_{IN} undervoltage warning enable.	0x0	RW
6	VOUT_OV_WARN_EN2		V_{OUT} overvoltage warning enable.	0x0	RW
5	VOUT_UV_WARN_EN2		V_{OUT} undervoltage warning enable.	0x0	RW
4	HS_INLIM_EN2		Hot swap in-limit enable.	0x0	RW
3	PIN_OP_WARN_EN2		P_{IN} overpower warning enable.	0x0	RW
2	OT_FAULT_EN2		Overtemperature fault enable.	0x0	RW
1	OT_WARN_EN2		Overtemperature warning enable.	0x0	RW
0	RESERVED		Always reads as 0.	0x0	RESERVED

PEAK_TEMPERATURE REGISTER (0xD7)
The PEAK_TEMPERATURE command requests the device to report the peak temperature value. Writing 0x0000 resets the registers.

Table 38. Bit Descriptions for PEAK_TEMPERATURE

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_TEMPERATURE		Peak temperature measurement, expressed in direct format.	0x000	RW

DEVICE_CONFIG REGISTER (0xD8)

The DEVICE_CONFIG command configures the severe overcurrent settings and GPO1/GPO2 output modes. The data in this address are readable.

Table 39. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
11	FHDIS		FET health disable.	0x0	RW
		0	FET health checks enabled.		
		1	FET health checks disabled.		
10	PWR_HYST_EN		When enabled, the general-purpose output alert hysteresis functions refer to power rather than current. The HYSTERETIC_ENx bit also needs to be set in ALERT_CONFIG.	0x0	RW
		0	Current hysteresis mode.		
		1	Power hysteresis mode.		
[9:8]	GPO2_MODE		GPO2 configuration mode.	0x0	RW
		00	Default. GPO2 is configured to generate SMBAlerts.		
		01	GPO2 can be used as a general-purpose digital output pin. Use the GPO2_INVERT bit to change the output state.		
		10	Reserved.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning bit selected for the output.		
7	GPO2_INVERT		GPO2 invert mode.	0x0	RW
		0	In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.		
		1	In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.		
[6:5]	GPO1_MODE		GPO1 configuration mode.	0x0	RW
		00	Default. GPO1 is configured to generate SMBAlerts.		
		01	GPO1 can be used as a general-purpose digital output pin. Use the GPO1_INVERT bit to change the output state.		
		10	GPO1 is configured as a convert (CONV) input pin.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning bit selected for the output.		
4	GPO1_INVERT		GPO1 invert mode.	0x0	RW
		0	In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.		
		1	In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.		
[3:2]	OC_TRIP_SELECT		Severe overcurrent threshold select.	0x11	RW
		00	125 %.		
		01	150 %.		
		10	200 %.		
		11	Default, 225 %.		
1	OC_RETRY_DIS		Severe OC retry mode.	0x0	RW
		0	Retry once immediately after severe overcurrent event.		
		1	Latch off after severe overcurrent event.		
0	OC_FILT_SELECT		Severe overcurrent filter select.	0x1	RW
		0	220 ns.		
		1	Default, 900 ns.		

POWER_CYCLE REGISTER (0xD9)

The POWER_CYCLE command forces the hot swap turn off and turn back on with the time interval programed on POWER_CYCLE_INTERVAL command.

PEAK_PIN REGISTER (0xDA)

The PEAK_PIN command requests the device to report the peak input power value. Writing 0x0000 resets the registers.

Table 40. Bit Descriptions for PEAK_PIN

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:0]	PEAK_PIN		Peak input power calculation, P_{IN}, expressed in direct format.	0x0000	RW

READ_PIN_EXT REGISTER (0xDB)

Reads the extended precision version of the calculated input power.

Table 41. Bit Descriptions for READ_PIN_EXT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[23:0]	READ_PIN_EXT		Extended precision version of peak input power calculation, P_{IN}, expressed in PMBus direct format.	0x000000	R

READ_EIN_EXT REGISTER (0xDC)
Reads the extended precision energy values in a single operation to ensure time consistent data.

Table 42. Bit Descriptions for READ_EIN_EXT

Bits	Bit Name	Data	Descriptions	Defaut	Access
[63:40]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 7 is the high byte, Byte 6 is the middle byte, and Byte 5 is the low byte.	0x000000	R
[39:24]	ROLLOVER_EXT		Number of times that the energy count has rolled over from 0x7FFFFF to 0x000000. This is an unsigned 16-bit binary value. Byte 4 is the high byte, and Byte 3 is the low byte.	0x0000	R
[23:0]	ENERGY_EXT		Extended precision energy accumulator value in PMBus direct format. Byte 2 is the high byte, Byte 1 is the middle byte, and Byte 0 is the low byte.	0x000000	R

POWER_CYCLE_INTERVAL REGISTER (0xDD)
The POWER_CYCLE_INTERVAL command sets the time interval on the POWER_CYCLE command. The data is readable.

Table 43. Bit Descriptions for POWER_CYCLE_INTERVAL

Bits	Bit Name	Data	Descriptions	Defaut	Access
[7:3]	RESERVED		Always reads as 000000.	0x0	RESERVED
[2:0]	PCYC_INTVL		Time interval from POWER_CYCLE command to turing back on again.	0x0	RW
		000	Defaut, 5 s.		
		001	10 s.		
		010	20 s.		
		011	30 s.		
		100	60 s.		
		101	120 s.		
		110	180 s.		
		111	240 s.		

HYSTERESIS_LOW REGISTER (0xF2)
The HYSTERESIS_LOW command sets the lower threshold for the hysteretic output signal which can be used on GPO.

Table 44. Bit Descriptions for HYSTERESIS_LOW

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:0]	HYSTERESIS_LOW		Value setting the lower hysteresis threshold, expressed in direct format.	0x0000	RW

HYSTERESIS_HIGH REGISTER (0xF3)
The HYSTERESIS_HIGH command sets the higher threshold for the hysteretic output signal which can be used on GPO.

Table 45. Bit Descriptions for HYSTERESIS_HIGH

Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:0]	HYSTERESIS_HIGH		Value setting the higher hysteresis threshold, expressed in direct format.	0xFFFF	RW

STATUS_HYSTERESIS REGISTER (0xF4)
The STATUS_HYSTERESIS command requests the device to report the overcurrent warning status and if the hysteresis comparison is above or below the programmable thresholds.

Table 46. Bit Descriptions for STATUS_HYSTERESIS

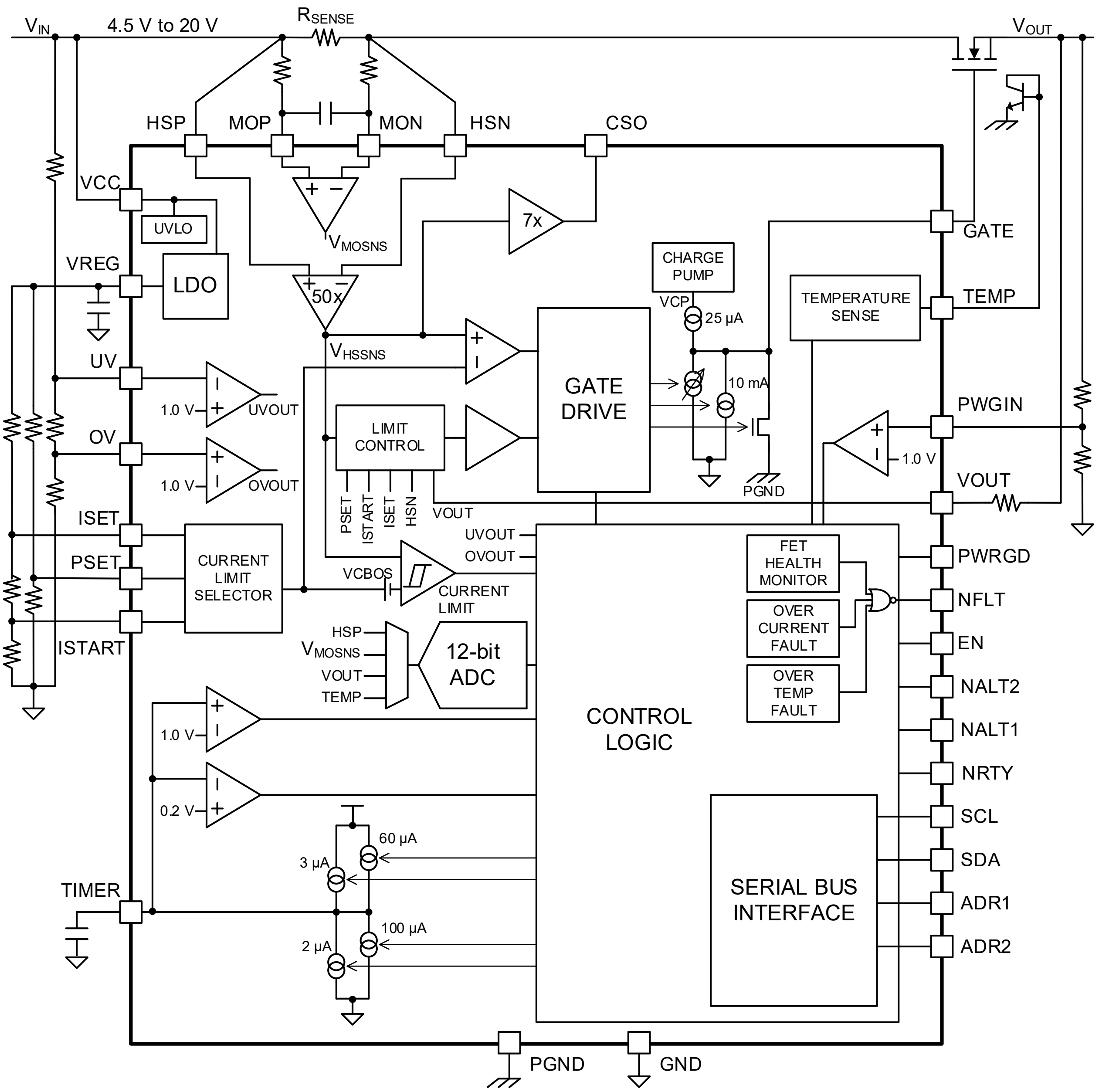
Bits	Bit Name	Data	Descriptions	Defaut	Access
[7:4]	RESERVED		Always reads as 0000.	0x0	RESERVED
3	IOUT_OC_WARN		I_{OUT} overcurrent warning.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
2	HYST_STATE		Hysteretic comparison output.	0x0	R
		0	Comparison output low.		
		1	Comparison output high.		
1	HYST_GT_HIGH		Hysteretic upper threshold comparison.	0x0	R
		0	Compared value is below upper threshold.		
		1	Compared value is above upper threshold.		
0	HYST_LT_LOW		Hysteretic lower threshold comparison.	0x0	R
		0	Compared value is above lower threshold.		
		1	Compared value is below lower threshold.		

STRT_UP_IOUT_LIM REGISTER (0xF6)
The STRT_UP_IOUT_LIM command sets the current limit level for the device start-up.

Table 47. Bit Descriptions for STRT_UP_IOUT_LIM

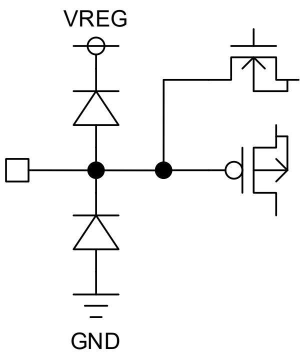
Bits	Bit Name	Data	Descriptions	Defaut	Access
[15:4]	RESERVED		Always reads as 0x000.	0x000	RESERVED
[3:0]	STRT_UP_IOUT_LIM		Current limit used during startup, expressed in direct format.	0xF	RW
		0000	Current limit equal to (ISTART × 1 / 16) (hot swap start up current limit level).		
		0001	Current limit equal to (ISTART × 2 / 16).		
		…	…		
		1110	Current limit equal to (ISTART × 15 / 16).		
		1111	Current limit equal to ISTART.		

Application Example

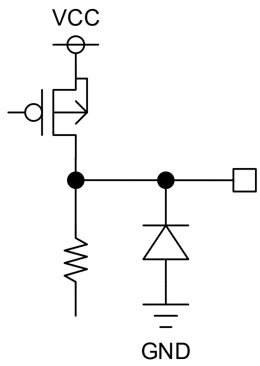


I/O Equivalence Circuits

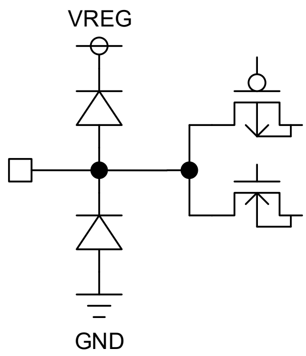
PSET , ISET



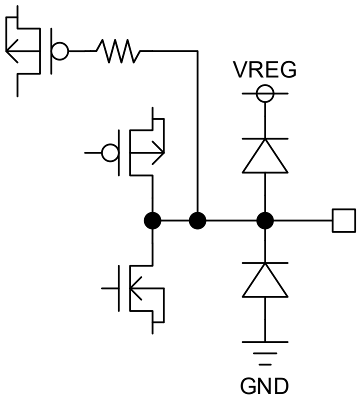
VREG



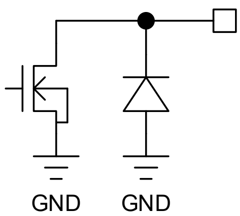
ISTART



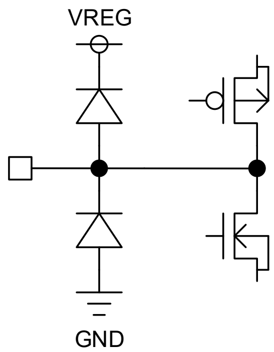
TIMER



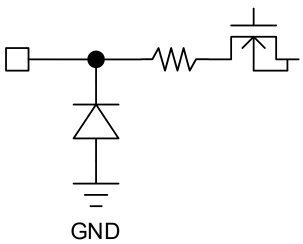
NFLT , PWRGD



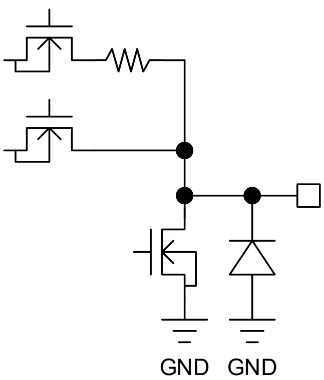
ADR1 , ADR2



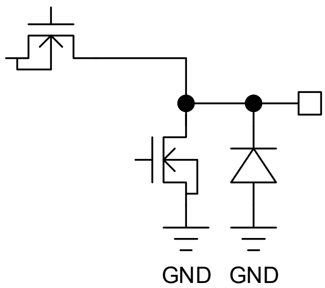
EN



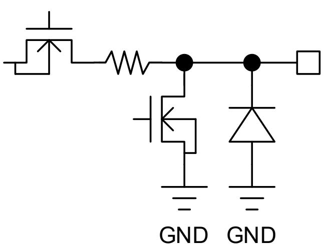
NALT1



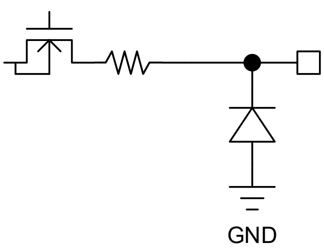
NALT2



SDA



SCL



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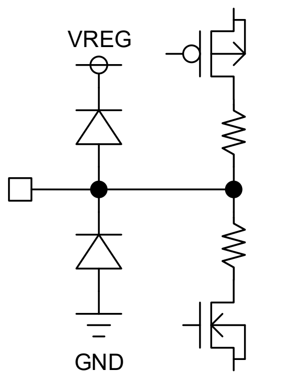
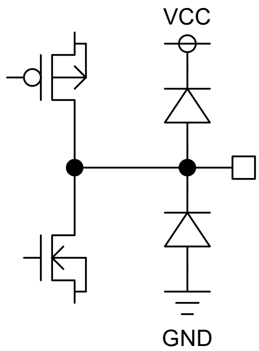
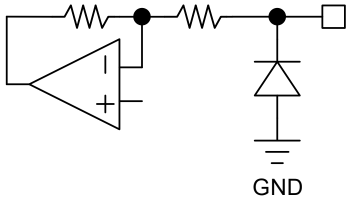
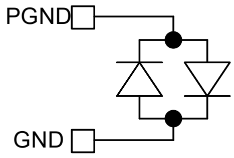
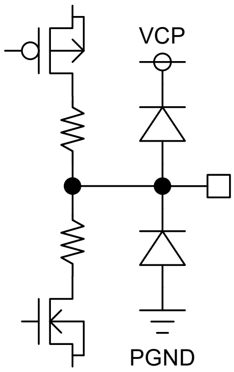
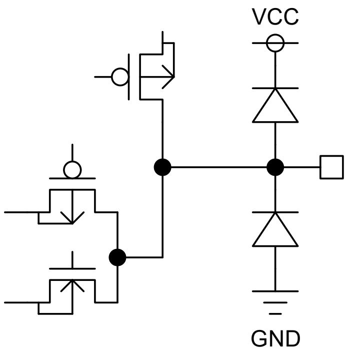
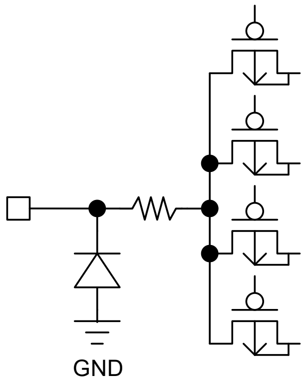
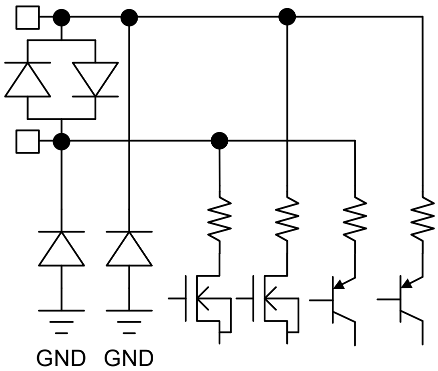
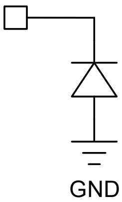
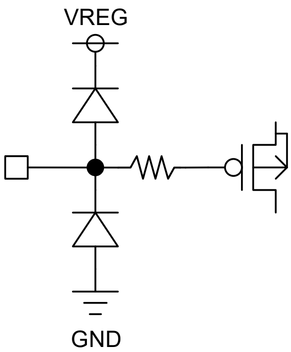


I/O Equivalence Circuits - continued

CSO	VOUT	GND , PGND
		
GATE	**TEMP**	**MOP , MON**
		
HSP , HSN	**VCC**	**UV , OV , PWGIN**
		

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

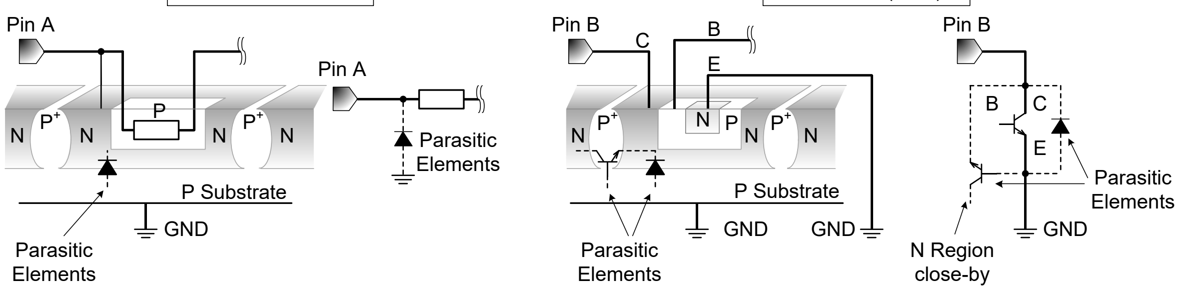


Figure 49. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

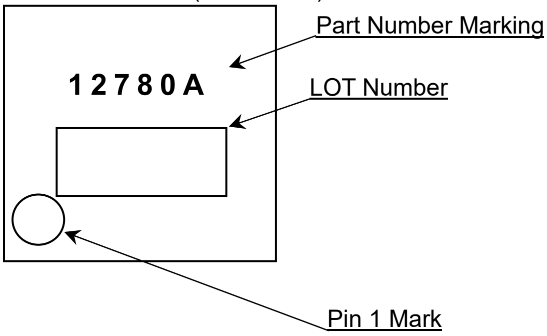
B D 1 2 7 8 0 A M U V - LB TR

Package
MUV: VQFN032V5050

Packaging and forming specification
LB: for Industrial Applications
TR: Embossed tape and reel

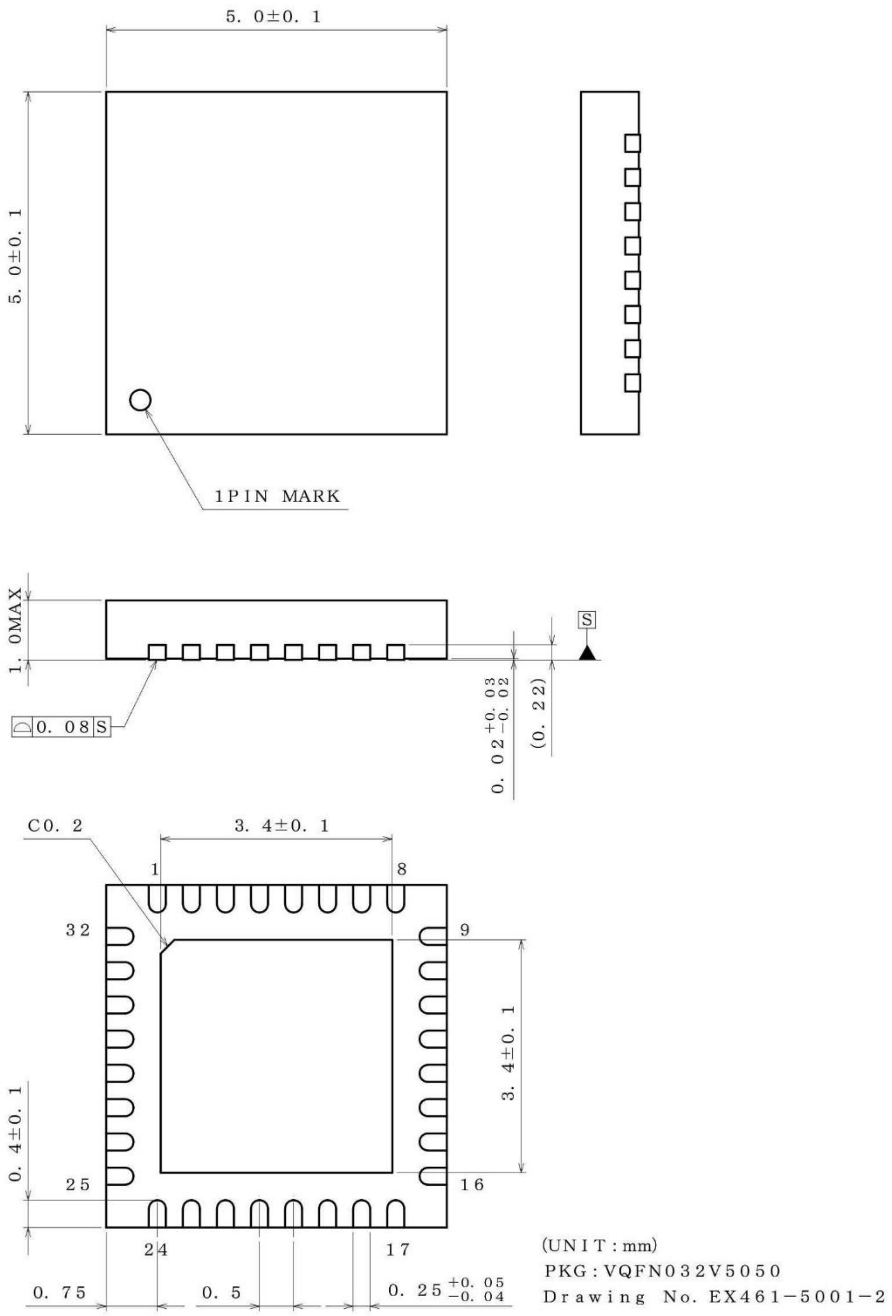
Marking Diagram

VQFN032V5050 (TOP VIEW)



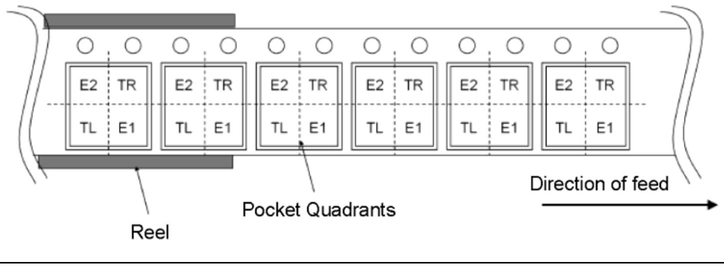
Physical Dimension and Packing Information

Package Name	VQFN032V5050



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
19.Sep.2025	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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