

# 2.7V to 5.5V, 2.0A 1ch Synchronous Buck Converter with Integrated FET

BD8960NV

## General Description

The BD8960NV is ROHM's high efficiency step-down switching regulator designed to produce a voltage as low as 1V from a supply voltage of 5.5V/3.3V. It offers high efficiency by using synchronous switches and provides fast transient response to sudden load changes by implementing current mode control.

## Features

- Fast Transient Response because of Current Mode Control System
- High Efficiency for All Load Ranges because of Synchronous Switches (Nch and Pch FET)
- Soft-Start Function
- Thermal Shutdown and ULVO Functions
- Short-Circuit Protection with Time Delay Function
- Shutdown Function

## Applications

Power Supply for LSI Including DSP, Microcomputer, and ASIC

## Key Specifications

■ Input Voltage Range:	2.7V to 5.5V
■ Output Voltage Range:	1.0V to 2.5V
■ Output Current:	2.0A (Max)
■ Switching Frequency:	1.0MHz(Typ)
■ Pch FET ON-Resistance:	200mΩ(Typ)
■ Nch FET ON-Resistance:	160mΩ(Typ)
■ Standby Current:	0μA (Typ)
■ Operating Temperature Range:	-25°C to +105°C

## Package

W(Typ) x D(Typ) x H(Max)



## Typical Application Circuit

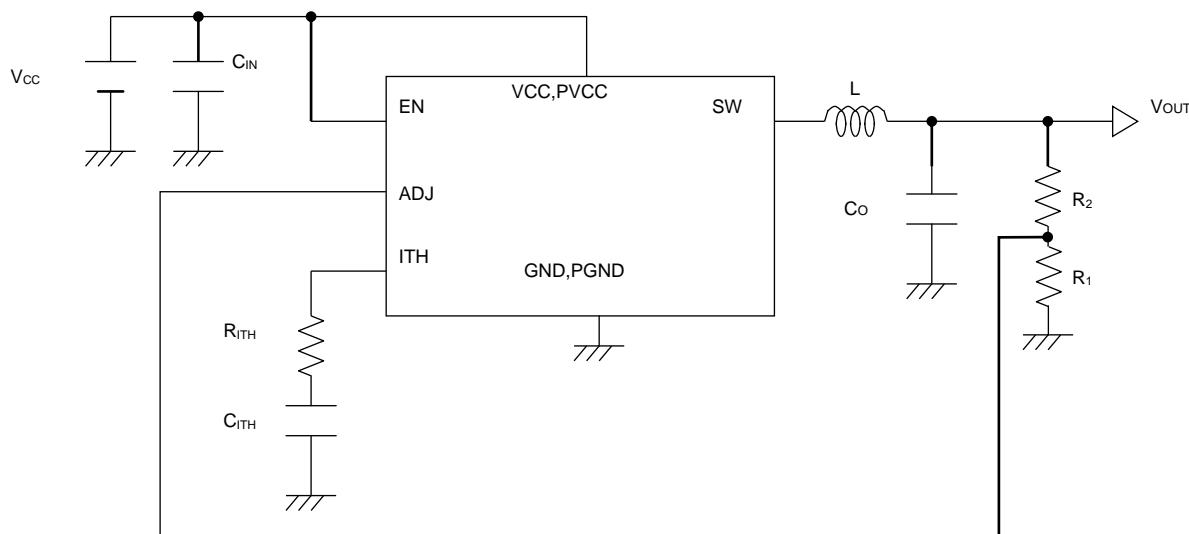


Figure 1. Typical Application Circuit

## Pin Configuration

(TOP VIEW)

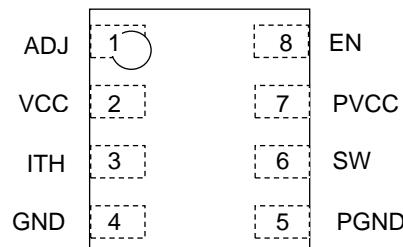


Figure 2. Pin Configuration

## Pin Description

Pin No.	Pin Name	Pin Function
1	ADJ	Output voltage detection pin
2	VCC	Power supply input pin
3	ITH	GmAmp output pin/connected to phase compensation capacitor
4	GND	Ground pin
5	PGND	Power switch ground pin
6	SW	Power switch node
7	PVCC	Power switch supply pin
8	EN	Enable pin(active high)

## Block Diagram

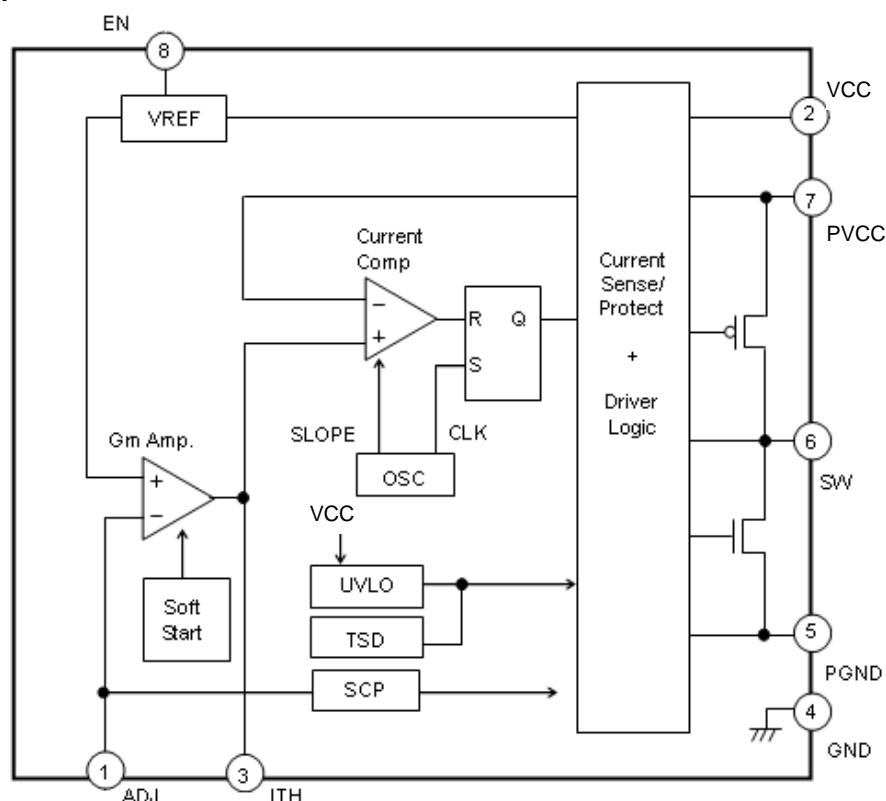


Figure 3. Block Diagram

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
VCC Voltage	V <sub>CC</sub>	-0.3 to +7 (Note 1)	V
PVCC Voltage	PV <sub>CC</sub>	-0.3 to +7 (Note 1)	V
EN Voltage	V <sub>EN</sub>	-0.3 to +7	V
SW, ITH Voltage	V <sub>SW</sub> , V <sub>ITH</sub>	-0.3 to +7	V
Power Dissipation 1	Pd1	0.90 (Note 2)	W
Power Dissipation 2	Pd2	3.90 (Note 3)	W
Operating Temperature Range	T <sub>opr</sub>	-25 to +105	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Maximum Junction Temperature	T <sub>jmax</sub>	+150	°C

(Note 1) Pd should not be exceeded.

(Note 2) Reduced by 7.2mW/°C over 25°C, Mounted on 70mm x 70mm x 1.6mm Glass Epoxy PCB.

(Note 3) Reduced by 31.2mW/°C over 25°C, Mounted on JESD51-7.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommended Operating Conditions (Ta=25°C)**

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
VCC Voltage	V <sub>CC</sub> (Note 4)	2.7 (Note 5)	3.3	5.5	V
PVCC Voltage	PV <sub>CC</sub> (Note 4)	2.7 (Note 5)	3.3	5.5	V
EN Voltage	V <sub>EN</sub>	0	-	V <sub>CC</sub>	V
SW Average Output Current	I <sub>SW</sub> (Note 4)	-	-	2.0	A
Output Voltage Setting Range	V <sub>OUT</sub>	1.0	-	2.5	V

(Note 4) Pd should not be exceeded.

(Note 5) In case the set output voltage is 1.6V or more, V<sub>CCMin</sub> = V<sub>OUT</sub> + 1.3V.**Electrical Characteristics (Ta=25°C, V<sub>CC</sub>=PV<sub>CC</sub>=3.3V, V<sub>EN</sub>=V<sub>CC</sub>, R<sub>1</sub>=10kΩ, R<sub>2</sub>=5kΩ, unless otherwise specified.)**

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Standby Current	I <sub>STB</sub>	-	0	10	µA	EN=GND
Bias Current	I <sub>CC</sub>	-	250	400	µA	VCC current
EN Low Voltage	V <sub>ENL</sub>	-	GND	0.8	V	Standby mode
EN High Voltage	V <sub>ENH</sub>	2.0	V <sub>CC</sub>	-	V	Active mode
EN Input Current	I <sub>EN</sub>	-	1	10	µA	V <sub>EN</sub> =3.3V
Oscillation Frequency	f <sub>OSC</sub>	0.8	1	1.2	MHz	
Pch FET ON-Resistance	R <sub>ONP</sub>	-	200	400	mΩ	PV <sub>CC</sub> =3.3V
Nch FET ON-Resistance	R <sub>ONN</sub>	-	160	350	mΩ	PV <sub>CC</sub> =3.3V
ADJ Voltage	V <sub>ADJ</sub>	0.788	0.800	0.812	V	
Output Voltage	V <sub>OUT</sub>	-	1.200	-	V	
ITH Sink Current	I <sub>THSI</sub>	10	20	-	µA	V <sub>ADJ</sub> =1.0V
ITH Source Current	I <sub>THSO</sub>	10	20	-	µA	V <sub>ADJ</sub> =0.6V
UVLO Threshold Voltage	V <sub>UVLO1</sub>	2.400	2.500	2.600	V	V <sub>CC</sub> =3V to 0V
UVLO Release Voltage	V <sub>UVLO2</sub>	2.425	2.550	2.700	V	V <sub>CC</sub> =0V to 3V
Soft Start Time	t <sub>s</sub>	0.5	1	2	ms	
Timer Latch Time	t <sub>LATCH</sub>	1	2	3	ms	SCP/TSD operated
Output Short Circuit Threshold Voltage	V <sub>SCP</sub>	-	V <sub>OUT</sub> x 0.5	V <sub>OUT</sub> x 0.7	V	V <sub>OUT</sub> =1.2V to 0V

## Typical Performance Curves

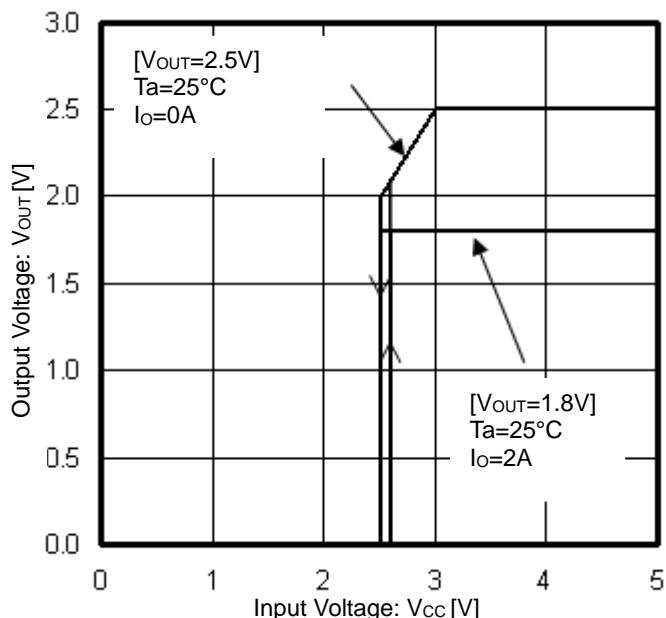


Figure 4. Output Voltage vs Input Voltage

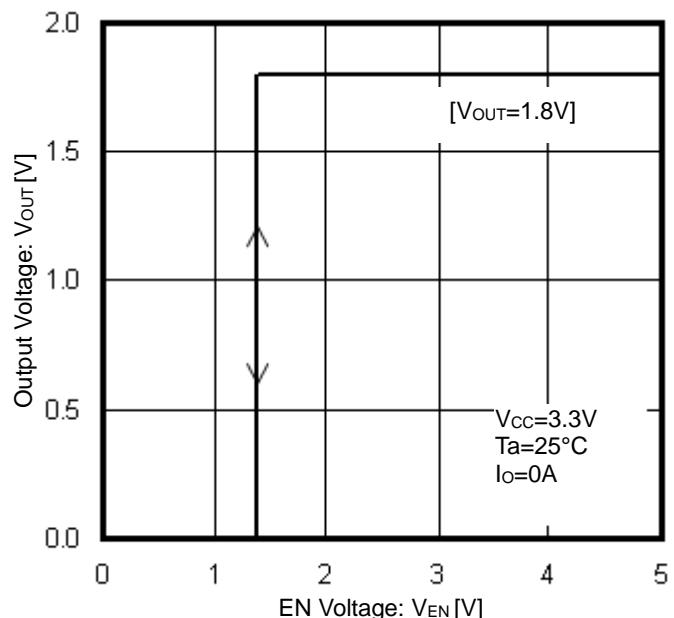


Figure 5. Output Voltage vs EN Voltage

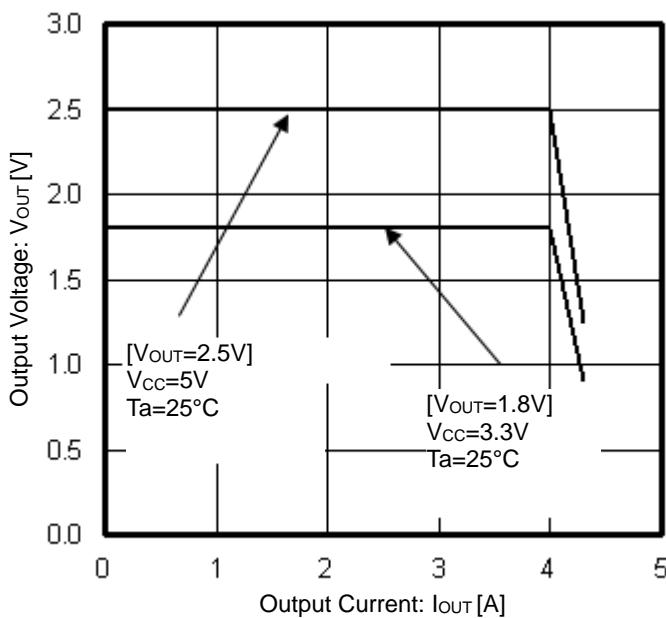


Figure 6. Output Voltage vs Output Current

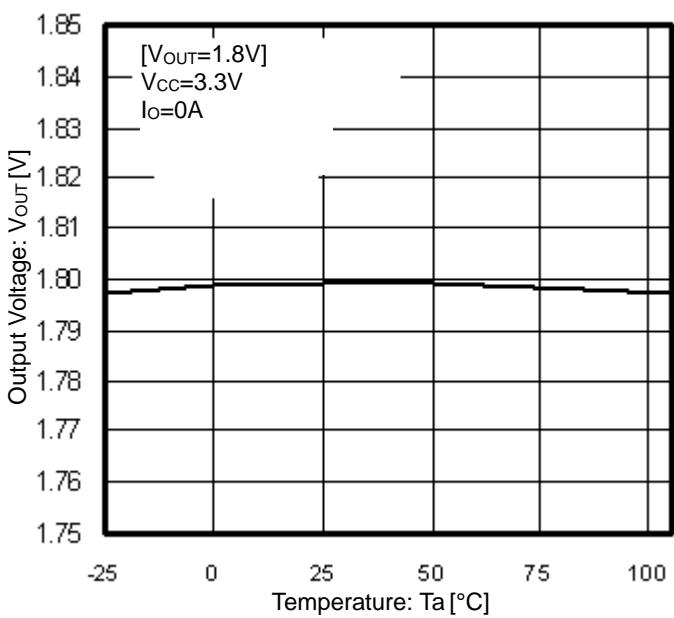
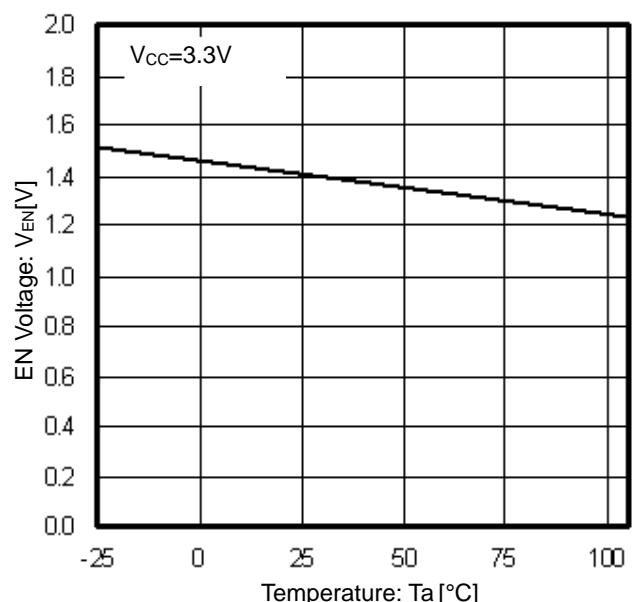
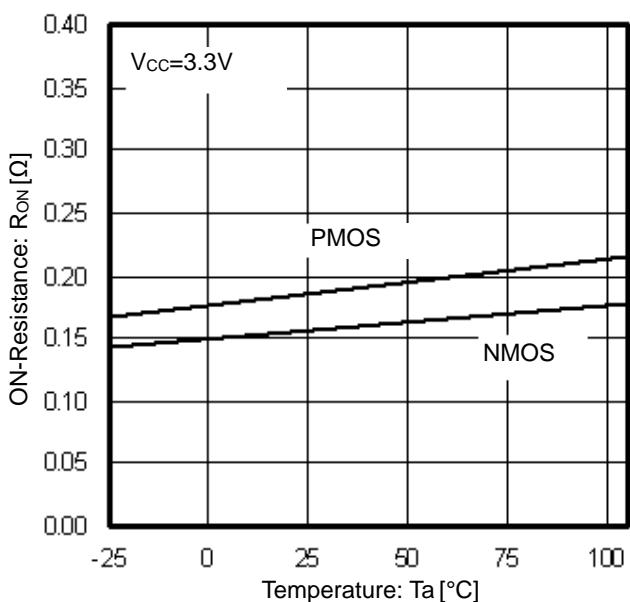
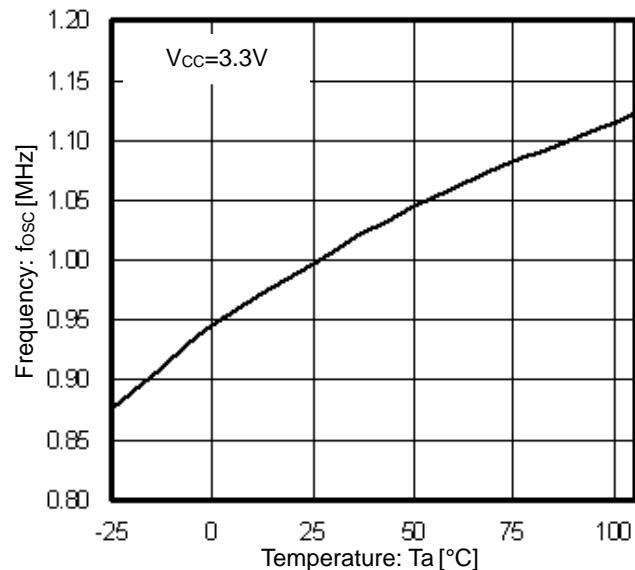
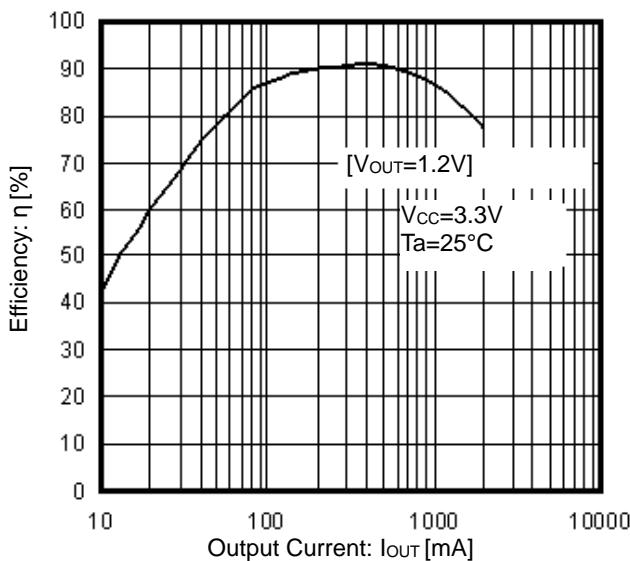


Figure 7. Output Voltage vs Temperature

## Typical Performance Curves - continued



## Typical Performance Curves - continued

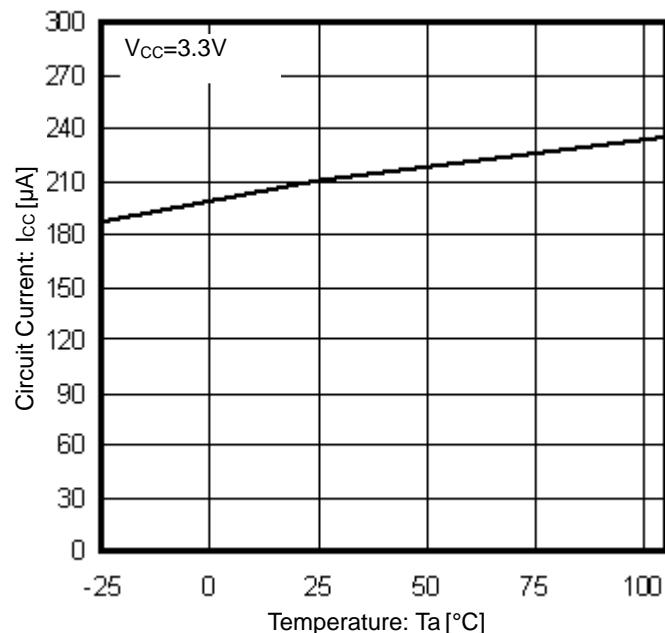


Figure 12. Circuit Current vs Temperature

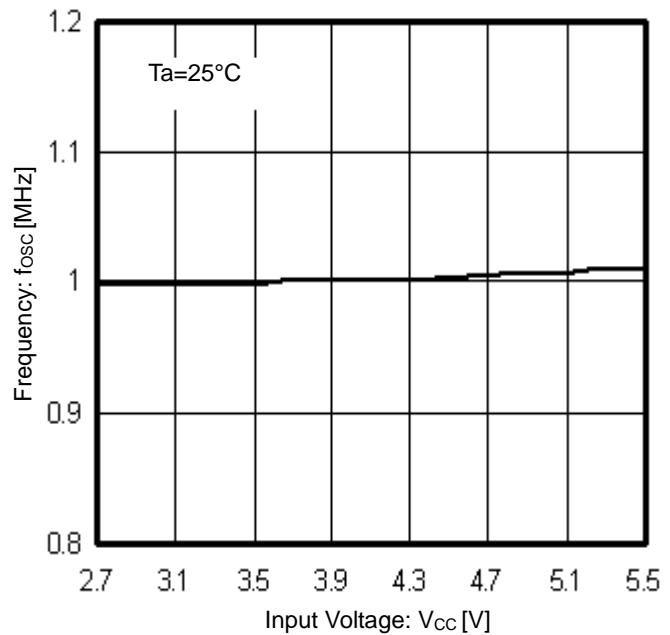


Figure 13. Frequency vs Input Voltage

## Typical Waveforms

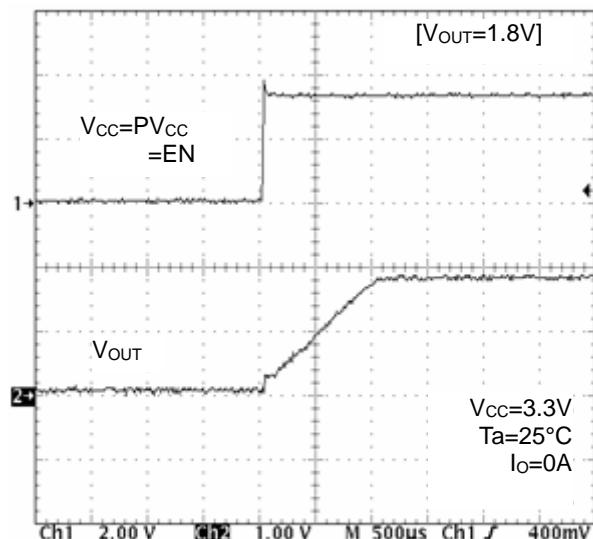
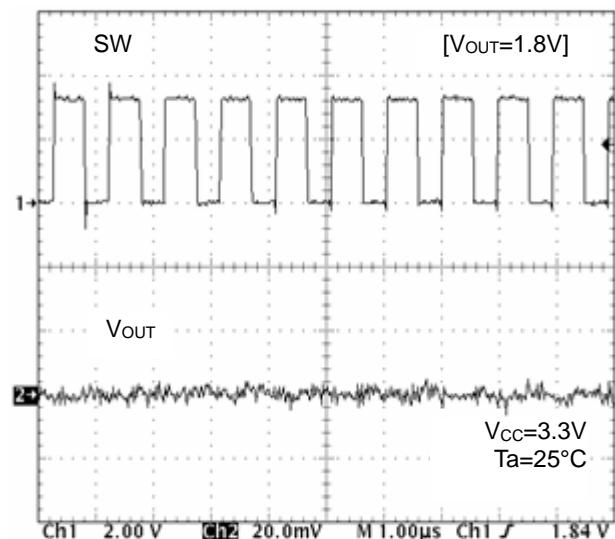
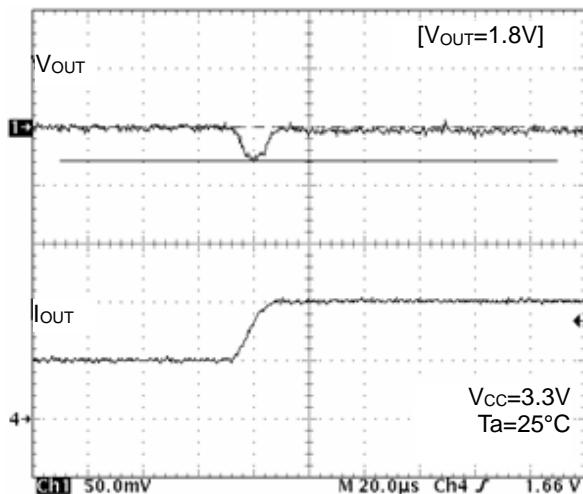
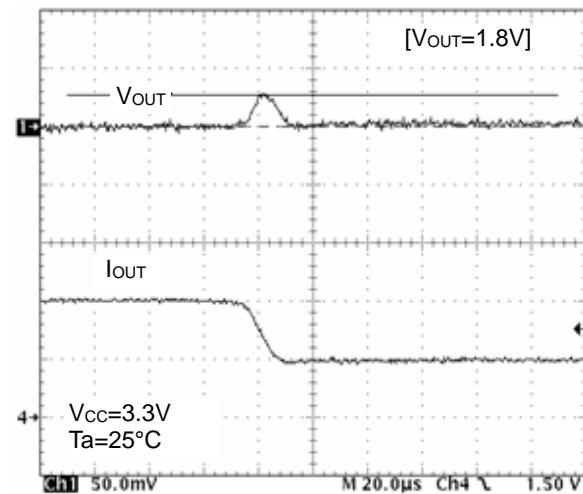


Figure 14. Soft Start Waveform

Figure 15. SW Waveform  
(I<sub>O</sub>=10mA)Figure 16. Transient Response  
(I<sub>O</sub>=1A to 2A, 10µs)Figure 17. Transient Response  
(I<sub>O</sub>=2A to 1A, 10µs)

## Application Information

### 1. Operation

BD8960NV is a synchronous step-down switching regulator that achieves fast transient response by employing current mode PWM control system.

#### (1) Synchronous Rectifier

Integrated synchronous rectification using two MOSFETS reduces power dissipation and increases efficiency when compared to converters using external diodes. Internal shoot-through current limiting circuit further reduces power dissipation.

#### (2) Current Mode PWM Control

The PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

##### (a) PWM (Pulse Width Modulation) control

The clock signal coming from OSC has a frequency of 1Mhz. When OSC sets the RS latch, the P-Channel MOSFET is turned ON and the N-Channel MOSFET is turned OFF. The opposite happens when the current comparator (Current Comp) resets the RS latch i.e. the P-Channel MOSFET is turned OFF and the N-Channel MOSFET is turned ON. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE" which is a voltage proportional to the current  $I_L$ , and the voltage feedback control signal, FB.

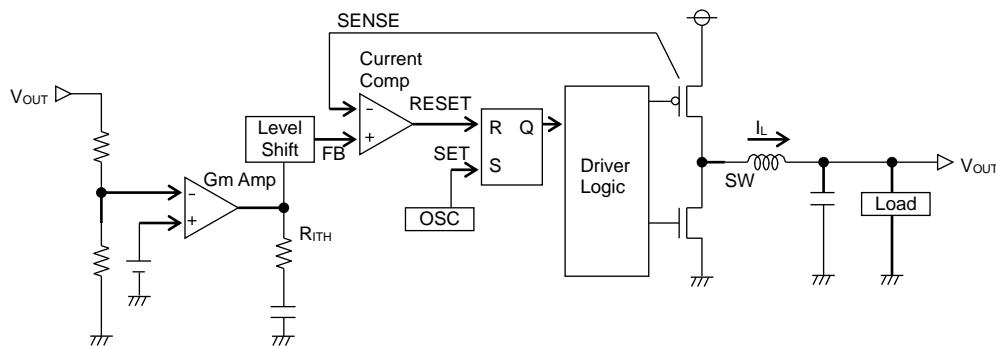


Figure 18. Diagram of Current Mode PWM Control

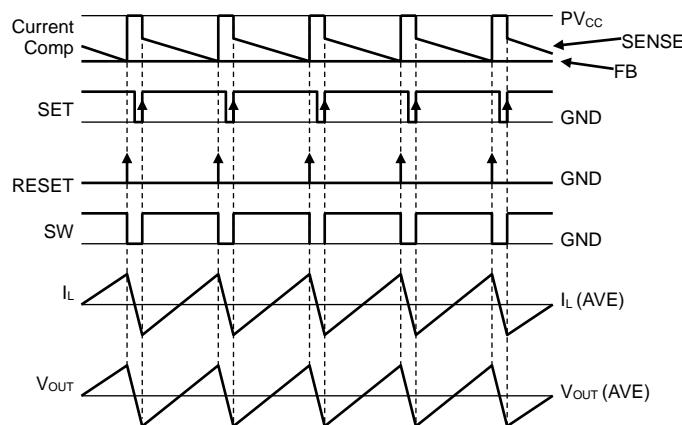


Figure 19. PWM Switching Timing Chart

## 2. Description of Functions

### (1) Soft-Start Function

During start-up, the soft-start circuit gradually establishes the output voltage to limit the input current. This prevents the overshoot in the output voltage and inrush current.

### (2) Shutdown Function

When the EN terminal is “low”, the device operates in Standby Mode and all functional blocks, including reference voltage circuit, internal oscillator and drivers, are turned OFF. Circuit current during standby is  $0\mu\text{A}$  (Typ).

### (3) UVLO Function

The UVLO circuit detects whether the supplied input voltage is sufficient to obtain the output voltage of this IC. The UVLO threshold, which has a hysteresis of 50mV (Typ), prevents output bouncing.

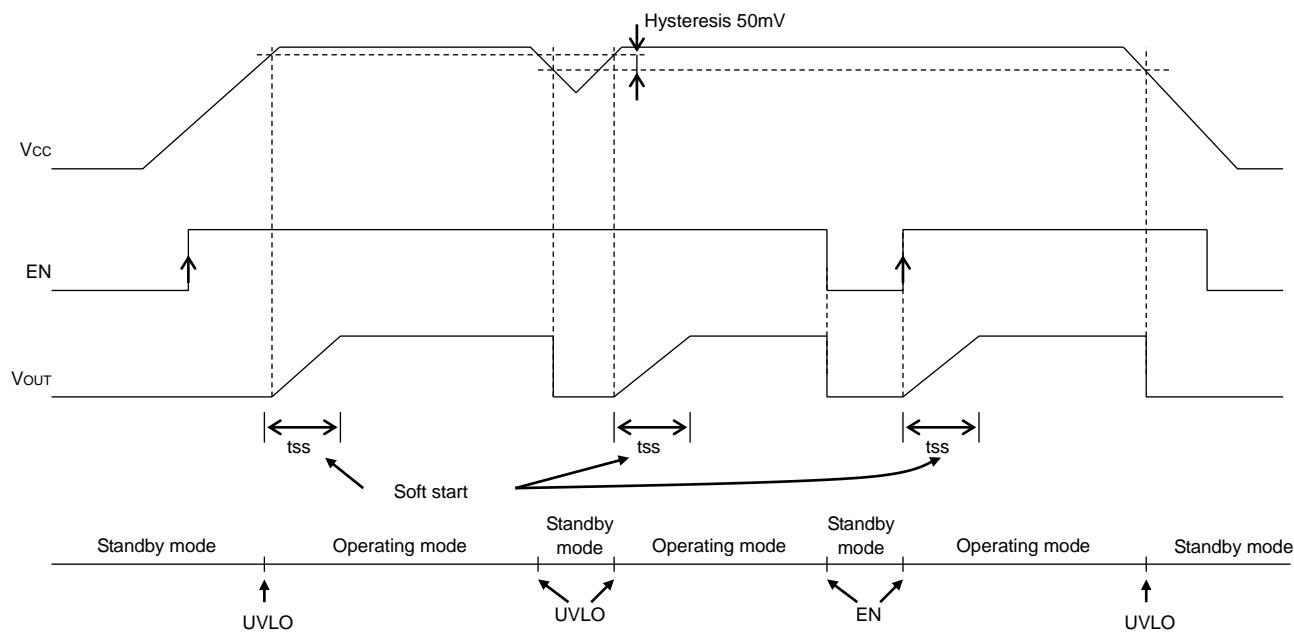


Figure 20. Soft Start, Shutdown, UVLO Timing Chart

### (4) Short-Circuit Protection Circuit with Time Delay Function

To protect the IC from breakdown, the short-circuit protection circuit turns the output OFF when the internal current limiter is activated continuously for a fixed time ( $t_{LATCH}$ ) or more. The output that is kept OFF may be turned on again by restarting EN or by resetting UVLO.

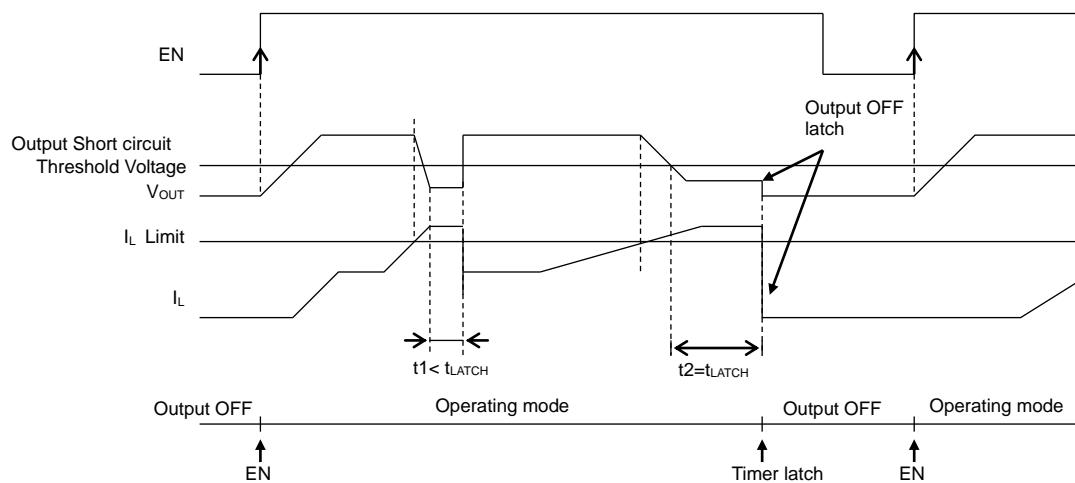
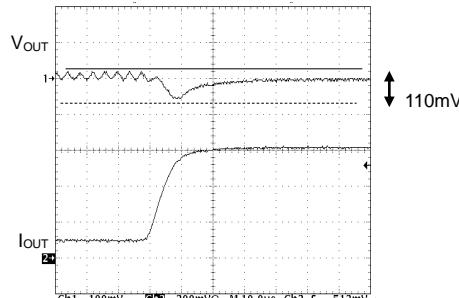


Figure 21. Short-Circuit Current Protection Circuit with Time Delay Timing Chart

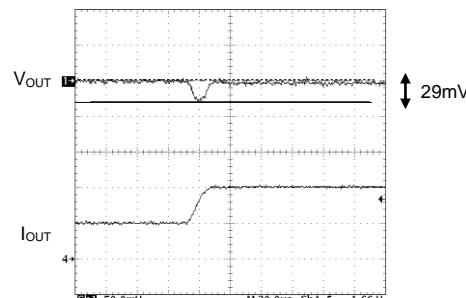
### 3. Information on Advantages

Advantage 1 : Offers fast transient response by using current mode control system

Conventional product (Load response  $I_{O}=0.1A$  to  $0.6A$ )



BD8960NV (Load response  $I_{O}=1A$  to  $2A$ )



Voltage drop due to sudden change in load was reduced by about 50%.

Figure 22. Comparison of Transient Response

Advantage 2 : Offers high efficiency because of its synchronous rectifiers

This IC utilizes the synchronous rectifying mode and uses low ON-Resistance MOSFET power transistors.

- { ON-Resistance of P-Channel MOS FET :  $200\text{m}\Omega$ (Typ)
- { ON-Resistance of N-Channel MOS FET :  $160\text{m}\Omega$ (Typ)

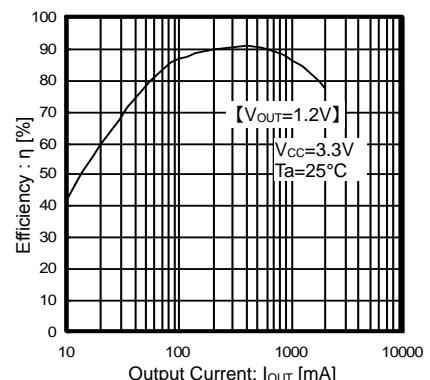


Figure 23. Efficiency

Advantage 3 : Supplied in smaller package due to small-sized power MOSFETs.

- ↓
- Output capacitor  $C_o$  required for current mode control:  $22\mu\text{F}$  ceramic capacitor
  - Inductance  $L$  required for the operating frequency of 1 MHz:  $2.2\mu\text{H}$  inductor

Reduces mounting area required.

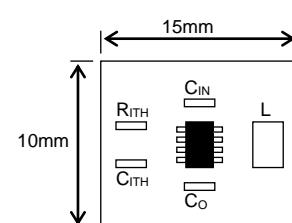
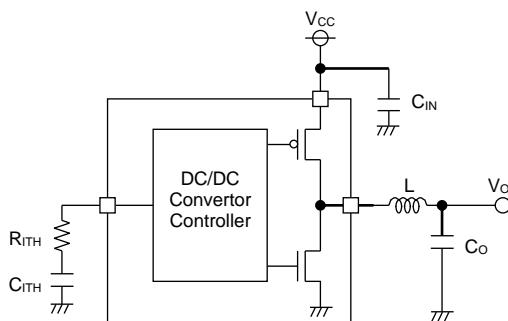


Figure 24. Example Application

#### 4. Switching Regulator Efficiency

Efficiency  $\eta$  may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100 = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{P_{OUT}}{P_{OUT} + P_{d\alpha}} \times 100 \quad [\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors  $P_{d\alpha}$  as follows:

Dissipation factors:

- (1) ON-Resistance Dissipation of Inductor and FET :  $P_d(I^2R)$

$$P_d(I^2R) = I_{OUT}^2 \times (R_{COIL} + R_{ON})$$

Where:

$R_{COIL}$  is the DC resistance of inductor

$R_{ON}$  is the ON-Resistance of FET

$I_{OUT}$  is the output Current

- (2) Gate Charge/Discharge Dissipation :  $P_d(\text{Gate})$

$$P_d(\text{Gate}) = C_{gs} \times f \times V^2$$

Where:

$C_{gs}$  is the gate capacitance of FET

$f$  is the switching frequency

$V$  is the gate driving voltage of FET.

- (3) Switching Dissipation :  $P_d(\text{SW})$

$$P_d(\text{SW}) = \frac{V_{IN}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

Where:

$C_{RSS}$  is the reverse transfer capacitance of FET

$I_{DRIVE}$  is the peak current of gate

- (4) ESR Dissipation of Capacitor :  $P_d(\text{ESR})$

$$P_d(\text{ESR}) = I_{RMS}^2 \times ESR$$

Where:

$I_{RMS}$  is the ripple current of capacitor

$ESR$  is the equivalent series resistance

- (5) Operating Current Dissipation of IC :  $P_d(\text{IC})$

$$P_d(\text{IC}) = V_{IN} \times I_{CC}$$

Where:

$I_{CC}$  is the circuit current

## 5. Consideration on Permissible Dissipation and Heat Generation

Since this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON-Resistance of FET are considered. This is because conduction losses are the most significant among other dissipations mentioned above, such as gate charge/discharge dissipation and switching dissipation.

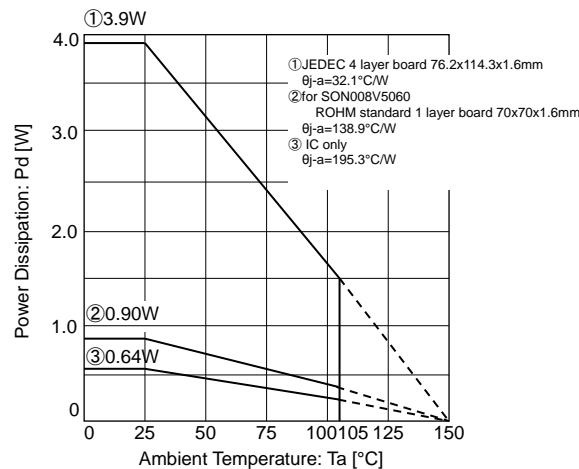


Figure 25. Thermal Derating Curve (SON008V5060)

If  $V_{CC}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $R_{ONP}=0.2\Omega$ ,  $R_{ONN}=0.16\Omega$   
 $I_{OUT}=2A$ , for example,  
 $D=V_{OUT}/V_{CC}=1.8/3.3=0.545$   
 $R_{ON}=0.545 \times 0.20 + (1-0.545) \times 0.16$   
 $=0.109+0.0728$   
 $=0.1818[\Omega]$

$$P=2^2 \times 0.1818 = 0.7272[W]$$

Since  $R_{ONP}$  is greater than  $R_{ONN}$  in this IC, the dissipation increases as the ON duty becomes greater. Taking into consideration the dissipation shown above, thermal design must be carried out with allowable sufficient margin.

$$P = I_{OUT}^2 \times R_{ON}$$

$$R_{ON} = D \times R_{ONP} + (1 - D)R_{ONN}$$

$D$  is the ON duty ( $=V_{OUT}/V_{CC}$ )

$R_{ONP}$  is the ON-Resistance of P-Channel MOS FET

$R_{ONN}$  is the ON-Resistance of N-Channel MOS FET

$I_{OUT}$  is the Output Current

## 6. Selection of Externally Connected Components

### (1) Selection of Inductor (L)

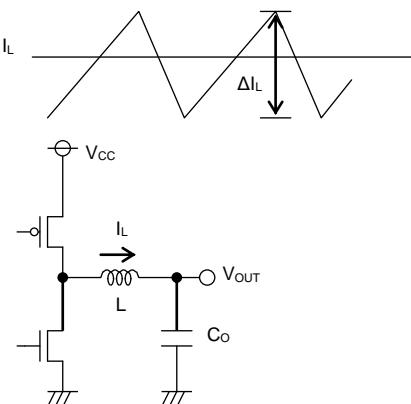


Figure 26. Output Ripple Current

The inductance significantly depends on output ripple current. As shown in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \quad [A] \dots (1)$$

Appropriate ripple current at output should be +/-20% of the maximum output current.

$$\Delta I_L = 0.2 \times I_{OUTMax} \quad [A] \dots (2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \quad [\text{H}] \dots (3)$$

Where:

$\Delta I_L$  is the Output ripple current, and

$f$  is the Switching frequency

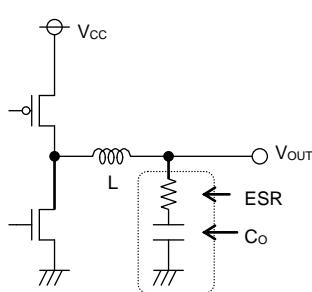
Note: Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If  $V_{CC}=3.3V$ ,  $V_{OUT}=1.8V$ ,  $f=1\text{MHz}$ ,  $\Delta I_L=0.2\text{A} \times 2\text{A}=0.4\text{A}$ , for example,(BD8960NV)

$$L = \frac{(3.3 - 1.8) \times 1.8}{0.4 \times 3.3 \times 1M} = 2.05\mu \rightarrow 2.2 \quad [\mu H]$$

Note: Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

### (2) Selection of Output Capacitor ( $C_O$ )



Output capacitor should be selected with the consideration of the stability region and the equivalent series resistance required to minimize ripple voltage.

Output ripple voltage is determined by equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \dots (4)$$

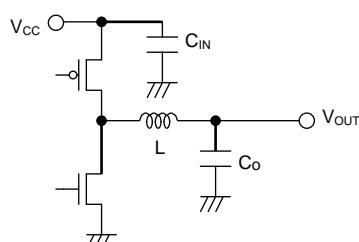
Where

$\Delta I_L$  is the Output ripple current, and

$ESR$  is the Equivalent series resistance of output capacitor

Note: Rating of the capacitor should be determined allowing sufficient margin against output voltage. A  $22\mu F$  to  $100\mu F$  ceramic capacitor is recommended. Less ESR allows reduction in output ripple voltage.

### (3) Selection of Input Capacitor ( $C_{IN}$ )



Input capacitor must be a low ESR capacitor with a capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current  $I_{RMS}$  is given by the equation (5):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \quad [A] \dots (5)$$

< Worst case >  $I_{RMSMax}$

$$\text{When } V_{CC} \text{ is twice the } V_{OUT}, \quad I_{RMS} = \frac{I_{OUT}}{2}$$

If  $V_{CC}=3.3V$ ,  $V_{OUT}=1.8V$ , and  $I_{OUTMax}=2\text{A}$ , (BD8960NV)

$$I_{RMS} = 2 \times \frac{\sqrt{1.8(3.3 - 1.8)}}{3.3} \approx 0.99 \quad [A_{RMS}]$$

A low ESR  $22\mu F/10V$  ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

(4) Calculating  $R_{ITH}$ ,  $C_{ITH}$  for Phase Compensation

As the Current Mode Control is designed to limit the inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of an output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

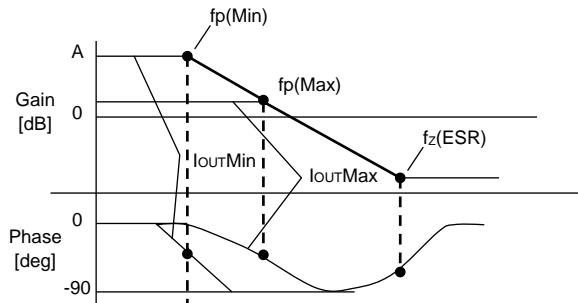


Figure 29. Open loop gain characteristics

$$f_p = \frac{1}{2\pi \times R_O \times C_O}$$

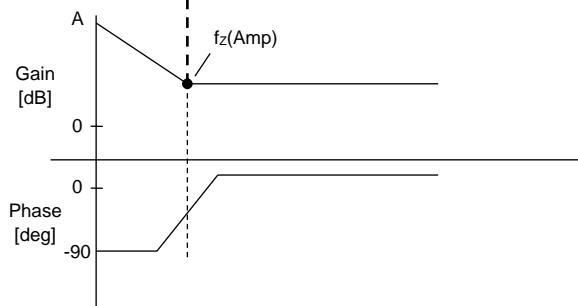
$$f_Z(ESR) = \frac{1}{2\pi \times ESR \times C_O}$$

## Pole at power amplifier

When the output current decreases, the load resistance  $R_O$  increases and the pole frequency decreases.

$$f_p(\text{Min}) = \frac{1}{2\pi \times R_{O\text{Max}} \times C_O} \quad [\text{Hz}] \leftarrow \text{with lighter load}$$

$$f_p(\text{Max}) = \frac{1}{2\pi \times R_{O\text{Min}} \times C_O} \quad [\text{Hz}] \leftarrow \text{with heavier load}$$



## Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR is reduced to half.)

$$f_Z(\text{Amp}) = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

Figure 30. Error amp phase compensation characteristics

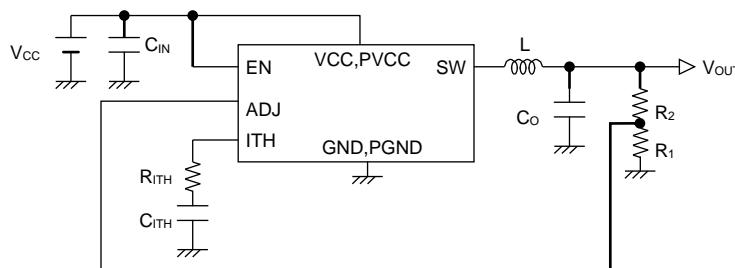


Figure 31. Typical Application Circuit

Stable feedback loop may be achieved by canceling the pole  $f_p$  (Min) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$f_Z(\text{Amp}) = f_p(\text{Min})$$

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{O\text{Max}} \times C_O}$$

## (5) Setting the Output Voltage

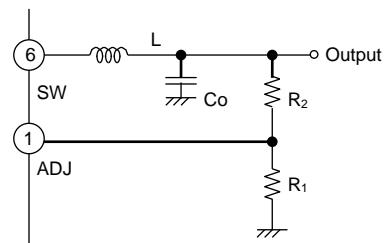
The output voltage  $V_{OUT}$  is determined by equation (6):

$$V_{OUT} = (R_2 / R_1 + 1) \times V_{ADJ} \quad \dots \dots (6)$$

Where:

$V_{ADJ}$  is the Voltage at ADJ terminal (0.8V Typ)

The required output voltage may be determined by adjusting  $R_1$  and  $R_2$ .



[Adjustable output voltage range : 1.0V to 2.5V]

Figure 32. Determination of Output Voltage

Use 1 kΩ to 100 kΩ resistor for  $R_1$ . If a resistor with resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

The lower limit of the input voltage depends on the output voltage. Basically, it is recommended to use the condition:

$$V_{CCMin} = V_{OUT} + 1.3V$$

Figure 33. shows the necessary output current value at the lower limit of input voltage. (DCR of inductor : 0.1Ω)  
This data is a characteristic value, so it doesn't guarantee the operating range.

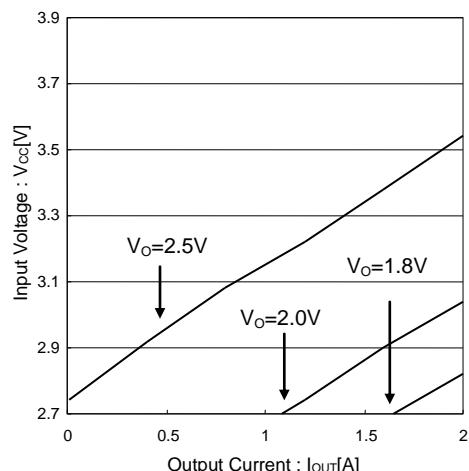


Figure 33. Minimum Input Voltage in each Output Voltage

## 7. BD8960NV Cautions on PC Board Layout

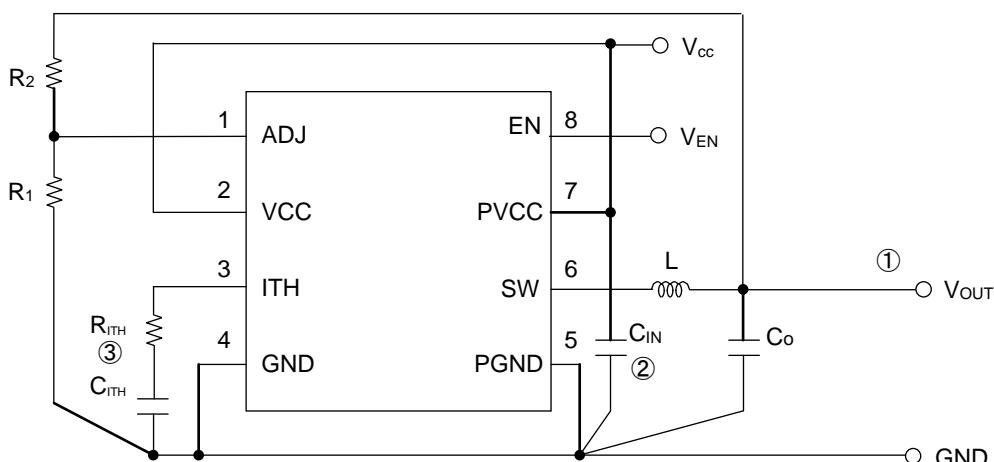


Figure 34. Layout Diagram

- ① For the sections drawn with heavy line, use thick conductor pattern as short as possible.
- ② Lay out the input ceramic capacitor  $C_{IN}$  closer to the pins PVCC and PGND, and the output capacitor  $C_O$  closer to the pin PGND.
- ③ Lay out  $C_{ITH}$  and  $R_{ITH}$  between the pins ITH and GND as neat as possible with least necessary wiring.

Note: SON008V5060 (BD8960NV) has thermal FIN on the reverse of the package.

The package thermal performance may be enhanced by bonding the FIN to GND plane which take a large area of PCB.

## 8. Recommended Components List for Above Application

Symbol	Part	Value	Manufacturer	Series
L	Coil	2.2μH	TDK	LTF5022-2R2N3R2
C <sub>IN</sub>	Ceramic capacitor	22μF	Kyocera	CM32X5R226M10A
C <sub>O</sub>	Ceramic capacitor	22μF	Kyocera	CM316B226M06A
C <sub>ITH</sub>	Ceramic capacitor	V <sub>OUT</sub> = 1.0V	680pF	Murata GMR18 Series
		V <sub>OUT</sub> = 1.2V	560pF	Murata GMR18 Series
		V <sub>OUT</sub> = 1.5V	470pF	Murata GMR18 Series
		V <sub>OUT</sub> = 1.8V	330pF	Murata GMR18 Series
		V <sub>OUT</sub> = 2.5V	330pF	Murata GMR18 Series
R <sub>ITH</sub>	Resistance	V <sub>OUT</sub> = 1.0V	10kΩ	Rohm MCR03 Series
		V <sub>OUT</sub> = 1.2V	12kΩ	Rohm MCR03 Series
		V <sub>OUT</sub> = 1.5V	15kΩ	Rohm MCR03 Series
		V <sub>OUT</sub> = 1.8V	18kΩ	Rohm MCR03 Series
		V <sub>OUT</sub> = 2.5V	18kΩ	Rohm MCR03 Series

Note: The parts list presented above is an example of the recommended parts. Although the parts are standard, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins.

## I/O Equivalent Circuit

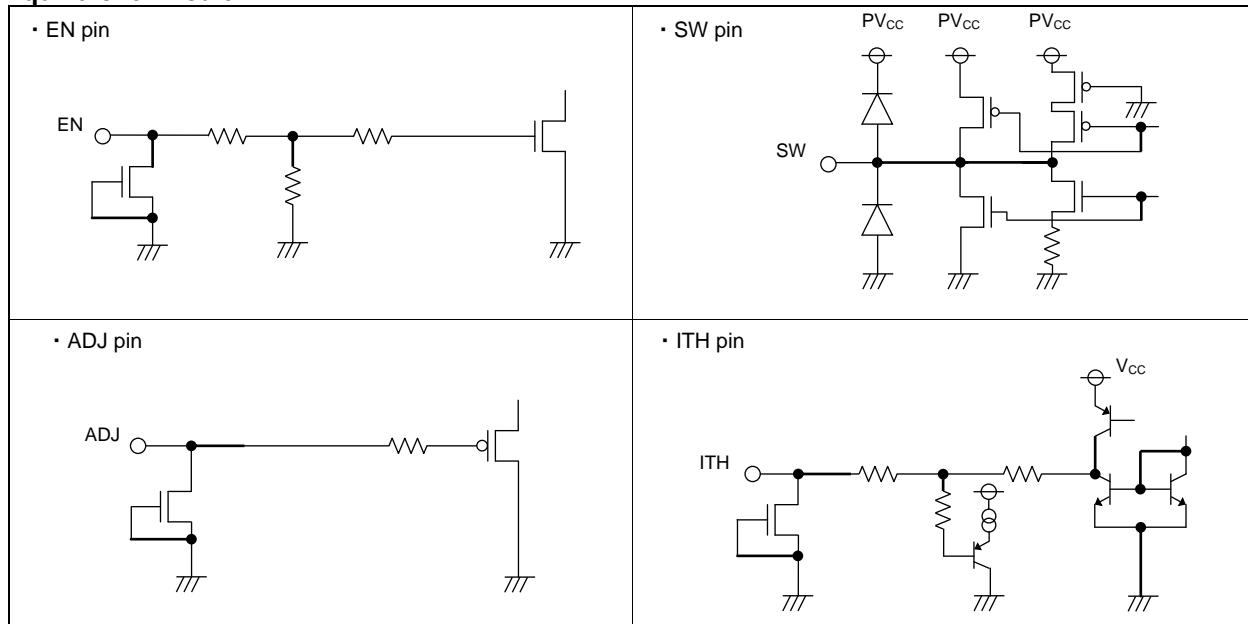


Figure 35. I/O Equivalent Circuit

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the  $P_d$  rating.

### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

### 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

### 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

### 12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

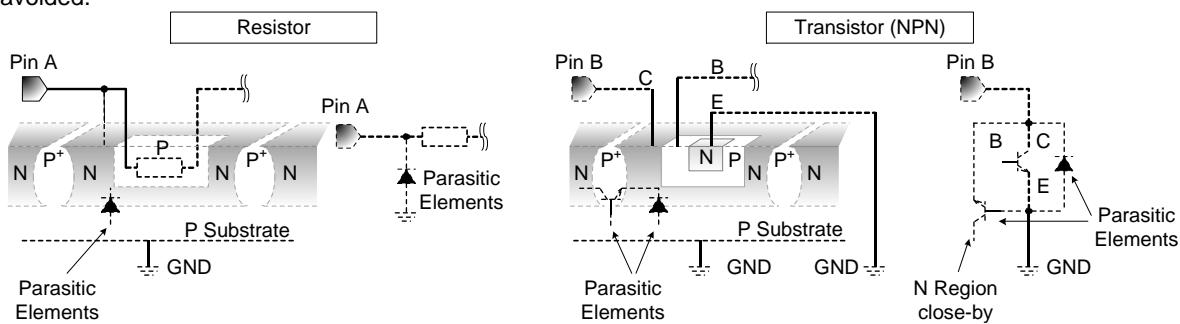


Figure 36. Example of monolithic IC structure

### 13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

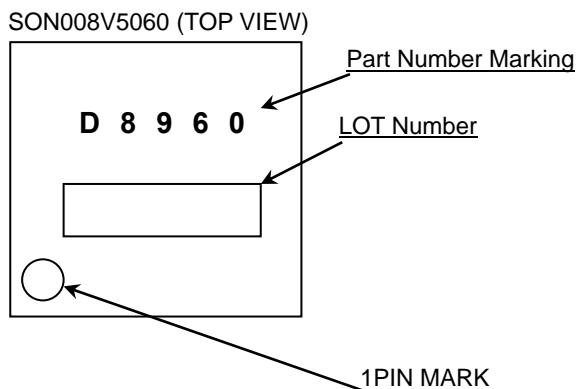
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

### 14. Selection of Inductor

It is recommended to use an inductor with a series resistance element (DCR)  $0.1\Omega$  or less. Especially, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over  $0.1\Omega$ , be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within.

**Ordering Information**

B D 8 9 6 0 N V	-	E 2
Part Number	Package NV:SON008V5060	Packaging and forming specification E2: Embossed tape and reel

**Marking Diagram**

## **Physical Dimension Tape and Reel information**

Package Name	SON008V5060
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The figure consists of three parts: a top view of the package with a pin mark, a detailed lead frame diagram with dimensions and pin numbers, and a tape layout diagram. The top view shows a square package with a circular pin mark at the bottom left. The lead frame diagram shows a rectangle with four pins on the top edge and four U-shaped lead frames on the sides. Pin 1 is at the top-left, followed by 2, 3, and 4. Below them are pins 8, 7, 6, and 5. Dimensions include 5.0 ± 0.15 mm width, 6.0 ± 0.15 mm height, 1.0 MAX height for the top pins, 0.8 ± 0.1 mm side height, 0.25 mm side width, 4.2 ± 0.1 mm total width, 1.27 mm pitch between pins 1-4 and 3-4, 0.59 mm side length, and 0.4 ± 0.05 mm bottom height. The tape layout shows the lead frame on a reel with a direction of feed arrow pointing right, and a note stating 'Order quantity needs to be multiple of the minimum quantity.'

**<Tape and Reel information>**

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel      1pin      Direction of feed

\*Order quantity needs to be multiple of the minimum quantity.

**Revision History**

Date	Revision	Changes
02.Mar.2012	001	New Release
02.Oct.2014	002	Typical Application Circuit and Marking Diagram modified. Applied the ROHM Standard Style and improved understandability.

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JAPAN	USA	EU	CHINA
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CLASS IV		CLASS III	CLASS III

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  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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