2.7 V to 5.5 V Input, 3.0 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9B306NF-Z

General Description

BD9B306NF-Z is one of the BD9Bx06NF-Z series of single synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. It can provide current up to 3 A. The output voltage can achieve a high accuracy due to ±1 % reference voltage. It features fast transient response due to constant on-time control system. The Light Load Mode control improves efficiency in light-load conditions. It is ideal for reducing standby power consumption of equipment. Power Good function makes it possible for system to control sequence. It achieves the high power density and offer a small footprint on the PCB by employing 6 pins 1.5 mm x 1.5 mm small package.

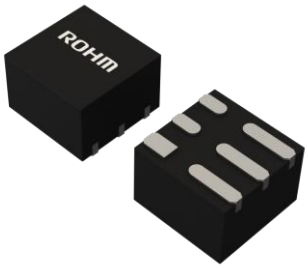
Features

- Single Synchronous Buck DC/DC Converter
- Constant On-time Control
- Light Load Mode Control
- ±1 % Reference Voltage Accuracy
- 100 % Duty Cycle
- Power Good Output
- Output Discharge Function
- Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Short Circuit Protection (SCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lockout Protection (UVLO)

Key Specifications

- Input Voltage Range: 2.7 V to 5.5 V
- Output Voltage Range: 0.6 V to 4.0 V
- Output Current: 3.0 A (Max)
- Switching Frequency: 2.2 MHz (Typ)
- High Side FET ON Resistance: 25 mΩ (Typ)
- Low Side FET ON Resistance: 25 mΩ (Typ)
- Shutdown Current: 0 μA (Typ)
- Quiescent Current at No Load: 4 μA (Typ)

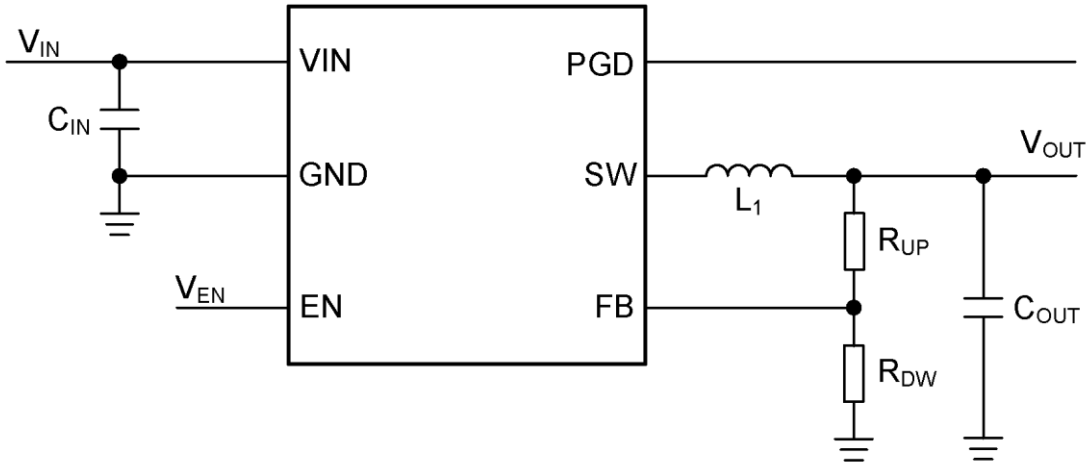
Package	**W (Typ) x D (Typ) x H (Max)**
VFN006V1515A	1.5 mm x 1.5 mm x 1.0 mm



Applications

- Printer, OA Equipment
- Laptop PC / Tablet PC / Server
- Storage Device (HDD / SSD)
- Step-down Power Supply for SoC, FPGA, and Microprocessor
- Video Surveillance
- Distributed Power Supply, Secondary Power Supply

Typical Application Circuit

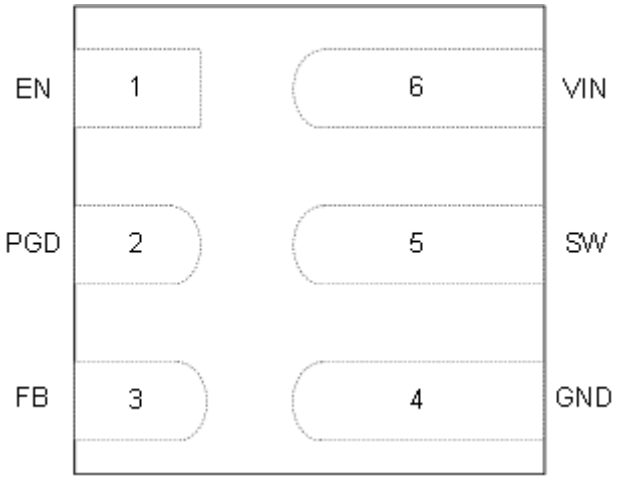


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration

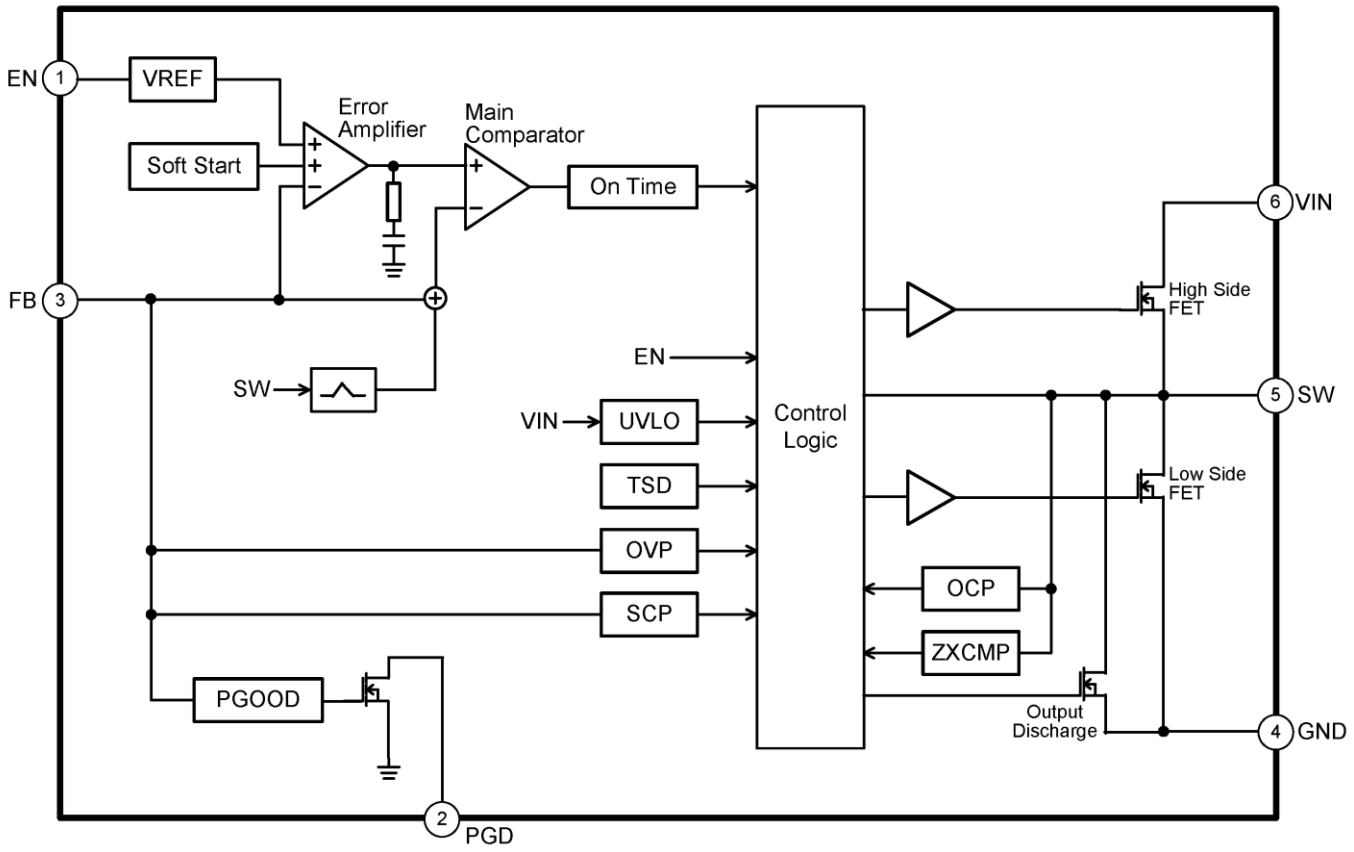
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	EN	Enable pin. The device starts up with setting V_{EN} to 1.00 V or more. The device enters the shutdown mode with setting V_{EN} to 0.40 V or less. This pin must not be left open.
2	PGD	Power Good pin. This pin is an open drain output that requires a pull-up resistor. See Function Explanations 1. Basic Operation (5) Power Good Output for setting the resistance. If not used, this pin can be left floating or connected to the ground.
3	FB	Output voltage feedback pin. See Application Examples 3. Output Voltage Setting for how to calculate the resistances of the output voltage setting.
4	GND	Ground pin.
5	SW	Switch pin. This pin is connected to the source of the High Side FET and the drain of the Low Side FET. Connect an inductor considering the direct current superimposition characteristic.
6	VIN	Power supply pin. Connecting 4.7 µF (Typ) ceramic capacitors is recommended. The detail of a selection is described in Application Examples 2. Input Capacitor.

Block Diagram



Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.
2. Soft Start
   The Soft Start circuit slows down the rise of output voltage during start-up and controls the current, which allows the prevention of output voltage overshoot and inrush current. The soft start time is fixed 1.25 ms (Typ).
3. Error Amplifier
   The Error Amplifier adjusts the Main Comparator input voltage to make the internal reference voltage equal to FB voltage.
4. Main Comparator
   The Main Comparator compares the Error Amplifier output voltage and FB voltage (V_{FB}). When V_{FB} becomes lower than the Error Amplifier output voltage, the output turns high and reports to the On Time block that the output voltage has dropped below the control voltage.
5. On Time
   This block generates On Time. The designed On Time is generated after the Main Comparator output turns high. The On Time is adjusted to control the frequency to be fixed even with input / output voltage is changed.
6. PGOOD
   The PGOOD block is for power good function.
7. UVLO
   The UVLO block is for under voltage lockout protection. The device is shutdown when input voltage V_{IN} falls to 2.200 V (Typ) or less. The threshold voltage has the 400 mV (Typ) hysteresis.
8. TSD
   The TSD block is for thermal protection. The device is shutdown when the junction temperature Tj reaches to 175 °C (Typ) or more. The device is automatically restored to normal operation with a hysteresis of 25 °C (Typ) when the Tj goes down.
9. OVP
   The OVP block is for output over voltage protection. When the FB voltage (V_{FB}) exceeds 110 % (Typ) or more of FB threshold voltage V_{FBTH}, the output MOSFETs are turned off. After V_{FB} falls 105 % (Typ) or less of V_{FBTH}, the output MOSFETs are returned to normal operation condition.
10. OCP
    The OCP block is for over current protection. This function operates by limiting the current that flows through the High Side FET and the Low Side FET at each cycle of the switching frequency.
11. SCP
    The SCP is for short circuit protection. When 256 times OCP are counted on the condition where the device completes the soft start and the output voltage falls below 92 % (Typ) of the setting voltage, the device is shutdown for 130 ms (Typ). After 130 ms shutdown, the device restarts. (HICCUP operation)
12. ZXCMP
    The ZXCMP is a comparator that monitors the inductor current. When inductor current falls below 0 A (Typ) while the Low Side FET is on, it turns the FET off.
13. Control Logic
    The Control Logic controls the switching operation and protection function operation.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +6	V
EN Voltage	V_{EN}	-0.3 to +V_{IN}	V
PGD Voltage	V_{PGD}	-0.3 to +6	V
FB Voltage	V_{FB}	-0.3 to +V_{IN}	V
SW Voltage (DC)	V_{SW}	-0.3 to V_{IN} + 0.3	V
SW Voltage (AC, less than 10 ns)	V_{SWAC}	-2.5 to +7	V
Maximum Junction Temperature *(Note 1)*	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The lifetime and reliability of the device is reduced if the device operates continually at the maximum junction temperature.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
VFN006V1515A				
Junction to Ambient	θ_{JA}	219.9	113.3	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	21.6	15.0	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	2.7	-	5.5	V
Operating Junction Temperature	Tj	-40	-	+125	°C
Output Current *(Note 1)*	I_{OUT}	0	-	3.0	A
Output Voltage Setting	V_{OUT}	0.6	-	4.0	V

(Note 1) Tj must be lower than 125 °C under the actual operating environment.

Electrical Characteristics

(Unless otherwise specified Tj = -40 to +125 °C, V_{IN} = 5 V, V_{EN} = 5 V, Typical values are at Tj = +25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Supply						
Shutdown Current	I_{SDN}	-	0	1.5	µA	V_{EN} = 0 V, Tj = 25 °C
Quiescent Current at No Load	I_Q	-	4	12	µA	I_{OUT} = 0 A, Tj = 25 °C No switching
UVLO Detection Threshold Voltage	V_{UVLO1}	2.125	2.200	2.275	V	V_{IN} falling
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	-	400	-	mV	
Enable						
EN Input Voltage High	V_{ENH}	1.0	-	V_{IN}	V	V_{EN} rising
EN Input Voltage Low	V_{ENL}	GND	-	0.4	V	V_{EN} falling
EN Input Current	I_{EN}	-	0	1	µA	V_{EN} = 5 V, Tj = 25 °C
Reference Voltage, Error Amplifier, Soft Start						
FB Threshold Voltage	V_{FBTH}	0.594	0.600	0.606	V	V_{IN} = 5 V, PWM mode
FB Input Current	I_{FB}	-	-	50	nA	V_{FB} = 0.6 V, Tj = 25 °C
Soft Start Time	t_{SS}	-	1.25	-	ms	
On Time						
On Time	t_{ON}	185	248	310	ns	V_{IN} = 3.3V, V_{OUT} = 1.8 V, PWM mode, Tj = 25 °C
SW (MOSFET)						
High Side FET ON Resistance	R_{ONH}	-	25	36	mΩ	V_{IN} = 5 V, Tj = 25 °C
Low Side FET ON Resistance	R_{ONL}	-	25	36	mΩ	V_{IN} = 5 V, Tj = 25 °C
High Side FET Leakage Current	I_{LKH}	-	0	10	µA	No switching, Tj = 25 °C
Low Side FET Leakage Current	I_{LKL}	-	0	10	µA	No switching, Tj = 25 °C
High Side FET Current Limit *(Note 3)*	I_{HOCP}	4.0	5.3	6.6	A	
Low Side FET Current Limit *(Note 3)*	I_{LOCP}	3.4	4.0	4.6	A	
SW Discharge Resistance	R_{DIS}	-	5	-	Ω	V_{EN} = 0 V, V_{SW} = 0.3 V
Power Good						
PGD Rising (Good) Voltage	V_{PGDRG}	94	96	98	%	V_{FB} rising, $V_{PGDRG} = V_{FB} / V_{FBTH} \times 100$
PGD Falling (Fault) Voltage	V_{PGDFF}	90	92	94	%	V_{FB} falling, $V_{PGDFF} = V_{FB} / V_{FBTH} \times 100$
PGD Falling (Good) Voltage	V_{PGDFG}	103	105	107	%	V_{FB} falling, $V_{PGDFG} = V_{FB} / V_{FBTH} \times 100$
PGD Rising (Fault) Voltage	V_{PGDRF}	108	110	112	%	V_{FB} rising, $V_{PGDRF} = V_{FB} / V_{FBTH} \times 100$
PGD Output Leakage Current	I_{LKPGD}	-	0	5	µA	V_{PGD} = 5 V, Tj = 25 °C
PGD Output Low Level Voltage	V_{PGDL}	-	0.125	0.4	V	I_{PGD} = 1 mA

(Note 3) This is design value. Not production tested.

Typical Performance Curves

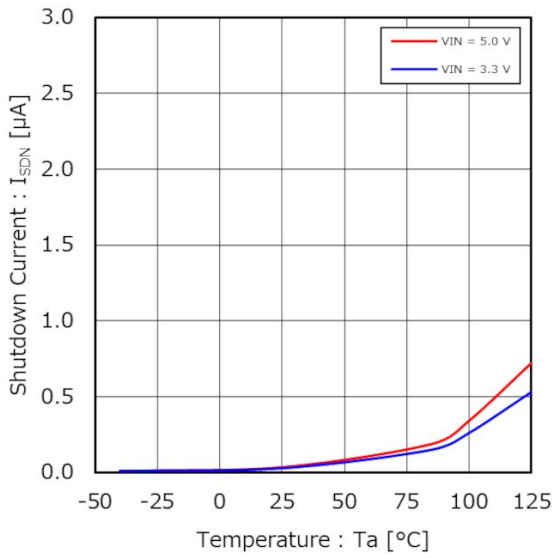


Figure 1. Shutdown Current vs Temperature

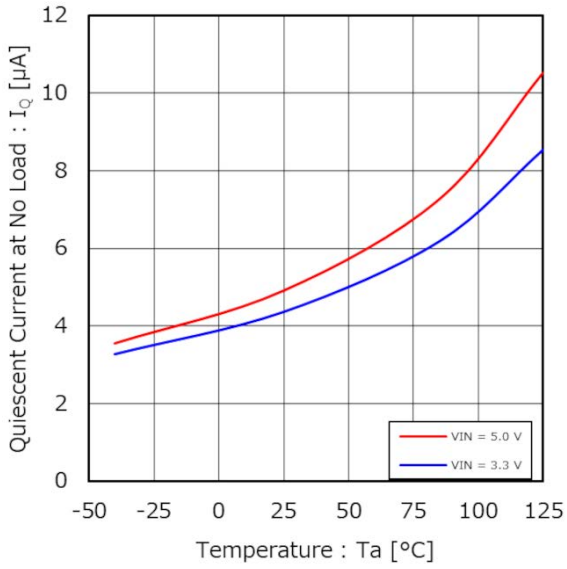


Figure 2. Quiescent Current at No Load vs Temperature

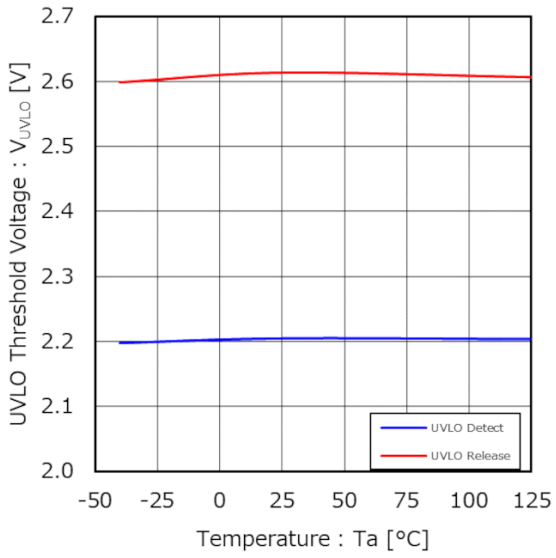


Figure 3. UVLO Threshold Voltage vs Temperature

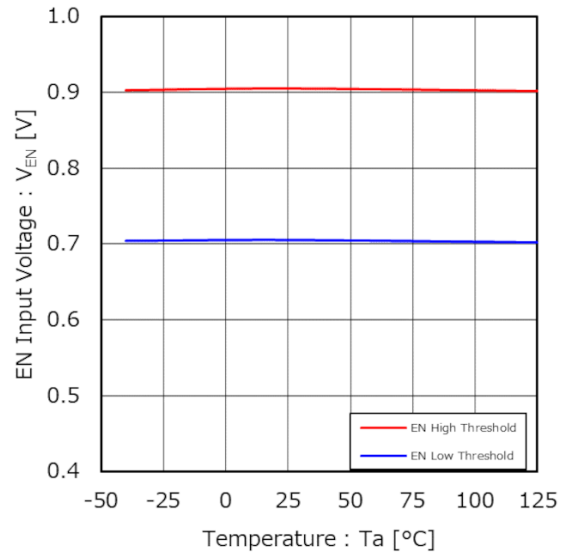


Figure 4. EN Input Voltage vs Temperature

Typical Performance Curves – continued

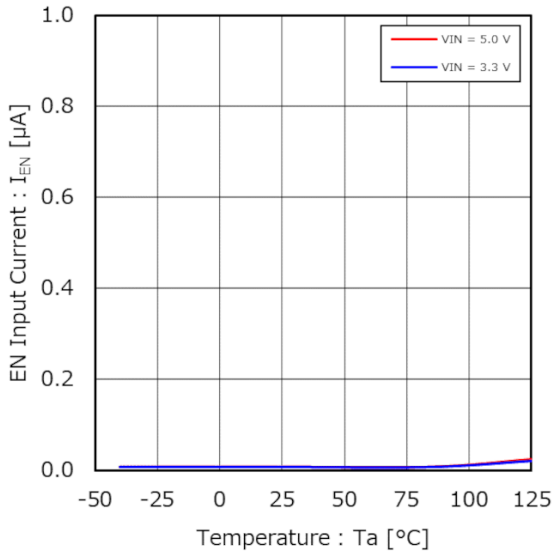


Figure 5. EN Input Current vs Temperature

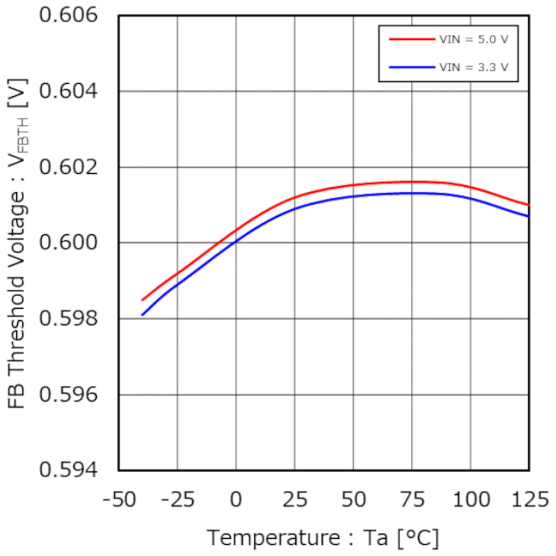


Figure 6. FB Threshold Voltage vs Temperature

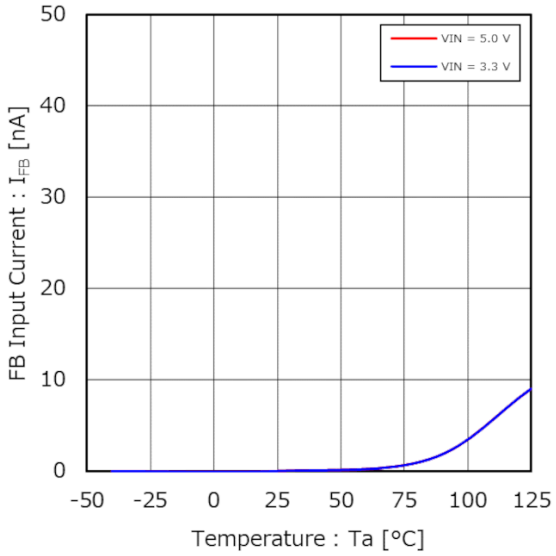


Figure 7. FB Input Current vs Temperature

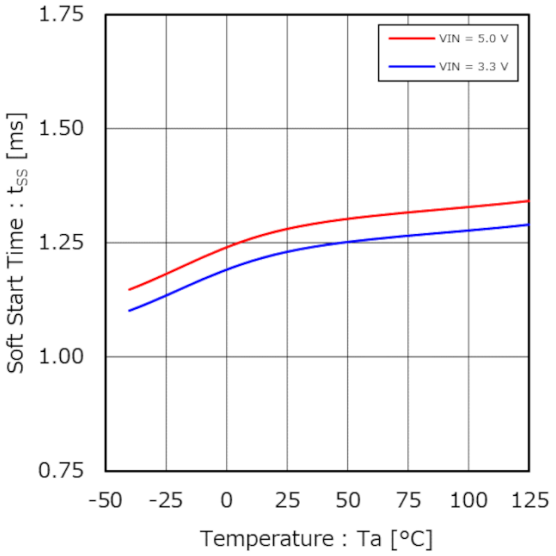


Figure 8. Soft Start Time vs Temperature

Typical Performance Curves – continued

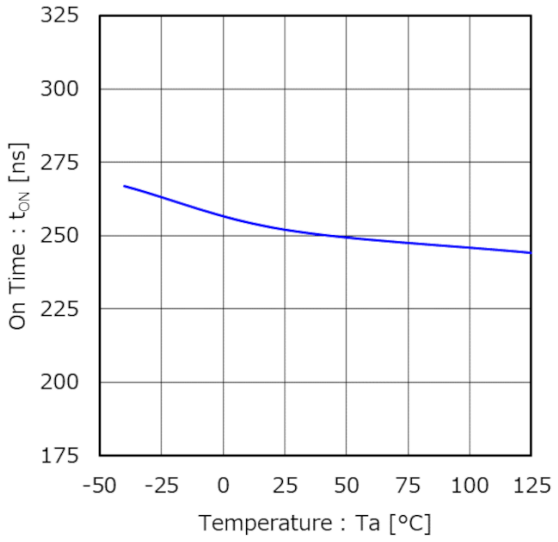


Figure 9. On Time vs Temperature
(V_{IN} = 3.3 V, V_{OUT} = 1.8 V, PWM Mode)

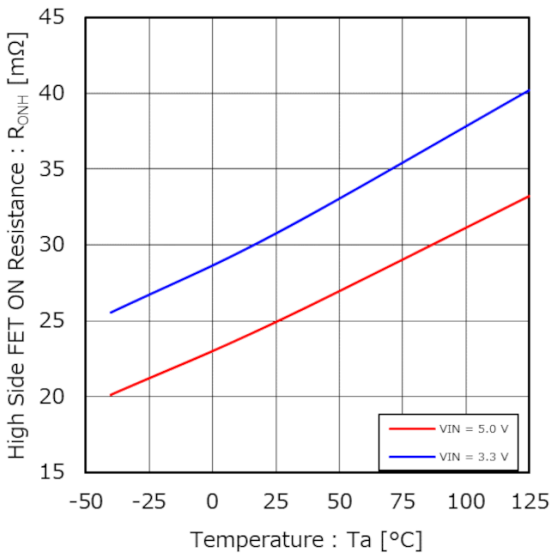


Figure 10. High Side FET ON Resistance vs Temperature

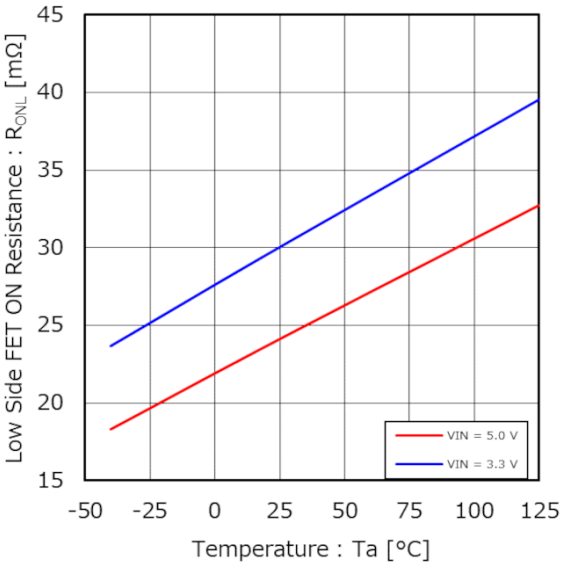


Figure 11. Low Side FET ON Resistance vs Temperature

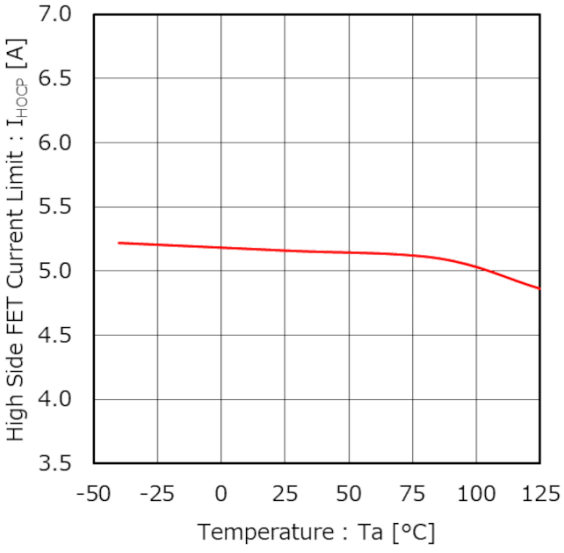


Figure 12. High Side FET Current Limit vs Temperature

Typical Performance Curves – continued

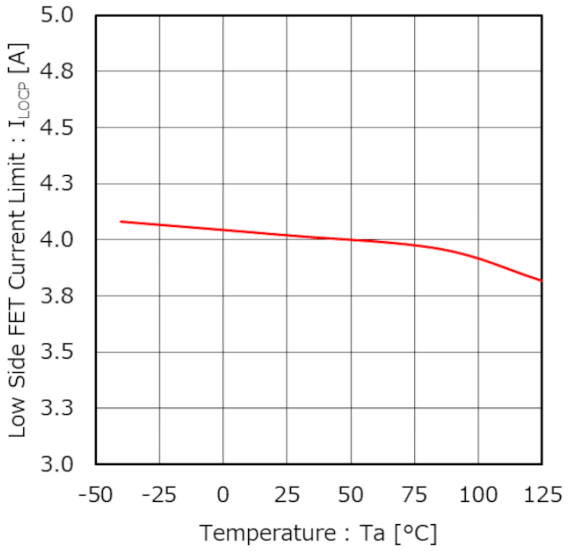


Figure 13. Low Side FET Current Limit vs Temperature

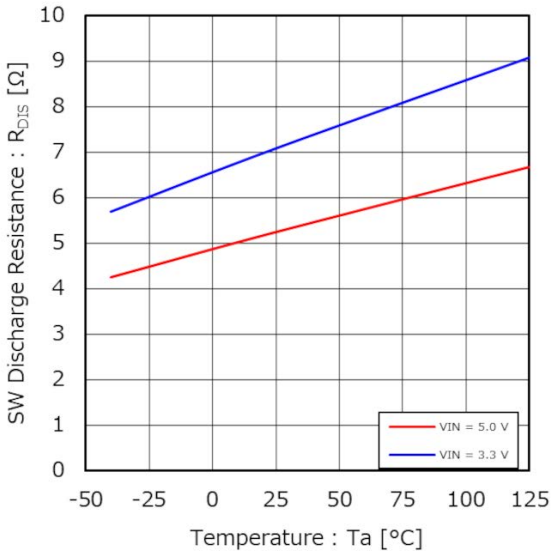


Figure 14. SW Discharge Resistance vs Temperature

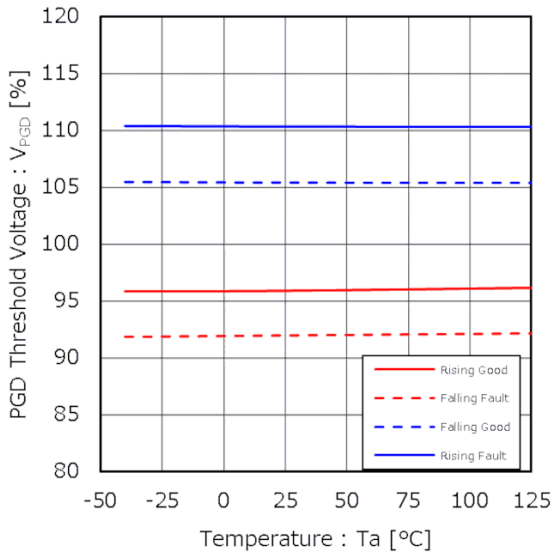


Figure 15. PGD Threshold Voltage vs Temperature

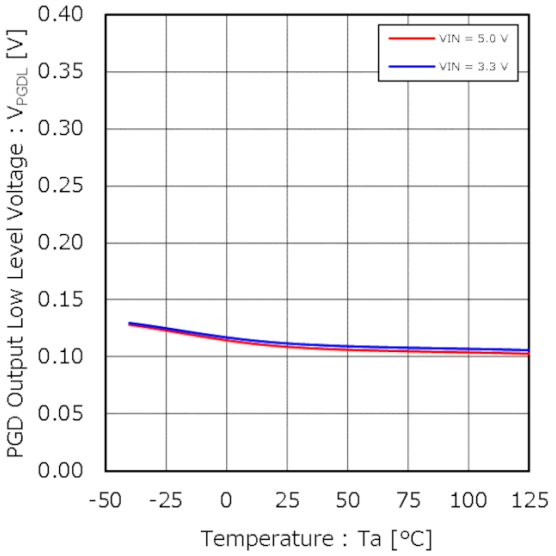


Figure 16. PGD Output Low Level Voltage vs Temperature

Function Explanations

1. Basic Operation

(1) DC/DC Converter Operation

BD9B306NF-Z is a synchronous buck DC/DC converter that achieves faster load transient response due to constant on-time control. The device performs switching operation in Pulse Width Modulation (PWM) Mode control at heavy load. It operates in Light Load Mode (LLM) control at lighter load to improve efficiency. In PWM mode, the device normally operates at a switching frequency of 2.2 MHz (Typ). At low and high duty cycles, the switching frequency is reduced as necessary to always ensure a proper regulation

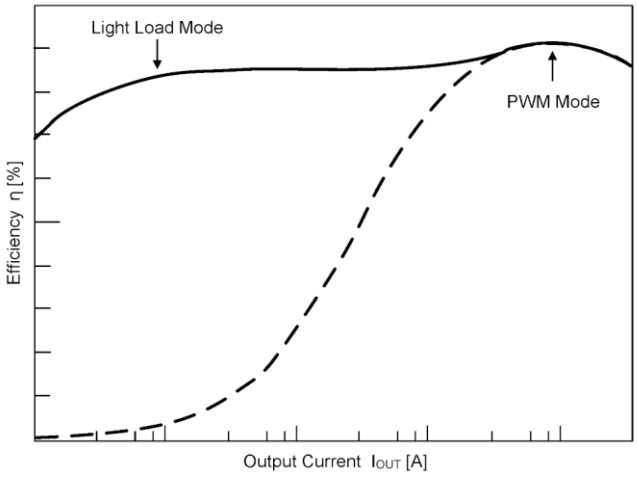


Figure 17. Efficiency Image between Light Load Mode Control and PWM Mode Control

(2) 100 % Duty Operation

The device operates in 100 % Duty mode when the input voltage V_{IN} and output voltage V_{OUT} levels are close. In this mode, the High Side FET is constantly ON and the Low Side FET is OFF. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the on resistance of the High Side FET and the DC resistance (DCR) of the inductor, as shown in the formula below.

$$V_{OUT} = V_{IN} - I_{OUT} \times (R_{ONH} + R_{DCR}) \ [\mathrm{V}]$$

where:

R_{ONH} is the High Side FET ON Resistance

R_{DCR} is the inductor DCR

1. Basic Operation - continued

(3) Enable Control

The start-up and shutdown can be controlled by the EN voltage (V_{EN}). When V_{EN} becomes 0.9 V (Typ) or more, the internal circuit is activated and the device starts up. When V_{EN} becomes 0.7 V (Typ) or less, the device is shutdown. In this shutdown mode, the High Side FET and the Low Side FET are turned off and the SW pin is connected to GND through an internal resistor 5 Ω (Typ) to discharge the output. The start-up with V_{EN} must be at the same time of the input voltage V_{IN} (V_{IN} = V_{EN}) or after supplying V_{IN}.

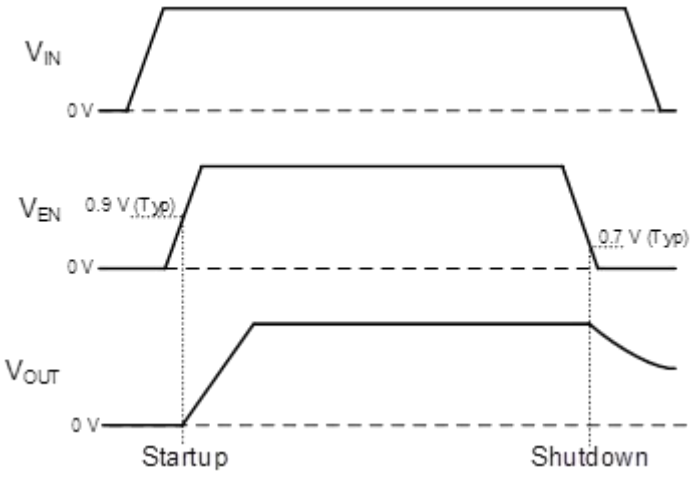


Figure 18. Start-up and Shutdown with Enable Control Timing Chart

(4) Soft Start

When V_{EN} goes high, soft start function operates and output voltage gradually rises. This soft start function can prevent overshoot of the output voltage and excessive inrush current. The soft start time t_{SS} is fixed 1.25 ms (Typ).

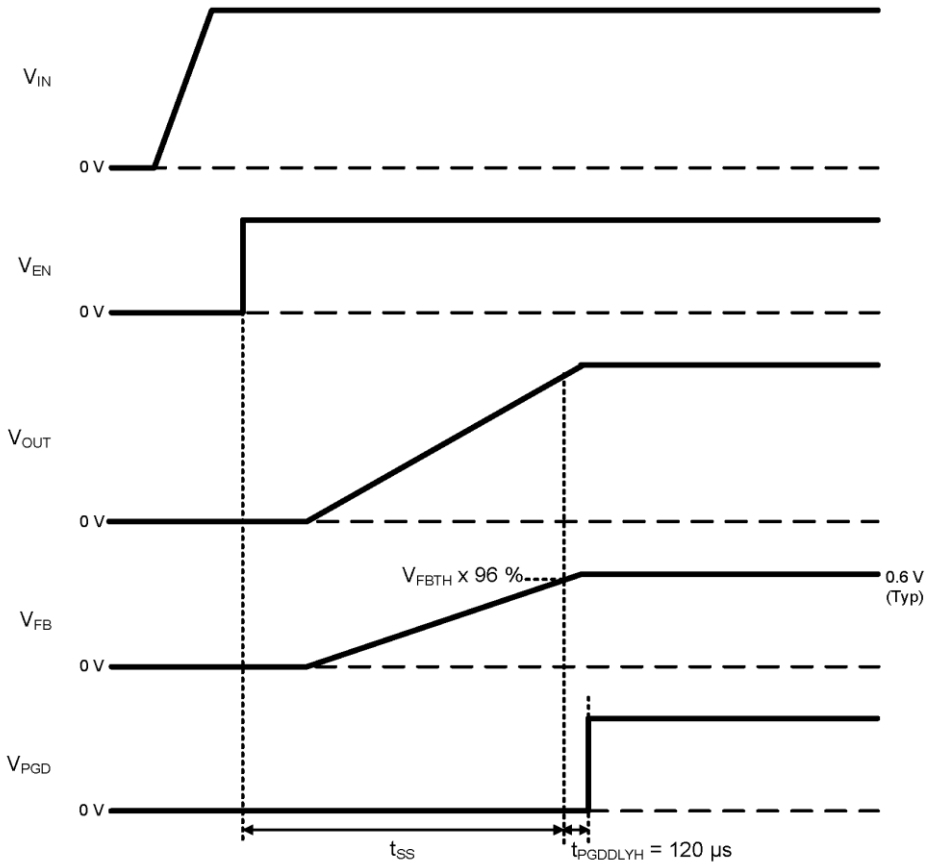


Figure 19. Soft Start Timing Chart

1. Basic Operation - continued

(5) Power Good Output

The Power Good function monitors the FB pin voltage (V_{FB}). When V_{FB} reaches 96 % (Typ) or more of the FB threshold voltage V_{FBTH} 0.6 V (Typ) and the condition continues for 120 µs (Typ), the built-in open drain Nch MOSFET connected to the PGD pin is turned off, and the PGD pin goes Hi-Z (High impedance). When V_{FB} becomes 92 % (Typ) or less of V_{FBTH} 0.6 V (Typ) and remains for 20 µs (Typ), the open drain Nch MOSFET is turned on and PGD pin is pulled down with 125 Ω (Typ).
The Power Good function also operates when the output over voltage is detected. When V_{FB} reaches 110 % (Typ) or more of the V_{FBTH} 0.6 V (Typ) and the condition continues for 120 µs (Typ), the open drain Nch MOSFET is turned on and PGD pin is pulled down with 125 Ω (Typ). When V_{FB} becomes 105 % (Typ) or less of V_{FBTH} 0.6 V (Typ) and remains for 20 µs (Typ), the built-in open drain Nch MOSFET connected to the PGD pin is turned off, and the PGD pin goes Hi-Z (High impedance).
It is recommended to connect a pull-up resistor of 10 kΩ to 100 kΩ to the the power supply less than 5.5 V. If the power good function is not used, this pin can be left floating or connected to the ground.

Table 1. PGD Output

State	Condition	PGD Output
Before Supply Input Voltage	V_{IN} < 0.7 V (Typ)	Hi-Z
Shutdown	V_{EN} ≤ 0.7 V (Typ)	Low (Pull-down)
Enable V_{EN} ≥ 0.9 V (Typ)	96 % (Typ) ≤ V_{FB} / V_{FBTH} ≤ 105 % (Typ)	Hi-Z
	V_{FB} / V_{FBTH} ≤ 92 % (Typ) or 110 % (Typ) ≤ V_{FB} / V_{FBTH}	Low (Pull-down)
UVLO	0.7 V (Typ) < V_{IN} ≤ 2.2 V (Typ)	Low (Pull-down)
TSD	Tj ≥ 175 °C (Typ)	Low (Pull-down)
SCP	Complete Soft Start V_{FB} / V_{FBTH} ≤ 92 % (Typ) OCP 256 counts	Low (Pull-down)

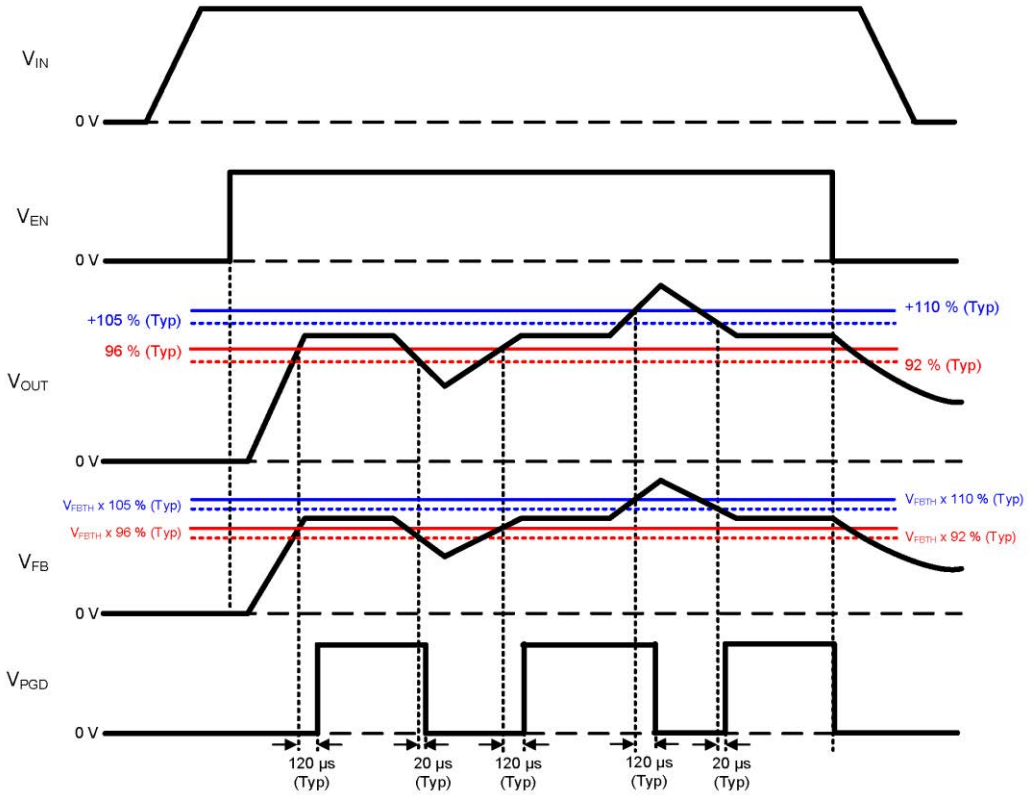


Figure 20. Power Good Timing Chart
(Connecting a pull-up resistor to the PGD pin)

1. Basic Operation - continued

(6) Output Discharge Function

When even one of the following conditions is satisfied, output is discharged with 5 Ω (Typ) resistor through the SW pin.

- Shutdown: $V_{EN} \leq 0.7$ V (Typ)
- UVLO: $V_{IN} \leq 2.2$ V (Typ)
- TSD: Tj ≥ 175 °C (Typ)
- SCP: Complete Soft Start, $V_{FB} / V_{FBTH} \leq 92$ % (Typ), and OCP 256 counts

When all of the above conditions are released, output discharge is stopped.

Function Explanations – continued

2. Protection

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Over Current Protection (OCP) restricts the flowing current through the Low Side FET and the High Side FET for every switching period. If the inductor current exceeds the Low Side FET Current Limit (I_{LOCP}) while the Low Side FET is on, the Low Side FET remains on even with FB voltage V_{FB} falls to V_{FBTH} = 0.6 V (Typ) or lower. If the inductor current becomes lower than I_{LOCP}, the High Side FET is able to be turned on. When the inductor current becomes the High Side Current Limit (I_{HOCP}) while the High Side FET is on, the High Side FET is turned off. Output voltage may decrease by changing frequency and duty due to the OCP operation.

Short Circuit Protection (SCP) function is a Hiccup mode. When Low Side OCP or High Side OCP operates 256 cycles while V_{FB} is V_{FBTH} x 92 % or less (V_{PGD} = Low), the device stops the switching operation for 130 ms (Typ). After the 130 ms (Typ), the device restarts. SCP does not operate during the soft start even if the device is in the SCP conditions. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

Table 2. The Operating Condition of OCP and SCP

V_{EN}	V_{FB}	Start-up	OCP	SCP
≥ 0.9 V (Typ)	≤ V_{FBTH} x 92 % (Typ)	During Soft Start	Enable	Disable
	> V_{FBTH} x 92 % (Typ)	Complete Soft Start	Enable	Disable
	≤ V_{FBTH} x 92 % (Typ)		Enable	Enable
≤ 0.7 V (Typ)	-	Shutdown	Disable	Disable

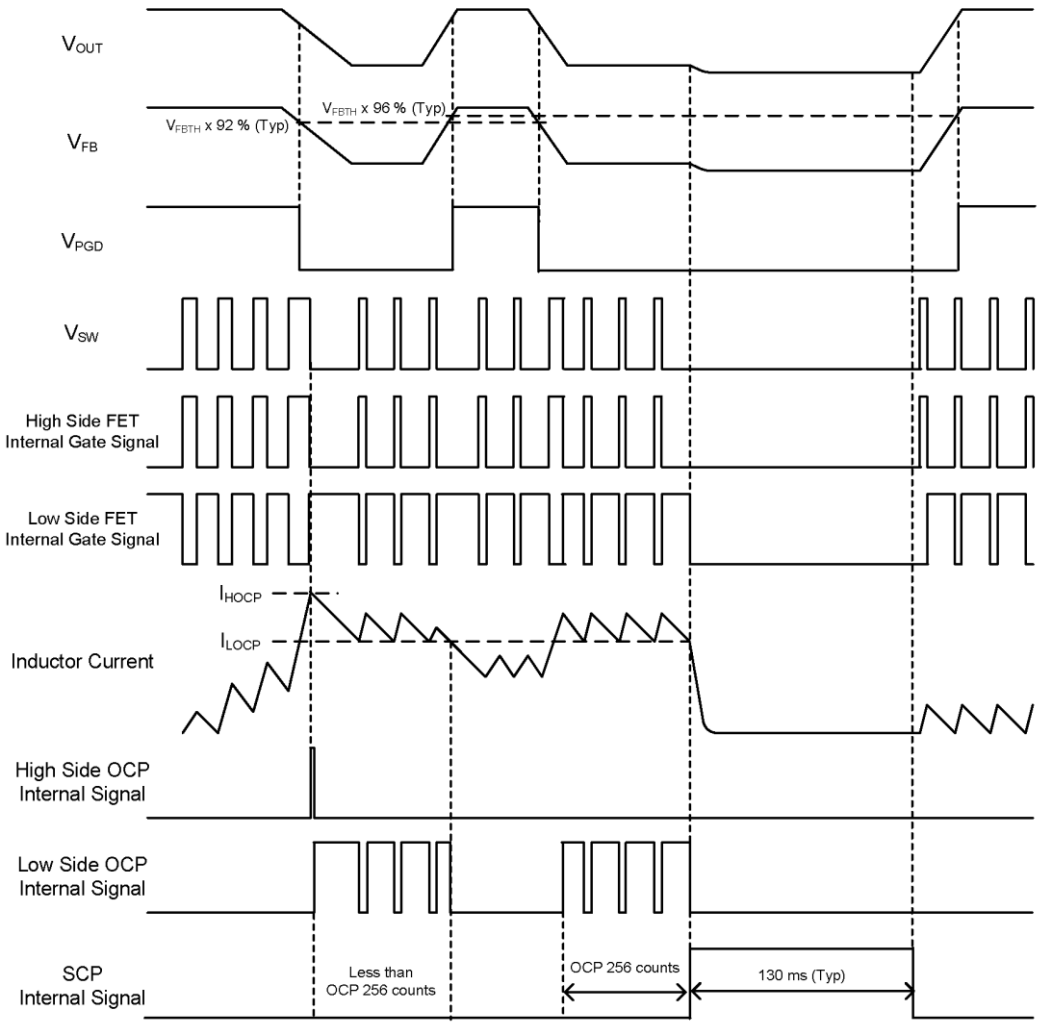


Figure 21. OCP and SCP Timing Chart

2. Protection - continued

(2) Under Voltage Lockout Protection (UVLO)

When input voltage V_{IN} falls to 2.2 V (Typ) or lower, the device is shutdown. When V_{IN} becomes 2.6 V (Typ) or more, the device starts up. The hysteresis is 400 mV (Typ).

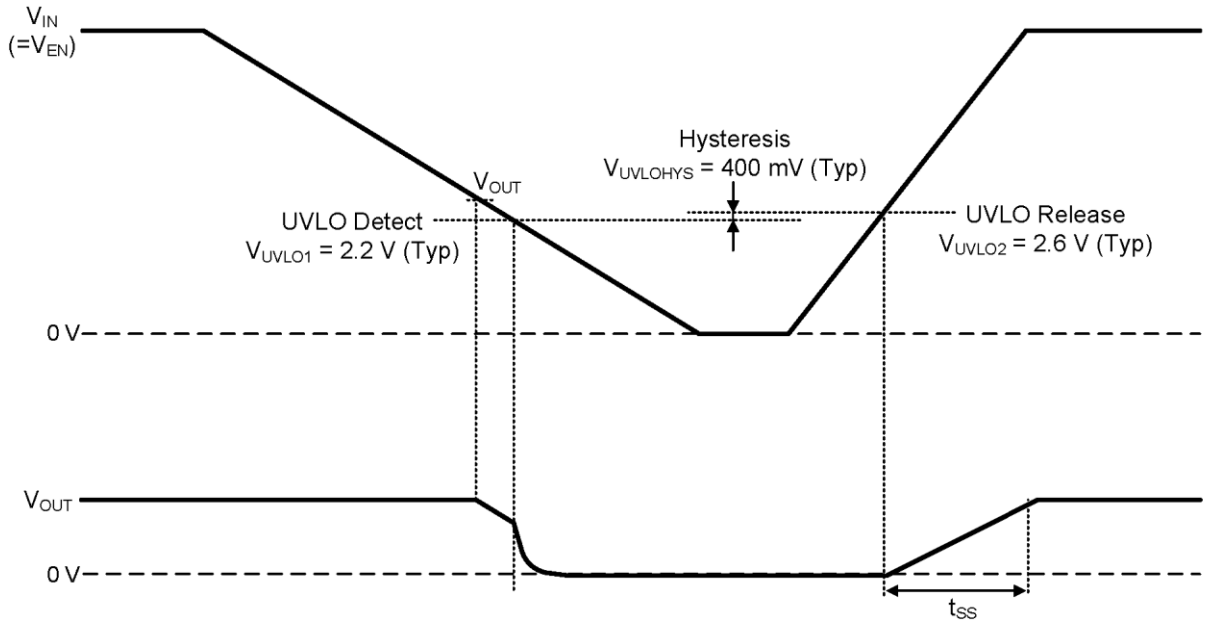


Figure 22. UVLO Timing Chart

(3) Thermal Shutdown Protection (TSD)

Thermal shutdown circuit prevents heat damage to the IC. The device should always operate within the IC's maximum junction temperature rating. However, if it continues exceeding the rating and the junction temperature Tj rises to 175 °C (Typ), the TSD circuit is activated and it turns the output MOSFETs off. When the Tj falls below the TSD threshold, the device is automatically restored to normal operation. The TSD threshold has a hysteresis of 25 °C (Typ). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

(4) Over Voltage Protection (OVP)

When the FB voltage V_{FB} exceeds V_{FBTH} x 110 % (Typ) or more, the output MOSFETs are turned off to prevent the increase in the output voltage. After the V_{FB} falls V_{FBTH} x 105 % (Typ) or less, the output MOSFETs are returned to normal operation condition. Switching operation will restart after V_{FB} falls below V_{FBTH}.

Application Examples

1. Typical Application

For the power supply design, the necessary parameters are as follows.

Table 3. Example of Application Specification

Parameter	Symbol	**Example Value**
Input Voltage	V_{IN}	5.0 V (Typ)
Output Voltage	V_{OUT}	1.8 V (Typ)
Maximum Output Current	I_{OUTMAX}	3.0 A

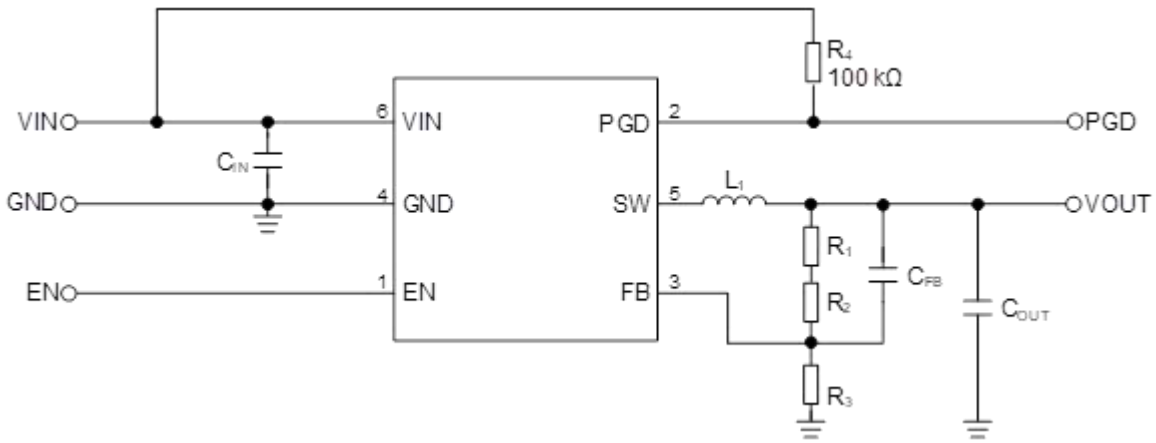


Figure 23. Application Circuit

2. Input Capacitor

Use ceramic type capacitor for the input capacitor C_{IN}. The input capacitor is used to reduce the input ripple noise and it is effective by being placed as close as possible to the VIN pin. Set the capacitor value so that it does not fall to 2.5 µF considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. Use the capacitor which has the comparatively same characteristics with the components (C_1) in "Application Characteristic Data (Reference Data)". Input ripple noise can be further reduced by using an input capacitor with a larger capacitance value. In addition, high frequency noise may be reduced by placing an additional capacitor of 0.1 µF or less as close as possible to the VIN and GND pins. The PCB layout and the position of the capacitor may lead to IC malfunction. Refer to "PCB Layout Design".

Application Examples - continued

3. Output Voltage Setting

The output voltage can be set by the feedback resistance ratio connected to the FB pin. By connecting R_1 and R_2 resistors in series as the upper resistor R_{UP} ($R_{UP} = R_1 + R_2$), the output voltage value can be finely adjusted. For stable operation, the parallel resistance of feedback resistors R_{UP} and R_{DW} should be set to 20 kΩ or more.

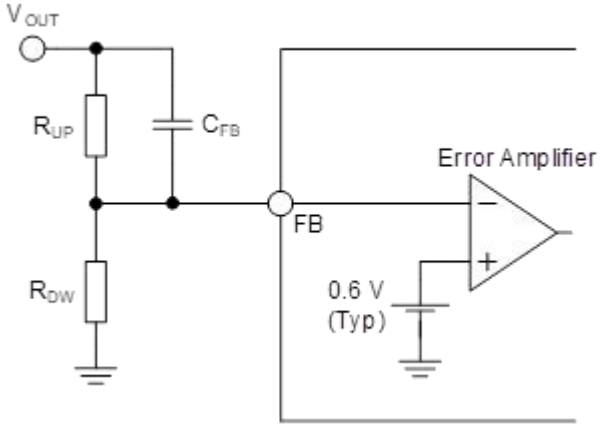


Figure 24. Feedback Resistor Circuit

The output voltage V_{OUT} can be calculated as

$$V_{OUT} = \frac{R_{UP}+R_{DW}}{R_{DW}} \times 0.6 \ [\mathrm{V}]$$

$$R_{UP} = R_1 + R_2$$
$$R_{DW} = R_3$$

$$1/(\frac{1}{R_{UP}} + \frac{1}{R_{DW}}) \geq 20 \ [\mathrm{k\Omega}]$$

The Constant On-time Control required the sufficient ripple voltage on FB voltage for the operation stability. This device is designed to correspond to low ESR output capacitors without a feedforward capacitor C_{FB} by injecting the ripple voltage to FB voltage inside the IC. However, it is recommended to connect C_{FB} in order to improve the load transient response and operating stability. The FB capacitor C_{FB} should be set within the range.

$$Open < C_{FB} < \frac{15\times(1-V_{OUT}/V_{IN})\times\sqrt{L_1 C_{OUT}}}{R_{UP}} \ [\mathrm{F}]$$

Load transient response and the loop stability depends on L_1, C_{OUT}, R_{UP}, R_{DW}, and C_{FB}. Actually, these characteristics may change depending on PCB layout, wiring, the type of components, and the conditions (temperature, etc.). Be sure to check them on the actual application.

Refer to Table 4 as recommended values for each output voltage setting.

Table 4. Recommended Feedback Resistances and C_{FB} Capacitance

入力電圧	出力電圧	R_{UP}		R_{DW}	C_{FB}
V_{IN}	V_{OUT}	R_1	R_2	R_3	C_7
5.0 V	0.6 V	100 kΩ	0 Ω	Open	120 pF
5.0 V	0.9 V	100 kΩ	0 Ω	200 kΩ	120 pF
5.0 V	1.0 V	100 kΩ	0 Ω	150 kΩ	120 pF
5.0 V	1.2 V	150 kΩ	0 Ω	150 kΩ	120 pF
5.0 V	1.5 V	150 kΩ	0 Ω	100 kΩ	120 pF
5.0 V	1.8 V	200 kΩ	0 Ω	100 kΩ	120 pF
5.0 V	2.5 V	270 kΩ	47 kΩ	100 kΩ	47 pF
5.0 V	3.3 V	200 kΩ	12 kΩ	47 kΩ	33 pF
3.3 V	0.6 V	100 kΩ	0 Ω	Open	120 pF
3.3 V	0.9 V	100 kΩ	0 Ω	200 kΩ	120 pF
3.3 V	1.0 V	100 kΩ	0 Ω	150 kΩ	120 pF
3.3 V	1.2 V	150 kΩ	0 Ω	150 kΩ	120 pF
3.3 V	1.5 V	150 kΩ	0 Ω	100 kΩ	120 pF
3.3 V	1.8 V	200 kΩ	0 Ω	100 kΩ	68 pF

Application Examples - continued

4. Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. Use the inductance value of 0.47 µH.

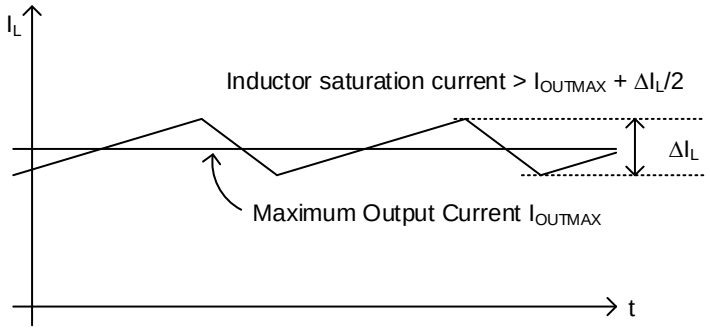


Figure 25. Waveform of Inductor Current

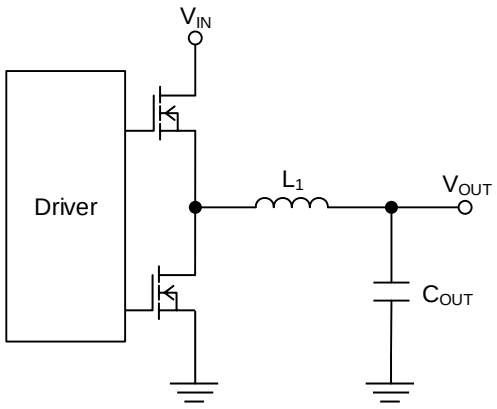


Figure 26. Output LC Filter Circuit

For example, given that V_{IN} = 5 V, V_{OUT} = 1.8 V, L_1 = 0.47 µH, and the switching frequency f_{SW} = 2.2 MHz, Inductor current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 1.11 \text{ [A]}$$

The rated current of the inductor (Inductor saturation current) must be larger than the sum of the maximum output current I_{OUTMAX} and 1/2 of the inductor ripple current ΔI_L. Table 5 is the list of recommended inductors.

Table 5. Recommended Inductors

Inductance [µH]	Part Name	Manufacturer	DCR [mΩ]	Current Rating [A]	L x W x H [mm]
0.47	DFE252012F-R47M	Murata	23	6.7	2.5 x 2.0 x 1.2
	DFE201610E-R47M	Murata	32	4.8	2.0 x 1.6 x 1.0
	LBENA2520MKTR47M0NK	TAIYO YUDEN	20	5.9	2.5 x 2.0 x 1.2
	LSEUC2016KKTR47M	TAIYO YUDEN	26	6.3	2.0 x 1.6 x 1.0
	TFM201610ALM-R47MTAA	TDK	34	5.1	2.0 x 1.6 x 1.0
	XGL4015-471ME	Coilcraft	7.5	10.5	4.0 x 4.0 x 1.5
	XFL4015-471ME	Coilcraft	8.36	6.6	4.0 x 4.0 x 1.6
	XEL3520-471ME	Coilcraft	10.85	8.0	3.5 x 3.2 x 2.0

4. Output LC Filter - continued

Use ceramic type capacitor for the output capacitor C_{OUT}. C_{OUT} affects the output ripple voltage. Select C_{OUT} so that it must satisfy the required ripple voltage characteristics.
The output ripple voltage can be estimated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \quad [\mathrm{V}]$$

where:

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

For example, given that C_{OUT} = 10 x 2 µF and R_{ESR} = 3 mΩ, ΔV_{RPL} can be calculated as below.

$$\Delta V_{RPL} = 1.11\,A \times \left(3\,m\Omega + \frac{1}{8 \times 10 \times 2\,\mu F \times 2.2\,MHz} \right) = 6.5\,[\mathrm{mV}]$$

The C_{OUT} capacitance of 20 µF (Typ) is recommended. Set the capacitor value so that it does not fall to 10 µF considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. Use the capacitor which has the comparatively same characteristics with the components (C_3, C_4, C_6) in "Application Characteristic Data (Reference Data)".

In addition, the total capacitance connected to V_{OUT} needs to satisfy the value obtained by the following equation.

$$C_{OUTMAX} < \frac{0.5\,m}{V_{OUT}} \times \left(1 - \frac{\Delta I_L}{2} \right) \quad [\mathrm{F}]$$

For example, given that V_{IN} = 5 V, V_{OUT} = 1.8 V, L_1 = 0.47 µH, f_{SW} = 2.2 MHz (Typ), C_{OUTMAX} can be calculated as below.

$$C_{OUTMAX} < \frac{0.5\,m}{1.8\,V} \times \left(1 - \frac{1.11\,A}{2} \right) = 123 \quad [\mu\mathrm{F}]$$

If the total capacitance connected to V_{OUT} is larger than C_{OUTMAX}, over current protection may be activated by the inrush current at start-up and prevented to turn on the output. Confirm this on the actual application.

Application Characteristic Data (Reference Data)

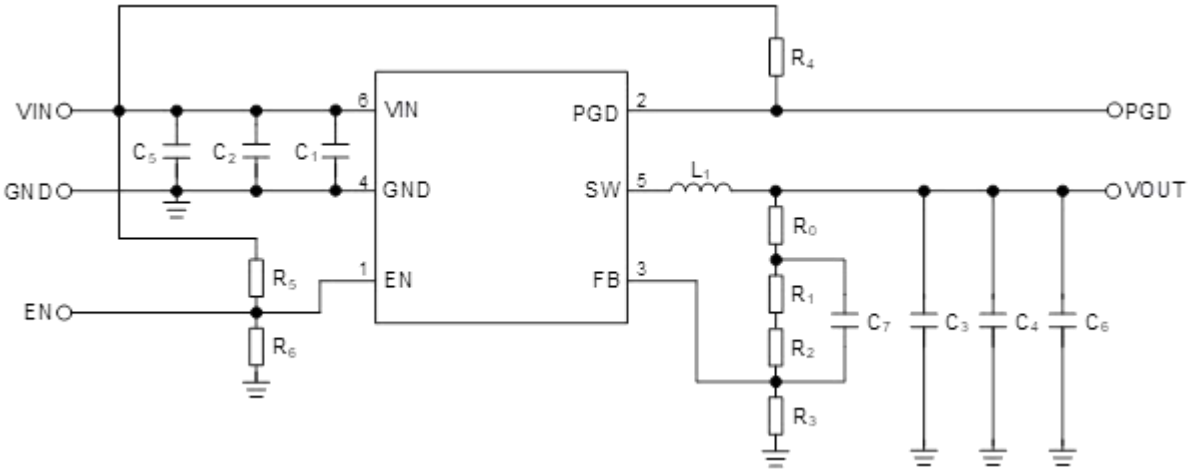


Figure 27. Application Measurement Schematic

Table 6. List of Components (Reference Example)

Part No.	Value	Part Name	Type	Size Code (mm)	Manufacturer
L_1	0.47 µH	XGL4015-471ME	Inductor	4040	Coilcraft
C_1	4.7 µF (6.3V, X7R)	JMK107BB7475MA	Ceramic Capacitor	1608	TAIYO YUDEN
C_2	-	-	-	-	-
C_3	10 µF (10 V, X7R)	GRM188Z71A106MA73	Ceramic Capacitor	1608	Murata
C_4	10 µF (10 V, X7R)	GRM188Z71A106MA73	Ceramic Capacitor	1608	Murata
C_5 *(Note 1)*	-	-	-	-	-
C_6	-	-	-	-	-
C_7	Depending on V_{OUT} *(Note 2)*	GRM1555C2A Series	Ceramic Capacitor	1005	Murata
R_1	Depending on V_{OUT} *(Note 2)* (1 %, 1/16 W)	MCR01MZPF Series	Chip Resistor	1005	ROHM
R_2	Depending on V_{OUT} *(Note 2)* (1 %, 1/16 W)	MCR01MZPF Series	Chip Resistor	1005	ROHM
R_3	Depending on V_{OUT} *(Note 2)* (1 %, 1/16 W)	MCR01MZPF Series	Chip Resistor	1005	ROHM
R_4	100 kΩ (1 %, 1/16 W)	MCR01MZPF1003	Chip Resistor	1005	ROHM
R_5	-	-	-	-	-
R_6	-	-	-	-	-
R_0 *(Note 3)*	Short	-	-	-	-

(Note 1) C_5 is for an additional input capacitor option. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple.
(Note 2) For the part value of output voltage setting, see "Table 4. Recommended feedback resistances, C_{FB} capacitance".
(Note 3) R_0 is an option, used for feedback's frequency characteristics measurement. By inserting a resistor at R_0, it is possible to measure the frequency characteristics (phase margin) using a FRA. However, the resistor will not be used in actual application, use this resistor pattern in short-circuit mode.

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

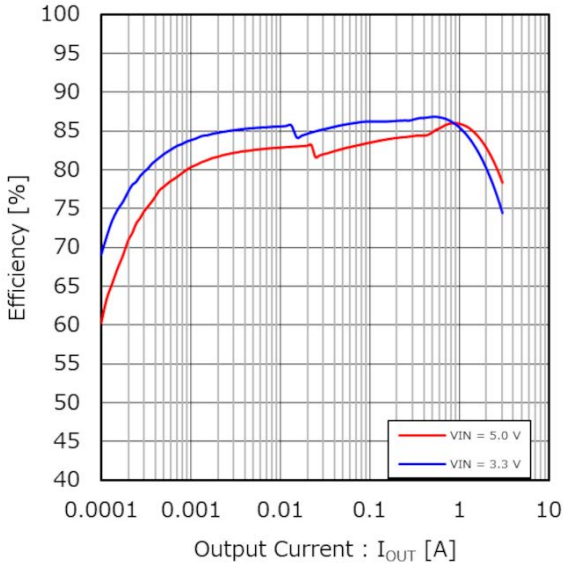


Figure 28. Efficiency vs Output Current
(V_{OUT} = 0.6 V)

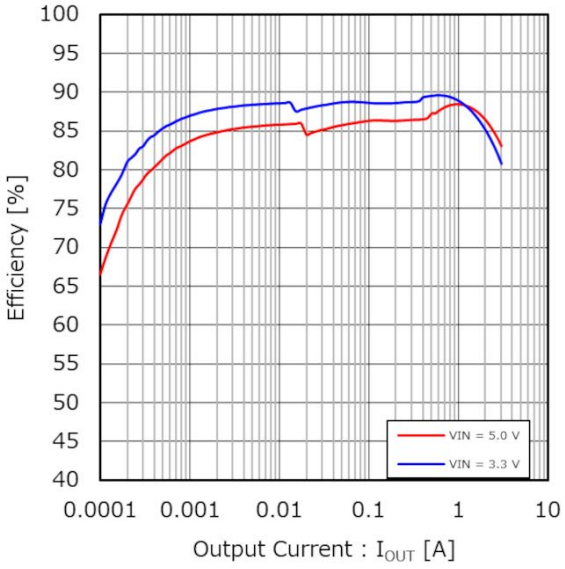


Figure 29. Efficiency vs Output Current
(V_{OUT} = 0.9 V)

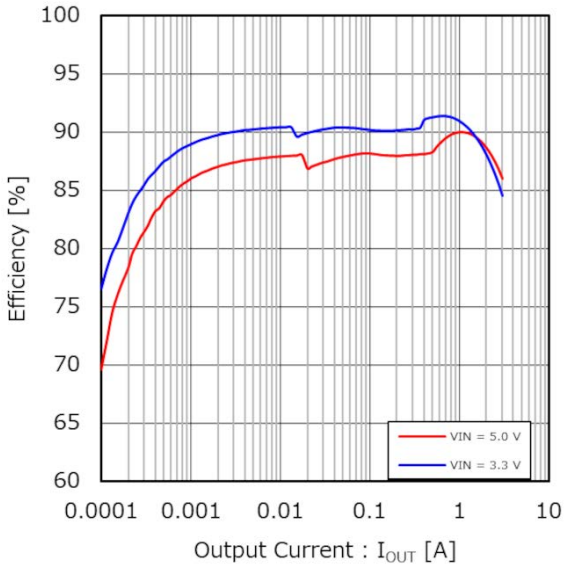


Figure 30. Efficiency vs Output Current
(V_{OUT} = 1.2 V)

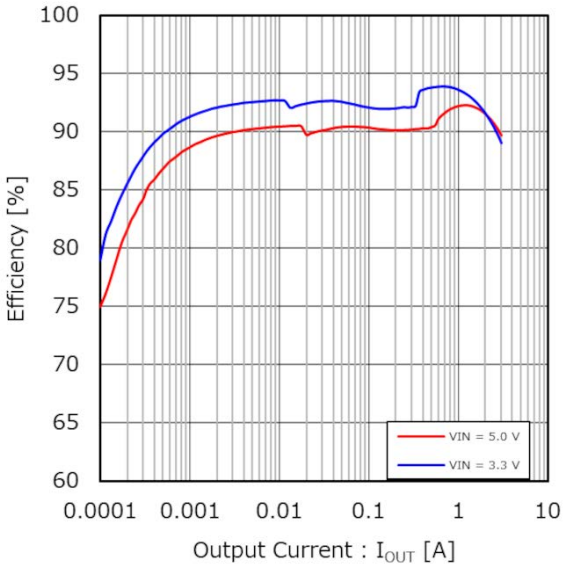


Figure 31. Efficiency vs Output Current
(V_{OUT} = 1.8 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

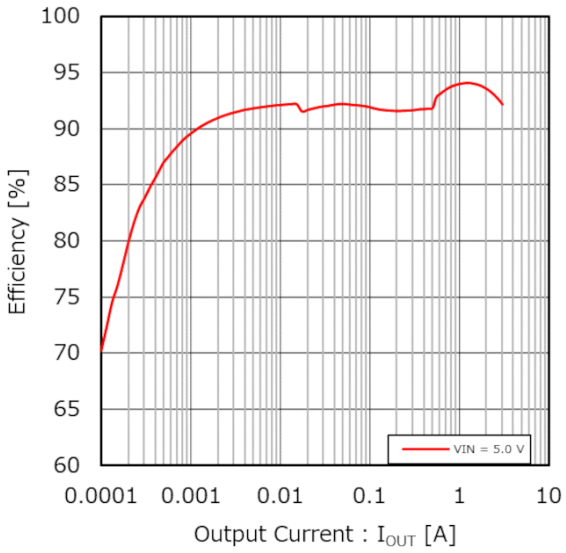


Figure 32. Efficiency vs Output Current
(V_{OUT} = 2.5 V)

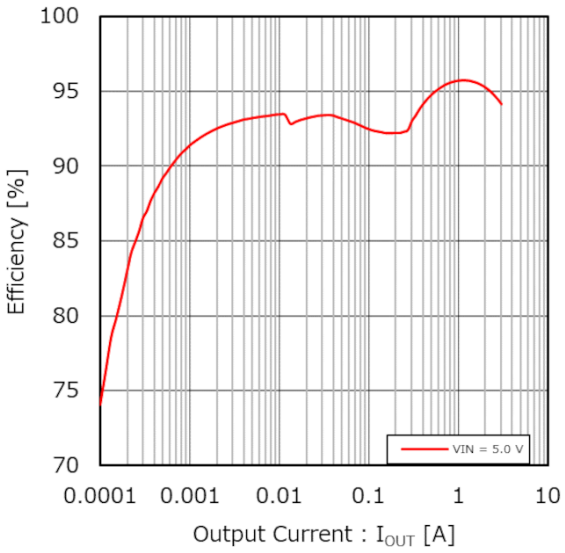


Figure 33. Efficiency vs Output Current
(V_{OUT} = 3.3 V)

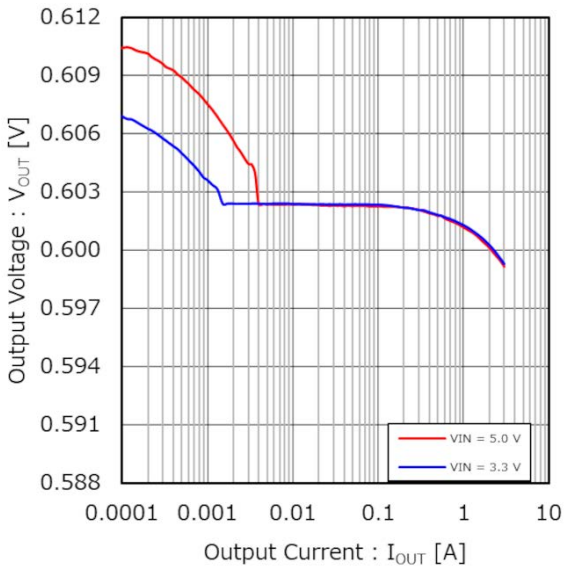


Figure 34. Output Voltage vs Output Current
(Load Regulation)
(V_{OUT} = 0.6 V)

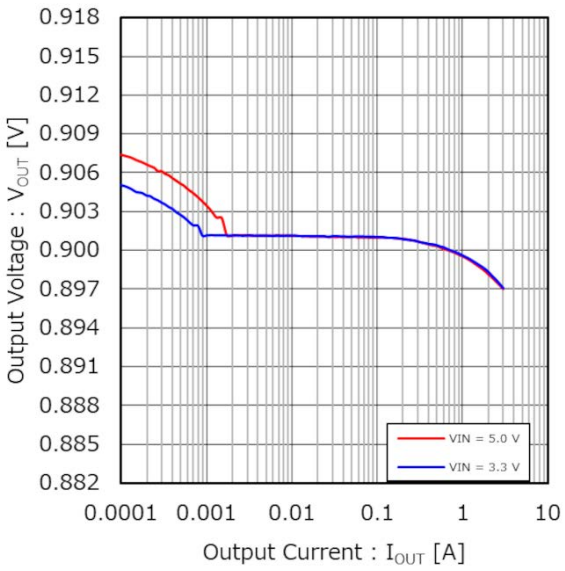


Figure 35. Output Voltage vs Output Current
(Load Regulation)
(V_{OUT} = 0.9 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

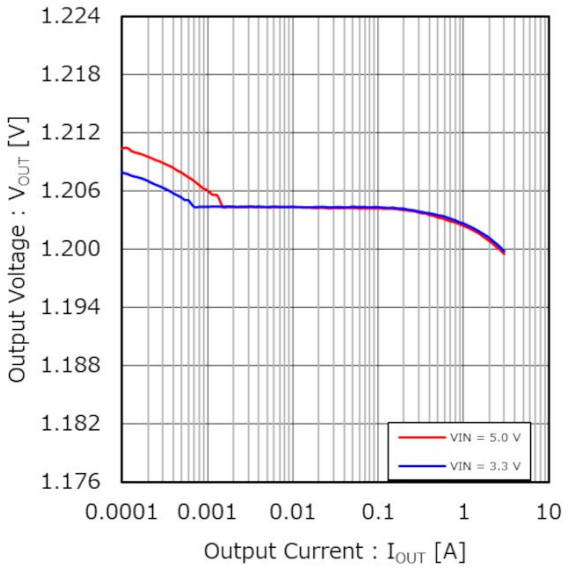


Figure 36. Output Voltage vs Output Current (Load Regulation) (V_{OUT} = 1.2 V)

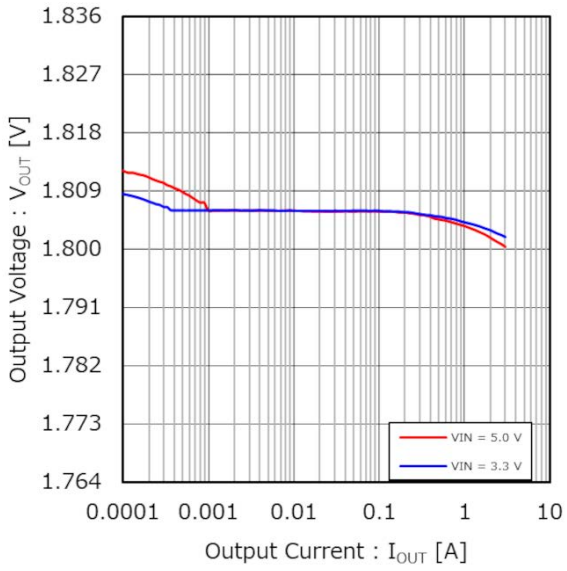


Figure 37. Output Voltage vs Output Current (Load Regulation) (V_{OUT} = 1.8 V)

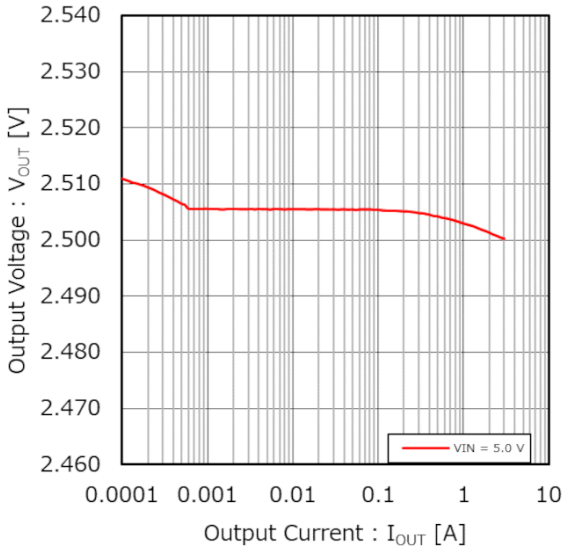


Figure 38. Output Voltage vs Output Current (Load Regulation) (V_{OUT} = 2.5 V)

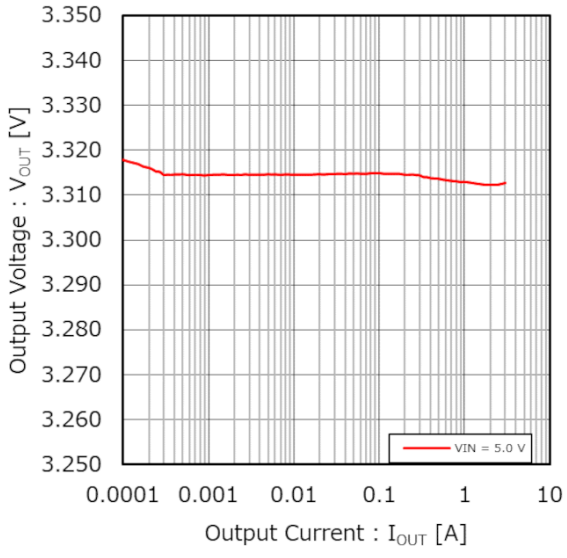


Figure 39. Output Voltage vs Output Current (Load Regulation) (V_{OUT} = 3.3 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

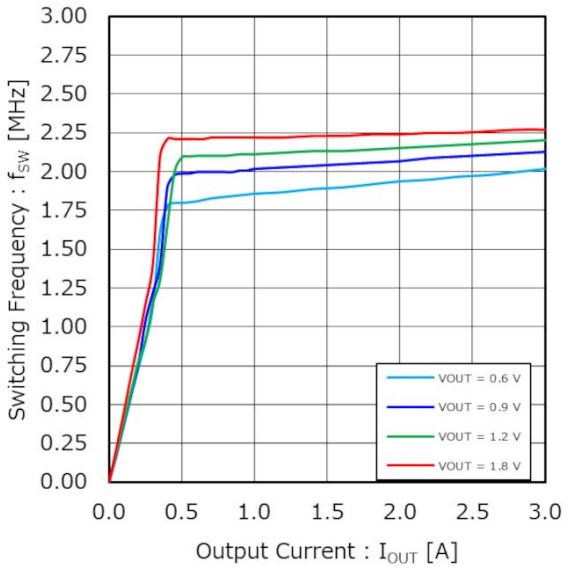


Figure 40. Switching Frequency vs Output Current
(V_{IN} = 3.3 V)

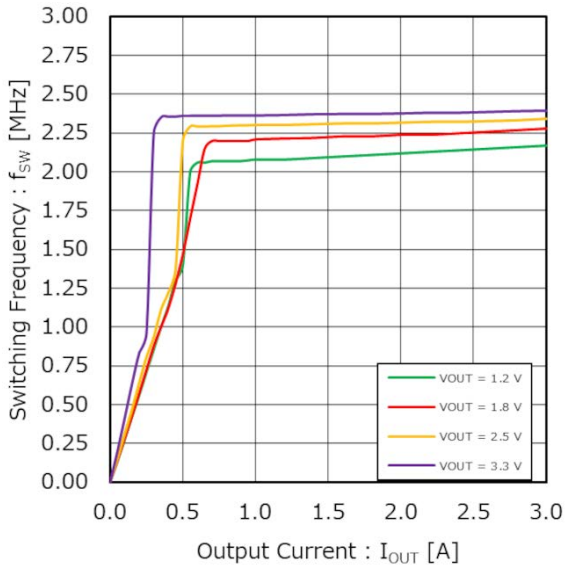


Figure 41. Switching Frequency vs Output Current
(V_{IN} = 5.0 V)

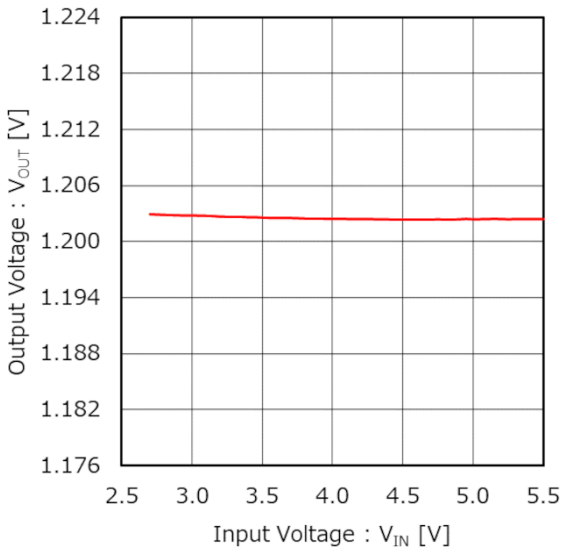


Figure 42. Output Voltage vs Input Voltage
(Line Regulation)
(V_{OUT} = 1.2 V, I_{OUT} = 1.0 A)

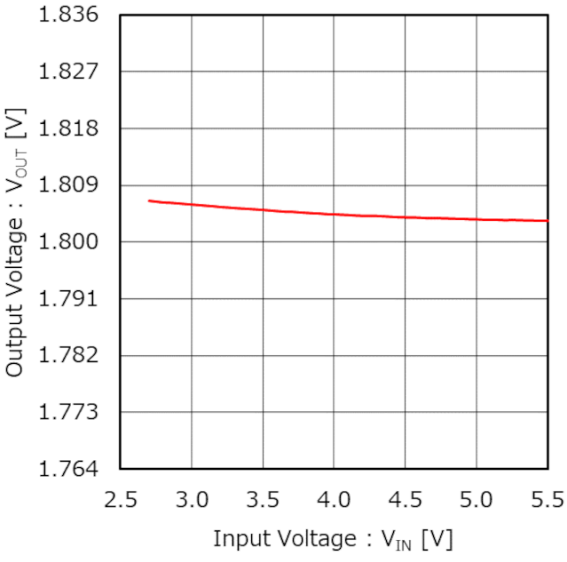


Figure 43. Output Voltage vs Input Voltage
(Line Regulation)
(V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

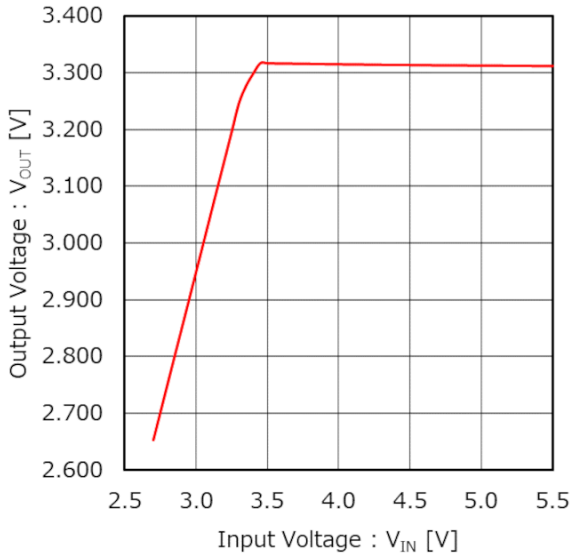


Figure 44. Output Voltage vs Input Voltage (Line Regulation)
(V_{OUT} = 3.3 V, I_{OUT} = 1.0 A)

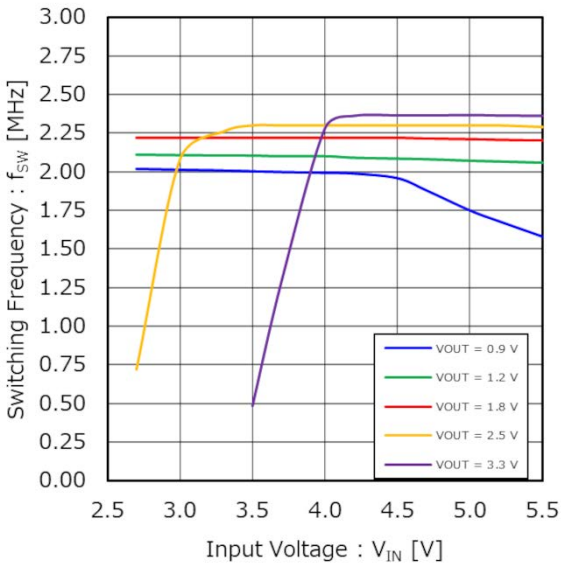


Figure 45. Switching Frequency vs Input Voltage
(I_{OUT} = 1.0 A)

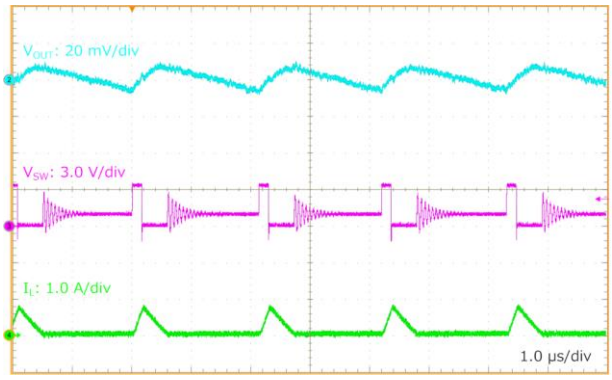


Figure 46. Output Ripple Voltage
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V, I_{OUT} = 0.1 A)

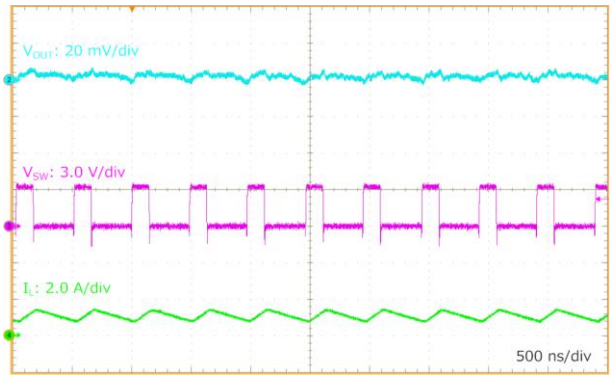


Figure 47. Output Ripple Voltage
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V, I_{OUT} = 1.0 A)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

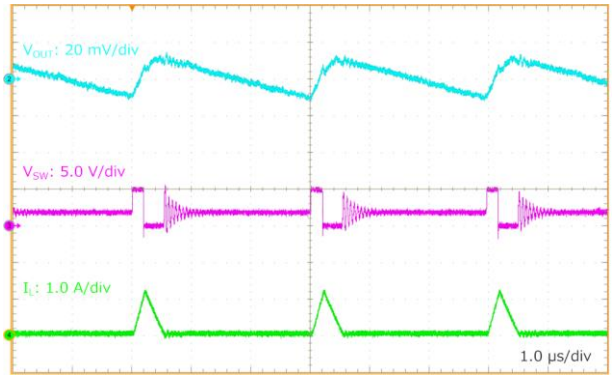


Figure 48. Output Ripple Voltage
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 0.1 A)

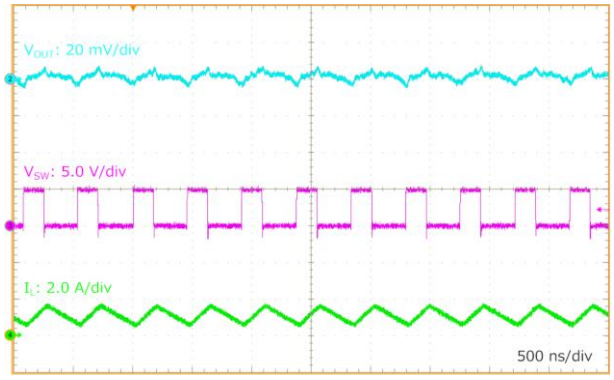


Figure 49. Output Ripple Voltage
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

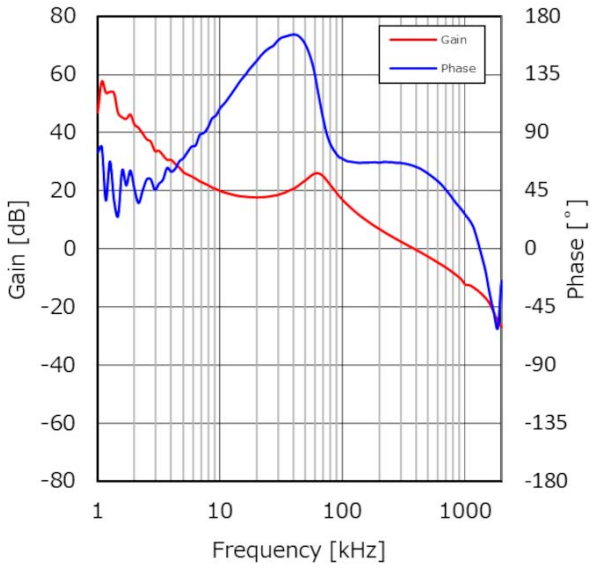


Figure 50. Frequency Characteristics
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V, I_{OUT} = 1.0 A)

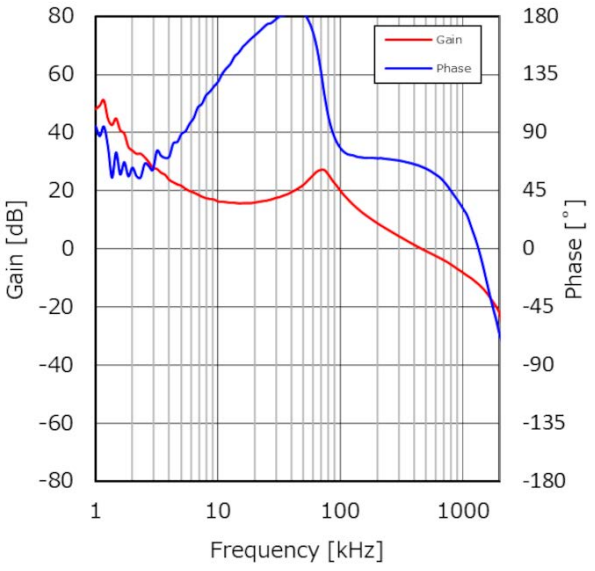


Figure 51. Frequency Characteristics
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

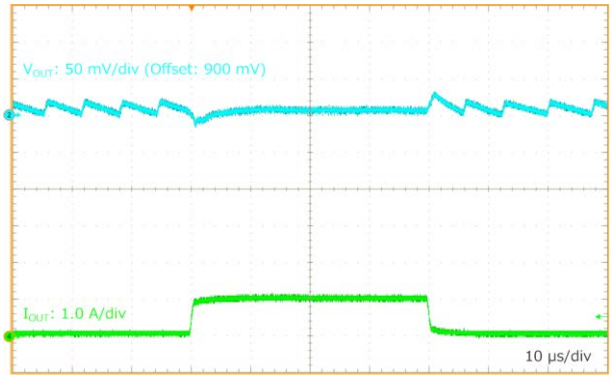


Figure 52. Load Transient Response
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V, I_{OUT} = 0.05 A to 1.0 A: 1 A/µs)

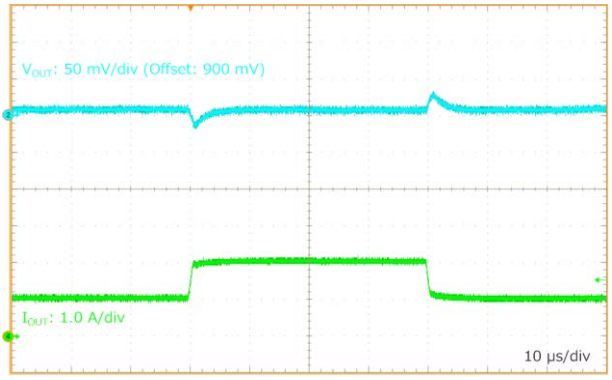


Figure 53. Load Transient Response
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V, I_{OUT} = 1.0 A to 2.0 A: 1 A/µs)

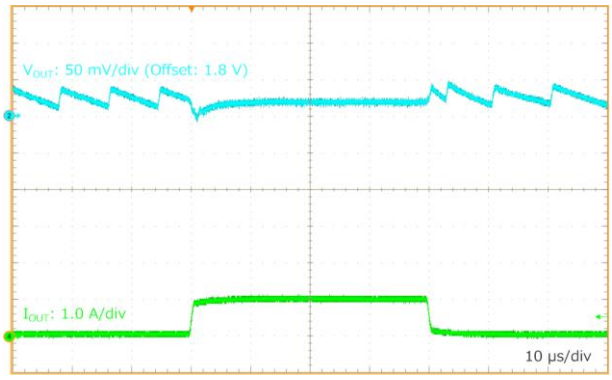


Figure 54. Load Transient Response
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 0.05 A to 1.0 A: 1 A/µs)

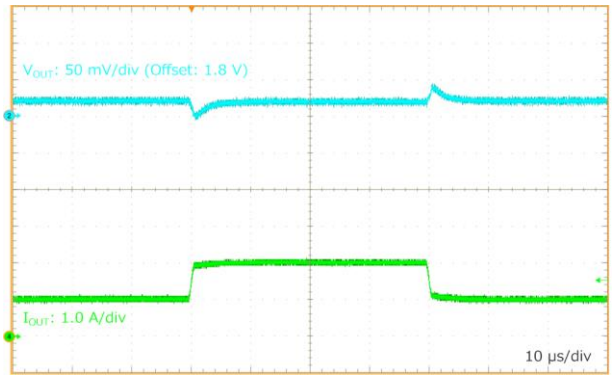


Figure 55. Load Transient Response
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, I_{OUT} = 1.0 A to 2.0 A: 1 A/µs)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

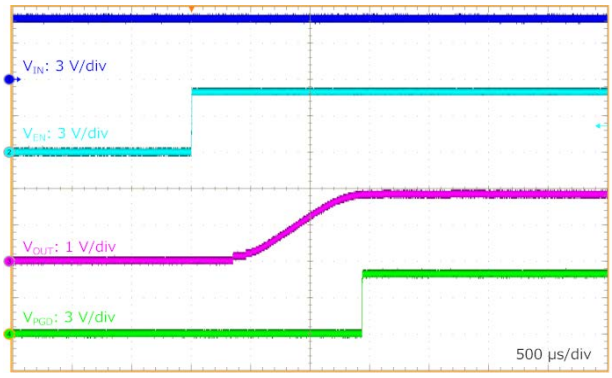


Figure 56. EN Start-up at No Load
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, V_{EN} = 0 V to 5 V)

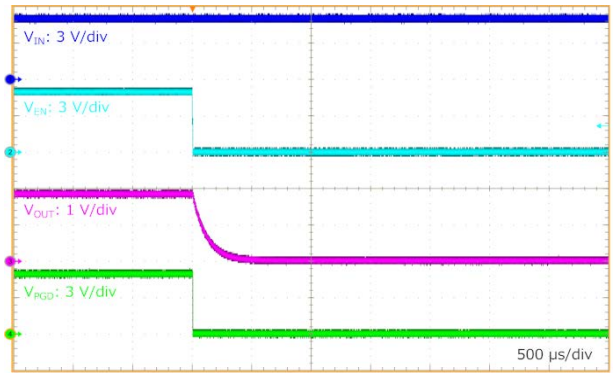


Figure 57. EN Shutdown at No Load
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, V_{EN} = 5 V to 0 V)

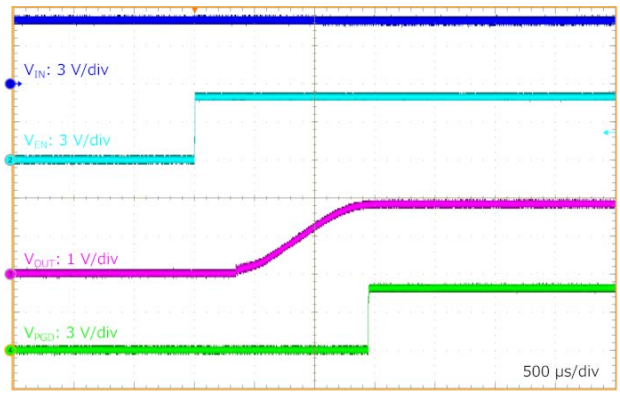


Figure 58. EN Start-up at R_{Load} = 0.6 Ω
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, V_{EN} = 0 V to 5 V)

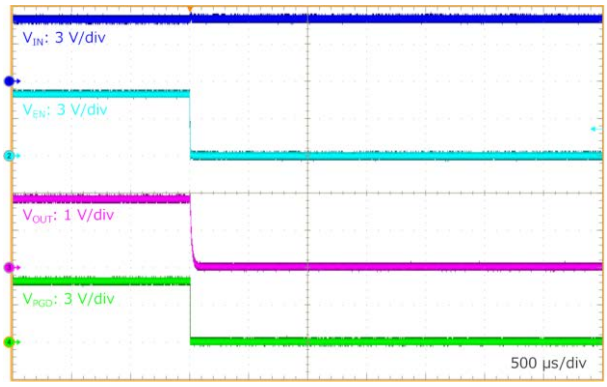


Figure 59. EN Shutdown at R_{Load} = 0.6 Ω
(V_{IN} = 5.0 V, V_{OUT} = 1.8 V, V_{EN} = 5 V to 0 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

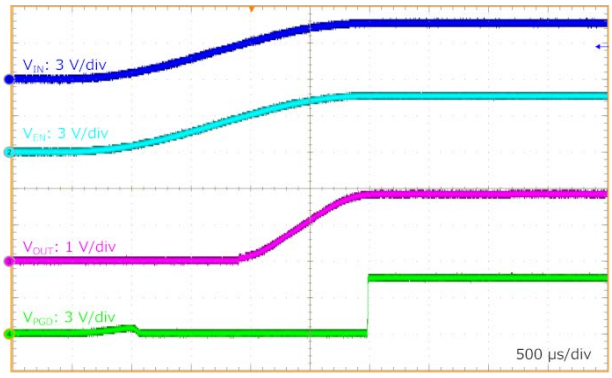


Figure 60. VIN Start-up at No Load
(V_{IN} = V_{EN} = 0 V to 5 V, V_{OUT} = 1.8 V)

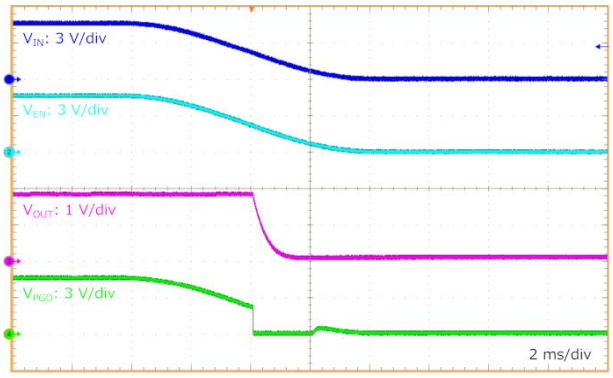


Figure 61. VIN Shutdown at No Load
(V_{IN} = V_{EN} = 5 V to 0 V, V_{OUT} = 1.8 V)

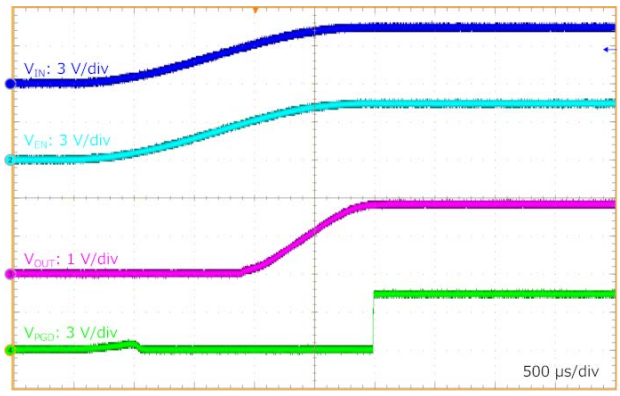


Figure 62. VIN Start-up at R_{Load} = 0.6 Ω
(V_{IN} = V_{EN} = 0 V to 5 V, V_{OUT} = 1.8 V)

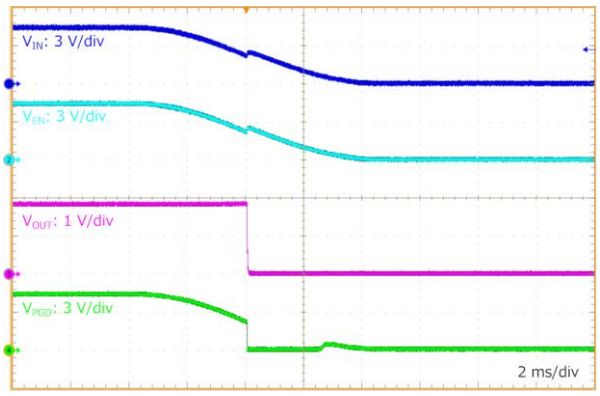


Figure 63. VIN Shutdown at R_{Load} = 0.6 Ω
(V_{IN} = V_{EN} = 5 V to 0 V, V_{OUT} = 1.8 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

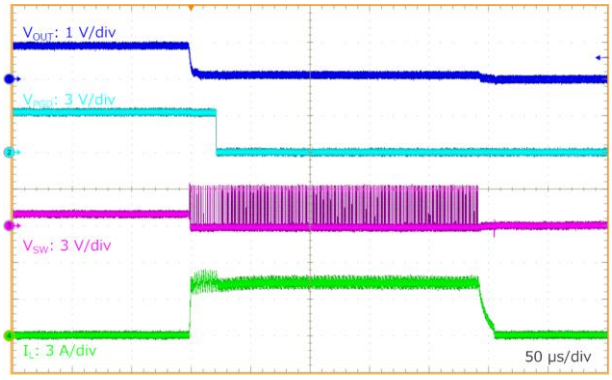


Figure 64. OCP Operation
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V to 0 V)

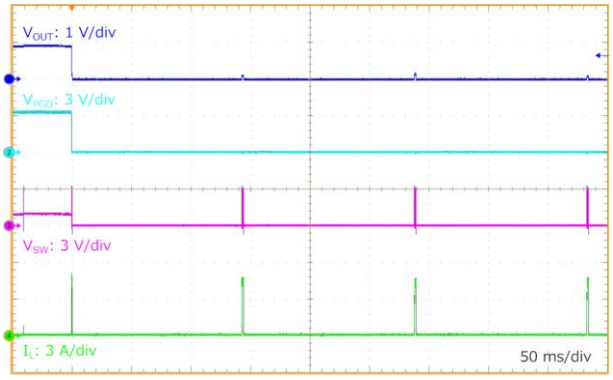


Figure 65. SCP Operation
(V_{IN} = 3.3 V, V_{OUT} = 0.9 V to 0 V)

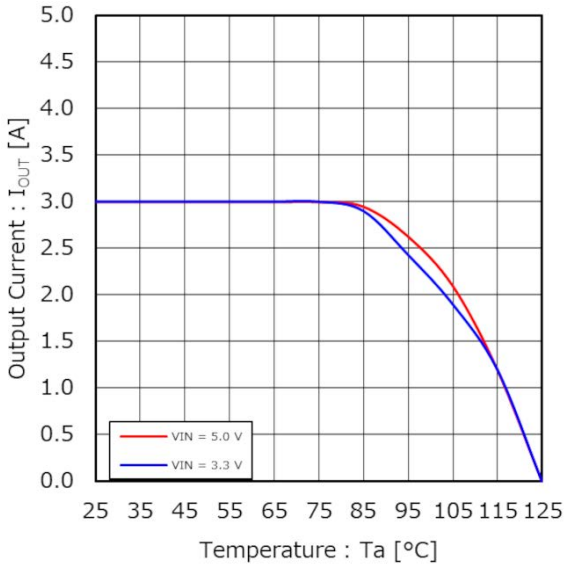


Figure 66. Thermal Derating
(V_{OUT} = 0.9 V)

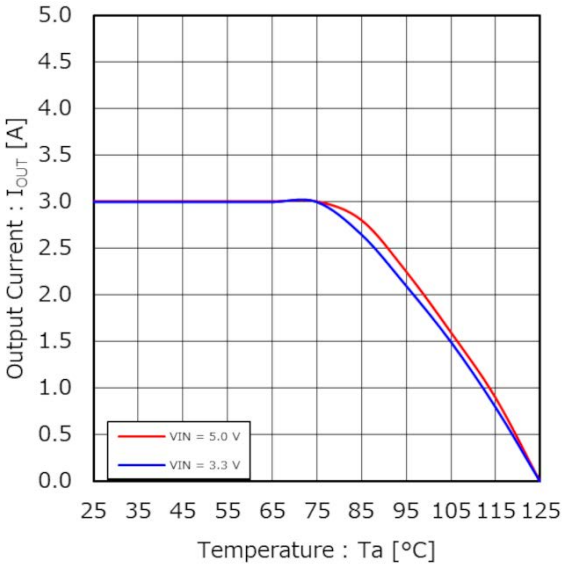


Figure 67. Thermal Derating
(V_{OUT} = 1.2 V)

Application Characteristic Data (Reference Data) – continued

The parts list of Table 6 is used.

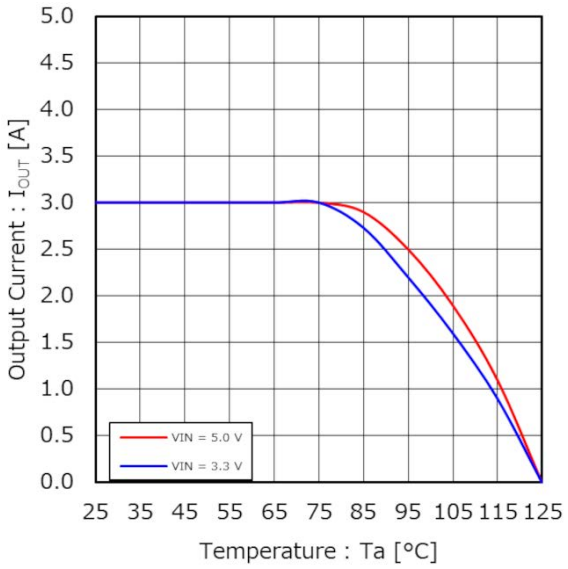


Figure 68. Thermal Derating
(V_{OUT} = 1.8 V)

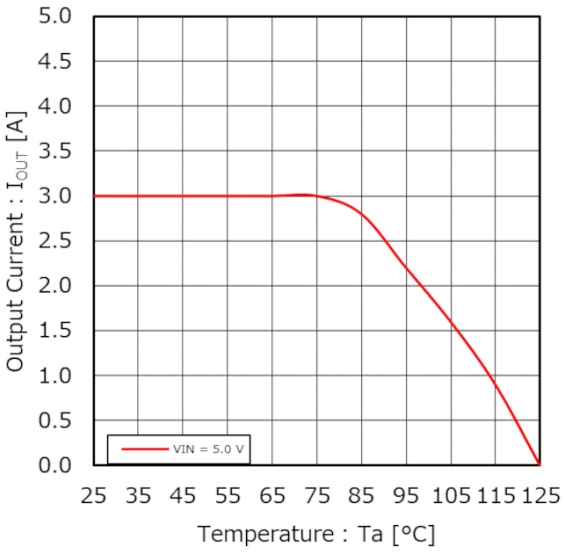


Figure 69. Thermal Derating
(V_{OUT} = 3.3 V)

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 70-a to Figure 70-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 70-a is a current path when High side switch is ON and Low side switch is OFF, the Loop 2 in Figure 70-b is when High side switch is OFF and Low side switch is ON. The thick line in Figure 70-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element High side and Low side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

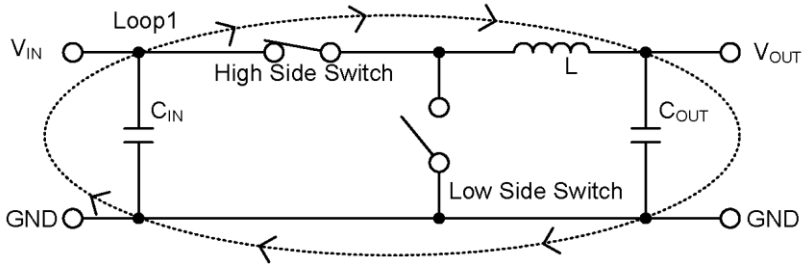


Figure 70-a. Current Path when High Side Switch = ON, Low Side Switch = OFF

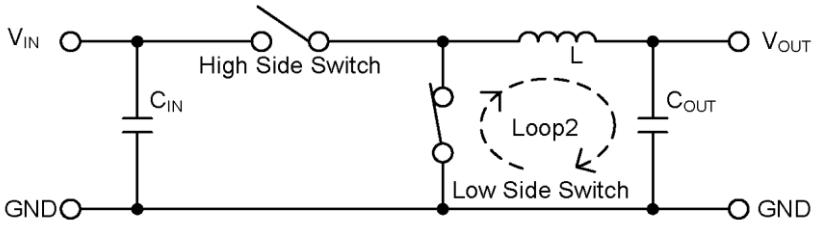


Figure 70-b. Current Path when High Side Switch = OFF, Low Side Switch = ON

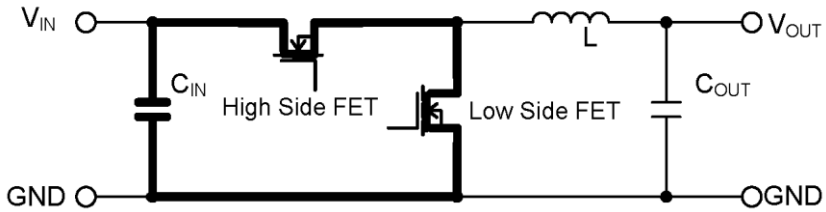


Figure 70-c. Difference of Current and Critical Area in Layout

PCB Layout Design – continued

When designing the PCB layout, pay attention to the following points:

- Connect the input capacitor C_{IN} as close as possible to the VIN pin and GND pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern L_1 as thick and as short as possible.
- R_{UP} and R_{DW} shall be located as close as possible to the FB pin and the wiring to the FB pin shall be as short as possible.
- Feedback line connected to the FB pin far from the SW nodes.
- R_0 is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_0, it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_0 is short-circuited for normal use.

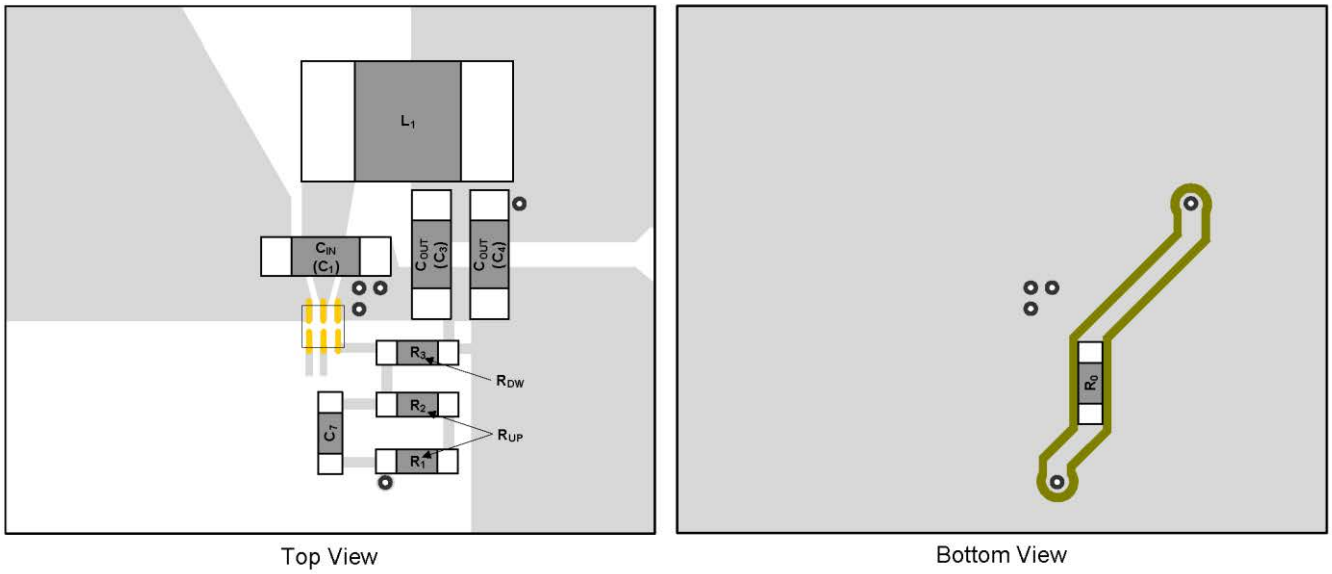


Figure 71. Example of PCB Layout

Thermal Design

For thermal design, be sure to operate at the chip junction temperature Tj of 125 °C or less.
(Be sure to take margins into account.)

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

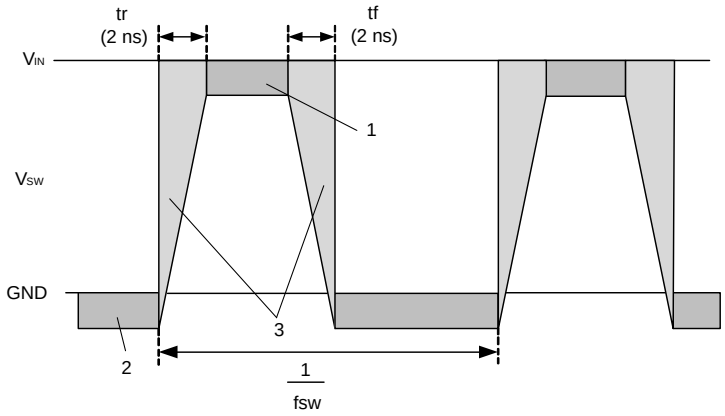
ψ_{JT} is junction to top characterization parameter (Thermal Resistance)
θ_{JA} is junction to ambient (Thermal Resistance)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

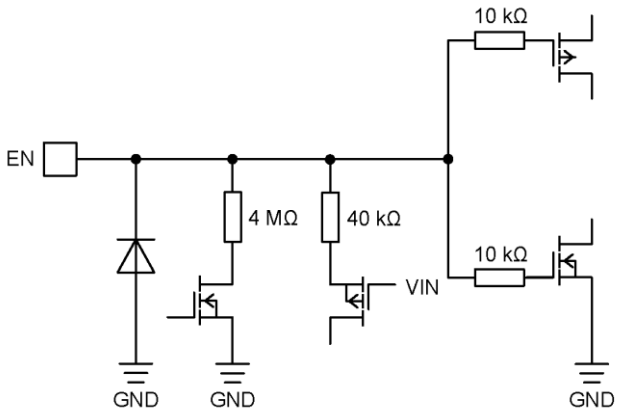
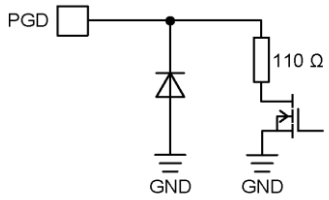
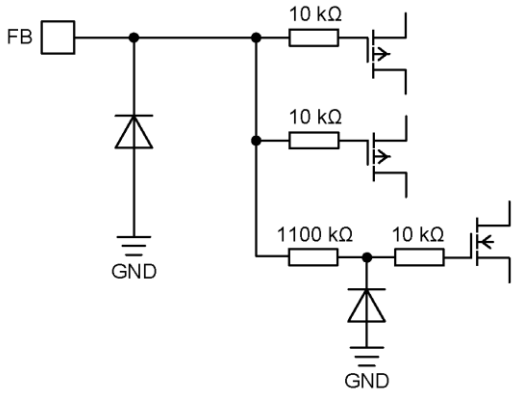
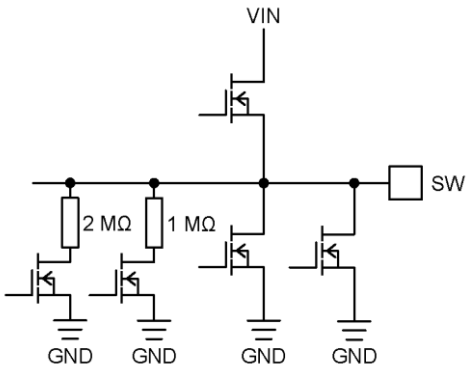
R_{ONH}	is the High Side FET ON Resistance (Electrical Characteristics) [Ω]
R_{ONL}	is the Low Side FET ON Resistance (Electrical Characteristics) [Ω]
I_{OUT}	is the Output Current [A]
V_{OUT}	is the Output Voltage [V]
V_{IN}	is the Input Voltage [V]
I_{CC}	is the Circuit Current [A] (Typ: 450 μA)
tr	is the Switching Rise Time [s] (Typ: 2 ns)
tf	is the Switching Fall Time [s] (Typ: 2 ns)
f_{SW}	is the Switching Frequency [Hz] (Typ: 2.2 MHz)



1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW}$

Figure 72. SW Waveform

I/O Equivalence Circuits

1. EN	2. PGD
	
3. FB	**5. SW**
	

(Note) Resistor values are typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **3Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

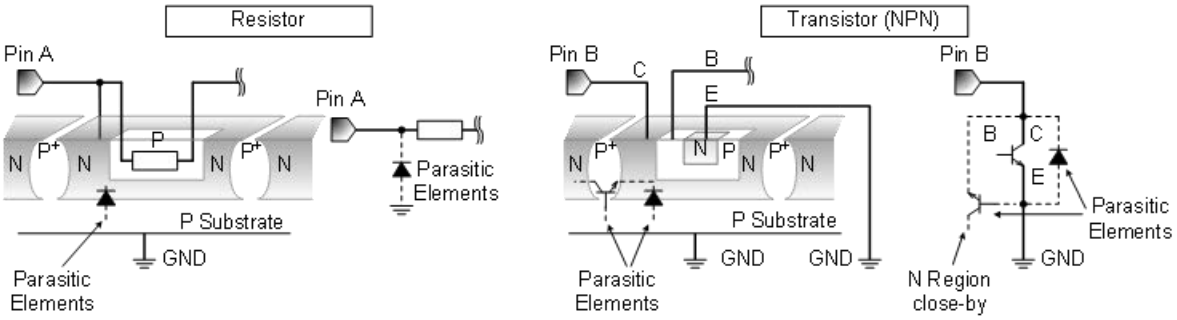


Figure 73. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

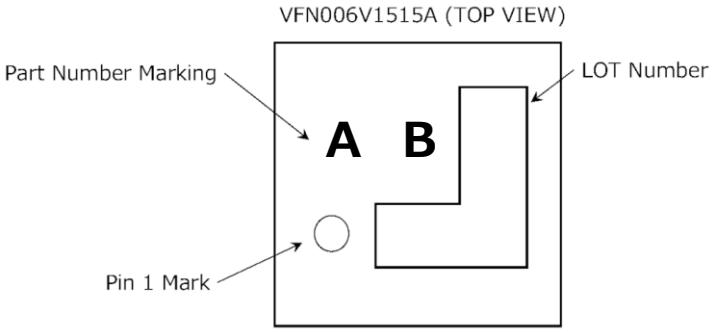
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B	D	9	B	3	0	6	N	F	-	Z	T	R

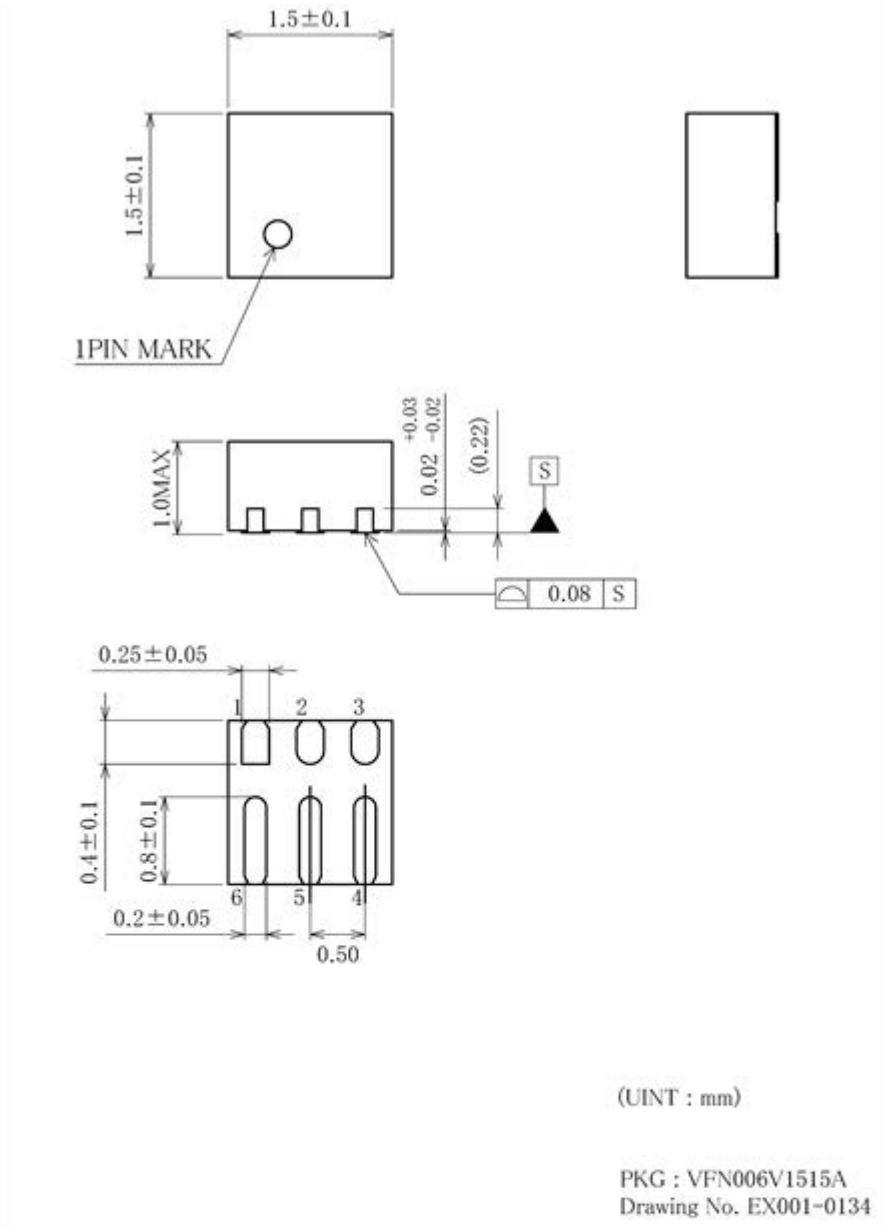
- Output Current: 3.0 A
- Package: NF: VFN006V1515A
- Packaging and forming specification: Z: Outsourced package; TR: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	VFN006V1515A



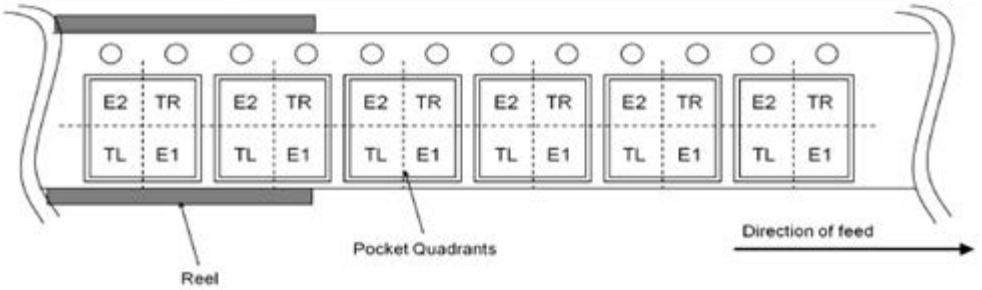
(UINT : mm)

PKG : VFN006V1515A
Drawing No. EX001-0134

NOTE:Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
01.Mar.2023	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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