4 V to 16 V Input, 12 A Integrated MOSFET Single Synchronous Buck DC/DC Converter

BD9DA00MF

General Description

BD9DA00MF is a synchronous buck DC/DC converter with built-in low on-resistance power MOSFETs. The device operates with output current up to 12 A. The output voltage accuracy is ±1%. It features fast transient response due to QuiCur™ and constant on-time control system. The Light Load Mode control improves efficiency in light-load conditions. It achieves high power density and offer a small footprint on the PCB by employing small package.

Key Specifications

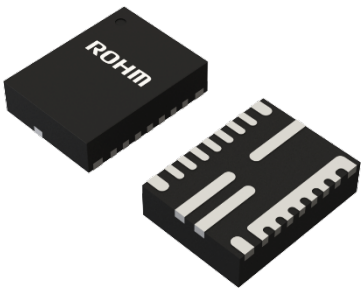
- Input Voltage Range: 4 V to 16 V
- Input Voltage Range with External VCC Bias: 2.7 V to 14 V
- Output Voltage Range: 0.6 V to 5.5 V
- Output Current: 12 A (Max)
- Switching Frequency: 600 kHz, 800 kHz, 1 MHz (Typ)
- High-Side FET ON Resistance: 16 mΩ (Typ)
- Low-Side FET ON Resistance: 4 mΩ (Typ)
- Shutdown Current: 0 µA (Typ)

Features

- QuiCur™
- Nano Pulse Control™
- Single Synchronous Buck DC/DC Converter
- Constant On-time Control
- Light Load Mode (LLM)
- Adjustable Soft Start
- Power Good Output
- Selectable Switching Frequency
- Output Voltage Remote Sense
- Adjustable Reference Voltage
- Output Discharge
- Over Voltage Protection (OVP)
- Adjustable Over Current Protection (OCP)
- Short Circuit Protection (SCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lockout Protection (UVLO)

Package

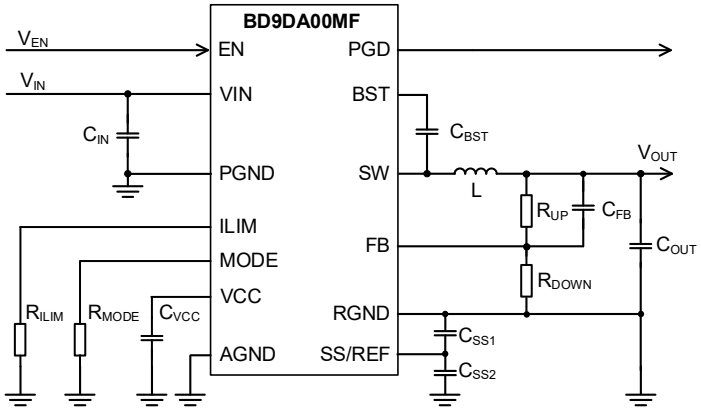
Package	W (Typ) x D (Typ) x H (Max)
UFN014V3040	3.0 mm x 4.0 mm x 1.0 mm



Applications

- Step-down Power Supply for SoC, FPGA, Microprocessor
- Servers

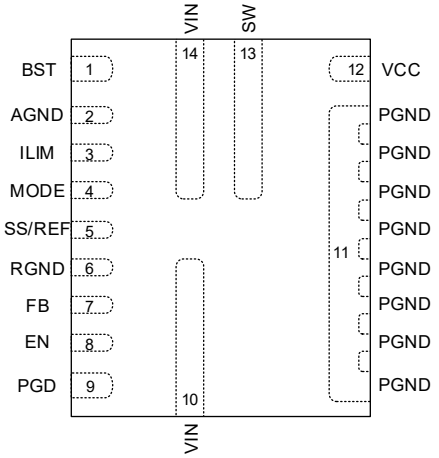
Typical Application Circuit



Contents

Pin Configuration

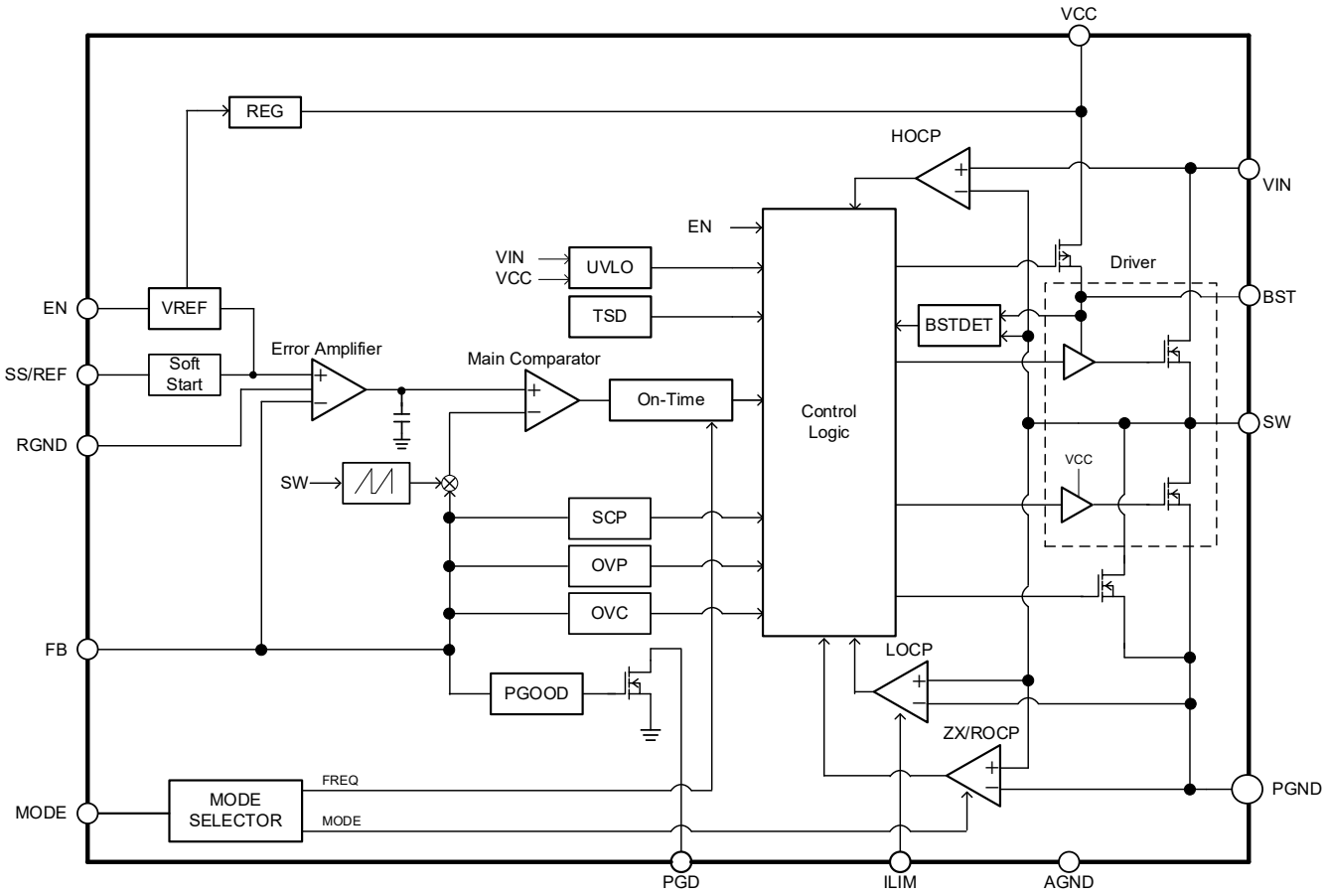
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	BST	Pin for bootstrap. Connect a bootstrap capacitor of 0.1 µF (Typ) between the BST pin and the SW pin. The voltage of this capacitor is the gate drive of the High-Side FET.
2	AGND	Ground pin for the control circuit.
3	ILIM	Current limit value setting pin. For the setting method, refer to Selection of Components Externally Connected 7. OCP Setting Resister.
4	MODE	Switching control mode setting pin. For the setting method, refer to Function Explanations 1. Basic Operation (11) Control Mode Selectable Function
5	SS/REF	Soft start time setting pin and Reference voltage setting pin.
6	RGND	Remote sense ground pin. It is also used as a ground for the internal reference voltage. If the remote sense function is not used, connect this pin to AGND.
7	FB	Output voltage feedback pin. For the setting method, refer to Selection of Components Externally Connected 3. Output Voltage Setting.
8	EN	Enable pin. The device starts up with setting V_{EN} to 1.22 V (Typ) or more. The device enters the shutdown mode with setting V_{EN} to 1.02 V (Typ) or less. This pin must not be left open.
9	PGD	Power Good pin. This pin is an open drain output that requires a pull-up resistor. If not used, this pin can be left floating or connected to the ground.
10, 14	VIN	Power supply pins.
11	PGND	Ground pins for the output stage of the switching regulator.
12	VCC	3.0 V (Typ) output power supply pin for the internal circuit. Connect a ceramic capacitor of 1.0 µF (Typ). Do not connect to any external loads except the MODE pin and a pull-up resistor for the PGD pin. It is also possible to apply voltage externally to this pin.
13	SW	Switch pin. This pin is connected to the source of the High-Side FET and the drain of the Low-Side FET. Connect a 0.1 µF bootstrap capacitor between this pin and the BST pin. Additionally, please connect an output LC filter to this pin. For the output LC filter setting method, refer to Selection of Components Externally Connected 2. Output LC Filter.

Block Diagram



Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. REG
   The REG block generates internal power supply. It outputs 3.0 V (Typ) and supplies to the control circuits and the Driver.

3. Soft Start
   The Soft Start circuit slows down the rise of output voltage during startup, which prevents output voltage overshoot. The soft start time can be set by connecting a capacitor to the SS/REF pin. For the setting method, refer to Selection of Components Externally Connected 4. Soft Start Capacitor.

4. Error Amplifier
   The Error Amplifier adjusts the Main Comparator input voltage to make the FB voltage equal to the internal reference voltage.

5. Main Comparator
   The Main Comparator compares the Error Amplifier output voltage and the voltage with Ramp superimposed on FB voltage (V_{FB}) . When V_{FB} becomes lower than the Error Amplifier output voltage, the output turns high and reports to the On-Time block that the output voltage has dropped below the control voltage.

6. On-Time
   The On-Time block generates On Time. The designed On Time is generated after the Main Comparator output turns high. The On Time is adjusted to control the frequency to be fixed even if input / output voltage is changed.

7. PGOOD
   The PGOOD block is for power good function.

8. OVC
   The OVC block is for output voltage clamp. When the FB pin voltage (V_{FB}) becomes 104 % (Typ) or more of the FB reference voltage V_{REF}, the Low-Side FET turns on and suppresses the rise of the output voltage. When V_{FB} becomes 103 % (Typ) or less of V_{REF}, the device returns to normal operation.

9. OVP
   The OVP block is for output over voltage protection. OVP function operates when the FB pin voltage V_{FB} becomes 116 % (Typ) or more of the FB reference voltage V_{REF}, and it depends on the device operation mode. Refer to Function Explanations 2. Protection (5) Over Voltage Protection (OVP).

10. UVLO
    The UVLO block is for under voltage lockout protection. The device shuts down when input voltage V_{IN} falls to 1.85 V (Typ) or less, or VCC voltage V_{CC} falls to 2.5 V (Typ) or less.

11. BSTDET
    The BSTDET block detects the low voltage between the SW and BST (ΔV_{BST-SW}). The Low-Side FET turns on and charges a bootstrap capacitor when ΔV_{BST-SW} is 2.1 V (Typ) or less.

12. TSD
    The TSD block is for thermal protection. The device shuts down when the junction temperature Tj reaches to 175 °C (Typ) or more. When Tj drops, the device restarts with a hysteresis of 25 °C (Typ).

13. HOCP
    The HOCP block is for over current protection of the High-Side FET. When the current that flows through the High-Side FET reaches the over current limit I_{HOCP} = 17.5 A (Typ), the device turns off the High-Side FET and turns on the Low-Side FET.

14. LOCP
    The LOCP block is for over current protection of the Low-Side FET. While the current that flows through the Low-Side FET over the value of over current limit, the device keep turning on the Low-Side FET.

15. SCP
    The SCP block is for short circuit protection. After 3 ms (Typ) from the beginning of soft start, and after SS/REF voltage (V_{SSREF}) reaches 0.6 V (Typ), if V_{FB} is 80 % (Typ) of FB reference voltage V_{REF} or less, or over current protection is detected for 31 consecutive cycles, the device shuts down for 117 ms (Typ). After 117 ms shutdown, the device restarts.

Description of Blocks – continued

16. ZX/ROCP
    The ZX/ROCP is a comparator that monitors the inductor current. When the inductor current falls below 0 A (Typ) while the Low-Side FET is on, it turns the FET off (Light Load Mode). When the current that flows through the Low-Side FET reaches the value of reverse detection current, the device turns off the Low-Side FET and turns on the High-Side FET (Forced CCM Mode).

17. Control Logic
    The Control Logic controls the switching operation and the protection function operation.

18. MODE SELECTOR
    The MODE SELECTOR block controls the switching frequency and the operating mode.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +18.0	V
SW Voltage (DC)	V_{SW}	-0.3 to V_{IN} + 0.3	V
SW Voltage (AC, 3 ns or less)	V_{SWAC}	-5.0 to +20.0	V
Voltage from GND to BST	V_{BST}	-0.3 to +22.5	V
Voltage from SW to BST	ΔV_{BST-SW}	-0.3 to +4.5	V
FB Voltage	V_{FB}	-0.3 to +4.5	V
VCC Voltage	V_{CC}	-0.3 to +4.5	V
MODE Voltage	V_{MODE}	-0.3 to +4.5	V
ILIM Voltage	V_{ILIM}	-0.3 to +4.5	V
PGD Voltage	V_{PGD}	-0.3 to +7.0	V
EN Voltage	V_{EN}	-0.3 to +7.0	V
SS/REF Voltage	V_{SSREF}	-0.3 to +4.5	V
RGND Voltage	V_{RGND}	-0.3 to +0.3	V
Maximum Peak Inductor Current	$I_{L\_PEAKMAX}$	18	A
Maximum Junction Temperature*(Note 1)*	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The lifetime and reliability of the device is reduced if the device operates continually at the maximum junction temperature.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		2s2p*(Note 4)*	EVK*(Note 5)*	
UFN014V3040				
Junction to Ambient	θ_{JA}	52.4	28.7	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	4.0	4.0	°C/W

(Note 2) Based on JESD51-2A (Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-7.

(Note 5) Evaluation Kit. Measured on FR-4 board 80.0 mm x 80.0 mm x 1.6 mm, Copper Thickness: All Layers 70µm.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	4	-	16	V
Input Voltage with External VCC Bias		2.7	-	14	V
External VCC Bias	V_{CC_EXT}	3.13	-	3.60	V
Operating Junction Temperature	Tj	-40	-	+125	°C
Output Current *(Note 1)*	I_{OUT}	0	-	12	A
Output Voltage Setting *(Note 2)*	V_{OUT}	0.6	-	5.5	V

(Note 1) Tj must be 125 °C or less under the actual operating environment.
(Note 2) At low duty cycles, the frequency is lowered accordingly. Additionally, at high duty cycles, the output voltage may be limited by the V_{IN} voltage. Please use the range of formulas listed in Selection of Components Externally Connected 3.Output Voltage Setting.

Electrical Characteristics (Unless otherwise specified Tj = -40 °C to +125 °C, V_{IN} = 12 V, V_{EN} = 2 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Supply						
Shutdown Current	I_{SDN}	-	0	10	µA	V_{EN} = 0 V
Operating Quiescent Current	I_Q	-	600	1200	µA	I_{OUT} = 0 A, No switching
Enable						
EN Threshold Voltage High	V_{ENH}	1.17	1.22	1.27	V	V_{EN} rising
EN Threshold Voltage Low	V_{ENL}	-	1.02	-	V	V_{EN} falling
EN Hysteresis Voltage	V_{ENHYS}	-	200	-	mV	
EN Input Current	I_{EN}	-	0	2	µA	V_{EN} = 2 V
VIN UVLO						
VIN UVLO Detection Threshold Voltage	$V_{INUVLO1}$	1.55	1.85	2.15	V	V_{IN} falling
VIN UVLO Release Threshold Voltage	$V_{INUVLO2}$	2.1	2.4	2.7	V	V_{IN} rising
VCC						
VCC UVLO Detection Threshold Voltage	$V_{CCUVLO1}$	2.35	2.50	2.65	V	V_{CC} falling
VCC UVLO Release Threshold Voltage	$V_{CCUVLO2}$	2.65	2.80	2.95	V	V_{CC} rising
VCC Output Voltage	V_{CC}	2.88	3.00	3.12	V	
Reference Voltage, Error Amplifier, Soft Start						
FB Reference Voltage	V_{REF}	0.594	0.600	0.606	V	Forced CCM mode
FB Input Current	I_{FB}	-	-	100	nA	V_{FB} = 0.6 V
Error Amplifier Offset Voltage	V_{OFFSET}	-3	0	+3	mV	
Soft Start Time	t_{SS}	0.75	1.00	1.25	ms	C_{SS1} + C_{SS2} = 0.044 µF
SS/REF Source Current	I_{SS_SO}	-	36	-	µA	$V_{SS/REF}$ = 0.2 V
SS/REF Sink Current	I_{SS_SI}	-	12	-	µA	$V_{SS/REF}$ = 1 V
Control						
On-Time 1	t_{ON1}	133	167	200	ns	V_{OUT} = 1.2 V, Forced CCM mode, 600 kHz setting
On-Time 2	t_{ON2}	100	125	150	ns	V_{OUT} = 1.2 V, Forced CCM mode, 800 kHz setting
On-Time 3	t_{ON3}	80	100	120	ns	V_{OUT} = 1.2 V, Forced CCM mode, 1 MHz setting
Minimum On-Time *(Note 3)*	t_{MINON}	-	45	-	ns	
Minimum Off-Time	t_{MINOFF}	-	150	-	ns	
SW (MOSFET)						
High-Side FET ON Resistance	R_{ONH}	-	16	-	mΩ	V_{BST} - V_{SW} = 3 V
Low-Side FET ON Resistance	R_{ONL}	-	4	-	mΩ	V_{CC} = 3 V
Discharge FET ON Resistance	R_{ON_DIS}	-	70	150	Ω	V_{CC} = 3 V

(Note 3) This is design value. No tested on outgoing inspection.

Electrical Characteristics – continued
(Unless otherwise specified Tj = -40 °C to +125 °C, V_{IN} = 12 V, V_{EN} = 2 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Good						
Power Good Rising Threshold Voltage	$V_{PGDTHGR}$	89.5	92.5	95.5	%	V_{FB} rising, $V_{PGDTHGR}$ = V_{FB} / V_{REF} x 100
Power Fault Rising Threshold Voltage	$V_{PGDTHFR}$	113	116	119	%	V_{FB} rising, $V_{PGDTHFR}$ = V_{FB} / V_{REF} x 100
Power Fault Falling Threshold Voltage	$V_{PGDTHFF}$	77	80	83	%	V_{FB} falling, $V_{PGDTHFF}$ = V_{FB} / V_{REF} x 100
PGD Low to High Delay Time	t_{DPGD}	0.63	0.90	1.17	ms	
PGD Output Leakage Current	I_{LKPGD}	-	-	3	µA	V_{PGD} = 3.3 V
PGD MOSFET ON Resistance	R_{PGD}	-	15	40	Ω	V_{CC} = 3 V
PGD Clamp Voltage 1	V_{PGDCL1}	-	600	-	mV	V_{IN} = 0 V, 100 kΩ pull up to 3.3 V, Tj = 25 °C
PGD Clamp Voltage 2	V_{PGDCL2}	-	700	-	mV	V_{IN} = 0 V, 10 kΩ pull up to 3.3 V, Tj = 25 °C
Protection						
OVP Threshold Voltage	V_{OVP}	113	116	119	%	V_{OVP} = V_{FB} / V_{REF} x 100
SCP Threshold Voltage	V_{SCP}	77	80	83	%	V_{SCP} = V_{FB} / V_{REF} x 100
Current Limit Threshold	V_{LIM}	1.15	1.20	1.25	V	
I_{ILIM} to I_{OUT} Ratio *(Note 1)*	I_{ILIM}/I_{OUT}	18.0	20.0	22.0	µA/A	4.7 kΩ ≤ R_{ILIM} ≤ 6.2 kΩ
		16.4	20.0	23.2		6.2 kΩ < R_{ILIM} ≤ 10 kΩ
Low-Side FET Reverse Detection Current *(Note 1)*	I_{ROCP}	-	6.5	-	A	

(Note 1) This is design value. No tested on outgoing inspection

Typical Performance Curves

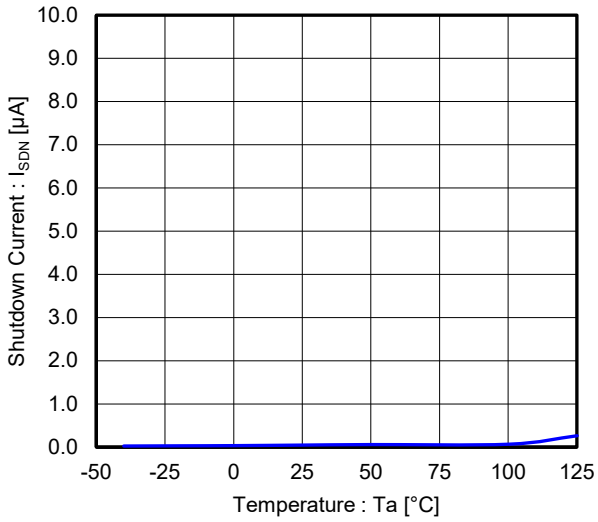


Figure 1. Shutdown Current vs Temperature
(V_{IN} = 12 V, V_{EN} = 0 V)

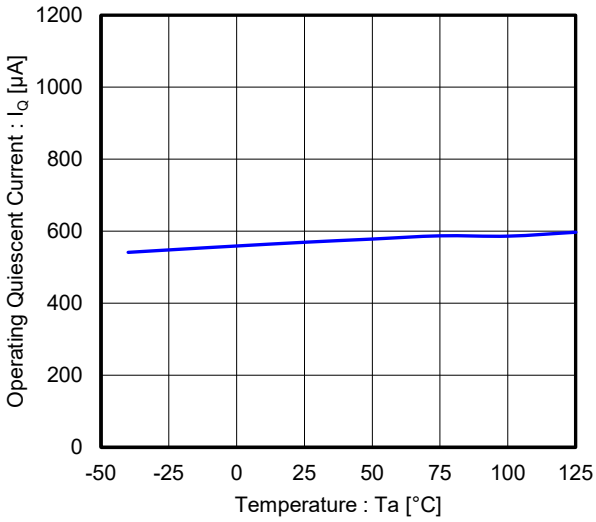


Figure 2. Operating Quiescent Current vs Temperature
(V_{IN} = 12 V, V_{EN} = 2 V)

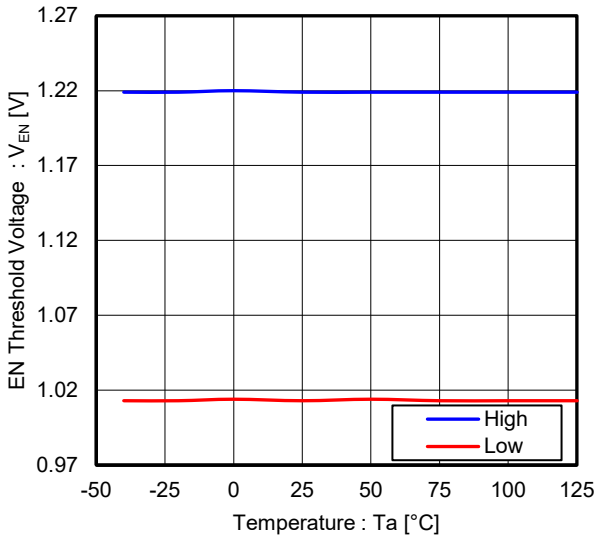


Figure 3. EN Threshold Voltage vs Temperature

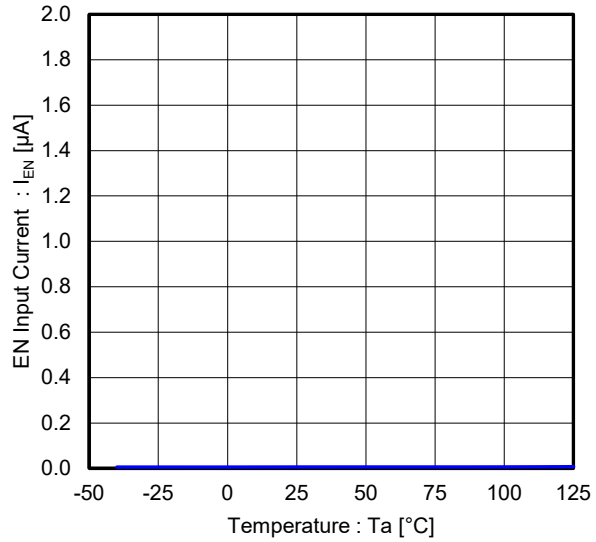


Figure 4. EN Input Current vs Temperature
(V_{EN} = 2 V)

Typical Performance Curves – continued

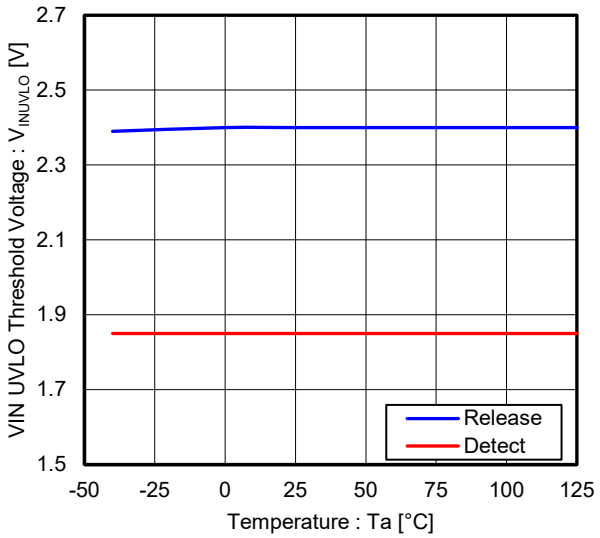


Figure 5. VIN UVLO Threshold Voltage vs Temperature
(V_{CC} = 3.3 V)

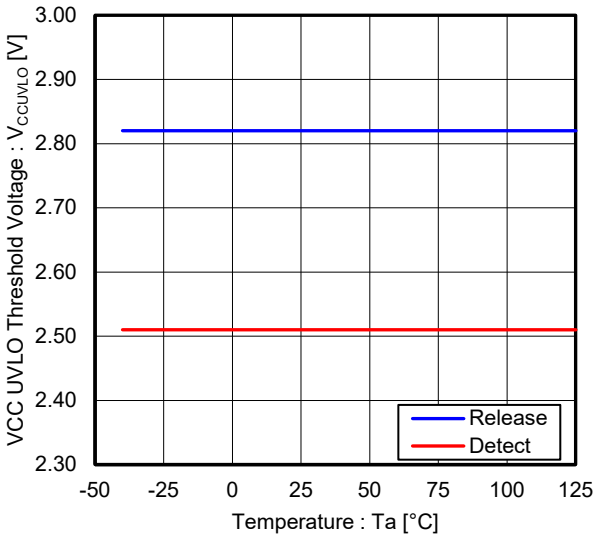


Figure 6. VCC UVLO Threshold Voltage vs Temperature
(V_{IN} = 2.7 V)

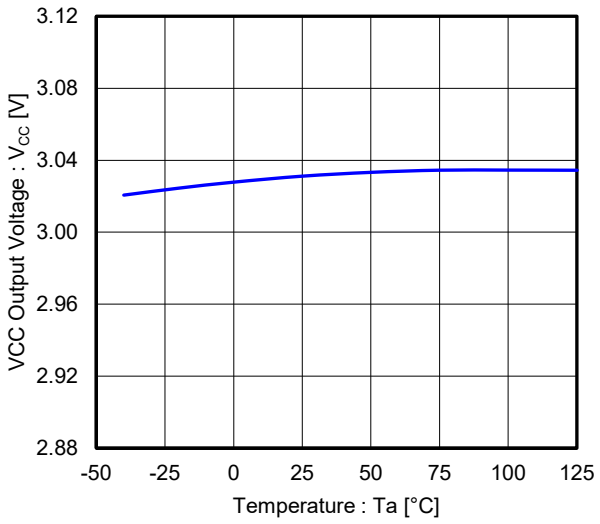


Figure 7. VCC Output Voltage vs Temperature
(V_{IN} = 12 V)

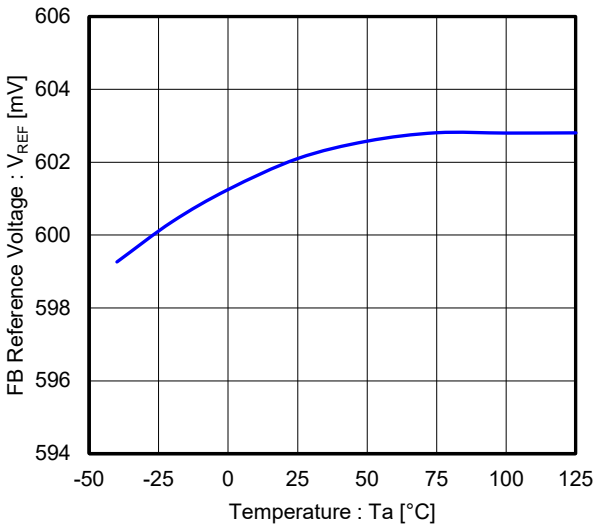


Figure 8. FB Reference Voltage vs Temperature

Typical Performance Curves – continued

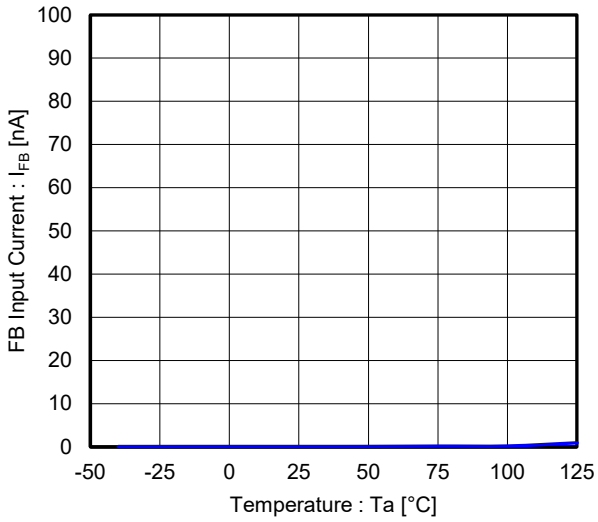


Figure 9. FB Input Current vs Temperature
(V_{FB} = 0.6 V)

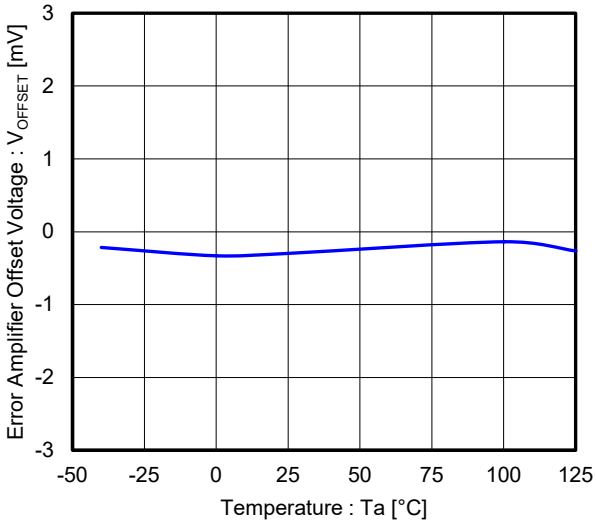


Figure 10. Error Amplifier Offset Voltage vs Temperature

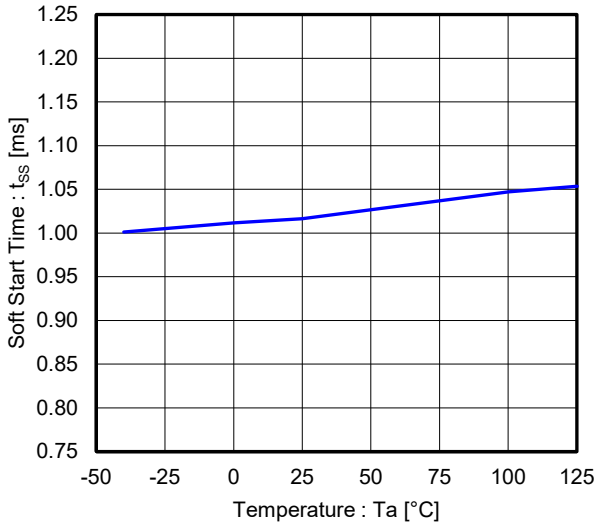


Figure 11. Soft Start Time vs Temperature

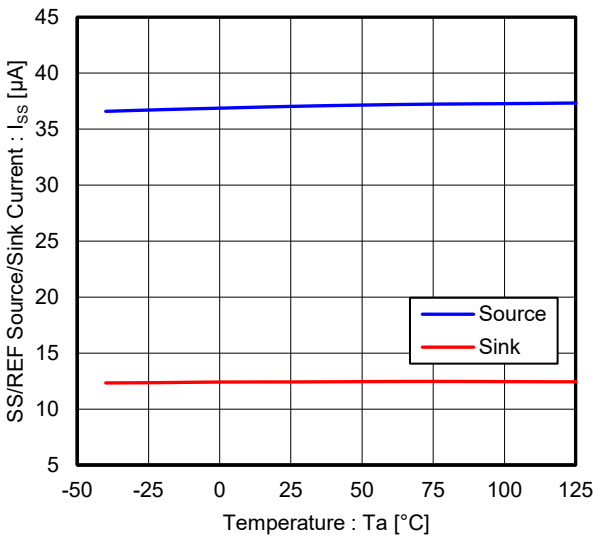


Figure 12. SS/REF Source/Sink Current vs Temperature

Typical Performance Curves – continued

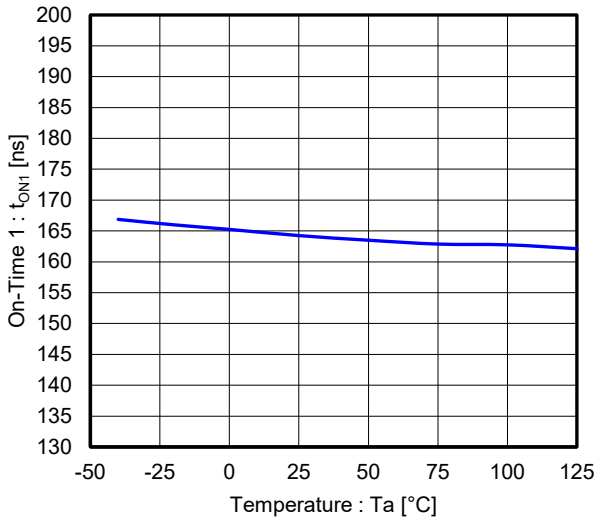


Figure 13. On-Time 1 (600 kHz setting) vs Temperature
(V_{IN} = 12 V, V_{OUT} = 1.2 V)

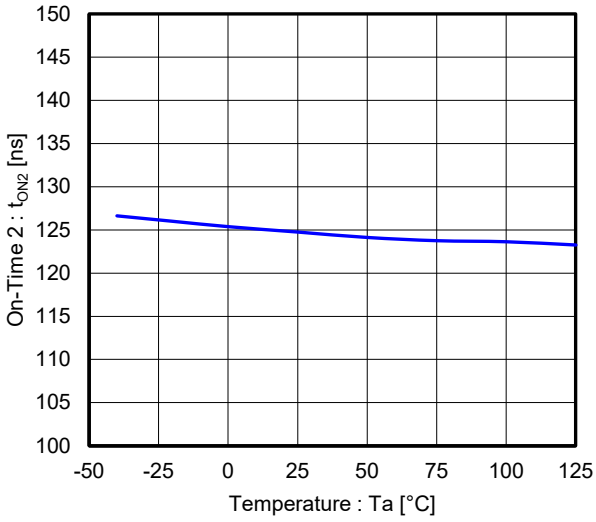


Figure 14. On-Time 2 (800 kHz setting) vs Temperature
(V_{IN} = 12 V, V_{OUT} = 1.2 V)

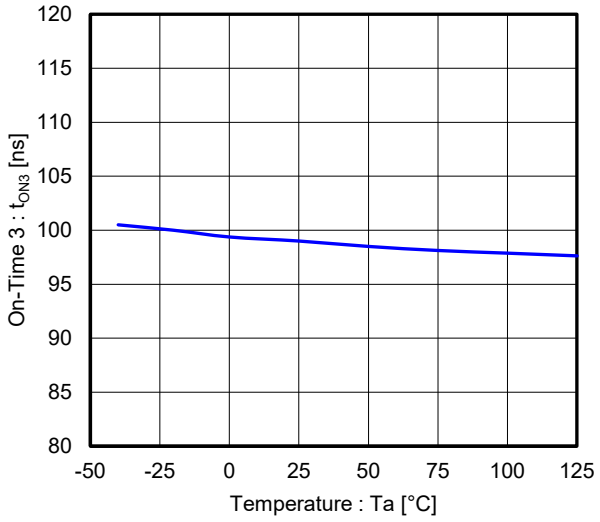


Figure 15. On-Time 3 (1 MHz setting) vs Temperature
(V_{IN} = 12 V, V_{OUT} = 1.2 V)

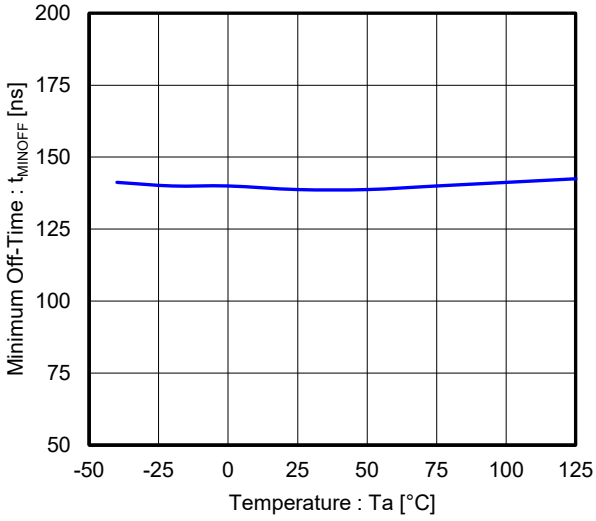


Figure 16. Minimum Off-Time vs Temperature

Typical Performance Curves – continued

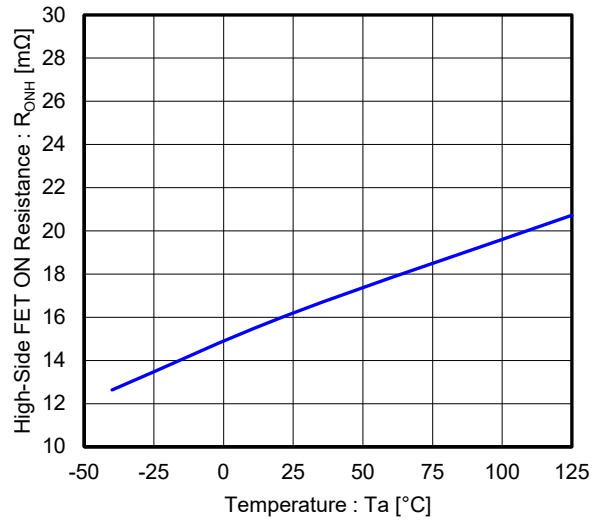


Figure 17. High-Side FET ON Resistance vs Temperature (V_{CC} = 3 V)

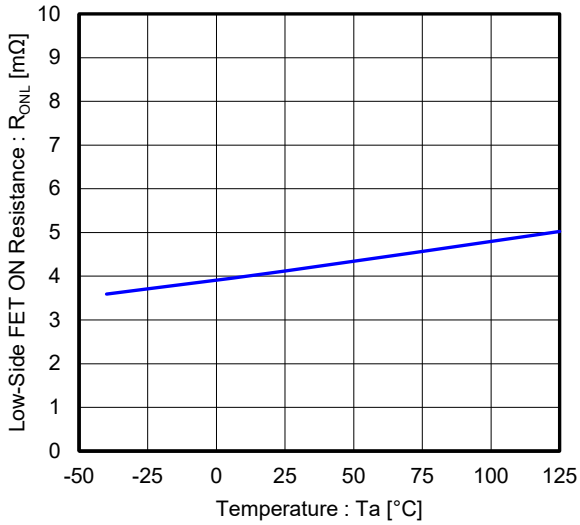


Figure 18. Low-Side FET ON Resistance vs Temperature (V_{CC} = 3 V)

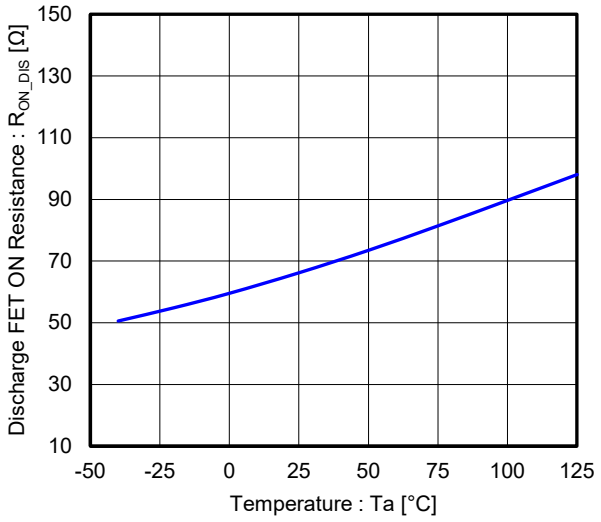


Figure 19. Discharge FET ON Resistance vs Temperature (V_{CC} = 3 V)

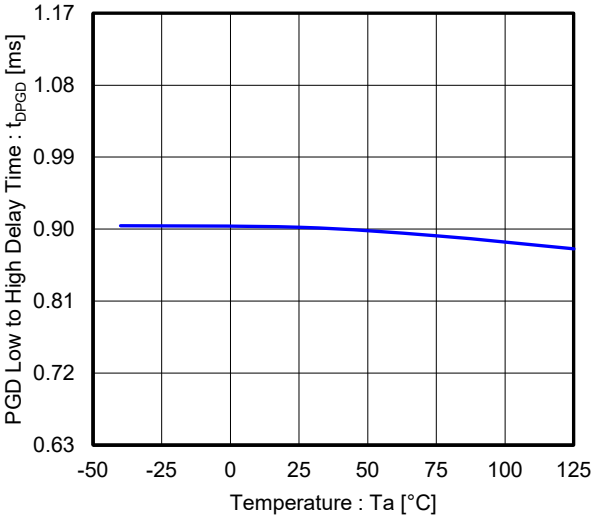


Figure 20. PGD Low to High Delay Time vs Temperature

Typical Performance Curves – continued

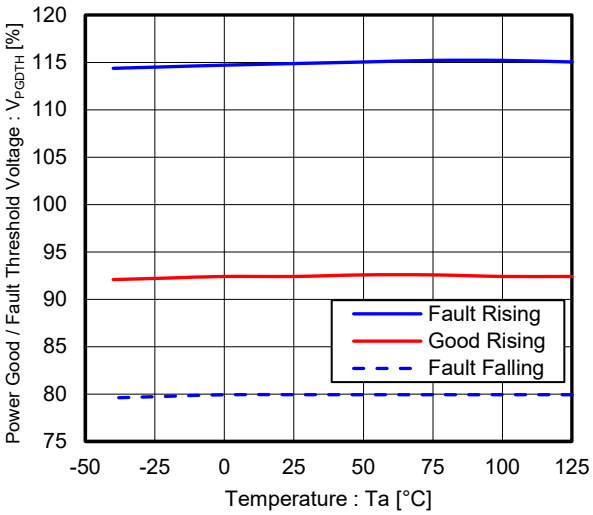


Figure 21. Power Good / Fault Threshold Voltage vs Temperature

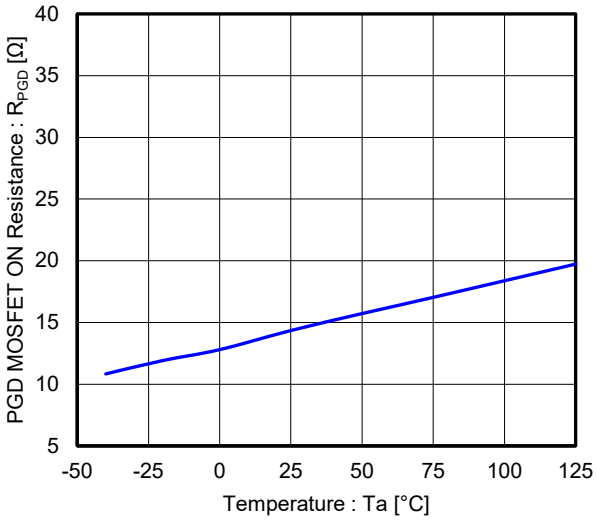


Figure 22. PGD MOSFET ON Resistance vs Temperature (V_{CC} = 3 V)

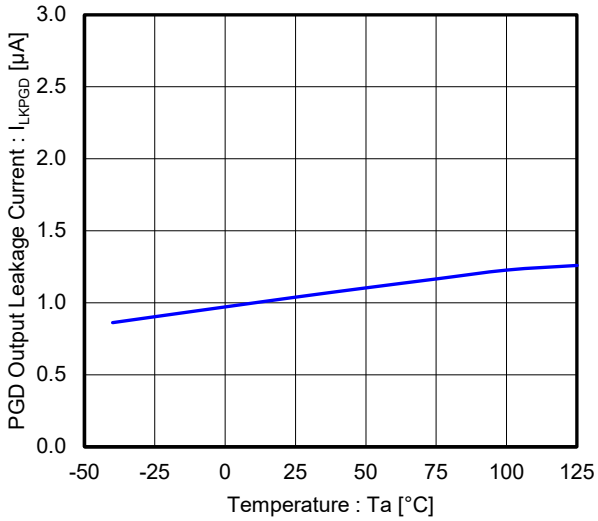


Figure 23. PGD Output Leakage Current vs Temperature (V_{PGD} = 3.3 V)

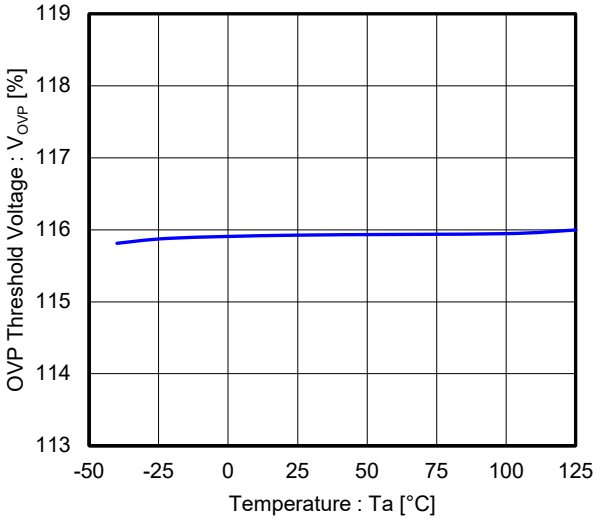


Figure 24. OVP Threshold Voltage vs Temperature

Typical Performance Curves – continued

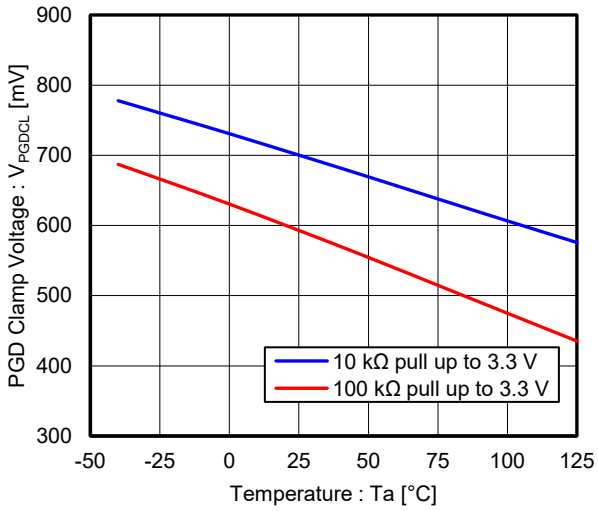


Figure 25. PGD Clamp Voltage vs Temperature

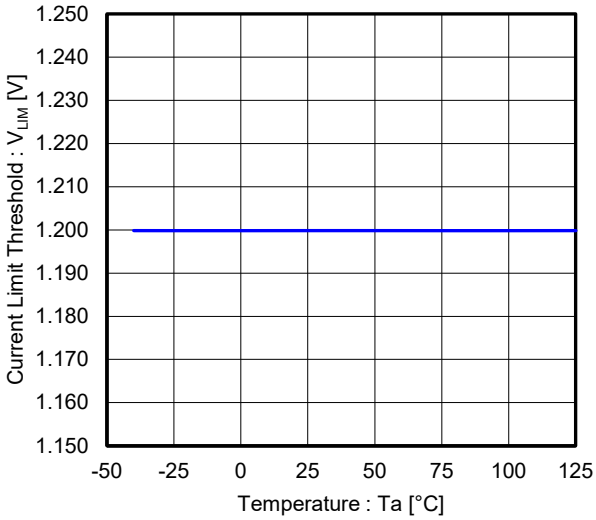


Figure 26. Current Limit Threshold vs Temperature

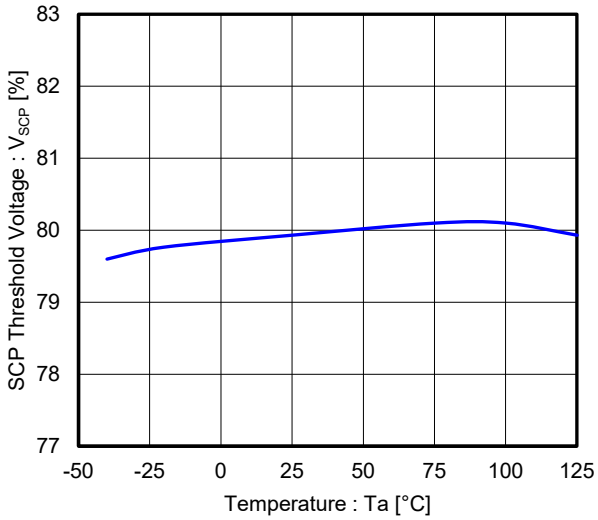


Figure 27. SCP Threshold Voltage vs Temperature

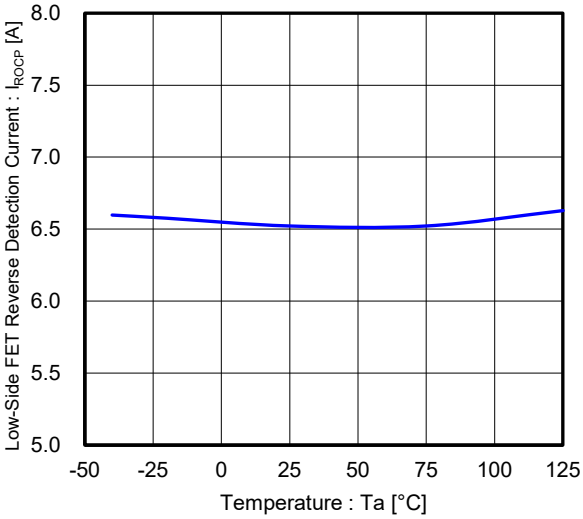


Figure 28. Low-Side FET Reverse Detection Current vs Temperature

Typical Performance Curves – continued

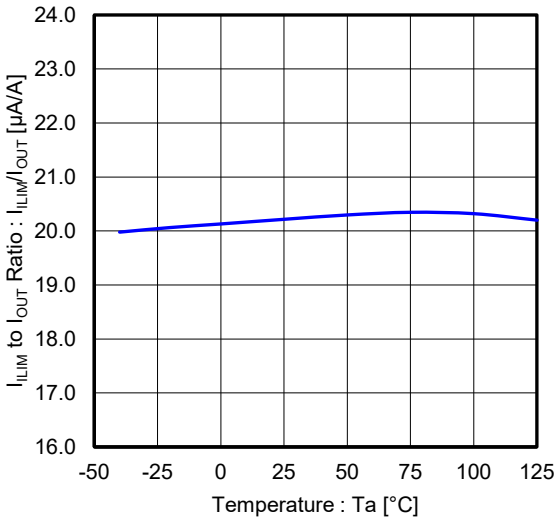


Figure 29. I_{ILIM} to I_{OUT} Ratio vs Temperature

Typical Performance Curves – continued

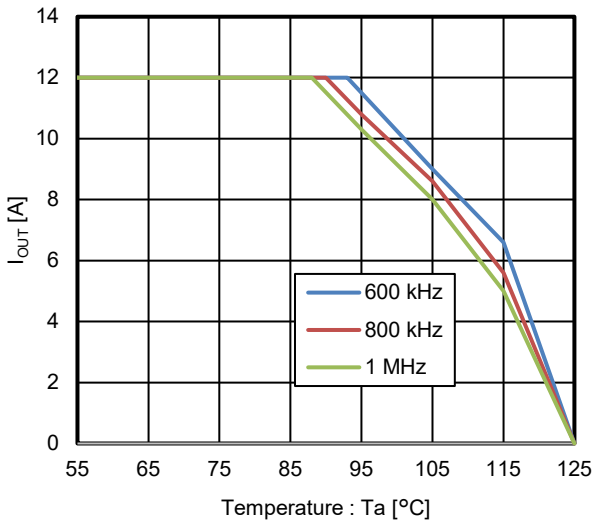


Figure 30. Thermal Derating
(V_{IN} = 12 V, V_{OUT} = 1.2 V)*(Note 1)*

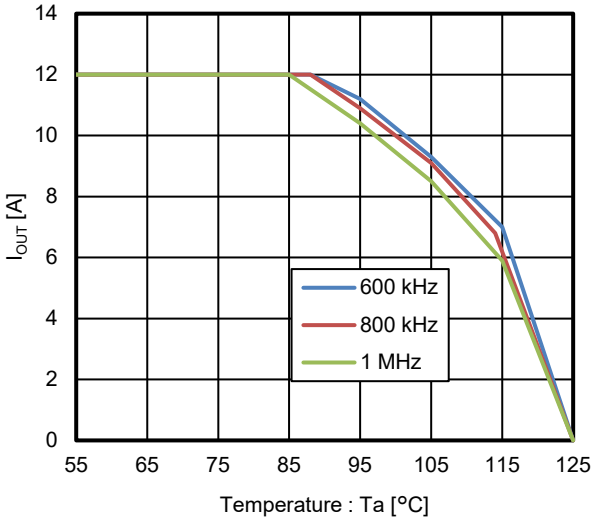


Figure 31. Thermal Derating
(V_{IN} = 12 V, V_{OUT} = 1.8 V)*(Note 1)*

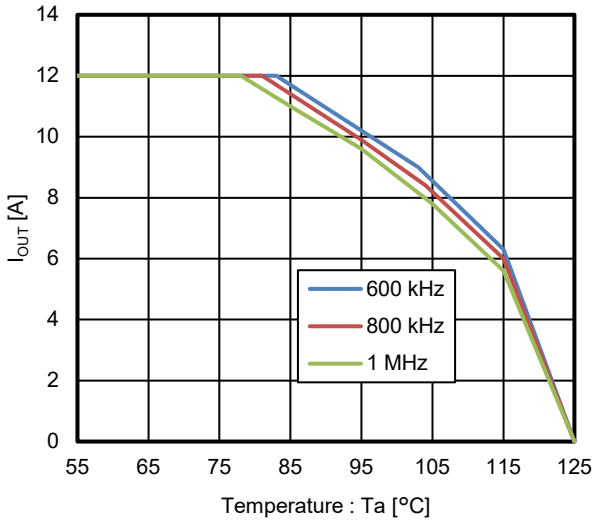


Figure 32. Thermal Derating
(V_{IN} = 12 V, V_{OUT} = 3.3 V)*(Note 1)*

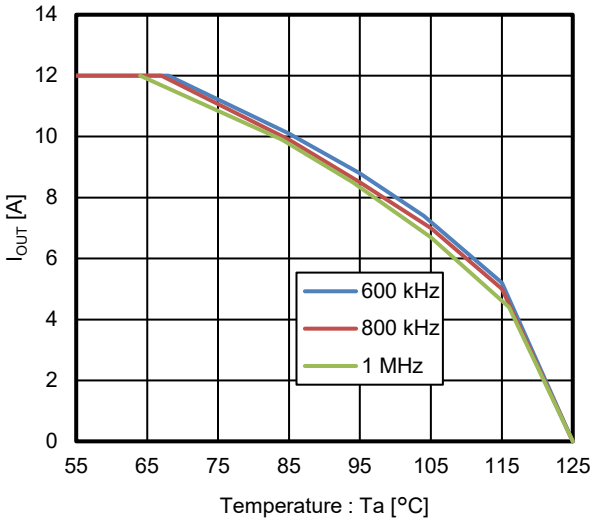


Figure 33. Thermal Derating
(V_{IN} = 12 V, V_{OUT} = 5.0 V)*(Note 1)*

(Note 1) Measured on FR-4 board 80.0 mm x 80.0 mm x 1.6 mm, Copper Thickness: All Layers 70 µm.

Typical Performance Curves – continued

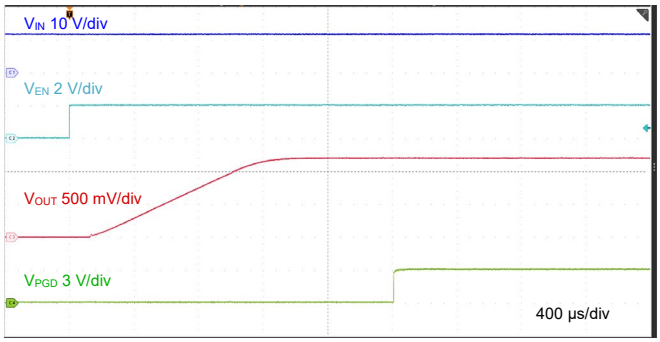


Figure 34. EN Start-up Waveform
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 6 A, CCM)

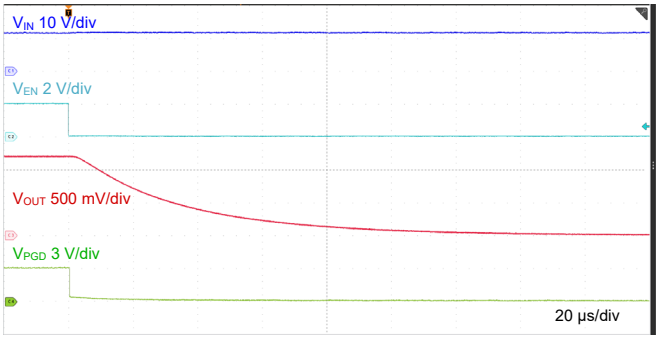


Figure 35. EN Shutdown Waveform
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 6 A, CCM)

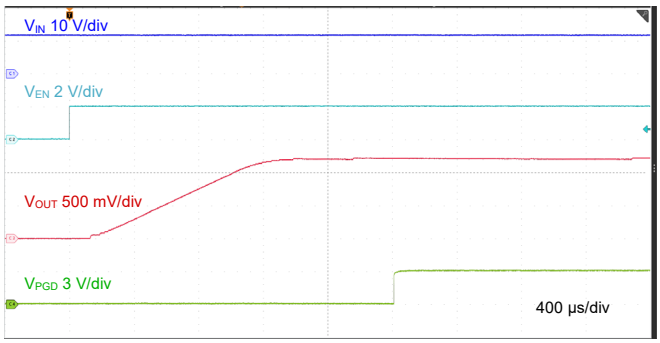


Figure 36. EN Start-up Waveform
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 0 A, LLM)

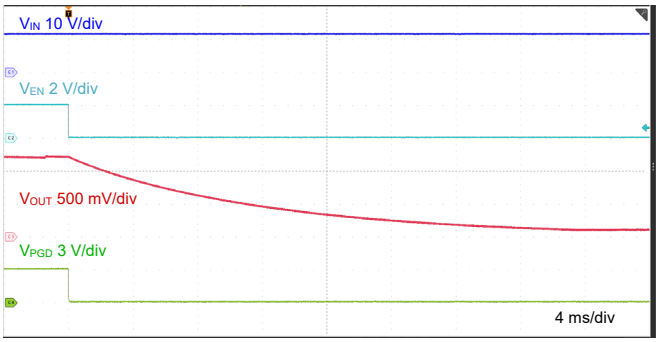


Figure 37. EN Shutdown Waveform
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 0 A, LLM)

Function Explanations

1. Basic Operation

(1) DC/DC Converter Operation

BD9DA00MF is a synchronous buck DC/DC converter that has original on-time control. The device operates with MODE pin setting. For the operation mode setting method, refer to Function Explanations 1. Basic Operation (11) Control Mode Selectable Function. When the operating mode is Light Load Mode (LLM), it utilizes switching operation in Continuous Conduction Mode (CCM) control for heavier load, and it operates in LLM control at lighter load to improve efficiency. When the operating mode is Forced CCM, the device operates in CCM control regardless of the output load.

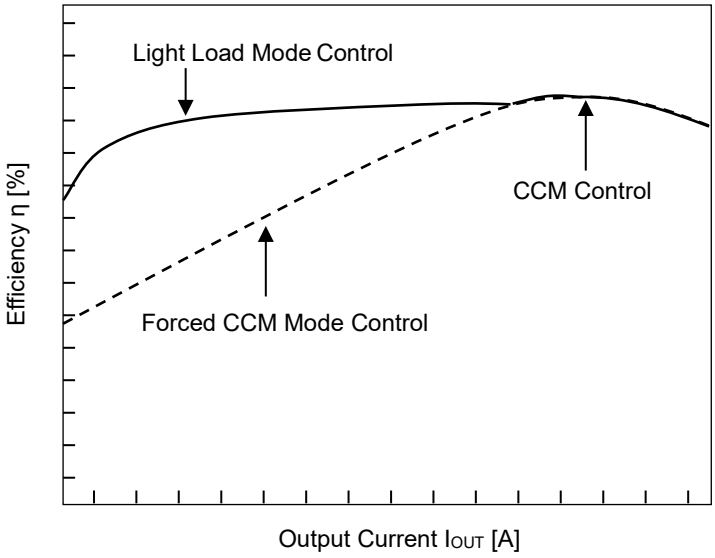


Figure 38. Efficiency Image between Light Load Mode Control and CCM Mode Control

(2) Enable Control

The start-up and shutdown can be controlled by the EN voltage (V_{EN}). When V_{EN} becomes 1.22 V (Typ) or more, the internal circuit is activated and the device starts up. When V_{EN} becomes 1.02 V (Typ) or less, the device shuts down. In the shutdown mode, the High-Side FET and the Low-Side FET are turned off and the SW pin is connected to GND through an internal discharge resistor R_{ON_DIS} = 70 Ω (Typ) and it discharges the output voltage V_{OUT} to 10 % (Typ) of the setting voltage.

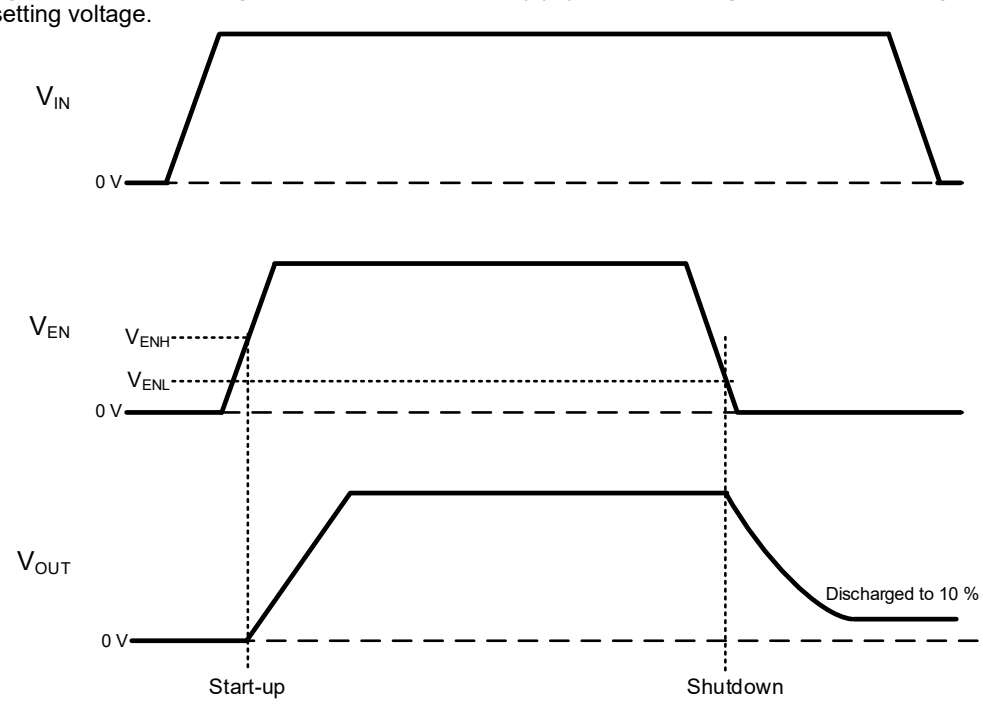


Figure 39. Start-up and Shutdown with Enable Control Timing Chart

1. Basic Operation – continued

(3) Soft Start

When the EN Voltage (V_{EN}) goes high, the soft start function operates and the output voltage gradually rises. This soft start function can prevent overshoot of the output voltage and excessive inrush current. The soft start time t_{SS} can be set by connecting a capacitor to the SS/REF pin. For the setting method, refer to Selection of Components Externally Connected 4. Soft Start Capacitor.

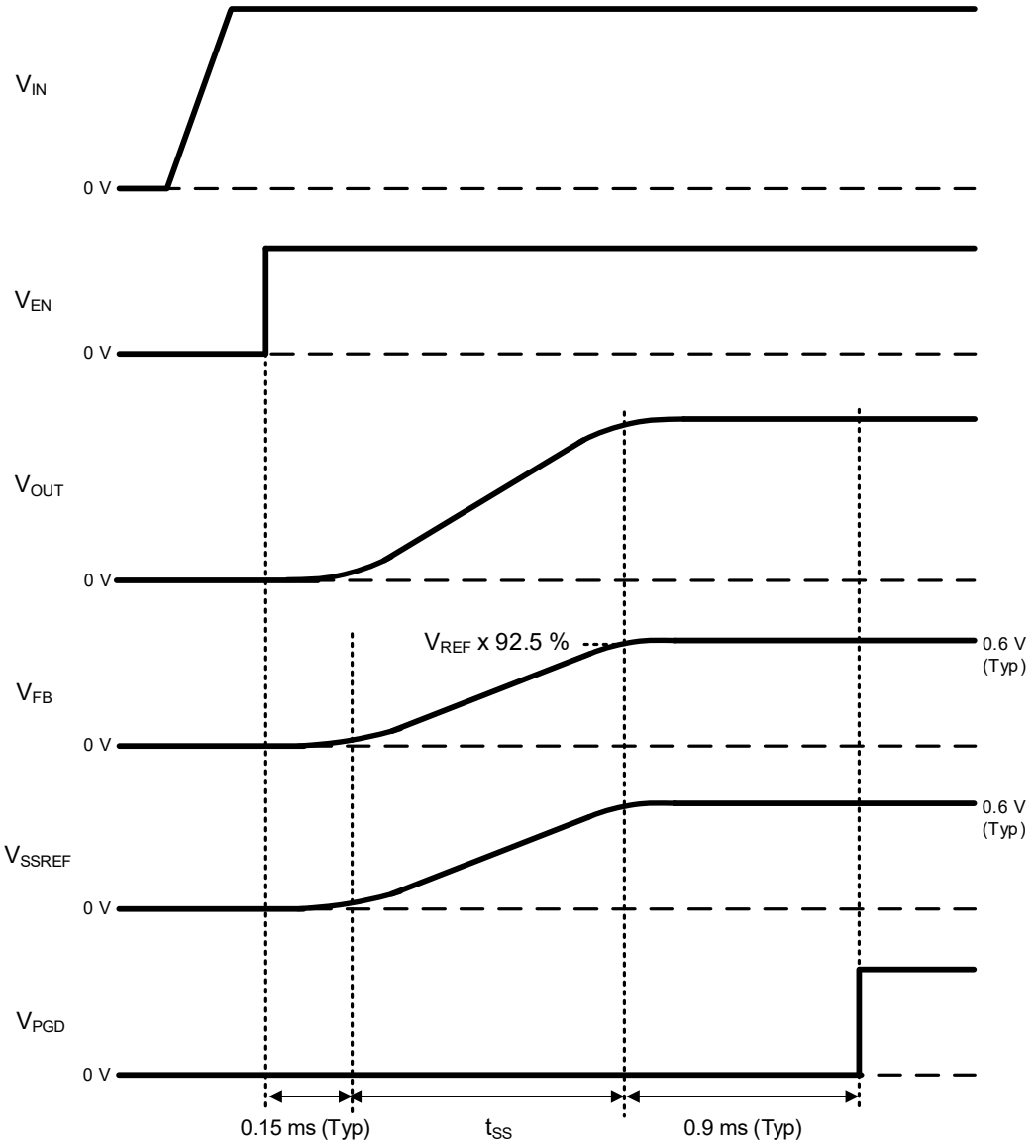


Figure 40. Soft Start Timing Chart

1. Basic Operation – continued

(4) Power Good

The power good function monitors the FB pin voltage (V_{FB}). It is recommended to connect the PGD pin to the VCC pin or a power supply of 5.5 V or less with a resistor of 1 kΩ to 100 kΩ. If the power good function is not used, this pin can be left floating or connected to the ground.

When V_{FB} becomes 92.5 % or more of the FB reference voltage V_{REF} 0.6 V (Typ) and keep the state for 0.9 ms (Typ), the open drain Nch MOSFET connected to the PGD pin is turned off and the PGD output goes Hi-Z (high impedance). When V_{FB} falls below 80 % of V_{REF} 0.6 V (Typ), the open drain Nch MOSFET is turned on and the PGD pin is pulled down with 15 Ω (Typ).

The power good function also operates when the output overvoltage is detected. When V_{FB} reaches 116 % (Typ) or more of V_{REF} 0.6 V (Typ), the open drain Nch MOSFET is latched in the ON state. The latched PGD output returns to Hi-Z and is pulled up after EN is toggled, or VIN UVLO or VCC UVLO is reset.

In the shutdown state (V_{EN} ≤ 0.7 V (Typ)) or VCC active state (0.8 V (Typ) ≤ V_{EN} ≤ 1.22 V (Typ) and V_{IN} < 2.0 V (Typ)), the PGD pin is clamped by the internal circuit. It is clamped to 600 mV (Typ) during pulled up to 3.3 V with 100 kΩ, and clamped to 700 mV (Typ) during pulled up to 3.3 V with 10 kΩ.

Table 1. PGD Output

State	Condition	PGD Output
Shutdown	V_{EN} ≤ 0.7 V (Typ)	Clamp
VCC Active 0.8 V (Typ) ≤ V_{EN} ≤ 1.22 V (Typ)	V_{IN} < 2.0 V (Typ)	Clamp
	V_{IN} ≥ 2.0 V (Typ)	Low (15 Ω Pull-down)
Enable V_{EN} ≥ 1.22 V (Typ)	V_{FB} / V_{REF} ≥ 92.5 % (Typ) for 0.9 ms (Typ)	High (3 MΩ Pull-down)
	Until PGD turns High	Low (15 Ω Pull-down)
OVP	Detect V_{FB} / V_{REF} ≥ 116 % (Typ)	Low (15 Ω Pull-down)
SCP	Detect V_{FB} / V_{REF} ≤ 80 % (Typ)	Low (15 Ω Pull-down)
UVLO	V_{IN} ≤ 1.85 V (Typ) or V_{CC} ≤ 2.5 V (Typ)	Low (15 Ω Pull-down)
TSD	Tj ≥ 175 °C (Typ)	Low (15 Ω Pull-down)

(5) Output Voltage Tracking Function

BD9DA00MF can be applied a reference voltage from an external power supply using the SS/REF pin. After the SS/REF pin voltage starts up to 0.6 V, it can be set in the range of 0.6 V to 1.4 V.

(6) Output Voltage Clamp Function (OVC)

When the FB pin voltage V_{FB} becomes V_{REF} x 104 % (Typ) or more, the Low-Side FET turns on and suppresses the output voltage rise. When V_{FB} becomes V_{REF} x 103 % (Typ) or less, it returns to normal operation. In the case of LLM setting, the device returns to the normal operating state after 15 times switching operation with CCM. The output voltage clamp function is enabled after the SS/REF pin voltage reaches 0.6 V (Typ).

(7) QuiCur™

QuiCur™ is a combination of technologies that provides fast load response. This technology reduces the amount of output voltage change in response to transient changes in load current. It also reduces the capacitance of output capacitors required for power supply ICs, thereby reducing the number of components and the board mounting area.

(8) Nano Pulse Control™

Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition.

(9) Bootstrap Capacitor Charge Function

The Low-Side FET turns on and charges to a bootstrap capacitor when the voltage between SW and BST (ΔV_{BST-SW}) becomes 2.1 V (Typ) or less.

(10) Output Discharge Function

When the device shuts down from the operating state by enable control, the internal discharge resistor R_{ON_DIS} = 70 Ω (Typ) connected to the SW pin turns ON and discharges the output voltage V_{OUT} to 10 % (Typ) of the setting voltage.

1. Basic Operation – continued

(11) Control Mode Selectable Function

BD9DA00MF has the MODE pin to set the switching frequency and operation mode. It cannot be changed during operation.

Table 2. Control Mode Setting

MODE Pin Condition	Switching Frequency	Operation Mode
Short to VCC	600 kHz (Typ)	Light Load Mode (LLM)
240 kΩ to GND	800 kHz (Typ)	Light Load Mode (LLM)
120 kΩ to GND	1 MHz (Typ)	Light Load Mode (LLM)
Short to GND	600 kHz (Typ)	Forced CCM Mode
30 kΩ to GND	800 kHz (Typ)	Forced CCM Mode
62 kΩ to GND	1 MHz (Typ)	Forced CCM Mode

(12) External Bias On VCC Pin Function

VCC outputs 3.0 V (Typ) from the internal LDO, it can also be applied externally. External bias improves efficiency and allows operation at 2.7 V ≤ V_{IN} ≤ 4.0 V.

When applying an external bias on the VCC pin, please note the following.

·The externally applied voltage V_{CC_EXT} should be 3.13 V ≤ V_{CC_EXT} ≤ 3.60 V.

·It should be enabled in a sequence where external application on the VCC pin completes before either the start-up by EN signal or VIN UVLO release.

(13) Remote Sense Function

BD9DA00MF has a remote sense function using the FB and RGND pins. The remote sense function compensates for output voltage drop due to the PCB wiring resistance. When this function is available, the V_{OUT} connection of the remote sensing signal $V_{OUTSNS+}$ must be connected to the feedback resistor R_{UP}. The ground connection of the remote sensing signal $V_{OUTSNS-}$ must be connected to the RGND pin. To maintain stable output voltage and minimize the ripple voltage, the pair of remote sensing lines must stay away from any noise sources such as inductor, SW nodes, and high frequency clock lines. In addition, connect a capacitor C_{RGND} of 0.1 µF or more between $V_{OUTSNS+}$ and $V_{OUTSNS-}$. In this case, It is recommended that R_{UP}, R_{DOWN}, C_{FB}, and C_{RGND} are placed at nearby BD9DA00MF. If the remote sense function is not used, RGND should be shorted to AGND with shortest trace. In this case C_{SS1} can be deleted, but C_{SS2} can be set within the range described in Selection of Components Externally Connected 4. Soft Start Capacitor.

It is recommended to use the RGND pin with an operating range of -50 mV to +50 mV.

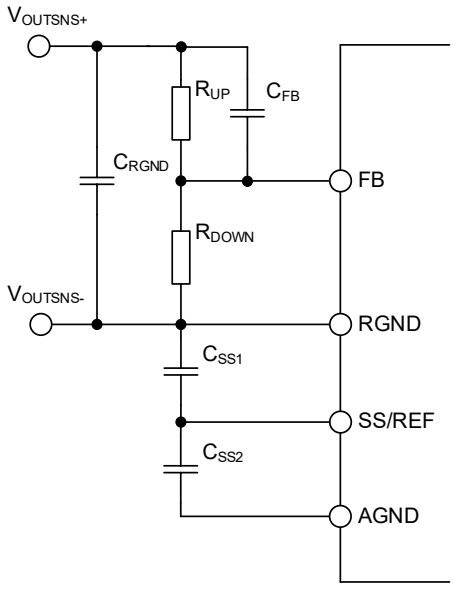


Figure 41. Circuit with Remote Sense Function

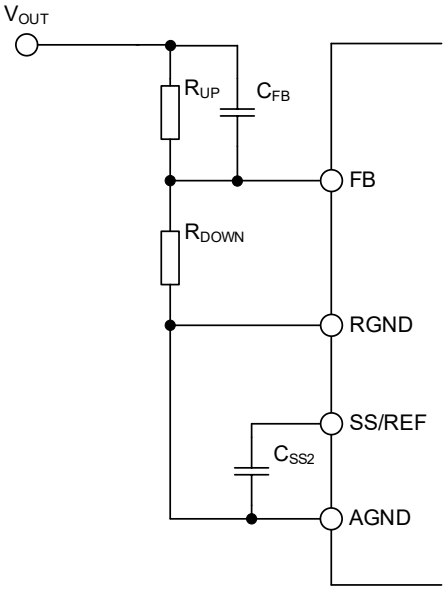


Figure 42. Circuit when Remote Sense Function is not used

Function Explanations – continued

2. Protection

(1) Over Current Protection (OCP) / Short Circuit Protection (SCP)

Over Current Protection (OCP) restricts the flowing current through the Low-Side FET and the High-Side FET for every switching period. When the Low-Side FET is on, the Low-Side FET remains on while the inductor current is more than the Low-Side OCP setting value I_{LOCP}. When the inductor current becomes I_{LOCP} or less, the device can turn on the High-Side FET. For I_{LOCP} settings, refer to the Selection of Components Externally Connected 7. OCP Setting Resister. When the inductor current becomes the High-Side OCP I_{HOCP} = 17.5 A (Typ) or more while the High-Side FET is on, the High-Side FET is turned off. Output voltage may decrease by changing frequency and duty due to the OCP operation.

Short Circuit Protection (SCP) function is a Hiccup mode. After 3 ms (Typ) from the beginning of soft start, and after SS/REF voltage (V_{SSREF}) reaches 0.6 V (Typ), if V_{FB} is 80 % (Typ) of FB reference voltage V_{REF} or less, or over current protection is detected for 31 consecutive cycles, the device shuts down for 117 ms (Typ), and then the device restarts. Do not exceed the maximum junction temperature (Tjmax = 125 °C) during OCP and SCP operation.

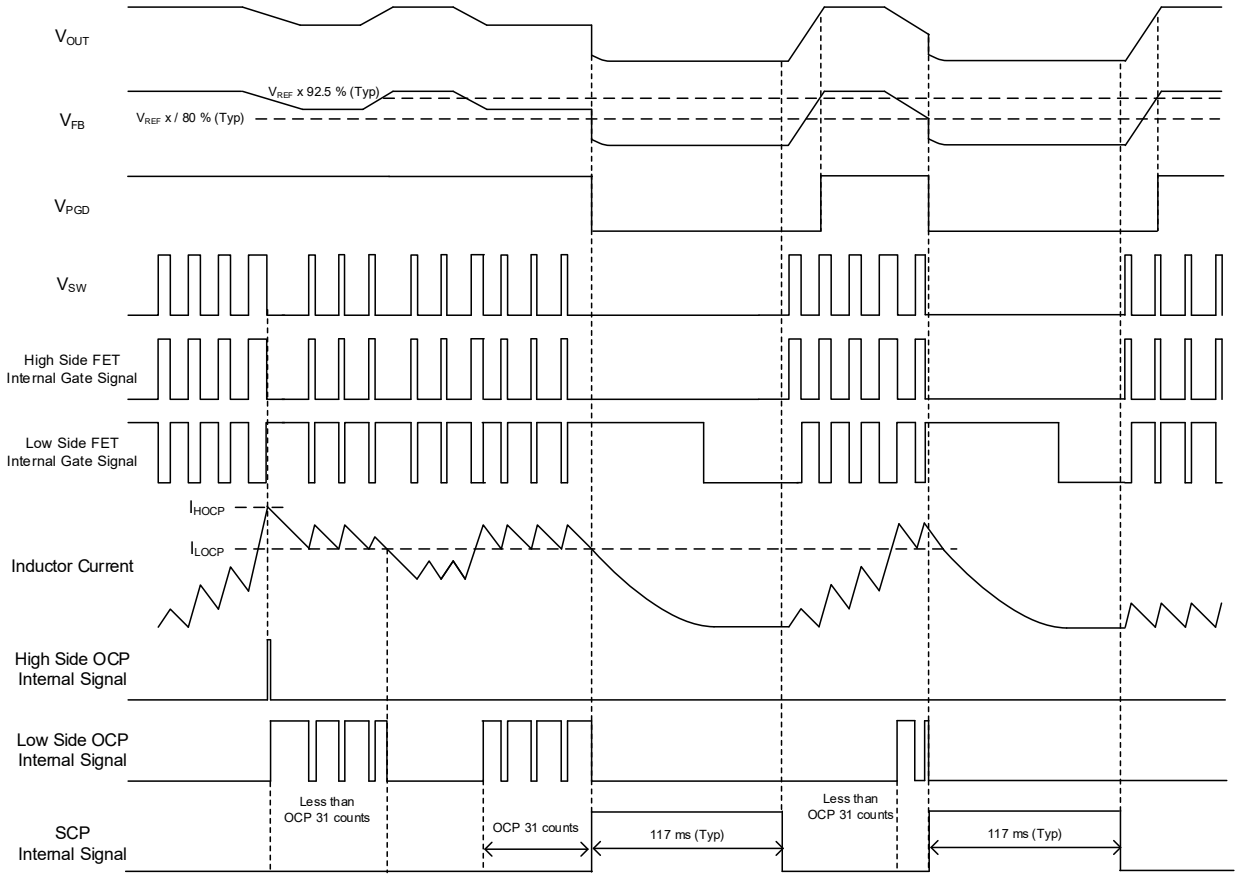


Figure 43. OCP and SCP Timing Chart

2. Protection – continued

(2) Low-Side Reverse Over Current Protection (ROCP)

While Low-Side FET is ON in the Forced CCM setting, if the inductor current exceeds the reverse detection current I_{ROCP} = 6.5 A (Typ), Low-Side FET is turned OFF and High-Side FET is turned ON.

(3) Under Voltage Lockout Protection (UVLO)

The device shuts down when the input voltage V_{IN} falls to 1.85 V (Typ) or less, or VCC voltage V_{CC} is 2.5 V (Typ) or less. It starts up when V_{IN} becomes 2.4 V (Typ) or more and V_{CC} becomes 2.8 V (Typ) or more. The hysteresis is 550 mV (Typ) and 300 mV (Typ), respectively.

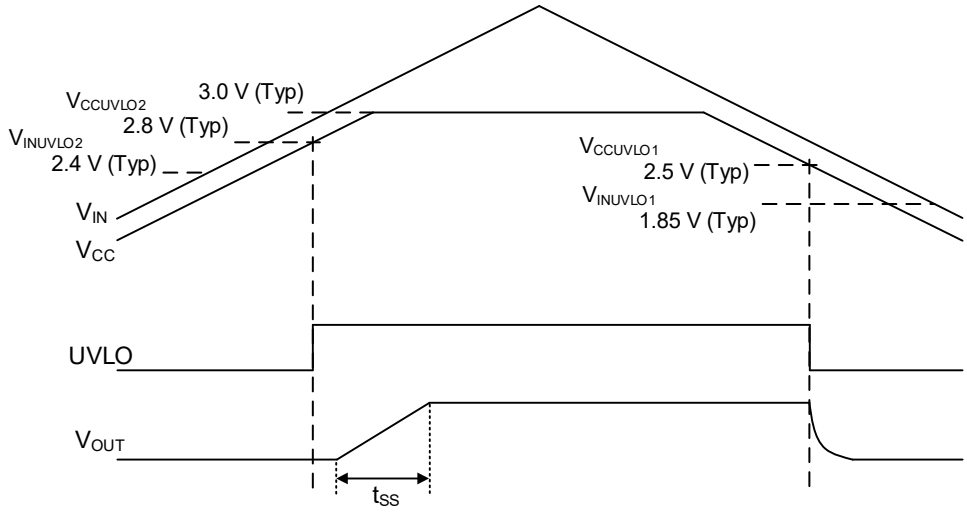


Figure 44. UVLO Timing Chart

(4) Thermal Shutdown Protection (TSD)

The thermal shutdown circuit prevents heat damage to the IC. If the junction temperature (Tj) exceeds the TSD detection temperature (175 °C, Typ), the output MOSFETs are turned off. When the Tj falls below the TSD release temperature (150 °C, Typ), the IC restarts up with soft start. The input voltage required for the restart is the same as that for the initial startup (Input voltage 4.0 V or more). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings. Therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

(5) Over Voltage Protection (OVP)

The overvoltage protection (OVP) is enabled after the SS/REF pin voltage reaches 0.6 V (Typ). OVP function operates when the FB pin voltage V_{FB} becomes 116 % (Typ) or more of the FB reference voltage V_{REF}, and it depends on the device operation mode.

During Forced CCM mode operation, after the device detects OVP, it latches off the High-Side FET and turns on the Low-Side FET. However, when the current flowing through the Low-Side FET reaches reverse detection current I_{ROCP}, the Low-Side FET is temporarily turned off and the High-Side FET is turned on for an ONTIME determined by the input/output status. After that, the Low-Side FET returns to the latched-on state.

During LLM mode operation, after the device detects OVP, it turns off the High-Side FET and turns on the Low-Side FET. When the Low-Side FET turns on, the output voltage decreases, and if V_{FB} falls below 50% (Typ) of V_{REF}, both the High-Side FET and Low-Side FET latch off. However, before V_{FB} falls below 50 % (Typ) of V_{REF}, when the current flowing through the Low-Side FET reaches I_{ROCP}, the Low-Side FET is temporarily turned off and the High-Side FET is turned on for an ONTIME determined by the input/output status. After that, the Low-Side FET returns to the on state. The device repeats this operation until V_{FB} is less than 50 % (Typ) of V_{REF}.

During both Forced CCM and LLM mode operation, the device resets the latched state by toggling EN or by detecting VIN UVLO or VCC UVLO.

Selection of Components Externally Connected

If you use settings other than the recommended constants shown in the application circuit examples, please contact our company.

1. Input Capacitor

Use ceramic type capacitor for the input capacitor. The input capacitor is used to reduce the input ripple noise and it is effective to be placed as close to the VIN pin as possible. Set the capacitor value so that it does not fall to 10 µF considering the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. The PCB layout and the position of the capacitor may lead to IC malfunction. Refer to the notes on the PCB layout when designing PCB layout. In addition, the capacitor with value 0.1 µF or 1 µF can be connected as close to the VIN pin and the PGND pin as possible in order to reduce the high frequency noise.

2. Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. For recommended inductance, use the values listed in Table 3.

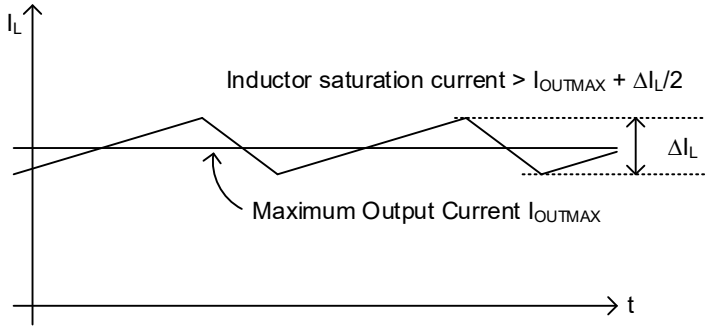


Figure 45. Waveform of Inductor Current

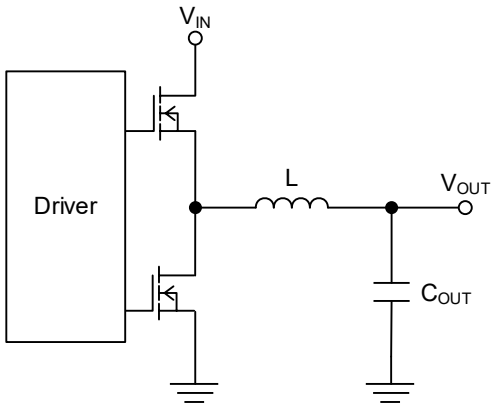


Figure 46. Output LC Filter Circuit

For example, given that V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 0.33 µH, and the switching frequency f_{SW} = 800 kHz, Inductor current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L} = 4.09 \text{ [A]}$$

The rated current of the inductor (Inductor saturation current) must be larger than the sum of the maximum output current I_{OUTMAX} and 1/2 of the inductor ripple current ΔI_L. The inductor peak current, which is value obtained by adding 1/2 of ΔIL to I_{OUTMAX} should be 15.5 A or less.

Use ceramic type capacitors for the output capacitor C_{OUT}.
C_{OUT} affects the output ripple voltage. Select C_{OUT} so that it must satisfy the required ripple voltage characteristics. The output ripple voltage can be estimated by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

where:
R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

For example, given that C_{OUT} = 47 µF and R_{ESR} = 3 mΩ in 4 parallel, ΔV_{RPL} can be calculated as below.

$$\Delta V_{RPL} = 4.09\ A \times \left(3\ m\Omega/4 + \frac{1}{8 \times 47\ \mu F \times 4 \times 800\ kHz} \right) = 6.5 \text{ [mV]}$$

2. Output LC Filter – continued

The total maximum effective capacitance connected to V_{OUT} needs to satisfy the value obtained by the following equation.

$$C_{OUTMAX} < \frac{t_{SSMIN}}{V_{OUT}} \times (I_{OUTMAX} + \frac{\Delta I_L}{2} - I_{OUTSS}) \text{ [F]}$$

where:
t_{SSMIN} is the minimum soft start time.
V_{OUT} is the output voltage.
I_{OUTMAX} is the maximum output current.
ΔI_L is the inductor current.
I_{OUTSS} is the maximum output current during soft start.

For example, given that V_{IN} = 12 V, V_{OUT} = 1.2 V, L = 0.33 µH, f_{SW} = 800 kHz, t_{SSMIN} = 0.75 ms, I_{OUTMAX} = 12 A, and I_{OUTSS} = 12 A, C_{OUTMAX} can be calculated as below.

$$C_{OUTMAX} < \frac{0.75\ ms}{1.2\ V} \times (12\ A + \frac{4.09\ A}{2} - 12\ A) = 1278 \text{ [µF]}$$

If the total capacitance connected to V_{OUT} is larger than C_{OUTMAX}, Over Current Protection may be activated by the inrush current at startup and prevented to turn on the output. Confirm this on the actual application.

In addition, the minimum effective value of the output capacitor (C_{OUTMIN}) should be within the range that satisfies the following equation.

$$1 + \left[\left\{\frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} + \frac{(\Delta I_{OUT} + \frac{\Delta I_L}{2}) \times L}{2 \times V_{OUT}}\right\} \times \left(I_{OUT} + \frac{\Delta I_L}{2}\right) - \frac{\Delta t \times \Delta I_{OUT}}{2}\right] \times \frac{1}{C_{OUTMIN} \times V_{OUT}} \leq 1.1$$

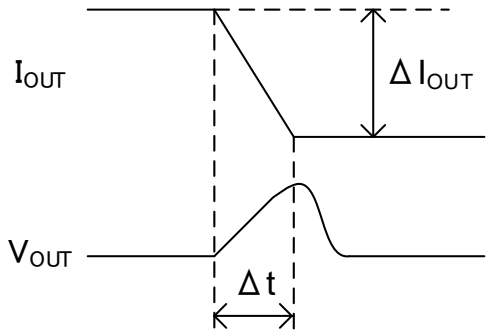


Figure 47. Waveform at Output Current Variation

where:
ΔI_{OUT} is the output current variation.
Δt is the output current variation time.
C_{OUTMIN} is the minimum effective value of the output capacitor.

When a capacitance smaller than C_{OUTMIN} is connected to V_{OUT}, OVP is detected by output variation during the transient response. When OVP is detected, Low-Side FET latches to the on state. Confirm this on the actual application.

Selection of Components Externally Connected – continued

3. Output Voltage Setting

The output voltage can be set by the feedback resistance ratio connected to the FB pin and the RGND pin.

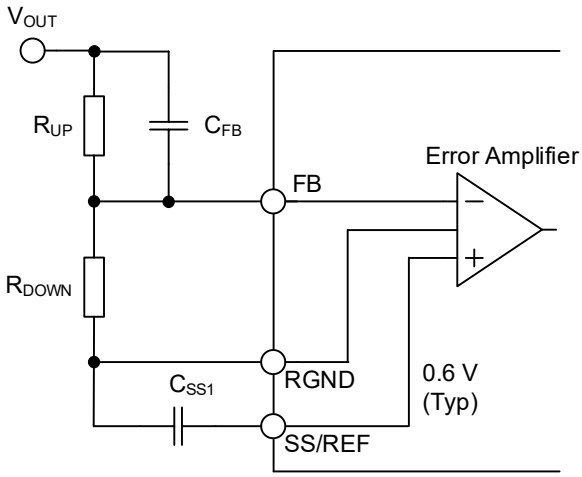


Figure 48. Feedback Resistor Circuit

The output voltage V_{OUT} can be calculated as below.

$$V_{OUT} = \frac{R_{UP}+R_{DOWN}}{R_{DOWN}} \times 0.6 \text{ [V]}$$

$$0.6 \leq V_{OUT} \leq 5.5 \text{ [V]}$$

However, R_{DOWN} should be set within the following formula.

$$R_{DOWN} \leq 10 \text{ [k}\Omega\text{]}$$

V_{OUT} should be used to satisfy the conditions of the following equation.

600 kHz : $V_{OUT} \leq (V_{IN} \times 0.86) - 0.095 \times I_{OUT}$ [V]

800 kHz : $V_{OUT} \leq (V_{IN} \times 0.82) - 0.095 \times I_{OUT}$ [V]

1 MHz : $V_{OUT} \leq (V_{IN} \times 0.78) - 0.095 \times I_{OUT}$ [V]

FB capacitor C_{FB} is optional. The device improves load response by connecting C_{FB}.
Load transient response and the loop stability depend on L, C_{OUT}, R_{UP}, R_{DOWN}, and C_{FB}. Actually, these characteristics may change depending on PCB layout, wiring, the type of components, and the conditions (temperature, etc.). Be sure to check them on the actual application. For recommended C_{FB}, use the values listed in Table 3.

Table 3. Recommended component constants and minimum effective output capacitance for each setting.

V_{IN} [V]	V_{OUT} [V]	Switching Frequency [kHz]	I_{OUTMAX} [A]	L_{TYP} [µH]	R_{UP} [kΩ]	R_{DOWN} [kΩ]	C_{FB_TYP} [pF]	C_{OUTMIN_EFF} *(Note 1)* [µF]
5	1.2	600	12	0.47	1.5	1.5	2200	170
5	3.3	600	10	0.47	6.8	1.5	68	170
12	1.2	600	12	0.47	1.5	1.5	2200	170
12	3.3	600	12	1	6.8	1.5	270	170
12	5	600	12	1.4	11	1.5	150	110
5	1.2	800	12	0.33	1.5	1.5	2200	135
5	3.3	800	8	0.33	6.8	1.5	100	135
12	1.2	800	12	0.33	1.5	1.5	2200	135
12	3.3	800	12	0.68	6.8	1.5	270	135
12	5	800	12	1	11	1.5	150	85
5	1.2	1000	12	0.25	1.5	1.5	2200	135
5	3.3	1000	6	0.33	6.8	1.5	180	135
12	1.2	1000	12	0.33	1.5	1.5	2200	135
12	3.3	1000	12	0.68	6.8	1.5	270	135
12	5	1000	12	0.68	11	1.5	150	85

(Note 1) Minimum effective capacitance of the output capacitor.

Selection of Components Externally Connected – continued

4. Soft Start Capacitor (Soft Start Time Setting)

The soft start time depends on the value of the capacitor connected to the SS/REF pin. By connecting a capacitor C_{SS} to the SS/REF pin, the soft start time can be set to t_{SS_EXT}, which is longer than t_{SS} = 1 ms (Typ). The t_{SS_EXT}, C_{SS1} (SS/REF pin to RGND pin), and C_{SS2} (SS/REF pin to AGND pin) can be calculated using below equation. C_{SS} (the sum of C_{SS1} and C_{SS2}) should be set between 1000 pF and 1 µF.

$$t_{SS\_EXT} = \frac{C_{SS} \times 0.6}{I_{SS\_SO}} \text{ [s]}$$

$$C_{SS} = C_{SS1} + C_{SS2} \text{ [F]}$$

where:
I_{SS_SO} is SS/REF Source Current 36 µA (Typ)

With C_{SS1} = 0.22 µF, C_{SS2} = 0.022 µF, t_{SS_EXT} can be calculated as below.

$$t_{SS\_EXT} = \frac{(0.22\ \mu F + 0.022\ \mu F) \times 0.6}{36\ \mu A} = 4.03 \text{ [ms]}$$

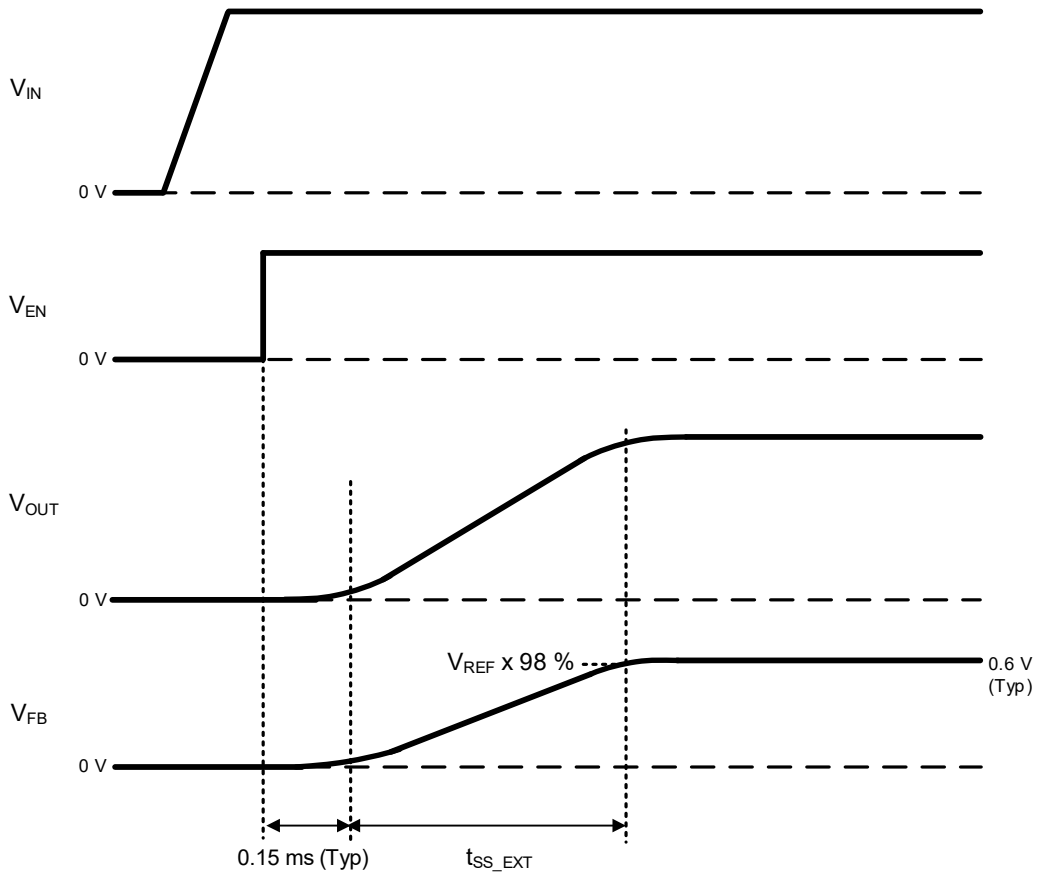


Figure 49. Adjustable Soft Start Timing Chart

Selection of Components Externally Connected – continued

5. VCC Capacitor

The VCC capacitor 1 µF is recommended. Connect the capacitor between the VCC pin and ground. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the effective capacitance of no less than 0.33 µF.

6. Bootstrap Capacitor

The bootstrap capacitor 0.1 µF is recommended. Connect the capacitor between the SW pin and the BST pin. For the capacitance, take temperature characteristics, DC bias characteristics, and etc. into consideration to set to the effective capacitance of no less than 0.022 µF.

7. OCP Setting Resistor

Low-Side OCP limits the valley of the inductor current. The OCP setting value I_{LOCP} can be set by the resistance R_{ILIM} of the ILIM pin to AGND.

When the Low-Side FET is on, the device monitors the inductor current and outputs 20 µ (Typ) times the current I_{ILIM} from the ILIM pin. While the multiple of I_{ILIM} current and R_{ILIM} exceeds the current limit threshold V_{LIM} 1.2 V (Typ), the Low-Side FET remains on even if FB voltage V_{FB} falls to 0.6 V (Typ) or less. If the multiple of I_{ILIM} current and R_{ILIM} becomes 1.2 V (Typ) or less, the High-Side FET is able to be turned on. I_{LOCP} can be calculated using the following formula. Set the R_{ILIM} value in the range of 4.7 kΩ to 10 kΩ. Also, set the peak inductor current I_{L_PEAK}, which is I_{LOCP} plus ΔI_L, so that it does not exceed $I_{L\_PEAKMAX}$ = 18 A.

$$I_{LOCP} = \frac{V_{LIM}}{I_{ILIM}/I_{OUT} \times R_{ILIM}} \text{ [A]}$$

where:
V_{LIM} is the current limit threshold 1.2 V (Typ)
I_{ILIM}/I_{OUT} is I_{ILIM} to I_{OUT} ratio 20 µA/A (Typ)

The OCP setting I_{OCP} of the output current is the value of I_{LOCP} plus 1/2 of ΔI_L. R_{ILIM} can be calculated from the target I_{OCP} using the following formula.

$$R_{ILIM} = \frac{V_{LIM}}{I_{ILIM}/I_{OUT}} \div \left(I_{OCP} - \frac{\Delta I_L}{2}\right) \text{ [Ω]}$$

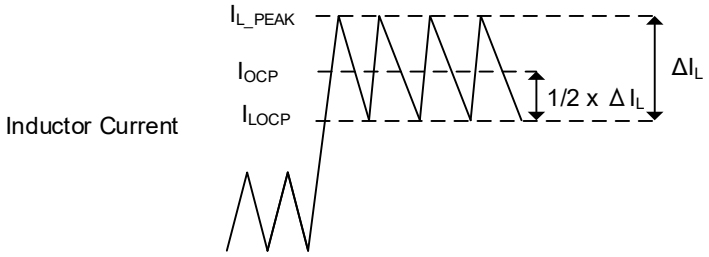


Figure 50. Inductor Current Waveform during OCP

8. EN Pull up Resistor

EN can also be connected to VIN directly through a pull-up resistor R_{ENUP}. R_{ENUP} should be selected so that the current flow to EN is 50 µA or less. R_{ENUP} can be calculated with the following formula.

$$R_{ENUP} > \frac{V_{IN}}{0.05} \text{ [kΩ]}$$

Application Characteristic Data(Reference Data)

Table 4. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	8 V to 16 V
Output Voltage	V_{OUT}	1.2 V (Typ)
Maximum Output Current	I_{OUTMAX}	12 A
Switching Frequency	f_{SW}	800 kHz (Typ)
Operation Mode	-	LLM Mode
Operating Temperature	Ta	25 °C

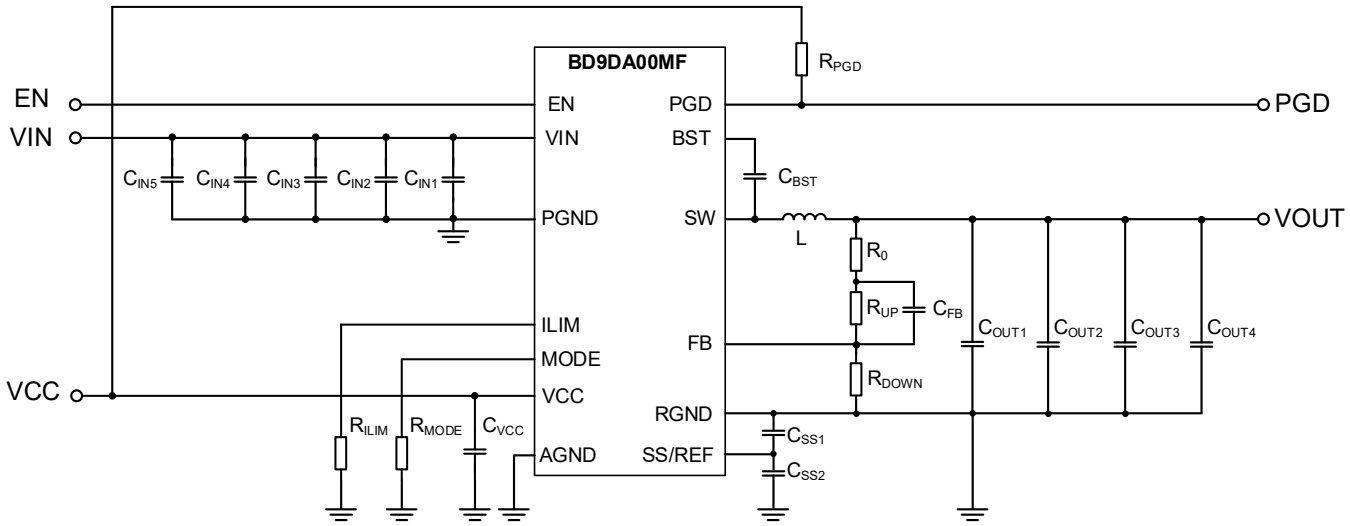


Figure 51. Application Circuit

Table 5. List of Components (Reference Example)

Part No.	Value	Part Name	Type	Size Code (mm)	Manufacturer
L	0.33 µH	SPM6550CT-R33L	Inductor	-	TDK
C_{IN1} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN2} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN3}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN4}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN5}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{OUT1}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT2}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT3}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT4}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{VCC}	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{BST}	0.1 µF, (X7R, 25 V)	GRM155R71E104KE14	Ceramic Capacitor	1005	Murata
C_{SS1}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{SS2}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{FB} *(Note 2)*	2200 pF, (X7R, 50 V)	GRM155R71H222KA01	Ceramic Capacitor	1005	Murata
R_{ILIM}	5.1 kΩ, (1 %, 1/16 W)	MCR01SMQPF5101	Chip Resistor	1005	ROHM
R_{MODE}	240 kΩ, (1 %, 1/16 W)	MCR01SMQPF2403	Chip Resistor	1005	ROHM
R_{PGD}	10 kΩ, (1 %, 1/16 W)	MCR01SMQPF1002	Chip Resistor	1005	ROHM
R_0 *(Note 3)*	Short	-	-	-	-
R_{UP}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM
R_{DOWN}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 1 µF ceramic capacitor C_{IN1}, C_{IN2} as close to the VIN pin and the PGND pin as possible.
(Note 2) C_{FB} is option, used to adjust the frequency response. If you are using a value other than those listed in Table 3, please confirm with the actual application.
(Note 3) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

Application Characteristic Data (Reference Data) – continued

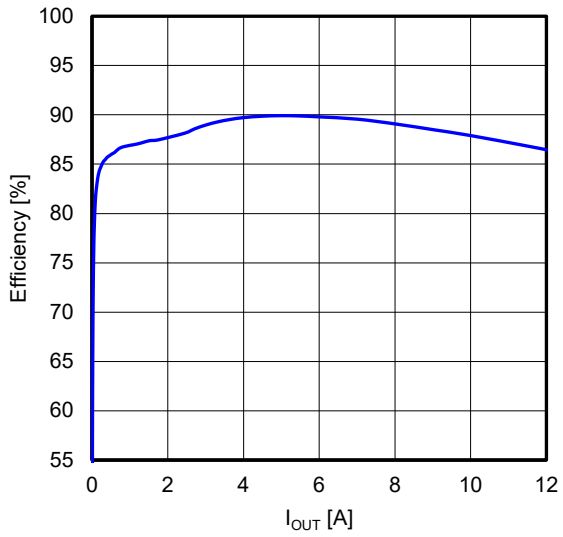


Figure 52. Efficiency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, LLM)

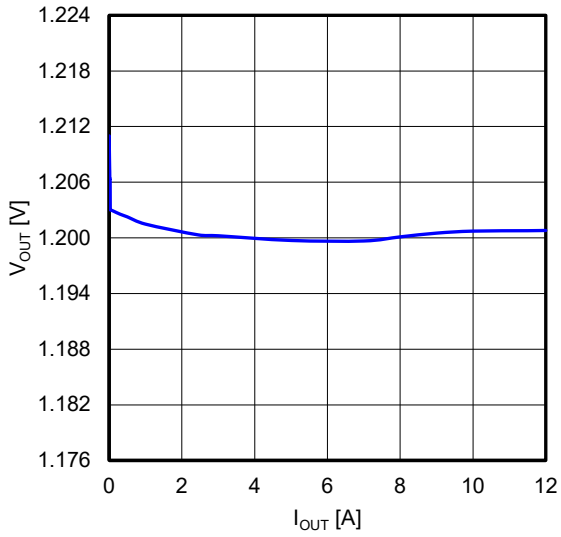


Figure 53. Load Regulation
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, LLM)

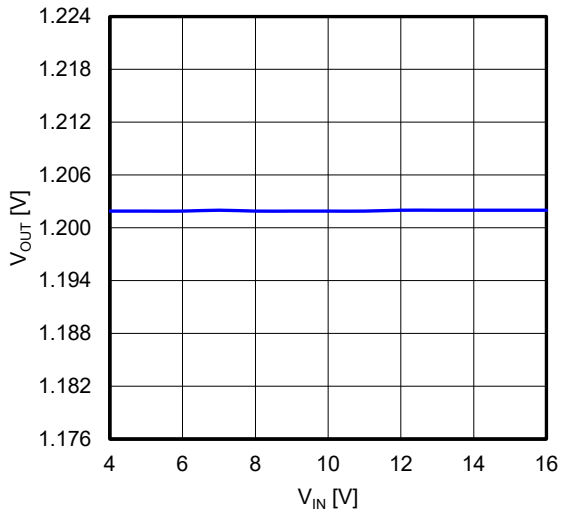


Figure 54. Line Regulation
(V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 0.1 A, LLM)

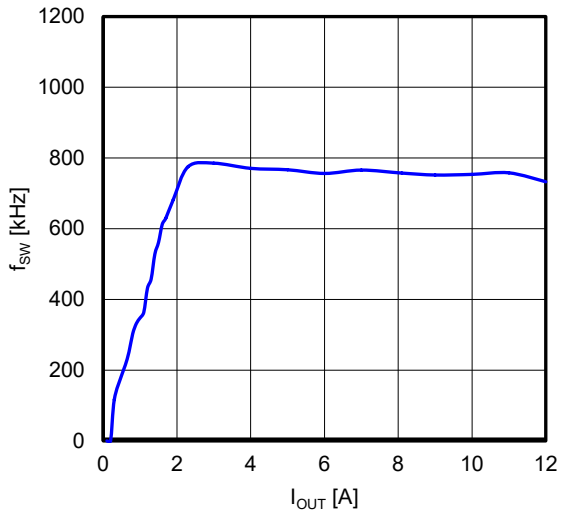


Figure 55. Switching Frequency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, LLM)

Application Characteristic Data (Reference Data) – continued

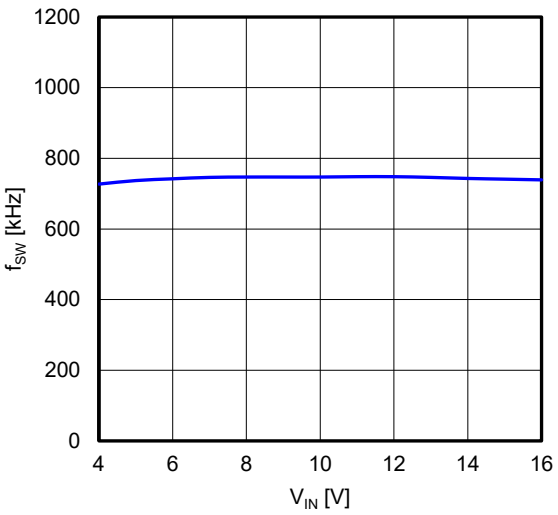


Figure 56. Switching Frequency vs Input Voltage
(V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 800 kHz, LLM)

Figure 57. Frequency Characteristics
(V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 800 kHz, LLM)

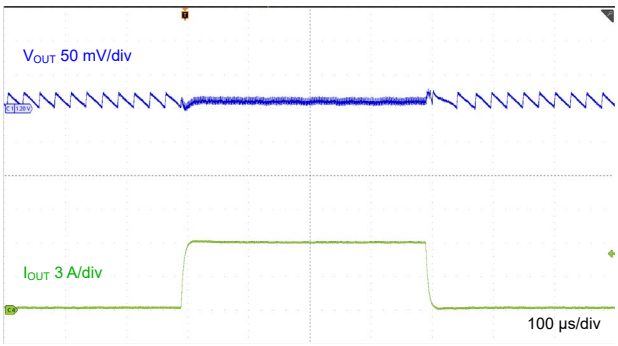


Figure 58. Load Transient Response
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, LLM,
I_{OUT} = 0.1 A to 6 A : 1 A/µs)

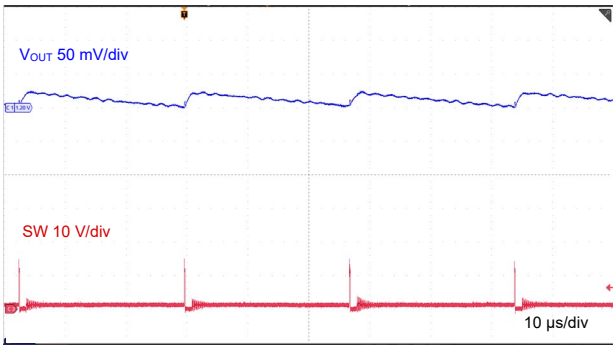


Figure 59. Output Ripple Voltage
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 0.1 A, LLM)

Application Characteristic Data (Reference Data) – continued

Table 6. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	8 V to 16 V
Output Voltage	V_{OUT}	1.2 V (Typ)
Maximum Output Current	I_{OUTMAX}	12 A
Switching Frequency	f_{SW}	800 kHz (Typ)
Operation Mode	-	Forced CCM Mode
Operating Temperature	Ta	25 °C

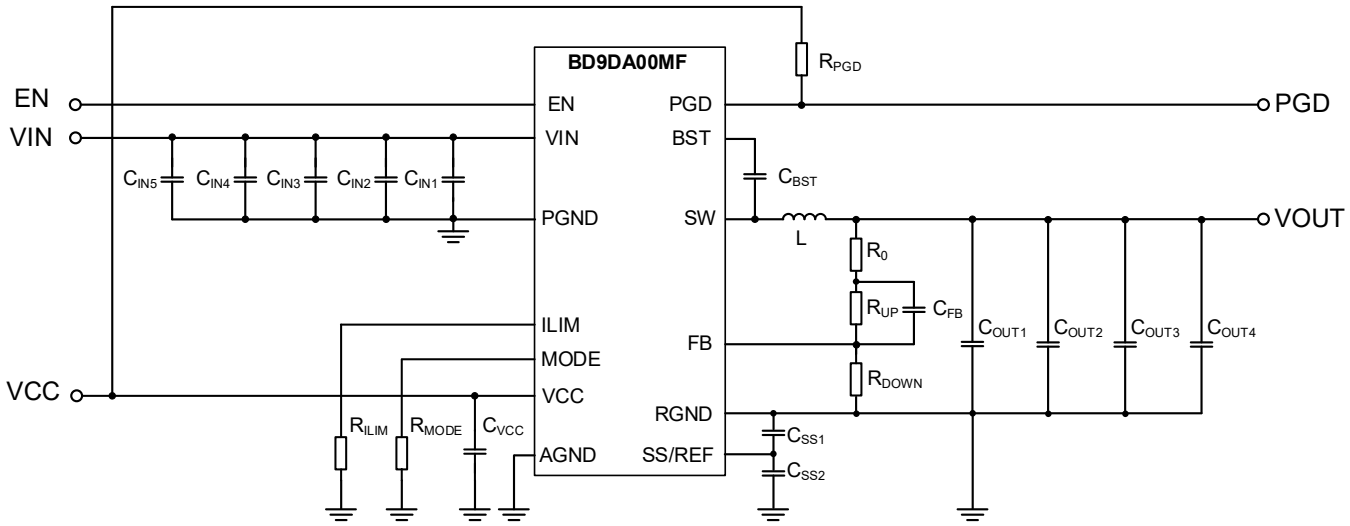


Figure 60. Application Circuit

Table 7. List of Components (Reference Example)

Part No.	Value	Part Name	Type	Size Code (mm)	Manufacturer
L	0.33 µH	SPM6550CT-R33L	Inductor	-	TDK
C_{IN1} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN2} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN3}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN4}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN5}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{OUT1}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT2}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT3}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT4}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{VCC}	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{BST}	0.1 µF, (X7R, 25 V)	GRM155R71E104KE14	Ceramic Capacitor	1005	Murata
C_{SS1}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{SS2}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{FB} *(Note 2)*	2200 pF, (X7R, 50 V)	GRM155R71H222KA01	Ceramic Capacitor	1005	Murata
R_{ILIM}	5.1 kΩ, (1 %, 1/16 W)	MCR01SMQPF5101	Chip Resistor	1005	ROHM
R_{MODE}	30 kΩ, (1 %, 1/16 W)	MCR01SMQPF3002	Chip Resistor	1005	ROHM
R_{PGD}	10 kΩ, (1 %, 1/16 W)	MCR01SMQPF1002	Chip Resistor	1005	ROHM
R_0 *(Note 3)*	Short	-	-	-	-
R_{UP}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM
R_{DOWN}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 1 µF ceramic capacitor C_{IN1}, C_{IN2} as close to the VIN pin and the PGND pin as possible.
(Note 2) C_{FB} is option, used to adjust the frequency response. If you are using a value other than those listed in Table 3, please confirm with the actual application.
(Note 3) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

Application Characteristic Data (Reference Data) – continued

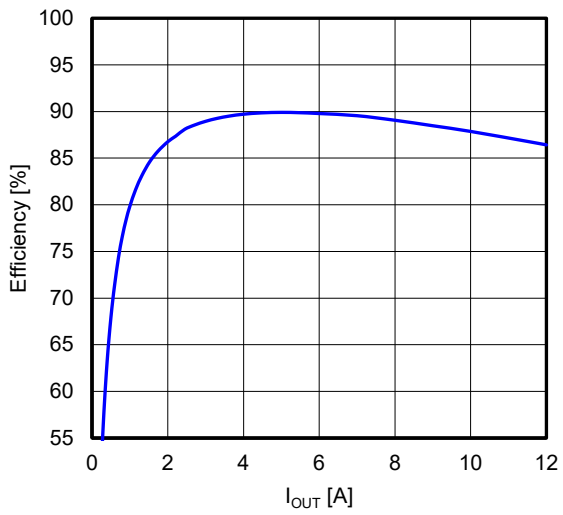


Figure 61. Efficiency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, Forced CCM)

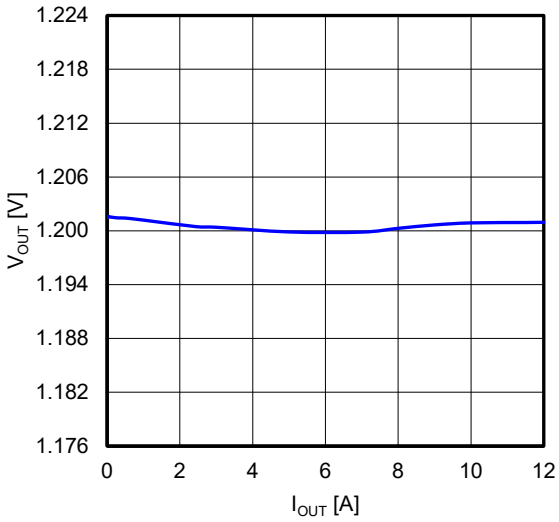


Figure 62. Load Regulation
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, Forced CCM)

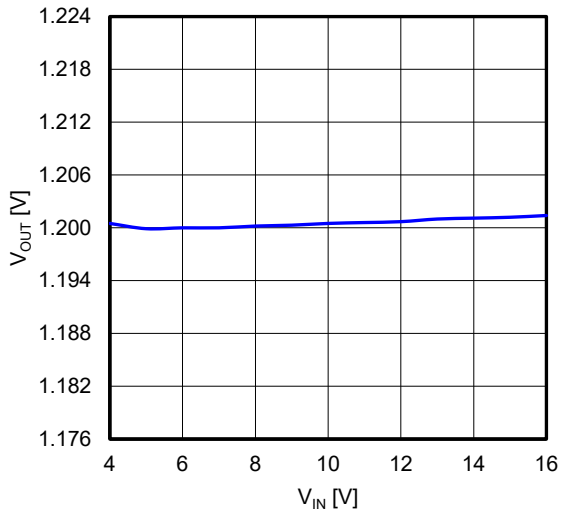


Figure 63. Line Regulation
(V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 6 A, Forced CCM)

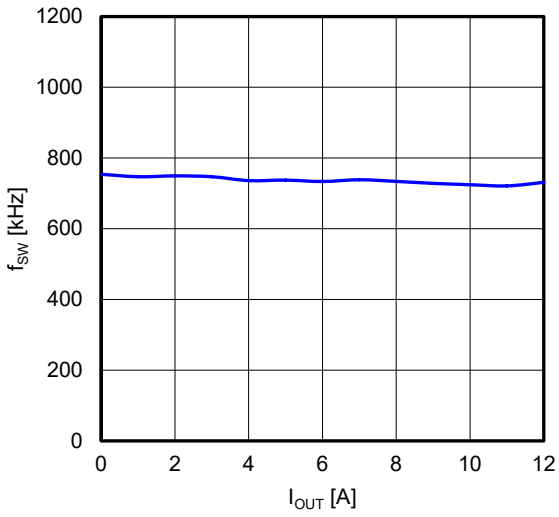


Figure 64. Switching Frequency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, Forced CCM)

Application Characteristic Data (Reference Data) – continued

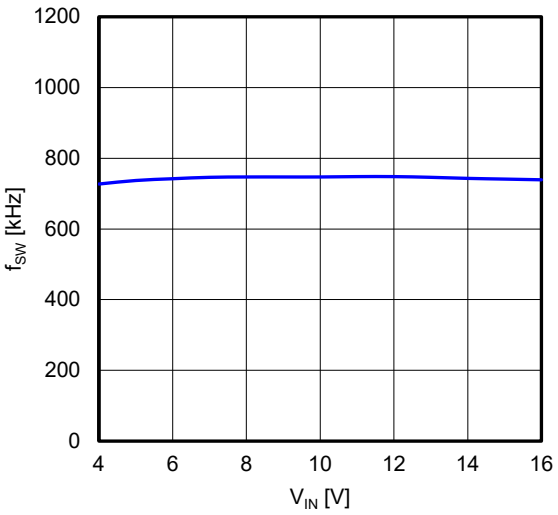


Figure 65. Switching Frequency vs Input Voltage
(V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 800 kHz, Forced CCM)

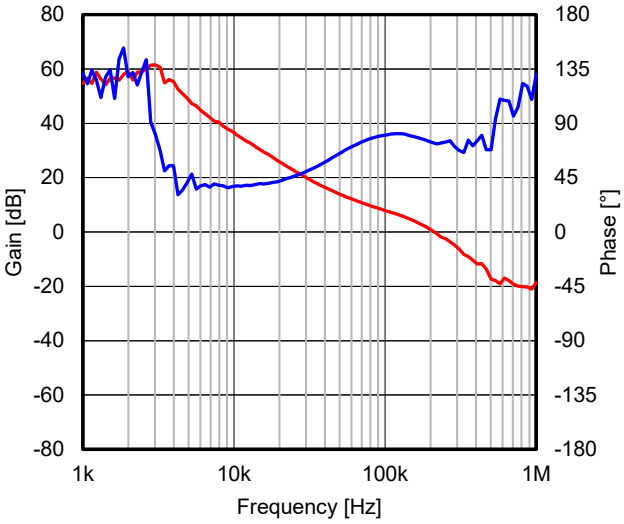


Figure 66. Frequency Characteristics
(V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 800 kHz, Forced CCM)

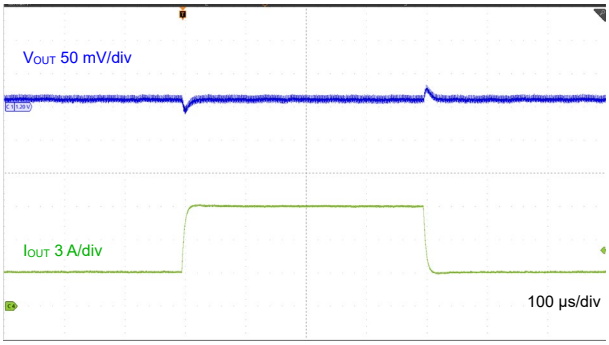


Figure 67. Load Transient Response
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, Forced CCM, I_{OUT} = 3 A to 9 A : 1 A/µs)

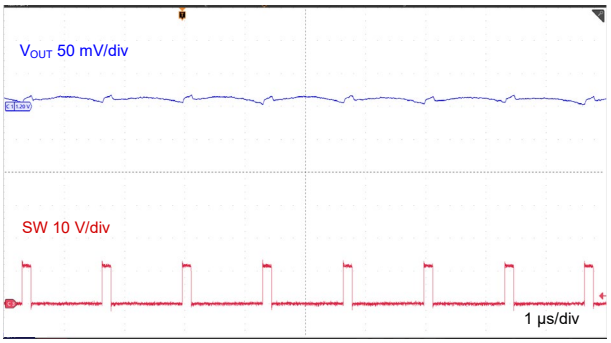


Figure 68. Output Ripple Voltage
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 800 kHz, I_{OUT} = 6 A, Forced CCM)

Application Characteristic Data (Reference Data) – continued

Table 8. Specification of Application

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	8 V to 16 V
Output Voltage	V_{OUT}	1.2 V (Typ)
Maximum Output Current	I_{OUTMAX}	12 A
Switching Frequency	f_{SW}	600 kHz (Typ)
Operation Mode	-	Forced CCM Mode
Operating Temperature	Ta	25 °C

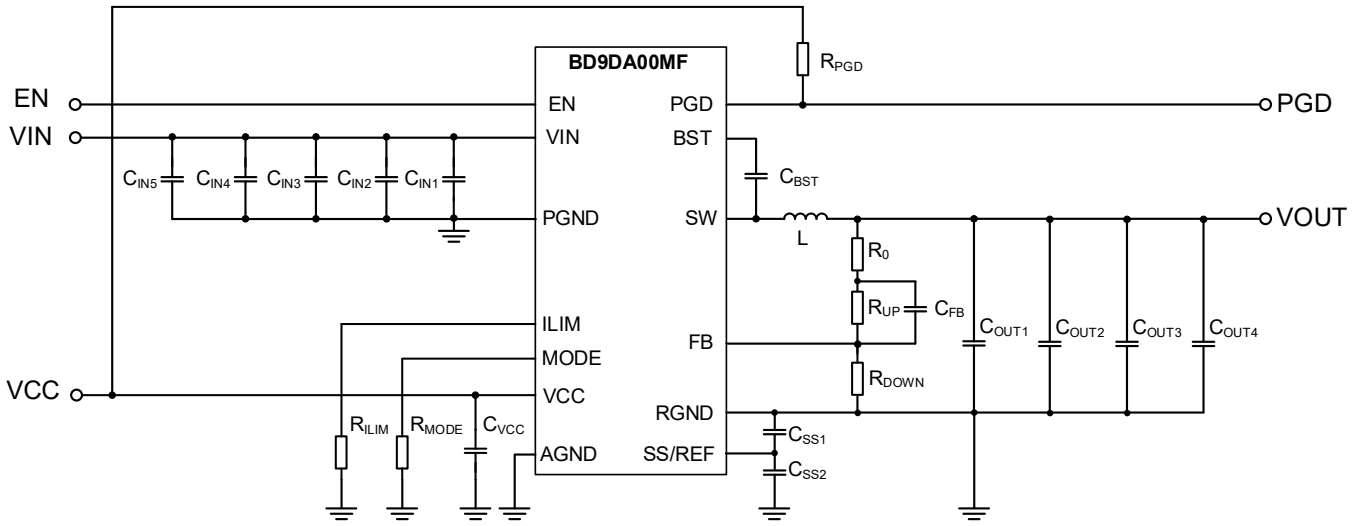


Figure 69. Application Circuit

Table 9. List of Components (Reference Example)

Part No.	Value	Part Name	Type	Size Code (mm)	Manufacturer
L	0.47 µH	SPM6530T-R47M170	Inductor	-	TDK
C_{IN1} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN2} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN3}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN4}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN5}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{OUT1}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT2}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT3}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT4}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{VCC}	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{BST}	0.1 µF, (X7R, 25 V)	GRM155R71E104KE14	Ceramic Capacitor	1005	Murata
C_{SS1}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{SS2}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{FB} *(Note 2)*	2200 pF, (X7R, 50 V)	GRM155R71H222KA01	Ceramic Capacitor	1005	Murata
R_{ILIM}	5.1 kΩ, (1 %, 1/16 W)	MCR01SMQPF5101	Chip Resistor	1005	ROHM
R_{MODE}	Short	-	-	-	-
R_{PGD}	10 kΩ, (1 %, 1/16 W)	MCR01SMQPF1002	Chip Resistor	1005	ROHM
R_0 *(Note 3)*	Short	-	-	-	-
R_{UP}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM
R_{DOWN}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 1 µF ceramic capacitor C_{IN1}, C_{IN2} as close to the VIN pin and the PGND pin as possible.
(Note 2) C_{FB} is option, used to adjust the frequency response. If you are using a value other than those listed in Table 3, please confirm with the actual application.
(Note 3) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

Application Characteristic Data (Reference Data) – continued

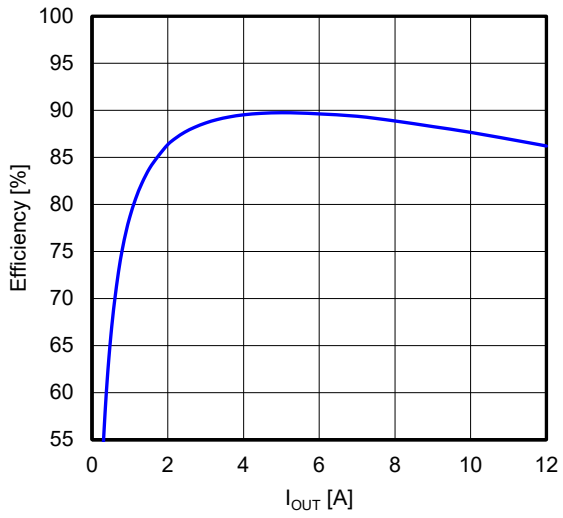


Figure 70. Efficiency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, Forced CCM)

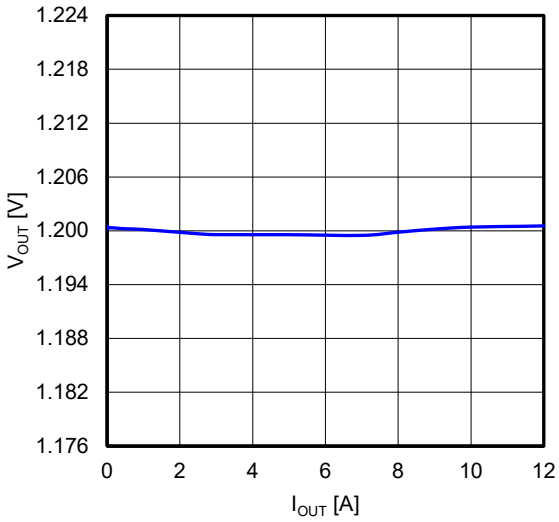


Figure 71. Load Regulation
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, Forced CCM)

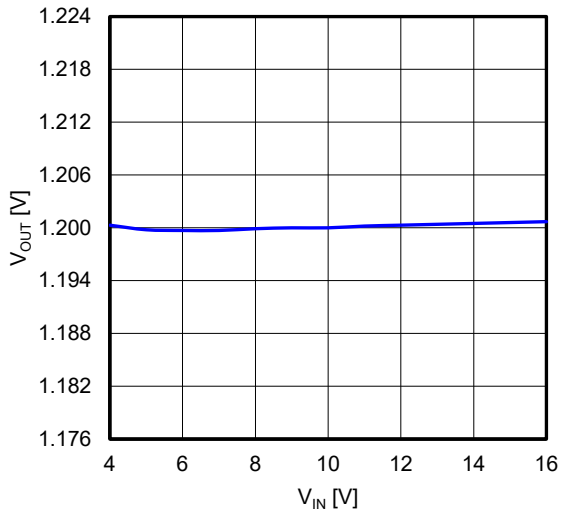


Figure 72. Line Regulation
(V_{OUT} = 1.2 V, f_{SW} = 600 kHz, I_{OUT} = 6 A, Forced CCM)

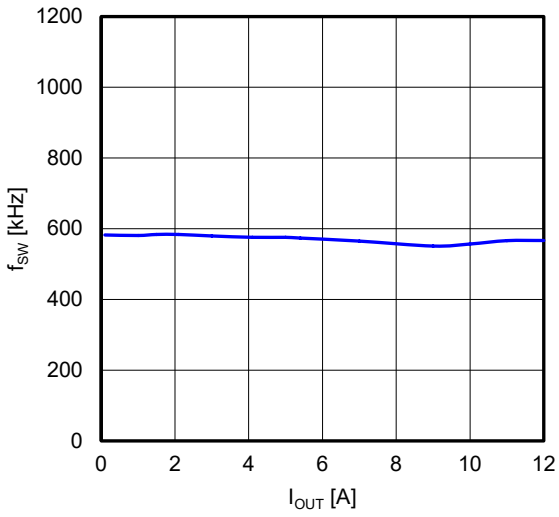


Figure 73. Switching Frequency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, Forced CCM)

Application Characteristic Data (Reference Data) – continued

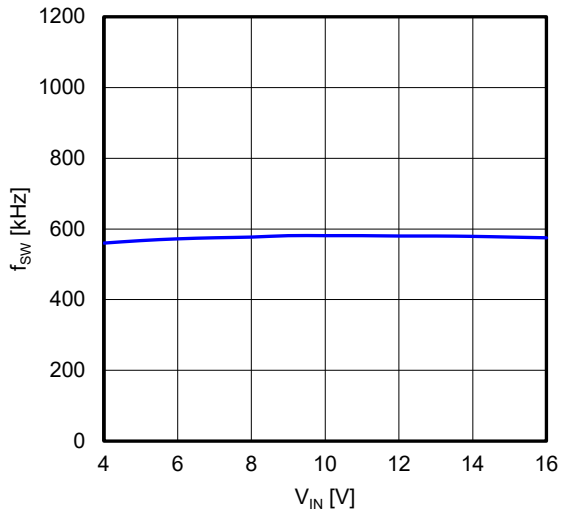


Figure 74. Switching Frequency vs Input Voltage
(V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 600 kHz, Forced CCM)

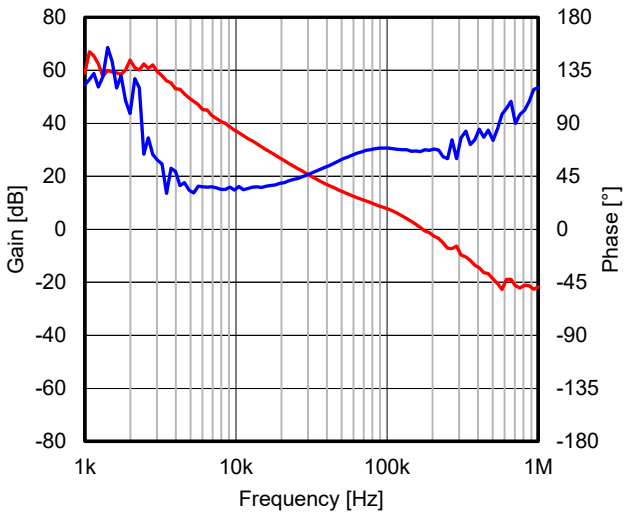


Figure 75. Frequency Characteristics
(V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 600 kHz, Forced CCM)

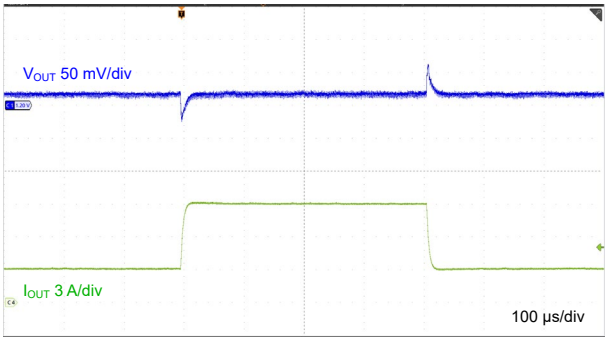


Figure 76. Load Transient Response
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, Forced CCM, I_{OUT} = 3 A to 9 A : 1 A/µs)

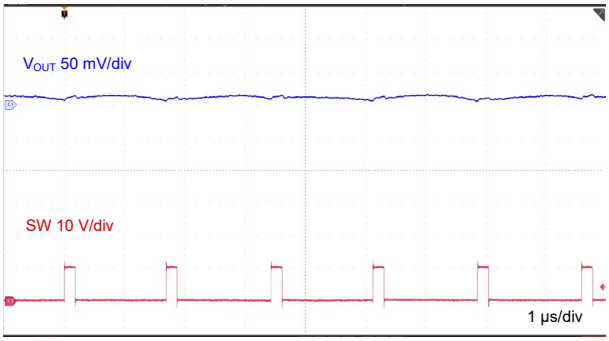


Figure 77. Output Ripple Voltage
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, I_{OUT} = 6 A, Forced CCM)

Application Characteristic Data (Reference Data) – continued

Table 10. Application Specification

Parameter	Symbol	Specification Value
Input Voltage	V_{IN}	8 V to 16 V
Output Voltage	V_{OUT}	1.2 V (Typ)
Maximum Output Current	I_{OUTMAX}	12 A
Switching Frequency	f_{SW}	1 MHz (Typ)
Operation Mode	-	Forced CCM Mode
Operating Temperature	Ta	25 °C

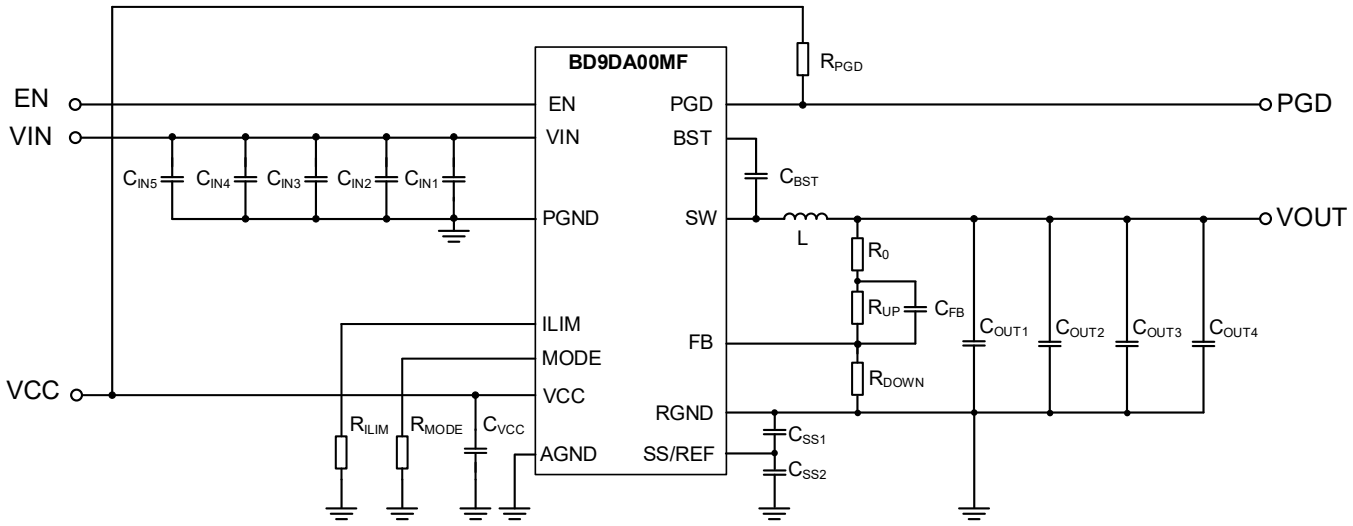


Figure 78. Application Circuit

Table 11. List of Components (Reference Example)

Part No.	Value	Part Name	Type	Size Code (mm)	Manufacturer
L	0.33 µH	SPM6550CT-R33L	Inductor	-	TDK
C_{IN1} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN2} *(Note 1)*	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{IN3}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN4}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{IN5}	10 µF, (X7R, 25 V)	GRM31CR71E106KA12	Ceramic Capacitor	3216	Murata
C_{OUT1}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT2}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT3}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{OUT4}	47 µF, (X5R, 6.3 V)	GRM21BR60J476ME01	Ceramic Capacitor	2012	Murata
C_{VCC}	1 µF, (X6S, 25 V)	GRM155C81E105KE11	Ceramic Capacitor	1005	Murata
C_{BST}	0.1 µF, (X7R, 25 V)	GRM155R71E104KE14	Ceramic Capacitor	1005	Murata
C_{SS1}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{SS2}	0.022 µF, (X7R, 25 V)	GRM155R71E223KA61	Ceramic Capacitor	1005	Murata
C_{FB} *(Note 2)*	2200 pF, (X7R, 50 V)	GRM155R71H222KA01	Ceramic Capacitor	1005	Murata
R_{ILIM}	5.1 kΩ, (1 %, 1/16 W)	MCR01SMQPF5101	Chip Resistor	1005	ROHM
R_{MODE}	62 kΩ, (1 %, 1/16 W)	MCR01SMQPF6202	Chip Resistor	1005	ROHM
R_{PGD}	10 kΩ, (1 %, 1/16 W)	MCR01SMQPF1002	Chip Resistor	1005	ROHM
R_0 *(Note 3)*	Short	-	-	-	-
R_{UP}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM
R_{DOWN}	1.5 kΩ, (1 %, 1/16 W)	MCR01SMQPF1501	Chip Resistor	1005	ROHM

(Note 1) In order to reduce the influence of high frequency noise, connect a 1 µF ceramic capacitor C_{IN1}, C_{IN2} as close to the VIN pin and the PGND pin as possible.
(Note 2) C_{FB} is option, used to adjust the frequency response. If you are using a value other than those listed in Table 3, please confirm with the actual application.
(Note 3) R_0 is an option, used for feedback's frequency response measurement. By inserting a resistor at R_0, it is possible to measure the frequency response (phase margin) using a FRA. However, the resistor is not used in actual application, use this resistor pattern in short-circuit mode.

Application Characteristic Data (Reference Data) – continued

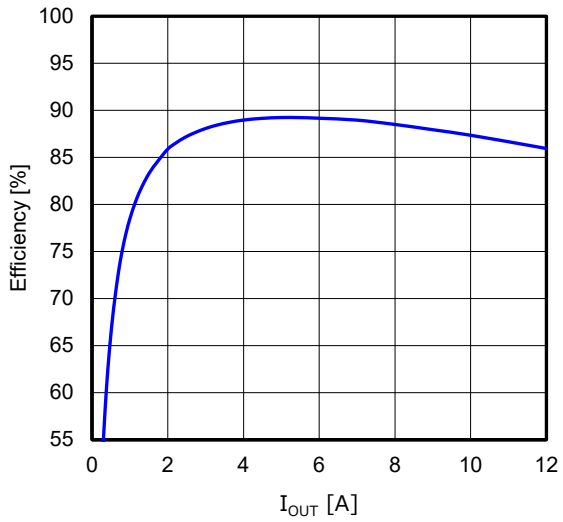


Figure 79. Efficiency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 1 MHz, Forced CCM)

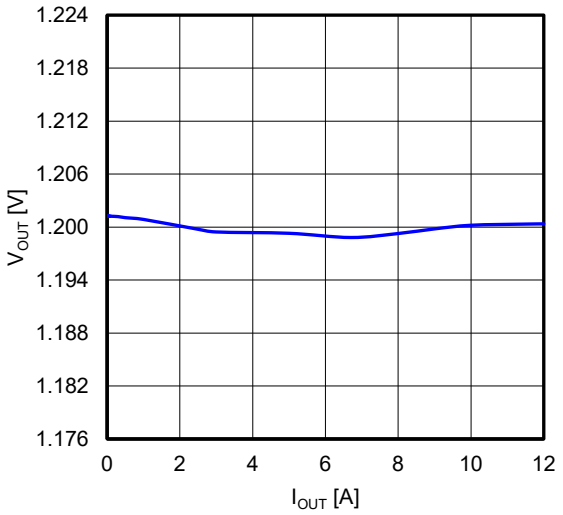


Figure 80. Load Regulation
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 1 MHz, Forced CCM)

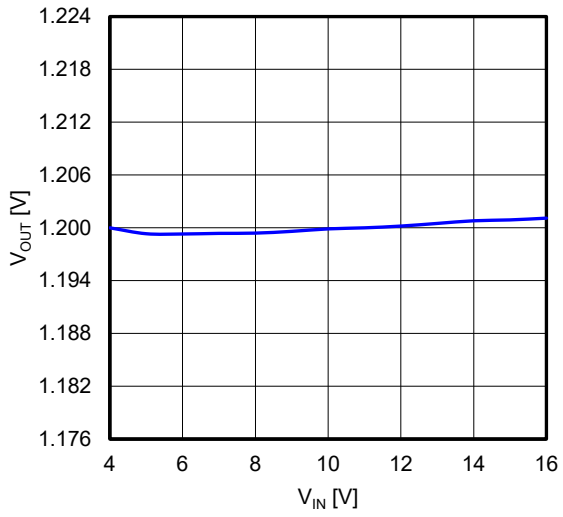


Figure 81. Line Regulation
(V_{OUT} = 1.2 V, f_{SW} = 1 MHz, I_{OUT} = 6 A, Forced CCM)

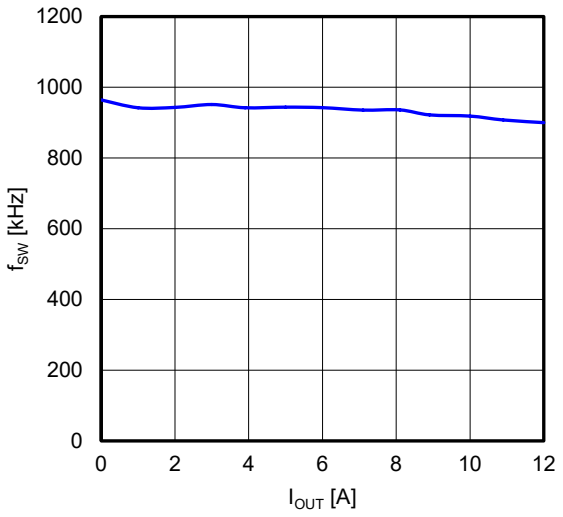


Figure 82. Switching Frequency vs Output Current
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 1 MHz, Forced CCM)

Application Characteristic Data (Reference Data) – continued

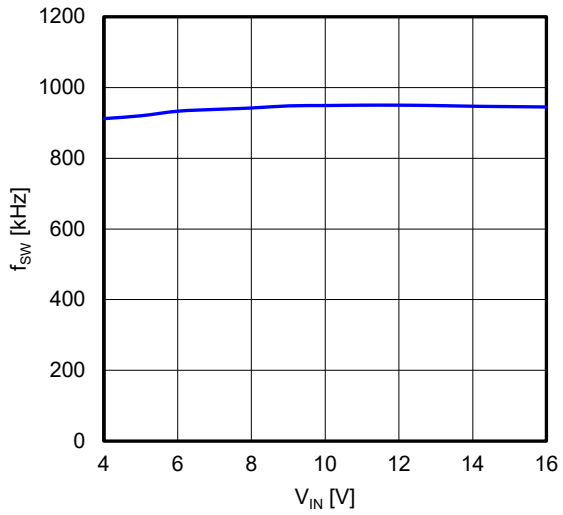


Figure 83. Switching Frequency vs Input Voltage
(V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 1 MHz, Forced CCM)

Figure 84. Frequency Characteristics
(V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 1 MHz, Forced CCM)

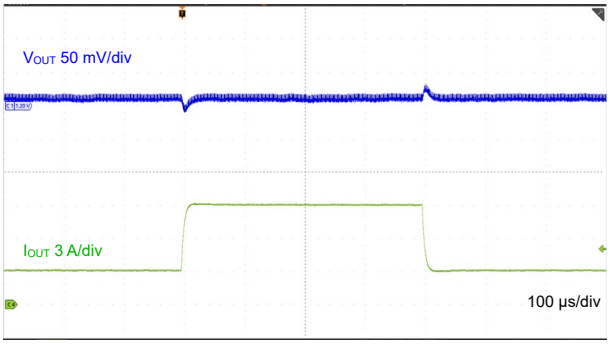


Figure 85. Load Transient Response
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 1 MHz, Forced CCM, I_{OUT} = 3 A to 9 A : 1 A/µs)

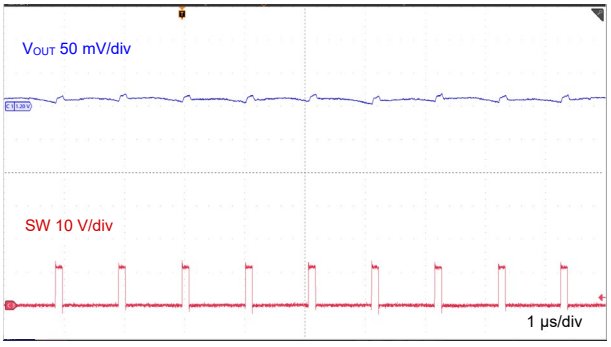


Figure 86. Output Ripple Voltage
(V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 1 MHz, I_{OUT} = 6 A, Forced CCM)

PCB Layout Design

PCB layout design for DC/DC converter is very important. The appropriate layout can avoid various problems concerning power supply circuit. Figure 87 to Figure 89 show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 87 is a current path when High-Side Switch is ON and Low-Side Switch is OFF, the Loop 2 in Figure 88 is when High-Side Switch is OFF and Low-Side Switch is ON. The thick line in Figure 89 shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element High-Side and Low-Side Switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

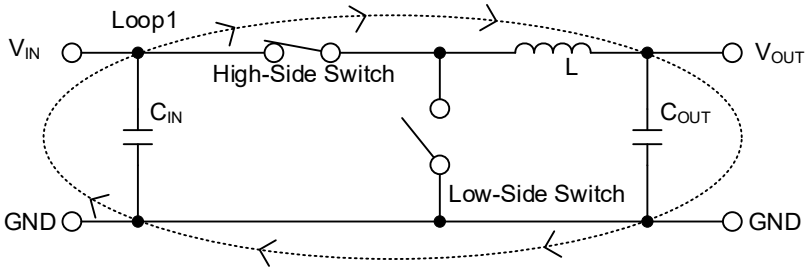


Figure 87. Current Path when High-Side Switch = ON, Low-Side Switch = OFF

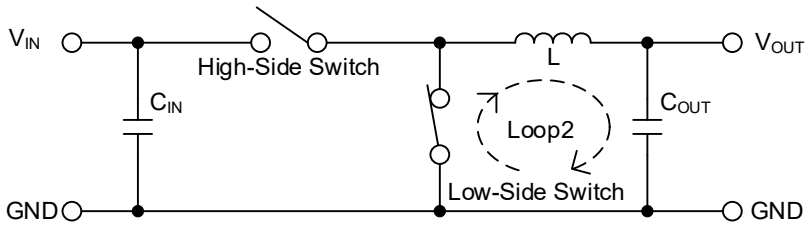


Figure 88. Current Path when High-Side Switch = OFF, Low-Side Switch = ON

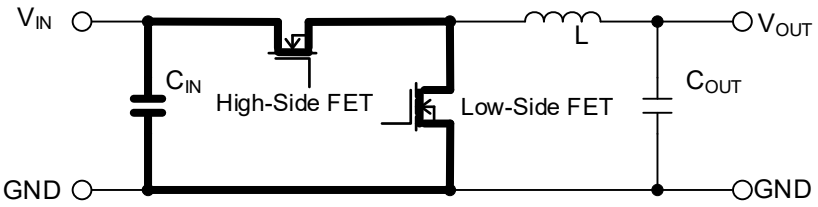


Figure 89. Difference of Current and Critical Area in Layout

PCB Layout Design – continued

When designing the PCB layout, pay attention to the following points:

- Connect the input capacitors C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4} and C_{IN5} as close to the VIN pin and PGND pin as possible on the same plane as the IC.
- Place two VIN VIAs and two PGND VIAs for C_{IN2}.
- Place as many VIN VIAs as possible directly under the IC to improve heat dissipation.
- Place a minimum of six PGND VIAs near the PGND pins of the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern L as thick and as short as possible.
- Feedback line connected to the FB pin far from the SW nodes.
- Place R_{UP}, R_{DOWN}, C_{FB}, and C_{RGND} as close to the IC on the same layer as possible to minimize the distance of the feedback line.
- Place the output capacitors C_{OUT1}, C_{OUT2}, C_{OUT3}, and C_{OUT4} away from the input capacitors C_{IN1}, C_{IN2}, C_{IN3}, C_{IN4}, and C_{IN5} to avoid the influence of harmonic noise from the input.
- Separate the reference ground and power ground and connect each with VIAs. Connect the reference ground to the power ground near C_{VCC}, where high frequency switching noise is minimal.
- Place the VCC bypass capacitor as close to the pin as possible.

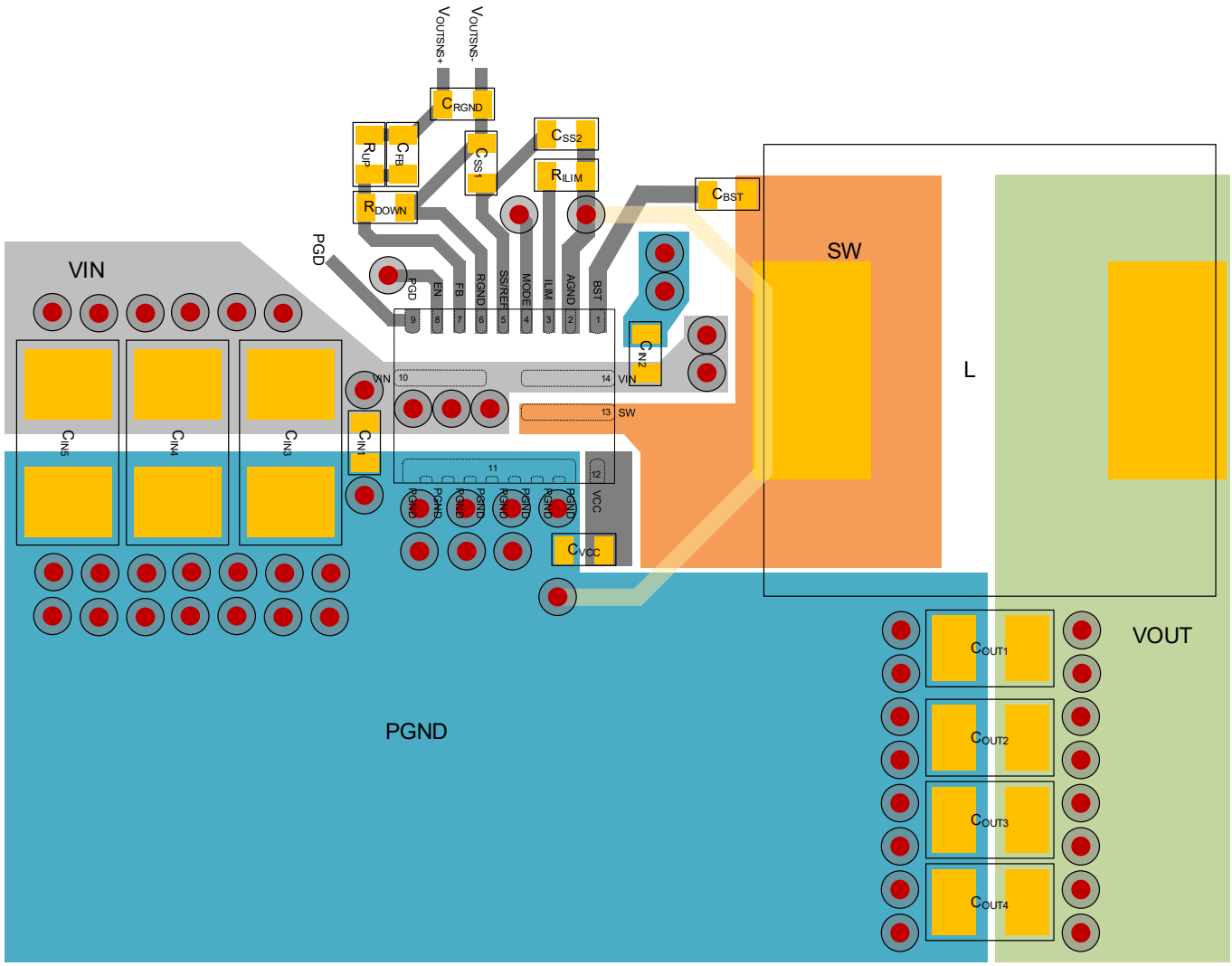
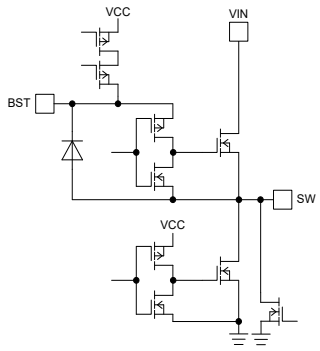
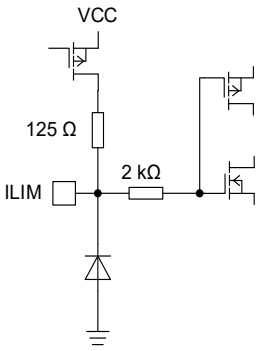
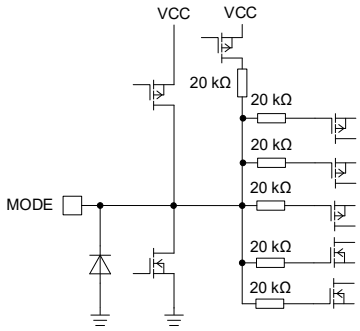
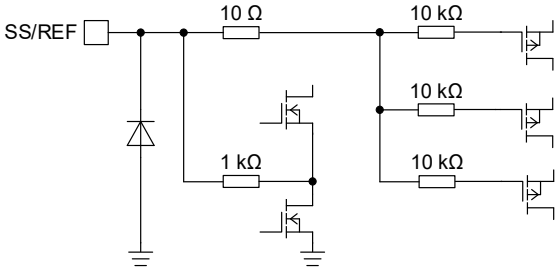


Figure 90. Recommended PCB Layout

I/O Equivalence Circuits

1. BST, 13. SW	3. ILIM
	
4. MODE	**5. SS/REF**
	
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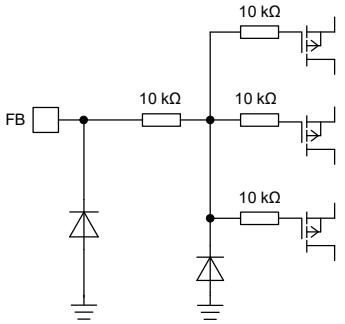
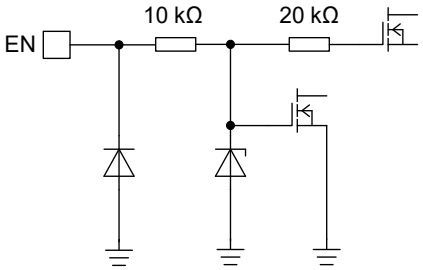
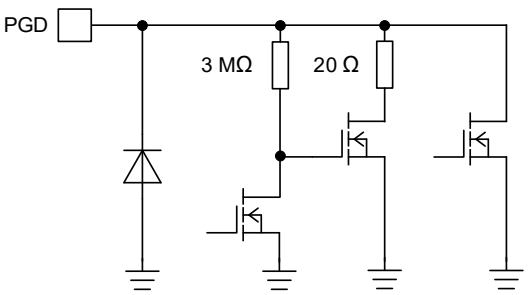
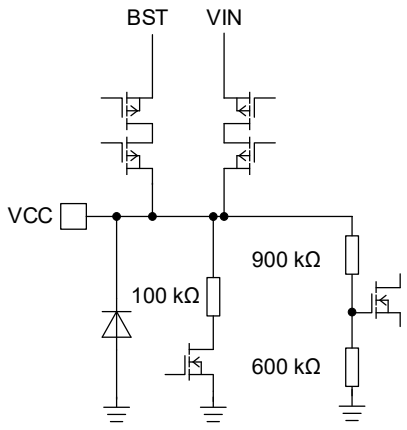
	
9. PGD	**12. VCC**
	

(Note) Resistor values are typical.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

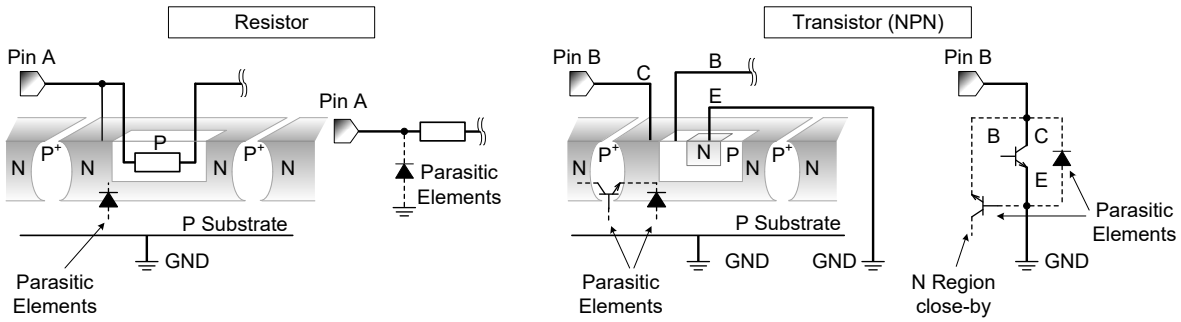


Figure 91. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn off power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

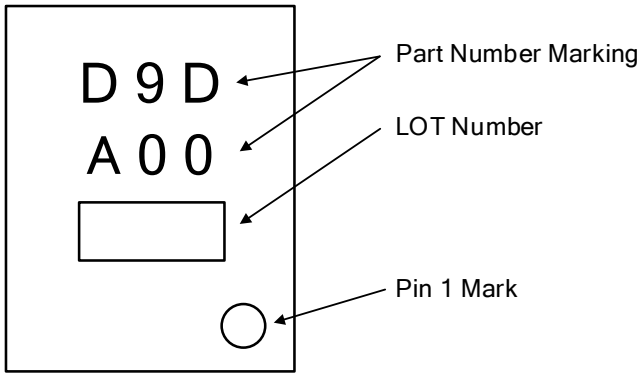
B D 9 D A 0 0 M F	-	E 2

Package
MF: UFN014V3040

Packaging and forming specification
E2: Embossed tape and reel

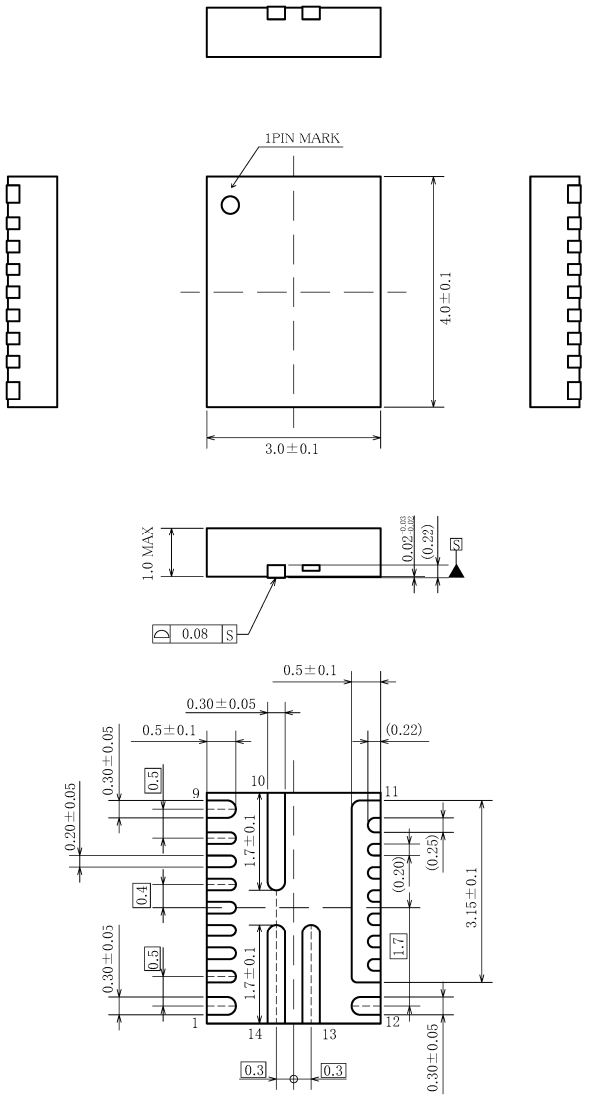
Marking Diagram

UFN014V3040 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	UFN014V3040



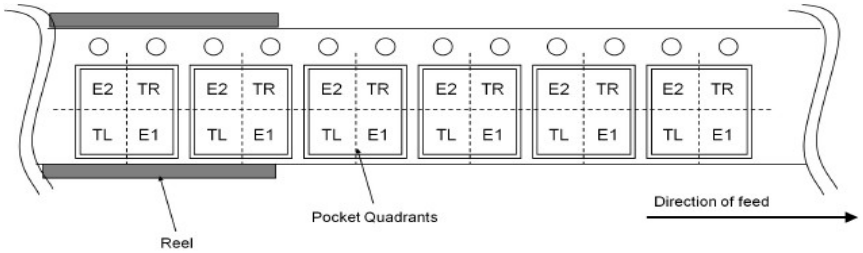
(UINT:mm)

PKG:UFN014V3040
Drawing No.EX657-5001

NOTE:Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
18.Mar.2025	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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