

5.5 V to 104.5 V Input Voltage Range 1 A Output Built-in MOSFET

5.5 V to 104.5 V Input, Ultra-low-Iq, 1 A Synchronous Buck DCDC Converter

BD9G146MUV-LB

General Description

This product is a ranked product for the industrial equipment market. This is the best product for use in these applications. BD9G146MUV-LB is synchronous Buck DCDC Converter and designed to regulate over a wide input voltage range from 5.5 V to 104.5 V. It can be used for high voltage 48 V bus system with Minimum controllable ON time 100 ns and large step-down conversion ratios. DCDC control method is Fixed Frequency Current Mode PWM Control. The Switching frequency can be set from 200 kHz to 1 MHz with an external resistor at RT pin.

Key Specifications

■ Input Voltage Range:	5.5 V to 104.5 V
■ Output Voltage Range:	2.5 V to 68 V
■ Output Current:	1 A (Max)
■ Switching Frequency Range:	200 kHz to 1 MHz
■ Hi-side NFET Rdson:	790 mΩ (Typ)
■ Lo-side NFET Rdson:	330 mΩ (Typ)
■ Shutdown Current	1 μA (Typ)
■ Operating Junction Temperature	-40 °C to +125 °C

Package

VQFN020V4040

W (Typ) x D (Typ) x H (Max)

4.0 mm x 4.0 mm x 1.0 mm

Features

- Wide Input Voltage Range 5.5 V to 104.5 V
- Wide Output Voltage Range 2.5 V to 68 V
- Built-in Hi-side NFET Rdson 790 mΩ, Lo-side NFET Rdson 330 mΩ
- Fixed Frequency Current Mode PWM Control
- Adjustable Frequency by RT 200 kHz to 1 MHz
- Soft Start
- Light Load Mode (LLM)
- Forced Pulse Wide Modulation (PWM) Mode
- Selectable Spread Spectrum Switching
- External Synchronization Function
- Ultra-low-Iq 10.0 μA No Switching
- Shutdown Current 1.0 μA
- Over Current Protection (OCP), Input Under Voltage Lockout (UVLO), Thermal Shutdown (TSD)

Applications

- Industrial Equipment
- 48 V/12 V Bus System
- High-cell Battery Application, e.g. E-bike
- Motor Drive
- Telecom System

Typical Application Circuit

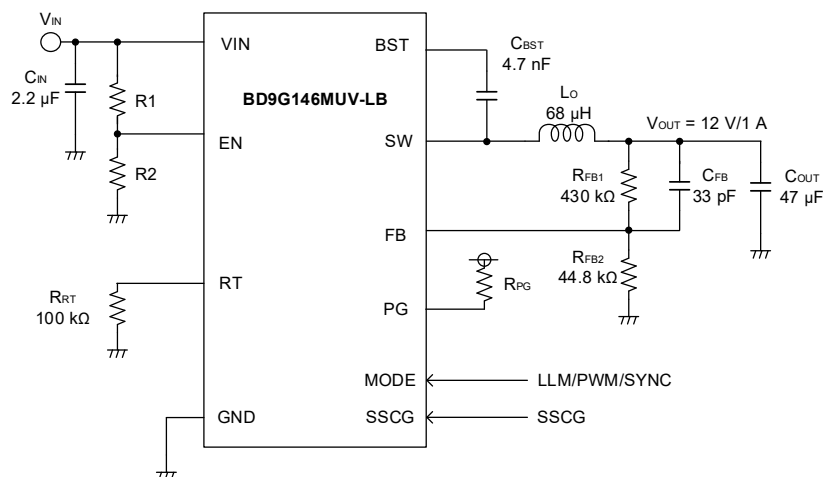


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

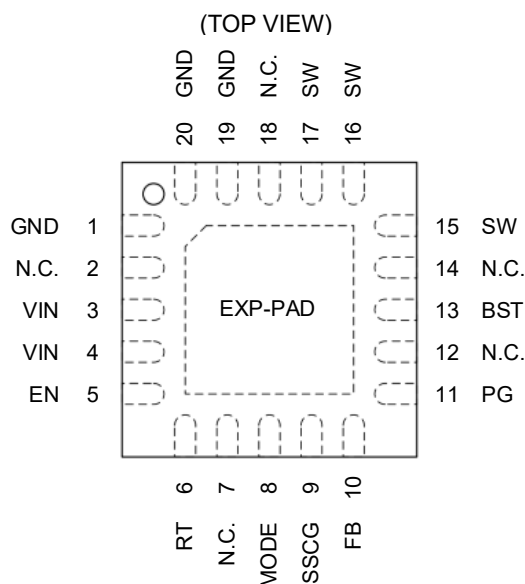


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Description
1, 19, 20	GND	Ground connection for internal circuits
2, 7, 12, 14, 18	N.C.	This pin is not connected to the chip. Use this as open. If this pin is used other than open and adjacent pins are expected to be shorted, please confirm if there is any problem with the actual application.
3, 4	VIN	Regulator supply input pin
5	EN	Enable input. ON/OFF control for the DCDC and UVLO programming pin. The EN voltage is above 1.4 V, the start-up sequence begins. Less than 1.31 V is disabled from enabled status.
6	RT	The internal oscillator frequency set pin. The internal oscillator is set with a single resistor connected between this pin and the GND pin.
8	MODE	Pin to select FPWM (Forced PWM) mode, AUTO (Automatically switched between PWM mode and LLM) mode, or SYNC (Activate synchronization) mode. In case of using FPWM mode, set high. In case of using AUTO mode, set low or open. In case of using SYNC mode, apply a clock to this pin.
9	SSCG	Pin to select Spread Spectrum function. Set high to enable Spread Spectrum and set low or open to disable Spread Spectrum.
10	FB	Voltage feedback pin. This pin is the error-amp input with the DC voltage is set at 1.125 V with feed-back operation.
11	PG	Power Good indicator. This pin is an open-drain output pin. Connect to a source voltage through an external pullup resistor between 10 kΩ to 100 kΩ.
13	BST	Connect a bootstrap capacitor of 4.7 nF (Typ) between this pin and the SW pin. The voltage of this capacitor is the gate drive of the High Side FET.
15, 16, 17	SW	Switching node that is internally connected to the source of the high-side NMOS buck switch and the drain of the low-side NMOS synchronous rectifier. Connect to the switching node of the power inductor.
-	EXP-PAD	The EXP-PAD is connected to the P substrate of the IC. Connect this pad to the internal PCB ground plane using multiple via holes to obtain excellent heat dissipation characteristics.

Block Diagram

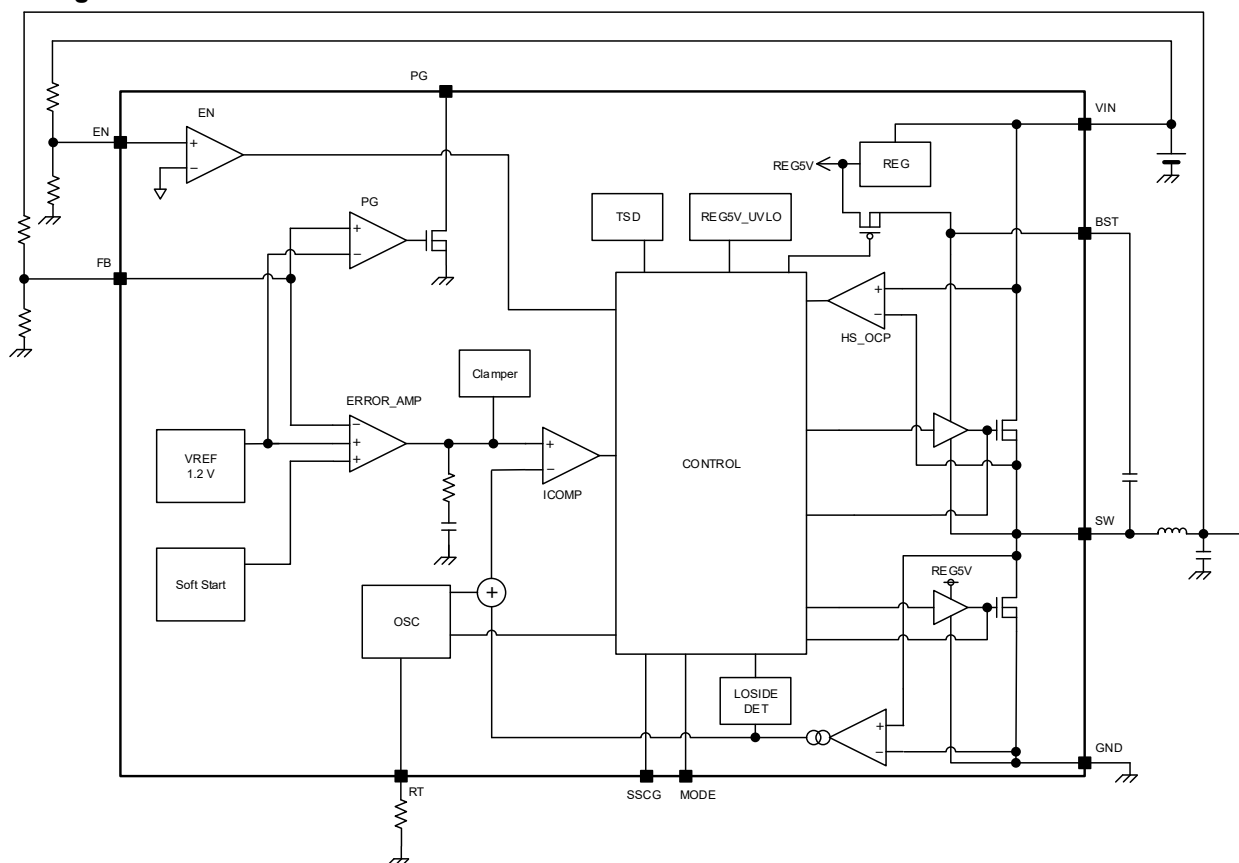


Figure 3. Block Diagram

Description of Blocks

1. VREF
This block generates reference voltage.
2. REG
Regulator for internal circuit power supply.
3. OSC
This block generates inner CLK.
The internal oscillator is set with a single resistor connected between this pin and the GND pin.
Recommended frequency range is 200 kHz to 1 MHz. If the RT pin connects to 100kΩ, frequency is set 300 kHz.
4. TSD
Thermal Shutdown Protection Circuit.
When it detects the temperature exceeding Maximum Junction Temperature ($T_J = 150\text{ }^{\circ}\text{C}$), it turns off the output FET, and resets Soft Start circuit. It has a hysteresis function. When the temperature decreases, the chip automatically returns to normal operation.
5. REG5V_UVLO
Under Voltage Lockout Circuit for Internal voltage REG5V.
This prevents internal circuit errors during increase and decrease of power supply voltage.
6. EN
ON/OFF control for the DCDC and UVLO programming.
The EN voltage is above 1.4 V, the start-up sequence begins. Less than 1.31 V is disabled from enabled status.
7. PG
If the FB voltage exceeds 1.069 V, PG switch turns off. If the FB voltage falls below 1.013 V, PG switch turns on.

Description of Blocks - continued

8. Soft Start
This is a circuit that gently raises the output voltage of the DCDC converter to prevent in-rush current during start-up. Soft Start Time is 3 ms (Typ) when the IC operates with the 300 kHz (Typ).
9. ERROR_AMP
This is an error amplifier that detects output signal, and outputs PWM control signal. Internal reference voltage is set to 1.125 V.
10. ICOMP
This is a comparator that outputs PWM signal from current feed-back signal and error-amp output for current-mode.
11. LO SIDE DET
This block stops the switching by detecting reverse current of the SW current at discontinuous current mode control.
12. HS_OCP
This block detects the current flowing through the High Side FET and limits the current of 1.4 A (Min) or more. This function works in abnormal situation such as the SW pin shorted to GND condition to prevent the High Side FET from destruction.
13. CONTROL
This block controls switching operation and protection functions.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{VIN}	-0.3 to +110	V
BST – GND	V_{BST}	-0.3 to +110	V
BST – SW ^(Note 1)	ΔV_{BST}	-0.3 to +7	V
EN – GND	V_{EN}	-0.3 to +110	V
SW – GND	V_{SW}	-1.0 to +110	V
SW – GND (5 ns pulse width)	V_{SWAC}	-4	V
RT – GND	V_{RT}	-0.3 to +110	V
PG – GND	V_{PG}	-0.3 to +110	V
FB – GND	V_{FB}	-0.3 to +110	V
MODE – GND	V_{MODE}	-0.3 to 7	V
SSCG – GND	V_{SSCG}	-0.3 to 7	V
Maximum Junction Temperature	T_{jmax}	150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Because this IC Voltage from SW to BST absolute maximum rating is 7.0 V, do not short VIN Pin to BST Pin after power ON.

Thermal Resistance^(Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 4)	2s2p ^(Note 5)	
VQFN020V4040				
Junction to Ambient	θ_{JA}	153.9	37.4	°C/W
Junction to Top Characterization Parameter ^(Note 3)	Ψ_{JT}	13	7	°C/W

(Note 2) Based on JESD51-2A (Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-9.

(Note 5) Using a PCB board based on JESD51-5, 9.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.5 mm x 101.5 mm x 1.6 mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.5 mm x 101.5 mm x 1.6 mm	1.20 mm	Φ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	99.5 mm x 99.5 mm	35 μ m	99.5 mm x 99.5 mm	70 μ m

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{VIN}	5.5	-	104.5	V
Output Current	I_{OUT}	-	-	1	A
Output Voltage	V_{OUT}	2.5	-	68	V
Switching Frequency	f_{SW}	200	-	1000	kHz
Operating Temperature	T_{opr}	-40	-	+125	°C

Electrical Characteristics (Unless otherwise specified $V_{VIN} = 24\text{ V}$, $V_{EN} = 2\text{ V}$, $T_j = -40\text{ °C}$ to $+125\text{ °C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VIN Shutdown Current	I_{SDN}	-	1.0	12.0	μA	
VIN SLEEP Current	I_{SLEEP}	-	10.0	25.0	μA	$V_{EN} = V_{VIN}$, $V_{FB} = 1.5\text{ V}$
EN ON Threshold Voltage	V_{ENH}	1.35	1.40	1.45	V	
EN OFF Threshold Voltage	V_{ENL}	1.26	1.31	1.36	V	
EN Input Current	I_{EN}	-1	0	+1	μA	
Reference Voltage	V_{FB}	1.114	1.125	1.136	V	
FB Input Current	I_{FB}	-1	0	+1	μA	
SW Switching Frequency	f_{SW}	200	-	1000	kHz	
Hi Side NFET Rdson	R_{ONH}	-	790	-	$\text{m}\Omega$	$T_a = 25\text{ °C}$
Low Side NFET Rdson	R_{ONL}	-	330	-	$\text{m}\Omega$	$T_a = 25\text{ °C}$
PG Low to High Threshold Voltage	V_{PGR}	1.034	1.069	1.104	V	
PG High to Low Threshold Voltage	V_{PGF}	0.978	1.013	1.048	V	
PG Pulldown Resistance	R_{PG}	-	45	-	Ω	$T_a = 25\text{ °C}$
Soft Start Time	t_{SS}	2.5	3.0	4.0	ms	$R_{RT} = 100\text{ k}\Omega$
Over Current Protection	I_{OCP}	1.05	1.30	1.85	A	Output Current, $T_a = 25\text{ °C}$
MODE Input Voltage High	V_{MODEH}	2.0	-	5.5	V	
MODE Input Voltage Low	V_{MODEL}	-	-	0.8	V	
MODE Input Current	I_{MODE}	-	50	80	μA	$V_{MODE} = 5\text{ V}$
SSCG Input Voltage High	V_{SSCGH}	2.0	-	5.5	V	
SSCG Input Voltage Low	V_{SSCGL}	-	-	0.8	V	
SSCG Input Current	I_{SSCG}	-	50	80	μA	$V_{SSCG} = 5\text{ V}$

Typical Performance Characteristics

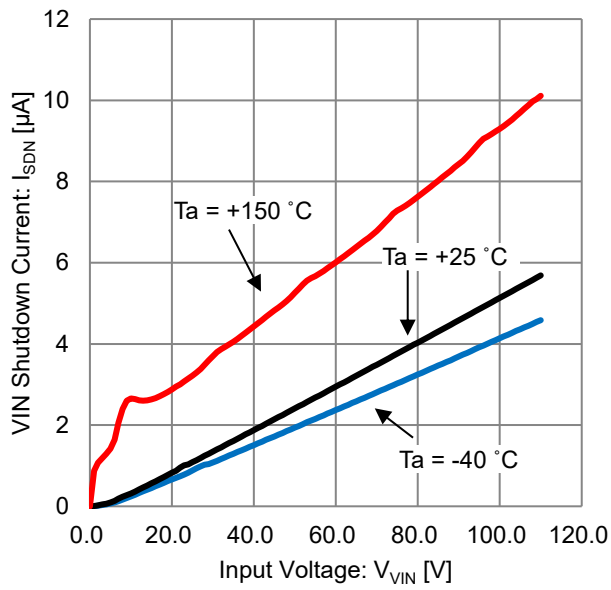


Figure 4. VIN Shutdown Current vs Input Voltage
($V_{EN} = 0\text{ V}$)

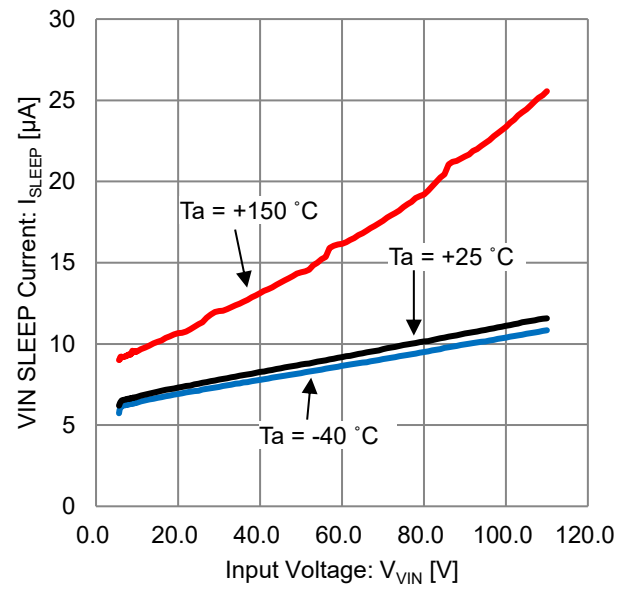


Figure 5. VIN SLEEP Current vs Input Voltage
($V_{EN} = V_{VIN}$, $V_{FB} = 1.5\text{ V}$)

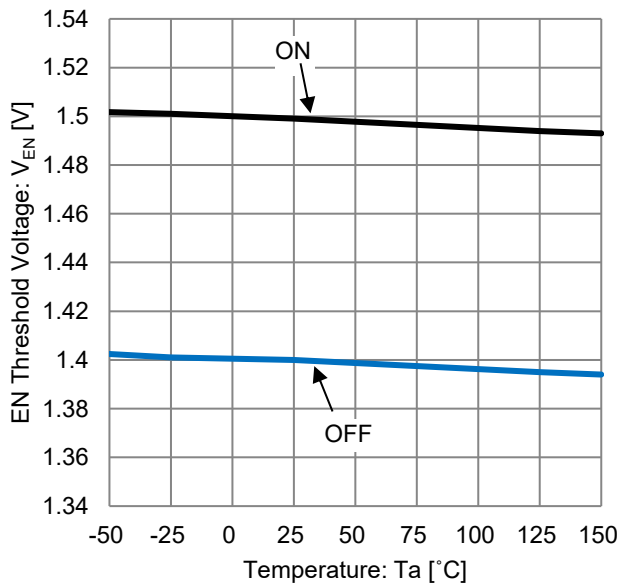


Figure 6. EN Threshold Voltage vs Temperature

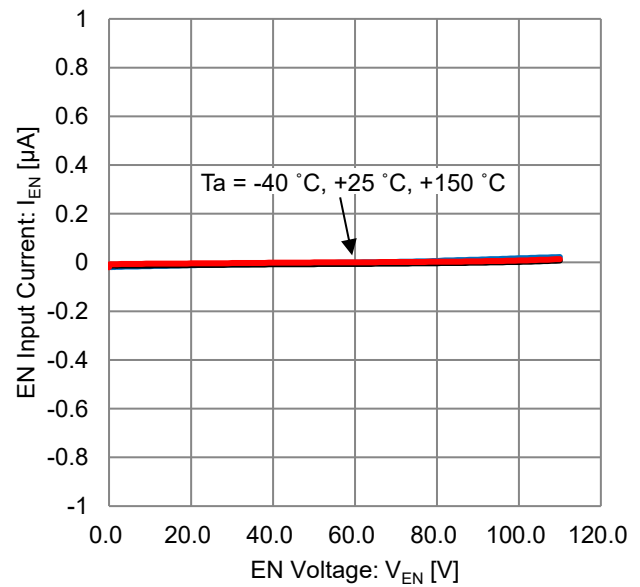


Figure 7. EN Input Current vs EN Voltage
($V_{VIN} = 110\text{ V}$)

Typical Performance Characteristics - continued

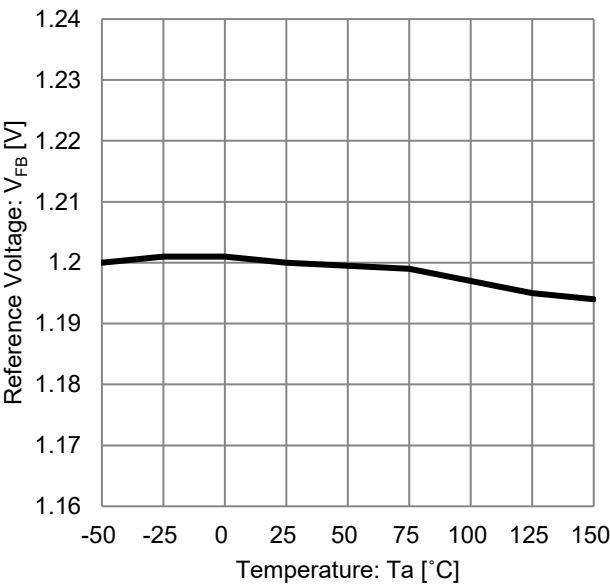


Figure 8. Reference Voltage vs Temperature

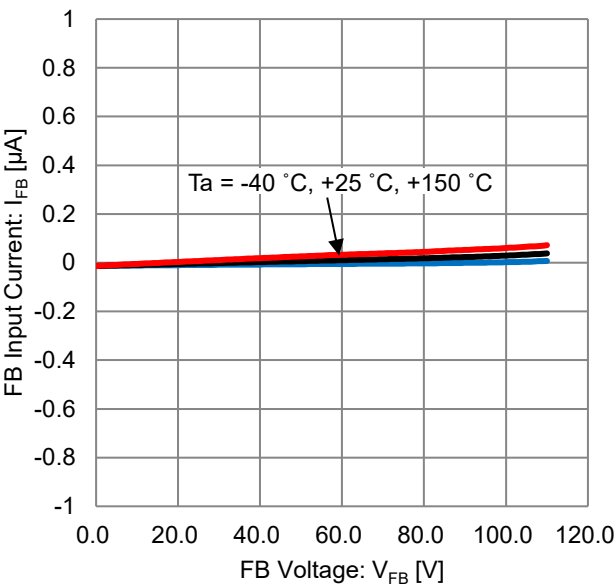


Figure 9. FB Input Current vs FB Voltage
($V_{VIN} = 110\text{ V}$)

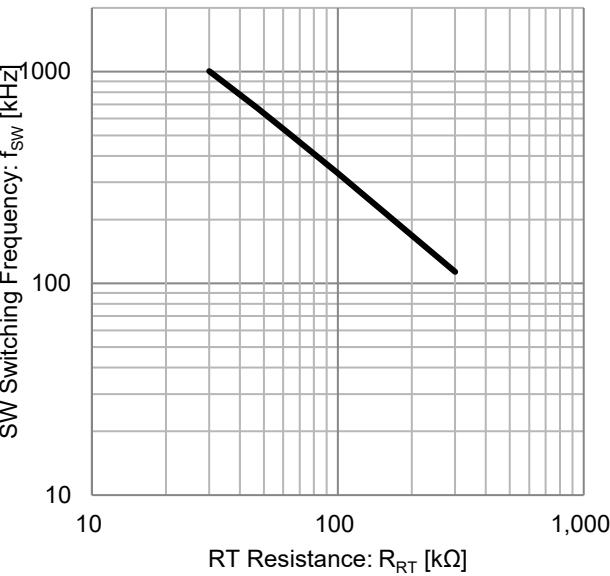


Figure 10. SW Switching Frequency vs RT Resistance

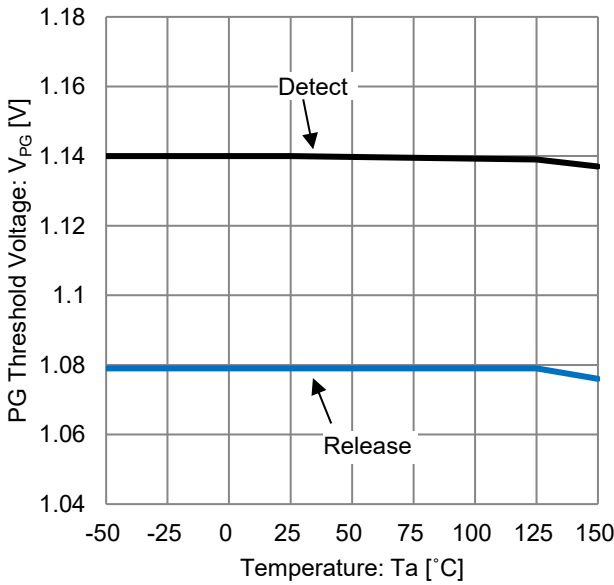


Figure 11. PG Threshold Voltage vs Temperature

Typical Performance Characteristics - continued

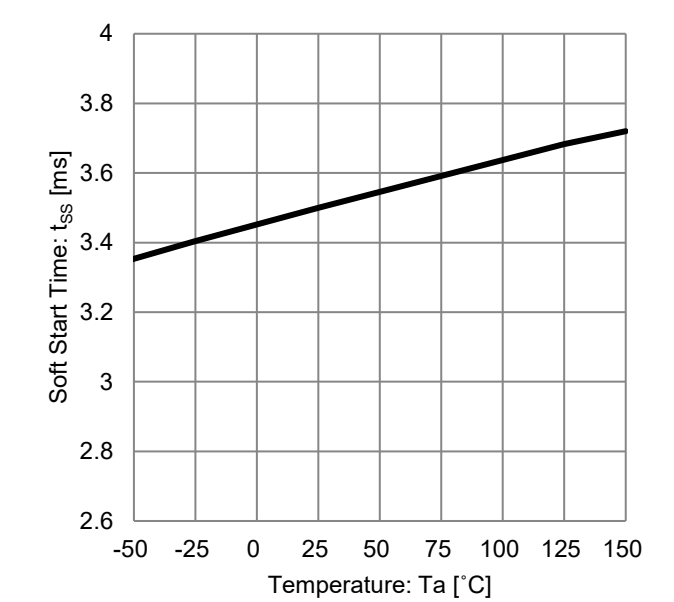


Figure 12. Soft Start Time vs Temperature
($R_{RT} = 100\text{ k}\Omega$)

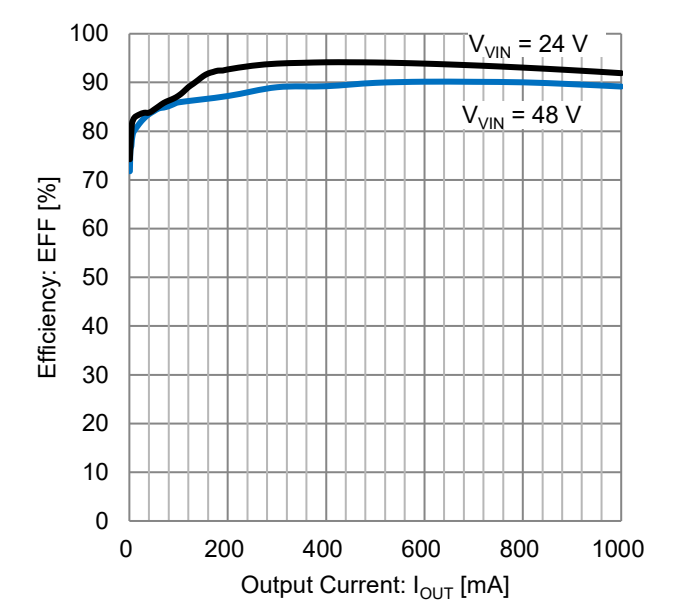


Figure 13. Efficiency vs Output Current
($V_{OUT} = 12\text{ V}$, $f_{SW} = 300\text{ kHz}$)

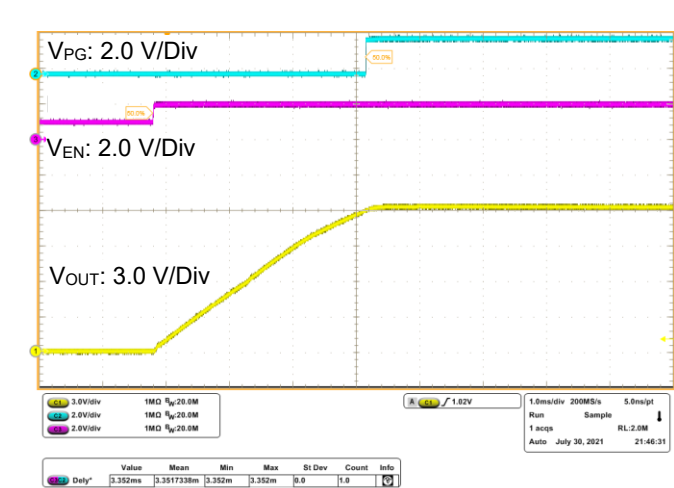


Figure 14. Startup
($V_{OUT} = 12\text{ V}$, $f_{SW} = 300\text{ kHz}$)

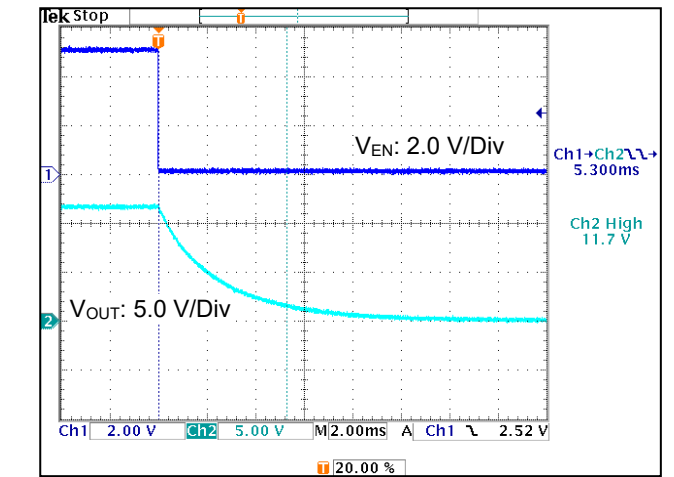


Figure 15. Shutdown
($V_{OUT} = 12\text{ V}$, $f_{SW} = 300\text{ kHz}$, Load Resistance = $60\text{ }\Omega$)

Detailed Description

1. Output Voltage Setting

The internal reference voltage of error-amplifier is 1.125 V. Output voltage is determined by the following formula.

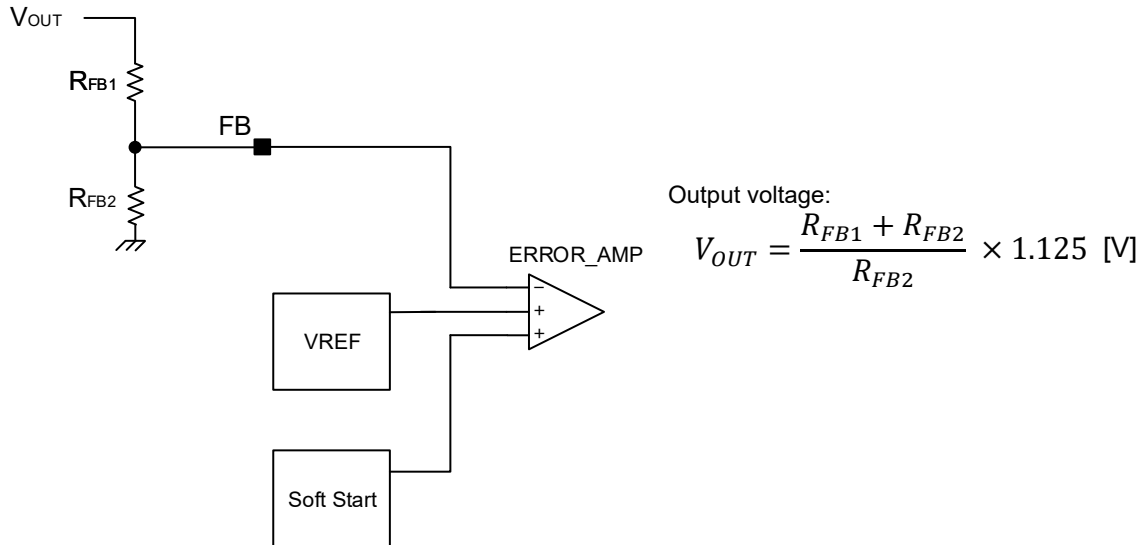


Figure 16. Output Voltage Setting

2. Min Duty (Don_min)

There are output voltage restrictions by Min Duty.

The Min Duty required is as follows with min on time (100 ns).

$$D_{on_min} = (100 \text{ ns} \times f_{osc}) \times 100 \text{ [%]}$$

3. Low Drop Out Operation

For the BST pin charge that is the drive voltage of the High-side Nch FET, input and output limit is set by Max Duty. Operation Duty is calculated as follows by input and output voltage to use and a load.

$$D_{on} = \frac{V_{OUT}}{V_{VIN} - R_{ONH} \times I_{OUT}} \times 100 \text{ [%]}$$

Max Duty is calculated as follows by forced-off time (Typ: 200 ns) and operating frequency.

$$D_{on_max} = (1 - 200 \text{ ns} \times f_{osc}) \times 100 \text{ [%]}$$

4. Frequency Setting

Arbitrary internal oscillator frequency setup is possible by connecting RT resistance. Recommended frequency range is 200 kHz to 1 MHz.

For setting frequency f [Hz], RT resistance is looked for using the following formula.

$$R_{RT} = \frac{\frac{475}{f} - 16.15 \times 10^{-6}}{14.623 \times 10^{-9}} \text{ [\Omega]}$$

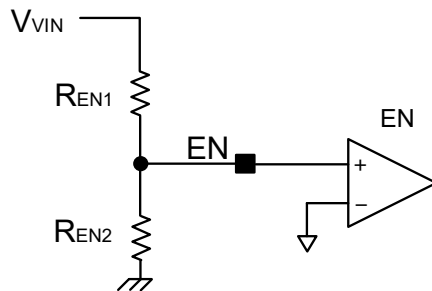
If setting frequency is 300 kHz, R_{RT} is 100 kΩ.

Detailed Description - continued

5. External UVLO Threshold Voltage Setting

The high precision reset function is built in the EN pin of BD9G146MUV-LB, and arbitrary low-voltage malfunction prevention setup is possible by connecting the EN pin to resistance division of input voltage.

When you use, please set R_{EN1} and R_{EN2} to arbitrary voltage of IC turned off (V_{uv}) and turned on (V_{rel}) like below.



VIN voltage of IC turned off:

$$V_{uv} = \frac{1.31}{R_{EN2}} (R_{EN1} + R_{EN2}) \quad [V]$$

VIN voltage of IC turned on:

$$V_{rel} = \frac{1.4}{R_{EN2}} (R_{EN1} + R_{EN2}) \quad [V]$$

Figure 17. External UVLO Threshold

6. MODE Control

The MODE pin selects the operating mode. In case of using FPWM mode, set high. In case of using AUTO mode, set low or open. In case of using SYNC mode, apply a clock to this pin. When transitioning into AUTO mode from FPWM mode, the mode transitions after approximately 16 switching cycles.

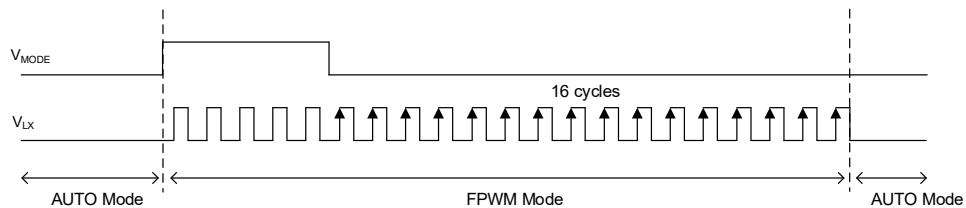


Figure 18. AUTO / FPWM Mode Transition

When transitioning into SYNC mode from AUTO or FPWM mode, the mode transitions after approximately 4 switching cycles with MODE pin. When exiting from SYNC mode, the device transitions to AUTO or FPWM mode after the clock signal is no longer detected and the internal matching condition is confirmed twice.

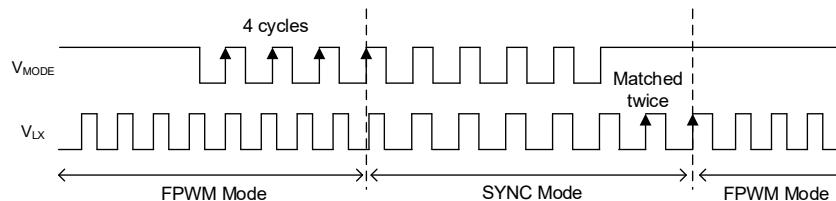


Figure 19. SYNC / FPWM Mode Transition

7. Spread Spectrum Control Generator (SSCG)

The SSCG pin selects the Spread Spectrum function. Set high to enable Spread Spectrum and set low or open to disable Spread Spectrum. When transitioning into AUTO mode from SSCG mode, the mode transitions after approximately 16 switching cycles.

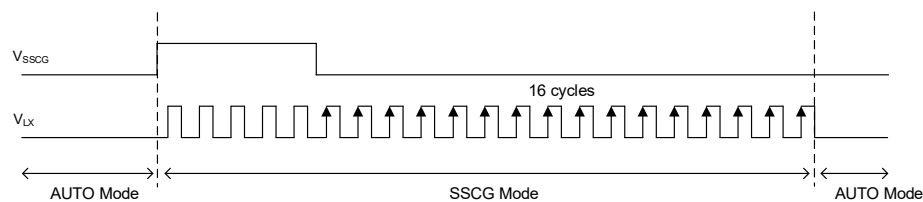


Figure 20. SSCG Mode Transition

Startup/Shutdown Timing Chart

Applying a high level to EN initiates V_{OUT} startup. When V_{OUT} reaches the PG threshold voltage, V_{PG} asserts high. V_{OUT} rises with the soft start ramp, and the startup time is determined by the soft start time corresponding to the switching frequency. Pulling EN low causes V_{OUT} to shut down and V_{PG} to assert low. V_{OUT} discharges according to the current load.

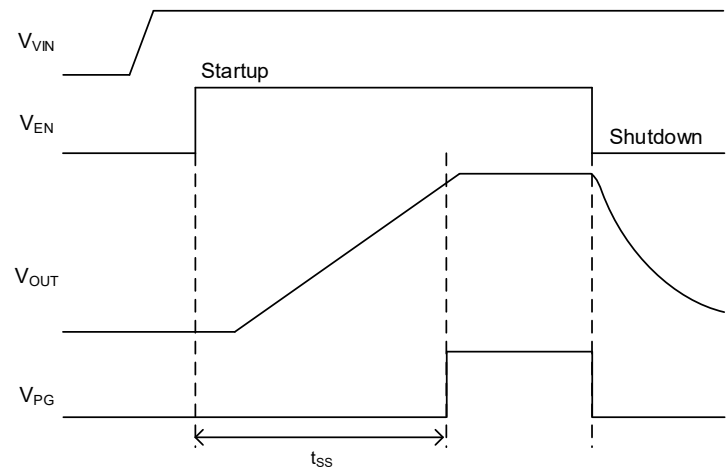


Figure 21. Startup/Shutdown Timing Chart

Application Examples

V_{OUT} = 12 V, f = 300 kHz
(All the external components can be substituted by equivalents)

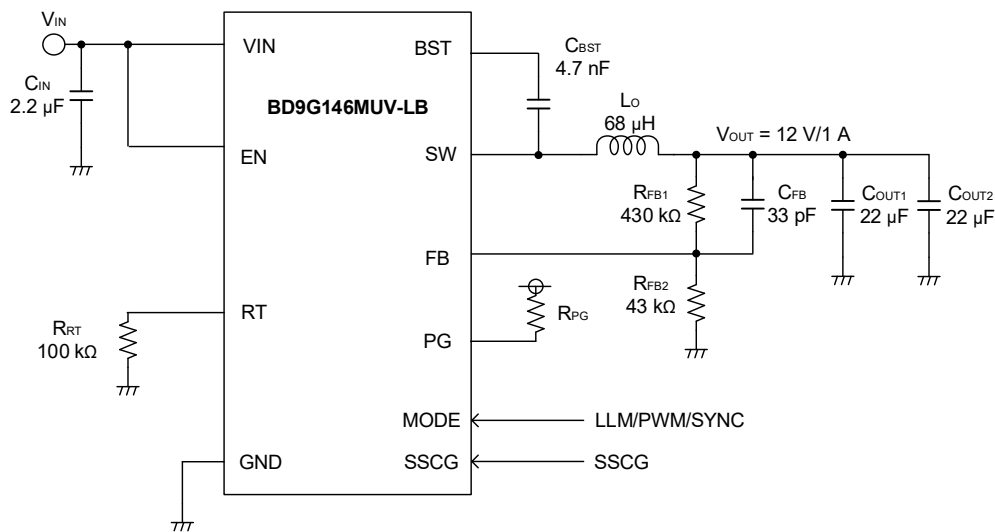


Figure 22. Application Example (V_{OUT} = 12 V, f = 300 kHz)

Table1. Parts List

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C _{IN}	3225	2.2 μF, X7R, 100 V	MBJCH32MAB7225KPPA18	Ceramic	Taiyo Yuden
C _{BST}	1005	4.7 nF, X7R, 100 V	MBASH105SB7472KFCA18	Ceramic	Taiyo Yuden
C _{FB}	1005	33 pF, C0H/CH, 50 V	MBASU105SCH330JFNA18	Ceramic	Taiyo Yuden
C _{OUT1}	3225	22 μF, X7R, 25 V	MBAST32MSB7226KPNA18	Ceramic	Taiyo Yuden
C _{OUT2}	3225	22 μF, X7R, 25 V	MBAST32MSB7226KPNA18	Ceramic	Taiyo Yuden
L _O	-	68 μH	7447714680	Inductor	WRUTH
R _{FB1}	1608	430 kΩ	MCR03EZPFX4303	Chip resistor	ROHM
R _{FB2}	1608	43 kΩ	MCR03EZPFX4302	Chip resistor	ROHM
R _{RT}	1608	100 kΩ	MCR03EZPJ104	Chip resistor	ROHM

I/O Equivalent Circuits

Pin Name	Equivalence circuit	Pin Name	Equivalence circuit
VIN		BST	
EN		PG	
RT		FB	
SW		MODE SSCG	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

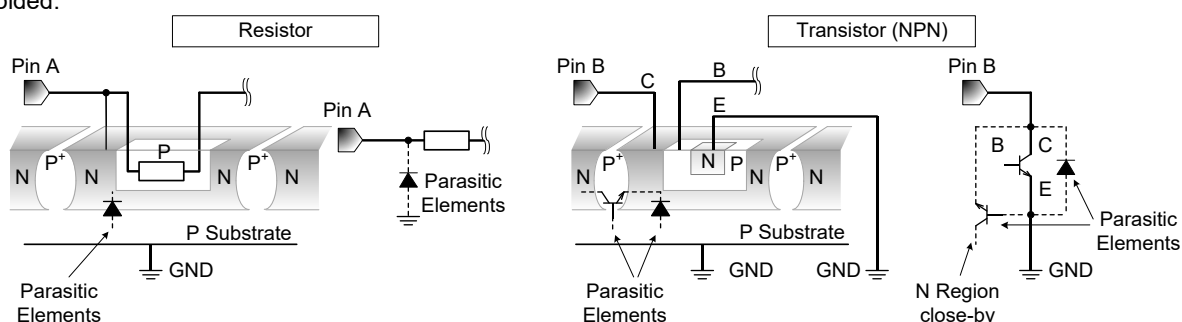


Figure 23. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

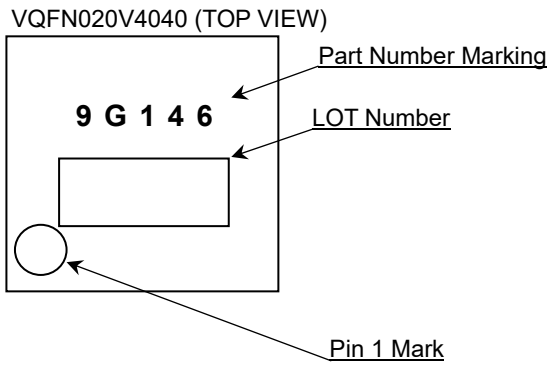
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

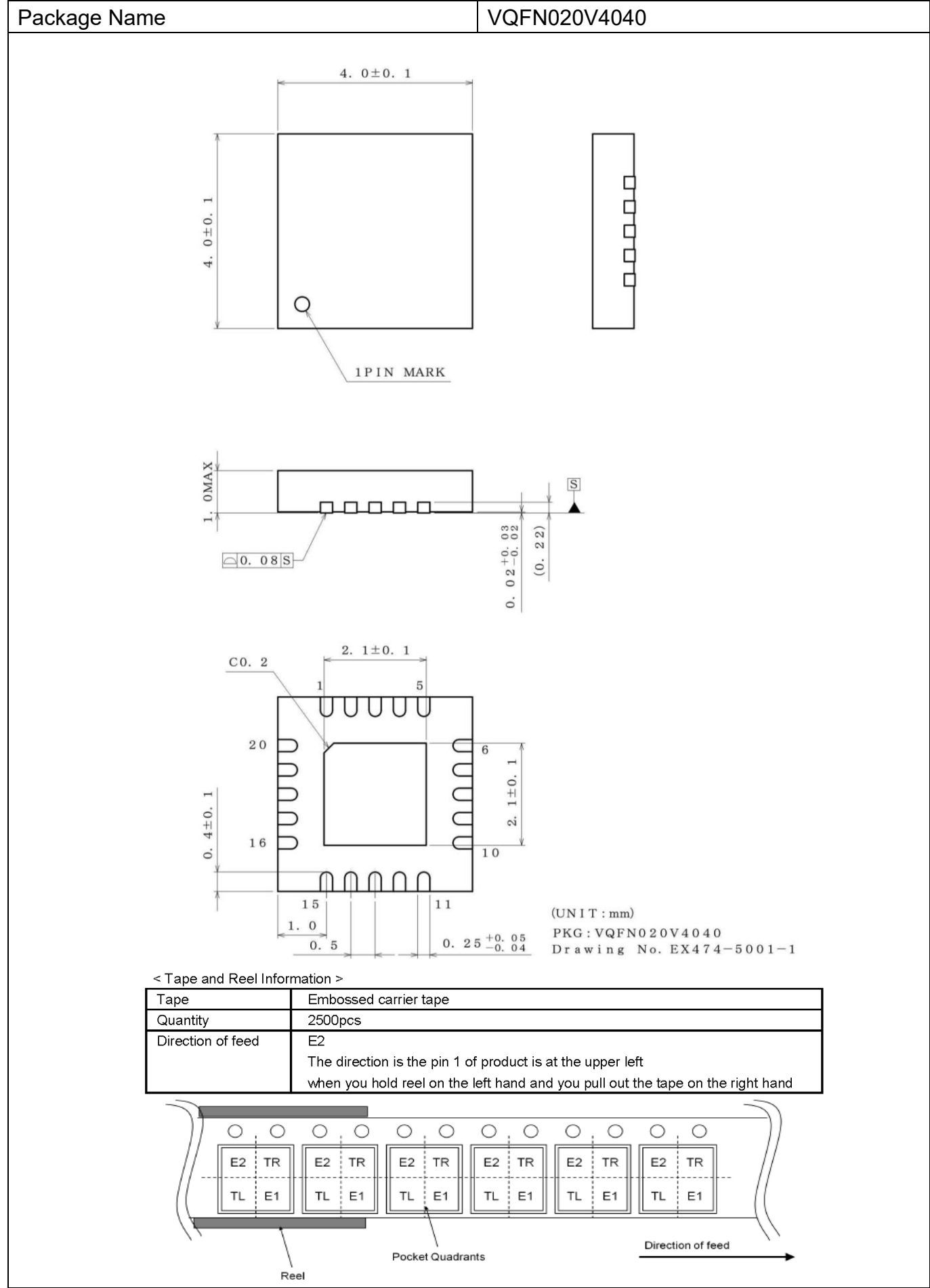
Ordering Information

B D 9 G 1 4 6 M U V										-	L B E 2			
Package					Product					Packaging and forming specification				
MUV: VQFN020V4040					LB: For industrial applications					E2: Embossed tape and reel				

Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
09.Mar.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - [a] Installation of protection circuits or other protective devices to improve system safety
 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
 - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application examples, their constants, software, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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