3.0 V to 36 V Input, 2 A Single Buck DC/DC Converter For Automotive

BD9P209NUF-C

General Description

This IC is a current mode synchronous buck DC/DC converter integrating POWER MOSFETs.

Features

- Nano Pulse Control™
- AEC-Q100 Qualified *(Note 1)*
- Functional Safety Supportive Automotive Products
- Minimum ON Pulse 45 ns (Typ)
- Synchronous Buck DC/DC Converter Integrating POWER MOSFETs
- Soft Start Function
- Current Mode Control
- Power Good Function
- Light Load Mode (LLM)
- Forced Pulse Wide Modulation (PWM) Mode
- Phase Compensation Included
- Spread Spectrum Switching
- External Synchronization Function
- Over Current Protection (OCP)
- Input Under Voltage Lockout (UVLO) Protection
- Thermal Shut Down (TSD) Protection
- Output Over Voltage Protection (OVP)
- Short Circuit Protection (SCP)

(Note 1) Grade 1

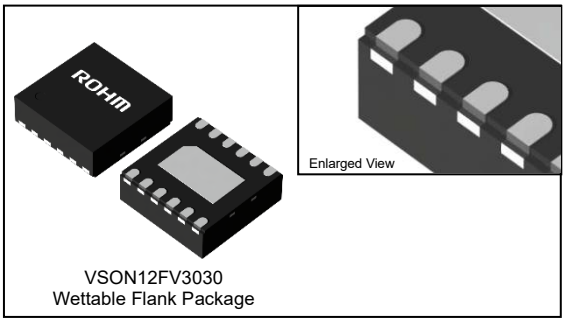
Applications

- Automotive Powered Supplies
- Consumer Powered Supplies

Key Specifications

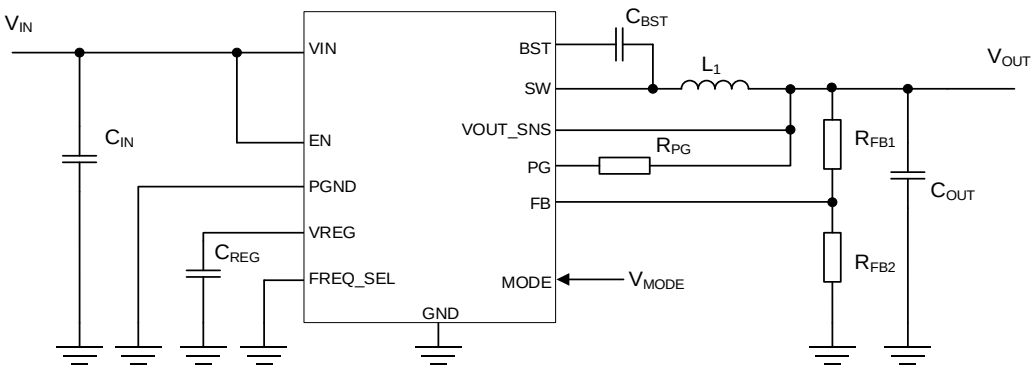
- Input Voltage Range: 3.0 V to 36 V
  (Initial startup is 3.5 V or more)
- Output Voltage Range: 1.0 V to 9.0 V
- Output Current: 2.0 A (Max)
- Switching Frequency:
  FREQ_SEL = H 400 kHz (Typ)
  FREQ_SEL = L 2.0 MHz (Typ)
- Output Voltage Accuracy: ±1.5 %
- Shutdown Current: 2.4 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VSON12FV3030	3.0 mm x 3.0 mm x 1.0 mm



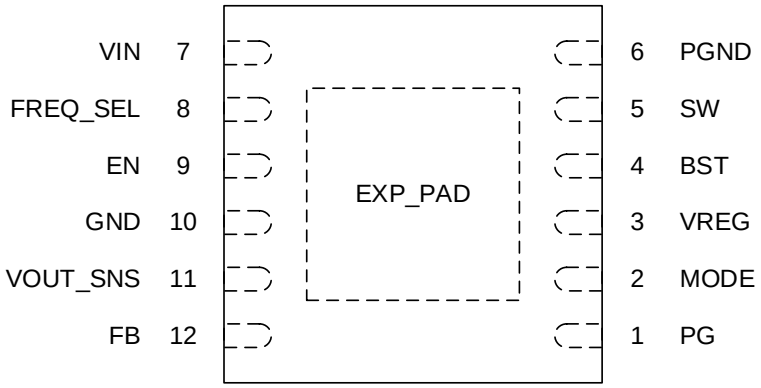
VSON12FV3030
Wettable Flank Package

Typical Application Circuits



Pin Configuration

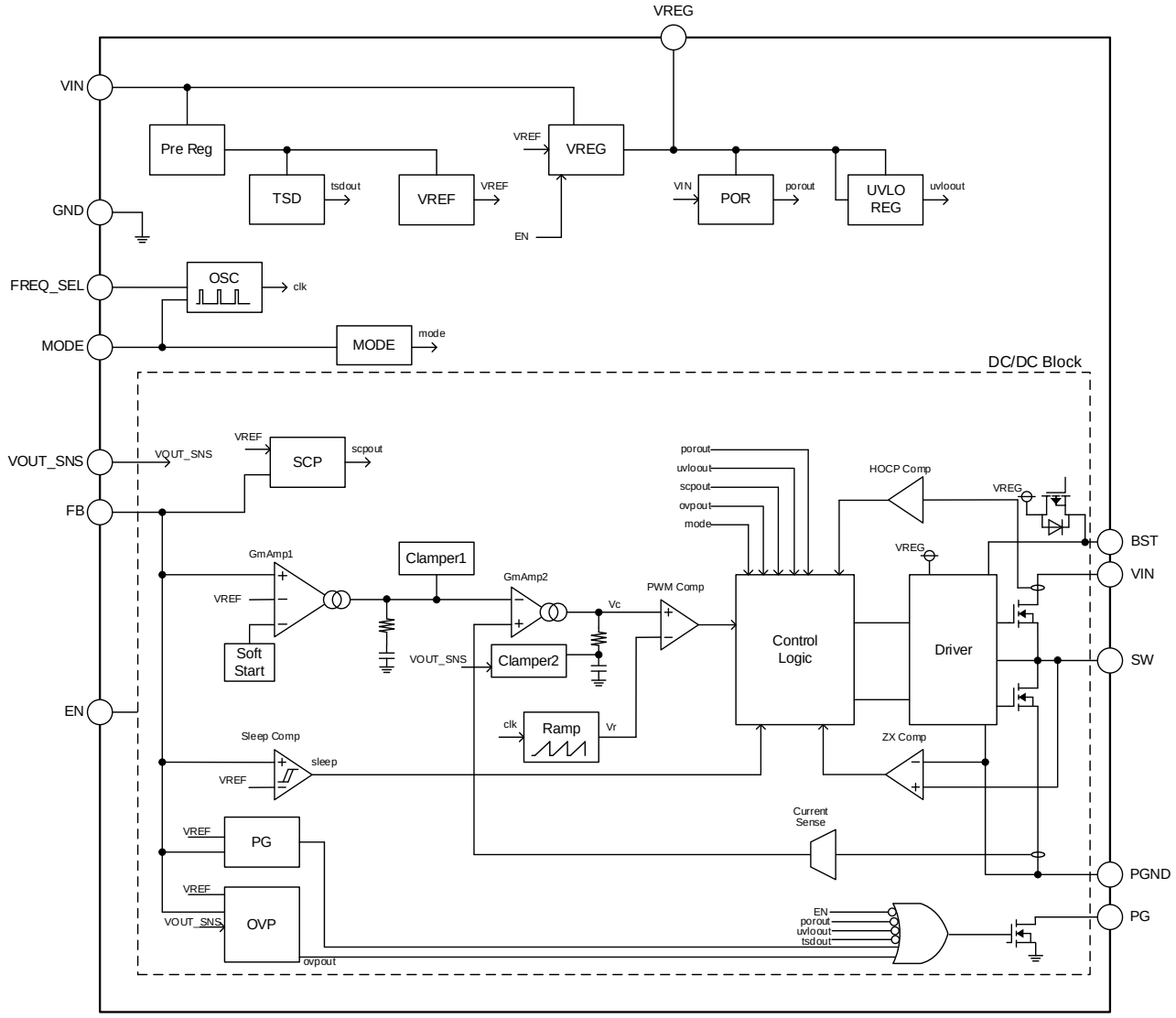
(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	PG	Output Power Good pin with open drain. Connect a pull-up resistor to the VREG pin or the power supply within the absolute maximum voltage ratings of the PG pin. Using a 5 kΩ to 100 kΩ resistance is recommended.
2	MODE	Pin to select FPWM (Forced PWM) mode, AUTO (Automatically switched between PWM mode and LLM) mode, or SYNC (Activate synchronization) mode. In case of using FPWM mode, set high level (1.5 V or higher). In case of using AUTO mode, set low level (0.5 V or lower) or open. In case of using SYNC mode, apply a clock to this pin.
3	VREG	Pin to output 3.3 V (Typ) for internal circuit. Connect a ceramic capacitor of 1.0 µF (Typ). Do not connect to any external loads except the FREQ_SEL pin, the MODE pin and a pull-up resistor to the PG pin.
4	BST	Connect a bootstrap capacitor of 0.1 µF (Typ) between this pin and the SW pins. The voltage of this capacitor is the gate drive of the High Side FET.
5	SW	Switching node pin. These pins are connected to the source of the internal High Side FET and the drain of the internal Low Side FET. Connect the power inductor and the bootstrap capacitor.
6	PGND	Ground pins for the output stage of the switching regulator.
7	VIN	Power supply input pin that is used for the output stage of the switching regulator. Connect input ceramic capacitors between the PGND pin and this pin.
8	FREQ_SEL	Pin to select switching frequency. Switching frequency is set to 400 kHz (Typ) at high level (1.5 V or higher), and 2.0 MHz (Typ) at low level (0.5 V or lower). Connect this pin to VREG (High) or GND (Low).
9	EN	Enable pin. Apply low level (0.5 V or lower) to disable device and apply high level (1.5 V or higher) to enable device. If connect this pin to another device, please inserting a limiting resistor of 10 kΩ or more.
10	GND	Ground pin.
11	VOUT_SNS	Pin to define the clamp voltage of GmAmp2 output and phase compensation. Connect this pin to the output voltage.
12	FB	Non-inverting input node of the GmAmp1. This pin is used for OVP, SCP and PG detection. Connect output voltage divider to this pin to set the output voltage.
-	EXP_PAD	A backside heat dissipation exposed pad. The EXP_PAD is connected to the P substrate of the IC. Connect this pad to the internal PCB ground plane using multiple via holes to obtain excellent heat dissipation characteristics.

Block Diagram



Description of Blocks

- Pre Reg
  This block is the internal power supply for TSD and VREF circuits.

- VREG
  This block is the internal power supply circuit. It outputs 3.3 V (Typ) and is the power supply to the control circuit and Driver.

- TSD
  This is the thermal shutdown circuit. It will shut down the device when the junction temperature (Tj) reaches to 175 °C (Typ) or more. When the Tj falls below the TSD threshold with hysteresis of 10 °C (Typ), the circuits are automatically restored to normal operation.

- VREF
  The VREF block generates the internal reference voltage.

- POR
  The POR block is power on reset for internal circuit. The IC releases power on reset and starts operation with soft start when the VIN rises to 3.35 V (Typ) or more.

- UVLO REG
  The UVLO block is for under voltage lockout protection. It will shut down the device when the VREG falls to 2.35 V (Typ) or less. This protection is released when VREG voltage increase to 2.42 V (Typ) or more.

- MODE
  This block detects the MODE pin signal and controls switching mode. When the MODE pin is high level (1.5 V or higher) or is applied external clock, switching operation becomes forced PWM mode regardless load current. When the MODE pin is open or low level (0.5 V or lower), switching operation changes between PWM and light load operation depending on load current.

- OSC
  This block generates the clock frequency. When the clock is applied to the MODE pin, it synchronizes to external clock.

- OVP
  This is the output over voltage protection (OVP) circuit. When FB pin voltage rises to 0.86 V (Typ) or more, V_{OUT} is reduced by forced PWM switching. After FB pin voltage falls to 0.84 V (Typ) or less, the operation recovers into normal condition. Or, when VOUT_SNS pin voltage 9.75 V (Typ) or more, V_{OUT} is reduced by forced PWM switching. After VOUT_SNS pin voltage falls 9.5 V (Typ) or less, the circuit operation recovers into normal condition.

- SCP
  This is the short circuit protection circuit. After soft start is completed, the switching is disabled if the output voltage falls SCP threshold voltage or less for 1 ms (FREQ_SEL = L, Typ) / 1.2 ms (FREQ_SEL = H, Typ). This short circuit protection is maintained for 32 ms (FREQ_SEL = L, Typ) / 41 ms (FREQ_SEL = H, Typ) and then automatically released.

- Soft Start
  This function starts up the output voltage taking 3 ms (FREQ_SEL = L, Typ) / 3.75 ms (FREQ_SEL = H, Typ) to prevent the overshoot.

- GmAmp1
  This block is an error amplifier and its inputs are the reference voltage 0.8 V (Typ) and the FB voltage.

- GmAmp2
  This block sends the signal Vc which is composed of the GmAmp1 output and the current sense signal to PWM Comp.

- Clamper1
  This block clamps GmAmp1 output voltage and inductor current. It works as the over current protection and LLM control current.

- Clamper2
  This block clamps GmAmp2 output voltage.

- Current Sense
  This block detects the amount of change in inductor current through the Low Side FET and sends a current sense signal to GmAmp2.

- PWM Comp
  This block compares the output voltage of the GmAmp2 (Vc) and the saw tooth waveform (Vr) to control the switching duty.

Description of Blocks - continued

- Ramp
  This block generates the saw tooth waveform (Vr) from the clock signal generated by OSC.

- Control Logic
  This block controls switching operation and protection functions.

- Driver
  This circuit drives the gates of the output FETs.

- Sleep Comp
  If feedback voltage becomes 0.810 V（Typ) or more, this block puts the device into SLEEP state. This state is released when output/feedback voltage becomes 0.808 V (Typ) or less.

- ZX Comp
  This block stops the switching by detecting reverse current of the SW current at LLM control.

- HOCP Comp
  This block detects the current flowing through the High Side FET and limits the current of 2.4 A (Min) or more. This function works in abnormal situation such as the SW pin shorted to GND condition in order to prevent the High Side FET from destruction.

- PG
  When the FB pin voltage reaches 0.765 V (Typ) or more of the normal regulation voltage, the open drain MOSFET connected to the PG pin turns off in 4.1 ms (FREQ_SEL = L, Typ) / 5.1 ms (FREQ_SEL = H, Typ) and the output of the PG pin becomes high by its external pull-up resistor.
  When the FB pin voltage reaches 0.745 V (Typ) or less, the PG pin open drain MOSFET turns on and the PG pin is pulled down with an impedance of 190 Ω (Typ).

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	-0.3 to +42	V
EN Voltage	V_{EN}	-0.3 to +42	V
BST Voltage	V_{BST}	-0.3 to +46.5	V
Voltage from SW to BST	ΔV_{BST}	V_{SW} -0.3 to V_{SW} +4.5	V
SW Voltage	V_{SW}	-0.3 to +42	V
FB, FREQ_SEL Voltage	V_{FB}, V_{FREQ_SEL}	-0.3 to +4.5	V
MODE, PG Voltage	V_{MODE}, V_{PG}	-0.3 to +7	V
VOUT_SNS Voltage	V_{VOUT_SNS}	-0.3 to +20	V
VREG Voltage	V_{REG}	-0.3 to +4.5	V
Storage Temperature Range	Tstg	-55 to +150	˚C
Maximum Junction Temperature	Tjmax	150	˚C
Human Body Model (HBM)*(Note 1)*	V_{ESD_HBM}	±2000	V

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) These voltages are guaranteed by design. Not tested.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
VSON12FV3030				
Junction to Ambient	θ_{JA}	180.9	45.9	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	12	5	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{IN}	3.0	-	36	V
Operating Temperature	Ta	-40	-	+125	˚C
Output Voltage *(Note 1)*	V_{OUT}	1.0	-	9.0	V
SW Minimum ON Time *(Note 2)*	t_{ONMIN}	-	45	80	ns
SW Minimum OFF Time *(Note 2)*	t_{OFFMIN}	-	85	120	ns
Output Current	I_{OUT}	-	-	2.0	A
Input Capacitor *(Note 3)*	C_{IN}	2.4	-	-	µF
VREG Capacitor *(Note 3)*	C_{REG}	0.6	1.0	2.0	µF
BST Capacitor *(Note 3)*	C_{BST}	0.05	0.10	0.20	µF

(Note 1) Although the output voltage is configurable at 1.0 V and higher, it may be limited by the SW min ON pulse width.
For the same reason, although the output voltage is configurable at 9.0 V and more, it may be limited by the SW minimum OFF pulse width.
(Note 2) Not tested.
(Note 3) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered.

Electrical Characteristics (Unless otherwise specified Tj = -40 ˚C to +150 ˚C, V_{IN} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Shutdown Current	I_{SDWN}	-	2.4	10.0	µA	V_{EN} = 0 V Tj = -40 ˚C to +125 ˚C
Quiescent Current from VIN	I_{Q_VIN1}	-	7.1	20.0	µA	V_{MODE} = 0 V V_{FB} = V_{FB1} x 1.04 (SLEEP)
	I_{Q_VIN2}	-	1500	3000	µA	V_{MODE} = 3.3 V V_{FB} = V_{FB1} x 1.04 (No SLEEP)
VIN Power On Reset Rising	V_{POR_R}	3.20	3.35	3.50	V	V_{IN} Sweep Up
VIN Power On Reset Falling	V_{POR_F}	2.70	2.85	3.00	V	V_{IN} Sweep Down
VREG Under Voltage Lockout Falling	V_{UVLO_F}	2.20	2.35	2.45	V	V_{REG} Sweep Down
VREG Under Voltage Lockout Rising	V_{UVLO_R}	2.30	2.42	2.55	V	V_{REG} Sweep Up
EN/MODE/FREQ_SEL						
EN Input Voltage High	V_{ENH}	1.5	-	36.0	V	
EN Input Voltage Low	V_{ENL}	0	-	0.5	V	
EN Hysteresis Voltage	V_{ENHYS}	0.05	0.25	0.50	V	
EN Input Current	I_{EN}	-	0	5	µA	V_{EN} = 5 V
MODE Input Voltage High	V_{MODEH}	1.5	-	5.5	V	
MODE Input Voltage Low	V_{MODEL}	0	-	0.5	V	
MODE Input Current	I_{MODE}	-	3.3	7.0	µA	V_{MODE} = 3.3 V
FREQ_SEL Input Voltage High	V_{SELH}	1.5	-	5.5	V	
FREQ_SEL Input Voltage Low	V_{SELL}	0	-	0.5	V	
FREQ_SEL Input Current	I_{SEL}	-	0	1	µA	V_{FREQ_SEL} = 3.3 V
VREG						
VREG Voltage	V_{REG}	3.0	3.3	3.6	V	
Oscillator						
Switching Frequency	f_{SWL}	1.8	2.0	2.2	MHz	V_{FREQ_SEL} = 0 V
	f_{SWH}	360	400	440	kHz	V_{FREQ_SEL} = 3.3 V
Synchronization Frequency Range	f_{SW_EXL}	1.8	-	2.5	MHz	External Clock Input, V_{FREQ_SEL} = 0 V
	f_{SW_EXH}	350	-	530	kHz	External Clock Input, V_{FREQ_SEL} = 3.3 V
Switching Frequency (Spread Spectrum)	f_{SWSSRL}	1.8	-	2.5	MHz	V_{FREQ_SEL} = 0 V
	f_{SWSSRH}	350	-	530	kHz	V_{FREQ_SEL} = 3.3 V
Spread Spectrum Modulation Rate	Δf_{SSCG}	-	8.5	-	%	
Spread Spectrum Modulation Cycle	t_{SSCG_CYCLEL}	-	512	-	µs	V_{FREQ_SEL} = 0 V
	t_{SSCG_CYCLEH}	-	640	-	µs	V_{FREQ_SEL} = 3.3 V

Electrical Characteristics - continued (Unless otherwise specified Tj = -40 ˚C to +150 ˚C, V_{IN} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VREF/GmAmp						
Feedback Reference Voltage	V_{FB1}	0.788	0.800	0.812	V	V_{FB} Voltage, PWM Mode
Enter SLEEP State Voltage	V_{FB2}	0.794	0.810	0.826	V	V_{FB} Rising, Light Load Mode
Exit SLEEP State Voltage	V_{FB3}	0.792	0.808	0.824	V	V_{FB} Falling, Light Load Mode
FB Input Current	I_{FB}	-0.1	0	+0.1	µA	V_{FB} = 0.9 V
VOUT_SNS Input Current	I_{VOUT_SNS}	-	0	2.0	µA	V_{VOUT_SNS} = 5.0 V Light Load Mode
Start Delay Time	t_{DLYL}	-	250	600	µs	V_{FREQ_SEL} = 0 V
	t_{DLYH}	-	300	700	µs	V_{FREQ_SEL} = 3.3 V
Soft Start Time	t_{SSL}	2.10	3.00	3.90	ms	V_{FB1} x 0.1 to V_{FB1} x 0.9, V_{FREQ_SEL} = 0 V
	t_{SSH}	2.60	3.75	4.90	ms	V_{FB1} x 0.1 to V_{FB1} x 0.9, V_{FREQ_SEL} = 3.3 V
Driver						
High Side FET ON Resistance	R_{ONH}	-	170	422	mΩ	V_{BST}-V_{SW} = 3.3 V
Low Side FET ON Resistance	R_{ONL}	-	125	310	mΩ	
Over Current Protection Threshold	I_{OCP}	2.20	2.80	3.25	A	
PG						
PG Threshold Voltage Low	V_{PGL}	0.720	0.745	0.770	V	V_{FB} Sweep Down
PG Threshold Voltage High	V_{PGH}	0.740	0.765	0.790	V	V_{FB} Sweep Up
PG Leakage Current	I_{PGLK}	-1	0	+1	µA	V_{PG} = 3.3 V, V_{FB} = 0.8 V
PG ON Resistance	R_{PG}	-	190	400	Ω	I_{PG} = 1 mA
PG Active Time	t_{PGACTL}	2.7	4.1	5.5	ms	V_{FREQ_SEL} = 0 V
	t_{PGACTH}	3.2	5.1	7.0	ms	V_{FREQ_SEL} = 3.3 V
PG Filtering Time	$t_{PGFILTL}$	72	144	216	µs	V_{FREQ_SEL} = 0 V
	$t_{PGFILTH}$	90	180	270	µs	V_{FREQ_SEL} = 3.3 V
OVP/SCP						
FB OVP Threshold Voltage High	V_{OVPH}	0.825	0.860	0.895	V	V_{FB} Sweep Up
FB OVP Threshold Voltage Low	V_{OVPL}	0.805	0.840	0.875	V	V_{FB} Sweep Down
VOUT_SNS OVP Threshold Voltage High	$V_{SNSOVPH}$	9.35	9.75	10.15	V	V_{VOUT_SNS} Sweep Up
VOUT_SNS OVP Threshold Voltage Low	$V_{SNSOVPL}$	9.10	9.50	9.90	V	V_{VOUT_SNS} Sweep Down
SCP Threshold Voltage High	V_{SCPH}	0.680	0.720	0.760	V	V_{FB} Sweep Up
SCP Threshold Voltage Low	V_{SCPL}	0.600	0.640	0.680	V	V_{FB} Sweep Down
SCP Deactivate Rate of VIN/VOUT_SNS	V_{SCP_DACTH}	1.53	1.67	1.81	V/V	SCP function is activated this value or more.
	V_{SCP_DACTL}	1.50	1.64	1.78	V/V	SCP function is deactivated this value or less.

Typical Performance Curves

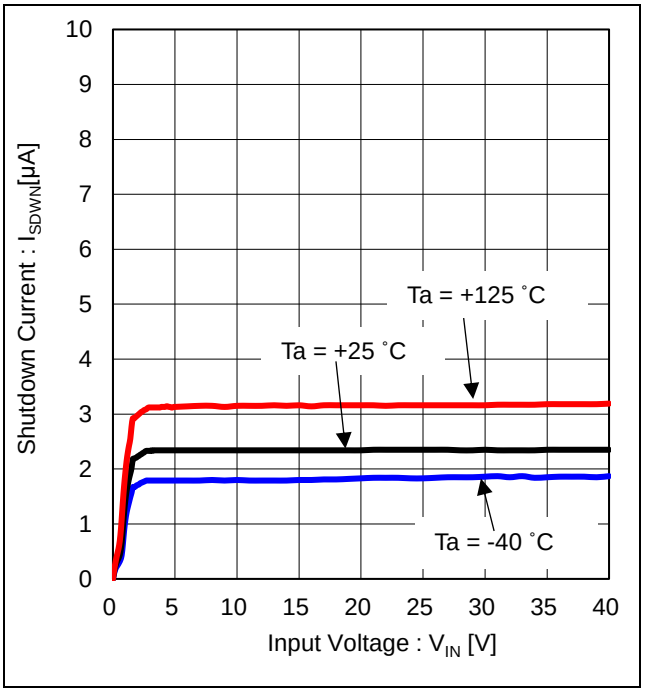


Figure 1. Shutdown Current vs Input Voltage

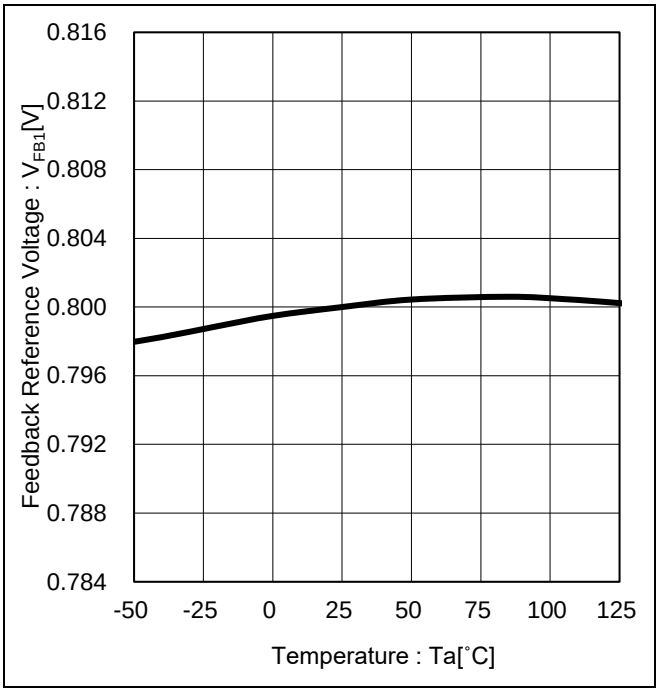


Figure 2. Feedback Reference Voltage vs Temperature

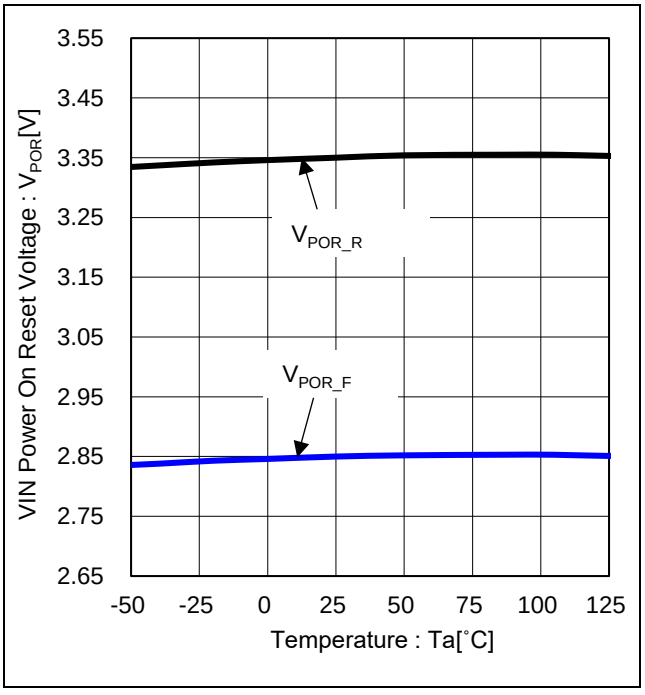


Figure 3. VIN Power On Reset Voltage vs Temperature

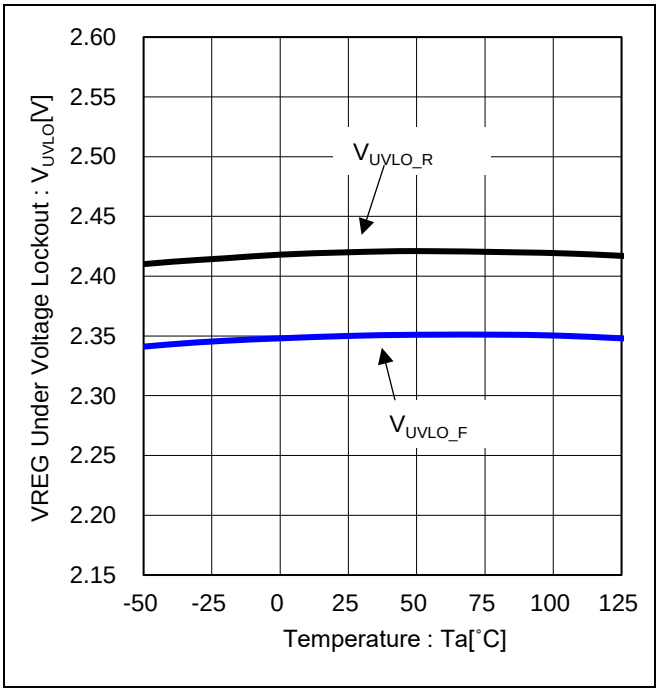


Figure 4. VREG Under Voltage Lockout vs Temperature

Typical Performance Curves - continued

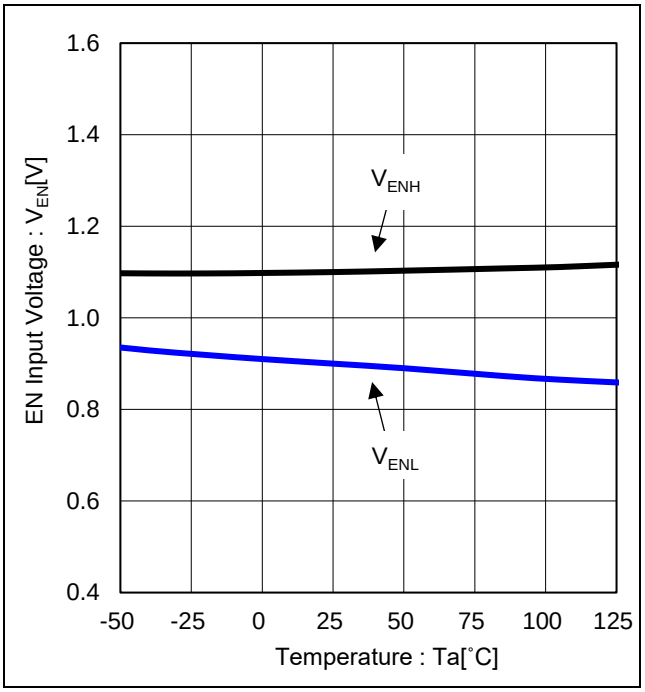


Figure 5. EN Input Voltage vs Temperature

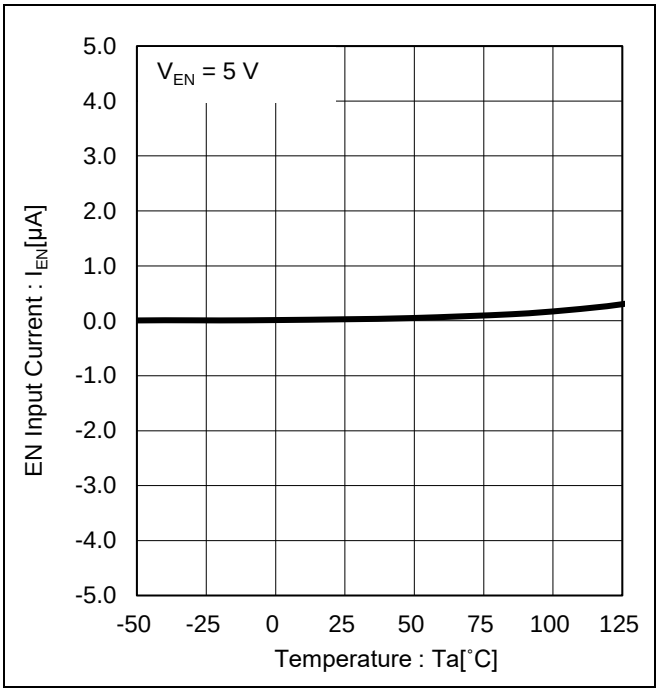


Figure 6. EN Input Current vs Temperature

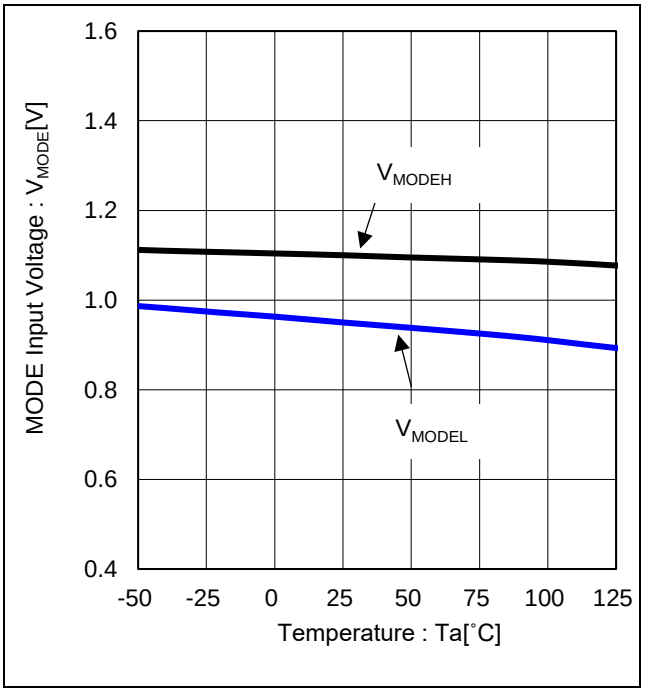


Figure 7. MODE Input Voltage vs Temperature

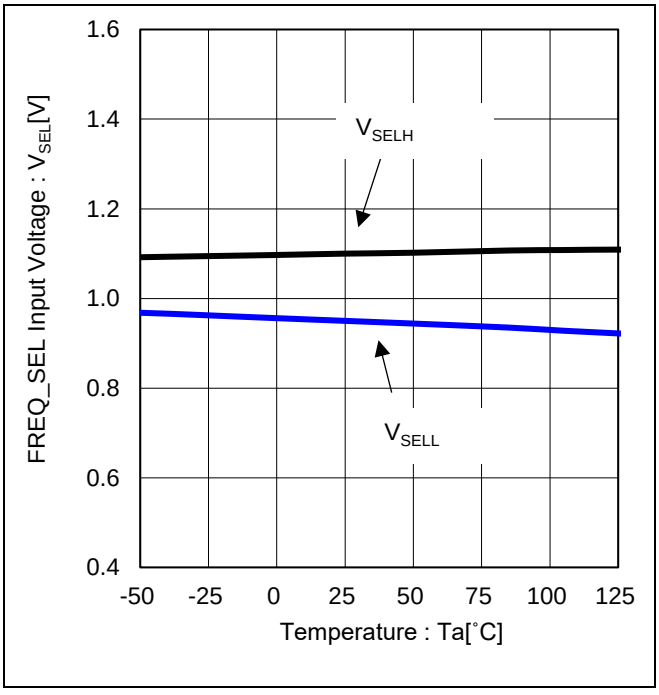


Figure 8. FREQ_SEL Input Voltage vs Temperature

Typical Performance Curves - continued

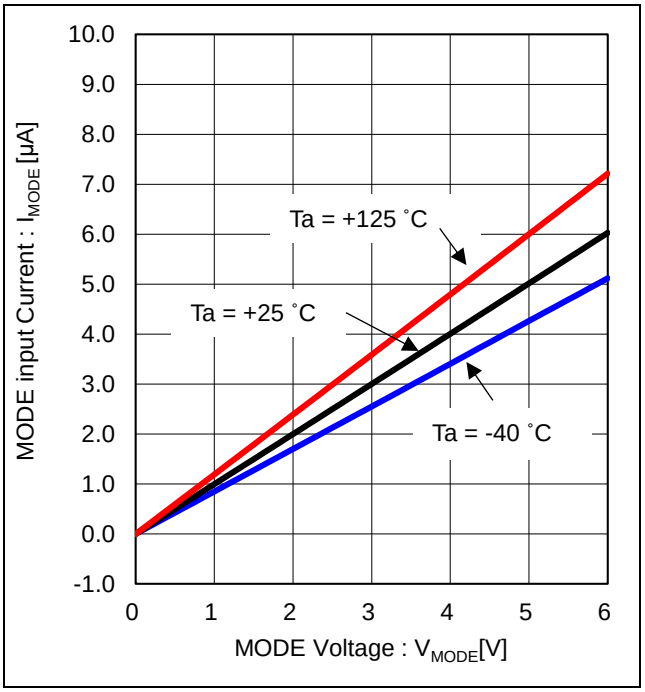


Figure 9. MODE Input Current vs MODE Voltage

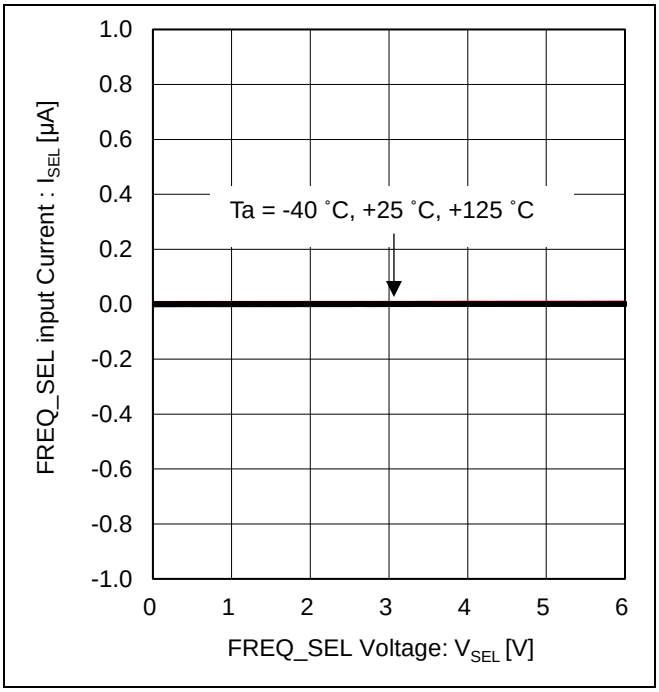


Figure 10. FREQ_SEL Input Current vs FREQ_SEL Voltage

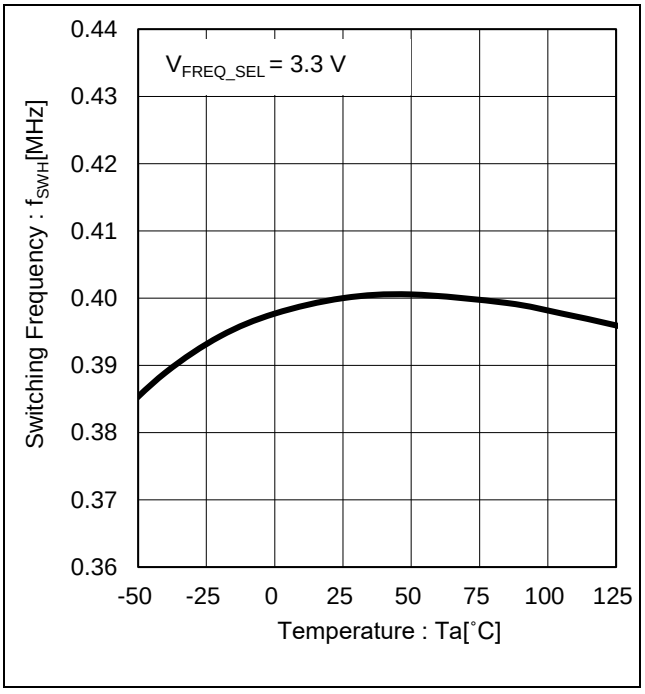


Figure 11. Switching Frequency(f_{SWH}) vs Temperature

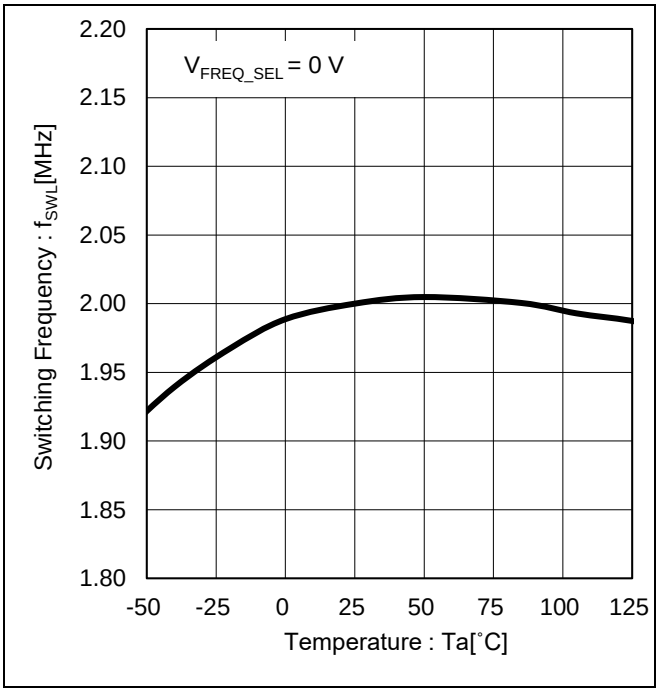


Figure 12. Switching Frequency(f_{SWL}) vs Temperature

Typical Performance Curves - continued

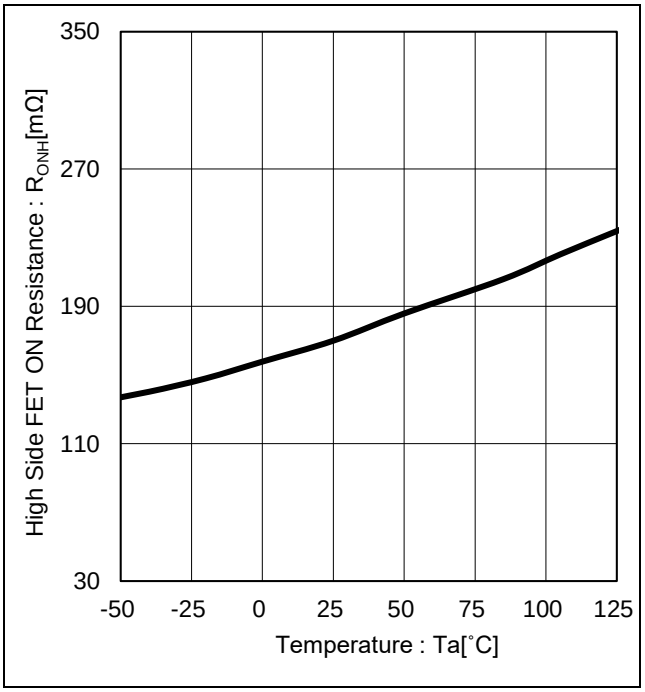


Figure 13. High Side FET ON Resistance vs Temperature

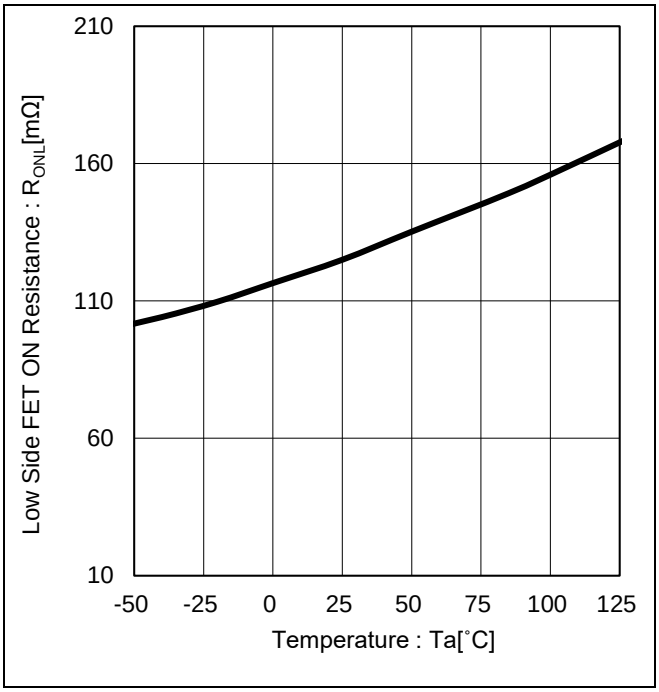


Figure 14. Low Side FET ON Resistance vs Temperature

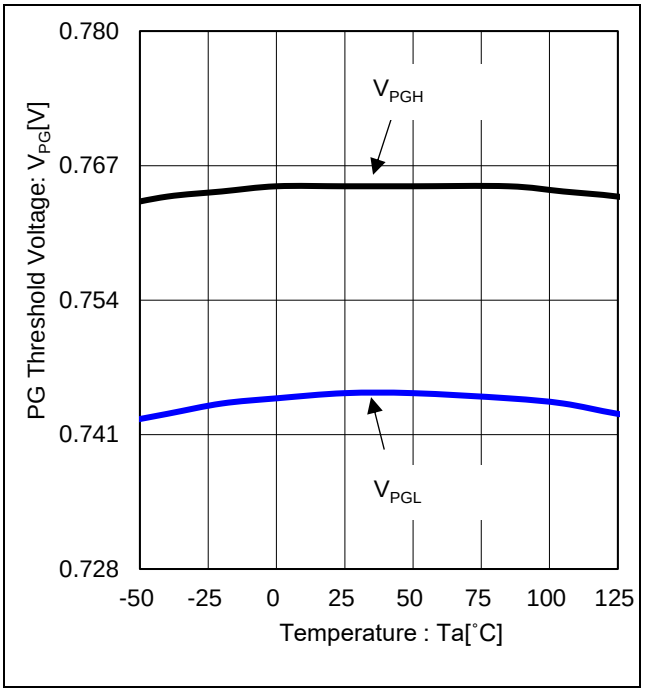


Figure 15. PG Threshold Voltage vs Temperature

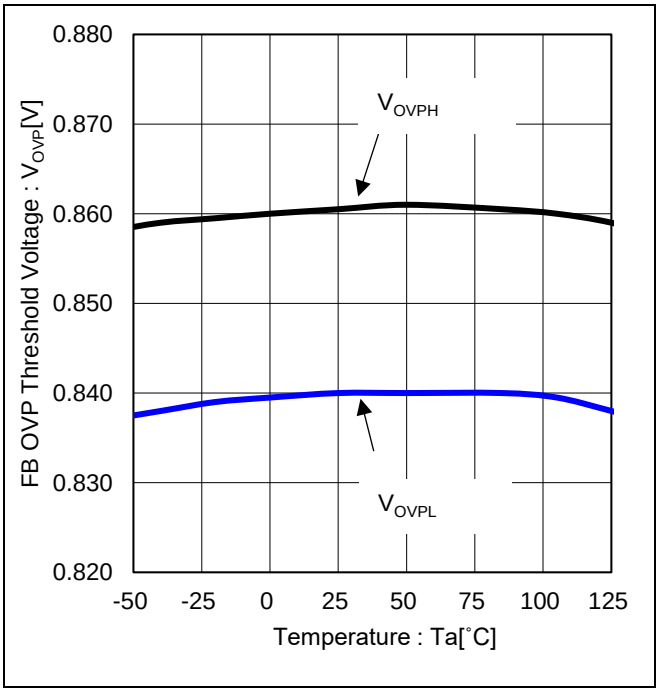


Figure 16. FB OVP Threshold Voltage vs Temperature

Typical Performance Curves - continued

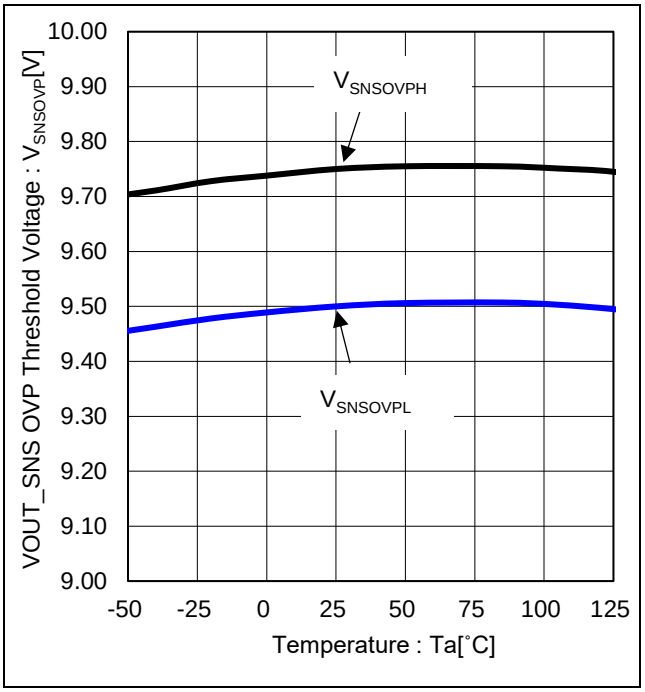


Figure 17. VOUT_SNS OVP Threshold Voltage vs Temperature

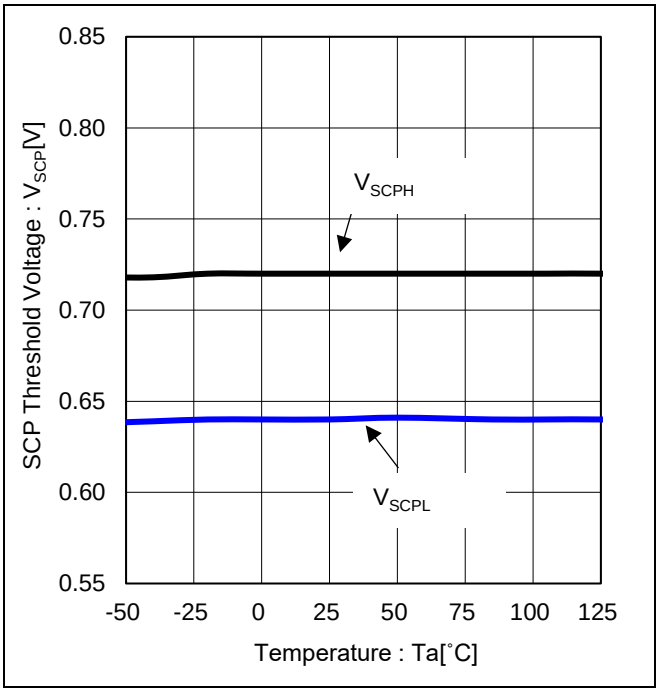


Figure 18. SCP Threshold Voltage vs Temperature

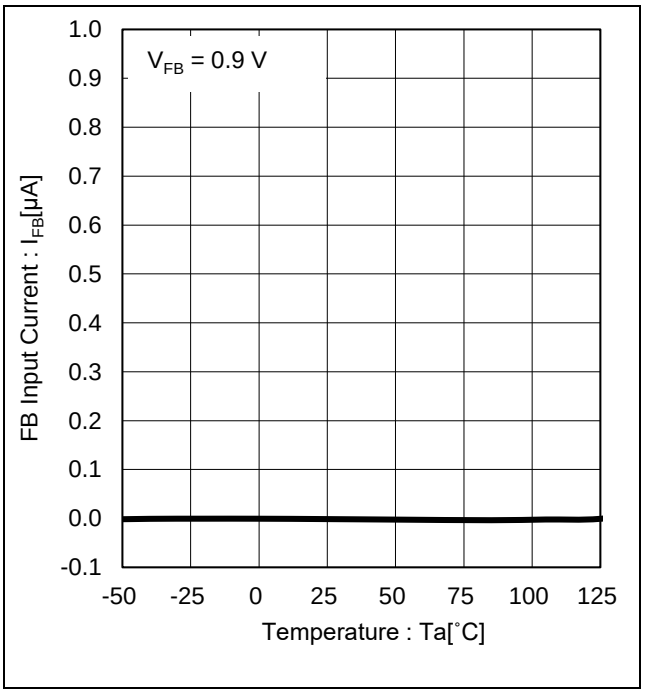


Figure 19. FB Input Current vs Temperature

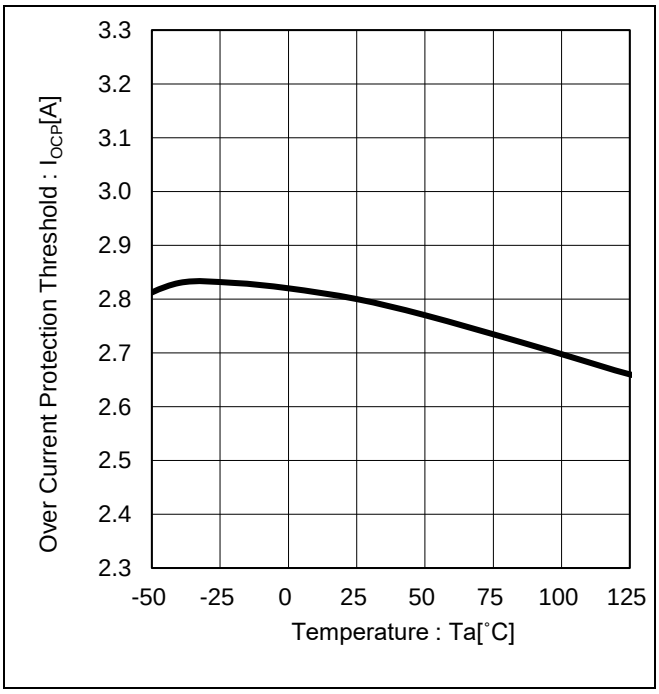


Figure 20. Over Current Protection Threshold vs Temperature

Typical Performance Curves - continued

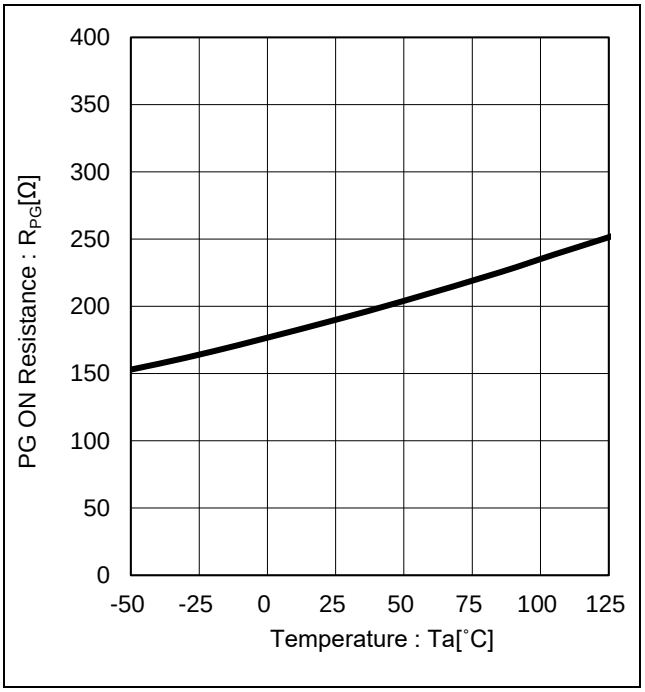


Figure 21. PG ON Resistance vs Temperature

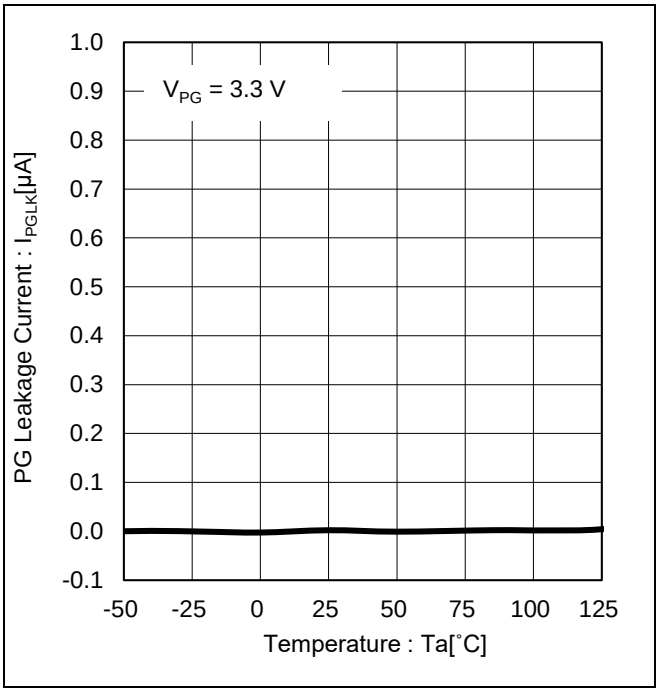


Figure 22. PG Leakage Current vs Temperature

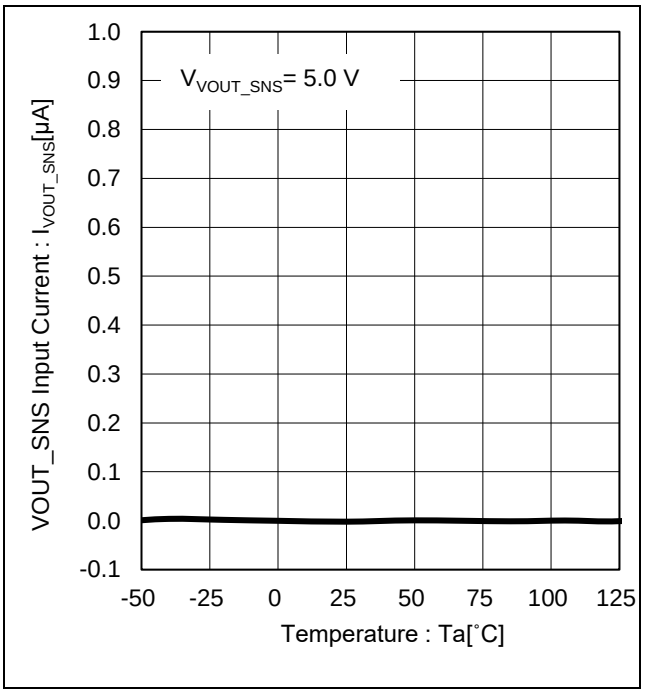


Figure 23. VOUT_SNS Input Current vs Temperature

Function Explanation

1. Nano Pulse Control™
   Nano Pulse Control™ is an original technology developed by ROHM Co., Ltd. It enables to control voltage stably, which is difficult in the conventional technology, even in a narrow SW ON time such as less than 50 ns at typical condition. Narrow SW ON Pulse enables direct convert of high input voltage to low output voltage. The output voltage V_{OUT} 3.3 V can be output directly from the supply voltage V_{IN} 24 V at 2.0 MHz.

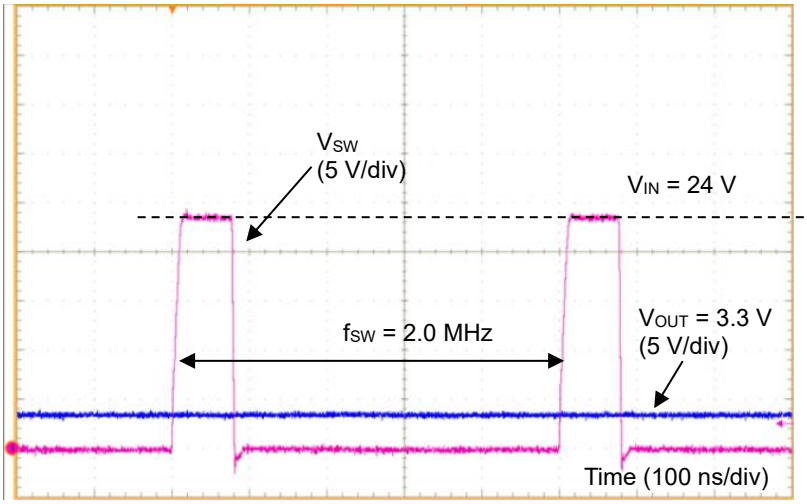


Figure 24. Switching Waveform (V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 1.0 A, f_{SW} = 2.0 MHz)

2. Light Load Mode Control and Forced PWM Mode Control
   Synchronous DC/DC converter with integrated POWER MOSFETs and realizes high transient response by using current mode Pulse Width Modulation (PWM) mode control architecture. Under a heavy load, the switching operation is performed with the PWM mode control at a fixed frequency. When the load is lighter, the operation is changed over to the Light Load Mode (LLM) control to improve the efficiency.

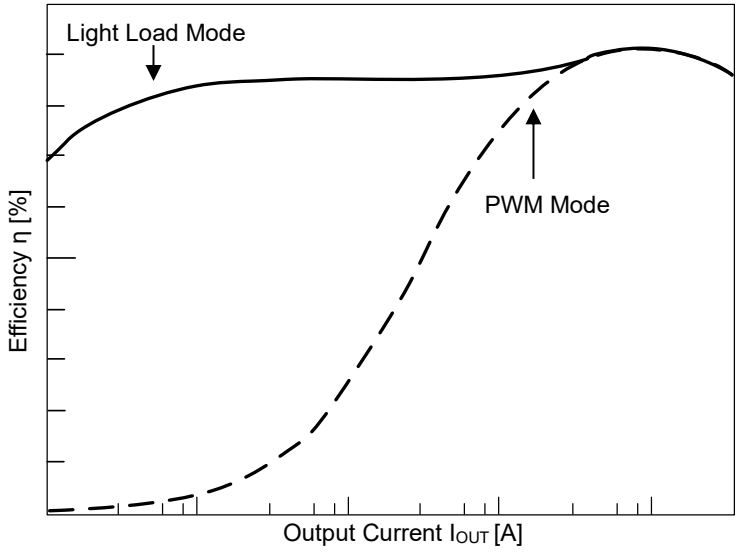


Figure 25. Efficiency (Light Load Mode, PWM Mode)

2. Light Load Mode Control and Forced PWM Mode Control - continued

If the output load decreases below 400 mA (Typ), the output voltage rises and power state is changed to SLEEP state when the output voltage exceeds to V_{FB2} (0.810 V of its setting voltage V_{FB1}). During SLEEP state, switching operation is stopped and the circuit current is reduced by stopping the circuit operation except for the monitor circuit of output voltage monitor. Then, the switching operation restarts when the output voltage decreases less than V_{FB3} (0.808 V of its setting voltage V_{FB1}) by the load current.

If the light load mode operation is not required, the IC operates in forced PWM mode by applying high voltage or an external clock to the MODE pin. In forced PWM mode, the IC operates with fixed frequency regardless of the output load and the ripple voltage of output can be reduced. Also, during soft start time, the IC operates in forced PWM mode regardless of the condition of the MODE pin. After detecting PG high, the IC operates according to the MODE pin condition.

In addition, good EMI performance in radio AM band may not be provided by a load condition in LLM. To avoid this, use Forced PWM mode.

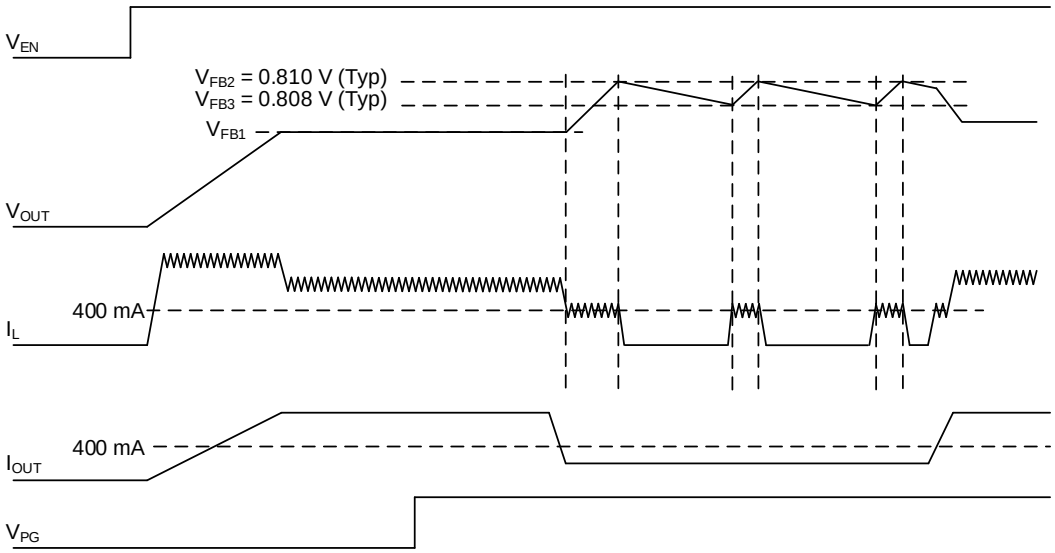


Figure 26. Timing Chart in Light Load Mode

Function Explanation - continued

3. Enable Control

The device shutdown can be controlled by the EN pin. When V_{EN} reaches V_{ENH} (1.5 V) or more, the internal circuit is activated. The V_{OUT} starts up with soft start operation. The delay time is implemented from the EN pin becoming high to V_{OUT} starting up. The delay time is t_{DLYL} (250 µs, Typ) when the FREQ_SEL pin is Low, and t_{DLYH} (300 µs, Typ) when the FREQ_SEL pin is High.

The soft start time (V_{OUT} x 0.1 to V_{OUT} x 0.9) is set to t_{SSL} (3.0 ms, Typ) when the FREQ_SEL pin is Low, and t_{SSH} (3.75 ms, Typ) when the FREQ_SEL pin is High. When an EN voltage becomes V_{ENL} (0.5 V) or less, the device is shutdown.

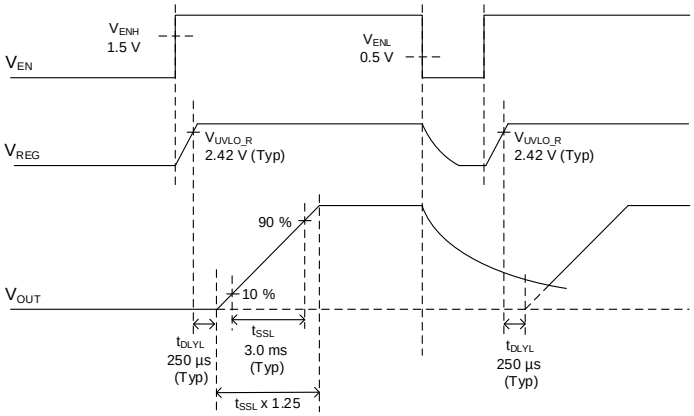


Figure 27. Enable ON/OFF Timing Chart (FREQ_SEL = L)

4. Power Good (PG) Function

The power good function monitors the FB pin voltage. When the FB pin voltage reaches V_{PGH} (0.765 V, Typ) or more, the open drain MOSFET on the PG pin is turned off in t_{PGACTL} (4.1 ms, Typ) when the FREQ_SEL pin is Low, and the output of the PG pin becomes high by its pull-up resistor. In addition, when the FB pin voltage reaches V_{PGL} (0.745 V, Typ) or less, the open drain MOSFET on the PG pin is turned on and the PG pin is pulled down with an impedance of R_{PG} (190 Ω, Typ). When the FREQ_SEL pin is High, the PG pin is turned off in t_{PGACTH} (5.1 ms, Typ). To reject noise, the filtering time is implemented after the FB pin voltage decreases below its threshold voltage (V_{PGL}). The filtering time is $t_{PGFILTL}$ (144 µs, Typ) when the FREQ_SEL pin is Low, and $t_{PGFILTH}$ (180 µs, Typ) when the FREQ_SEL pin is High.

The power good function also works when output over voltage is detected. If the FB pin voltage reaches V_{OVPH} (0.860 V, Typ) or more, the open drain MOSFET on the PG pin is turned on. Then, when the FB pin voltage goes below V_{OVPL} (0.840 V, Typ) or less, the open drain MOSFET on the PG pin is turned off. The power good active time and filtering time are activated when over voltage conditions are detected.

The PG output voltage low level ($V_{PG\_LOW\ (Max)}$) when the open drain MOSFET is turned on is calculated by the following equation. It is recommended to use resistance of 5 kΩ to 100 kΩ and pull it up to the VREG pin or the power supply in the absolute maximum voltage ratings of the PG pin. During shutdown condition, the PG pin is pulled down regardless the output voltage as far as V_{IN} is 2 V or higher.

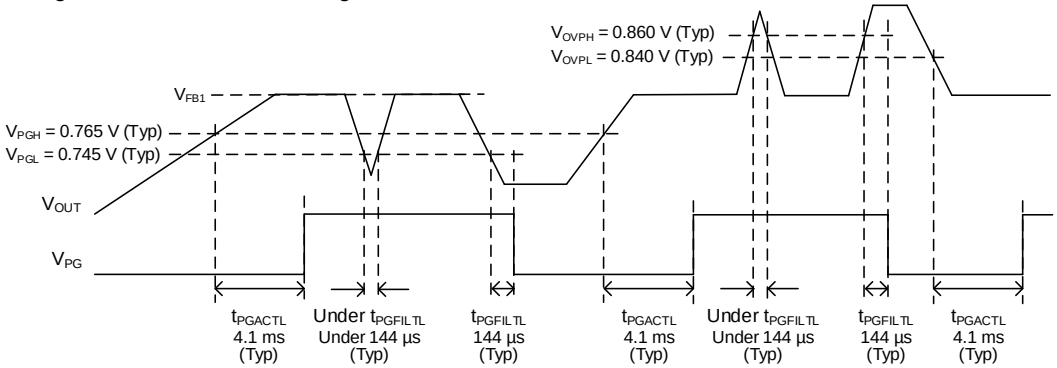


Figure 28. Power Good Timing Chart (FREQ_SEL = L)

$$V_{PG\_LOW(Max)} = V_{PULL-UP} \times \frac{R_{PG(Max)}}{R_{PG(Max)}+R_{PULL-UP}}\ [V]$$

Where:

$V_{PG\_LOW(Max)}$	is the PG Low voltage level (Max) [V]
$V_{PULL-UP}$	is the Voltage of pull-up power source [V]
$R_{PG(Max)}$	is the PG ON Resistance (Max) [Ω]
$R_{PULL-UP}$	is the value of pull-up resistor to V_{PULL_UP} [Ω]

Function Explanation - continued

5. External Synchronization Function

By inputting a clock signal to the MODE pin, the switching frequency can be synchronized with the external clock signal. When the FREQ_SEL pin is Low, a clock signal with a frequency range of 1.8 MHz to 2.5 MHz and the duty range between 25 % to 75 %. When the FREQ_SEL pin is High, a clock signal with a frequency range of 350 kHz to 530 kHz and the duty range between 25 % to 75 %. Synchronous mode starts after four rising edges of the clock signal. This function becomes active after V_{PG} goes High. If the interval between rising edges is 0.9 µs (Typ) or more when the FREQ_SEL pin is Low, or 4.1 µs (Typ) or more when the FREQ_SEL pin is High, synchronous mode is disabled, and switching operation by the internal clock becomes active (Non-Synchronous mode). The spread spectrum function is disabled during synchronous mode.

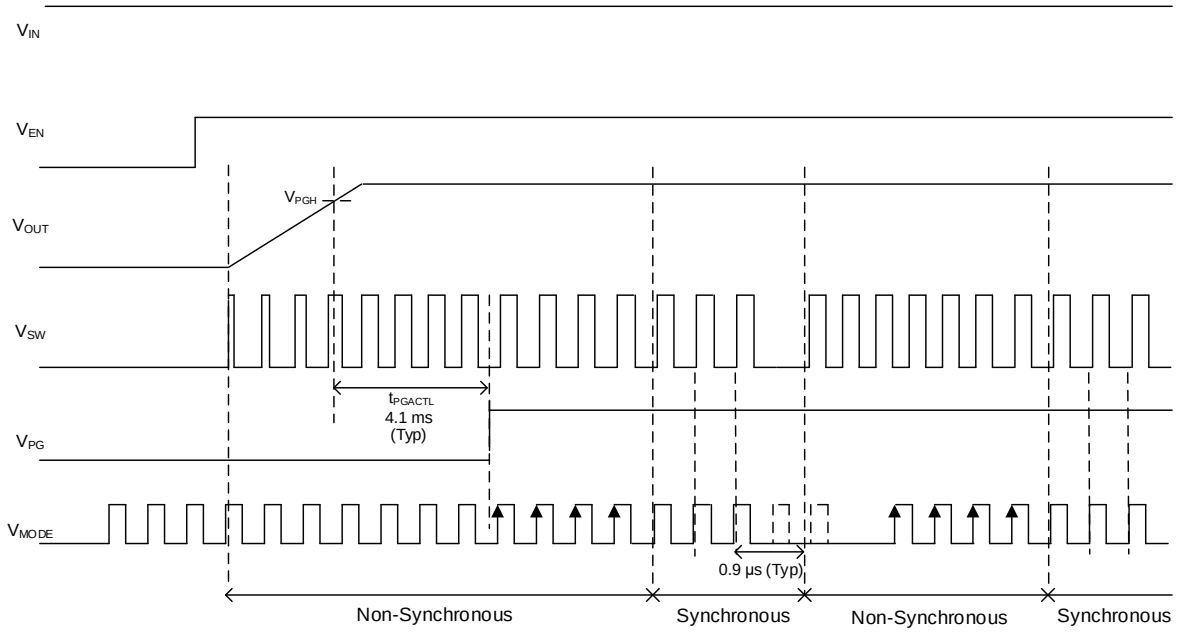


Figure 29. External Synchronization Function (FREQ_SEL = L)

Function Explanation - continued

6. Frequency Division Function

This device drives the High Side FET with a bootstrap and requires the ON time of the Low Side FET to charge the BST pin. Therefore, the minimum OFF time of the SW pin is specified, and the output voltage is limited by the minimum OFF time under the condition in which the voltage between input and output are close. To prevent this situation, OFF pulses are skipped when the voltage between input and output are small to keep the High Side FET turned on and increase the ON duty of the SW pin. The OFF pulse skip is done for 15 consecutive switching cycles in maximum when the FREQ_SEL pin is Low(The switching frequency becomes a one sixteenth of nominal frequency). The OFF pulse skip is done for 3 consecutive switching cycles in maximum when the FREQ_SEL pin is High. In this case, the output voltage can be calculated with the following equation. When performing external synchronization during the operation of the frequency division function, there is a possibility that the output ripple may increase depending on the frequency setting. It is recommended to either adjust the frequency closer to the typical setting or disable the external synchronization function.

$$V_{OUT} = MaxDuty \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT}$$
$$= \left(1 - t_{OFFMIN} \times \frac{f_{SW}}{16}\right) \times (V_{IN} - R_{ONH} \times I_{OUT}) - R_{DC} \times I_{OUT} \text{ [V]}$$

Where:

$MaxDuty$	is the SW pin Maximum ON Duty Cycle [%]
V_{IN}	is the Input Voltage [V]
R_{ONH}	is the High Side FET ON Resistance [Ω]
I_{OUT}	is the Output Current [A]
R_{DC}	is the DCR of Inductor [Ω]
t_{OFFMIN}	is the SW pin Minimum OFF Time [s]
f_{SW}	is the Switching Frequency [Hz]

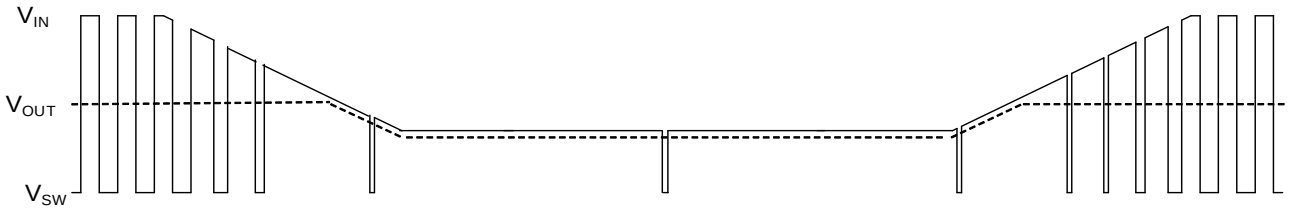


Figure 30. Frequency Division Function

Function Explanation - continued

7. Spread Spectrum Function
   The switching frequency is varied with triangular wave of Δf_{SSCG} (+8.5 %, Typ) amplitude bottomed on typical frequency f_{SWL} (2.0 MHz, Typ). The period of the triangular wave is t_{SSCG_CYCLEL} (512 µs, Typ) when the FREQ_SEL pin is Low, and t_{SSCG_CYCLEH} (640 µs, Typ) when the FREQ_SEL pin is High. However, this function is masked when the PG output is low.

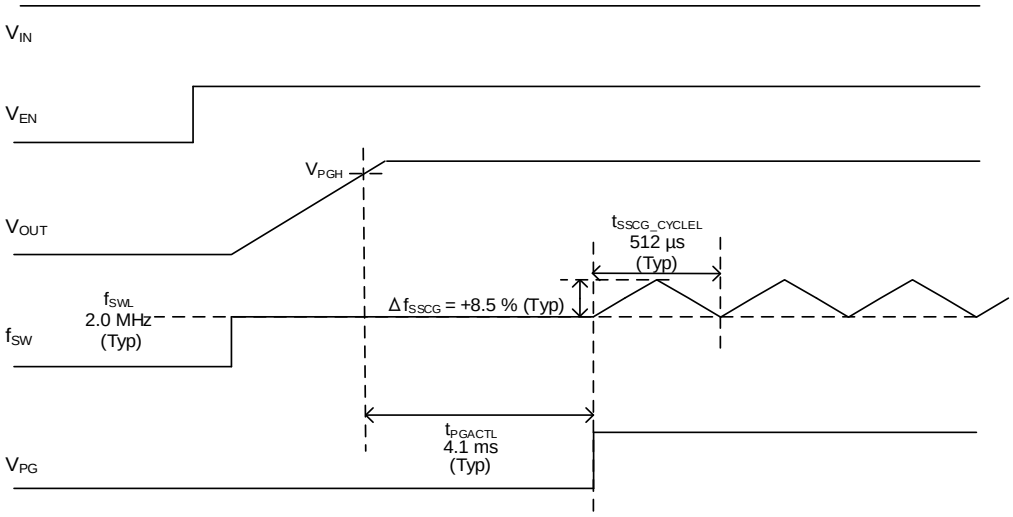


Figure 31. Spread Spectrum Function (FREQ_SEL = L)

Protect Function

1. Over Current Protection (OCP)
   The Over Current Protection (OCP) monitors the average inductor current. The OCP detection level is I_{OCP} (2.8 A, Typ). When the average inductor current exceeds to its setting value, the duty cycle of the switching is limited and the output voltage decreases. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should never be used in applications where the protection circuit operates continuously (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

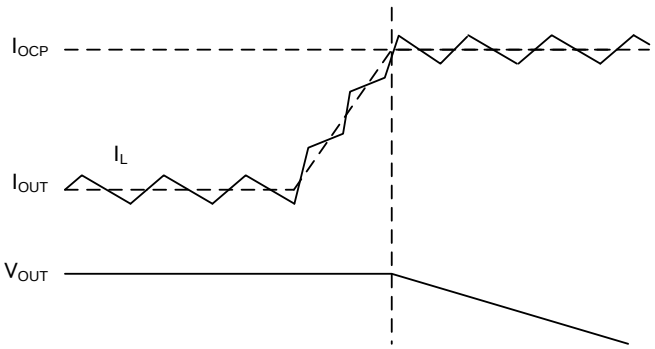


Figure 32. Over Current Protection

2. Short Circuit Protection (SCP)
   The Short Circuit Protection (SCP) block compares the FB pin voltage with the internal reference voltage VREF. When the FREQ_SEL pin is Low, if the FB pin voltage has decreased to V_{SCPL} (0.64 V, Typ) or less and remained there for 1.0 ms (Typ), SCP stops the operation for 32 ms (Typ) and subsequently initiates a restart. If the FB pin voltage decreases to V_{SCPL} (0.64 V, Typ) or less and increases to V_{SCPH} (0.72 V, Typ) or more within 1.0 ms afterwards, SCP protection is released and output voltage recovers to normal operation.
   The SCP function is deactivated during 8.2 ms (Typ) from V_{OUT} starting up. In addition, when VIN decreases and V_{OUT} also decreases, the SCP function is deactivated not to detect short circuit protection. In this case, the Light Load Mode Control is disabled. The SCP function is likewise deactivated when VIN voltage is lower than V_{SCP_DACTL} (164 %, Typ) of the VOUT_SNS pin voltage, and then is activated after 8.2 ms (Typ) from VIN voltage exceeds V_{SCP_DACTH} (167 %, Typ) of the VOUT_SNS pin voltage. Therefore, in the case of short circuit from VIN close to V_{OUT} condition, SCP stops the switching operation after 9.2 ms (Typ) from short circuit. However, the device should never be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).
   When the FREQ_SEL pin is High, SCP function detection time is 1.2 ms (Typ), SCP function stop time is 41 ms (Typ), SCP function mask time is 10.2 ms (Typ).

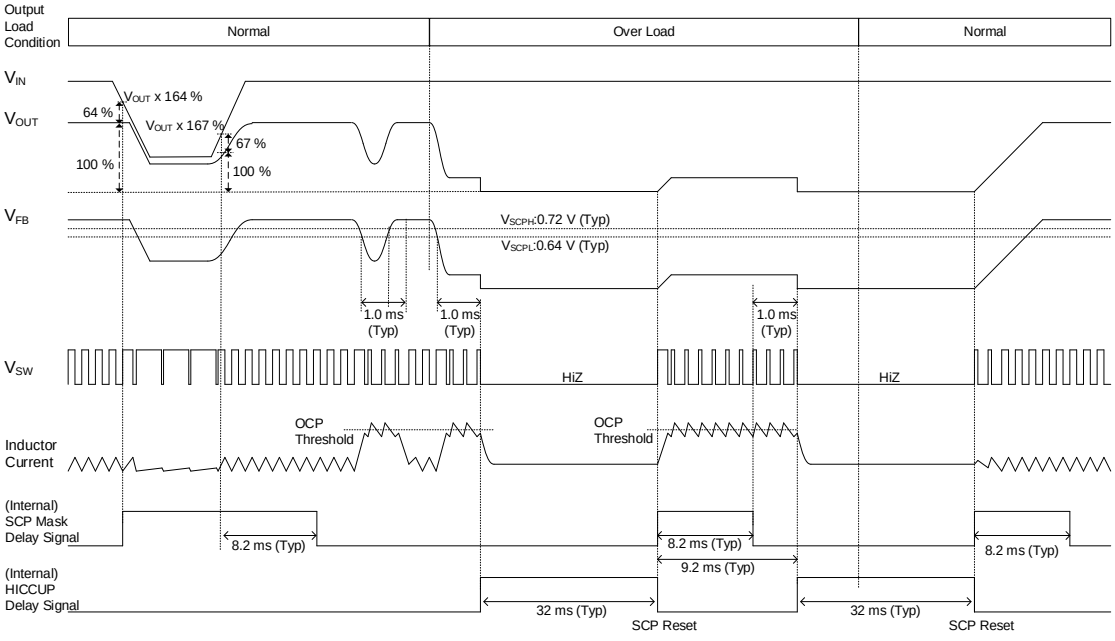


Figure 33. Short Circuit Protection (SCP) Timing Chart (FREQ_SEL = L)

Protect Function - continued

3. Power On Reset (POR)/Under Voltage Lockout Protection (UVLO)
The UVLO and POR are integrated to prevent the malfunction when the power supply voltage is decreased. The POR monitors the VIN pin voltage. UVLO monitors the VREG pin voltage.
In the sequence of VIN rising, the VREG pin voltage also rises up to 3.3 V (Typ) following VIN voltage. First, UVLO is released when VREG voltage increase above V_{UVLO_R} (2.42 V, Typ). Next, POR is released when VIN voltage increase above V_{POR_R} (3.35 V, Typ). When both POR and UVLO are released, the IC starts up with soft start.
In the sequence of VIN falling, VREG voltage also falls. When VIN voltage decrease below V_{POR_F} (2.85 V, Typ) POR is detected and switching is stopped. VREG voltage decreases below V_{UVLO_F} (2.35 V, Typ), UVLO is detected and puts the IC goes into standby state.

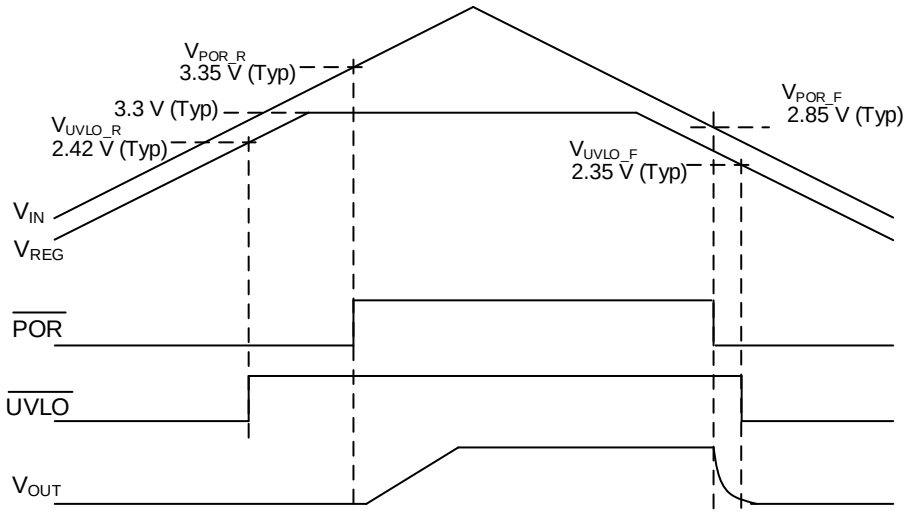


Figure 34. POR/UVLO Timing Chart

4. Thermal Shut Down (TSD)
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. If junction temperature (Tj) exceeds TSD detection temperature (175 °C, Typ), the POWER MOSFETs are turned off. When the Tj falls below the TSD temperature (165 °C, Typ), the IC restarts up with soft start. Where the input voltage required for the restart is the same as that for the initial startup (Input voltage 3.5 V or more). Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

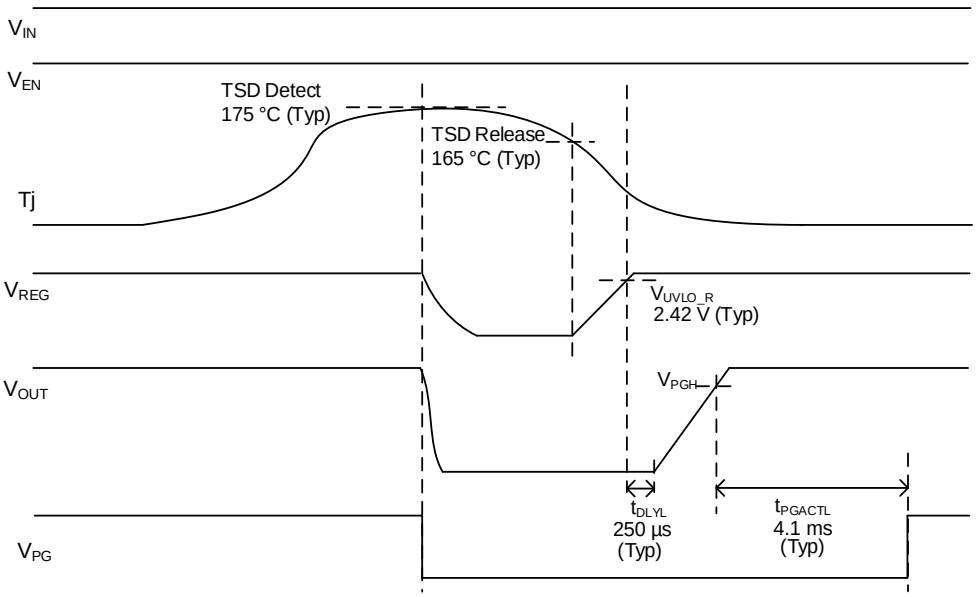


Figure 35. TSD Timing Chart (FREQ_SEL = L)

Protect Function - continued

5. Over Voltage Protection (OVP)
This IC has Over Voltage Protection (OVP) monitoring FB to prevent the increase of output voltage in case of external injected current to V_{OUT}. When the FB pin voltage exceeds V_{OVPH} (0.860 V, Typ), the switching regulator sinks current from V_{OUT} by changing state to PWM. The sink current during OVP is restricted to I_{NCP} (2.5 A, Typ). In addition, the PG pin is pulled down to GND during OVP detection. To prevent the malfunction by noise, the internal delay is implemented after OVP detection. The delay time is $t_{PGFILTL}$ (144 µs, Typ) when the FREQ_SEL pin is Low, and $t_{PGFILTH}$ (180 µs, Typ) when the FREQ_SEL pin is High. When the FB pin voltage falls below V_{OVPL} (0.840 V, Typ), OVP function is released. When the FREQ_SEL pin is Low, the PG pin is kept low and PWM switching is also kept during t_{PGACTL} (4.1 ms, Typ) after OVP function is released. When the FREQ_SEL pin is High, the PG pin is kept low and PWM switching is also kept during t_{PGACTH} (5.1 ms, Typ).

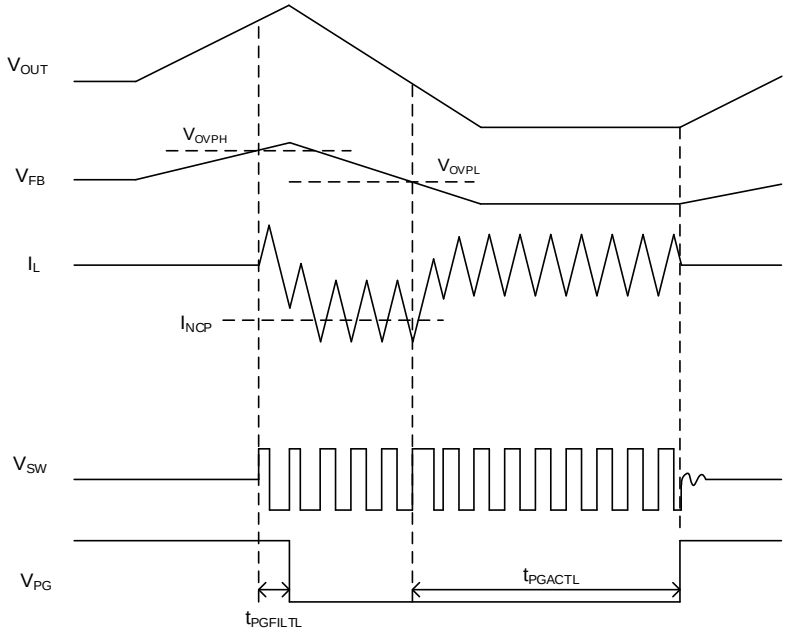


Figure 36. FB OVP Timing Chart (FREQ_SEL = L)

If V_{OUT} is shorted to the Battery Line as following figure, the DC/DC converter sinks current from V_{OUT} to the Low Side FET. If a Reverse Polarity Protection Diode is on the Battery Line, the VIN voltage results in being boosted up and might exceed the absolute maximum ratings.

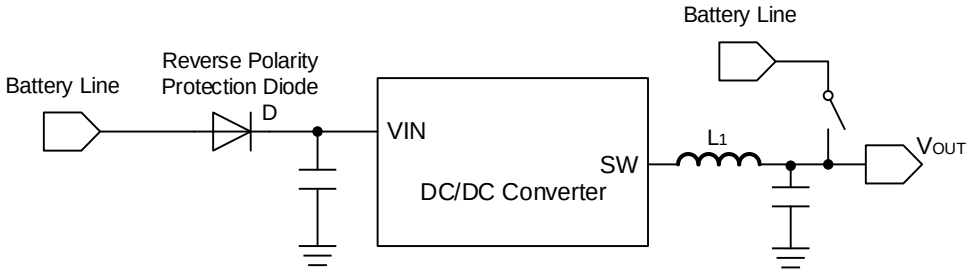


Figure 37. V_{OUT} shorted to Battery Line

Selection of Components Externally Connected

Contact us if not use the recommended constant in the application circuit.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Sample Specification

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	3.0 V to 36 V
Output Voltage	V_{OUT}	5.0 V
Output Ripple Voltage	ΔV_{P-P}	20 mV_{p-p}
Output Current	I_{OUT}	Max 2.0 A
Switching Frequency	f_{SW}	2.0 MHz
Operating Temperature Range	Ta	-40 °C to +125 °C

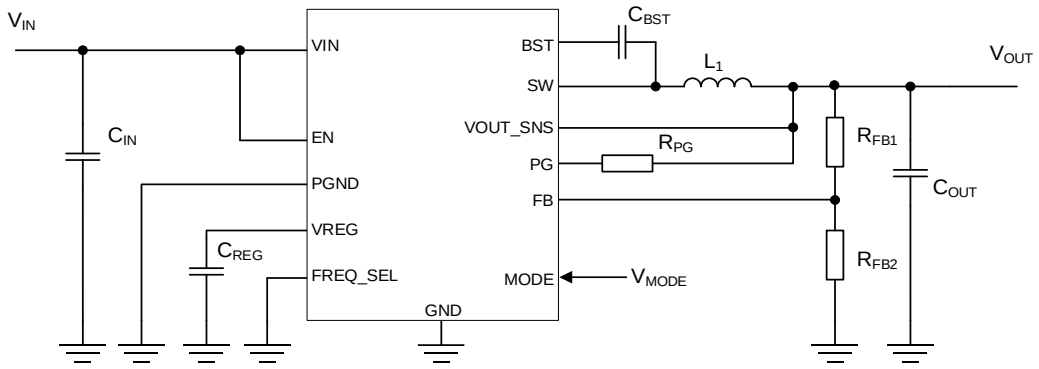


Figure 38. Application Sample Circuit

Selection of Components Externally Connected - continued

1. Selection of the Inductor L_1 value
The inductor in the switching regulator supplies a continuous current to the load and functions as a filter to smooth the output voltage. In current mode control, the sub-harmonic oscillation may happen. The slope compensation is integrated into the IC to prevent the sub-harmonic oscillation. The sub-harmonic oscillation depends on the rate of increase of output switch current. If the inductor value is too small, the sub-harmonic oscillation may happen because the inductor ripple current ΔI_L is increased. If the inductor value is too large, the feedback loop may not achieve stability because the inductor ripple current ΔI_L is decreased.

Table 2. Recommended inductor value

Output Voltage	Switching Frequency	Inductor Value
5 V	400 kHz	10 µH
	2 MHz	3.3 µH
3.3 V	400 kHz	10 µH
	2 MHz	3.3 µH

The peak to peak inductor current is shown by the following equation:

$$\Delta I_L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times f_{SW}\times L} \text{ [A]}$$

Where:
V_{IN} is the input voltage [V]
V_{OUT} is the output voltage [V]
f_{SW} is the switching frequency [Hz]
L is the inductor value [H]

$\Delta V_{P\text{-}P}$ (Output peak-to-peak ripple voltage) is shown in the following equation.

$$\Delta V_{P-P} = \Delta I_L \times ESR + \frac{\Delta I_L}{8\times C_{OUT}\times f_{SW}} \text{ [V]} \quad \text{(a)}$$

Where:
ESR is the equivalent series resistance of the output capacitor [Ω]
C_{OUT} is the output capacitance [F]
f_{SW} is the switching frequency [Hz]

The shielded type (closed magnetic circuit type) is the recommended type of inductor to be used. It is important not to magnetic saturate the core in any situation, so please make sure that the definition of rated current is different according to the manufactures. Please check the rated current at maximum ambient temperature of application to inductor manufacturer.

Selection of Components Externally Connected - continued

2. Selection of Output Capacitor C_{OUT}

The output capacitor is selected based on the ESR that is required from the previous page equation (a). ΔV_{P-P} can be reduced by using a capacitor with a small ESR.

The ceramic capacitor is the best option that meets this requirement. It is because not only it has a small ESR but the ceramic capacitor also contributes to the size reduction of the application circuit. Please confirm the frequency characteristics of ESR from the datasheet of the capacitor manufacturer, and consider a low ESR value for the switching frequency being used. It is necessary to consider that the capacitance of the ceramic capacitor changes obviously according to DC biasing characteristic. For the voltage rating of the ceramic capacitor, twice or more the maximum output voltage is usually required. By selecting a high voltage rating, it is possible to reduce the influence of DC bias characteristics. Moreover, in order to maintain good temperature characteristics, the one with the characteristics of X7R or better is recommended. Because the voltage rating of a large ceramic capacitor is low, the selection becomes difficult for an application with high output voltage. In that case, please connect multiple ceramic capacitors.

These capacitors are rated in ripple current. The RMS values of the ripple current that can be obtained in the following equation and must not exceed the ripple current rating.

$$I_{COUT(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \text{ [A]}$$

Where:

$I_{COUT(RMS)}$ is the value of the ripple electric current [A]

Next, the output ceramic capacitor C_{OUT} is recommended to the following.

Table 3. Output Ceramic Capacitor Recommended Capacitance Value

Switching Frequency	1 V ≤ V_{OUT} < 3.3 V	3.3 V ≤ V_{OUT} < 5 V	V_{OUT} ≥ 5.0 V
400 kHz	$C_{OUT} \geq \frac{400}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{217.8}{V_{OUT}}$ [µF]	$C_{OUT} \geq 44$ [µF]
2 MHz	$C_{OUT} \geq \frac{88}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{72.6}{V_{OUT}}$ [µF]	$C_{OUT} \geq 22$ [µF]

When selecting the capacitor ensure that the capacitance of the following equation is maintained at the characteristics of DC Bias, AC Voltage, temperature, and tolerance.

Table 4. Output ceramic capacitor minimum capacitance value

Switching Frequency	1 V ≤ V_{OUT} < 3.3 V	3.3 V ≤ V_{OUT} < 5 V	V_{OUT} ≥ 5.0 V
400 kHz	$C_{OUT} \geq \frac{255}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{138.6}{V_{OUT}}$ [µF]	$C_{OUT} \geq 28$ [µF]
2 MHz	$C_{OUT} \geq \frac{56}{V_{OUT}}$ [µF]	$C_{OUT} \geq \frac{46.2}{V_{OUT}}$ [µF]	$C_{OUT} \geq 14$ [µF]

If the capacitance falls below this value, the oscillation may happen. When using the electrolytic capacitor and the conductive polymer hybrid aluminum electrolytic capacitor, please place it in addition to the ceramic capacitors with the capacity described above. Actually, the changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and layout of the PCB. Please confirm stability and responsiveness in actual application. And please place PCB patterns that allows C_{OUT} adjustment from the initial design in case of insufficient stability and responsiveness.

In addition, for the total value of capacitance in the output line $C_{OUT(Max)}$, please choose a capacitance value less than the value obtained by the following equation:

$$C_{OUT(Max)} < \frac{t_{SS(Min)} \times 1.25 \times (I_{OCP(Min)} - I_{OUT\_START(Max)})}{V_{OUT}} \text{ [F]}$$

Where:

$I_{OCP(Min)}$ is the OCP operation current (Min) [A]

$t_{SS(Min)}$ is the Soft Start Time (Min) [s]

$I_{OUT\_START(Max)}$ is the maximum load current during startup [A]

V_{OUT} is the output voltage [V]

2. Selection of Output Capacitor C_{OUT} - continued
If the limits from the above-mentioned are exceeded, startup failure may happen. If the capacitance value is extremely large, over-current protection may be activated by the inrush current at startup preventing the output to turn on. Please confirm this on the actual application.
Also, in case of large changing input voltage and load current, select the capacitance by verifying that the actual application setup meets the required specification.

3. Selection of Input Capacitor C_{IN}, C_{BLK}
For input capacitors, there are two variation types of capacitor: decoupling capacitors C_{IN} and bulk capacitors C_{BLK}. Ceramic capacitors with total values 2.4 µF or more are necessary for the decoupling capacitors C_{IN} for ripple noise reduction. If a low ESR electrolytic capacitor with large capacitance is connected parallel to the decoupling capacitors as a bulk capacitor, ceramic capacitors with 0.5 µF or more are necessary for the decoupling capacitors. (However, to reduce EMI noise level, 2.4 µF or more are recommended for ceramic capacitors.) These capacitor values including device variation, temperature characteristics, DC bias characteristics, and aging change must be larger than minimum value. It is effective for switching noise reduction to place one of ceramic capacitor close to the PVIN and the VIN pins. The voltage rating of the capacitors is recommended to be 1.2 times or more the maximum input voltage, more than twice the normal input voltage. Also, the IC might not operate properly when the PCB layout or the position of the capacitor is not good. Please check “PCB Layout Design” on page 48.

The bulk capacitor is optional. The bulk capacitor prevents the decrease in the line voltage and serves as a backup power supply to keep the input voltage constant. A low ESR electrolytic capacitor with large capacitance is suitable for the bulk capacitor. It is necessary to select the best capacitance value for each of application. In that case, please take note not to exceed the rated ripple current of the capacitor.

The RMS value of the input ripple current $I_{CIN(RMS)}$ is obtained in the following equation:

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left\{ {I_{OUT(Max)}}^2 \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + \frac{1}{12} \times {\Delta I_L}^2 \right\}} \text{ [A]}$$

Where:

$I_{OUT(Max)}$	is the Output Current (Max) [A]
V_{IN}	is the input voltage [V]
V_{OUT}	is the output voltage [V]
ΔI_L	is the peak to peak inductor current [A]

In addition, in automotive and other applications requiring high reliability, it is recommended to connect the capacitors in parallel to accommodate multiple electrolytic capacitors and minimize the chances of drying up. For ceramic capacitors, it is recommended to make two series + two parallel structures to decrease the risk of capacitor destruction due to short circuit conditions.

When the impedance on the input side is high for some reason (because the wiring from the power supply to the VIN pin is long, etc.), then high capacitance is required. In actual conditions, it is necessary to verify that there are no problems like IC is turned off, or the output overshoots due to the change in V_{IN} at transient response.

4. Selection of the Bootstrap Capacitor
For Bootstrap capacitor C_{BST}, please connect a 0.1 µF (Typ) ceramic capacitor as close as possible between the BST pin and the SW pin.

5. Selection of the VREG Capacitor.
For VREG capacitor C_{REG}, please connect a 1.0 µF (Typ) ceramic capacitor between the VREG pin and GND.

Selection of Components Externally Connected - continued

6. Selection of Output Voltage Setting Resistor R_{FB1}, R_{FB2}

The output voltage is set with output voltage setting resistors R_{FB1} and R_{FB2}. The reference voltage of GmAmp1 is set to 0.80 V and the IC operates to regulate the FB pin voltage to 0.80 V. The output voltage is defined by the formula (1). R_{FB1} and R_{FB2} should be adjusted to set the required output voltage. If R_{FB1} and R_{FB2} are large, the current flowing through on these resistors is small and the circuit current at no load can be reduced. However, the phase shift is likely to happen because of the parasitic capacitance of IC and PCB on the FB pin. Therefore, the combined resistance R_{FB1}//R_{FB2} should be set to 200 kΩ or less.

$$V_{OUT} = \frac{R_{FB1}+R_{FB2}}{R_{FB2}} \times 0.80 \text{ [V]} \qquad (1)$$

$$C_{FB1} \leq \frac{5576}{R_{FB1}} \text{[pF]} \qquad (2)$$

Where:

R_{FB1} is the output voltage setting resistors [kΩ]

R_{FB2} is the output voltage setting resistors [kΩ]

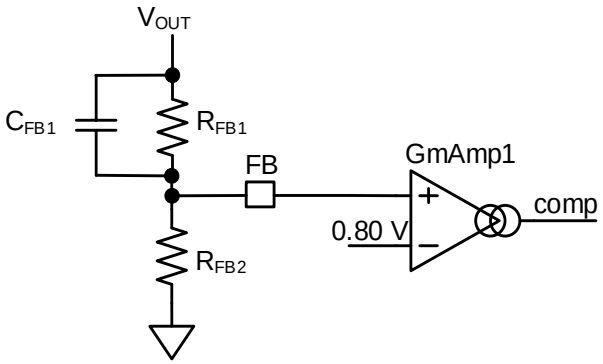


Figure 39. Output Voltage setting Resistor

The changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used. Please ensure a phase margin of 35° or more and a gain margin of 5 dB or more in actual application. If it cannot ensure, C_{FB1} should be chosen to satisfy formula (2) as a guide.

the voltage between input and output increases and the ON time of the SW decreases to under t_{ONMIN}, the switching frequency is decreased. To ensure stable switching frequency, the output voltage must satisfy the following equation. If this equation is not satisfied, the SW pulse is skipped. In this case, the switching frequency decreases and the output voltage ripple increases.

$$V_{OUT} \geq V_{IN(Max)} \times f_{SW(Max)} \times t_{ONMIN(Max)} \text{ [V]}$$

Where:

$V_{IN(Max)}$ is the Input Voltage (Max) [V]

$f_{SW(Max)}$ is the Switching Frequency (Max) [Hz]

$t_{ONMIN(Max)}$ is the SW Minimum ON time (Max) [s]

If the voltage between input and output decreases, the ON time of the SW increases by skipping the off time and the switching frequency is decreased. To keep switching frequency stably, the following equation must be satisfied.

$$V_{OUT} \leq V_{IN(Min)} \times (1 - f_{SW(Max)} \times t_{OFFMIN(Max)}) \text{ [V]}$$

Where:

$V_{IN(Max)}$ is the Input Voltage (Max) [V]

$f_{SW(Max)}$ is the Switching Frequency (Max) [Hz]

$t_{OFFMIN(Max)}$ is the SW Minimum OFF Time (Max) [s]

Application Examples 1

Table 5. Specification Example 1

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	5.0 V
Switching Frequency	f_{SW}	2 MHz
Output Current	I_{OUT}	Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

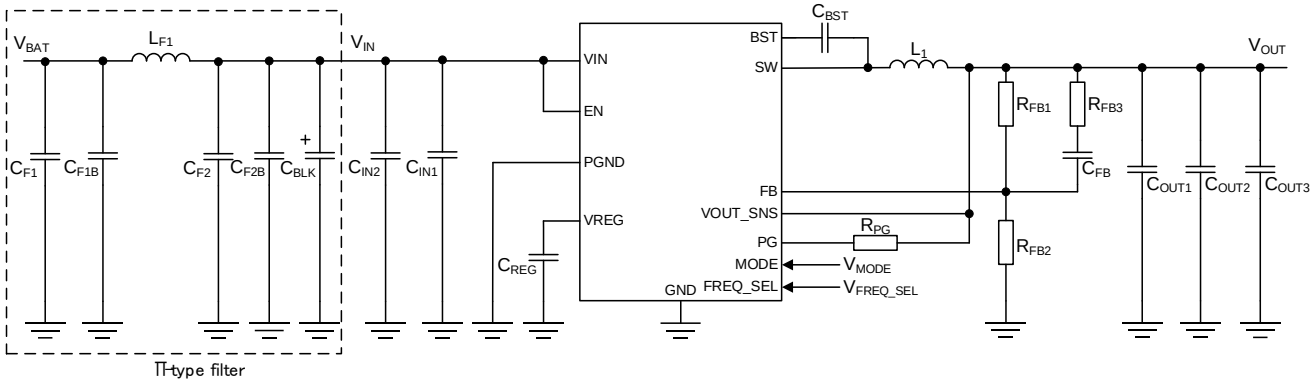


Figure 40. Reference Circuit

Table 6. Application Example 1 Parts List

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
C_{F1B}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{F2B}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic Capacitor	NICHICON
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{PG}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip Resistor	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	-	-	-	-	-
C_{OUT3}	-	-	-	-	-
C_{FB}	1005	22 pF, C0G, 50 V	GCM1555C1H220J	Ceramic	MURATA
R_{FB1}	1005	68 kΩ, 1 %, 1/16 W	MCR01MZPF6802	Chip Resistor	ROHM
R_{FB2}	1005	13 kΩ, 1 %, 1/16 W	MCR01MZPF1302	Chip Resistor	ROHM
R_{FB3}	1005	1 kΩ, 1 %, 1/16 W	MCR01MZPF1001	Chip Resistor	ROHM

Application Examples 1 - continued
(Ta = 25 °C)

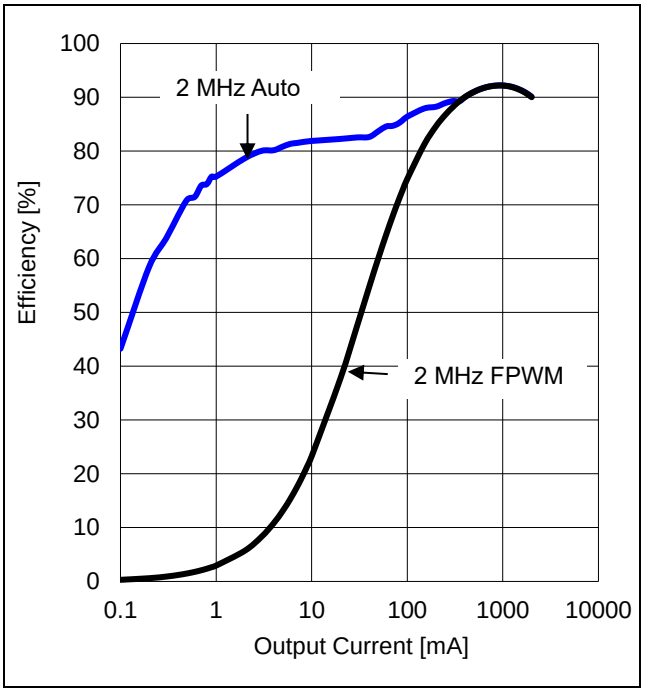


Figure 41. Efficiency vs Output Current
(V_{IN} = 12 V)

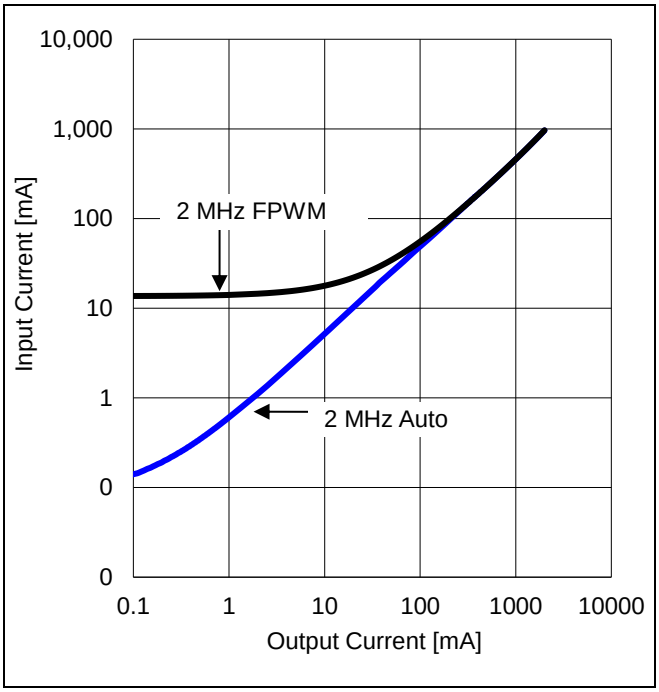


Figure 42. Input Current vs Output Current
(V_{IN} = 12 V)

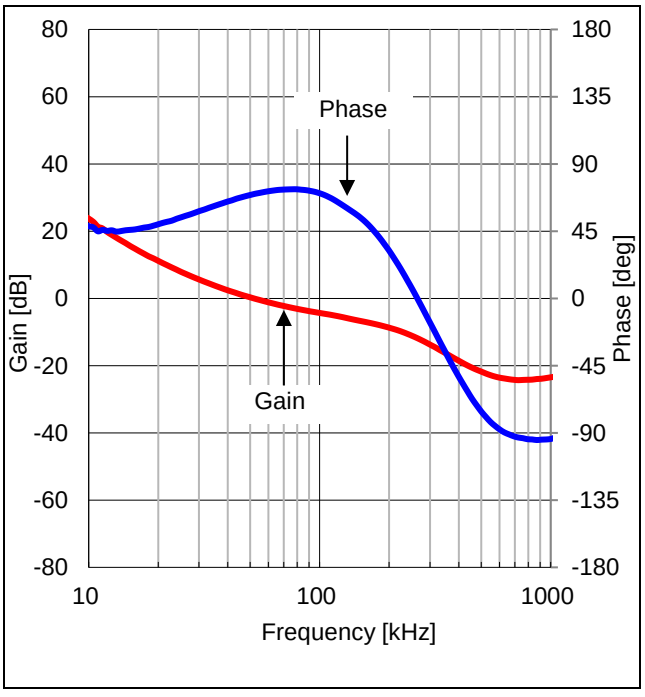


Figure 43. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

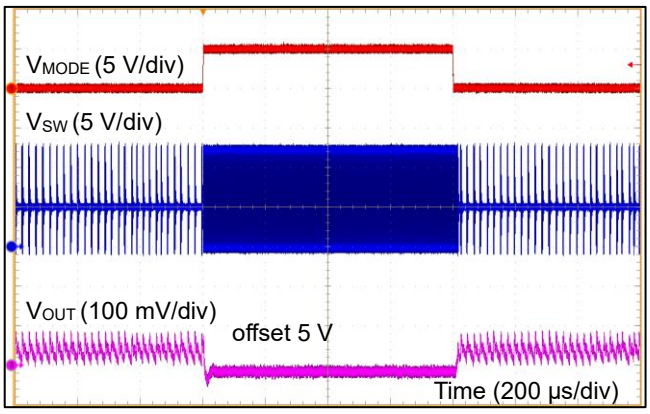


Figure 44. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 1 - continued
(Ta = 25 °C)

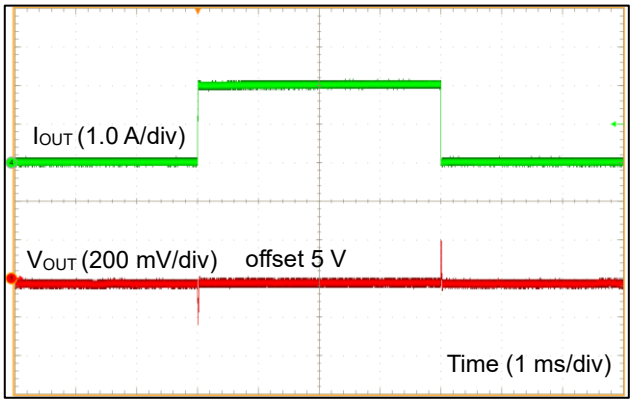


Figure 45. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

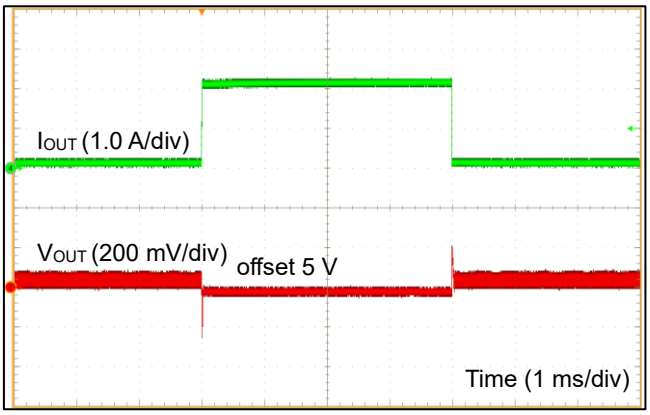


Figure 46. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0.1 A to 2 A)

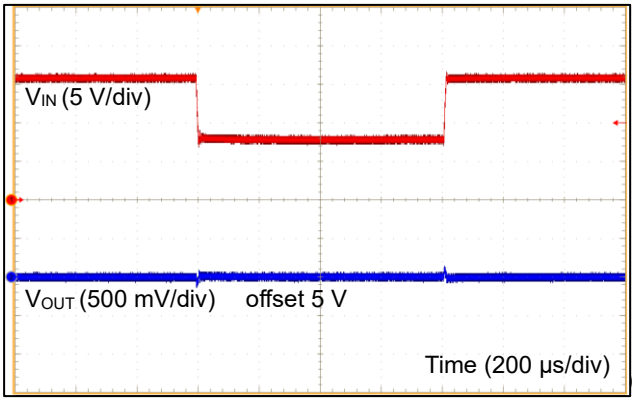


Figure 47. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

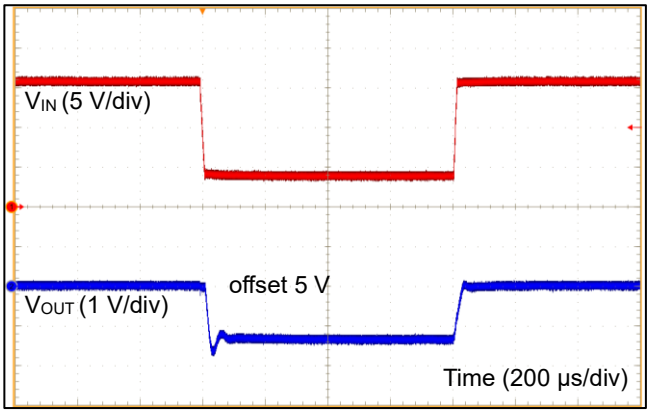


Figure 48. Line Response 2
(V_{IN} = 16 V to 4 V, I_{OUT} = 2 A)

Application Examples 1 - continued
(Ta = 25 °C)

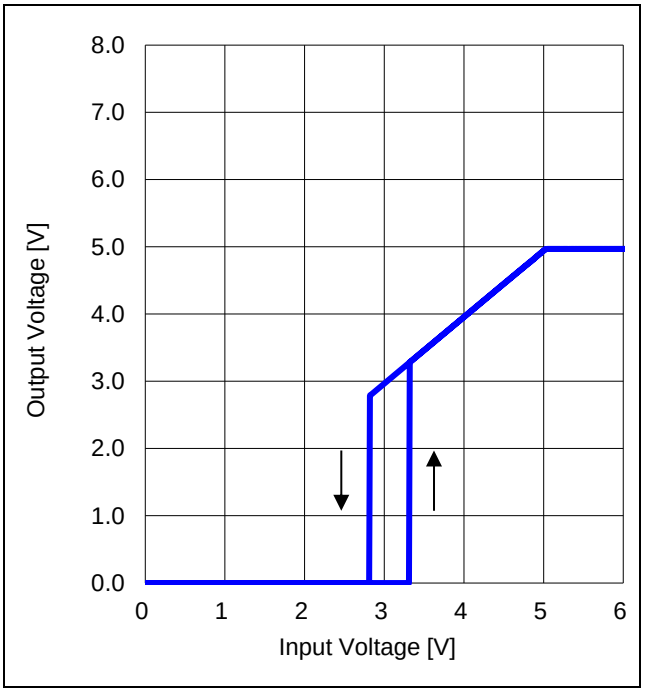


Figure 49. Output Voltage vs Input Voltage 1
(R_{LOAD} = 250 Ω)

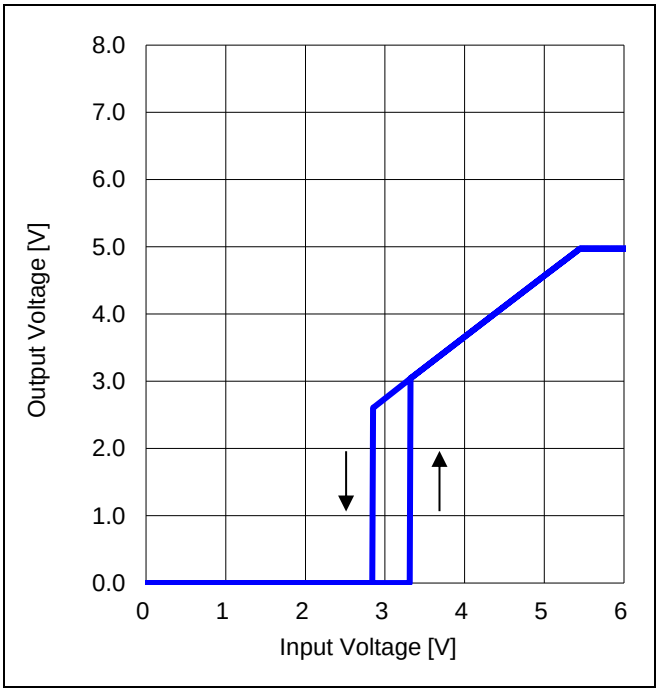


Figure 50. Output Voltage vs Input Voltage 2
(R_{LOAD} = 2.5 Ω)

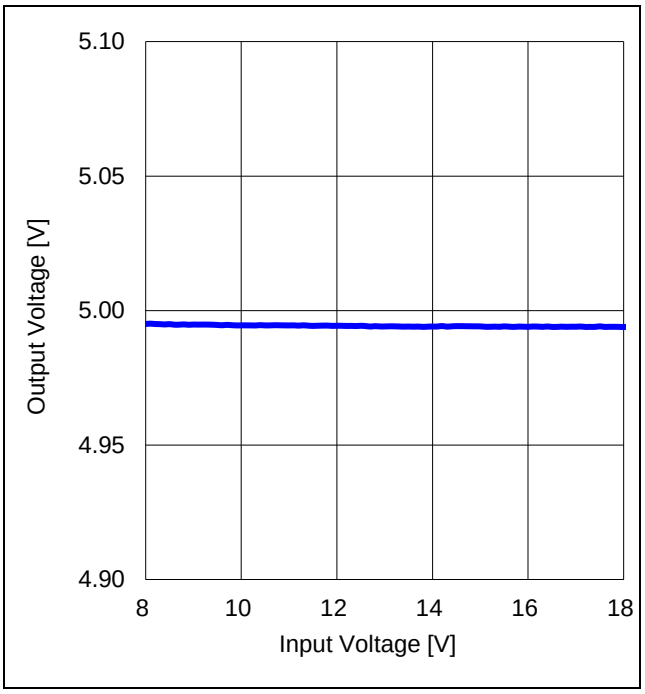


Figure 51. Line Regulation
(I_{OUT} = 2 A)

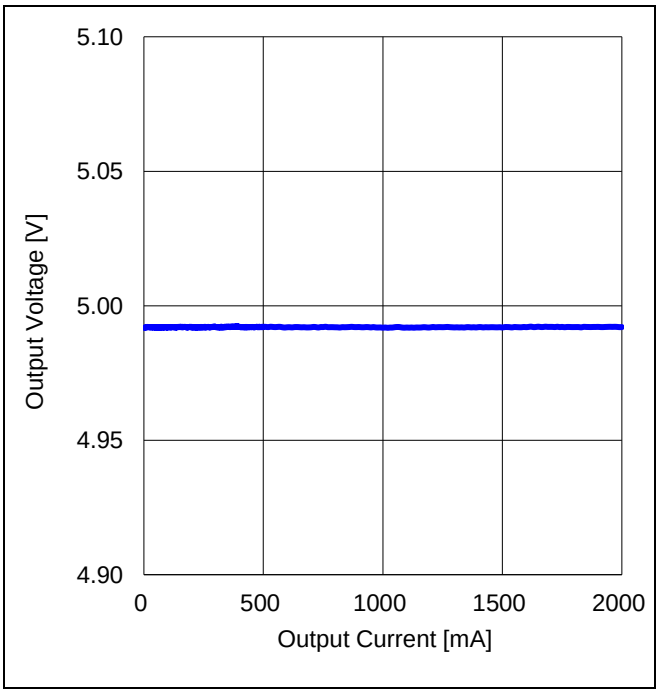


Figure 52. Load Regulation
(V_{IN} = 12 V, V_{MODE} = 5 V)

Application Examples 1 - continued
(Ta = 25 °C)

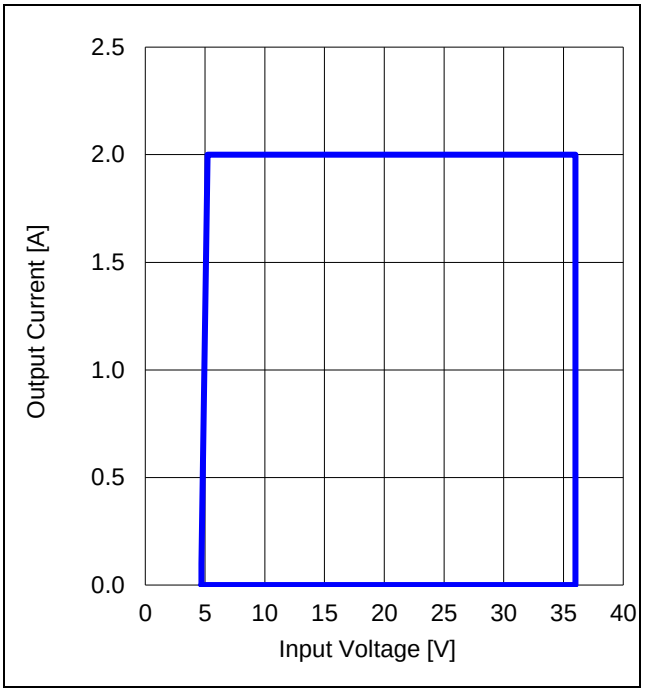


Figure 53. Output Current vs Input Voltage(Note 1)
Operating Range: Tj < 150 °C

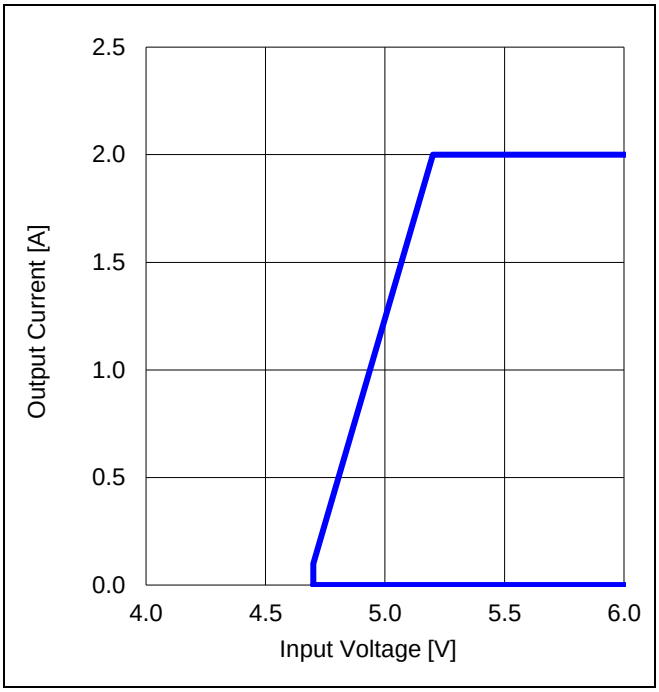


Figure 54. Output Current vs Input Voltage(Note 1)
Operating Range: Tj < 150 °C

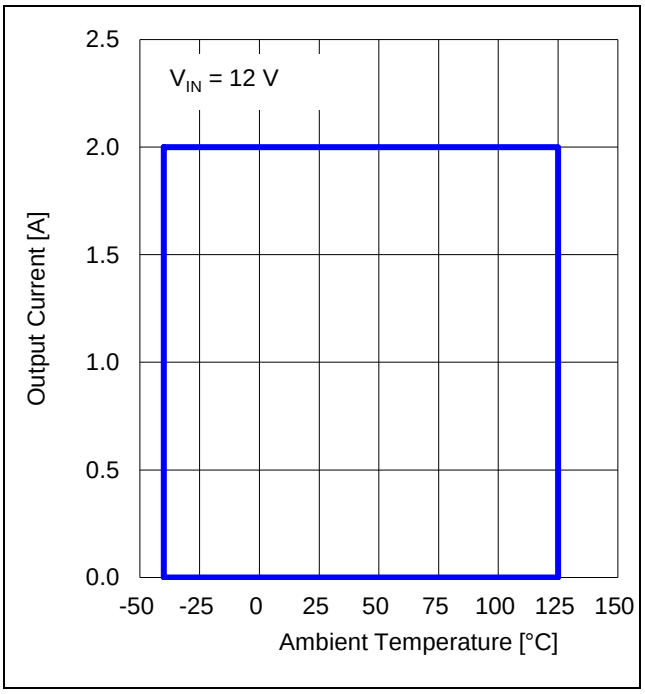


Figure 55. Output Current vs Ambient Temperature(Note 1)
Operating Range: Tj < 150 °C

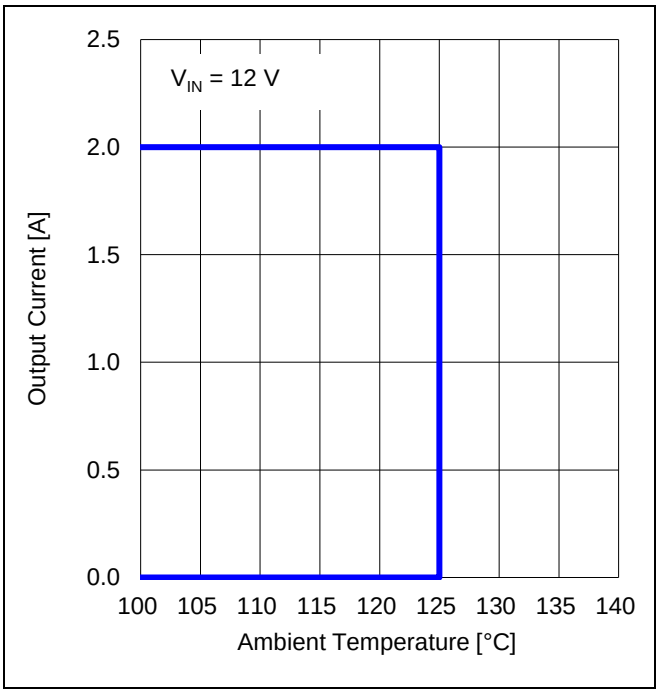


Figure 56. Output Current vs Ambient Temperature(Note 1)
Operating Range: Tj < 150 °C

(Note 1) Measured on FR-4 board 100 mm x 75 mm, Copper Thickness: Top and Bottom 70 µm, 2 Internal Layers 35 µm.

Application Examples 2

Table 7. Specification Example 2

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	3.3 V
Switching Frequency	f_{SW}	2 MHz
Output Current	I_{OUT}	Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

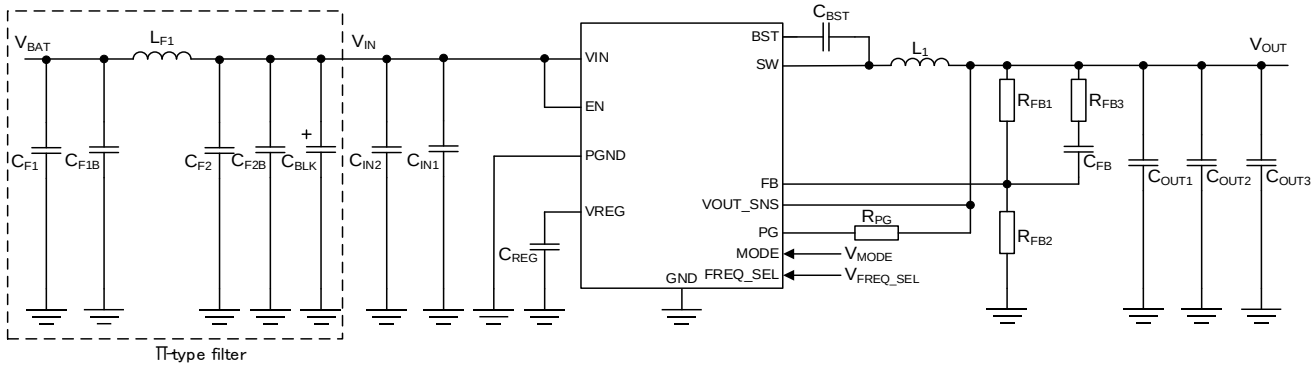


Figure 57. Reference Circuit

Table 8. Application Example 2 Parts List

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
C_{F1B}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{F2B}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic Capacitor	NICHICON
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{PG}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip Resistor	ROHM
L_1	W6.0 x H4.5 x L6.3 mm^3	3.3 µH	CLF6045NIT-3R3N-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	-	-	-	-	-
C_{OUT3}	-	-	-	-	-
C_{FB}	1005	22 pF, C0G, 50 V	GCM1555C1H220J	Ceramic	MURATA
R_{FB1}	1005	75 kΩ, 1 %, 1/16 W	MCR01MZPF7502	Chip Resistor	ROHM
R_{FB2}	1005	24 kΩ, 1 %, 1/16 W	MCR01MZPF2402	Chip Resistor	ROHM
R_{FB3}	1005	1 kΩ, 1 %, 1/16 W	MCR01MZPF1001	Chip Resistor	ROHM

Application Examples 2 - continued
(Ta = 25 °C)

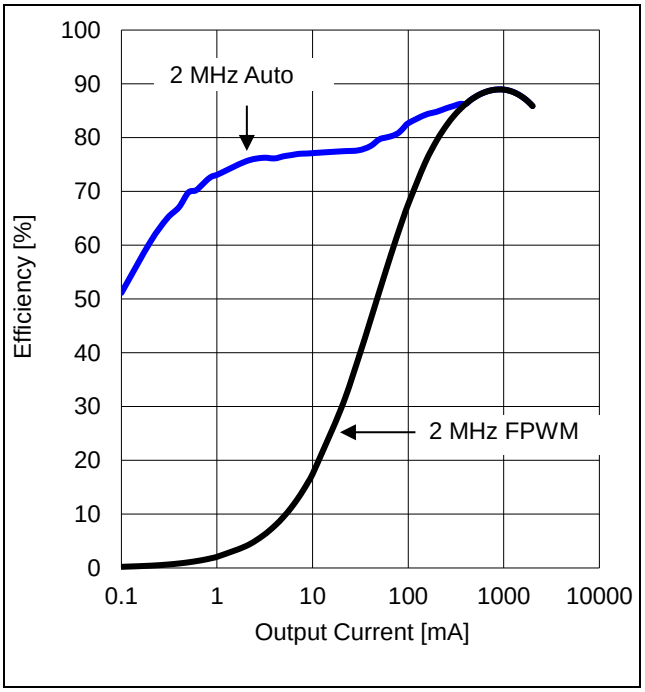


Figure 58. Efficiency vs Output Current
(V_{IN} = 12 V)

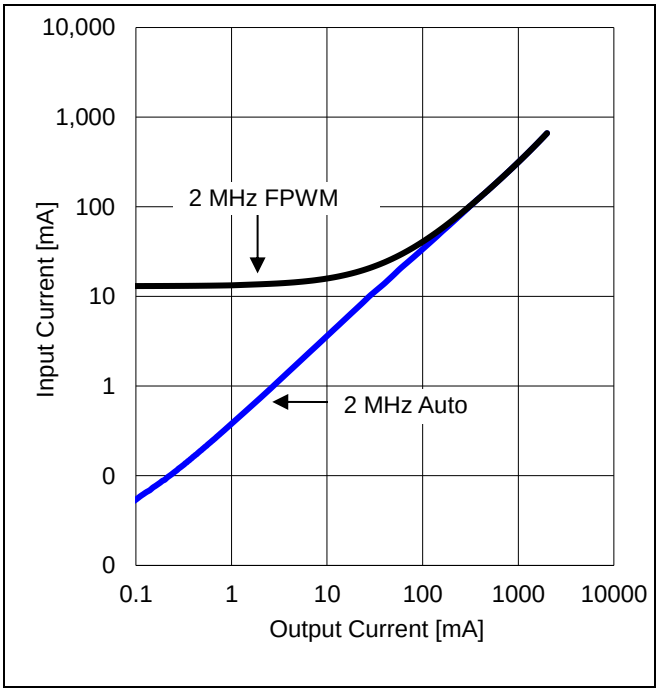


Figure 59. Input Current vs Output Current
(V_{IN} = 12 V)

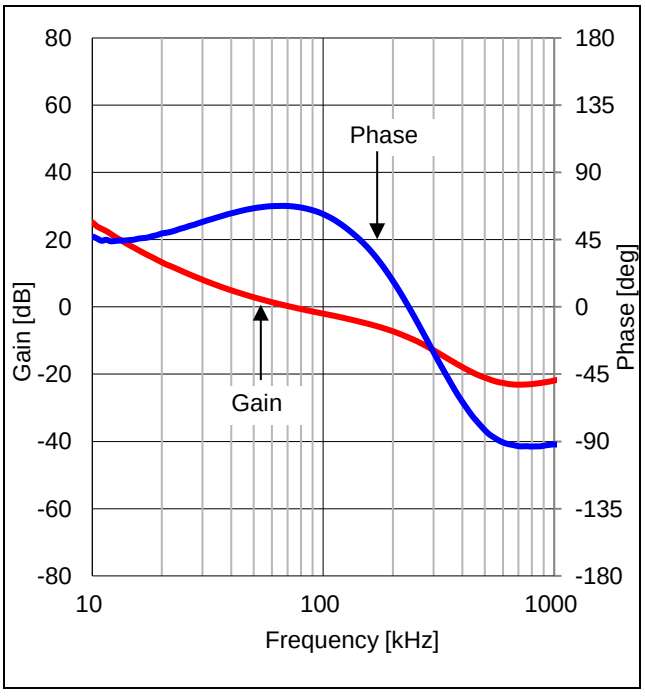


Figure 60. Frequency Characteristics
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

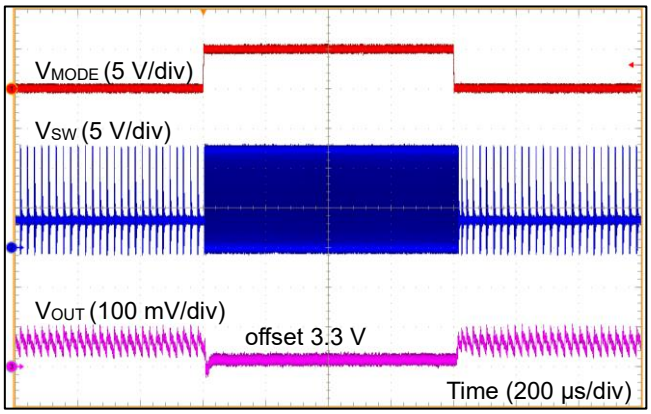


Figure 61. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 2 - continued
(Ta = 25 °C)

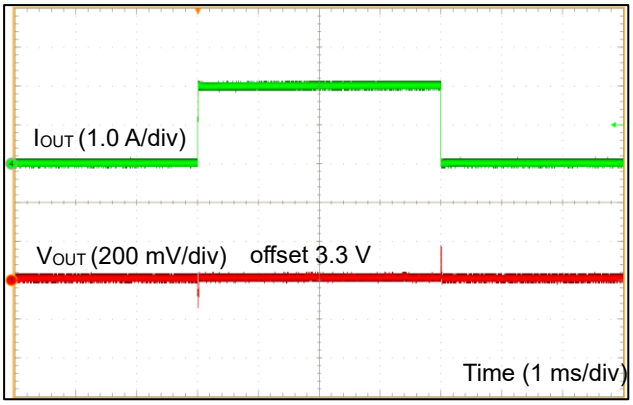


Figure 62. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

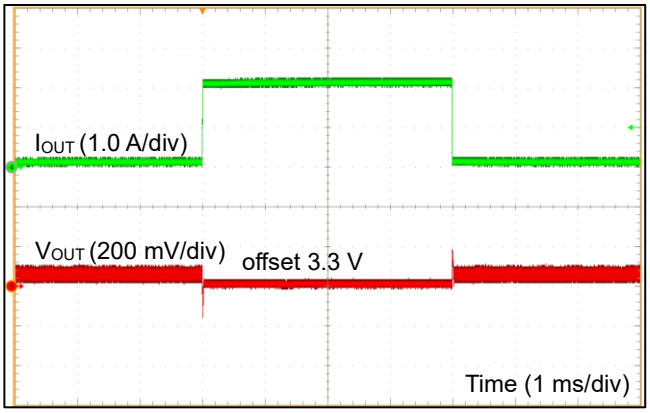


Figure 63. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0.1 A to 2 A)

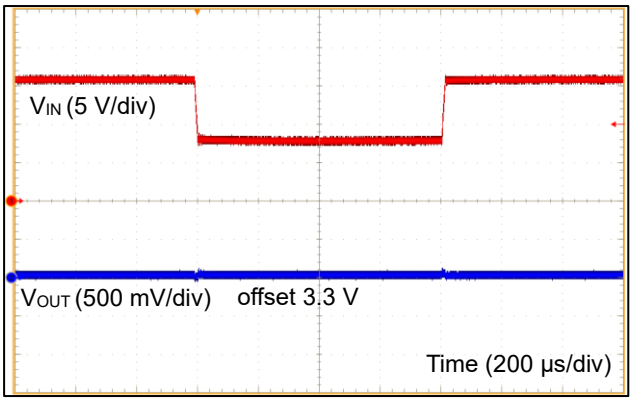


Figure 64. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

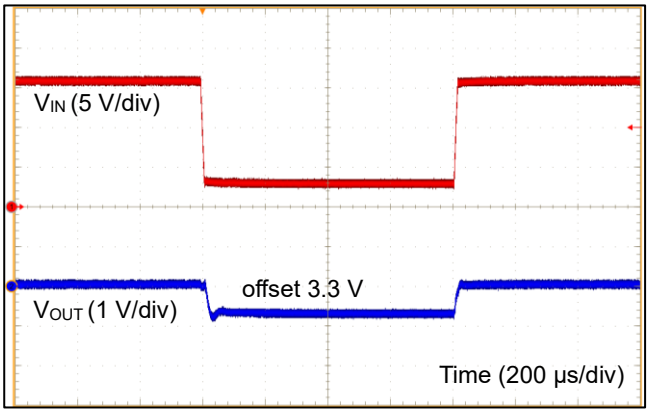


Figure 65. Line Response 2
(V_{IN} = 16 V to 4 V, I_{OUT} = 2 A)

Application Examples 2 - continued
(Ta = 25 °C)

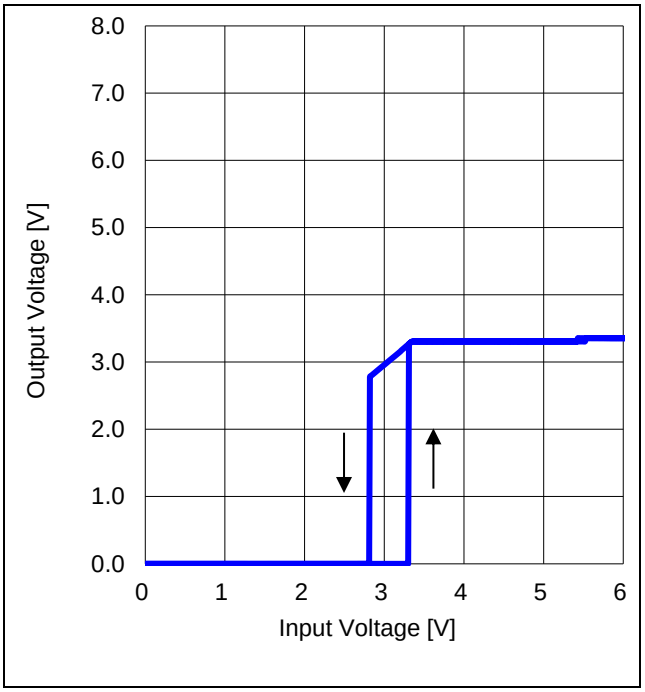


Figure 66. Output Voltage vs Input Voltage 1
(R_{LOAD} = 165 Ω)

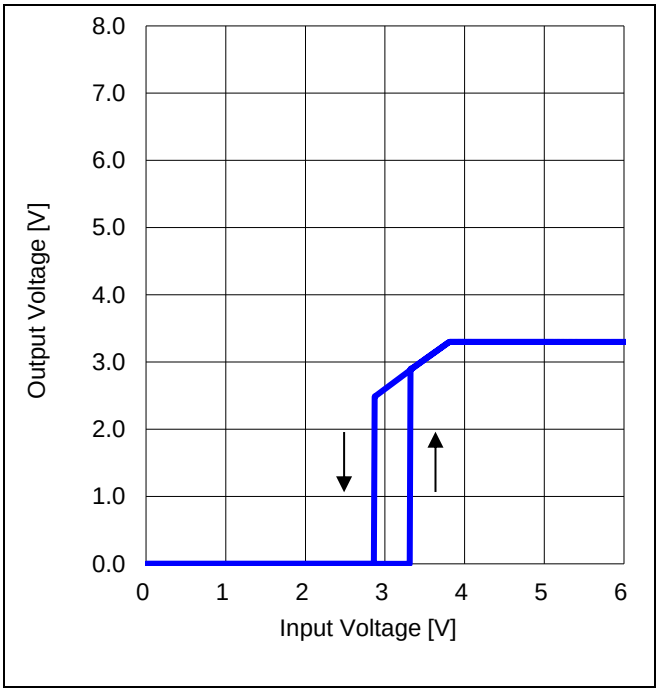


Figure 67. Output Voltage vs Input Voltage 2
(R_{LOAD} = 1.65 Ω)

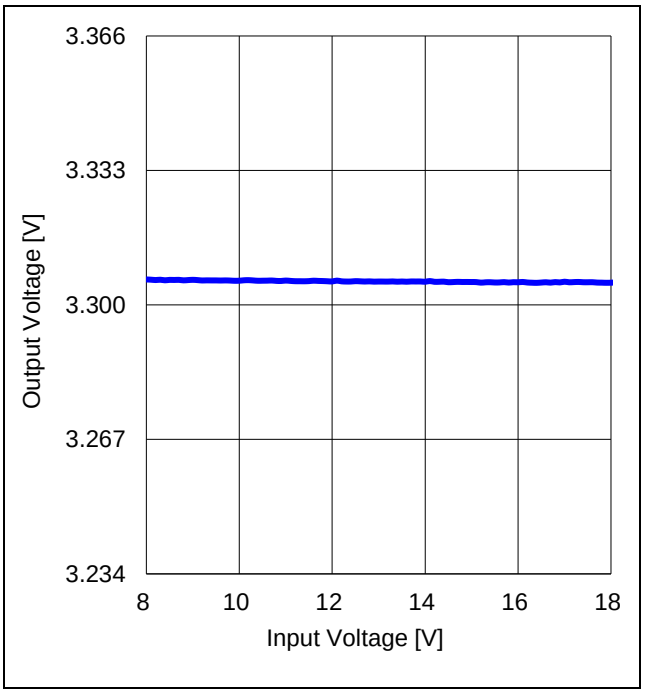


Figure 68. Line Regulation
(I_{OUT} = 2 A)

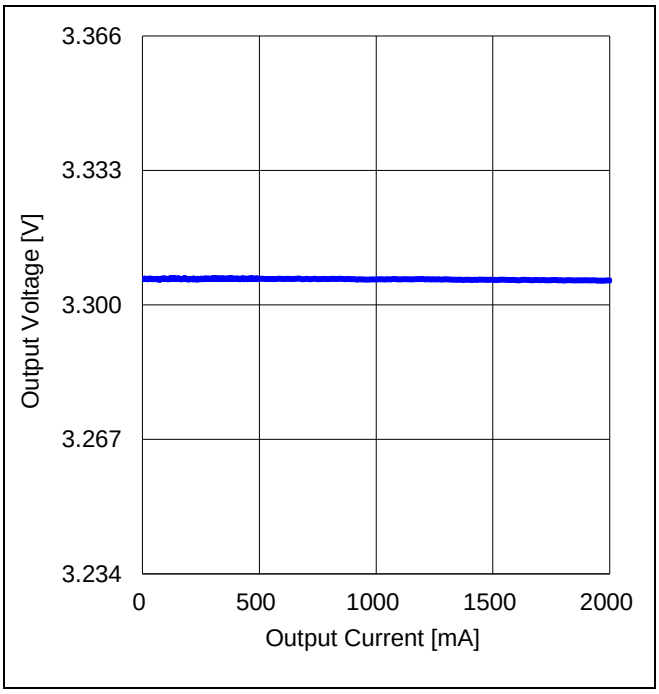


Figure 69. Load Regulation
(V_{IN} = 12 V, V_{MODE} = 5 V)

Application Examples 2 - continued
(Ta = 25 °C)

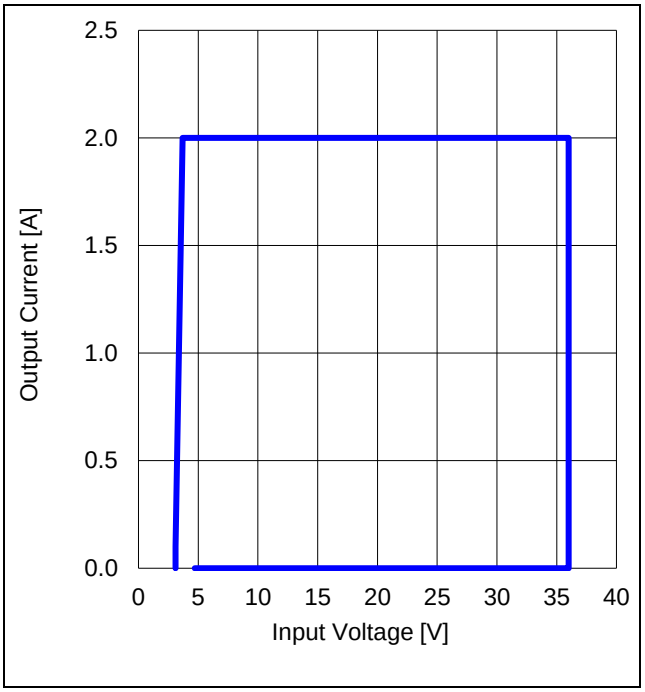


Figure 70. Output Current vs Input Voltage(Note 1)
Operating Range: Tj < 150 °C

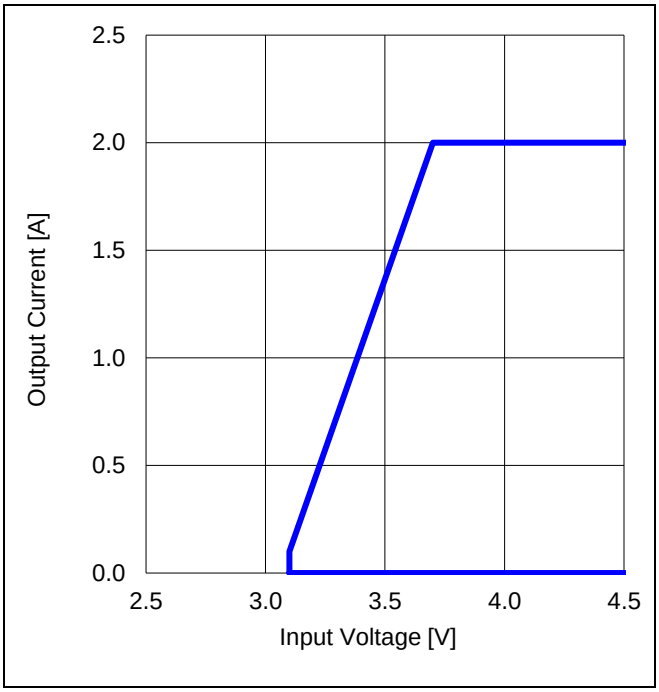


Figure 71. Output Current vs Input Voltage(Note 1)
Operating Range: Tj < 150 °C

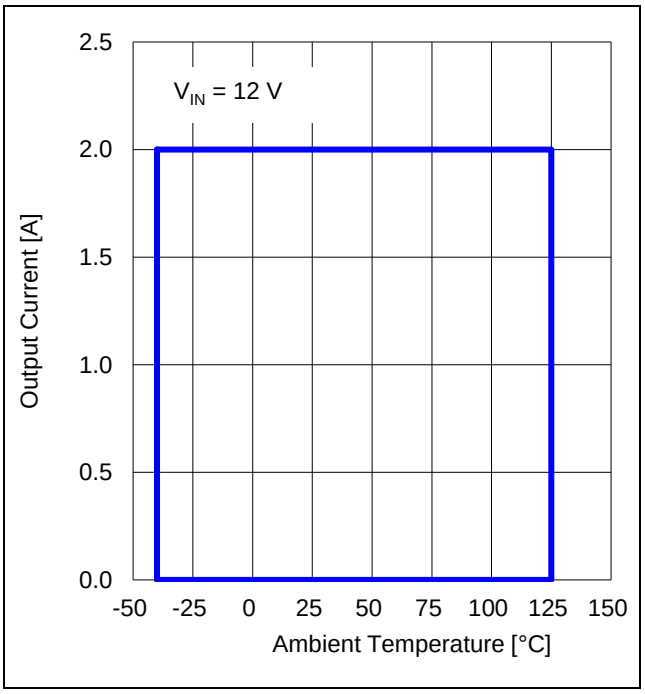


Figure 72. Output Current vs Ambient Temperature(Note 1)
Operating Range: Tj < 150 °C

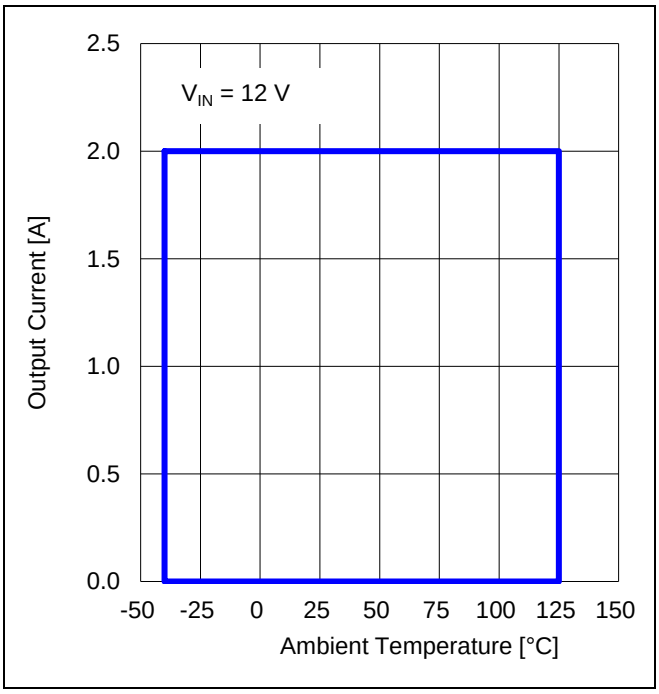


Figure 73. Output Current vs Ambient Temperature(Note 1)
Operating Range: Tj < 150 °C

(Note 1) Measured on FR-4 board 100 mm x 75 mm, Copper Thickness: Top and Bottom 70 µm, 2 Internal Layers 35 µm.

Application Examples 3

Table 9. Specification Example 3

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	5.0 V
Switching Frequency	f_{SW}	400 kHz
Output Current	I_{OUT}	Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

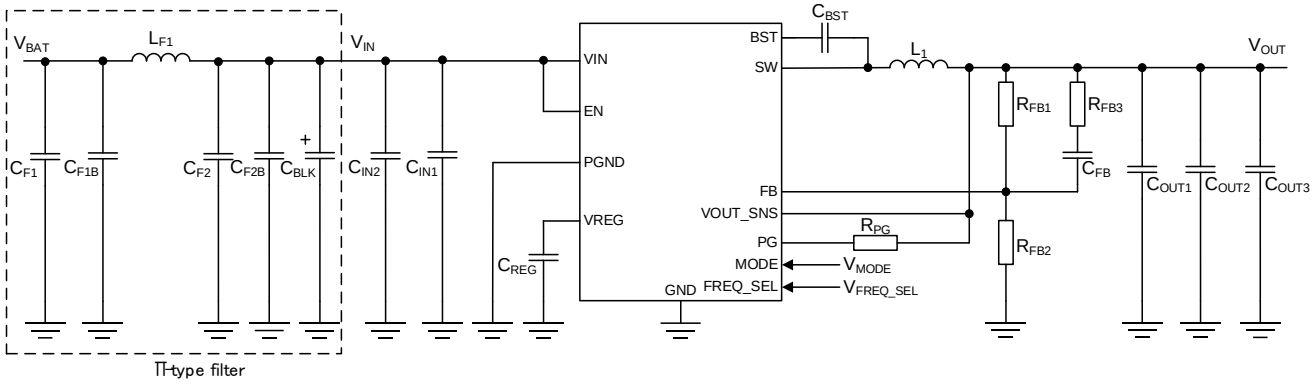


Figure 74. Reference Circuit

Table 10. Application Example 3 Parts List

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
C_{F1B}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{F2B}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic Capacitor	NICHICON
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{PG}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip Resistor	ROHM
L_1	W7.0 x H4.5 x L7.4 mm^3	10 µH	CLF7045NIT-100M-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT3}	-	-	-	-	-
C_{FB}	1005	22 pF, C0G, 50 V	GCM1555C1H220J	Ceramic	MURATA
R_{FB1}	1005	68 kΩ, 1 %, 1/16 W	MCR01MZPF6802	Chip Resistor	ROHM
R_{FB2}	1005	13 kΩ, 1 %, 1/16 W	MCR01MZPF1302	Chip Resistor	ROHM
R_{FB3}	1005	1 kΩ, 1 %, 1/16 W	MCR01MZPF1001	Chip Resistor	ROHM

Application Examples 3 - continued
(Ta = 25 °C)

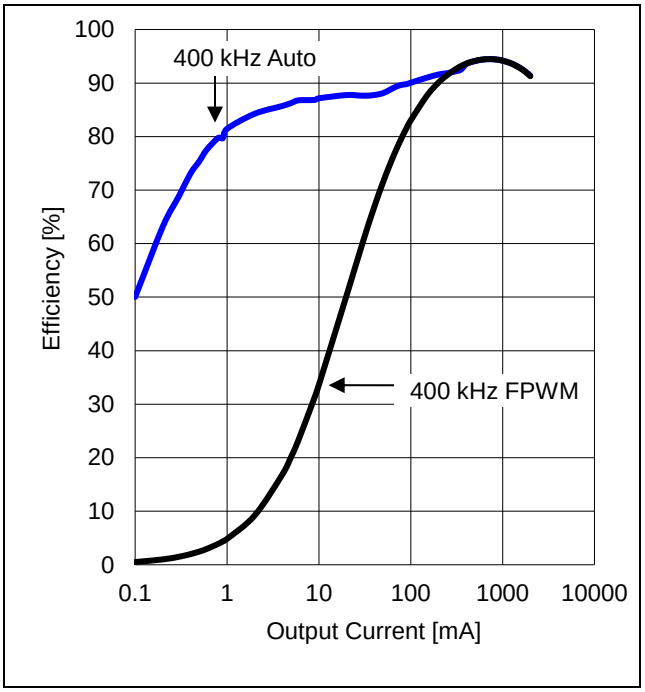


Figure 75. Efficiency vs Output Current
(V_{IN} = 12 V)

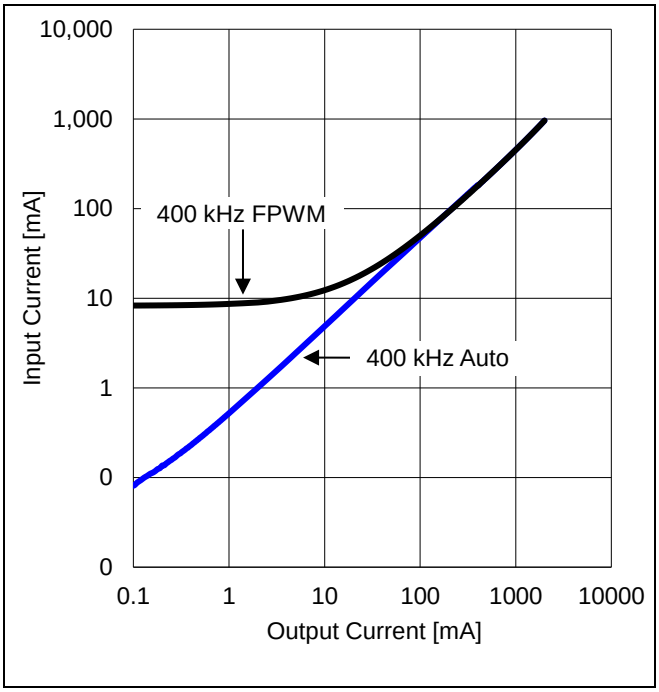


Figure 76. Input Current vs Output Current
(V_{IN} = 12 V)

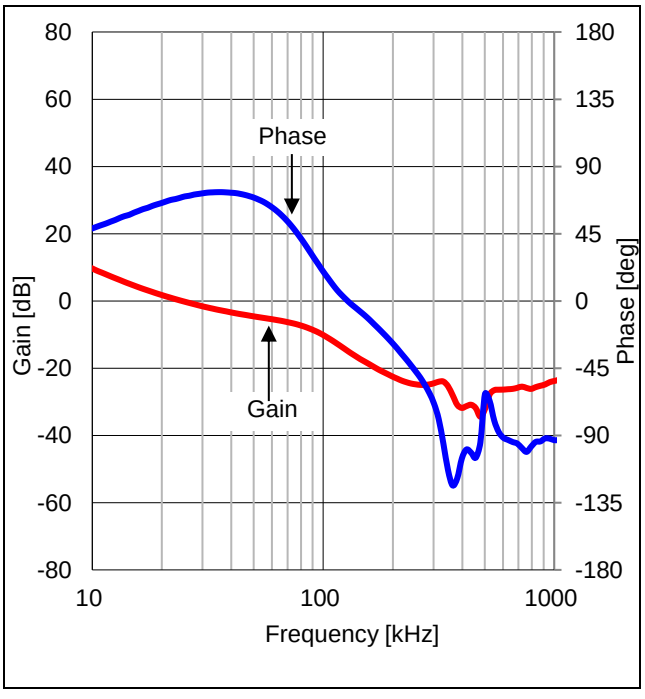


Figure 77. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

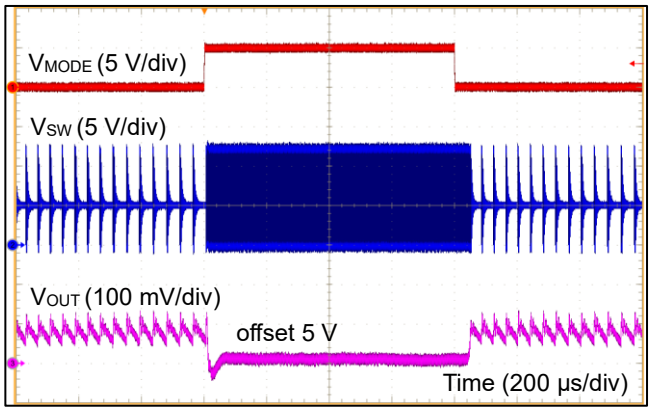


Figure 78. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 3 - continued
(Ta = 25 °C)

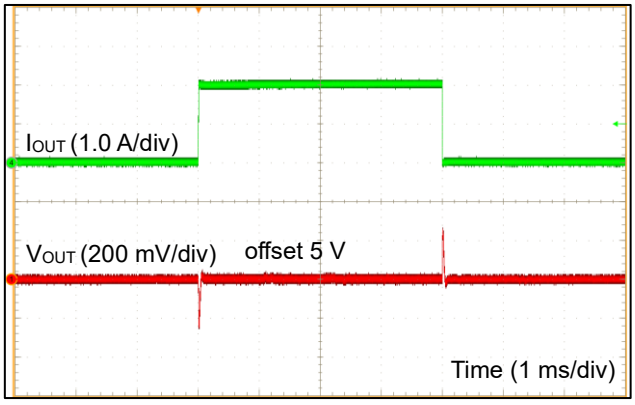


Figure 79. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

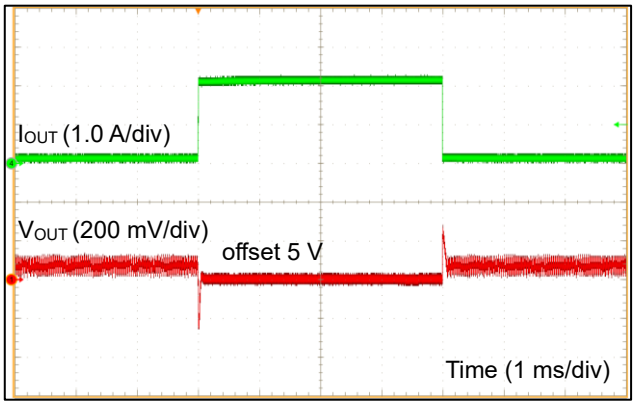


Figure 80. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0.1 A to 2 A)

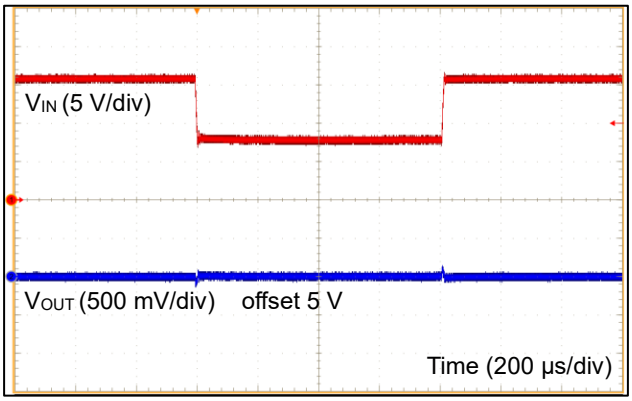


Figure 81. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

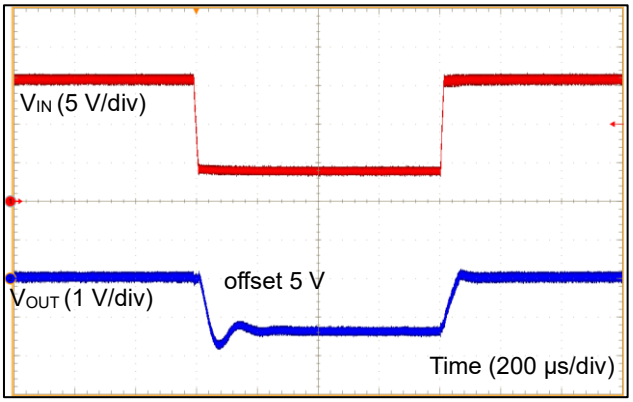


Figure 82. Line Response 2
(V_{IN} = 16 V to 4 V, I_{OUT} = 2 A)

Application Examples 3 - continued
(Ta = 25 °C)

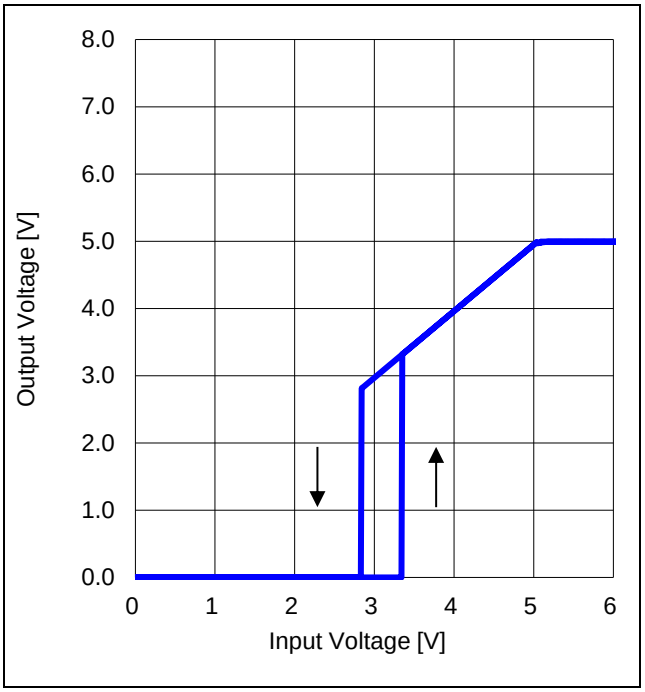


Figure 83. Output Voltage vs Input Voltage 1
(R_{LOAD} = 250 Ω)

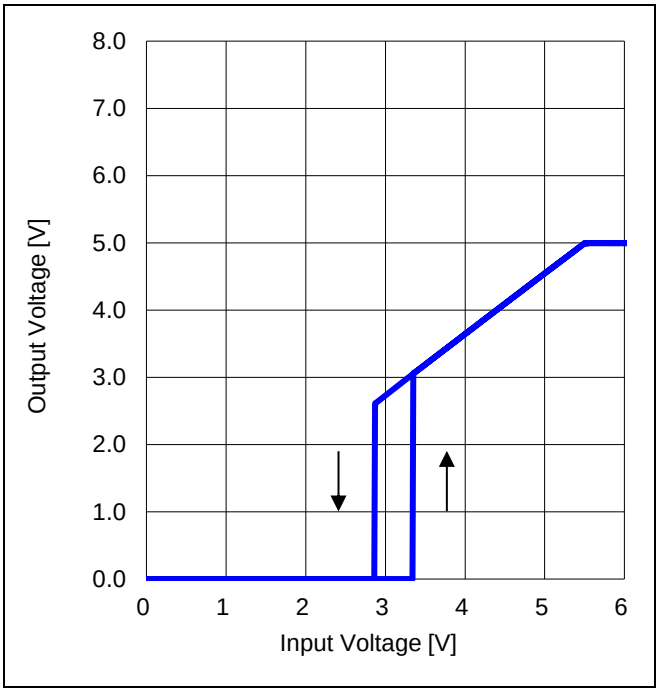


Figure 84. Output Voltage vs Input Voltage 2
(R_{LOAD} = 2.5 Ω)

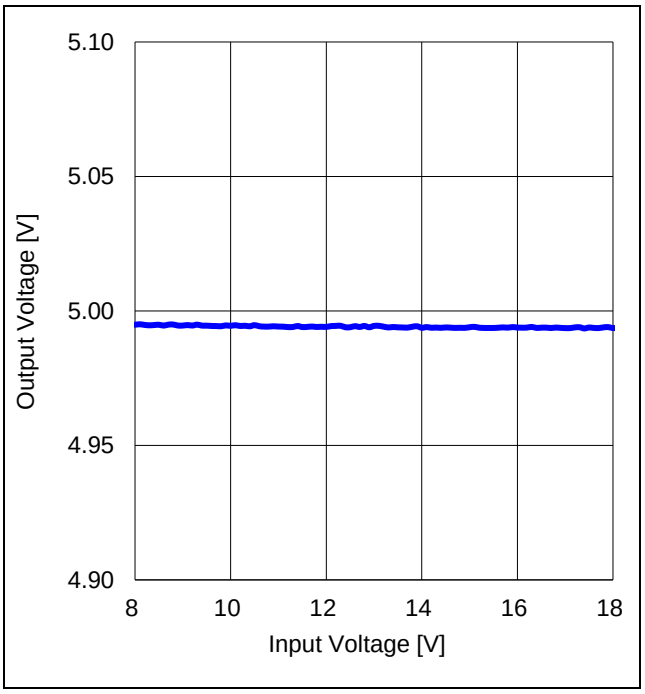


Figure 85. Line Regulation
(I_{OUT} = 2 A)

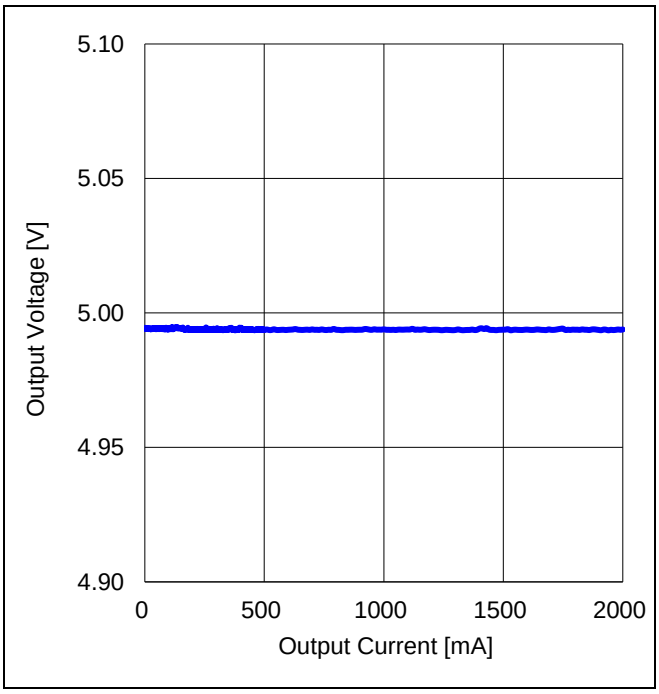


Figure 86. Load Regulation
(V_{IN} = 12 V, V_{MODE} = 5 V)

Application Examples 4

Table 11. Specification Example 4

Parameter	Symbol	Specification Case
Input Voltage	V_{IN}	8 V to 18 V
Output Voltage	V_{OUT}	3.3 V
Switching Frequency	f_{SW}	400 kHz
Output Current	I_{OUT}	Max 2.0 A
Operating Temperature Range	Ta	-40 °C to +125 °C

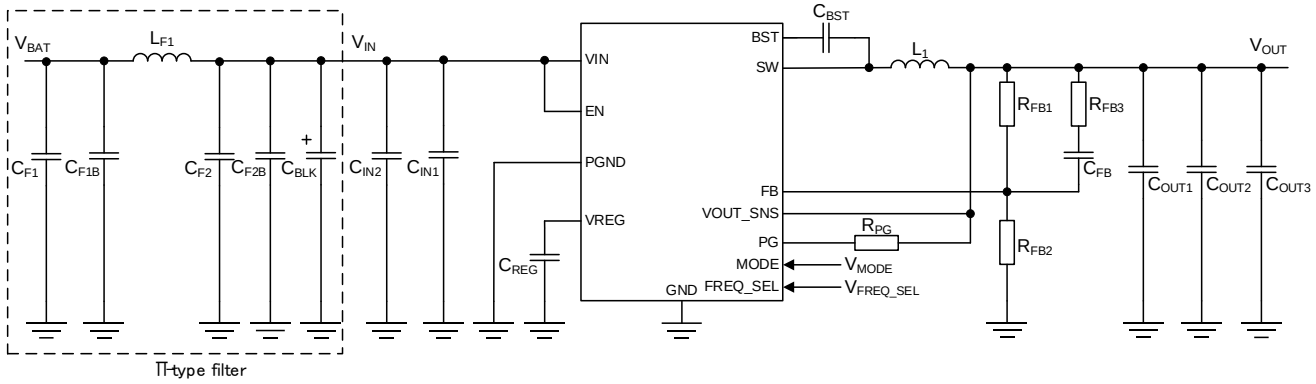


Figure 87. Reference Circuit

Table 12. Application Example 4 Parts List

No.	Package	Parameters	Part Name (Series)	Type	Manufacturer
C_{F1}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
C_{F1B}	3225	2.2 µF, X7R, 50 V	GCM31CR71H225K	Ceramic	MURATA
L_{F1}	W6.0 x H4.5 x L6.3 mm^3	2.2 µH	CLF6045NIT-2R2N-D	Inductor	TDK
C_{F2}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{F2B}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{BLK}	φ10 mm x L10 mm	220 µF, 35 V	UWD1V221MCL1GS	Electrolytic Capacitor	NICHICON
C_{IN2}	3225	4.7 µF, X7R, 50 V	GCM32ER71H475K	Ceramic	MURATA
C_{IN1}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
C_{REG}	2012	1 µF, X7R, 16 V	GCM21BR71C105K	Ceramic	MURATA
C_{BST}	1005	0.1 µF, X7R, 50 V	GCM155R71H104K	Ceramic	MURATA
R_{PG}	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip Resistor	ROHM
L_1	W7.0 x H4.5 x L7.4 mm^3	10 µH	CLF7045NIT-100M-D	Inductor	TDK
C_{OUT1}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT2}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{OUT3}	3225	22 µF, X7R, 10 V	GCM32ER71A226K	Ceramic	MURATA
C_{FB}	1005	22 pF, C0G, 50 V	GCM1555C1H220J	Ceramic	MURATA
R_{FB1}	1005	75 kΩ, 1 %, 1/16 W	MCR01MZPF7502	Chip Resistor	ROHM
R_{FB2}	1005	24 kΩ, 1 %, 1/16 W	MCR01MZPF2402	Chip Resistor	ROHM
R_{FB3}	1005	1 kΩ, 1 %, 1/16 W	MCR01MZPF1001	Chip Resistor	ROHM

Application Examples 4 - continued
(Ta = 25 °C)

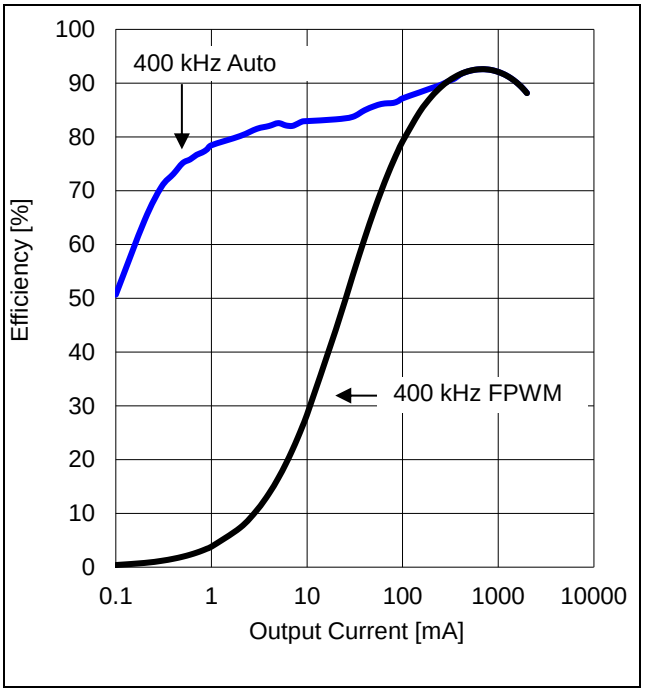


Figure 88. Efficiency vs Output Current
(V_{IN} = 12 V)

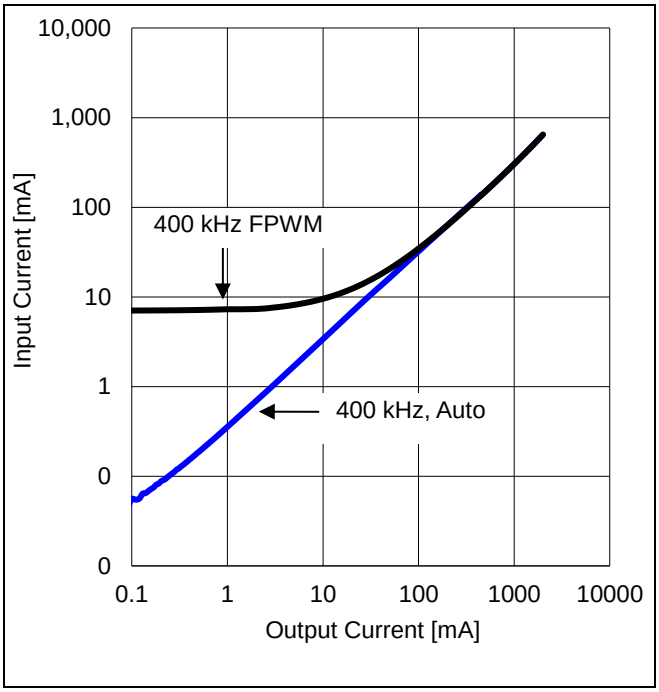


Figure 89. Input Current vs Output Current
(V_{IN} = 12 V)

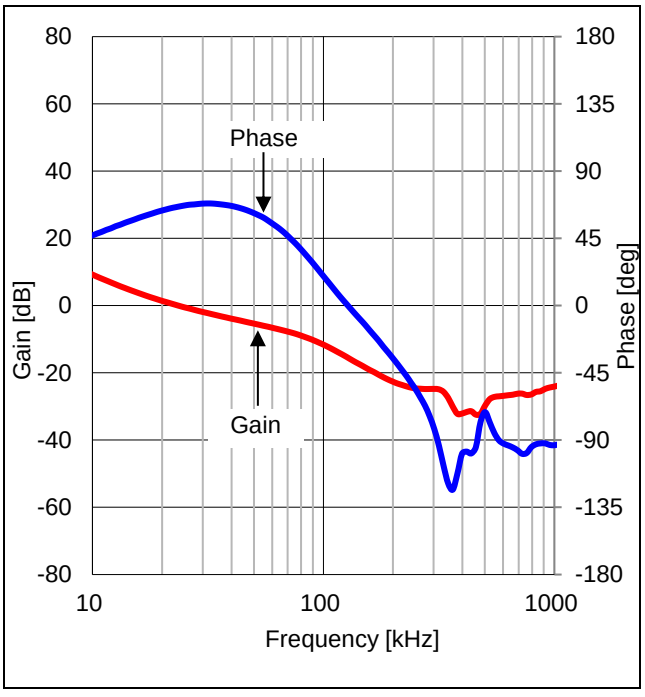


Figure 90. Frequency Characteristic
(V_{IN} = 12 V, I_{OUT} = 1.0 A)

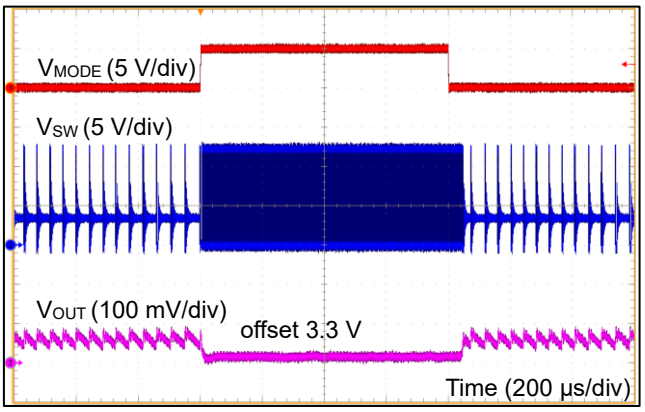


Figure 91. MODE ON/OFF Response
(V_{IN} = 12 V, I_{OUT} = 50 mA)

Application Examples 4 - continued
(Ta = 25 °C)

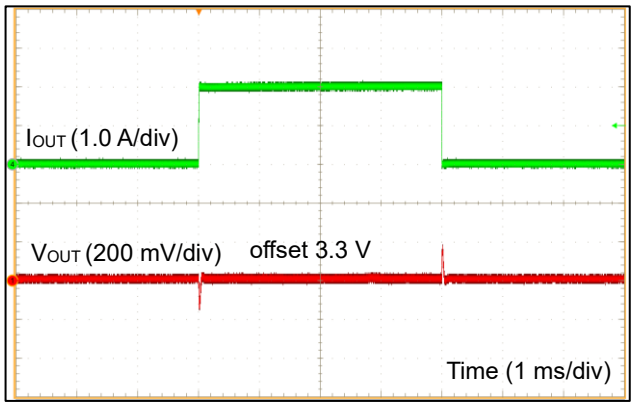


Figure 92. Load Response 1
(V_{IN} = 12 V, V_{MODE} = 5 V, I_{OUT} = 0 A to 2 A)

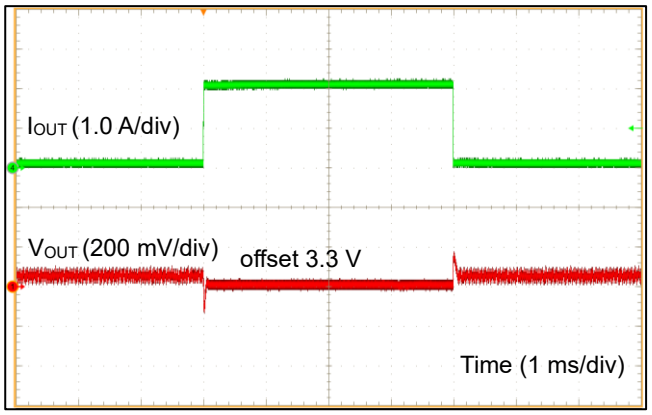


Figure 93. Load Response 2
(V_{IN} = 12 V, V_{MODE} = 0 V, I_{OUT} = 0.1 A to 2 A)

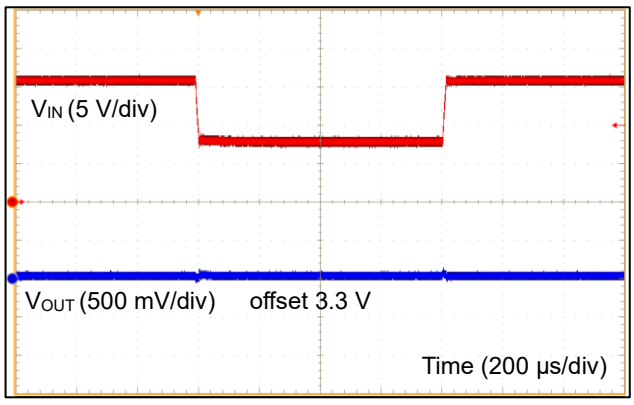


Figure 94. Line Response 1
(V_{IN} = 16 V to 8 V, I_{OUT} = 2 A)

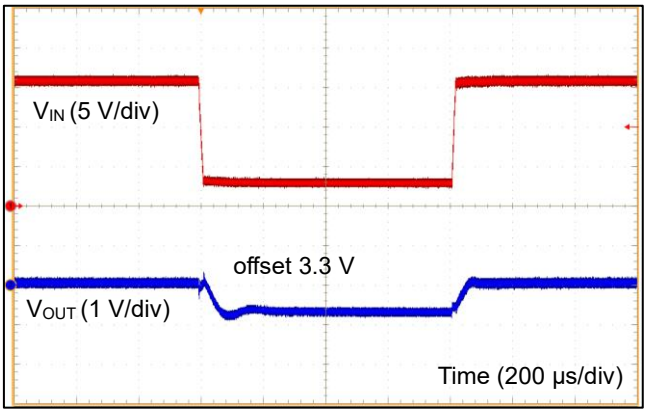


Figure 95. Line Response 2
(V_{IN} = 16 V to 4 V, I_{OUT} = 2 A)

Application Examples 4 - continued
(Ta = 25 °C)

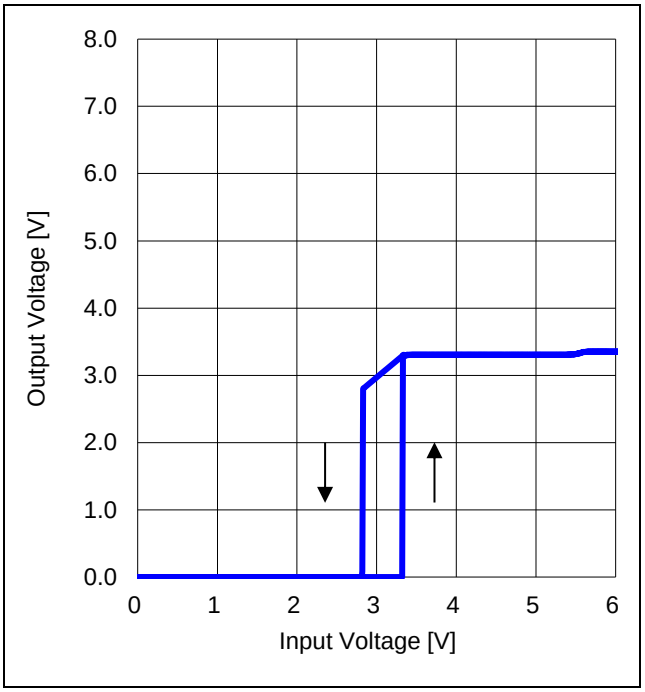


Figure 96. Output Voltage vs Input Voltage 1
(R_{LOAD} = 165 Ω)

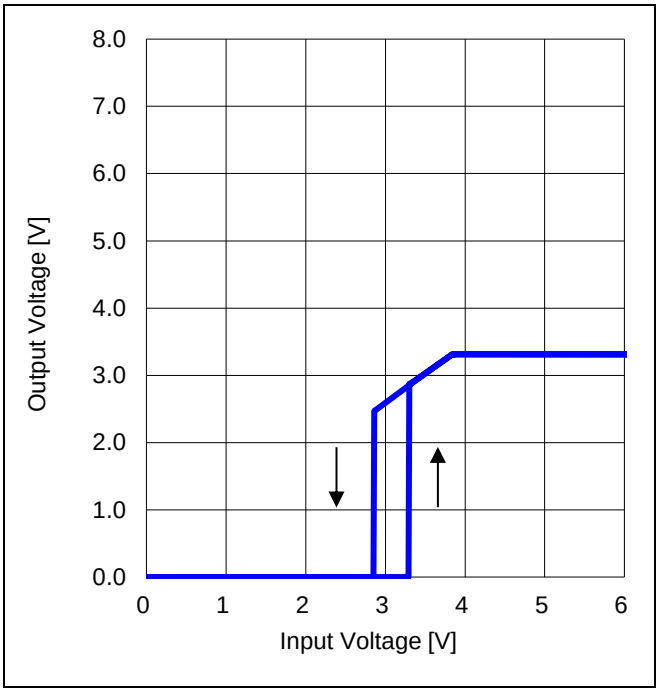


Figure 97. Output Voltage vs Input Voltage 2
(R_{LOAD} = 1.65 Ω)

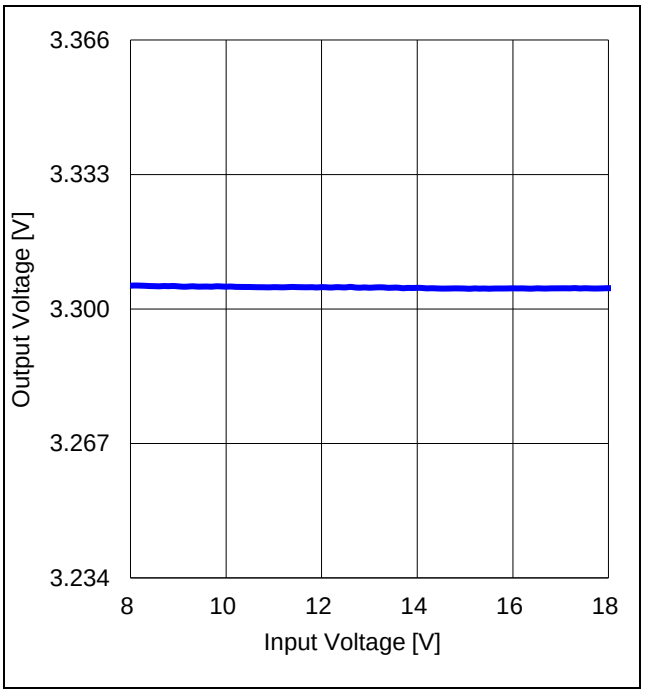


Figure 98. Line Regulation
(I_{OUT} = 2 A)

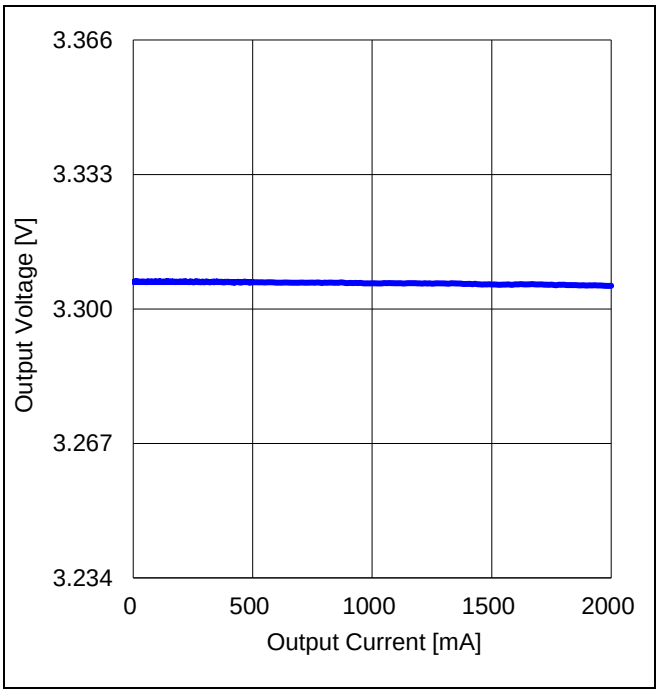


Figure 99. Load Regulation
(V_{IN} = 12 V, V_{MODE} = 5 V)

Automotive Power Supply Line Circuit

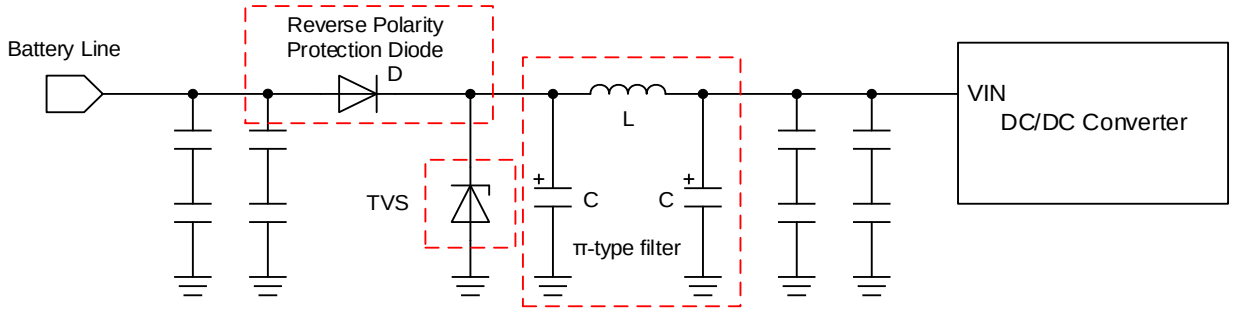


Figure 100. Automotive Power Supply Line Circuit

As a reference, the automotive power supply line circuit example is given in figure above.
The π-type filter is a third-order LC filter. In general, it is used in combination with decoupling capacitors for high frequency. Since large attenuation characteristics can be obtained, excellent characteristic is also obtained as an EMI filter. Devices used for π-type filters should be placed close to each other.
TVS (Transient Voltage Suppressors) is used for primary protection of the automotive power supply line. Since it is necessary to withstand high energy of load dump surge, a general zener diode is insufficient. Recommended device is shown in the following table.
In addition, a reverse polarity protection diode is needed considering if a power supply such as Battery is accidentally connected in the opposite direction.

Table 13. Reference Parts of Automotive Power Supply Line Circuit

Device	Part Name (series)	Manufacturer	Device	Part Name (series)	Manufacturer
L	CLF series	TDK	TVS	SMB series	Vishay
L	XAL series	Coilcraft	D	S3A to S3M series	Vishay
C	CJ series / CZ series	NICHICON			

Recommended Parts Manufacturer List

Table 14. Recommended Parts Manufacturers for Reference

Type	Manufacturer	URL
Electrolytic Capacitor	NICHICON	www.nichicon.co.jp
Ceramic Capacitor	Murata	www.murata.com
Hybrid Capacitor	Suncon	www.sunelec.co.jp
Inductor	TDK	product.tdk.com
Inductor	Coilcraft	www.coilcraft.com
Inductor	SUMIDA	www.sumida.com
Diode	Vishay	www.vishay.com
Diode/Resistor	ROHM	www.rohm.com

PCB Layout Design

PCB layout design for DC/DC converter power supply IC is as important as the circuit design. Appropriate layout can avoid various problems caused by power supply circuit. The following explains the current path of a buck DC/DC converter and methods to reduce noise caused by current fluctuations.

The figure below shows Loop1, which represents the current flowing through the converter when the High Side Switch is ON and the Low Side Switch is OFF.

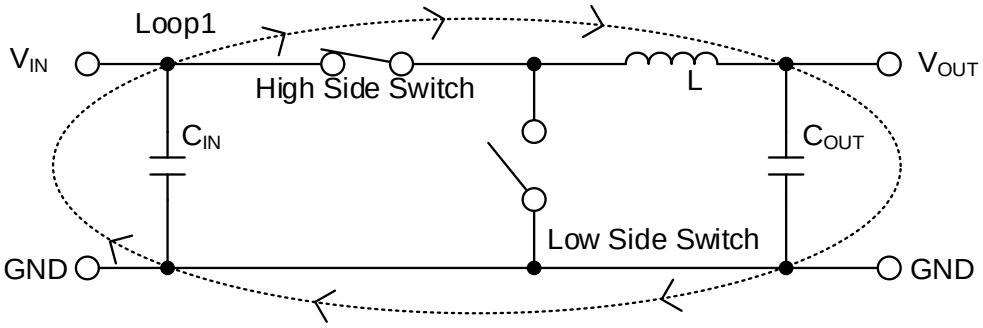


Figure 101. Current Path when High Side Switch = ON, Low Side Switch = OFF

The figure below shows Loop2, which represents the current flowing through the converter when the High Side Switch is OFF and the Low Side Switch is ON.

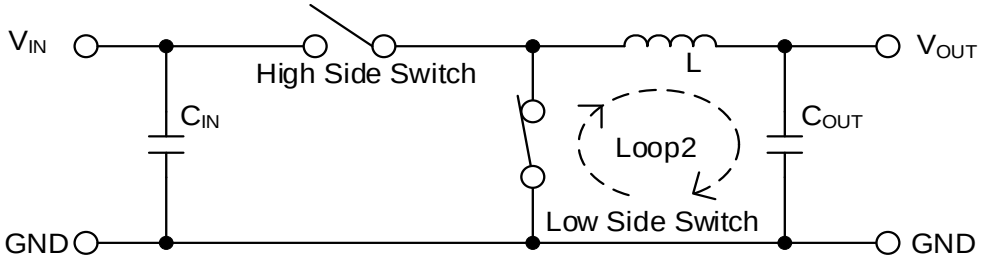


Figure 102. Current Path when High Side Switch = OFF, Low Side Switch = ON

The figure below shows the bold line, which represents the difference between Loop1 and Loop2. Each time the High-Side Switch and Low-Side Switch transition from OFF to ON or from ON to OFF, the current in the bold-line section fluctuates sharply. Since this system undergoes rapid changes, the waveform contains several high-frequency components. Therefore, reducing the area of the bold-line section formed by the input capacitor and the IC as much as possible helps minimize noise. For more details, please refer to the application note "PCB Layout Techniques for Buck Converters" in the Switching Regulator series.

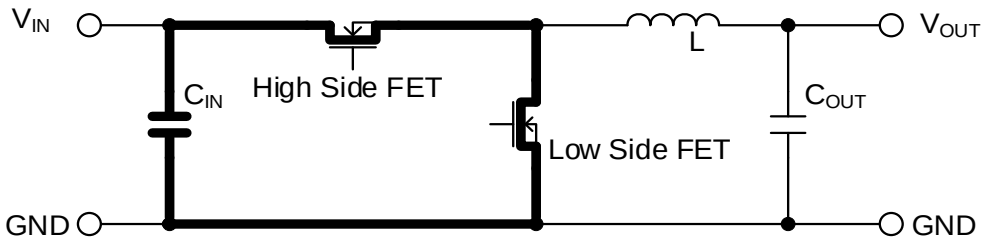


Figure 103. Difference of Current and Critical Area in Layout

PCB Layout Design - continued

When designing the PCB layout, please pay extra attention to the following points.

1. The decoupling capacitors for the VIN pin should be placed closest to the VIN pin and the PGND pin. In addition, placing a capacitor 0.1 µF (C_{IN1}) close to the VIN pin results in minimizing the high-frequency noise.
2. The device, the input capacitor, the output inductor and the output capacitor should be placed on the same surface side of the board and the connection of each part should be made on the same layer.
3. Place the ground plane in a layer closest to the surface layer where the device is mounted.
4. The GND pin is the reference ground and the PGND pin is the power ground. These pins should be connected through the back side of the device. The power systems ground should be connected to the ground plane using as many vias as possible.
5. The capacitor for VREG should be placed closest to the VREG pin, the GND pin and the PGND pin. As shown in the Recommended Board Layout Example, it can be realized that connecting with the shortest distance for the GND pin and the PGND pin by placing the capacitor for VREG on the closest to the VREG pin and wiring at the back side of the IC.
6. Place Bootstrap capacitor C_{BST} close to the SW pin and the BST pin.
7. To minimize the emission noise from switching node, the distance between the SW pin to inductor should be as short as possible and not to expand the copper area more than necessary.
8. Place the output capacitor close to the inductor and power ground area.
9. Make the feedback line from the output away from the inductor and the switching node. If this line is affected by external noise, an error may be occurred in the output voltage or the control may become unstable. Therefore, move the feedback line to back side layer of the board through via and connect it to the VOUT_SNS pin.
10. R_{FB1} and R_{FB2} Feedback resistors are needed for this IC. Place R_{FB1}, R_{FB2} close to the FB pin.
11. R_{FB0} is for measuring the frequency characteristic of the feedback. By inserting a resistor in R_{FB0}, the frequency characteristics (phase margin) of the feedback can be measured. R_{FB0} should be short-circuited for the normal use.

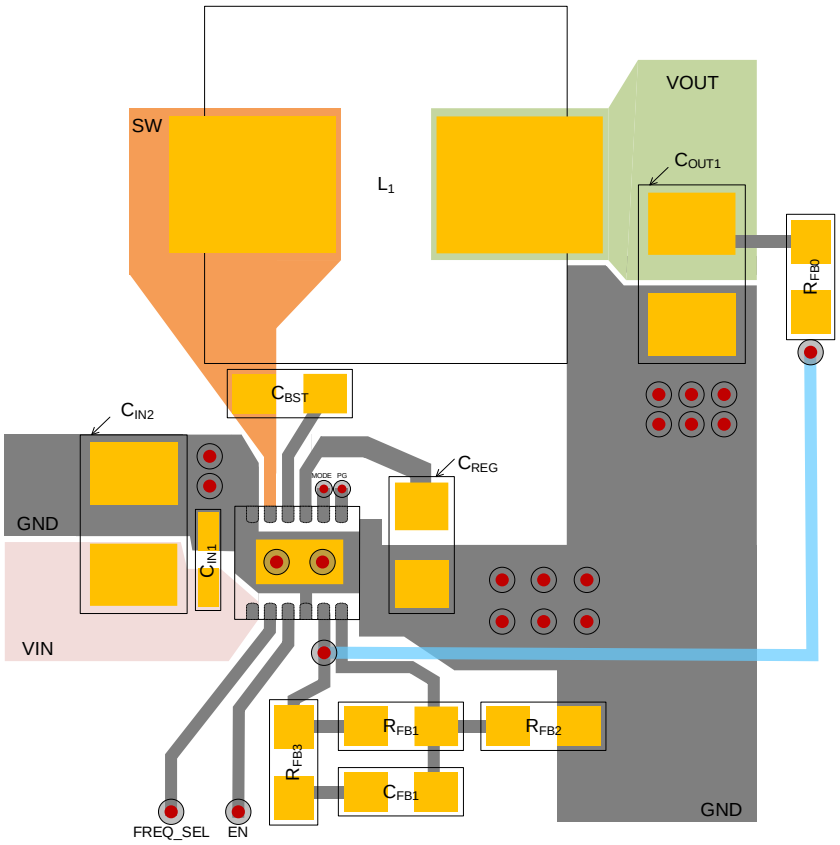


Figure 104. Recommended Board Layout Example

Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \ [°C]$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \ [°C]$$

Where:

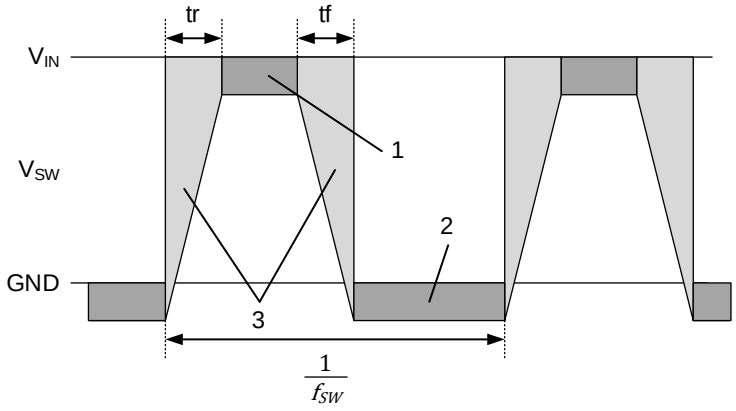
ψ_{JT} is junction to top characterization parameter
θ_{JA} is junction to ambient

The heat loss W of the IC can be obtained by the formula shown below.
This formula is approximation, please confirm this on the actual application circuit.

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{Q\_VIN2} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \ [W]$$

Where:

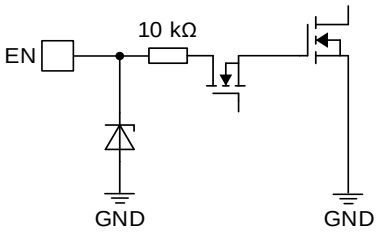
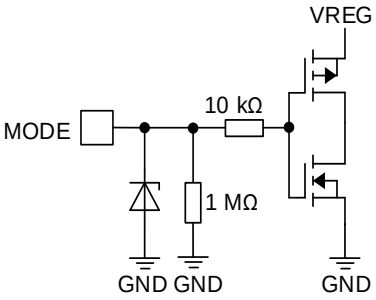
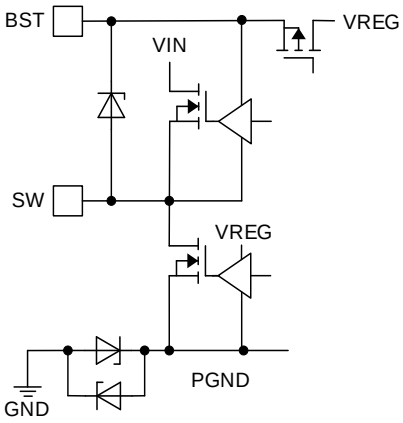
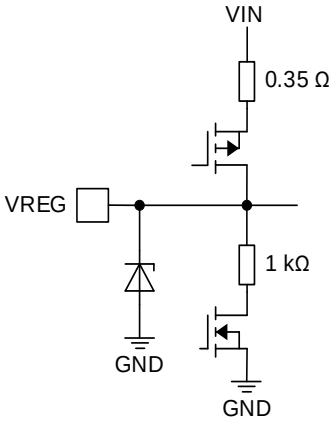
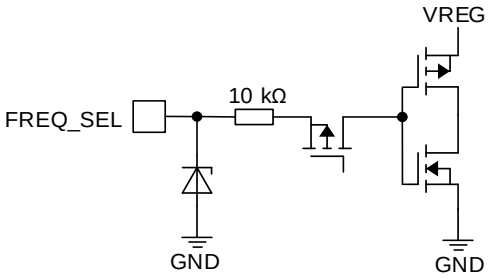
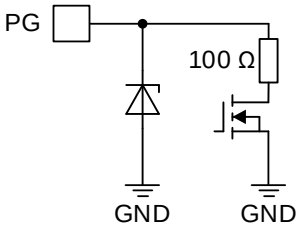
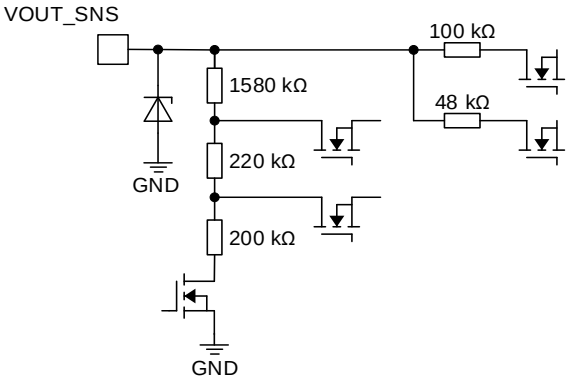
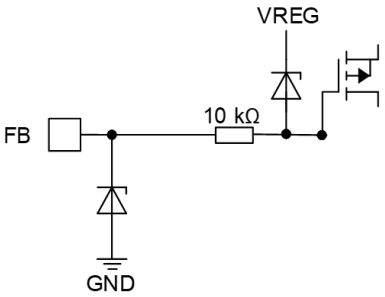
R_{ONH} is the High Side FET ON Resistance [Ω]
R_{ONL} is the Low Side FET ON Resistance [Ω]
I_{OUT} is the Load Current [A]
V_{OUT} is the Output Voltage [V]
V_{IN} is the Input Voltage [V]
I_{Q_VIN2} is the Quiescent Current from VIN [A]
tr is the Switching Rise Time [s] (5 ns, Typ)
tf is the Switching Fall Time [s] (2 ns, Typ)
f_{SW} is the Switching Frequency [Hz]



1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW}$

Figure 105. SW Waveform

I/O Equivalence Circuits

9. EN	2. MODE
	
5. SW, 4. BST	**3. VREG**
	
8. FREQ_SEL	**1. PG**
	
11. VOUT_SNS	**12. FB**
	

*Resistance value is Typ.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

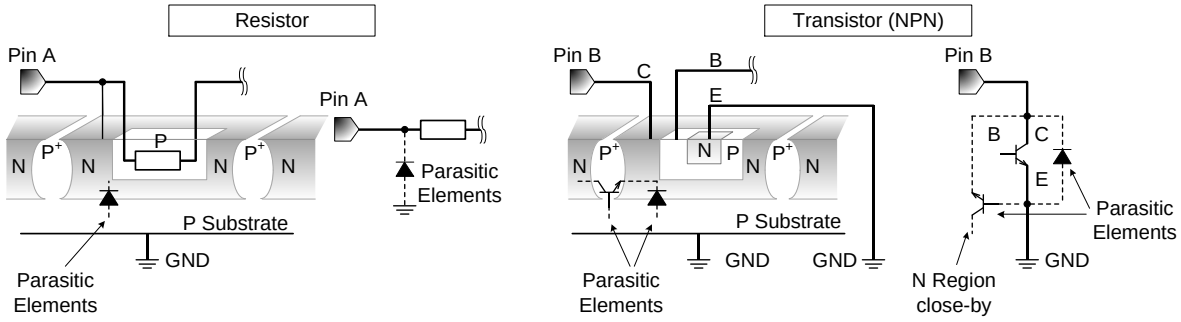


Figure 106. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

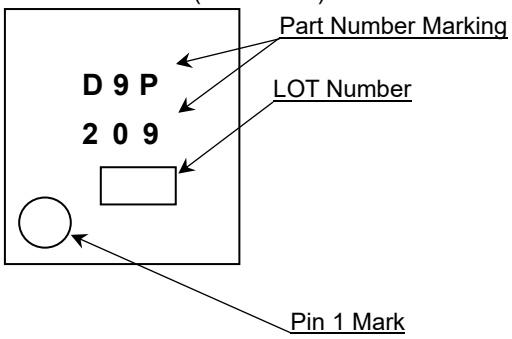
B	D	9	P	2	0	9	N	U	F	-	C E 2

Package
NUF: VSON12FV3030

Product Rank
C: for Automotive
Packaging Specification
E2: Embossed tape and reel

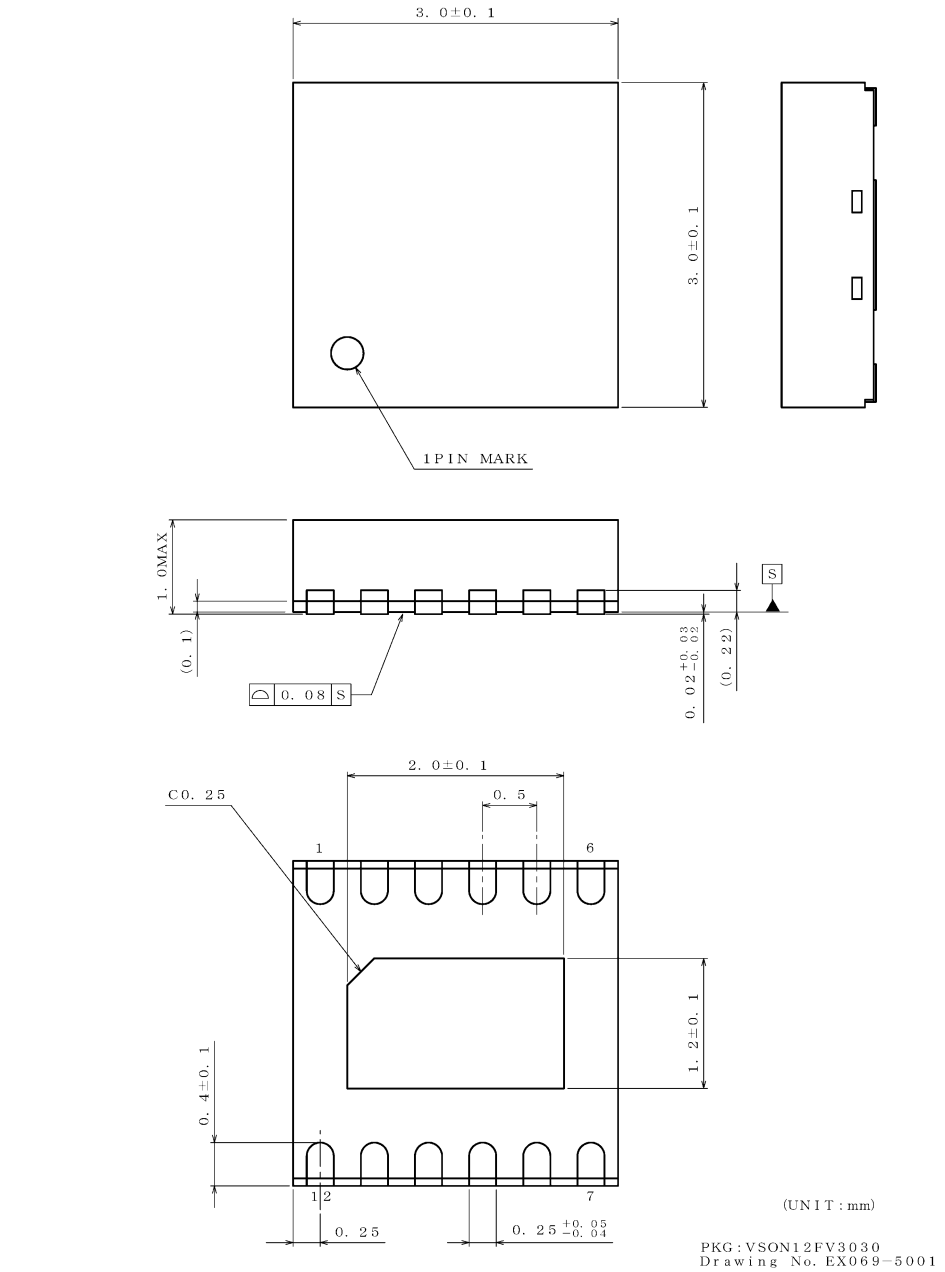
Marking Diagrams

VSON12FV3030 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VSON12FV3030



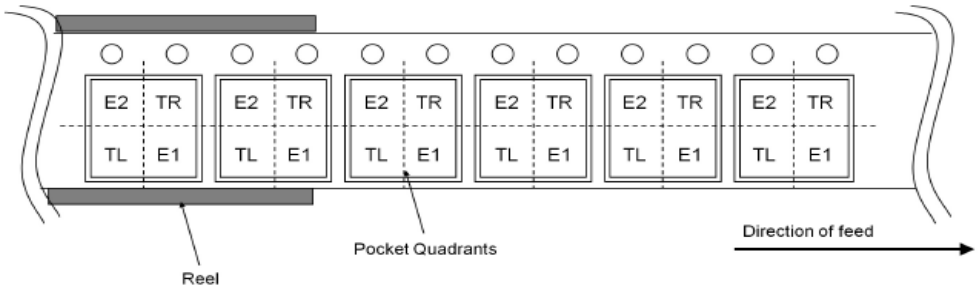
(UNIT : mm)

PKG : VSON12FV3030
Drawing No. EX069-5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
31.Mar.2025	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.