Power LSI series for Digital Camera and Digital Video Camera

Strobe Charge Control IC

BD4233NUX

●Outline

The strobe charge IC is a self-oscillating switching regulator that uses a transformer. It provides highly efficient applications for charging capacitors in sets with various strobes.

●Key Specifications

・SW pin input range:	48V
・SW pin peak current:	0.5A±20%
・Full charge detection voltage DC:	1.0V±1.1%
・Full charge detection voltage AC 200nsec:	1.0V-1.1%~1.35%
・Full charge detection voltage AC 100nsec:	1.0V-1.1%~1.6%
・Vth(START,IGBT_AN)	0.6V~1.5V

●Features

1) Built-in lowVth48V DMOS
2) Adjustable transformer primary-side peak current by RADJ pin
3) Charging control switching with the START pin
4) Includes high precision full charge voltage detection circuit and output pin
5) Various built-in protective circuits (TSD, UVLO, SDP)
6) Built-in IGBT driver

●Package

3.0mm×2.0mm×0.6mm　VSON010X3020

●Use

Digital still cameras、Mobile Phone

●Recommended Application Circuit

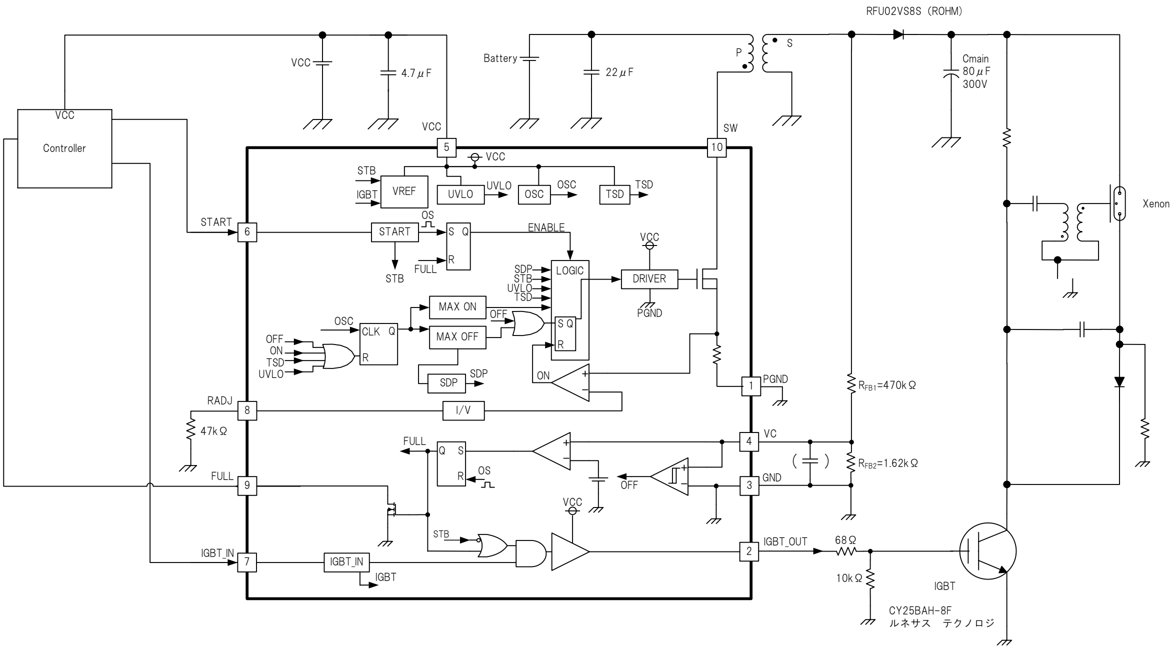


Fig.1 Application circuit

○Products：Silicon monolithic IC　○This product is not designed for normal operation with in a radioactive

Status of this document
The Japanese version of this document is the official specification. Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

●**package**

SON 10pin package VSON010X3020
(2.0mm×3.0mm×0.6mm)

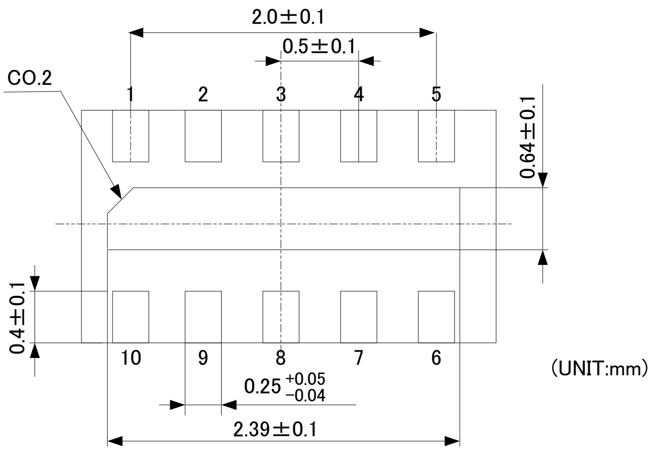


Fig.2

●**Pin Description**

Pin No.	Pin Name	Function
1	PGND	Power GND
2	IGBT_OUT	IGBT Driver output pin
3	GND	GND pin
4	VC	Full charge detection pin
5	VCC	VCC supply pin
6	START	Charge start signal input pin
7	IGBT_IN	IGBT Driver output start signal input pin
8	RADJ	Ipeak current control setting pin
9	FULL	Full charge detection signal output pin
10	SW	Switching pin

●**Block Diagram**

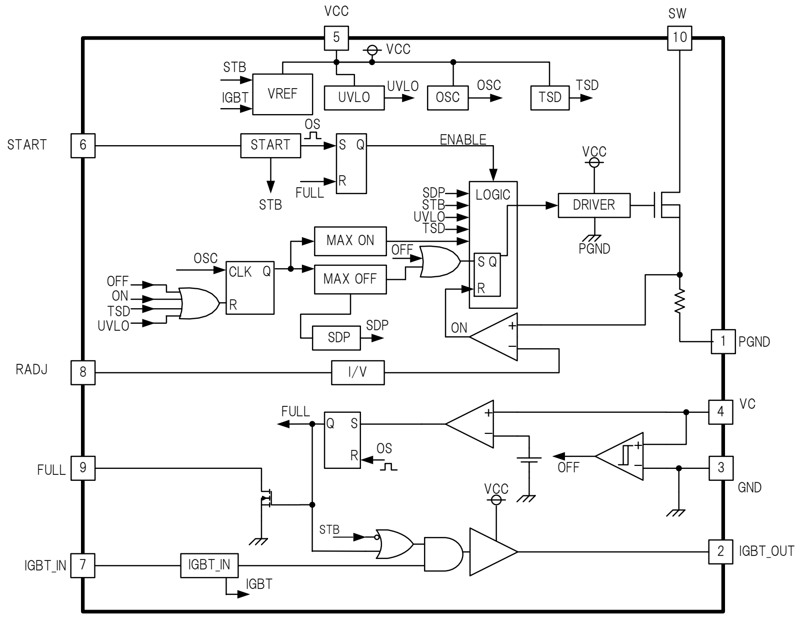


Fig.3

●**Absolute maximum ratings (Ta=25℃)**

Parameter	Symbol	Rating	Unit
VCC supply voltage	VCC	-0.3～7	V
SW pin	VSW	48	V
VC pin	VC	-0.6～7	V
START pin	START	-0.3～7	V
FULL pin	FULL	-0.3～7	V
IGBT_IN pin	IGBT_IN	-0.3～7	V
Operating temperature range	Topr	-35～+85	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tjmax	150	℃
Power dissipation	Pd	1540	mW

Table 1. Absolute Maximum Ratings

●**Operating condition**

Parameter	Symbol	Rating	Unit
VCC supply voltage range	VCC	2.5～5.5	V
VC pin	VC	-0.6～VCC	V
START Input pin voltage range	VSTART	0～VCC	V
IGBT_IN Input pin voltage range	VIGBT_IN	0～VCC	V
FULL Input pin voltage range	VFULL	0～5.5	V
SW pin current	ISW	0.5～2	A

Table 2. Operating Conditions

●Electrical characteristics

(**Unless specified, Ta=25℃, VCC=V(START)=3.4V,V(IGBT_IN)=0V**

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Overall device]						
VCC circuit current	ICC	-	1.5	3	mA	
Circuit current standby operation	ISTB	-	-	1	μA	START=0V
[Standby control START pin]						
START pin high voltage H1	VSTH	1.5	-	-	V	
START pin high voltage H2	VSTH	1.3	-	-	V	
START pin low voltage	VSTL	-	-	0.6	V	
Input bias current	ISTART	12	24	36	μA	START=3.4V
[Transformer primary-side driver block]						
SW pin leak current	ISWL	-	-	1	μA	SW=48V
SW pin peak current	IPEAK	0.4	0.5	0.6	A	RADJ=100kΩ
SW saturation voltage	VSAT	-	0.2	0.4	V	ISW=0.5A
RADJ adjustable range	RADJ	33	-	100	kΩ	
[Charging control block]						
Max on time	TONMAX	25	50	100	μs	
Max off time	TOFFMAX	12.5	25	50	μs	
[Transformer secondary-side detection block]						
VC pin input current	IVC	-	-	1	μA	VC=VCC
Full charge detection voltage	VFULLTH	0.989	1	1.011	V	
Full charge detection voltage AC1	VFULLTH_AC1	0.9890	1	1.0135	V	VC=200ns pulse input→FULL=H→L
Full charge detection voltage AC2	VFULLTH_AC2	0.9890	1	1.0160	V	VC=100ns pulse input→FULL=H→L
FULL pin ON resistor	RFULLL	0.5	1	2	kΩ	VC=VCC,FULL=0.5V
FULL pin leak current	IFULLL	-	-	1	μA	FULL=3.4V
[Protection circuit block]						
UVLO detect voltage	VUVLOTH	1.95	2.1	2.25	V	VCC detection
UVLO hysteresis	VUVLOHYS	120	200	280	mV	
[IGBT driver block]						
Output short high current	Ioso	90	140	200	mA	IGBT_IN=3.4V,START=0V,IGBT_OUT=0V
Output short low current	Iosi	30	60	90	mA	IGBT_IN=0, START=0V,IGBT_OUT=3.4V
IGBT_IN input high voltage Range H1	VIGBTH1	1.5	-	-	V	START=0V
IGBT_IN input high voltage range H2	VIGBTH2	1.3	-	-	-	START=0V,VCC =2.5V～5.5V Ta=-25℃～85℃
IGBT_IN input high voltage range	VIGBTL	-	-	0.6	V	START=0V
IGBT_IN sink current	IIGBT_IN	12	24	36	μA	START=0V
IGBT_IN response time Rise	Tres_rise	-	15	80	ns	IGBT_IN→IGBT_OUT response time (rise)
IGBT_IN response time Fall	Tres_fall	-	60	200	ns	IGBT_IN→IGBT_OUT response time (fall)

Table 3.

○This product is not designed for normal operation within a radioactive environment.

●Electrical characteristics data (1)

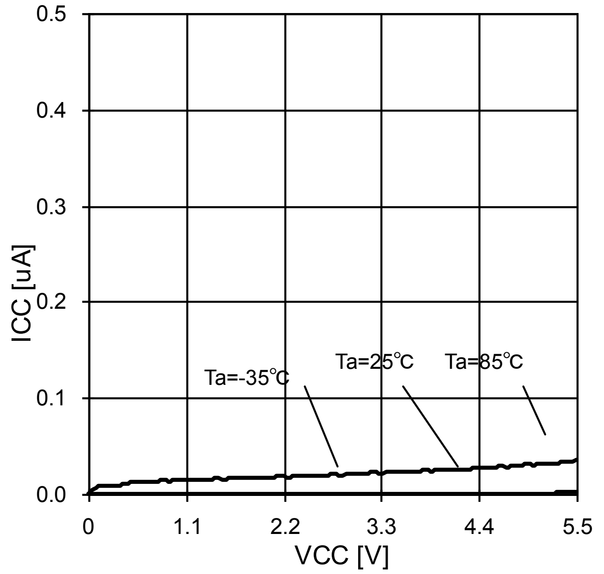


Fig.4 Circuit Current
(Standby Condition)

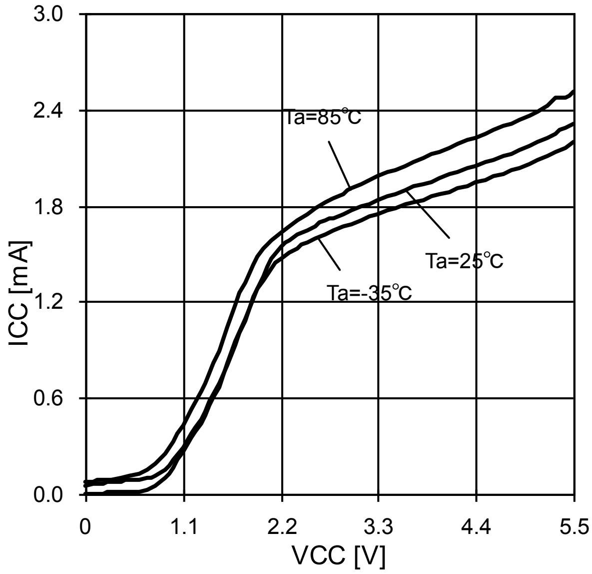


Fig.5 Circuit Current
(pwr_tr_on)

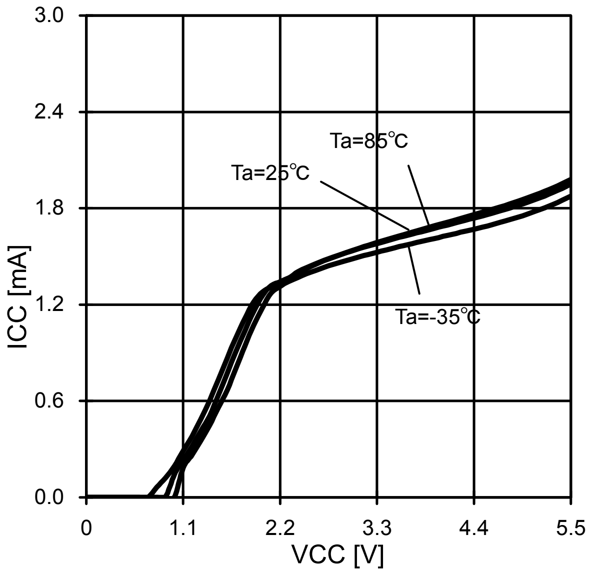


Fig.6 Circuit Current
(pwr_tr_off)

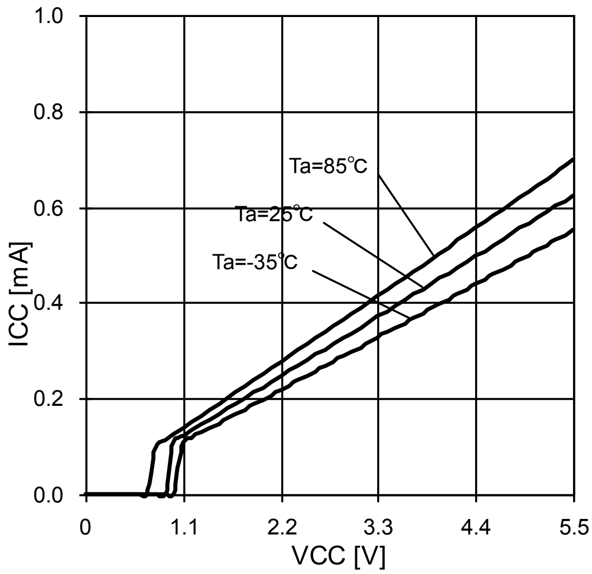


Fig.7 Circuit Current - VCC
(IGBTDRV=ON)

●**Electrical characteristics data (2)**

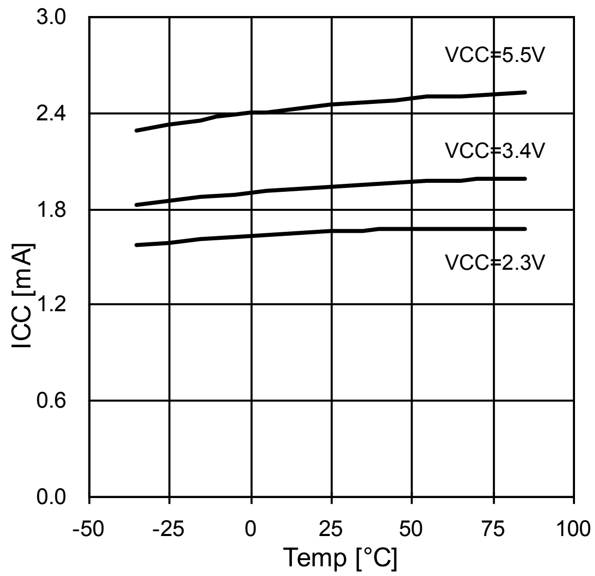


Fig.8 Circuit Current – Temp
(pwr_tr_on)

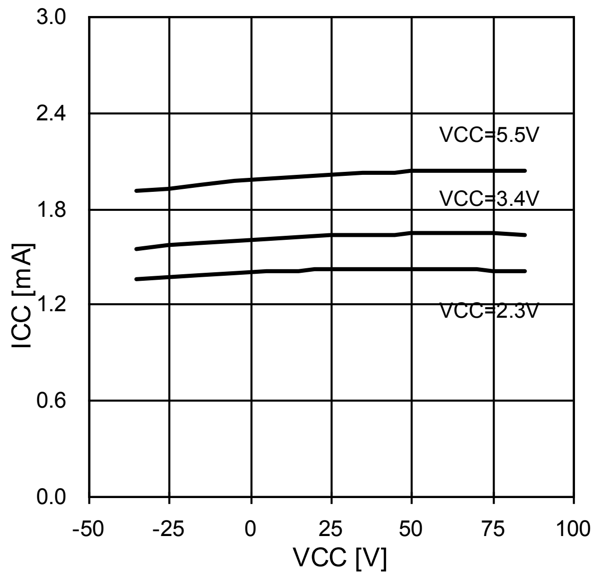


Fig.9 Circuit Current – Temp
(pwr_tr_off)

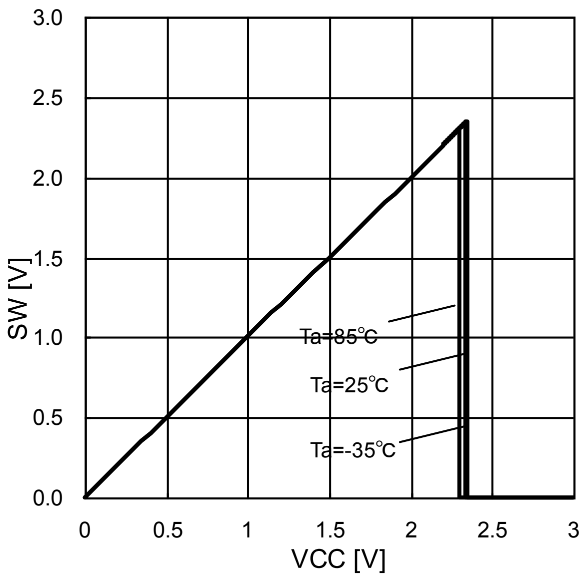


Fig.10 VCC UVLO Check
(Detect)

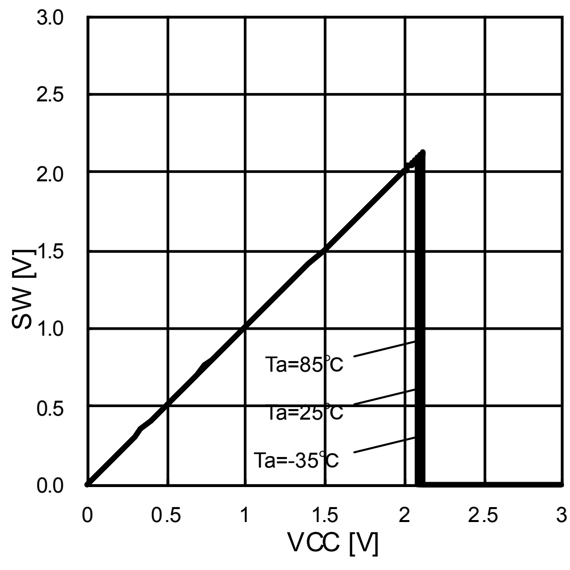


Fig. 11 VCC UVLO Check
(Release)

●Electrical characteristics data (3)

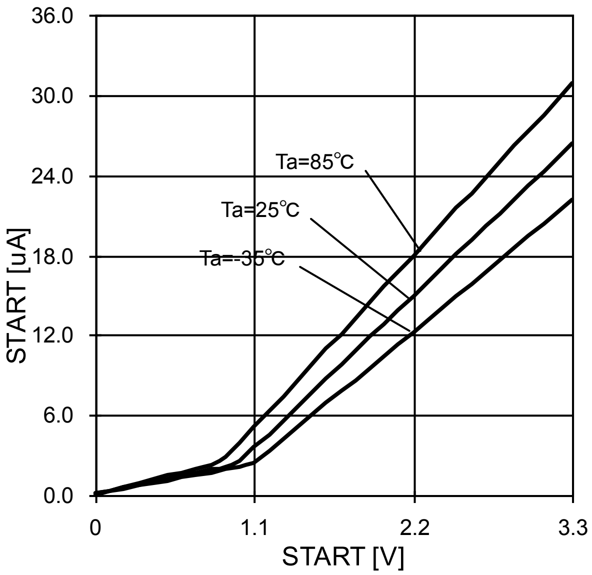


Fig.12 START Input Current

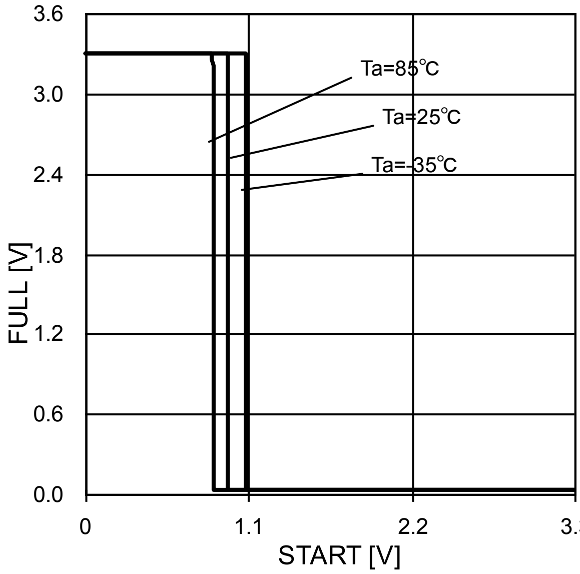


Fig.13 Start Threshold Voltage

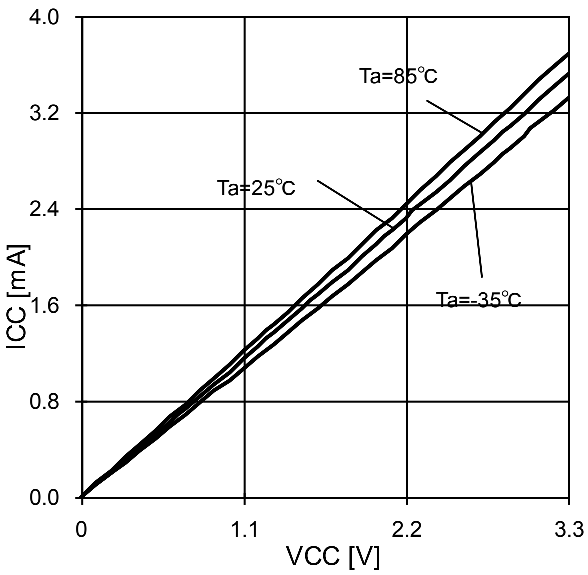


Fig.14 FULL Sink Current

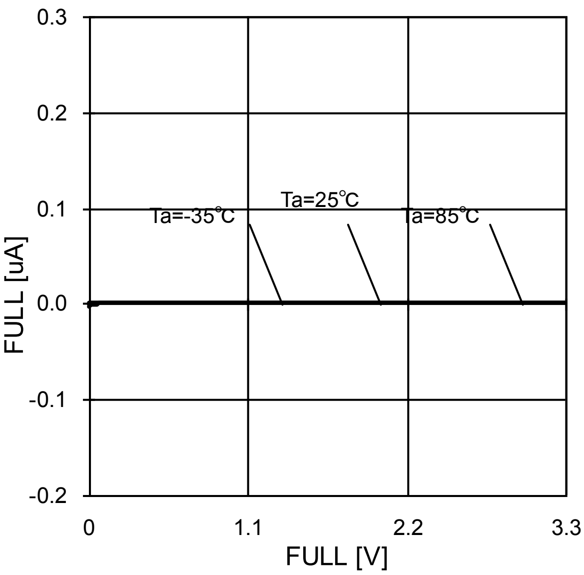


Fig. 15 FULL Pin Leak Current

●**Electrical characteristics data (4)**

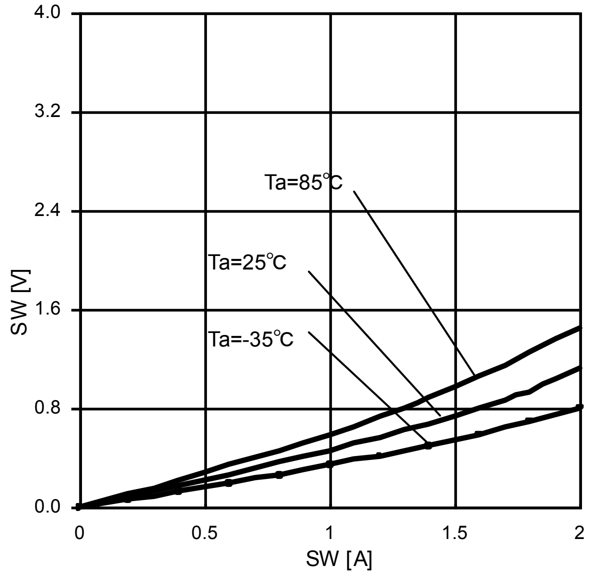


Fig.16 SAT Voltage

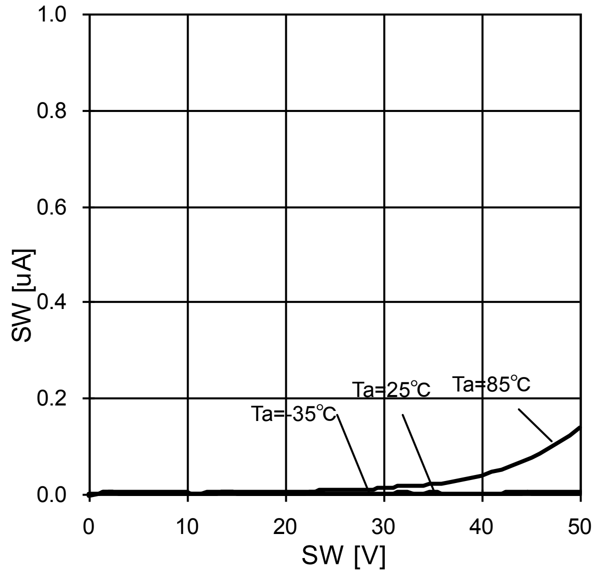


Fig.17 SW Leak Current

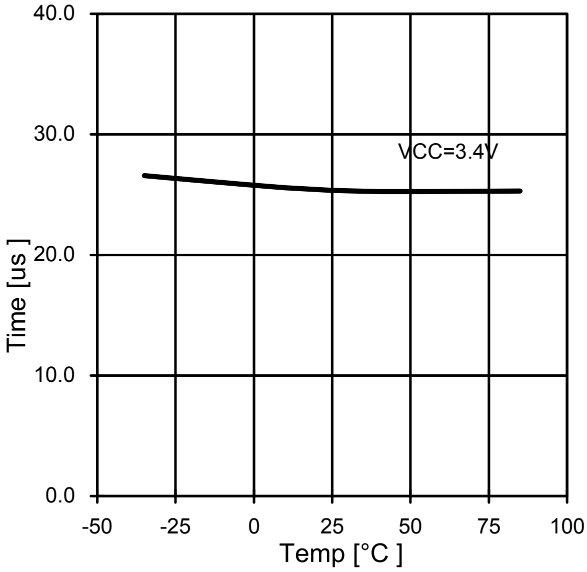


Fig.18 START Delay Time

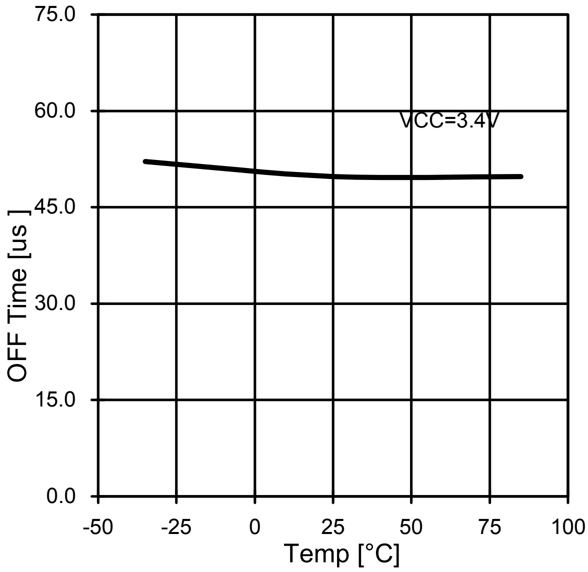


Fig. 19 MAX OFF Time

●**Electrical characteristics data (5)**

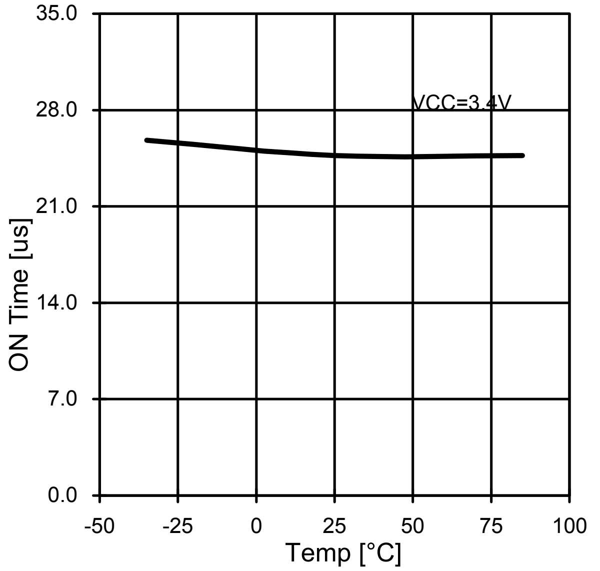


Fig.20 MAX ON Time

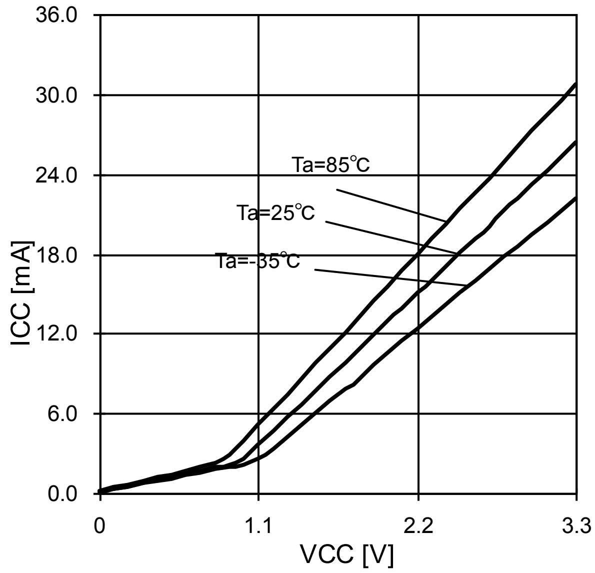


Fig.21 IGBT_IN Input Current

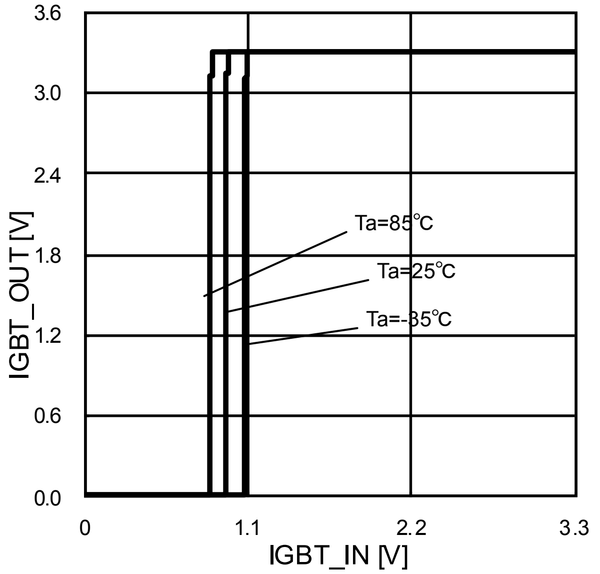


Fig.22 IGBT_IN Threshold Voltage

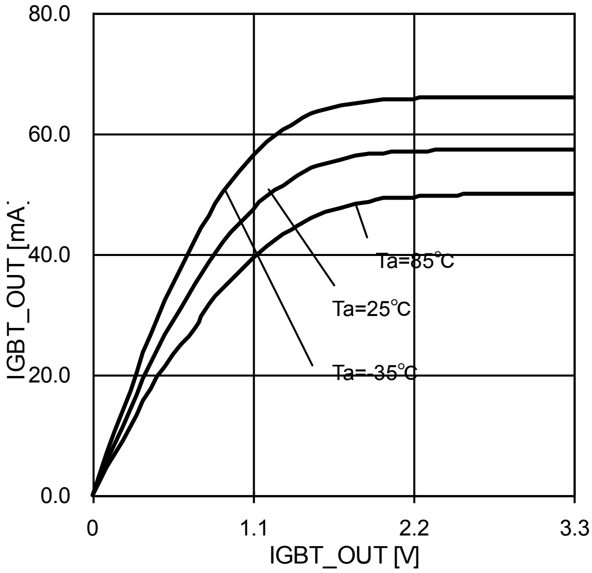


Fig. 23 IGBT_OUT Sink Current

●**Electrical characteristics data (6)**

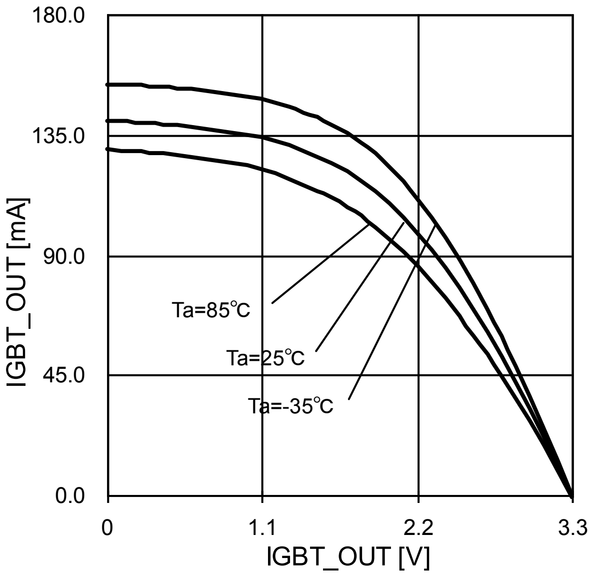


Fig.24 IGBT_OUT Source Current

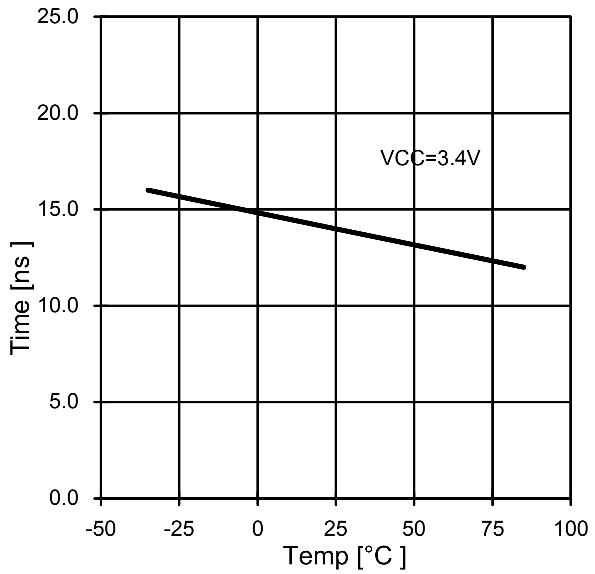


Fig.25 IGBT Response time Rise1
(START=0)

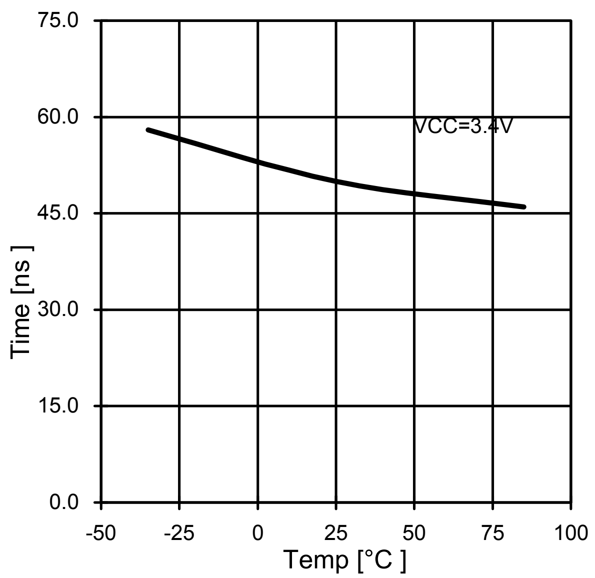


Fig.26 IGBT Response time Fall1
(START=0)

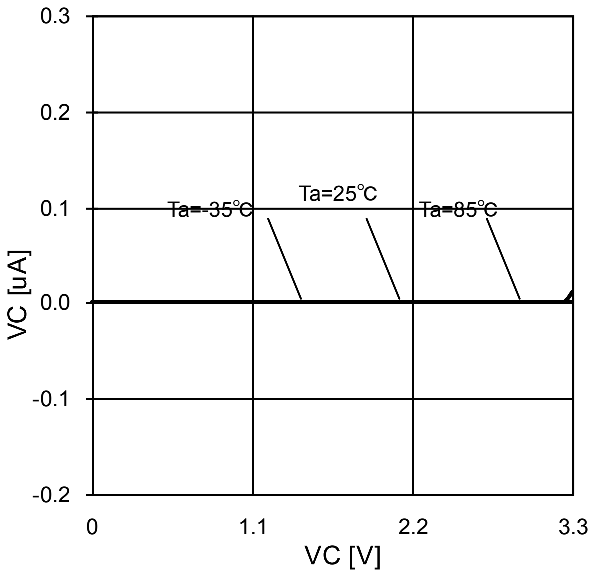


Fig.27 VC Input Current

●Electrical characteristics data (7)

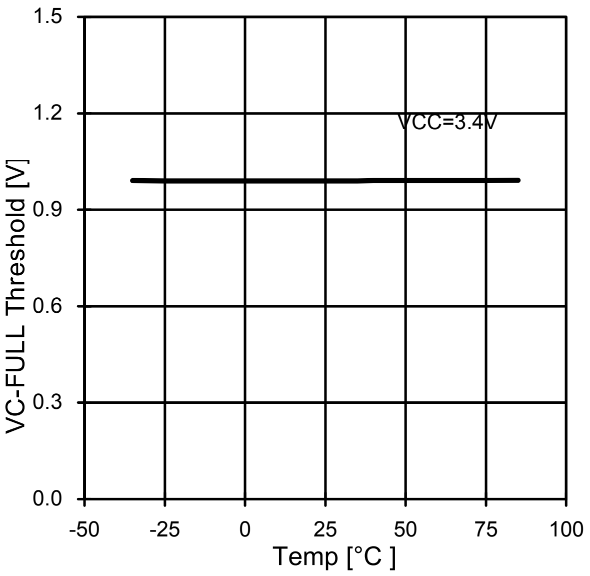


Fig.28 VC FULL Threshold Voltage vs TEMP
(Monitor FULL, sweep VC from –0.2 to 0.2)

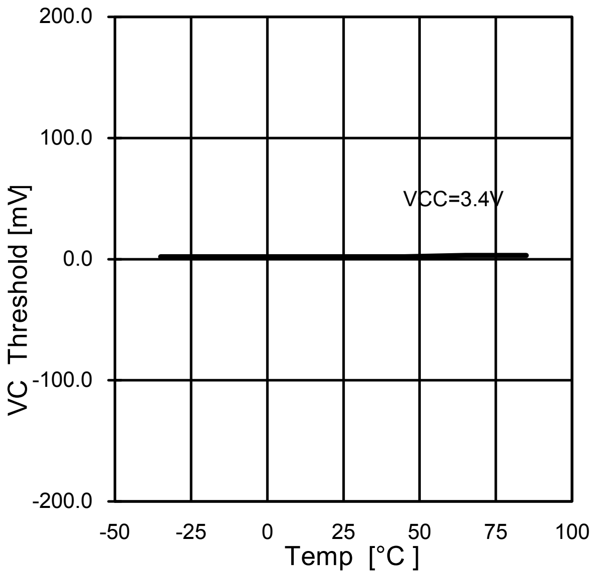


Fig. 29 VC OFF Threshold Voltage vs TEMP
(Monitor SW, sweep VC from –0.2 to 0.2)

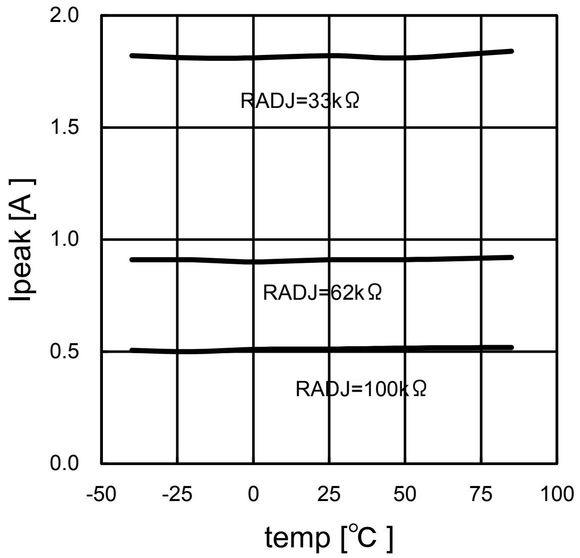


Fig. 30 ICOMP Peak Current

●Timing Chart and Description of Operation

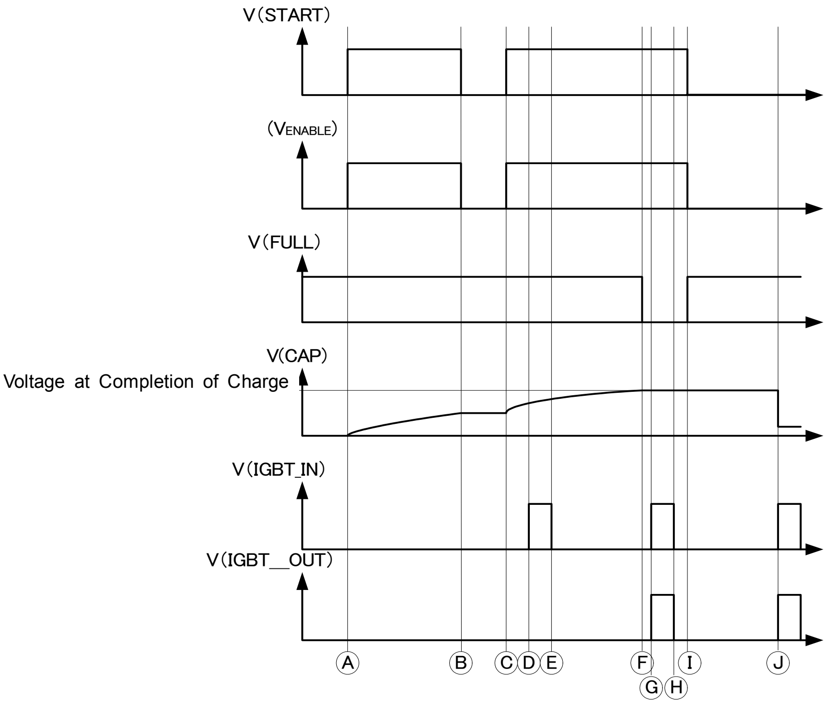


Fig 31. Timing Chart 1: Overall Operation

■Charge start/stop

In this IC, a charging operation starts when the START pin is set to "H" (See Time Ⓐ and Ⓒ in Fig 31.). In order to maintain the charging operation, the START pin must be set to "H". (See Time Ⓐ to Ⓑ, Ⓒ toⒾ in Fig 31.) If any of the conditions ① to ③ are satisfied, the charging operation stops.

① The START pin is set to "L".
② Charging is completed. The VC pin voltage reaches the specified voltage. (See Time Ⓕ in Fig 31.)
③ The protective circuit is activated (See Fig 33 and the Protective Circuit.)。

To re-charge, set the START pin to "L", and the FULL pin is changed from “L” to “H”. Also, if the CHARGE_ON pin is changed from "L" to "H" again, the charging operation re-starts. (See Time Ⓒ in Fig 31.)

■IGBT driver

Set the IGBT_IN pin to "H" when the IGBT driver satisfies the following 4 conditions. The "H" signal is output to the IGBT_OUT pin. (See Time Ⓖ and Ⓙ in Fig 31.)

① The VCC voltage is the UVLO release voltage or more.
② The FULL pin is set at "L".
③ Even if the IGBT_IN pin is set to "H" while the START pin is set to "H", the IGBT_OUT pin remains at "L" and no light flashes.

●Timing Chart and Description of Operation

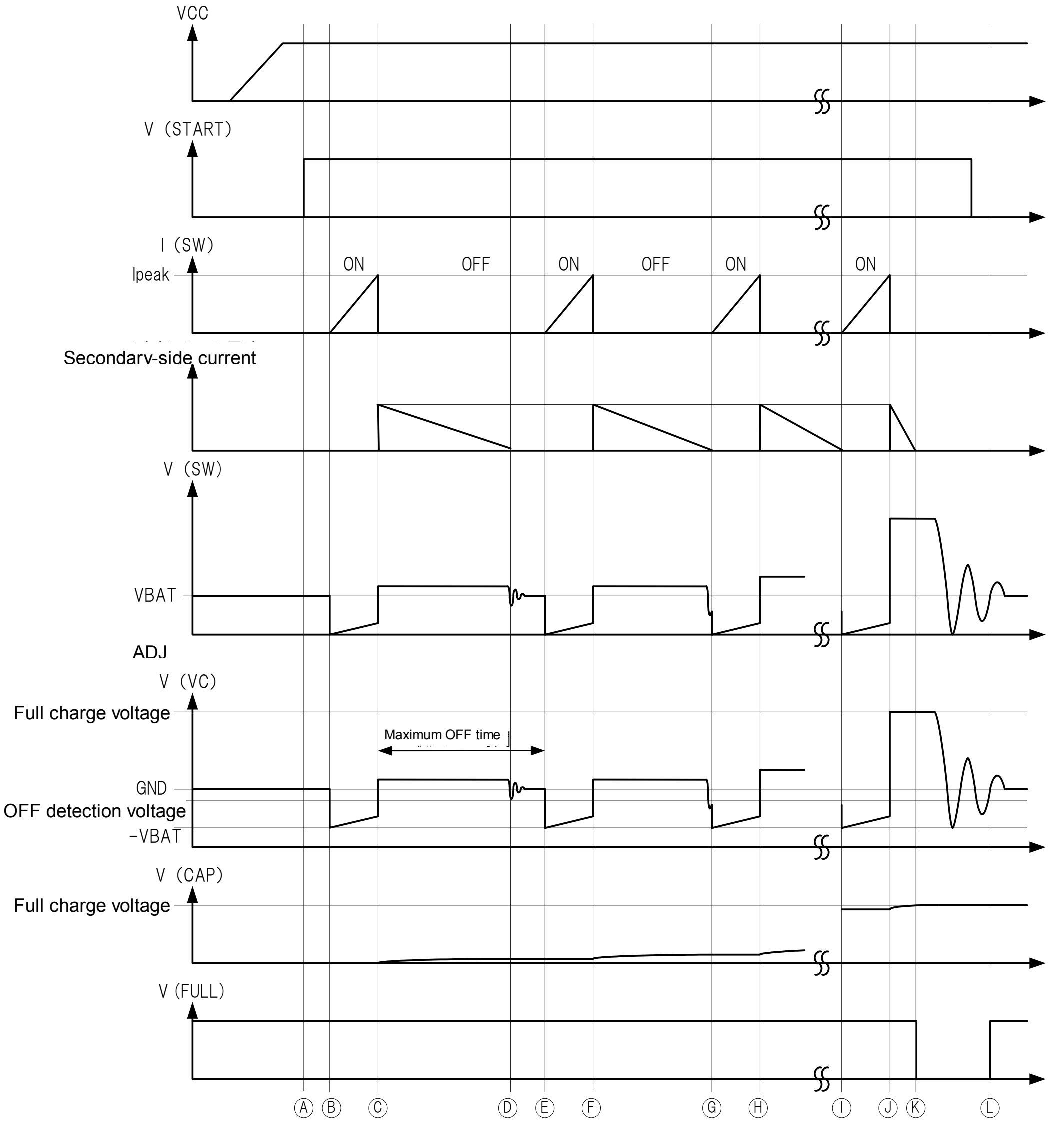


Fig 32. Timing Chart 2: Switching Operation

■Charging operation

The switching operation of this IC is shown in Fig.32 Timing Chart 2.
If the START pin is set to "H", all internal circuits are reset , the internal PowerTr is turned ON. (See Fig 32. Time Ⓐ→Ⓑ.) While the internal PowerTr is turned ON, a current is passed into the SW pin. When the current specified at the RADJ pin voltage is reached, the PowerTr is turned OFF. (See Time Ⓒ in Fig 32.) The time t_{ON} when the PowerTr is ON is indicated as follows:

$$t_{ON} = L_P\left(\frac{I_{PEAK}}{V_{BAT}}\right) \quad (1)$$

L_P: Transformer primary-side inductance value
I_{PEAK} : Primary-side peak current
V_{BAT} : Battery voltage

When the PowerTr is turned OFF, the magnetic energy stored in the transformer is released to the transformer secondary-side. While the energy is released, the VC pin voltage and the SW pin voltage indicated by the following equations are generated:

$$V(VC) = -(VBATV \cdot \mathrm{Np}) \cdot (R_{FB2} // R_{FB3}) \Big/ \left(R_{FB1} + (R_{FB2} // R_{FB3})\right) \quad (2)$$

$$V(VC) = (V_{cap} + V_{diode}) \cdot R_{FB2} \Big/ \left(R_{FB1} + R_{FB2}\right) \quad (3)$$

$$V(SW) = V_{cap} \Big/ N_P + V_{BAT} \quad (4)$$

V(VC) : Full charge detection voltage
V_{cap} : Main capacitor voltage
V_{diode}: Diode forward voltage
V(SW): SW pin voltage
N_P: S winding vs. P winding Winding ratio

When the energy release to the transformer secondary-side is completed, the VC pin voltage and the SW pin voltage produce resonance by the parasitic capacitance and the transformer inductance. (See Time Ⓓ in Fig 32.) At this time, unless the VC pin voltage becomes the GND voltage or less shown, the PowerTr remains OFF till the maximum OFF time is reached. (See Time Ⓔ in Fig 32.) As soon as the OFF detection voltage or less is reached, the PowerTr is turned ON. (See Time Ⓖ in Fig 32.) The time, t_{OFF} when the secondary-side releases energy is represented by the following equation:

$$t_{OFF} = L_S \left(\frac{I_{PEAK}}{V_{cap} \times N_P} \right) \quad (5)$$

L_S : Secondary-side inductance

After the above operations are repeated, if it is detected that the VC pin voltage reaches the full charge detection voltage, the FULL pin is set to "L" and the switching operation is stopped.

●**Timing Chart and Description of Operation(about protection function)**

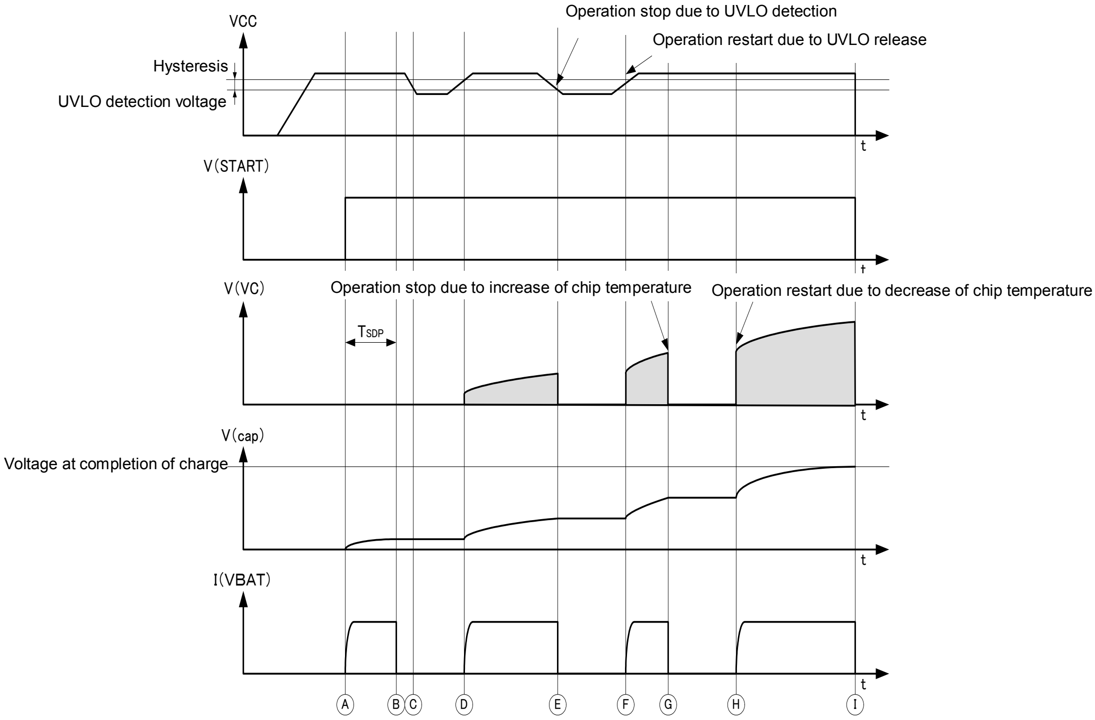


Fig 33. Timing Chart 3: Under Protective Circuit Operation

■Protection Functions

◆UVLO

If the VCC voltage is reduced to the UVLO detection voltage specified in the electrical characteristics or less, the UVLO protective circuit is activated and the charging operation temporarily stops. (See Time Ⓒ and Ⓔ in Fig 33.) After that, when the VCC voltage becomes the UVLO release voltage or more, the charging operation automatically restarts. (See Time Ⓓ and Ⓕ in Fig 33.)

This UVLO also works for the IGBT_OUT pin. If the VCC voltage becomes the UVLO detection voltage or less, the IGBT_OUT voltage is forced to be set to "L".

◆Thermal Shut Down (TSD)

It protects the IC against thermal runaway due to excessive temperature rise (Tj>175°C [TYP]). After detection, the charging operation temporarily stops (See time Ⓖ in Fig 33.), and when the chip temperature decreases, (Tj<150°C [TYP]), it automatically restarts. (See Time Ⓗ in Fig 33.)

◆VC pin short detection (SDP)

If the VC pin becomes the GND level due to any failure and the PowerTr repeats switching 2^{16}(=65536) times which is the SDP count number (TSDP) at the maximum OFF time, it is judged as an error and the charging operation is forced to be stopped. (See Time Ⓑ in Fig 33.) If the START pin is changed from "L" to "H" and the UVLO detection is released, it restarts.

◆Maximum OFF time

When it is detected that the internal PowerTr is left OFF for over the maximum OFF time specified in the electrical characteristics, the PowerTr is forced to be turned ON. This occurs unless the VC pin voltage becomes the OFF detection voltage specified in the electrical characteristics or less. (See Time Ⓓ in Fig 32.)

◆Maximum ON time

When it is detected that the internal PowerTr is left ON for over the maximum ON time specified in the electrical characteristics, it is judged as an error and the PowerTr is forced to be turned ON. This condition occurs when the SW pin is released or the current specified as the ADJ pin voltage does not pass. If the START pin is changed from "L" to "H" and the UVLO detection is released, it restarts.

●Setup for main capacitor full charge voltage

VC pin node is divided by between transformer Secondary node and Fast recovery diode anode side by resistor R_{FB1}, R_{FB2} and R_{FB3}. When VC pin voltage reach until full charge voltage as Fig.32 timing chart Ⓙ~Ⓚ,charge is stopped.

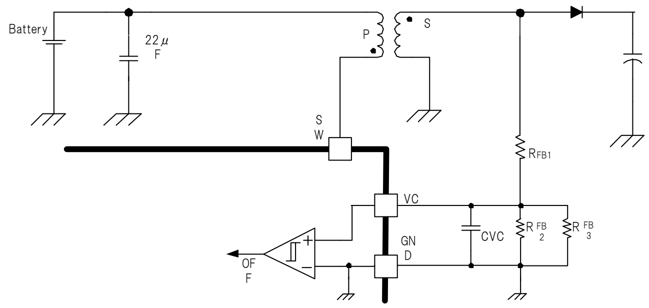


Fig 34. VC pin external parts

It is possible to setup by full charge detection voltage described electrical characteristics, and $R_{FB1.2.3}$ using below calculating formula.

$$VC(Vcap) = V(VC_{TH}) \cdot \frac{(R_{FB1} + (R_{FB2} // R_{FB3}))}{(R_{FB2} // R_{FB3})} - Vdiode \quad (6)$$

Vcap : main capacitor voltage
$V(VC_{TH})$: full detection voltage typical=1V
$R_{FB1、2、3}$: VC pin external resistor
Vdiode : diode VF voltage

VC pin need external capacitor to prevent from overshoot contributed parasitic capacitor of transformer secondary side and R_{FB1} pattern (See page 17「Caution about VC pin」 and Page18「How to prevent VC pin overshoot」.)
Parasitic capacitor increase overshoot, it is need to increase CVC external capacitor to prevent from overshoot ,VC pin voltage pulse width get thin by time constant $R_{FB1、2、3}$ and CVC. This cause increasing full detection voltage.

(example of setup)set up of main capacitor voltage=320V
R_{FB1}＝470kΩ(ROHM KTR18 、P=0.25W、absolute voltage=400V)
R_{FB2}＝2.0kΩ
R_{FB3}＝5.6kΩ

◆About R_{FB1}

R_{FB1} is applied high voltage as ΔV_{RFB1}=（main capacitor voltage＋FRD VF－full charge detection voltage）.
Be caution not to reach electrical power R_{FB1} calculated by I_{FB1} and ΔV_{RFB1}.

$$I_{RFB1} = (V_{cap} + V_{diode})/(R_{FB1} + (R_{FB2} // R_{FB3}) \quad (7)$$

$$P_{RFB1} > I_{RFB1} \cdot \Delta R_{FB1} \quad (8)$$

●Caution about VC pin

Transformer secondary side is switching high voltage, it cause VC pin overshoot with pattern of capacitance coupling of transformer secondary side to R_{FB1} High voltage pattern layout must be short and thin .and connect external capacitor between VC pin and GND to prevent VC pin overshoot.

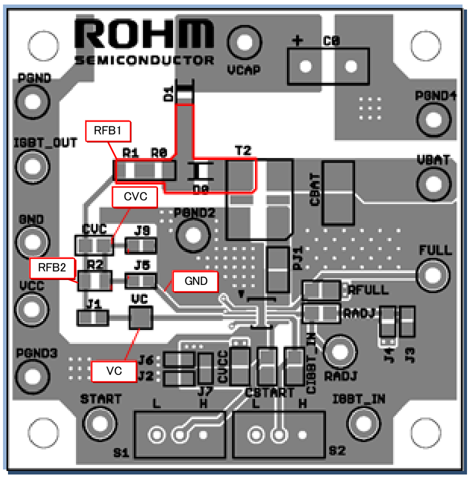


Fig35. PCB layout pattern of bourd

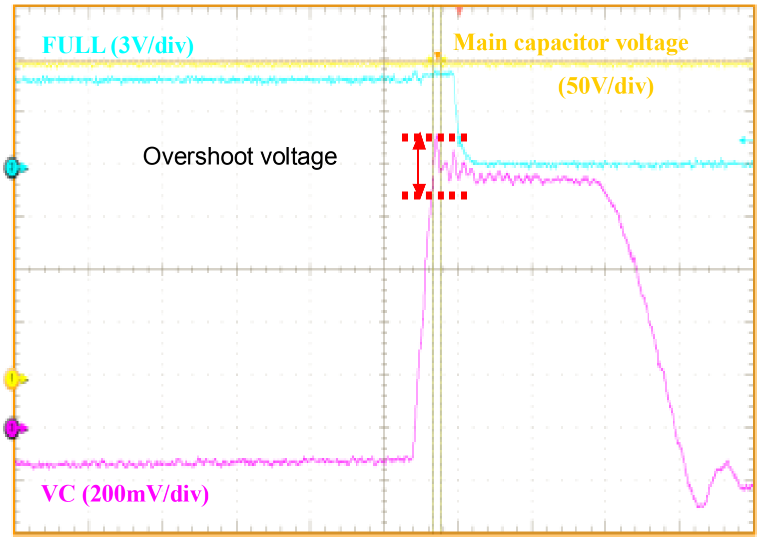


Fig36.Waveforme of VC pin overshoot voltage

● Countermeasure of VC pin overshoot

It is possible to simulate for VC pin over shoot as equivalent circuit schematic considered parasitic capacitor Cin from transformer secondary and R1(R_{FB1})as fig. 37.
If parasitic capacitor Cin is increased VC pin overshoot voltage is increased as figure 38.
It is possible to be down overshoot by increasing external capacitor CVC as figure41.
When VC pin voltage pulse width is thin, full charge detection comparator cannot response, VC full charge detection is increased as fig40.
If pulse width 100nsec, difference from DC detection and AC detection voltage over 0.5%.
It guarantee pulse response characteristics by 「full charger detection AC1」「full charger detection AC2」of electric character.

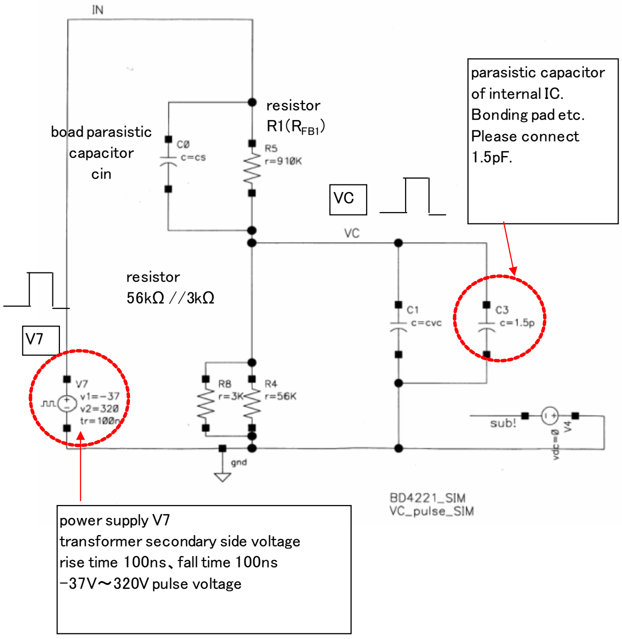


Fig37.egullvalent circuit schematic of external capacitor

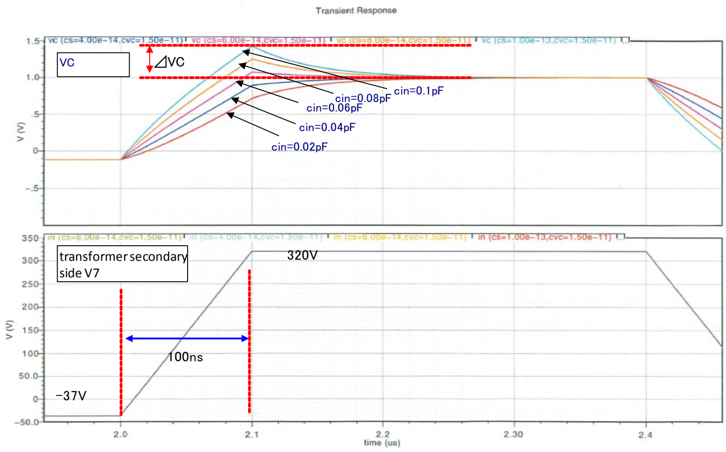


Fig38. Simulation result of VC pin overshoot with cin

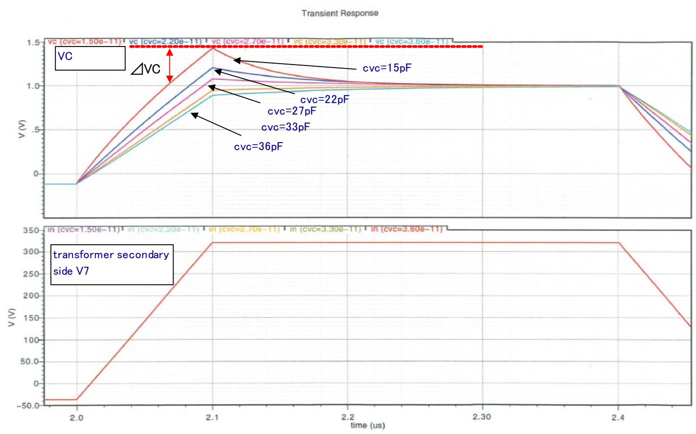


Fig39. Simulation result of VC pin overshoot with cvc

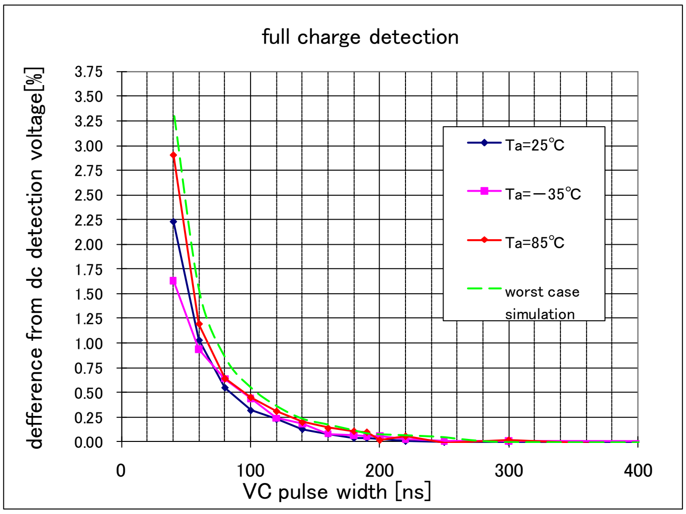
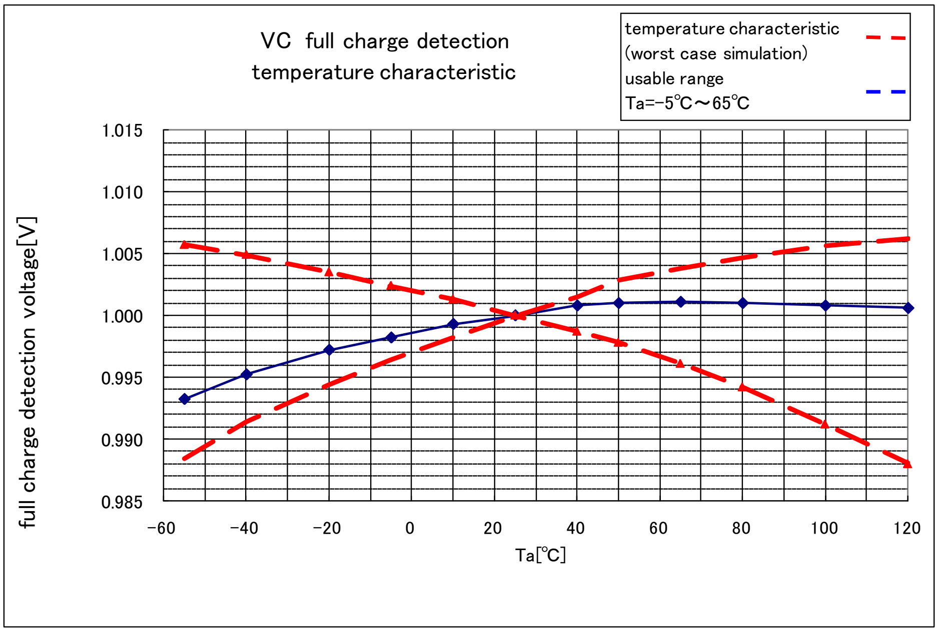


Fig40. Full charge detection voltage for VC pin ac pulse input

Full detection voltage temperature characteristics as figure 41.
Ta=-5℃～65℃,0.9961V～1.0038V(-0.39%～+0.38%).
Ta=-35℃～85℃,0.9920V～1.005V(-0.8%～+0.5%).



Typ=1.000V

Ta=-5℃～65℃
Min 0.9961V (-0.39%)
Max 1.0038V (+0.38%)

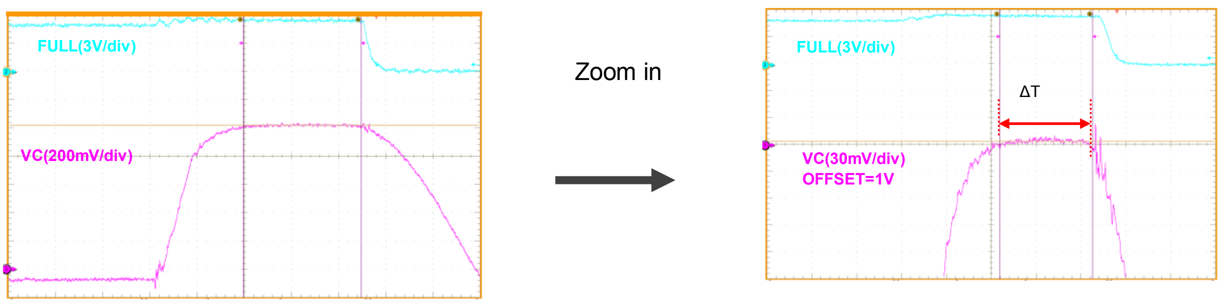
Ta=-35℃～85℃
Min 0.9920V(-0.8%)
Max 1.005V(+0.5%)

Fig41. full charge detection voltage temperature characteristics

●How to judge VC pulse voltage

Measure flat part of VC pin wave form figure 42 by oscilloscope when full charge detect.
Pulse width is 200nsec to use 「full charge detection AC1」Pulse width is 100nsec to use 「full charge detection AC2」
(Recommend to check with worst condition of VBAT is low, low temperature, and Ipeak is low)

(Example of VC pin wave form)
condition : Ta=25℃
VBAT=3.6V、Ipeak=0.92A
Lp=10μH、Ls=1.3mH
Np : Ns=14T : 143T
ΔT=210nsec



100nsec/div

100nsec/div

Fig42. Setup of VC pin voltage to flat

●How to set up primary side peak current.

BD4233NUX set up primary side peak current by adjustment of RADJ external resistor as below.

$$I_{PEAK\_DC} = (0.5/RADJ \times 23.8 \times 10^3) - 0.015)/(20.55 \times 10^3) \times 10^5 \quad [A]$$

I_{PEAK_DC} : primary-side DC current

Relation of RADJ external resistor and DC peak current as fig 43.

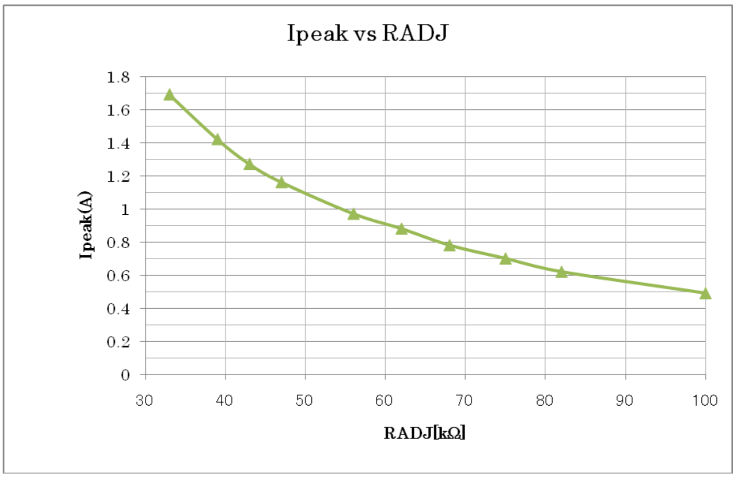


Fig43.. RADJ-primary peak current

For application using, Ipeak have difference between above graph and application Ipeak because of 200nsec delay. This delay time occur rising Ipeak as below formula(12).

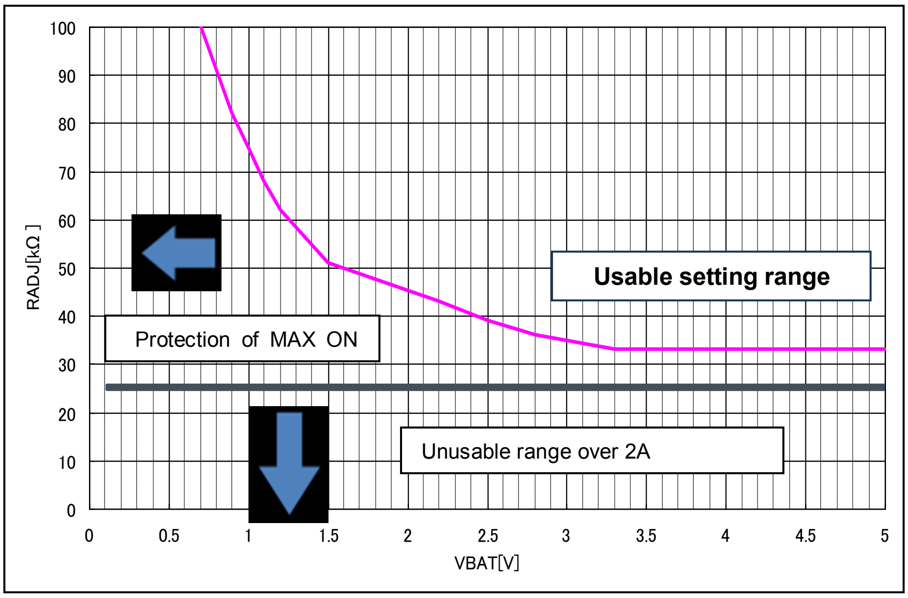
$$I_{PEAK\Delta} = \frac{VBAT}{L_P} T_{IPEAK} \qquad (12)$$

IpeakΔ : rising Ipeak by delay time
Lp : transformer primary side inductance
T_{IPEAK} : Ipeak delay time

●Usable setting of VBAT and RADJ pin external resistor

Please use with usable range of fig 44 at Ta=-35℃～85℃

When VBAT voltage is low, power transistor can't get Vds voltage by transformer primary side dc resistor and SW pin resistor. Ipeak current can't reach current detection, charge is stop by MAXON protection. (fig 44. Protection of MAXON)。 To change Ipeak current, RADJ external resistor is unusable under 33kΩbecause Ipeak current is over 2A that is SW pin absolute range(fig 44. Unusable range over 2A).



Conditions:
Ta=85℃
VCC=3.4V
VBAT=0V～5.0V
RADJ=33kΩ～100kΩ
transformer : TTRN-0530H
main capacitor : 80μF
FRD : CRF03（TOSHIBA）

Fig 44.

● **Selection of components externally connected**

■Transformer

In BD4233NUX, each parameter is set as follows:

◆Winding ratio

□Ratio of primary winding vs. secondary winding $N_{P(S+F)}$

Set the ratio $N_{P(S+F)}$ so that it does not exceed 48V which is the operating condition of the SW pin. The setting equation is as follows:

$$N_P \geq \frac{V_{cap} + V_{diode}}{48} \quad (11)$$

Check the surge voltage of the SW pin and change the winding ratio as required. A larger ratio than necessary results in a reduction of efficiency.

◆Secondly-side inductance value

In order to set the pulse width at OFF, when the full charge detection is conducted, to a certain value or more, set the secondly inductance value according to the following equation:

$$L_S \geq \frac{N_P \times 200 \times 10^{-9}}{I_{PEAK}} \cdot \frac{V(VC_{TH}) \cdot (R_{FB1} + R_{FB2})}{R_{FB2}} \quad (12)$$

L_S: Secondly-side inductance value
I_{PEAK}: Primary-side peak current
VC_{TH} : full charge detection voltage

■Diode

Note the following points when selecting a diode.

◆ Recovery time Trr

A diode with a long recovery time affects the charging time and efficiency. Due to dissipation associated with the reduction of efficiency, the surface temperature of the diode package rises, resulting in deterioration of diode characteristics. Therefore, select a diode with the shortest recovery time possible. (Recommendation: 100 nsec or less)

◆ Backward voltage

Select a diode with which the backward voltage rating does not exceed the reverse bias voltage applied to the diode. The reverse bias voltage applied to the diode is represented as follows:

$$V_{reverse} = V_{cap} \quad (13)$$

$V_{reverse}$: Diode backward voltage
V_{cap}: Main capacitor voltage

◆Forward current

Select a diode of which the forward current rating is determined allowing sufficient margin against the secondary peak current..

$$I_s = I_{PEAK} / N_P \quad (14)$$

$$I_{diode} > I_s \quad (15)$$

I_s: Secondary-side peak current
N_P: S winding vs. P winding Winding ratio
I_{PEAK}: Primary-side peak current
I_{diode}: Diode forward current rating

■Main capacitor

Select a main capacitor for which the withstand voltage should be determined allowing sufficient margin against the fill charge voltage.

■IGBT

The IGBT controls the trigger pulse that ionizes xenon gas from the photo flash lamp, and passes a heavy-current (100A or more) to the xenon tube to fire a flash. The IGBT driver drives the gate of IGBT to fire a flash. If the gate potential of IGBT falls rapidly, electric charge remains partly in the internal gate parasitic capacitance due to the IGBT internal gate parasitic resistance. As a result, the IGBT is not partly turned OFF, a current crowding occurs, and the IGBT is broken. Therefore, according to the IGBT specifications, connect the series resistance and pull-down resistance to the IGBT driver output.

●Layout Pattern of Board

The layout pattern of the board has very significant effects on the charging characteristics because it involves a high voltage and a heavy current. Therefore, it must be determined carefully.

・A heavy current is passed in the path of the bypass capacitor from the battery - the transformer primary-side - SW pin - PGND pin. Make the loop as short as possible, and secure low impedance and sufficient current capacity. Create an obtuse angle at a corner or increase the number of vias to prevent the overload of current to corners and vias.

・At the secondary-side of the transformer, switching operation is conducted at a high voltage. If the parasitic capacity of board (other transformers, current diodes, etc.) or the impedance is large, a large amount of energy is lost. Therefore, due care should be taken in the design. Make the high-voltage path as short and as small as possible. Secure sufficient distance between the board and the surrounding components and wiring to prevent a pressure burst.

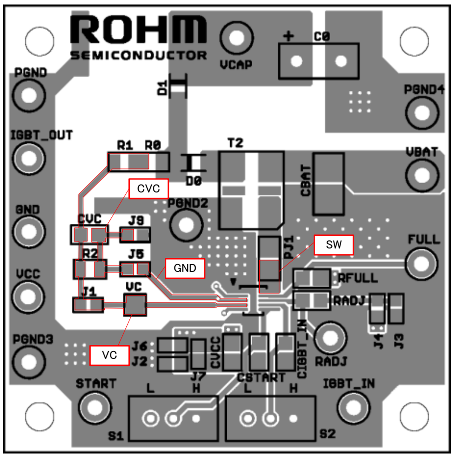
●Important Cautions on PCB Layout Pattern around Transformer

When the VC pin becomes open due to the PCB layout pattern around the transformer, the capacitive coupling between the SW pin and the VC pin may occur and noise superimposed on the VC pin voltage may lead to a false detection of the OFF detection circuit, resulting in no functioning of SDP protection.

Lay out the SW pin and the VC pin so that they are not close to each other to prevent the effect of switching noise at the boosting operation. In order to prevent a false detection error more securely, it is recommended that a capacitor of approx. 10 pF be connected to the VC pin relative to the GND.

See the recommended pattern as shown below.

［TOP　Layer］



［Bottom　Layer］

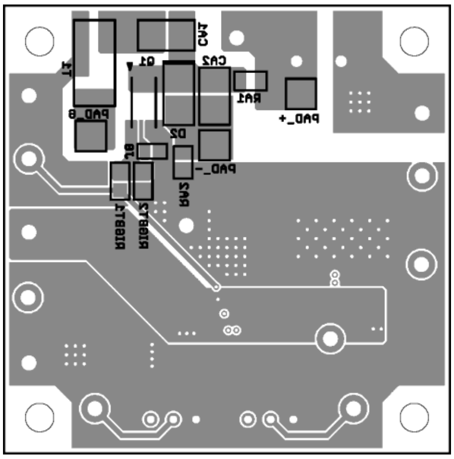


Fig 45. PCB Layout Pattern

●**Equivalent Circuit around Each Pin**

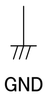
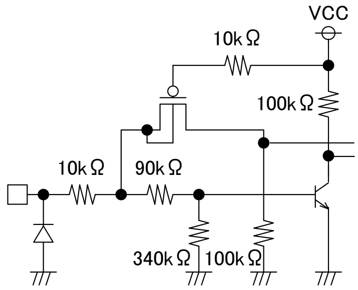
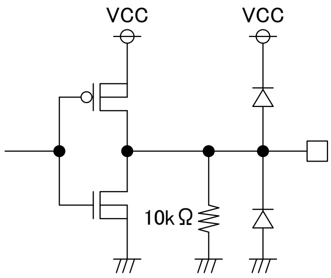
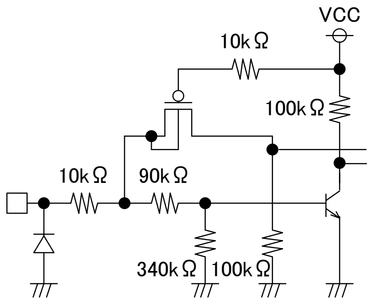
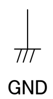
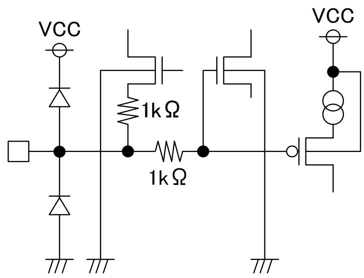
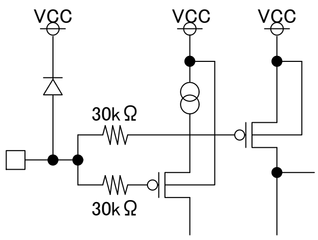
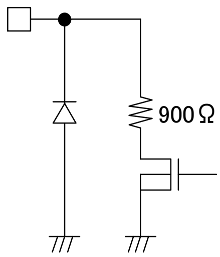
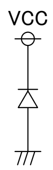
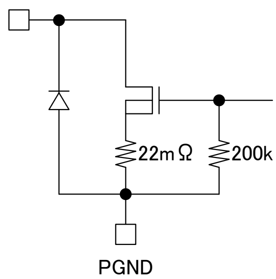
端子名	端子等価回路図	端子名	端子等価回路図
PGND		START	
IGBT_OUT		IGBT_IN	
GND		RADJ	
VC		FULL	
VCC		SW	

図 46. 端子等価回路図

●Precautions for Use

◆Absolute Maximum Rating

Although we pay due attention to the quality control of these products, the possibility of deterioration or destruction may exist when impressed voltage, operating temperature range, etc., exceed the absolute maximum rating. In addition, it is impossible to assume a destructive situation, such as short circuit mode, open circuit mode, etc. If a special mode exceeding the absolute maximum rating is assumed, please review to provide physical safety means such as fuse, etc.

◆GND Potential

Maintain the PGND pin potential at the minimum level under the operating conditions. Furthermore, maintain the pin except the VC pin at a voltage higher than the PGND pin voltage including an actual transient phenomenon.

The SW pin sometimes is charged by a negative voltage depending on the characteristics of the external transformer.

If any change in or damage of electrical characteristics is suspected due to the SW pin being charged by a negative voltage, it is recommended that a Schottky diode should be connected between the SW pin and the PGND pin.

◆Thermal Design

Work out the thermal design with sufficient margin taking power dissipation (Pd) at the actual operation condition into account.

◆Short Circuit between Pins and Incorrect Mounting

Sufficient caution is required for IC direction or displacement when installing IC on PCB. If IC is installed incorrectly, it may be broken. Also, the threat of destruction may exist in short circuits caused by foreign object invasion between outputs or output and GND of the power supply.

◆Common Impedance

When providing a power supply and GND wirings, give sufficient consideration to lowering common impedance, reducing ripple (i.e. making thick and short wiring, reduction ripple by LC, etc.) as much as possible.

◆Test mode

If any voltage higher than the VCC pin voltage is applied to the CHARGE_ON pin, FLASH_ON pin, IGBT_EN pin and I_PEAK pin, a test sequence is activated. Therefore, be sure to use at a voltage lower than the VCC pin voltage.

When you impress the voltage of 2/3 or more of the VCC terminal to RADJ terminal, and the voltage more than the VCC terminal voltage to IGBT-_IN terminal, START terminal, it enters the sequence for the test. Therefore, please use it to be sure to become a voltage below the above-mentioned voltage.

◆Protective circuit

The output circuit of this IC does not have a built-in protective circuit against abnormal conditions such as overcurrent protection. Therefore, if a load exceeding the package allowable power supply is applied or a short circuit occurs, the IC may be damaged. Before use, carefully design the circuit around the set.

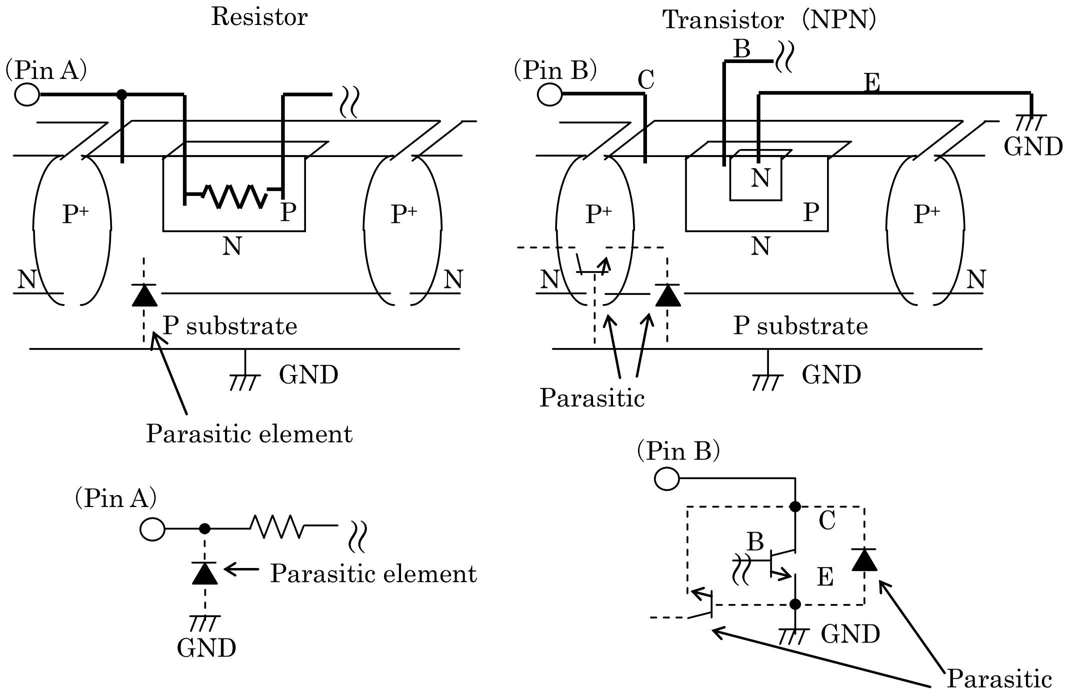


Fig 47. Other adjacent elements

◆IC Pin Input

This is the monolithic IC and has P^+ isolation and P substrate for element isolation between each element. By the P layer and N layer of each element, a P-N junction is formed and various parasitic elements are configured.

For example, in the case of a resistor and transistor being connected to a pin as shown in Fig.-47;

P-N junction operates as a parasitic diode when GND > (Pin A) in the case of the resistor, and when GND > (Pin B) in the case of the transistor (NPN)

Also, a parasitic NPN transistor operates by the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when GND > (Pin B).

The parasitic element consequently emerges through the potential relationship because of IC's structure. The parasitic element pulls interference out of the circuit which may be the cause of malfunction or destruction. Therefore, excessive caution is required to avoid operation of the parasitic element which is caused by applying voltage to an input pin lower than GND (P board), etc.

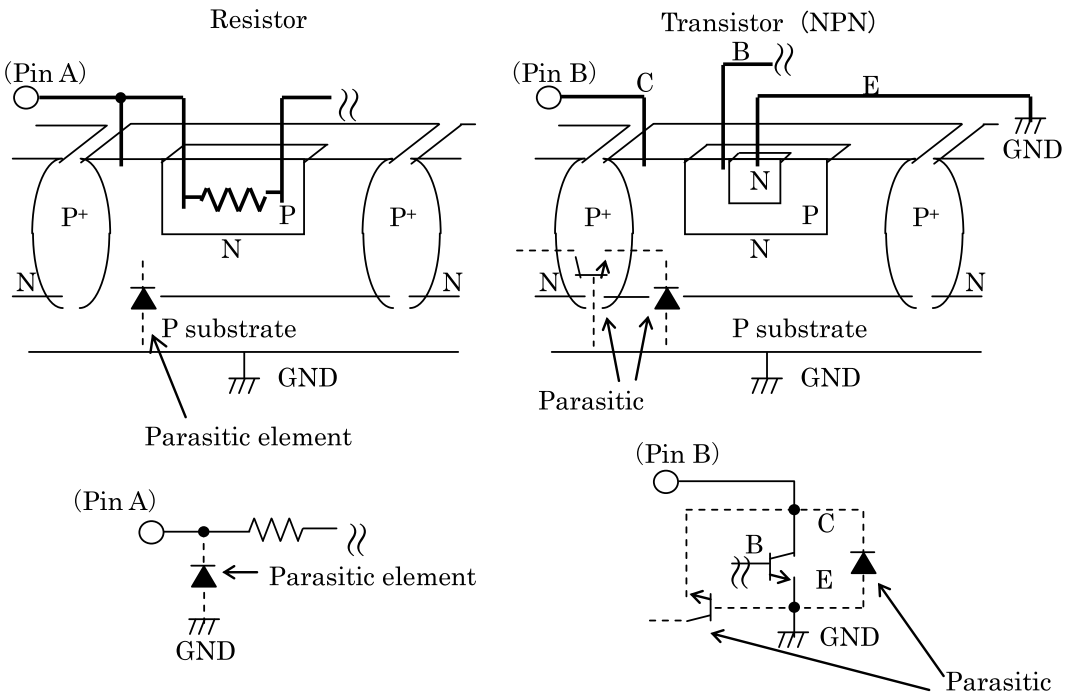


Fig 47. Other adjacent elements

◆VC pin minus voltage

When Power transistor is active, VC pin occur minus voltage with formula (2) at figure 32 between B to C page12.Please set up transformer ratio not to over absolute voltage -0.6V.

◆SW pin AC pulse input voltage

Please set up to transformer ratio not to reach 53V AC pulse of SW pin voltage.

◆SW pin minus voltage

When transformer secondary side current is discharged, discharge current is not zero at FRD recovery time. SW pin minus voltage is occurred by SW pin minus current that is occurred by transformer ratio. (fig 48 Ⓐ→Ⓑ、Ⓓ→Ⓔ、Ⓖ→Ⓗ、Ⓙ→Ⓚ)。
Please set up SW pin minus voltage is not under -1.5V because it might cause malfunction of IC.

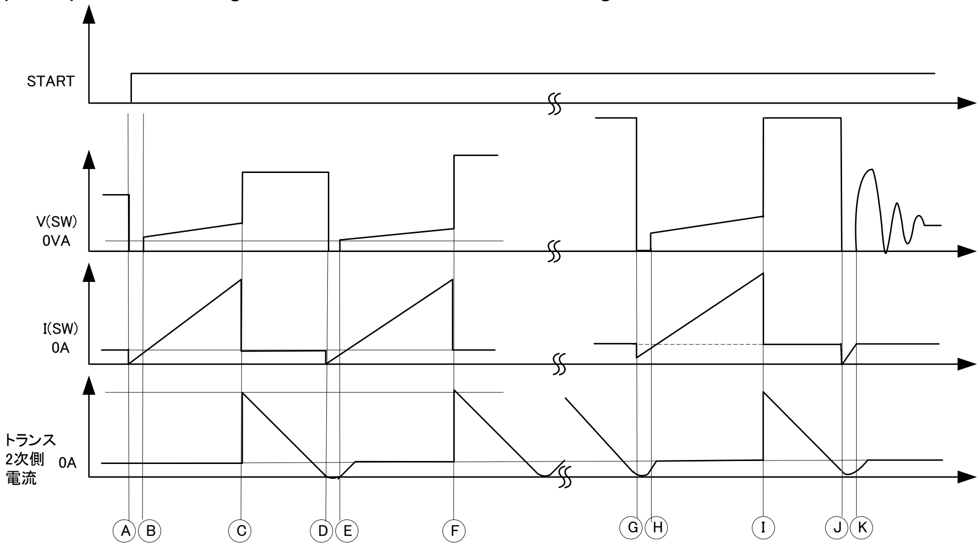


Fig 48. SW pin minus voltage

● **Heat reduction characteristics**

Reduced by 12.32 mW/°C at Ta=25°C or more

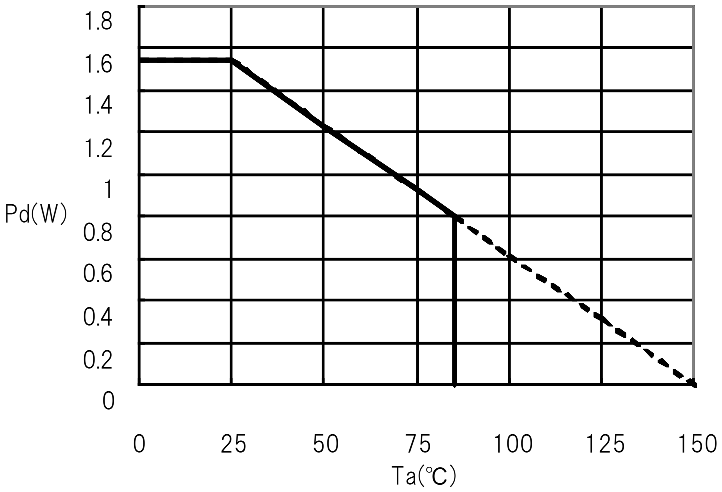
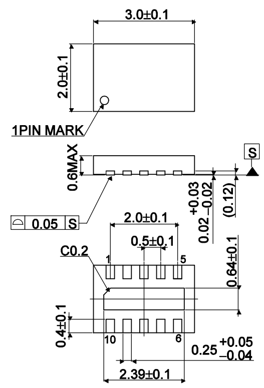


Fig 49. Heat reduction characteristics (VSON010V3020)

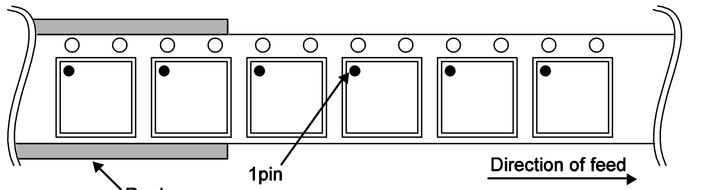
● Ordering part number

VSON010X3020



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Fig 50. Selecting a model name when ordering.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

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