Datasheet

Automotive PMIC Series for Processors, SoCs and Applications

8 Phase to 1 Phase Selectable Buck Controller with Maximum 160 A Output Current, 3.0 V to 5.5 V

BD96240MUF-C

General Description

BD96240MUF-C is a Switching Regulator that incorporates buck converter controller, LDO, A/D conversions, Power Monitor Unit and Control Unit for SoCs. BD96240MUF-C controls up to 8 Phase BD9634x (Driver MOSFET) series.

Features

- AEC-Q100 Qualified(Note 1)
- Safety Mechanism is Implemented to Support Functional Safety (ASIL-B)
- Up to 8 Phase Switching Regulator
- Programmable Output Voltage
- VID (Voltage Identification) Function
- Built-in Detection
  OVD (Over Voltage Detection), UVD (Under Voltage Detection), TW (Thermal Warning)
- Built-in Protection
  OVP (Over Voltage Protection), UVP (Under Voltage Protection), TSD (Thermal Shutdown)
- Built-in UVLO (Under Voltage Lockout), OVLO (Over Voltage Lockout)
- Digital Built-in Self-test (DBIST)
- Analog Built-in Self-test (ABIST)
- Pin Built-in Self-test for Critical Signal Pins (INTB and PGOOD)
- Built-in Mutual Monitoring of VREF and OSC
- Interrupt Output Pin (INTB)

(Note 1) Grade1

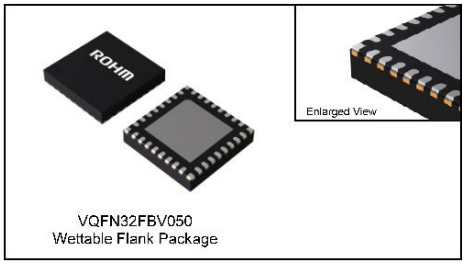
Applications

- In-vehicle Infotainment Systems (IVI Systems)
- Instrument Cluster Panel
- Advanced Driver Assistance Systems (ADAS)

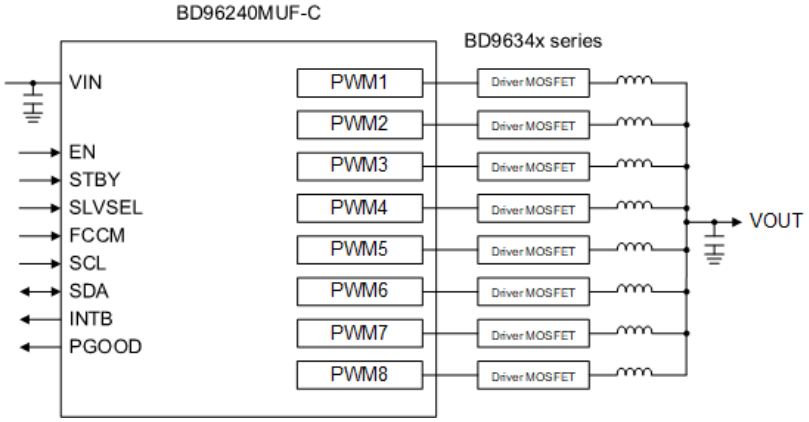
Key Specifications

- Input Voltage Range: 3.0 V to 5.5 V
- Output Voltage Range: 0.6 V to 2.0 V
- Switching Frequency: 2.25 MHz (Typ)
- Shutdown Current: 0 µA (Typ)
- Operating Ambient Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN32FBV050	5.0 mm x 5.0 mm x 1.0 mm



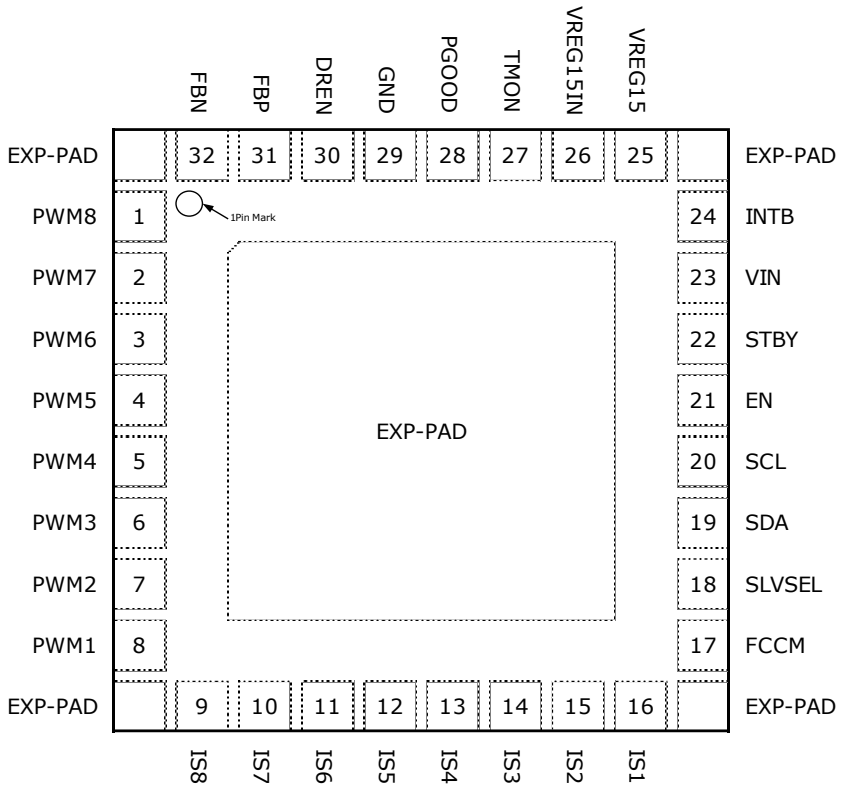
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration



(TOP VIEW)

Figure 1. Pin Configuration

Pin Descriptions

Table 1. Pin Descriptions

Pin No.	Pin Name	Function
1	PWM8	PWM output pin (Phase8).
2	PWM7	PWM output pin (Phase7).
3	PWM6	PWM output pin (Phase6).
4	PWM5	PWM output pin (Phase5).
5	PWM4	PWM output pin (Phase4).
6	PWM3	PWM output pin (Phase3).
7	PWM2	PWM output pin (Phase2).
8	PWM1	PWM output pin (Phase1).
9	IS8	Output current sense of Phase8 input pin.
10	IS7	Output current sense of Phase7 input pin.
11	IS6	Output current sense of Phase6 input pin.
12	IS5	Output current sense of Phase5 input pin.
13	IS4	Output current sense of Phase4 input pin.
14	IS3	Output current sense of Phase3 input pin.
15	IS2	Output current sense of Phase2 input pin.
16	IS1	Output current sense of Phase1 input pin.
17	FCCM	Forced CCM mode setting pin. (Low: PFM mode, High: Forced CCM mode)
18	SLVSEL	Target Address is selectable from 7 options. (See the chapter “Electrical Characteristics” or “Target Address Selection” for details).
19	SDA	I^2C interface data pin.
20	SCL	I^2C interface clock pin.
21	EN	Enable pin.
22	STBY	Stand-by request pin.
23	VIN	Power supply pin. (Note) VIN should be connected to power supply of BD9634X series (VIN and PVIN).
24	INTB	Interrupt pin to microcontroller or SoCs.
25	VREG15	Output of 1.536 V (LDO) internal regulator.
26	VREG15IN	Power supply pin. Connect to VREG15.
27	TMON	Input monitoring pin for BD9634x series die temperature. Connect to TEMP of BD9634x series.
28	PGOOD	PGOOD is an active high output signal. PGOOD indicates that output voltage is stable.
29	GND	Ground.
30	DREN	Enable pin for each BD9634x series. Connect to EN of BD9634x series.
31	FBP	Remote sense amplifier’s positive input.
32	FBN	Remote sense amplifier’s negative input.
-	EXP-PAD (CENTER)	Exposed Pad in the center. Connect to GND. EXP-PAD(CENTER) and EXP-PAD(CORNER) are shorted in the package.
-	EXP-PAD (CORNER)	Exposed Pad at the 4-corners. Connect to floating PCB pattern or GND PCB pattern. EXP-PAD(CENTER) and EXP-PAD(CORNER) are shorted in the package.

Block Diagram

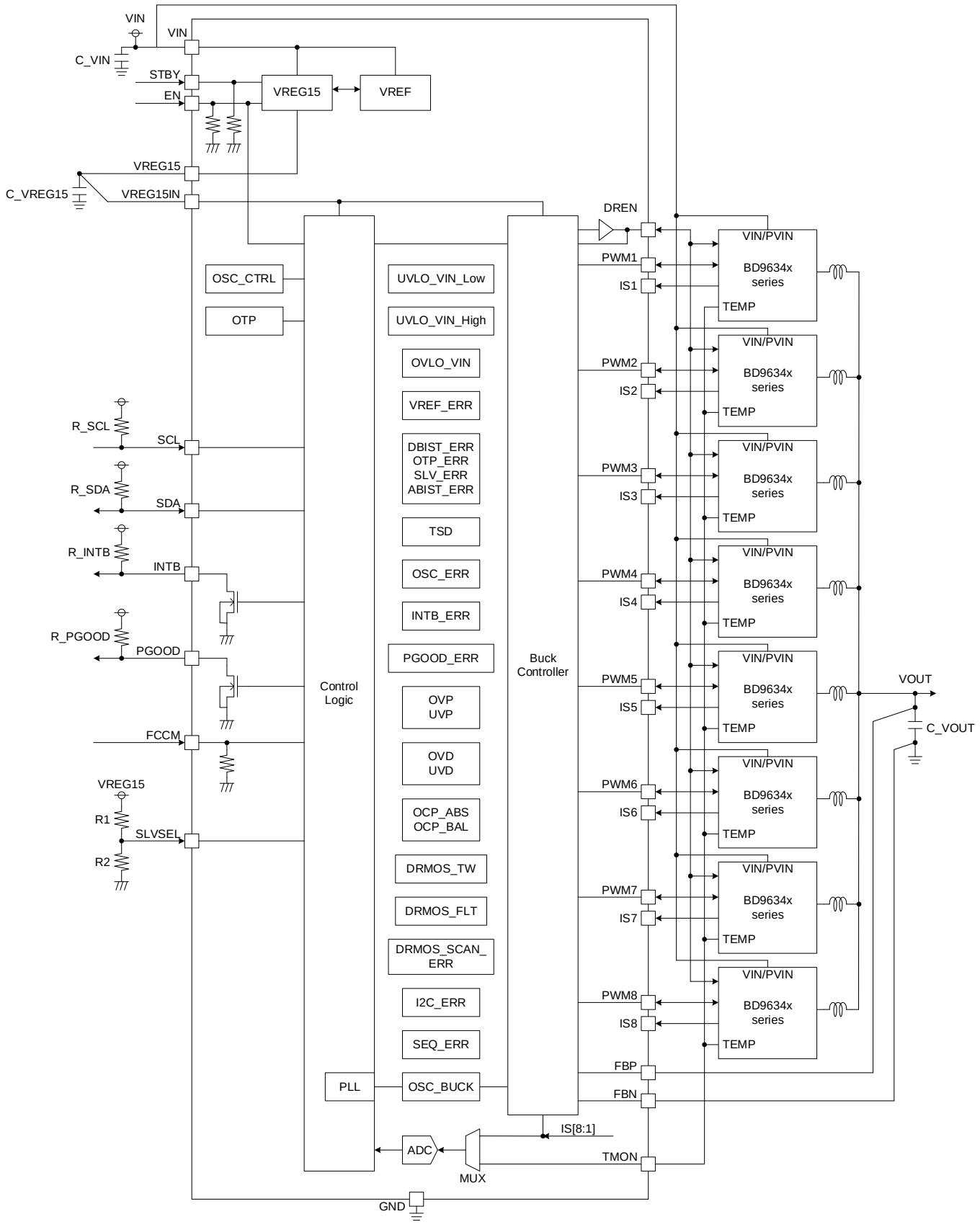


Figure 2. Block Diagram

Description of Blocks

1. General Blocks

Table 2. General Blocks Description

Name	Description
VREG15	VREG15 is the 1.536 V output voltage of the internal regulator.
VREF	VREF is the internal reference voltage for VREG15 monitoring.
OSC_CTRL	OSC_CTRL is the internal oscillator for Control Logic block.
OSC_BUCK	OSC_BUCK is the internal oscillator for Buck Controller.
Buck Controller	Buck Controller is the step-down regulator controller. Buck Controller controls up to 8 phases of BD9634x series.
Control Logic	Control Logic is the controller block of Protection, Sequence, Register setting and Interface.
IS	IS is BD9634x series current monitoring pin. Current of each Phase is adjusted by monitoring each IS to keep current balance between Phase x and Phase x+1.
TMON	TMON is BD9634x series temperature monitoring pin. The highest temperature among working phase of Driver MOSFET (BD9634x series) is monitored.
PLL	PLL is Phase Locked Loop. PLL synchronizes with the OSC_BUCK.

Description of Blocks – continued

2. Protection and Warning Blocks

Table 3. Protection and Warning Blocks Description

Name	Description	Buck Controller Behavior	State	INTB level	PGOOD level
UVLO_VIN_Low	Lower threshold Under Voltage Lockout for VIN.	Shutdown	-	-	Go to Low
UVLO_VIN_High	Higher threshold Under Voltage Lockout for VIN.	Shutdown	Go to UVLO_WAIT	-	Go to Low
OVLO_VIN	Over Voltage Lockout for VIN.	Shutdown	Go to UVLO_WAIT	Go to Low	Go to Low
VREF_ERR	Error when there is significant difference between VREG15 and VREF.	Shutdown	Go to ERROR	Go to Low	Go to Low
DBIST_ERR	Error of Digital Built-in Self-test.	Shutdown	Go to ERROR	Go to Low	Keep Low
OTP_ERR	Error of Digital Built-in Self-test for OTP block or ECC for OTP data.	Shutdown	Go to ERROR	Go to Low	Keep Low
SLV_ERR	Target address setting error which is asserted when target address which is set by resistor divider is not the same value in 3 consecutive times.	Shutdown	Go to ERROR	Go to Low	Keep Low
ABIST_ERR	Error of Analog Built-in Self-test.	Shutdown	Go to ERROR	Go to Low	Keep Low
TSD	Thermal Shutdown Protection. When Tj reaches the threshold temperature, TSD circuit controls State to ERROR.	Shutdown	Go to ERROR	Go to Low	Go to Low
OSC_ERR	Monitoring the OSC_CTRL and OSC_BUCK while EN = H.	Shutdown	Go to ERROR	Go to Low	Go to Low
INTB_ERR	INTB pin response error.	Shutdown	Go to ERROR	Go to Low	Go to Low
PGOOD_ERR	PGOOD pin response error.	Shutdown	Go to ERROR	Go to Low	Go to Low
OVP	Over Voltage Protection.	Shutdown	Go to ERROR	Go to Low	Go to Low
UVP	Under Voltage Protection.	Shutdown	Go to ERROR	Go to Low	Go to Low
OVD	Over Voltage Detection.	Continue operating	Active	Go to Low	Go to Low
UVD	Under Voltage Detection.	Continue operating	Active	Go to Low	Go to Low
OCP_ABS	Over Current Protection of each phase.	Continue operating	Active	Go to Low	Keep High
OCP_BAL	Current difference protection between the average current and each phase.	Continue operating	Active	Go to Low	Keep High
DRMOS_TW	Thermal Warning (140 °C). (Monitoring TEMP (BD9634x series) voltage.)	Continue operating	Active	Go to Low	Keep High
DRMOS_FLT	Driver MOSFET fault (TSD, HOCP, LOCP, NOCP, DBIST_ERR or OTP_ERROR).	Shutdown	Go to ERROR	Go to Low	Go to Low
DRMOS_SCAN_ERR	Error of Driver MOSFET configuration check and connection check.	Shutdown	Go to ERROR	Go to Low	Keep Low
I^2C_ERR	I^2C read/write error which is detected by CRC.	Continue operating	Active	Go to Low	Keep High
SEQ_ERR	Shutdown error with Time-out (1 s) execution	Shutdown	Go to ERROR	Go to Low	Go to Low

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage 1	VIN	-0.3 to +6.0	V
Input Voltage 2	VREG15IN	-0.3 to +2.0	V
Input Voltage 3	IS1, IS2, IS3, IS4, IS5, IS6, IS7, IS8, FBP, TMON, SLVSEL, FCCM, EN, STBY	-0.3 to V_{IN} +0.3	V
Input Voltage 4	FBN	-0.3 to +0.3	V
Input Voltage 5	SDA, SCL	-0.3 to +6.0	V
Output Voltage 1	VREG15	-0.3 to +2.0	V
Output Voltage 2	PWM1, PWM2, PWM3, PWM4, PWM5, PWM6, PWM7, PWM8, INTB, PGOOD, DREN	-0.3 to V_{IN} +0.3	V
Output Pin Current Low 1	INTB, PGOOD	-3.0	mA
Output Pin Current Low 2	SDA	-20.0	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150*(Note 1)*	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1): Operation is not guaranteed.

Thermal Resistance *(Note 1)*

Table 5. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN32FBV050				
Junction to Ambient	θ_{JA}	111.6	42.8	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23	17	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mm

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mm	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Parameter	Symbol	PIN	Min	Typ	Max	Unit
Power Supply Voltage	V_{OPR1}	VIN*(Note 1)*	3.0	5.0	5.5	V
Operating Ambient Temperature	Ta	-	-40	+25	+125	°C
Operating Junction Temperature	Tj	-	-40	+25	+150	°C

(Note 1) VIN should be connected to power supply of BD9634X series (VIN and PVIN).

Electrical Characteristics

Table 7. Electrical Characteristics (Unless otherwise specified VIN = 5 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[General]						
VIN Total Current 1	I_{VIN1}	-	0	10	µA	Tj = 25 °C, I_{VIN} V_{EN} = Low, V_{STBY} = Low
VIN Total Current 2	I_{VIN2}	-	0.9	1.5	mA	I_{VIN} and $I_{VREG15IN}$ V_{EN} = Low, V_{STBY} = High
VIN Total Current 3	I_{VIN3}	-	3.4	5.5	mA	I_{VIN} and $I_{VREG15IN}$ V_{EN} = High, V_{STBY} = High
UVLO_VIN_Low Threshold Voltage	$V_{UVLOVINL}$	2.21	2.30	2.39	V	V_{IN}: Sweep down
UVLO_VIN_Low Hysteresis Voltage	$V_{UVLOVINL\_HYS}$	-	47	-	mV	V_{IN}: Sweep up
UVLO_VIN_High Threshold Voltage	$V_{UVLOVINH}$	2.50	2.55	2.60	V	V_{IN}: Sweep down
UVLO_VIN_High Hysteresis Voltage	$V_{UVLOVINH\_HYS}$	-	70	-	mV	V_{IN}: Sweep up
OVLO_VIN Threshold Voltage	$V_{OVLOVIN}$	5.55	5.72	5.78	V	V_{IN}: Sweep up
OVLO_VIN Hysteresis Voltage	$V_{OVLOVIN\_HYS}$	-	80	-	mV	V_{IN}: Sweep down
[LDO (1.536 V)]						
LDO Output Voltage	V_{REG15}	1.505	1.536	1.567	V	
[Buck Controller]						
Feedback Voltage	V_{FBP}	0.742	0.750	0.758	V	Initial boot voltage
Programmable Output Voltage Range	V_{FBP_RNG}	0.6	-	2.0	V	Select output voltage (10 mV/bit) by Address 0x23
Offset Voltage Range	V_{FBP_OFS}	-317.5	0	+317.5	mV	Select offset voltage (2.5 mV/bit) by Address 0x24
Soft Start Time	t_{SS}	675	750	825	µs	V_{FBP} = 0.75 V
Slew Rate	SR	0.56	0.63	0.70	mV/µs	Dynamic Voltage Shift
Over Voltage Protection	V_{OVP}	+100	+125	+150	mV	V_{FBP} = 0.75 V
Under Voltage Protection	V_{UVP}	-150	-125	-100	mV	V_{FBP} = 0.75 V
Over Voltage Detection	V_{OVD}	+50	+75	+100	mV	V_{FBP} = 0.75 V
Under Voltage Detection	V_{UVD}	-100	-75	-50	mV	V_{FBP} = 0.75 V
Current Balance Accuracy*(Note 1)*	$I_{CURRENTBAL}$	-2	0	+2	A	Tj = 25 °C I_{OUT} per phase > 10 A
Phase Over Current Protection	I_{OCPABS}	30	-	-	A	
Monitoring Phase Current Against Average Current	I_{OCPBAL}	-4	-	+4	A	Phase current - Average current
Shutdown Detecting Voltage	$V_{SHUTDOWN}$	0.1	0.2	0.3	V	V_{FBP}: Sweep down
Switching Frequency	f_{SW}	2.025	2.250	2.475	MHz	
FBP Discharge ON Resistance 1	R_{ONDIS1}	4	8	16	Ω	V_{IN} = 5.0 V
FBP Discharge ON Resistance 2	R_{ONDIS2}	5	10	20	Ω	V_{IN} = 3.3 V
FBN Input Voltage Range	V_{FBN}	-0.1	0	+0.1	V	

(Note 1) Current Balance Accuracy is affected by mounting condition of BD96340MFF-C and PCB layout around BD96340MFF-C.

Electrical Characteristics – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
[Logic Input Voltage] (EN)						
Input Voltage Low EN	V_{ILEN}	-0.3	-	+0.4	V	
Input Voltage High EN	V_{IHEN}	1.4	-	V_{IN}+0.3	V	
Pull down Resistance EN	R_{DOWNEN}	-	100	-	kΩ	
[Logic Input Voltage] (STBY)						
Input Voltage Low STBY	V_{ILSTBY}	-0.3	-	+0.4	V	
Input Voltage High STBY	V_{IHSTBY}	1.4	-	V_{IN}+0.3	V	
Pull down Resistance STBY	$R_{DOWNSTBY}$	-	100	-	kΩ	
[Logic Input Voltage] (FCCM)						
Input Voltage Low FCCM	V_{ILFCCM}	-0.3	-	+0.4	V	
Input Voltage High FCCM	V_{IHFCCM}	1.4	-	V_{IN}+0.3	V	
Pull down Resistance FCCM	$R_{DOWNFCCM}$	-	100	-	kΩ	
[Logic Input Voltage] (SLVSEL)						
SLVSEL Input Voltage 1	$V_{SLVSEL1}$	3/16 x V_{REG15} -0.05	3/16 x V_{REG15}	3/16 x V_{REG15} +0.05	V	Target Address: 0x31
SLVSEL Input Voltage 2	$V_{SLVSEL2}$	5/16 x V_{REG15} -0.05	5/16 x V_{REG15}	5/16 x V_{REG15} +0.05	V	Target Address: 0x32
SLVSEL Input Voltage 3	$V_{SLVSEL3}$	7/16 x V_{REG15} -0.05	7/16 x V_{REG15}	7/16 x V_{REG15} +0.05	V	Target Address: 0x33
SLVSEL Input Voltage 4	$V_{SLVSEL4}$	9/16 x V_{REG15} -0.05	9/16 x V_{REG15}	9/16 x V_{REG15} +0.05	V	Target Address: 0x34
SLVSEL Input Voltage 5	$V_{SLVSEL5}$	11/16 x V_{REG15} -0.05	11/16 x V_{REG15}	11/16 x V_{REG15} +0.05	V	Target Address: 0x35
SLVSEL Input Voltage 6	$V_{SLVSEL6}$	13/16 x V_{REG15} -0.05	13/16 x V_{REG15}	13/16 x V_{REG15} +0.05	V	Target Address: 0x36
SLVSEL Input Voltage 7	$V_{SLVSEL7}$	V_{REG15} -0.05	V_{REG15}	-	V	Target Address: 0x37
Input Current SLVSEL	$I_{LEAKSLVSEL}$	-	0	1	µA	
[Logic Output Voltage Low] (INTB)						
Output Voltage Low INTB	V_{OLINTB}	-	-	0.7	V	I_{LOAD} = -3 mA
Leak Current INTB	$I_{LEAKINTB}$	-	0	1	µA	
[Logic Output Voltage Low] (PGOOD)						
Output Voltage Low PGOOD	$V_{OLPGOOD}$	-	-	0.7	V	I_{LOAD} = -3 mA
Leak Current PGOOD	$I_{LEAKPGOOD}$	-	0	1	µA	

Typical Performance Curves

Unless otherwise specified: VIN = 5.0 V, Ta = 25 °C, I_{OUT} = 0 A

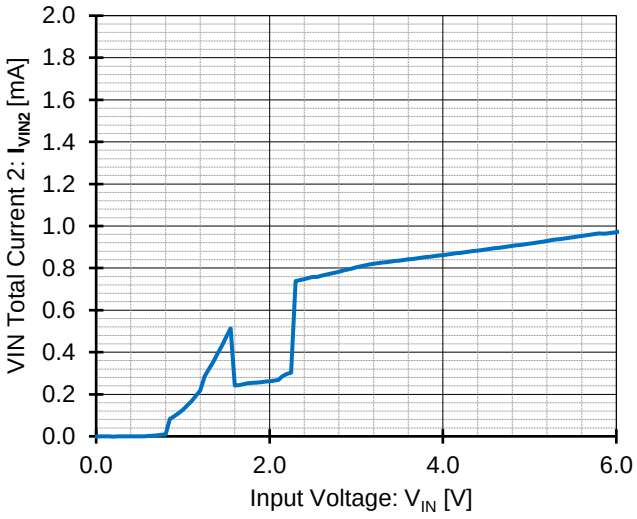


Figure 3. VIN Total Current 2 vs Input Voltage 1 (Ta = 25 °C)

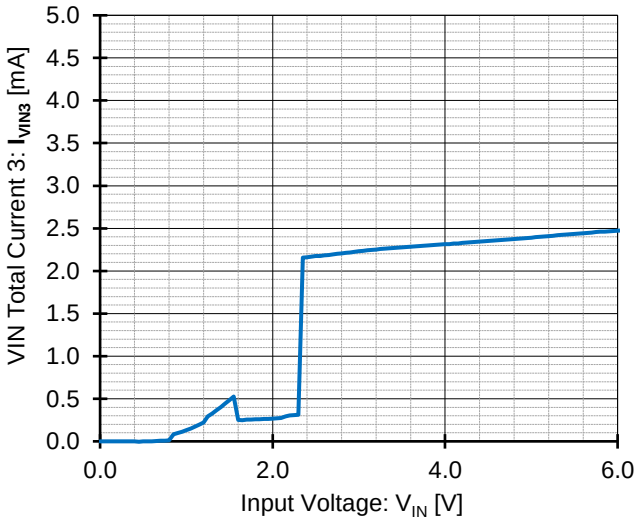


Figure 4. VIN Total Current 3 vs Input Voltage 1 (Ta = 25 °C)

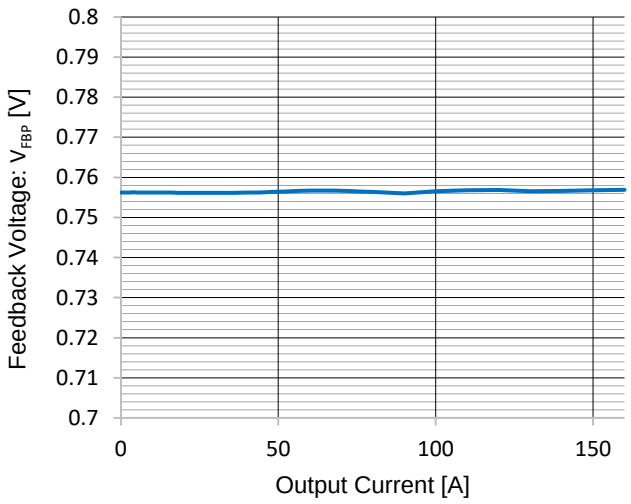


Figure 5. Feedback Voltage (8phase) vs Output Current (VIN = 5.0 V, Ta = 25 °C)

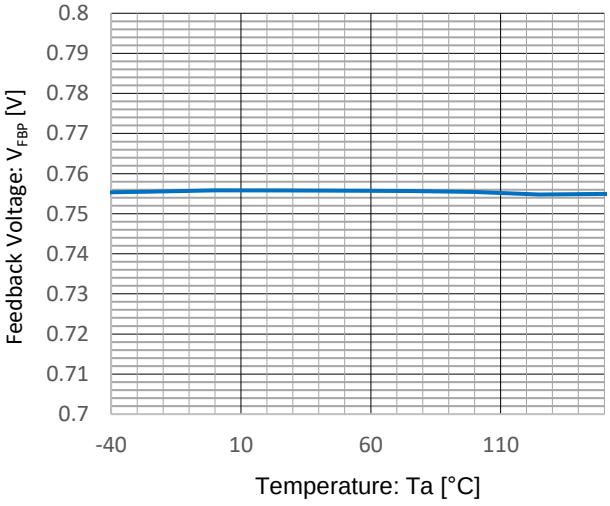


Figure 6. Feedback Voltage (8phase) vs Temperature (VIN = 5.0 V)

Typical Performance Curves - continued

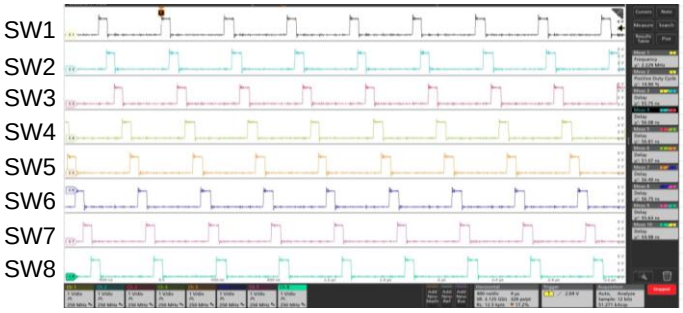


Figure 7. BD9634x series SW Pin Switching Waveform(8phase) (VIN = 5.0 V, Ta = 25 °C)

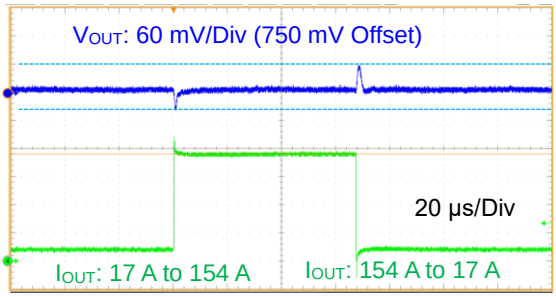


Figure 8. Load Transient (8phase) (VIN = 5.0 V, Ta = 25 °C)

Typical Performance Curves – continued

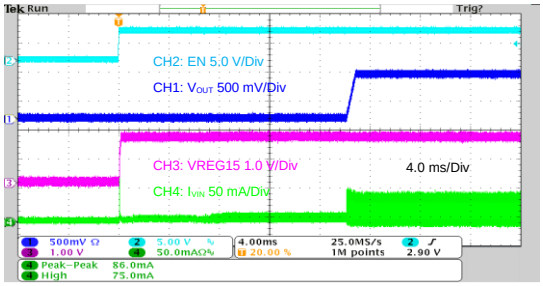


Figure 9. Soft Start Waveform (VIN = 5.0 V, Ta = 25 °C)

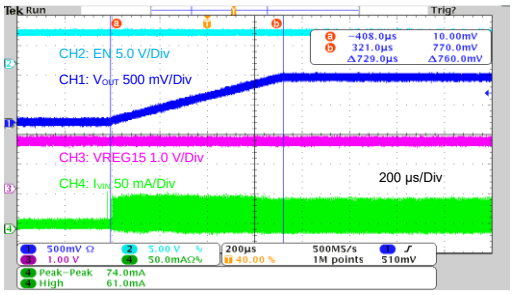


Figure 10. Soft Start Waveform(Zoom Up)
(VIN = 5.0 V, Ta = 25 °C)

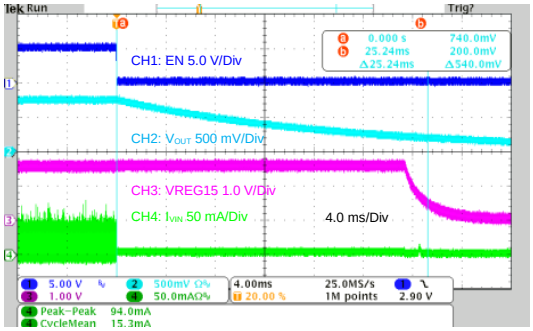


Figure 11. Shutdown Waveform
(VIN = 5.0 V, Ta = 25 °C)

Typical Performance Curves – continued

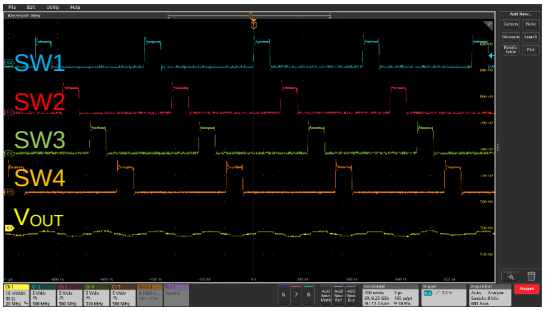


Figure 12. BD9634x series SW Pin and Ripple Voltage(4phase) (VIN = 5.0 V, Ta = 25 °C)

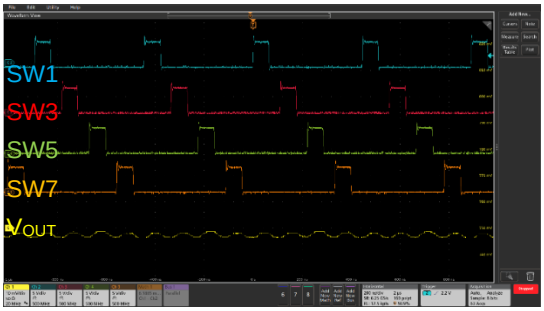


Figure 13. BD9634x series SW Pin and Ripple Voltage(8phase)1/2 (VIN = 5.0 V, Ta = 25 °C)

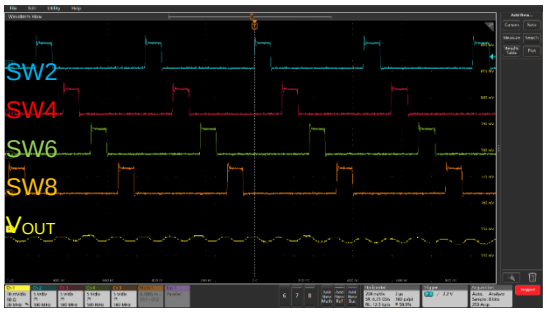


Figure 14. BD9634x series SW Pin and Ripple Voltage(8phase)2/2 (VIN = 5.0 V, Ta = 25 °C)

Typical Performance Curves – continued

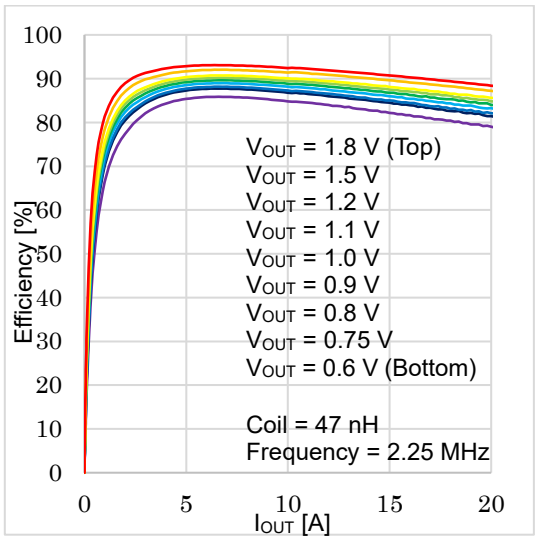


Figure 15. Efficiency vs I_{OUT}
(w/o DCR loss)(VIN = 3.3 V, Ta = 25 °C)

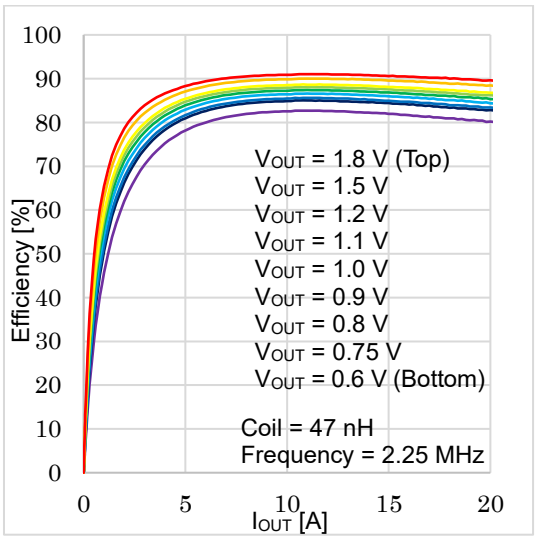


Figure 16. Efficiency vs I_{OUT}
(w/o DCR loss)(VIN = 5 V, Ta = 25 °C)

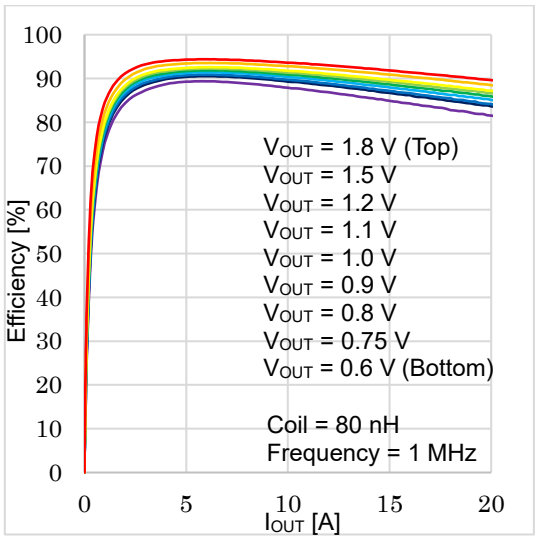


Figure 17. Efficiency vs I_{OUT}
(w/o DCR loss)(VIN = 3.3 V, Ta = 25 °C)

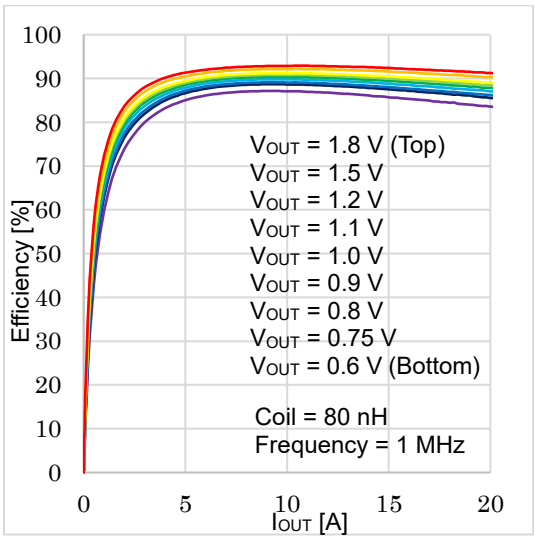


Figure 18. Efficiency vs I_{OUT}
(w/o DCR loss)(VIN = 5 V, Ta = 25 °C)

State Transition Diagram

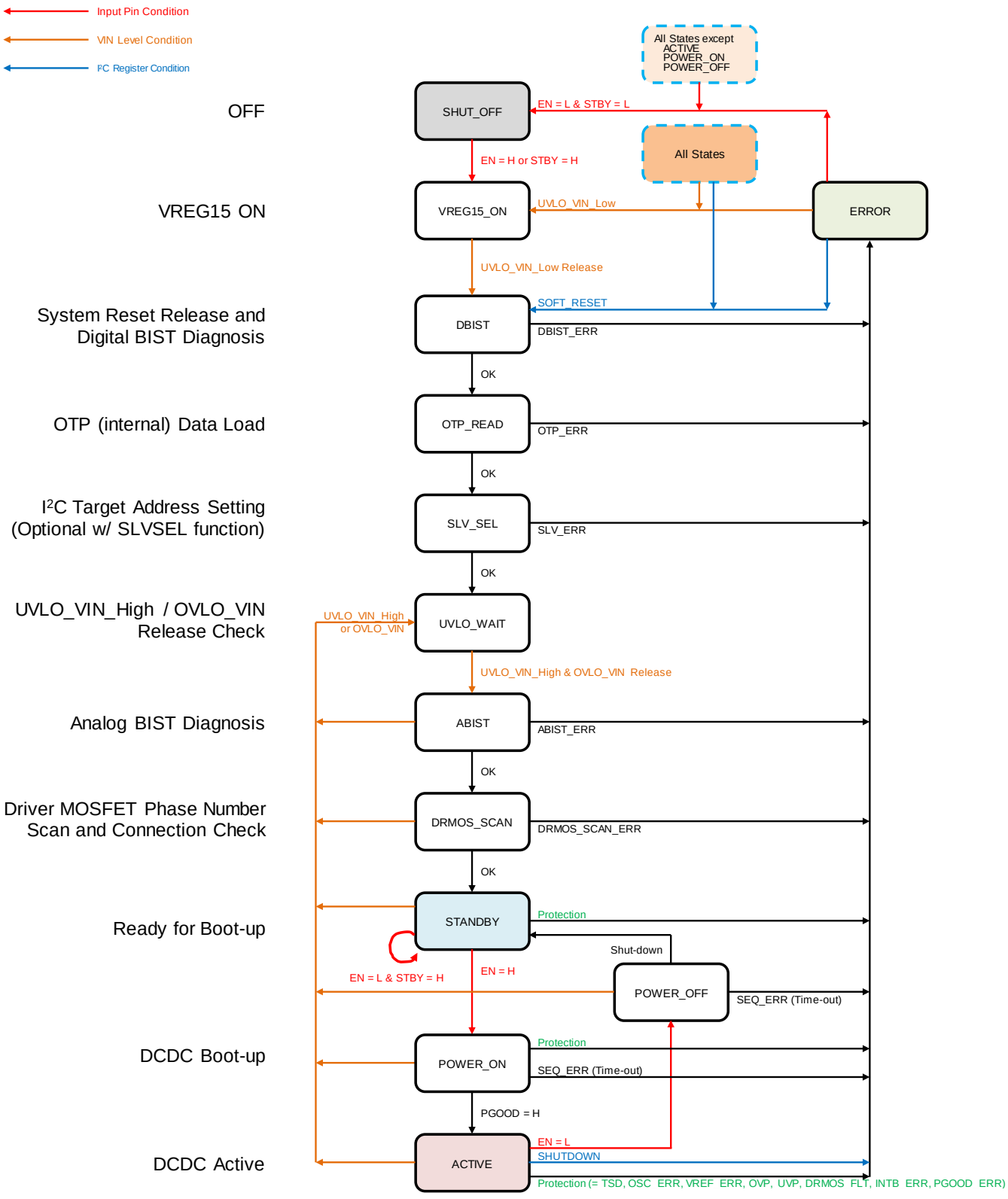


Figure 19. State Transition Diagram

Timing Chart

1. EN ON (STBY OFF) Sequence

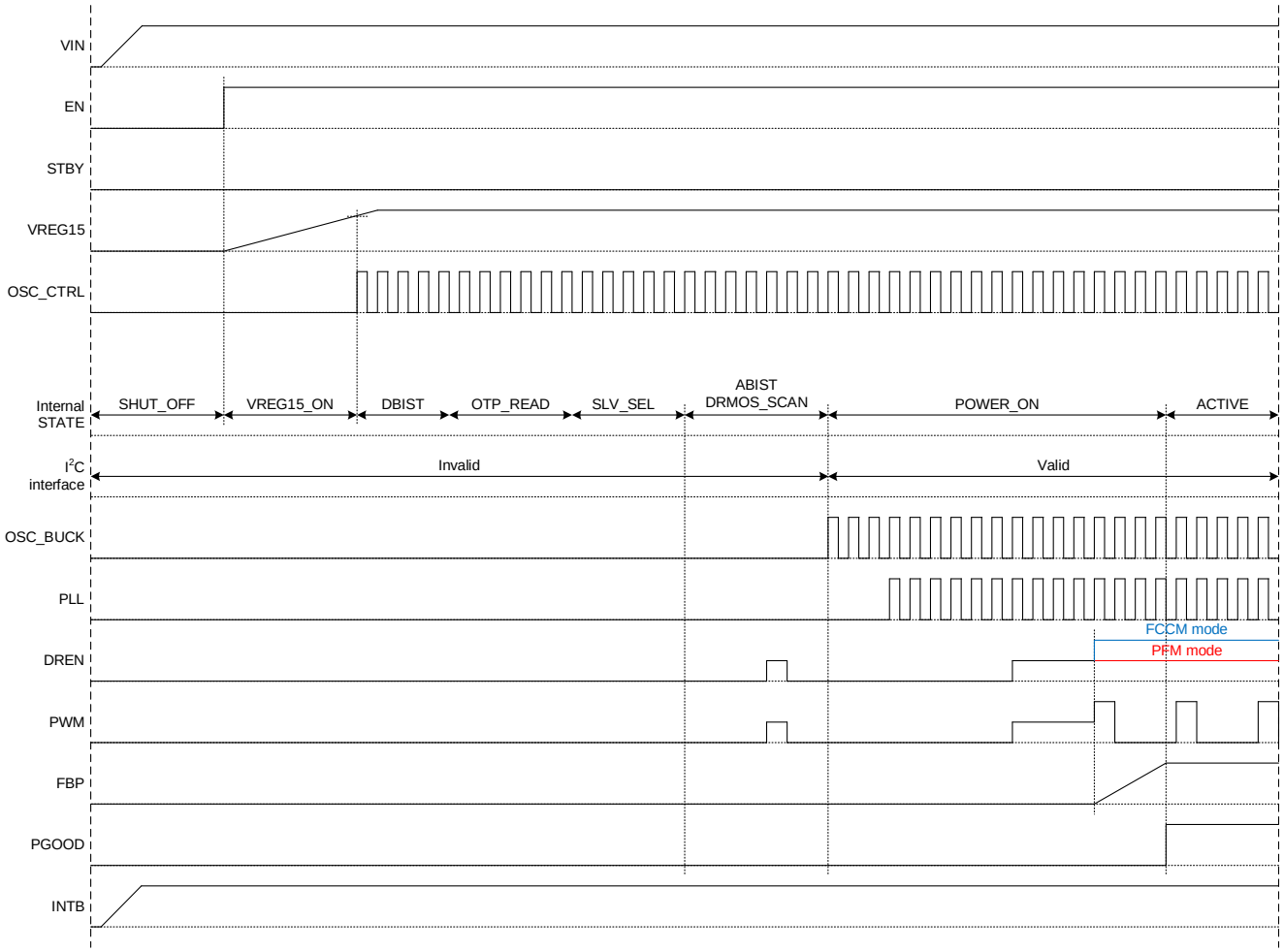


Figure 20. EN ON (STBY OFF) Sequence Timing Chart

Timing Chart – continued

2. STBY ON, EN ON Sequence

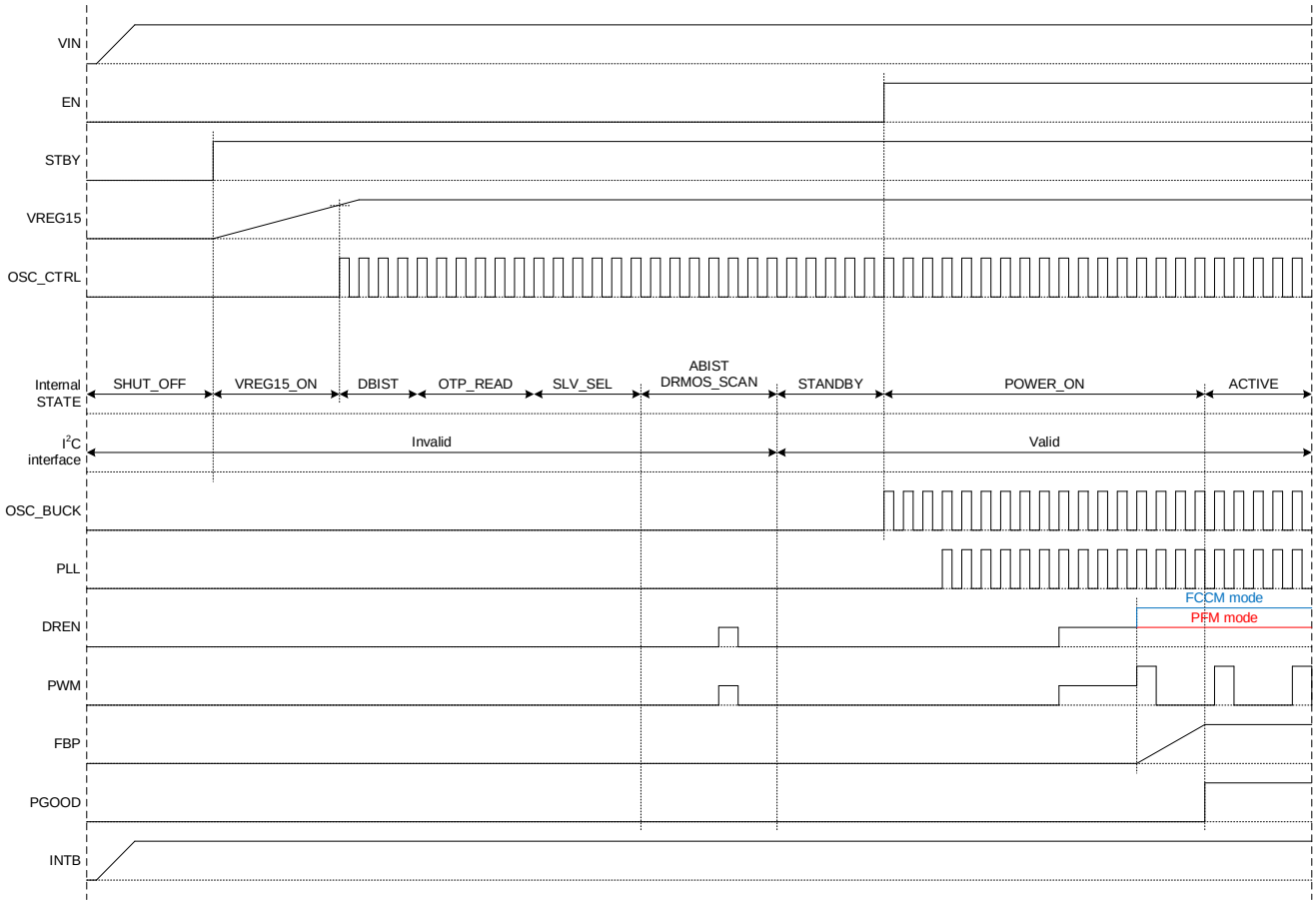


Figure 21. STBY ON, EN ON Sequence Timing Chart

Timing Chart – continued

3. EN OFF (STBY ON) Sequence

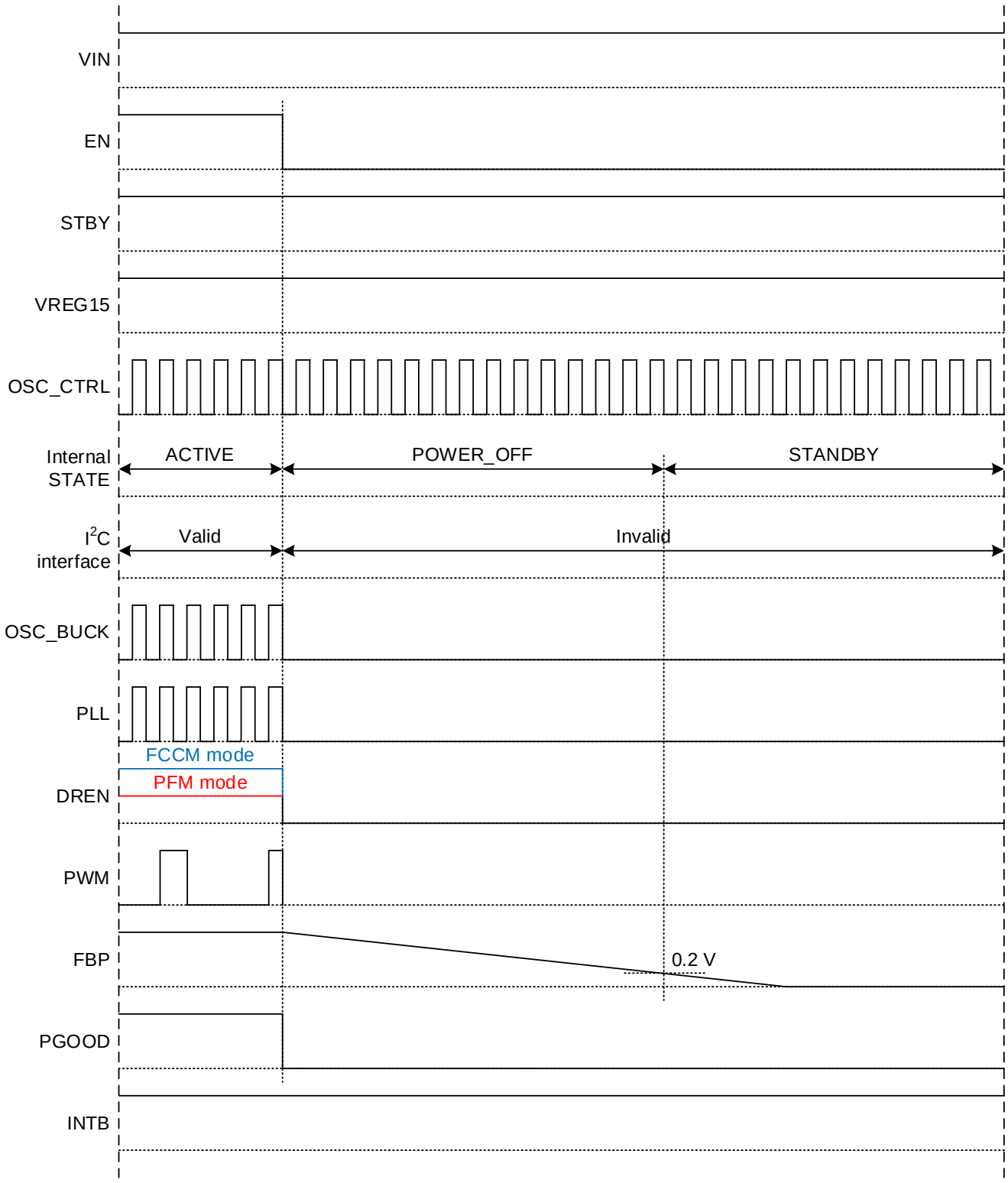


Figure 22. EN OFF (STBY ON) Sequence Timing Chart

Timing Chart – continued

4. EN OFF (STBY OFF) Sequence

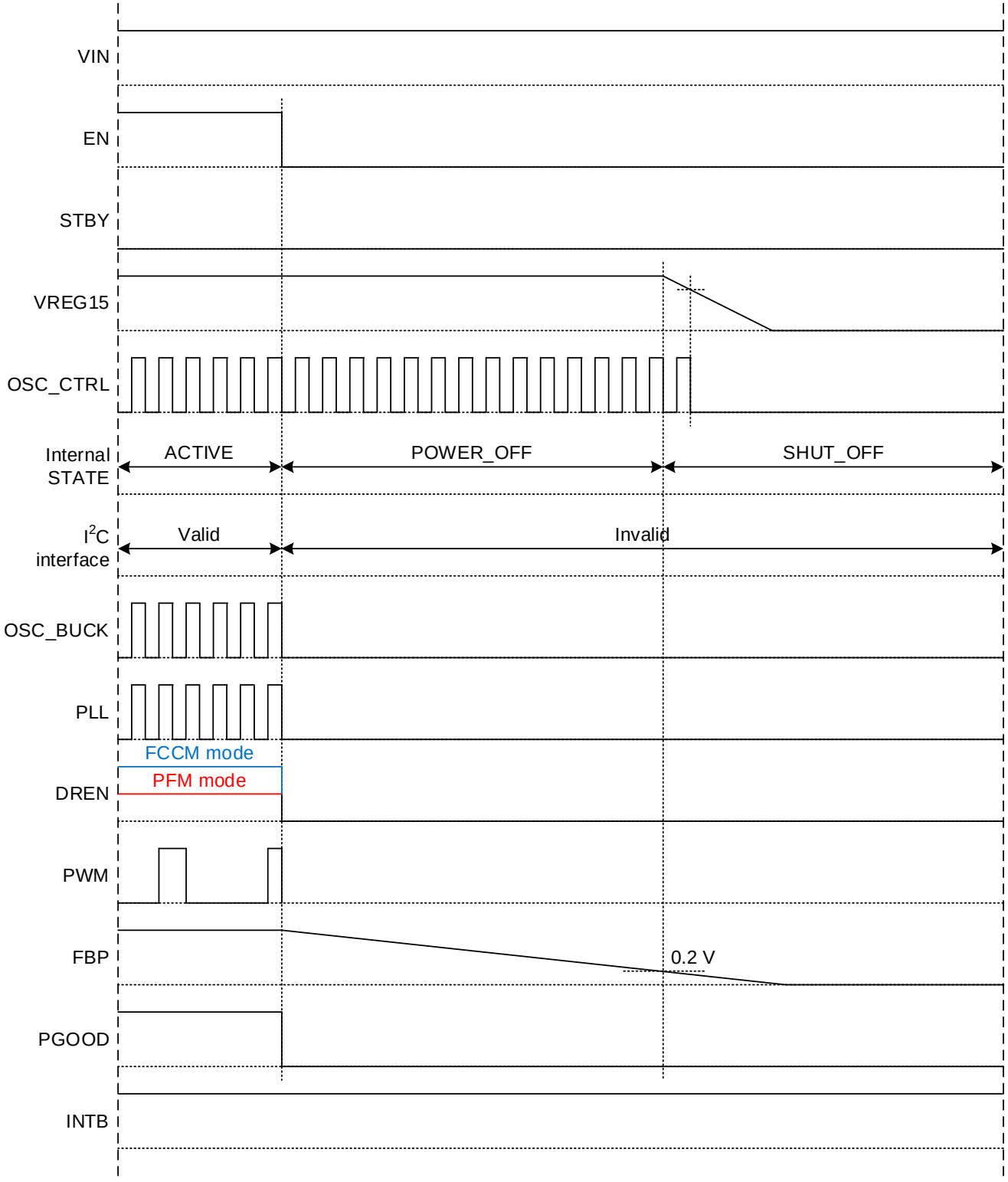


Figure 23. EN OFF (STBY OFF) Sequence Timing Chart

Timing Chart – continued

5. VIN, EN ON Sequence

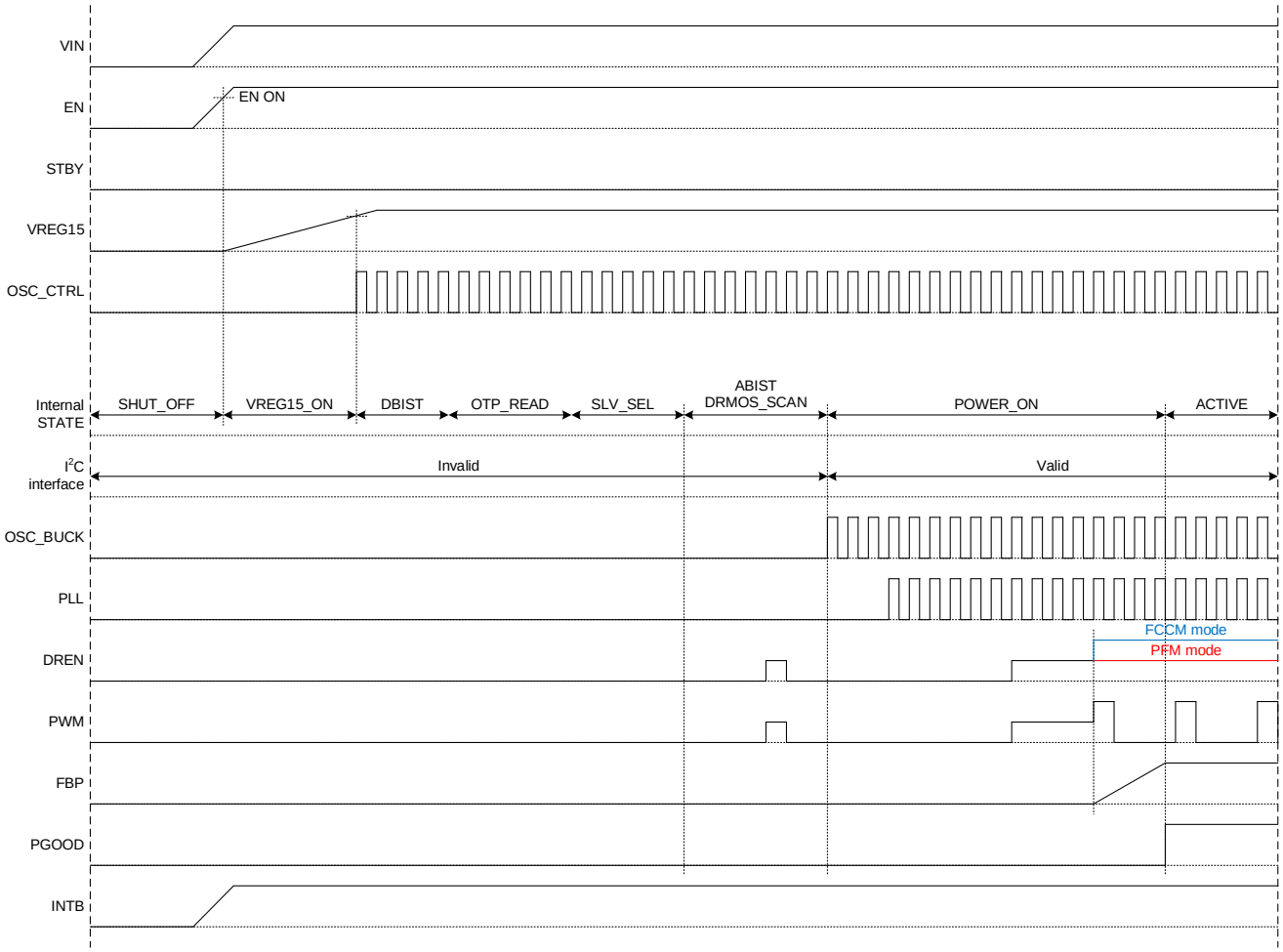


Figure 24. VIN, EN ON Sequence Timing Chart

Timing Chart – continued

6. UVLO Sequence

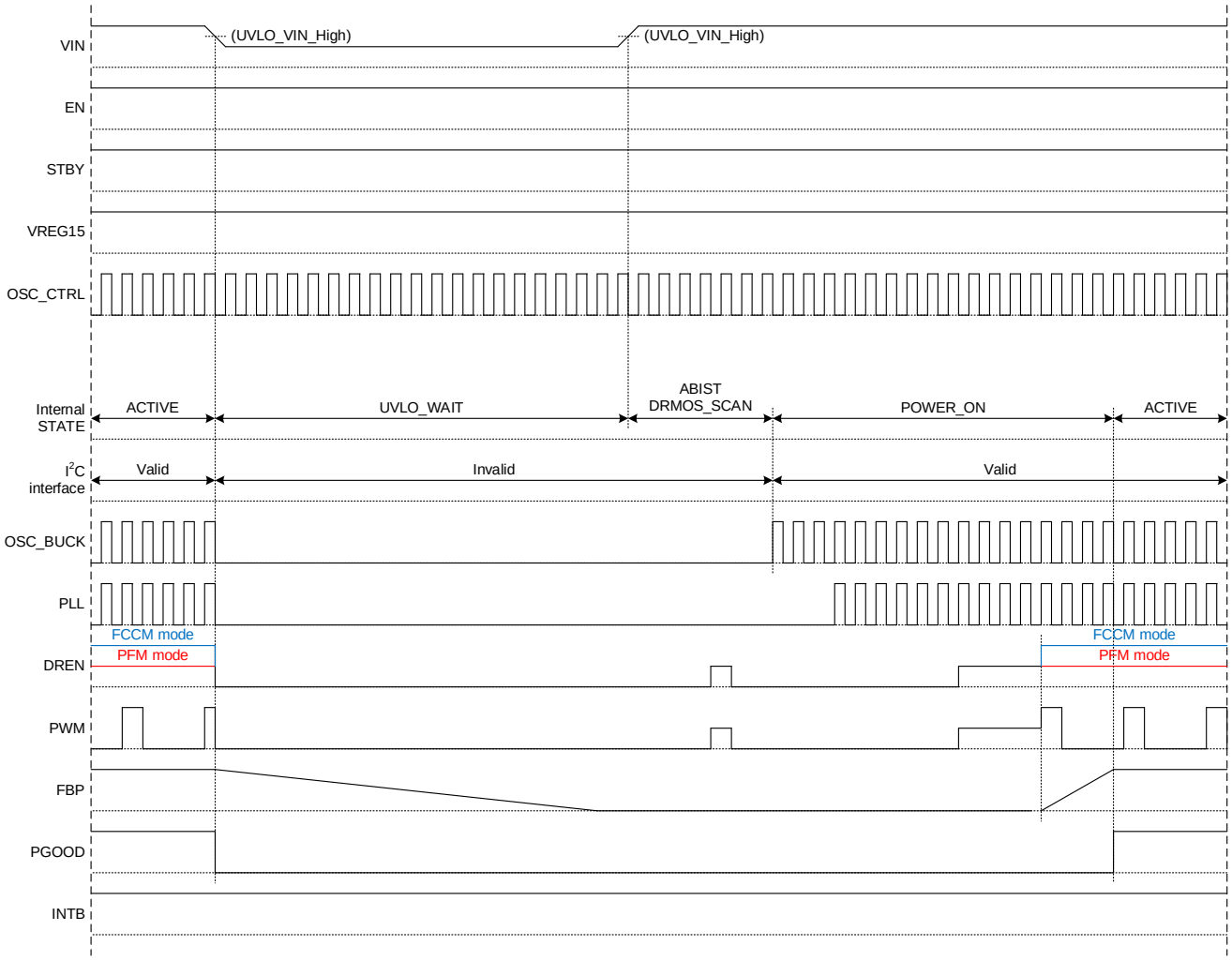


Figure 25. UVLO Sequence Timing Chart

Timing Chart – continued

7. ERROR State

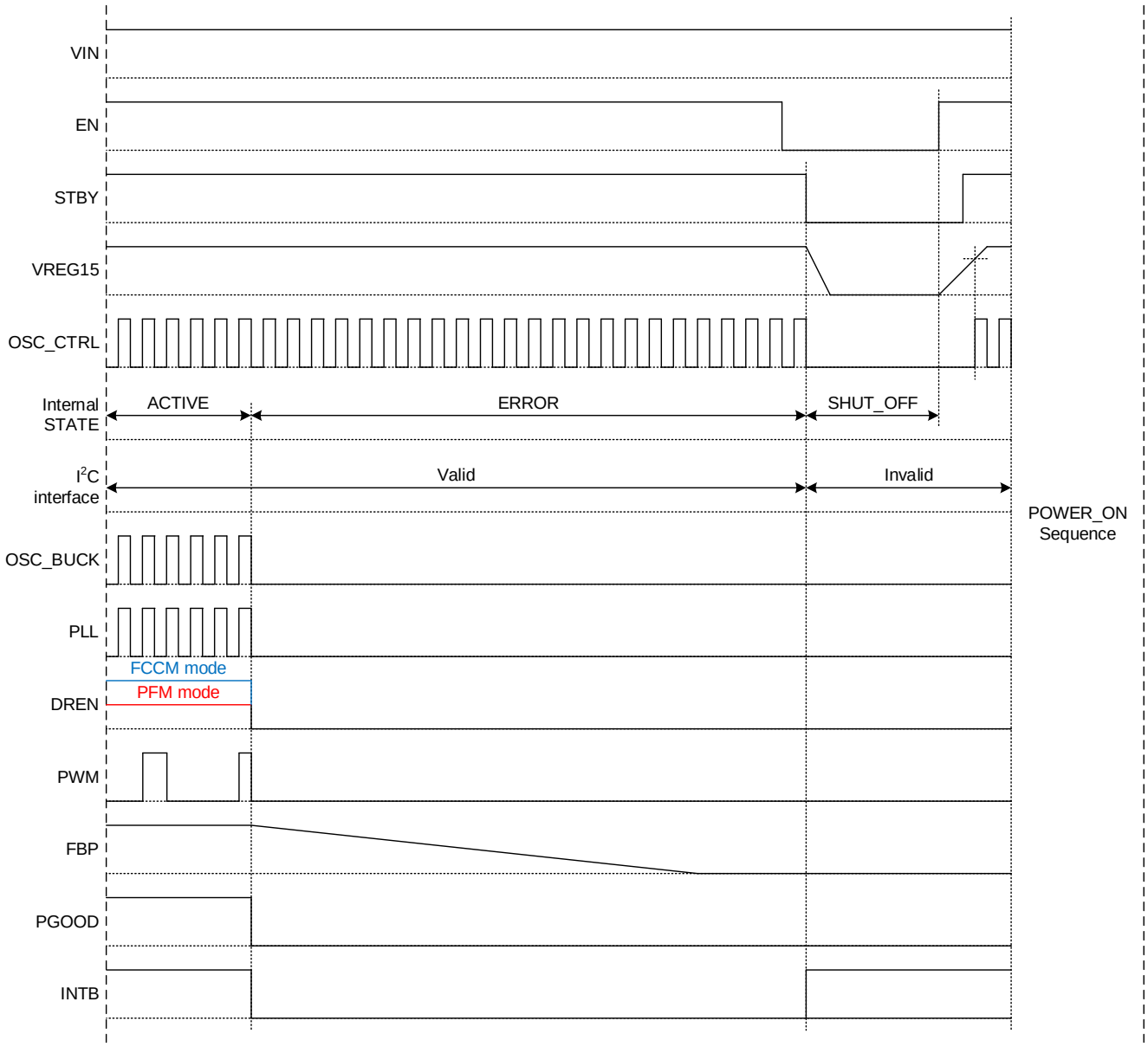


Figure 26. ERROR State Timing Chart

Register Map

Table 8. Register Map

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x00	Vendor Code	VENDOR [7:0]								RO	0x01
0x01	Product Code	PRODUCT [7:0]								RO	0x40
0x02	Product Revision	REVISION [7:0]								RO	0x03
0x03	PMIC State					STATE [3:0]				RO	-
0x04	INT_REQ	SYS_ERR2	SYS_ERR1	CMD_CHK	TSD_OVLO	DRMOS	OCP_BAL	OCP_ABS	OUT_ERR	R/W *1	-
0x05	INT[0]					V1_OVD	V1_UVD	V1_OVP	V1_UVP	R/W *1	-
0x06	INT[1]	PH8_OCP_ABS	PH7_OCP_ABS	PH6_OCP_ABS	PH5_OCP_ABS	PH4_OCP_ABS	PH3_OCP_ABS	PH2_OCP_ABS	PH1_OCP_ABS	R/W *1	-
0x07	INT[2]	PH8_OCP_BAL	PH7_OCP_BAL	PH6_OCP_BAL	PH5_OCP_BAL	PH4_OCP_BAL	PH3_OCP_BAL	PH2_OCP_BAL	PH1_OCP_BAL	R/W *1	-
0x08	INT[3]							DRMOS_TW	DRMOS_FLT	R/W *1	-
0x09	INT[4]							OVLO_VIN	TSD	R/W *1	-
0x0A	INT[5]							SHUTDOWN	INTB_TEST	R/W *1	-
0x0B	INT[6]			I^2C_ERR	SEQ_ERR	OSC_ERR	VREF_ERR	PGOOD_ERR	INTB_ERR	R/W *1	-
0x0C	INT[7]			DRMOS_SCAN_ERR	ABIST_ERR		SLV_ERR	OTP_ERR	DBIST_ERR	R/W *1	-
0x0D	IMON	IMON [7:0]								RO	-
0x0E											
0x0F	IMON1	IMON1 [7:0]								RO	-
0x10	IMON2	IMON2 [7:0]								RO	-
0x11	IMON3	IMON3 [7:0]								RO	-
0x12	IMON4	IMON4 [7:0]								RO	-
0x13	IMON5	IMON5 [7:0]								RO	-
0x14	IMON6	IMON6 [7:0]								RO	-
0x15	IMON7	IMON7 [7:0]								RO	-
0x16	IMON8	IMON8 [7:0]								RO	-
0x17	DRMOSTMP	DRMOSTMP [7:0]								RO	-
0x18	Active Phase	PH8	PH7	PH6	PH5	PH4	PH3	PH2	PH1	RO	-
0x19											
0x1A	System BIST				EN_READ (*RO)	PGOOD_SBIST_EN	INTB_SBIST_EN	ABIST_RUN (*W)	INTB_ASSERT (*W)	R/W *2	0x00
0x1B	OTP Refresh								OTP_RELOAD (*W)	R/W *2	0x00
0x1C	SOFT_RESET	ACCESS KEY [7:0]								R/W	0x00
0x1D	SHUTDOWN	ACCESS KEY [7:0]								R/W	0x00
0x1E	I^2C_CRC	ACCESS KEY [7:0]								R/W	0x00
0x1F											
0x20	INT_MASK	SYS_ERR2	SYS_ERR1	CMD_CHK	TSD_OVLO	DRMOS	OCP_BAL	OCP_ABS	OUT_ERR	R/W	0x00
0x21	INT[6]_MASK			I^2C_ERR	SEQ_ERR	OSC_ERR	VREF_ERR	PGOOD_ERR	INTB_ERR	R/W	0x00
0x22	INT[7]_MASK			DRMOS_SCAN_ERR	ABIST_ERR	EEP_ERR	SLV_ERR	OTP_ERR	DBIST_ERR	R/W	0x00
0x23	Output Voltage1	VOUT [7:0]								R/W	0x4B
0x24	Output Voltage2	POSNEG	OFFSET [6:0]							R/W	0x00
0x25											
0x26											
0x27	Slew Rate		SS_SLEW_RATE [2:0]				VID_SLEW_RATE [2:0]			R/W	0x30
0x28	Switching Frequency							SW_FREQ [1:0]		R/W *3	0x01
0x29	SSCG		SSCG_WIDTH [2:0]				SSCG_FREQ [2:0]			R/W *3	0x00

(Note 1) RO: Read Only
(Note 2) R/W: Read/Write
(Note 3) R/W*1: Read/Write (Cleared to 0 by Write 1)
(Note 4) R/W*2: Read/Write (*W: Write (auto-return-0), *RO: Read Only)
(Note 5) R/W*3: Read/Write (Write command is ignored in POWER_ON, ACTIVE and POWER_OFF. Only I^2C ACK is responded.)
(Note 6) Do not access the address 0x2A to 0xFF

Register Map – continued

1. Vendor Code

Address: 0x00

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x00	Vendor Code	VENDOR [7:0]								RO	0x01

Bit [7:0] VENDOR To identify ROHM vendor ID

2. Product Code

Address: 0x01

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x01	Product Code	PRODUCT [7:0]								RO	0x40

Bit [7:0] PRODUCT To identify product ID

3. Product Revision

Address: 0x02

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x02	Product Revision	REVISION [7:0]								RO	0x03

Bit [7:0] REVISION To identify revision ID

4. PMIC State

Address: 0x03

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x03	PMIC State					STATE [3:0]				RO	-

Bit [3:0] STATE To identify system state

0000: NA
0001: NA
0010: System state is in DBIST
0011: System state is in OTP_READ
0100: NA
0101: System state is in SLV_SEL
0110: NA
0111: System state is in UVLO_WAIT
1000: System state is in ABIST
1001: System state is in DRMOS_SCAN
1010: System state is in STANDBY
1011: System state is in POWER_ON
1100: System state is in ACTIVE
1101: System state is in POWER_OFF
1110: System state is in ERROR
1111: NA

Register Map – continued

5. INT_REQ

Address: 0x04

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x04	INT_REQ	SYS_ERR2	SYS_ERR1	CMD_CHK	TSD_OVLO	DRMOS	OCP_BAL	OCP_ABS	OUT_ERR	R/W *1	-

INT_REQ is the internal factor notification register. INTB is asserted when any INT_REQ bit is set to 1.
All INT [0] to INT [7] registers have to be cleared first, then notified INT_REQ bit can be cleared to 0 by Write 1, and INTB is de-asserted.
The detailed factor can be traced in INT [0] to INT [7].

Bit [0]	OUT_ERR	To identify INT [0] (address: 0x05) error
Bit [1]	OCP_ABS	To identify INT [1] (address: 0x06) error
Bit [2]	OCP_BAL	To identify INT [2] (address: 0x07) error
Bit [3]	DRMOS	To identify INT [3] (address: 0x08) error
Bit [4]	TSD_OVLO	To identify INT [4] (address: 0x09) error
Bit [5]	CMD_CHK	To identify INT [5] (address: 0x0A) error
Bit [6]	SYS_ERR1	To identify INT [6] (address: 0x0B) error
Bit [7]	SYS_ERR2	To identify INT [7] (address: 0x0C) error

6. INT [0]

Address: 0x05

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x05	INT[0]					V1_OVD	V1_UVD	V1_OVP	V1_UVP	R/W *1	-

INT [0] is the detailed factor of INT_REQ Bit [0].
Notified INT [0] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

V1_UVP (V1_OVP)
V1_UVP (V1_OVP) shows the protection of under (over) output voltage.
When V1_UVP or V1_OVP is detected, State is changed to ERROR and INTB is asserted.

V1_UVD (V1_OVD)
V1_UVD (V1_OVD) shows the detection of under (over) output voltage.
When V1_UVD or V1_OVD is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	V1_UVP	To identify UVP
Bit [1]	V1_OVP	To identify OVP
Bit [2]	V1_UVD	To identify UVD
Bit [3]	V1_OVD	To identify OVD

7. INT [1]

Address: 0x06

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x06	INT[1]	PH8_OCP_ABS	PH7_OCP_ABS	PH6_OCP_ABS	PH5_OCP_ABS	PH4_OCP_ABS	PH3_OCP_ABS	PH2_OCP_ABS	PH1_OCP_ABS	R/W *1	-

INT [1] is the detailed factor of INT_REQ Bit [1].
Notified INT [1] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

OCP_ABS shows the protection of each phase over current.
When OCP_ABS is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	PH1_OCP_ABS	To identify OCP_ABS of Phase 1
Bit [1]	PH2_OCP_ABS	To identify OCP_ABS of Phase 2
Bit [2]	PH3_OCP_ABS	To identify OCP_ABS of Phase 3
Bit [3]	PH4_OCP_ABS	To identify OCP_ABS of Phase 4
Bit [4]	PH5_OCP_ABS	To identify OCP_ABS of Phase 5
Bit [5]	PH6_OCP_ABS	To identify OCP_ABS of Phase 6
Bit [6]	PH7_OCP_ABS	To identify OCP_ABS of Phase 7
Bit [7]	PH8_OCP_ABS	To identify OCP_ABS of Phase 8

Register Map – continued

8. INT [2]

Address: 0x07

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x07	INT[2]	PH8_OCP_BAL	PH7_OCP_BAL	PH6_OCP_BAL	PH5_OCP_BAL	PH4_OCP_BAL	PH3_OCP_BAL	PH2_OCP_BAL	PH1_OCP_BAL	R/W *1	-

INT [2] is the detailed factor of INT_REQ Bit [2].
Notified INT [2] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

OCP_BAL shows the protection of the difference between each phase current and average current.
When OCP_BAL is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	PH1_OCP_BAL	To identify OCP_BAL of Phase 1
Bit [1]	PH2_OCP_BAL	To identify OCP_BAL of Phase 2
Bit [2]	PH3_OCP_BAL	To identify OCP_BAL of Phase 3
Bit [3]	PH4_OCP_BAL	To identify OCP_BAL of Phase 4
Bit [4]	PH5_OCP_BAL	To identify OCP_BAL of Phase 5
Bit [5]	PH6_OCP_BAL	To identify OCP_BAL of Phase 6
Bit [6]	PH7_OCP_BAL	To identify OCP_BAL of Phase 7
Bit [7]	PH8_OCP_BAL	To identify OCP_BAL of Phase 8

9. INT [3]

Address: 0x08

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x08	INT[3]							DRMOS_TW	DRMOS_FLT	R/W *1	-

INT [3] is the detailed factor of INT_REQ Bit [3].
Notified INT [3] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

DRMOS_FLT
DRMOD_FLT shows TSD, HOCP, LOCP, NOCP, DBIST_ERR or OTP_ERR which is detected and informed by Driver MOSFET.
When DRMOS_FLT is detected, State is changed to ERROR and INTB is asserted.

DRMOS_TW
DRMOS_TW shows thermal warning which is informed by voltage level from Driver MOSFET.
When DRMOS_TW is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	DRMOS_FLT	To identify DRMOS_FLT
Bit [1]	DRMOS_TW	To identify DRMOS_TW

10. INT [4]

Address: 0x09

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x09	INT[4]							OVLO_VIN	TSD	R/W *1	-

INT [4] is the detailed factor of INT_REQ Bit [4].
Notified INT [4] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

TSD
TSD shows the thermal protection.
When TSD is detected, State is changed to ERROR and INTB is asserted.

OVLO_VIN
OVLO_VIN shows the protection of over input voltage.
When OVLO_VIN is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	TSD	To identify TSD
Bit [1]	OVLO_VIN	To identify OVLO_VIN

Register Map – continued

11. INT [5]

Address: 0x0A

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x0A	INT[5]							SHUTDOWN	INTB_TEST	R/W *1	-

INT [5] is the detailed factor of INT_REQ Bit [5].
Notified INT [5] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

INTB_TEST
INTB_TEST shows Write command 1 in INTB_ASSERT bit (0x1A).
When INTB_TEST is detected, INTB is asserted only to check INTB connectivity and State never goes to ERROR.

SHUTDOWN
SHUTDOWN shows Write command 0x8E in SHUTDOWN (0x1D).
When SHUTDOWN is detected, State is changed to ERROR and INTB is asserted.

Bit [0]	INTB_TEST	To identify INTB_TEST
Bit [1]	SHUTDOWN	To identify SHUTDOWN

12. INT [6]

Address: 0x0B

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x0B	INT[6]			I^2C_ERR	SEQ_ERR	OSC_ERR	VREF_ERR	PGOOD_ERR	INTB_ERR	R/W *1	-

INT [6] is the detailed factor of INT_REQ Bit [6].
Notified INT [6] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

INTB_ERR
INTB_ERR shows the improper logic output of INTB pin.
Monitoring INTB pin condition is set by INTB_SBIST_EN bit (0x1A).
When INTB_ERR is detected, State is changed to ERROR and INTB is asserted.

PGOOD_ERR
PGOOD_ERR shows the improper logic output of PGOOD pin.
Monitoring PGOOD pin condition is set by PGOOD_SBIST_EN bit (0x1A).
When PGOOD_ERR is detected, State is changed to ERROR and INTB is asserted.

VREF_ERR
VREF_ERR shows the error of the difference between VREG15 and VREF.
When VREF_ERR is detected, State is changed to ERROR and INTB is asserted.

OSC_ERR
OSC_ERR shows the error of the difference between OSC_CTRL and OSC_BUCK.
When OSC_ERR is detected, State is changed to ERROR and INTB is asserted.

SEQ_ERR
SEQ_ERR shows the shutdown with Time-out (1 s) execution.
When SEQ_ERR is detected with EN = Low and STBY = High, State is changed to ERROR and INTB is asserted.
When SEQ_ERR is detected with EN = Low and STBY = Low, State is changed to SHUT_OFF.

I^2C_ERR
I^2C_ERR shows CRC error of I^2C.
When I^2C_ERR is detected, INTB is asserted only and State never goes to ERROR.

Bit [0]	INTB_ERR	To identify INTB_ERR
Bit [1]	PGOOD_ERR	To identify PGOOD_ERR
Bit [2]	VREF_ERR	To identify VREF_ERR
Bit [3]	OSC_ERR	To identify OSC_ERR
Bit [4]	SEQ_ERR	To identify SEQ_ERR
Bit [5]	I^2C_ERR	To identify I^2C_ERR

Register Map – continued

13. INT [7]

Address: 0x0C

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x0C	INT[7]			DRMOS_SCAN_ERR	ABIST_ERR		SLV_ERR	OTP_ERR	DBIST_ERR	R/W *1	-

INT [7] is the detail factor of INT_REQ [7].
Notified INT [7] bit has to be cleared to 0 by Write 1 before INT_REQ is cleared.

DBIST_ERR
DBIST_ERR shows the incompletion of digital BIST.
When DBIST_ERR is detected, State is changed to ERROR and INTB is asserted.

OTP_ERR
OTP_ERR shows the fault of OTP loading.
When OTP_ERR is detected, State is changed to ERROR and INTB is asserted.

SLV_ERR
SLV_ERR shows that target address which is set by divided resistance is not same value in 3 times continuously.
When SLV_ERR is detected, State is changed to ERROR and INTB is asserted.

ABIST_ERR
ABIST_ERR shows the incompletion of analog BIST.
When ABIST_ERR is detected, State is changed to ERROR and INTB is asserted.

DRMOS_SCAN_ERR
DRMOS_SCAN_ERR shows the connection error of Driver MOSFET.
When DRMOS_SCAN_ERR is detected, State is changed to ERROR and INTB is asserted.

Bit [0]	DBIST_ERR	To identify DBIST_ERR
Bit [1]	OTP_ERR	To identify OTP_ERR
Bit [2]	SLV_ERR	To identify SLV_ERR
Bit [4]	ABIST_ERR	To identify ABIST_ERR
Bit [5]	DRMOS_SCAN_ERR	To identify DRMOS_SCAN_ERR

14. IMON

Address: 0x0D

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x0D	IMON	IMON [7:0]								RO	-

Bit [7:0]	IMON	To identify total current of IMON1 to IMON8 (0xFF = 768 mV / ISENSE Gain (mV/A) x Active Phase Number)

15. IMONx (x = 1, 2, 3, 4, 5, 6, 7, 8)

Address: 0x0F to 0x16

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x0F	IMON1	IMON1 [7:0]								RO	-
0x10	IMON2	IMON2 [7:0]								RO	-
0x11	IMON3	IMON3 [7:0]								RO	-
0x12	IMON4	IMON4 [7:0]								RO	-
0x13	IMON5	IMON5 [7:0]								RO	-
0x14	IMON6	IMON6 [7:0]								RO	-
0x15	IMON7	IMON7 [7:0]								RO	-
0x16	IMON8	IMON8 [7:0]								RO	-

Bit [7:0]	IMONx	To identify output current of each Phase (0x00 is 0 A. 0xFF depends on BD9634x series ISENSE Gain. (0xFF = 768 mV / ISENSE Gain (mV/A)))

16. DRMOSTMP

Address: 0x17

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x17	DRMOSTMP	DRMOSTMP [7:0]								RO	-

Bit [7:0]	DRMOSTMP	To identify Driver MOSFET temperature at EN = ON. To identify BD96240MUF-C temperature at EN = OFF. (-40 °C (0x00) to +150 °C (0xFF))

Register Map – continued

17. Active Phase

Address: 0x18

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x18	Active Phase	PH8	PH7	PH6	PH5	PH4	PH3	PH2	PH1	RO	-

Bit [0]	PH1	To identify Driver MOSFET connection of Phase 1 0: Phase 1 is not connected. 1: Phase 1 is connected.
Bit [1]	PH2	To identify Driver MOSFET connection of Phase 2 0: Phase 2 is not connected. 1: Phase 2 is connected.
Bit [2]	PH3	To identify Driver MOSFET connection of Phase 3 0: Phase 3 is not connected. 1: Phase 3 is connected.
Bit [3]	PH4	To identify Driver MOSFET connection of Phase 4 0: Phase 4 is not connected. 1: Phase 4 is connected.
Bit [4]	PH5	To identify Driver MOSFET connection of Phase 5 0: Phase 5 is not connected. 1: Phase 5 is connected.
Bit [5]	PH6	To identify Driver MOSFET connection of Phase 6 0: Phase 6 is not connected. 1: Phase 6 is connected.
Bit [6]	PH7	To identify Driver MOSFET connection of Phase 7 0: Phase 7 is not connected. 1: Phase 7 is connected.
Bit [7]	PH8	To identify Driver MOSFET connection of Phase 8 0: Phase 8 is not connected. 1: Phase 8 is connected.

18. System BIST

Address: 0x1A

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x1A	System BIST				EN_READ (*RO)	PGOOD_SBIST_EN	INTB_SBIST_EN	ABIST_RUN (*W)	INTB_ASSERT (*W)	R/W *2	0x00

INTB_ASSERT
INTB_ASSERT is to execute INTB assertion to check connectivity with system level.
INTB_ASSERT bit is auto-return-0.

ABIST_RUN
ABIST_RUN is to execute ABIST during ACTIVE state.
ABIST_RUN bit is auto-return-0.

INTB_SBIST_EN
INTB_SBIST_EN is to set monitoring INTB pin condition during STANDBY and ACTIVE state.

PGOOD_SBIST_EN
PGOOD_SBIST_EN is to set monitoring PGOOD pin condition during STANDBY and ACTIVE state.

EN_READ
EN_READ is to monitor EN pin condition during STANDBY and ACTIVE state.
EN_READ bit is Read command only.

Bit [0]	INTB_ASSERT	1:	To execute INTB assertion
Bit [1]	ABIST_RUN	1:	To execute ABIST
Bit [2]	INTB_SBIST_EN	0:	Monitoring INTB pin condition is disabled
		1:	Monitoring INTB pin condition is enabled
Bit [3]	PGOOD_SBIST_EN	0:	Monitoring PGOOD pin condition is disabled
		1:	Monitoring PGOOD pin condition is enabled
Bit [4]	EN_READ	0:	the EN pin is Low
		1:	the EN pin is High

Register Map – continued

19. OTP Refresh

Address: 0x1B

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x1B	OTP Refresh								OTP_RELOAD (*W)	R/W *2	0x00

OTP_RELOAD is to reload OTP default value.
OTP_RELOAD bit is auto-return-0.

Bit [0]	OTP_RELOAD	To execute OTP_RELOAD

20. SOFT_RESET

Address: 0x1C

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x1C	SOFT_RESET	ACCESS KEY [7:0]								R/W	0x00

SOFT_RESET is to change State to DBIST by writing ACCESS KEY.

Bit [7:0]	ACCESS KEY (0x8E)	To set SOFT_RESET
Bit [7:0]	Any bits except 0x8E	Not to set SOFT_RESET

21. SHUTDOWN

Address: 0x1D

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x1D	SHUTDOWN	ACCESS KEY [7:0]								R/W	0x00

SHUTDOWN is to change State to ERROR by writing ACCESS KEY.

Bit [7:0]	ACCESS KEY (0x8E)	To set SHUTDOWN
Bit [7:0]	Any bits except 0x8E	Not to set SUHTDOWN

22. I^2C_CRC

Address: 0x1E

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x1E	I^2C_CRC	ACCESS KEY [7:0]								R/W	0x00

I^2C_CRC is to select CRC function by writing ACCESS KEY.

Bit [7:0]	ACCESS KEY (0xD9)	To select CRC function
Bit [7:0]	Any bits except 0xD9	Not to select CRC function

Register Map – continued

23. INT_MASK

Address: 0x20

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x20	INT_MASK	SYS_ERR2	SYS_ERR1	CMD_CHK	TSD_OVLO	DRMOS	OCP_BAL	OCP_ABS	OUT_ERR	R/W	0x00

To select whether INTB is asserted or not when INT_REQ bit is set 1.

Bit [0]	OUT_ERR	To set INTB assertion mask when OUT_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [1]	OCP_ABS	To set INTB assertion mask when OCP_ABS is detected 0: INTB is asserted 1: INTB is not asserted
Bit [2]	OCP_BAL	To set INTB assertion mask when OCP_BAL is detected 0: INTB is asserted 1: INTB is not asserted
Bit [3]	DRMOS	To set INTB assertion mask when DRMOS is detected 0: INTB is asserted 1: INTB is not asserted
Bit [4]	TSD_OVLO	To set INTB assertion mask when TSD_OVLO is detected 0: INTB is asserted 1: INTB is not asserted
Bit [5]	CMD_CHK	To set INTB assertion mask when CMD_CHK is detected 0: INTB is asserted 1: INTB is not asserted
Bit [6]	SYS_ERR1	To set INTB assertion mask when SYS_ERR1 is detected 0: INTB is asserted 1: INTB is not asserted
Bit [7]	SYS_ERR2	To set INTB assertion mask when SYS_ERR2 is detected 0: INTB is asserted 1: INTB is not asserted

24. INT [6]_MASK

Address: 0x21

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x21	INT[6]_MASK			I^2C_ERR	SEQ_ERR	OSC_ERR	VREF_ERR	PGOOD_ERR	INTB_ERR	R/W	0x00

To select INTB is asserted or not when INT [6] bit is set 1.

Bit [0]	INTB_ERR	To set INTB assertion mask when INTB_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [1]	PGOOD_ERR	To set INTB assertion mask when PGOOD_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [2]	VREF_ERR	To set INTB assertion mask when VREF_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [3]	OSC_ERR	To set INTB assertion mask when OSC_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [4]	SEQ_ERR	To set INTB assertion mask when SEQ_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [5]	I^2C_ERR	To set INTB assertion mask when I^2C_ERR is detected 0: INTB is asserted 1: INTB is not asserted

Register Map – continued

25. INT [7]_MASK

Address: 0x22

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x22	INT[7]_MASK			DRMOS_SCAN_ERR	ABIST_ERR		SLV_ERR	OTP_ERR	DBIST_ERR	R/W	0x00

To select INTB is asserted or not when INT [7] bit is set 1.

Bit [0]	DBIST_ERR	To set INTB assertion mask when DBIST_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [1]	OTP_ERR	To set INTB assertion mask when OTP_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [2]	SLV_ERR	To set INTB assertion mask when SLV_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [4]	ABIST_ERR	To set INTB assertion mask when ABIST_ERR is detected 0: INTB is asserted 1: INTB is not asserted
Bit [5]	DRMOS_SCAN_ERR	To set INTB assertion mask when DRMOS_SCAN_ERR is detected 0: INTB is asserted 1: INTB is not asserted

Register Map – continued

26. Output Voltage1

Address: 0x23

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x23	Output Voltage1	VOUT [7:0]								R/W	0x4B

Bit [7:0] VOUT — To set output voltage from 0.6 V (0x3C) to 2.0 V (0xC8 to 0xFF) by 10 mV/LSB
(Default value is 0.75 V (0x4B))
(Output Voltage = VOUT + OFFSET (lower than 0 V is clamped at 0 V and higher than 2.0 V is clamped at 2.0 V))
(Note)
Output voltage setting from 0 V to 0.6 V is prohibited.

27. Output Voltage2

Address: 0x24

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x24	Output Voltage2	POSNEG	OFFSET [6:0]							R/W	0x00

Bit [6:0] OFFSET — To set output voltage offset (Default value is 0 mV)
(0 mV to 317.5 mV (2.5 mV/bit))

Bit [7] POSNEG — To set positive or negative offset
0: Positive offset
1: Negative offset

28. Slew Rate

Address: 0x27

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x27	Slew Rate		SS_SLEW_RATE [2:0]				VID_SLEW_RATE [2:0]			R/W	0x30

Bit [2:0] VID_SLEW_RATE — To set voltage shift slew rate setting
(Default value is 0.63 mV/µs)

000: 0.63 mV/µs
001: 0.83 mV/µs
010: 1.25 mV/µs
011: 2.5 mV/µs
100: 5 mV/µs
101: 10 mV/µs
110: 20 mV/µs
111: 30 mV/µs

Bit [6:4] SS_SLEW_RATE — To set soft start slew rate setting (Default value is 1 mV/µs)
000: 5 mV/µs
001: 2.5 mV/µs
010: 1.25 mV/µs
011: 1 mV/µs
100: 0.83 mV/µs
101: 0.63 mV/µs
110: 0.5 mV/µs
111: 0.25 mV/µs

Slew Rate has to be selected with the consideration of rush current described in P.53

29. Switching Frequency

Address: 0x28

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x28	Switching Frequency							SW_FREQ [1:0]		R/W *3	0x01

Bit [1:0] SW_FREQ — To set switching frequency (Default value is 2.25 MHz)
00: NA
01: 2.25 MHz
10: NA
11: NA

Register Map – continued

30. SSCG

Address: 0x29

Address	Register Name	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	R/W	Default
0x29	SSCG		SSCG_WIDTH [2:0]				SSCG_FREQ [2:0]			R/W *3	0x00

Bit [2:0]	SSCG_FREQ	To set SSCG modulation frequency 000: OFF 001: 0.1 kHz 010: 0.5 kHz 011: 1 kHz 100: 2.5 kHz 101: 5 kHz 110: NA 111: NA
Bit [6:4]	SSCG_WIDTH	To set SSCG modulation width 000: 0.4 % 001: 2 % 010: 4 % 011: 6 % 100: 8 % 101: 10 % 110: NA 111: NA

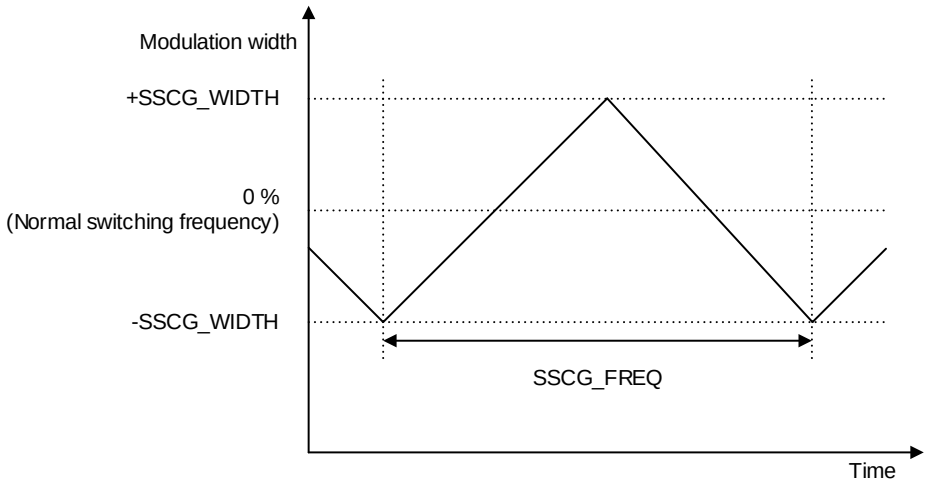


Figure 27. Modulation Waveform of SSCG

Register Description

1. I²C Interface

I²C interface (Target) is installed in BD96240MUF-C.

- The BD96240MUF-C supports multi-controller communication as a Target on the I²C interface.
- The BD96240MUF-C supports 7-bits addressing (10-bits addressing and general call address are not supported.)
- I²C interface communication is valid during STANDBY, POWER_ON, ACTIVE and ERROR.
- If the data line (SDA) is stuck at Low, the bus is cleared by the following procedures.
  - Send 18 clock pulses to release SDA bus.
  - Reset Control Logic by EN = Low and STBY = Low.
  - Remove VIN supply.

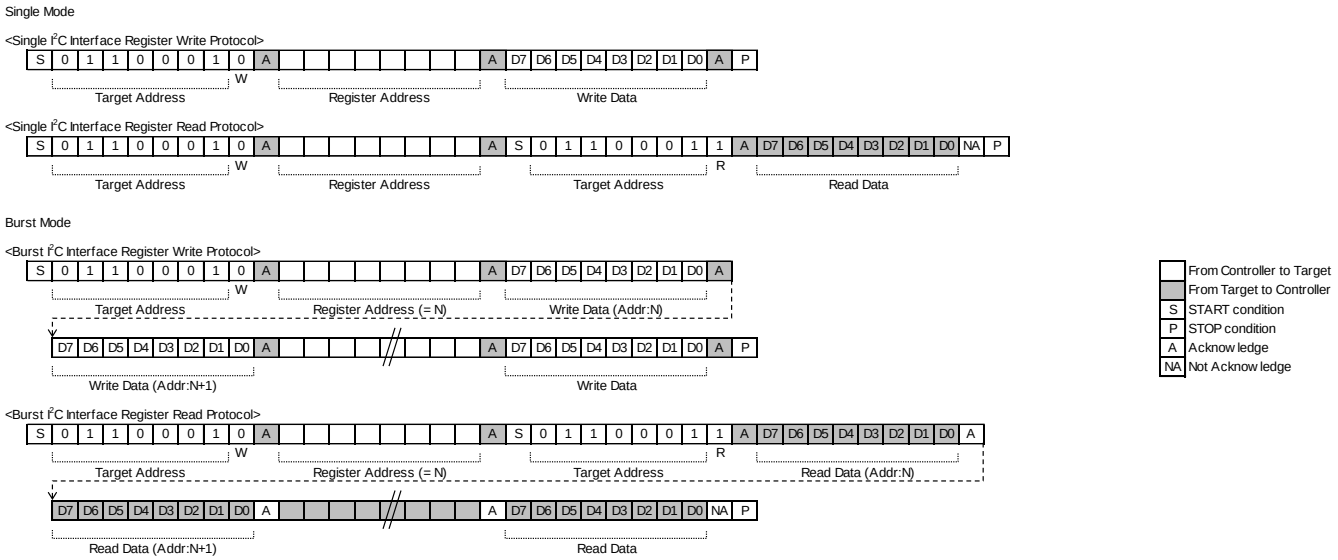


Figure 28. I²C Protocol Access (Example of Target Address: 0x31)

1. I²C Interface – continued

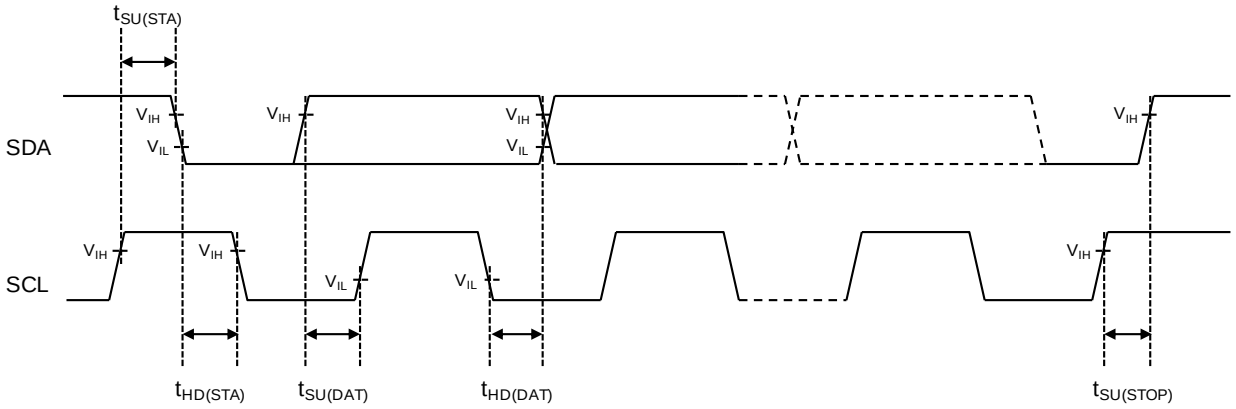


Figure 29. Definition of timing of I²C interface

Table 9. Characteristics of SCL and SDA

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCL Clock Frequency	F_{REQ}	-	-	1000	kHz	
SDA/SCL Input Voltage Low	V_{IL}	-0.3	-	+0.4	V	
SDA/SCL Input Voltage High	V_{IH}	1.4	-	5.5	V	
SDA Hold Time	$t_{HD\ (DAT)}$	0	-	-	ns	
SDA Setup Time	$t_{SU\ (DAT)}$	50	-	-	ns	
Start Condition Hold Time	$t_{HD\ (STA)}$	0.26	-	-	µs	
Start Condition Setup Time	$t_{SU\ (STA)}$	0.26	-	-	µs	
Stop Condition Setup Time	$t_{SU\ (STOP)}$	0.26	-	-	µs	
Input Current SDA	I_{INSDA}	-1	0	+1	µA	
Input Current SCL	I_{INSCL}	-1	0	+1	µA	
Output Voltage Low SDA	V_{OLSDA}	-0.3	-	+0.4	V	I_{LOAD} = -20 mA

Register Description – continued

2. CRC Function

CRC function is selected by setting address: 0x1E (ACCESS KEY is 0xD9).
CRC code is added in 8 bit at Target Address, Register Address, Write Data and Read data of I^2C communication.
The polynomial expression of CRC is $X^8 + X^5 + X^4 + 1$ and the initial value is 0x00, MSB first.

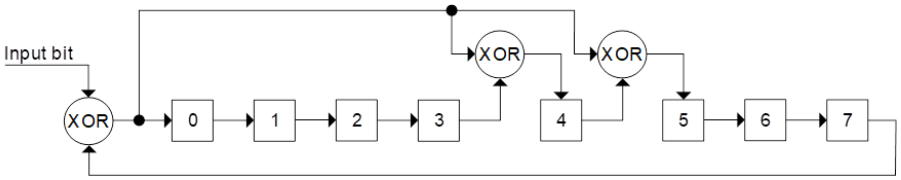


Figure 30. Polynomial Expression of CRC

In case of CRC error detection,
In Write register: Data is not written in the register after detecting CRC error (include Burst I^2C Register Write).
In Read register: 0xFF is replied in both Read Data and CRC Code.

When CRC error is detected, I^2C_ERR bit (address: 0x0B) is set 1 and INTB is asserted.

2. CRC Function – continued

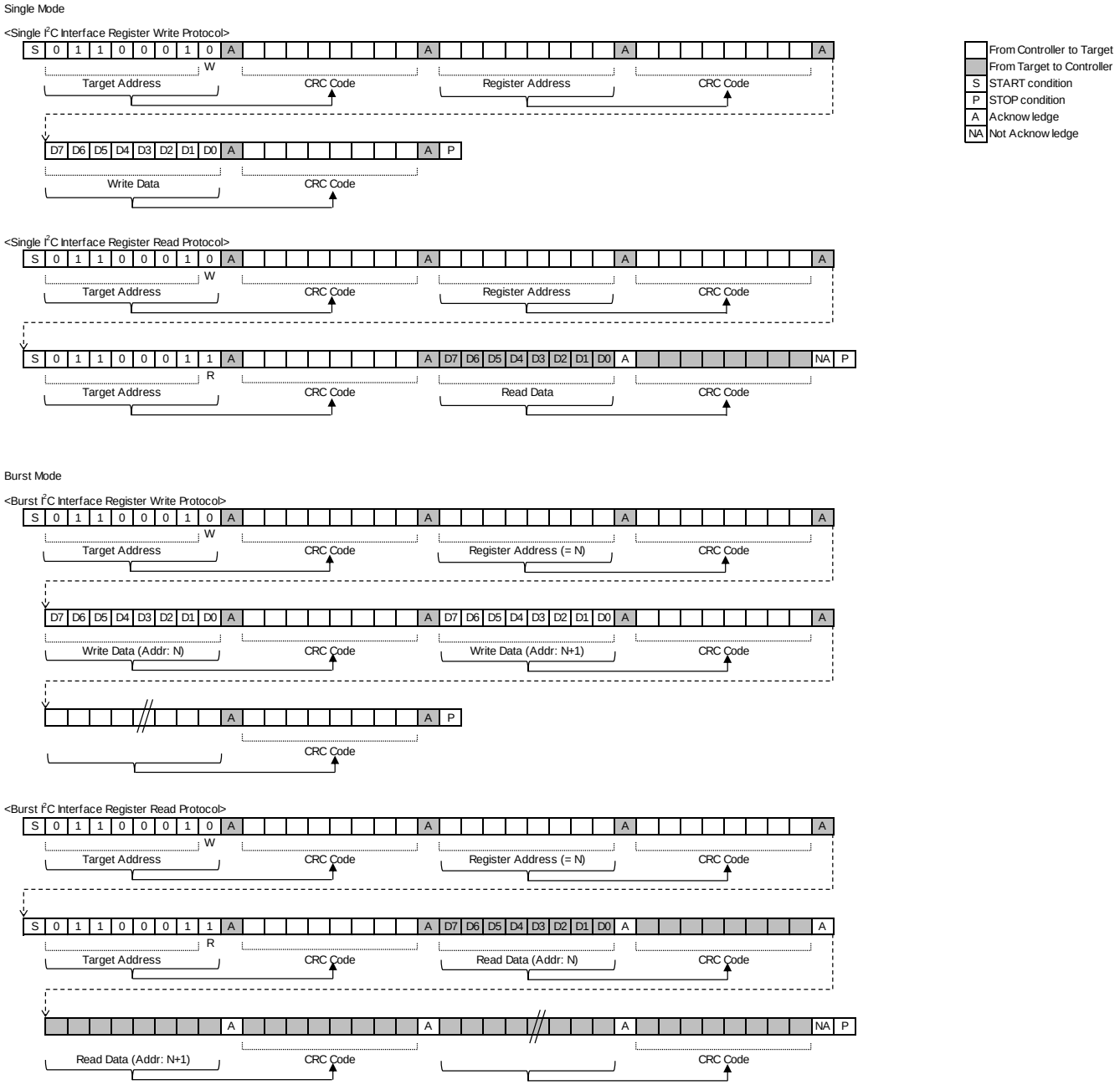


Figure 31. I²C Protocol Access of CRC (Example of Target Address: 0x31)

Register Description – continued

3. Target Address Selection

Target Address is selected from 7 options based on the divided voltage level.
Table 10 shows the recommended resistance value for selecting each Target Address.
(See the chapter “Block Diagram” about the placement of R1 and R2.)

Table 10. Recommended Resistance Value of SLVSEL

	R1*(Note 1)*	R2*(Note 1)*	Target Address	Target Address at ERROR state*(Note 2)*
SLVSEL Input Voltage 1	560 kΩ	120 kΩ	0x31	0x31 or 0x30
SLVSEL Input Voltage 2	220 kΩ	100 kΩ	0x32	0x32 or 0x30
SLVSEL Input Voltage 3	150 kΩ	120 kΩ	0x33	0x33 or 0x30
SLVSEL Input Voltage 4	120 kΩ	150 kΩ	0x34	0x34 or 0x30
SLVSEL Input Voltage 5	100 kΩ	220 kΩ	0x35	0x35 or 0x30
SLVSEL Input Voltage 6	120 kΩ	560 kΩ	0x36	0x36 or 0x30
SLVSEL Input Voltage 7	330 kΩ	-	0x37	0x37 or 0x30

(Note 1) Resistance tolerance is within ±5 %.
(Note 2) As Target Address is determined in SLV_SEL state and the default value is 0x30, any Errors before SLV_SEL(including SLV_ERR) makes Target Address as “0x30” regardless of SLVSEL input voltage.

Register Description – continued

4. Interruption Factor (INTB)

The interruption signal is notified from the INTB pin when BD96240MUF-C detects the warning or error condition and the detection history is registered to the notification INT [X] register (X = 0 to 7).
By reading out this, it is possible to know which warning or error is detected.
INTB is cleared by Write 1 to the notified INT_REQ bit and INT [X] bit.
(Note: INT_REQ bit has to be cleared to 0 by Write 1 after INT [0] to INT [7] is cleared.)

Interruption signal is masked by setting MASK register. INT_REQ, INT [6] and INT [7] can be masked.
INT_MASK is to select whether INTB is asserted or not when INT_REQ bit is set 1.
INT [6] MASK is to select whether INTB is asserted or not when INT [6] bit is set 1.
INT [7] MASK is to select whether INTB is asserted or not when INT [7] bit is set 1.

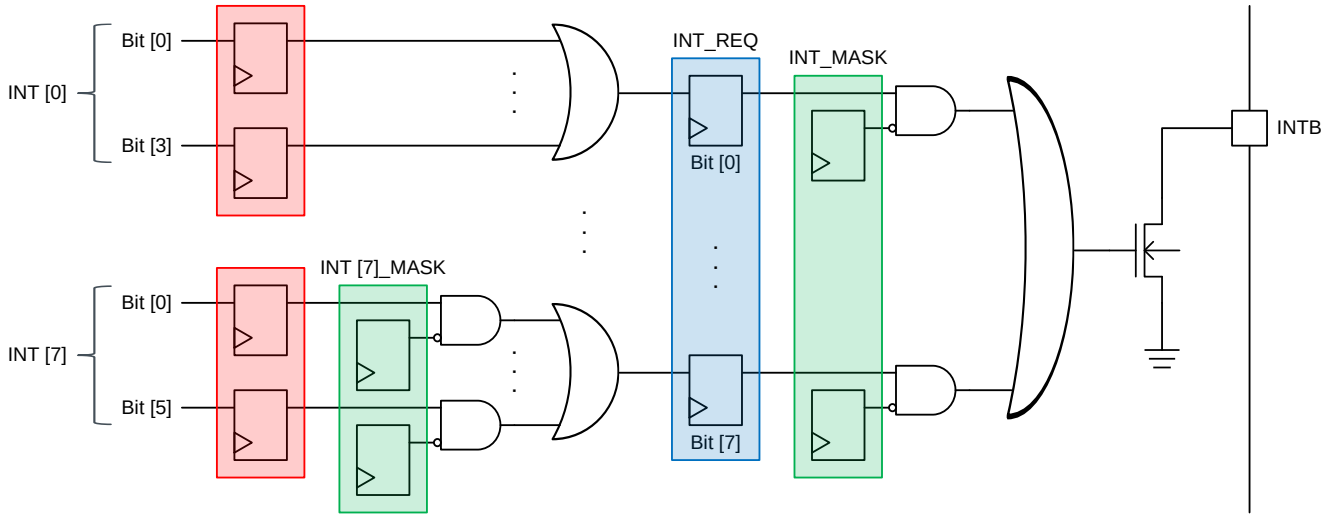


Figure 32. Block Diagram of INTB, INT_REQ and INT [X] (X = 0 to 7)

Block Operation Description

1. Phase Number Scan

Phase number is automatically scanned and set during boot-up sequence. Unused phase's PWM pin of Controller has to be tied to VREG15 output of Controller to be indicated as unused.
If all the 8 phases are not used, lower phase number has to be used without any unused phase in the middle.
Acceptable phase configuration is below. Other phase configuration leads to ERROR and No Boot-up.

1 phase: PWM1
2 phase: PWM1, 2
3 phase: PWM1, 2, 3
4 phase: PWM1, 2, 3, 4
5 phase: PWM1, 2, 3, 4, 5
6 phase: PWM1, 2, 3, 4, 5, 6
7 phase: PWM1, 2, 3, 4, 5, 6, 7
8 phase: PWM1, 2, 3, 4, 5, 6, 7, 8

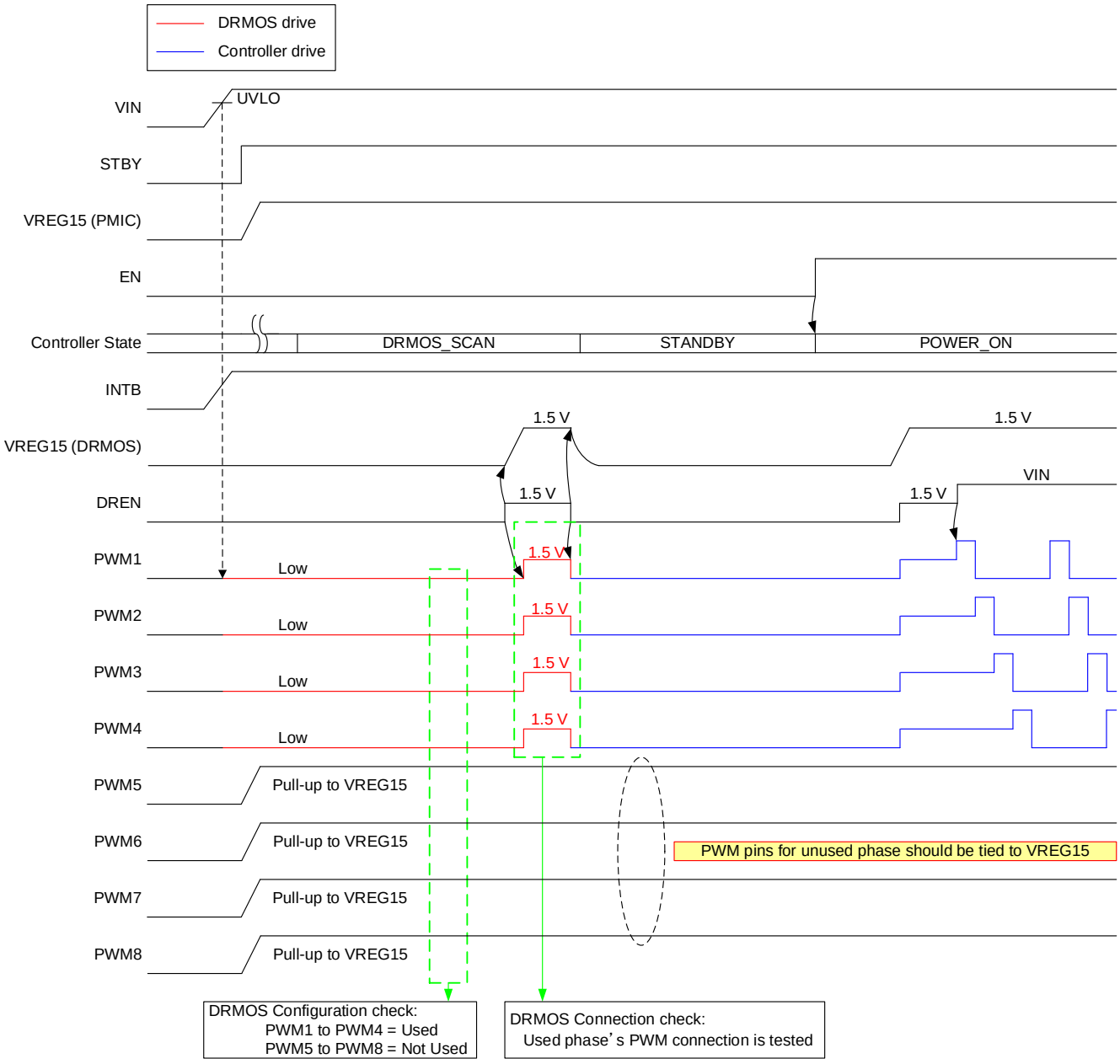


Figure 33. Driver MOSFET Phase Number Scan Example (Normal case with 4 phase)

1. Phase Number Scan – continued

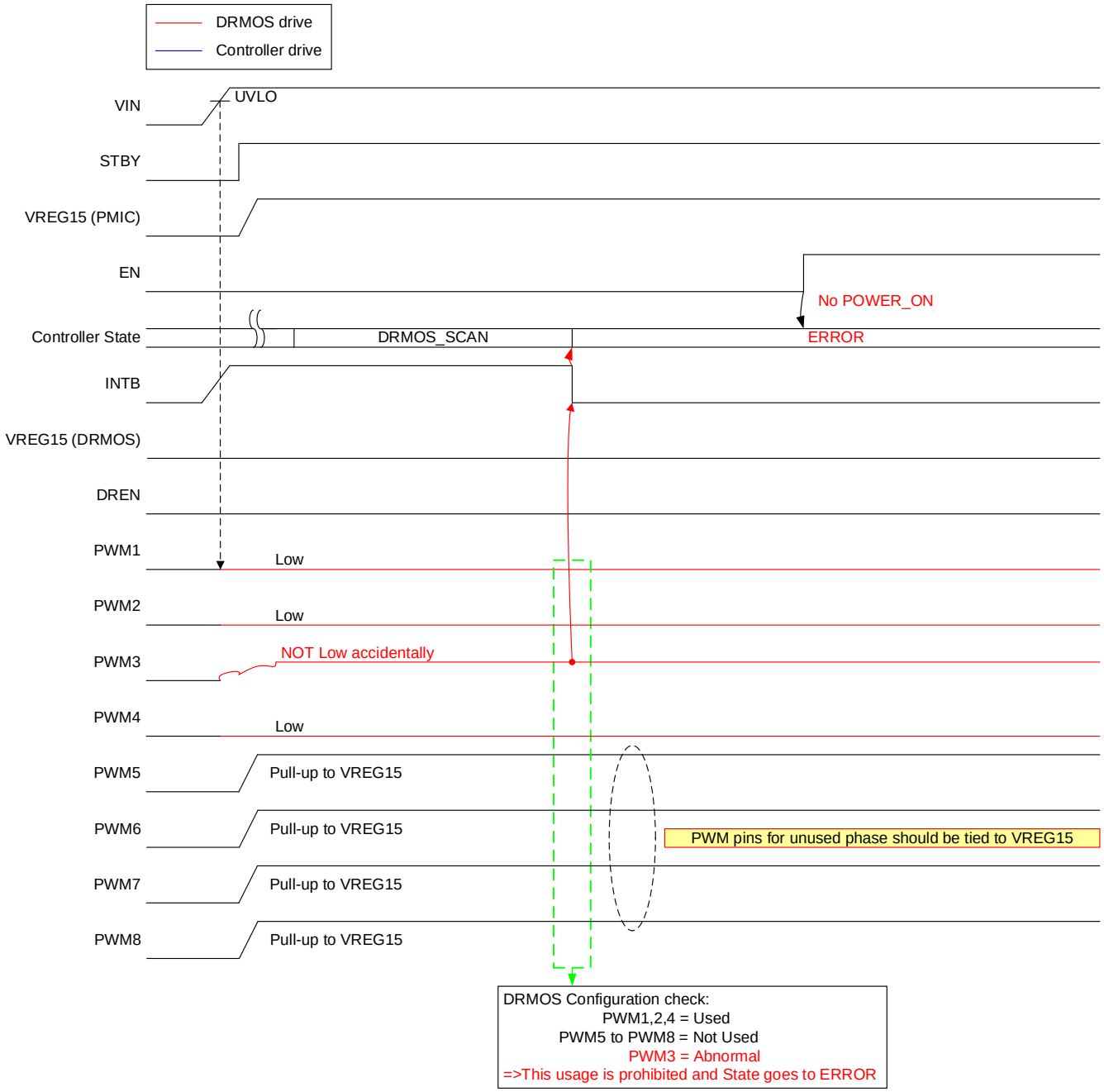


Figure 34. Driver MOSFET Phase Number Scan Example (Error case 1)

1. Phase Number Scan – continued

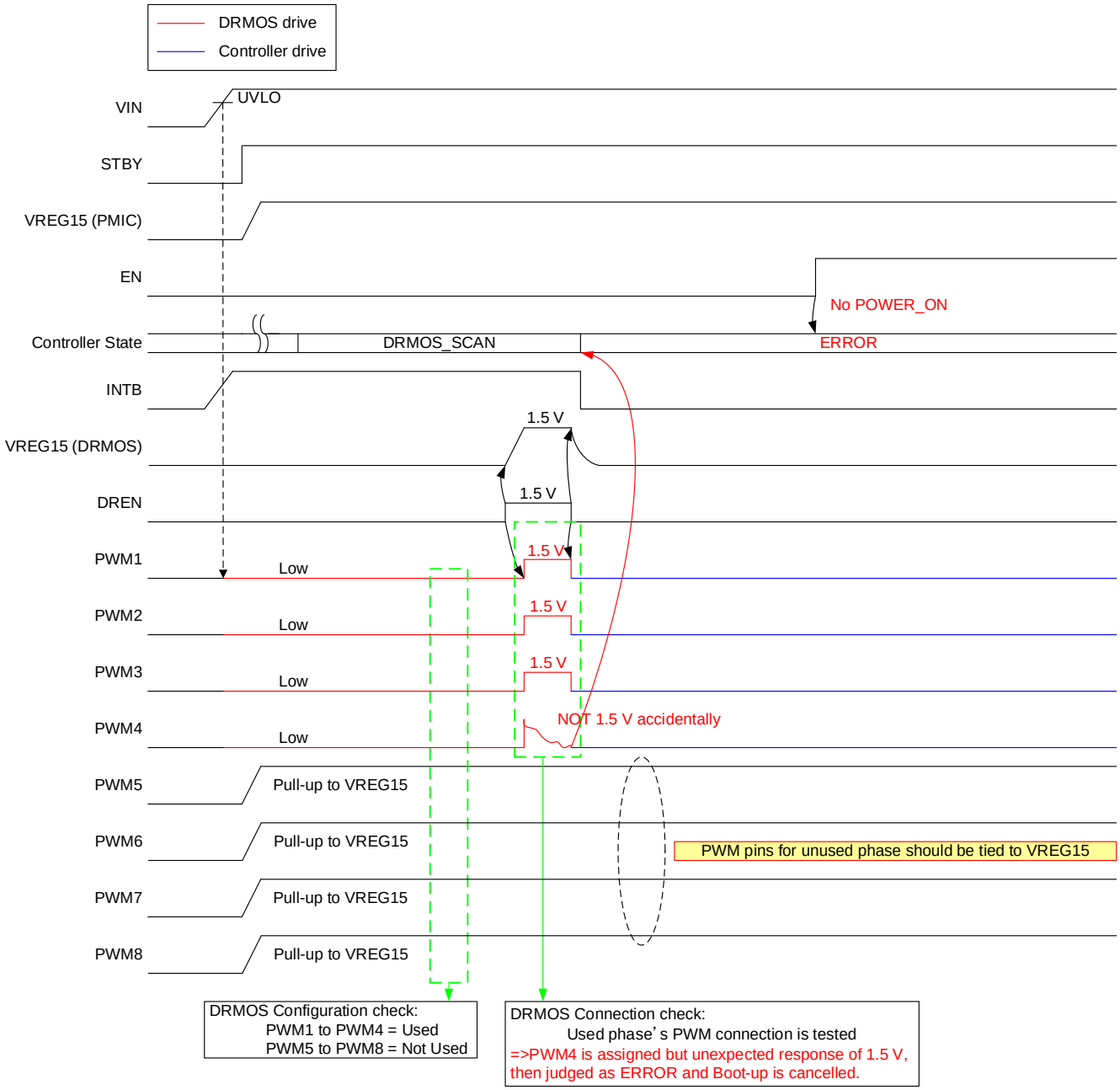


Figure 35. Driver MOSFET Phase Number Scan Example (Error case 2)

Block Operation Description – continued

2. Absolute OCP (OCP_ABS), Balance OCP (OCP_BAL) operation

OCP_ABS and OCP_BAL are detected by monitoring ISENSE input. When ISENSE reaches OCP_ABS or OCP_BAL threshold, INTB signal is asserted only (not leads to shutdown).

OCP_ABS threshold is fixed current value. When maximum ISENSE reaches OCP_ABS threshold and keeps for 10 µs (maximum) continuously, INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.

OCP_BAL (+, -) threshold is defined by Ave. current value +/-4 A (default). When maximum ISENSE reaches OCP_BAL (+) threshold and keeps for 10 µs (maximum) continuously, BD96240MUF-C asserts INTB signal. When minimum ISENSE reaches OCP_BAL (-) threshold and keeps for 10 µs (maximum), INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.

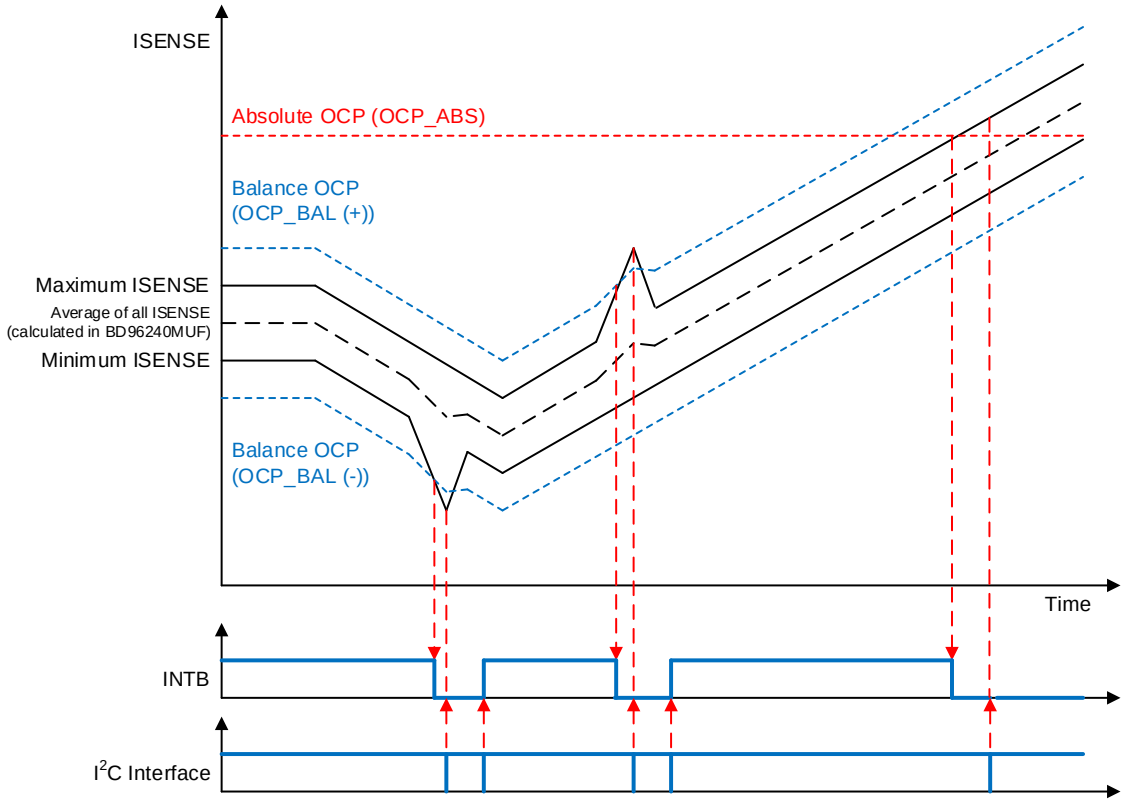


Figure 36. Timing Chart of OCP_ABS and OCP_BAL

Name	Deglitch time to set INTB flag	Buck Controller Behavior	State	INTB level	PGOOD level
OCP_ABS	10 µs (maximum)	Continue operating	Active	Go to Low	Keep High
OCP_BAL	10 µs (maximum)	Continue operating	Active	Go to Low	Keep High

Block Operation Description – continued

3. Voltage Detection Function

To avoid the shutdown without knowing the output voltage issue (OVP or UVP), the voltage warning level (OVD or UVD) is provided before reaching the protection voltage level.
When output voltage reaches OVD threshold and keeps for 10 µs (maximum) continuously, INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.
When output voltage reaches UVD threshold and keeps for 2 µs (maximum) continuously, INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.

When output voltage reaches OVP threshold and keeps for 10 µs (maximum) continuously, shutdown is occurred, State is changed to ERROR and INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.
When output voltage reaches UVP threshold and keeps for 2 µs (maximum) continuously, shutdown is occurred, State is changed to ERROR and INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.

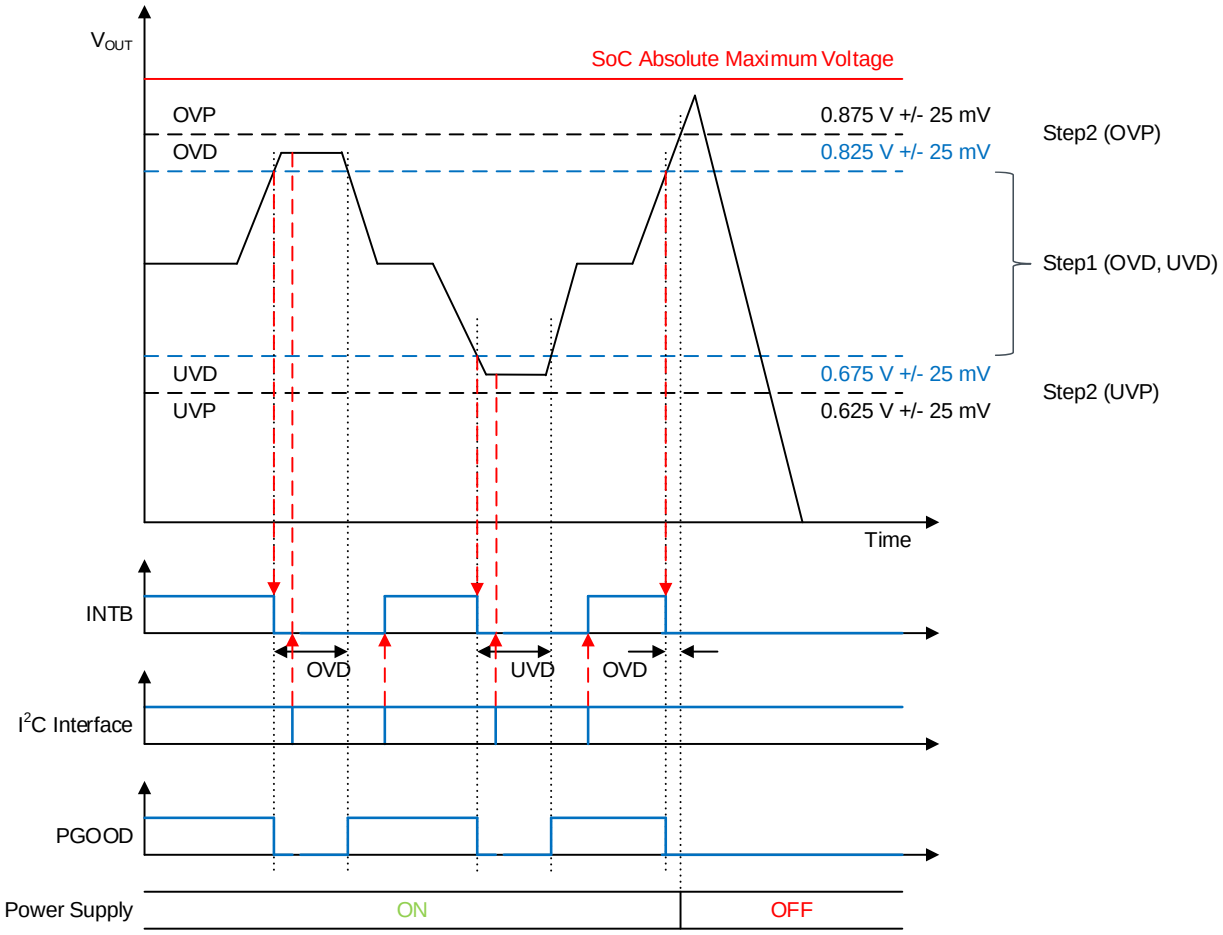


Figure 37. Timing Chart of Voltage Detection Function

Name	Deglitch time to set INTB flag	Buck Controller Behavior	State	INTB level	PGOOD level
OVD	10 µs (maximum)	Continue operating	Active	Go to Low	Go to Low
UVD	2 µs (maximum)	Continue operating	Active	Go to Low	Go to Low
OVP	10 µs (maximum)	Shutdown	Go to ERROR	Go to Low	Go to Low
UVP	2 µs (maximum)	Shutdown	Go to ERROR	Go to Low	Go to Low

Block Operation Description – continued

4. Thermal Detection Function

A built-in internal thermal shutdown (TSD) circuit is provided to protect IC from the damage due to excess temperature. TSD threshold temperature is +175 °C (typ). When Tj of BD9634x series reaches its own TSD threshold temperature, shutdown is occurred (BD9634x series controls the DREN pin to Low) and State is changed to ERROR.
To avoid the shutdown without knowing TSD, the thermal warning level (TW) is provided before reaching BD9634x series TSD– which is monitoring TEMP voltage. TW threshold temperature on a temperature conversion is 140 °C (typ).
When Tj of BD9634x series reaches TW threshold and keeps for 1 ms (maximum) continuously, INTB signal is asserted. INTB signal is cleared after INT_REQ is cleared.

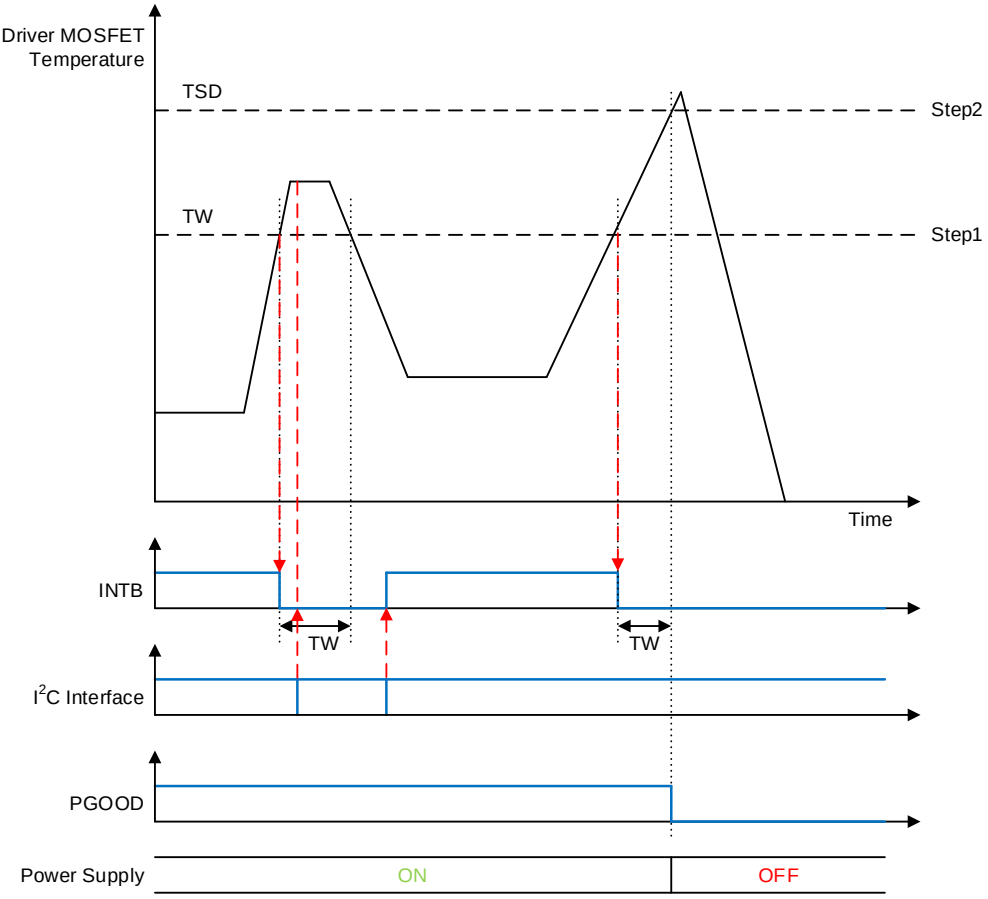


Figure 38. Timing Chart of Thermal Detection Function

Name	Deglitch time to set INTB flag	Buck Controller Behavior	State	INTB level	PGOOD level
TW	1 ms (maximum)	Continue operating	Active	Go to Low	Keep High
TSD	1 ms (maximum)	Shutdown	Go to ERROR	Go to Low	Go to Low

Block Operation Description – continued

5. Selection of Output Capacitor

Rush current is calculated in the following equation.

$$Irush = Icharge + I_{OUT} \quad [A]$$
$$Icharge = C_{OUT} \times Slewrate \quad [A]$$

Where :

$Icharge$	Charge or discharge current to/from output capacitor during changing output voltage.
C_{OUT}	Output capacitor.
$Slewrate$	Voltage shift per second.
I_{OUT}	Output current.

Irush has to be set less than 20 A/phase during charging current to output capacitor and more than -10 A during discharging current from output capacitor by adjusting the output capacitor or the slew rate of output voltage.

6. I_{OUT} Monitoring Accuracy

The following graphic shows the I_{OUT} monitoring accuracy as a reference. The I_{OUT} monitoring accuracy is affected by R_ISETx (Figure 42) accuracy.

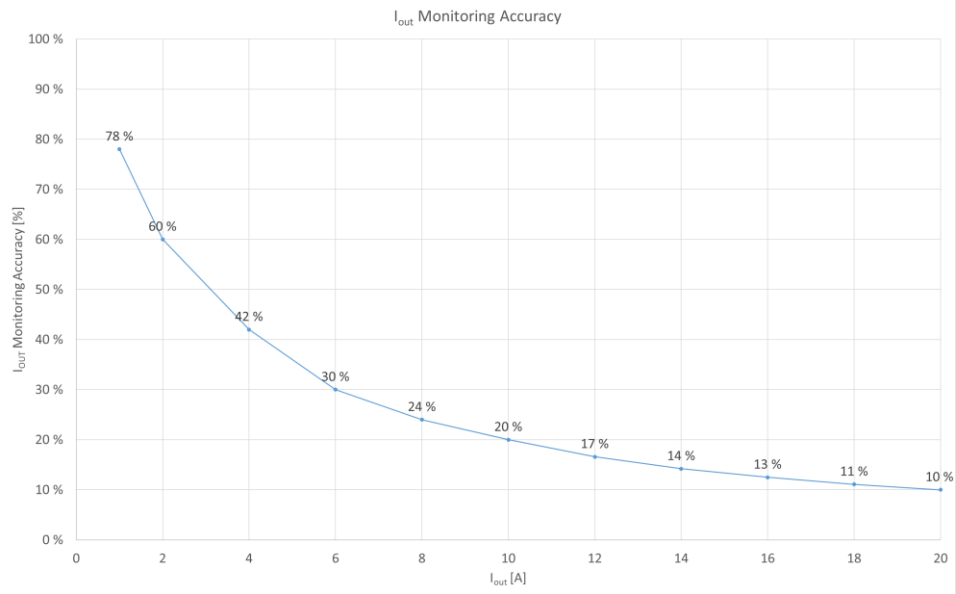


Figure 39. I_{OUT} Monitoring Accuracy

Block Operation Description – continued

7. ADC Round Robin Operation

BD96240MUF-C controls the ADC converter and the multiplexer as follows: select IS1 (Phase1 current), start a conversion and store the result in the corresponding register, proceed with the remaining 15 channels (including 7 reserve channels) and start again with IS1. The conversion of 1 channel is completed with 5 µs (The conversion of 1 loop is completed with 80 µs (= 5 µs x 16 channels)).

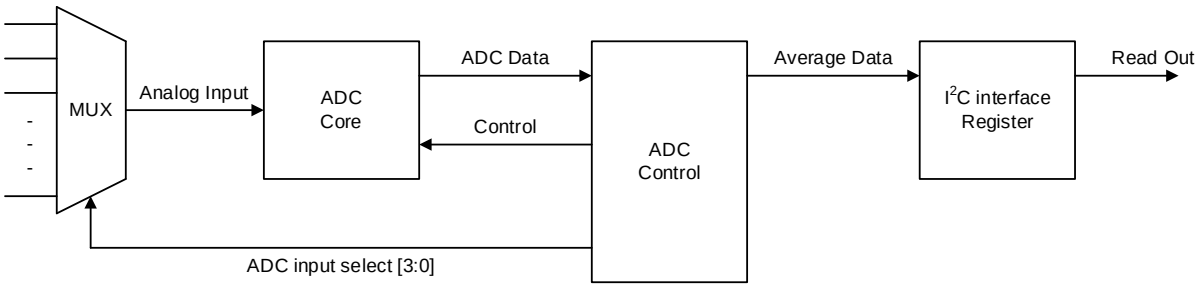


Figure 40. ADC Block Diagram

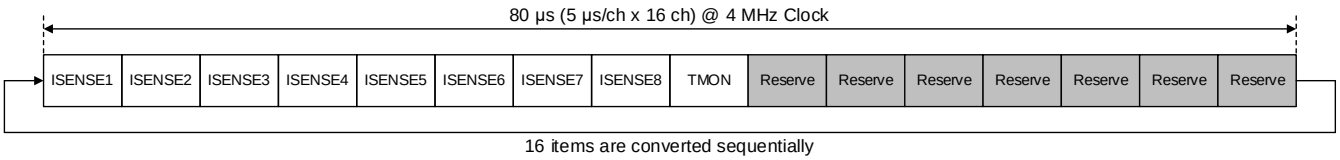


Figure 41. Round Robin Operation

Block Operation Description – continued

8. Digital Built-in Self-test (DBIST)

The self-diagnosis of digital circuit (DBIST) is executed automatically during DBIST state. When DBIST isn't complete, State is changed to ERROR and INTB signal is asserted. The error information is registered in DBIST_ERR (address: 0x0C). INTB signal is cleared after INT_REQ is cleared.

9. Analog Built-in Self-test (ABIST)

The self-diagnosis of analog circuit (ABIST) is executed automatically during ABIST state and is executed manually during ACTIVE state with I^2C interface command (ABIST_RUN (address: 0x1A)). OVD, UVD and SHUTDOWN comparator diagnosis are covered by ABIST execution. When ABIST isn't complete, State is changed to ERROR and INTB signal is asserted. The error information is registered in ABIST_ERR (address: 0x0C). INTB signal is cleared after INT_REQ is cleared.

(Note 1)
The manual ABIST run time is 330 µs (typical). During this time, the actual output voltage isn't monitored. So real OVD, UVD and SHUTDOWN aren't detected.

(Note 2)
When FBP pin voltage is more than 0.2 V during ABIST state, there is possibility to detect ABIST error with Time-out (1 s) execution.

10. Pin Built-in Self-test (Pin BIST)

The self-diagnosis of critical pin (Pin BIST) is monitored continuously during STANDBY and ACTIVE state by setting I^2C serial interface command (INTB_SBIST_EN and PGOOD_SBIST_EN (address: 0x1A)). INTB and PGOOD pin diagnosis are covered by Pin BIST execution (INTB_SBIST_EN for the INTB pin and PGOOD_SBIST_EN for the PGOOD pin). When the wrong signal condition is monitored, State is changed to ERROR and INTB signal is asserted. The error information is registered in INTB_ERR (address: 0x0B) for INTB pin error and PGOOD_ERR (address: 0x0B) for PGOOD pin error. INTB signal is cleared after INT_REQ is cleared.

Application Example

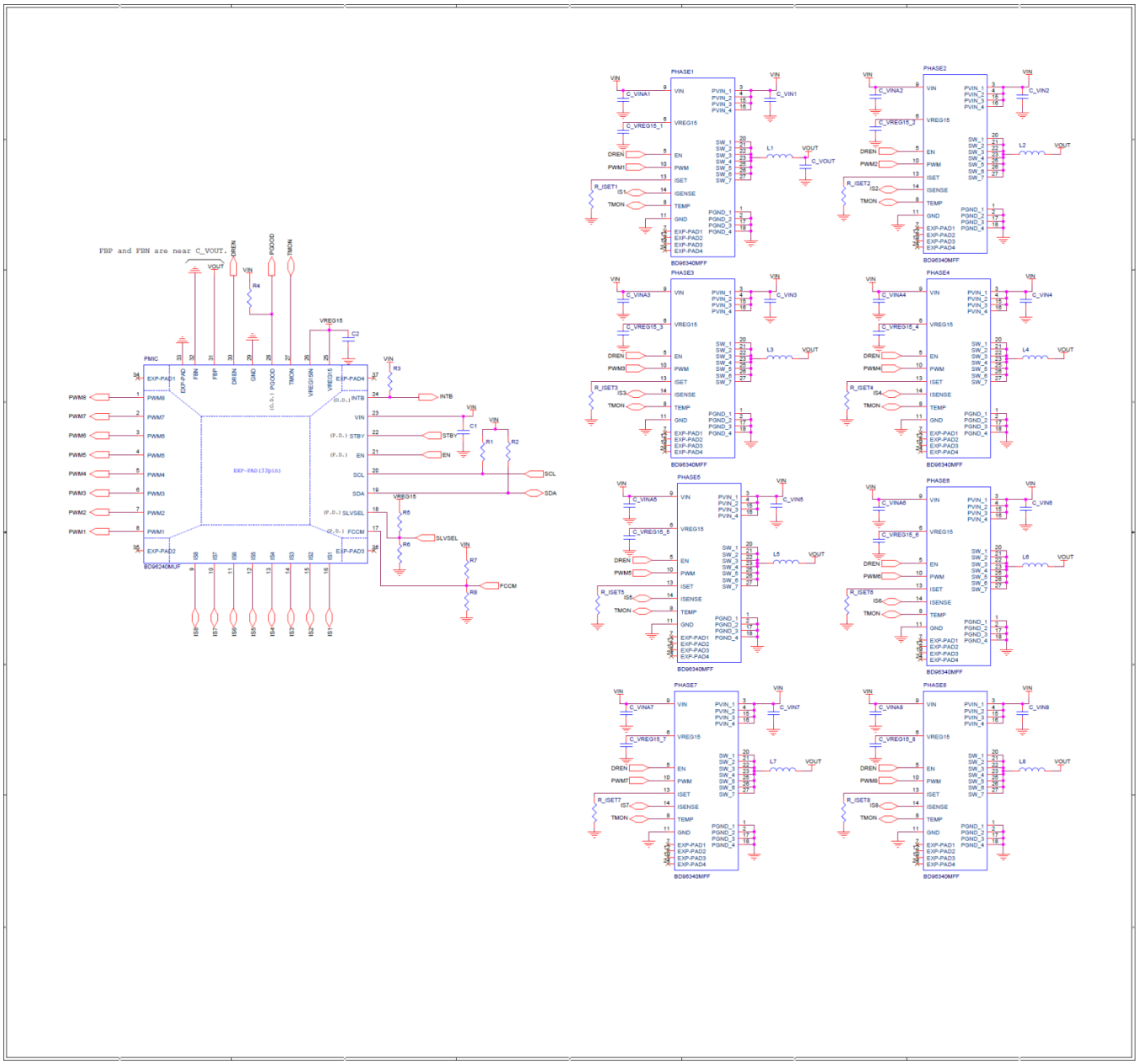


Figure 42. Application Circuit

Application Example – continued

Table 11. Application Circuit Components List

Parts name	Value			UNIT	Vendor	Parts Number	Size (mm)
	MIN(*1)	TYP	MAX				
C1	-	10	-	µF	TDK	CGA4J1X7S1C106K	2012
C2	-	1	2.2	µF	TDK	CGA2B1X7T0G105M	1005
C_VINA1, C_VINA2, C_VINA3, C_VINA4, C_VINA5, C_VINA6, C_VINA7, C_VINA8,	-	10	-	µF	TDK	CGA4J1X7S1C106K	2012
C_VIN1, C_VIN2, C_VIN3, C_VIN4, C_VIN5, C_VIN6, C_VIN7, C_VIN8,	-	10 x 2	-	µF	TDK	CGA4J1X7S1C106K	2012
C_VREG15_1, C_VREG15_2, C_VREG15_3, C_VREG15_4, C_VREG15_5, C_VREG15_6, C_VREG15_7, C_VREG15_8,	-	1	2.2	µF	TDK	CGA2B1X7T0G105M	1005
C_VOUT	-	300(*2)	-	µF	TDK	CGA3E1X7T0G106M	1608
L1, L2, L3, L4, L5, L6, L7, L8,	-	47	-	nH	-	-	-
R1, R2	-	1	-	kΩ	Rohm	MCR01MZPJ102	1005
R3, R4	-	10	-	kΩ	Rohm	MCR01MZPJ103	1005
R5 or R6	-	10	-	kΩ	Rohm	MCR01MZPJ103	1005
R7 or R8	-	10	-	kΩ	Rohm	MCR01MZPJ103	1005
R_ISET1, R_ISET2, R_ISET3, R_ISET4, R_ISET5, R_ISET6, R_ISET7, R_ISET8,	-	12(*3)	-	kΩ	Rohm	MCR01MZPD1202	1005

(*1) Set in consideration of temperature properties and DC bias properties not to become less than the minimum.
Consider it based on enough evaluations with the actual model.
(*2) Value per 1phase. Contact ROHM FAE for the most appropriate value with your application.
(*3) Refer to BD96340MFF-C datasheet to adjust this resistor. This resistor is 0.5 % accuracy.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

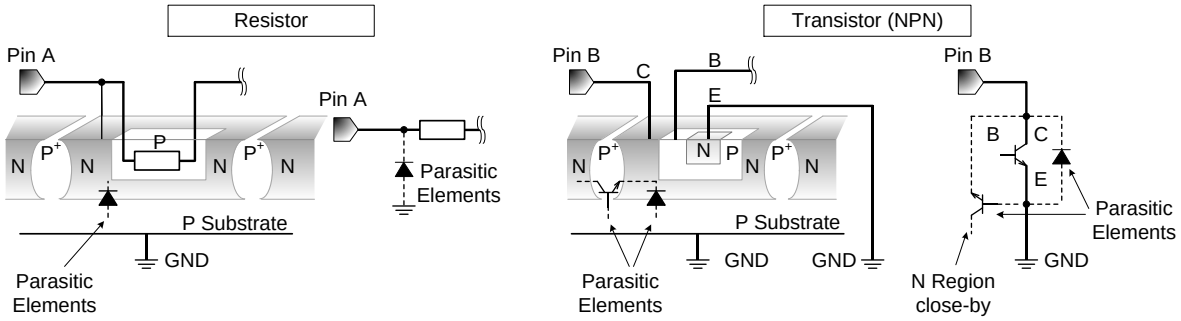


Figure 43. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

15. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

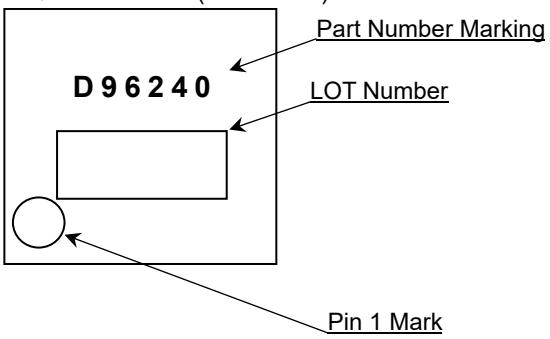
B	D	9	6	2	4	0	M	U	F	-	C E 2

Package
MUF: VQFN32FBV050

Product Rank
C: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

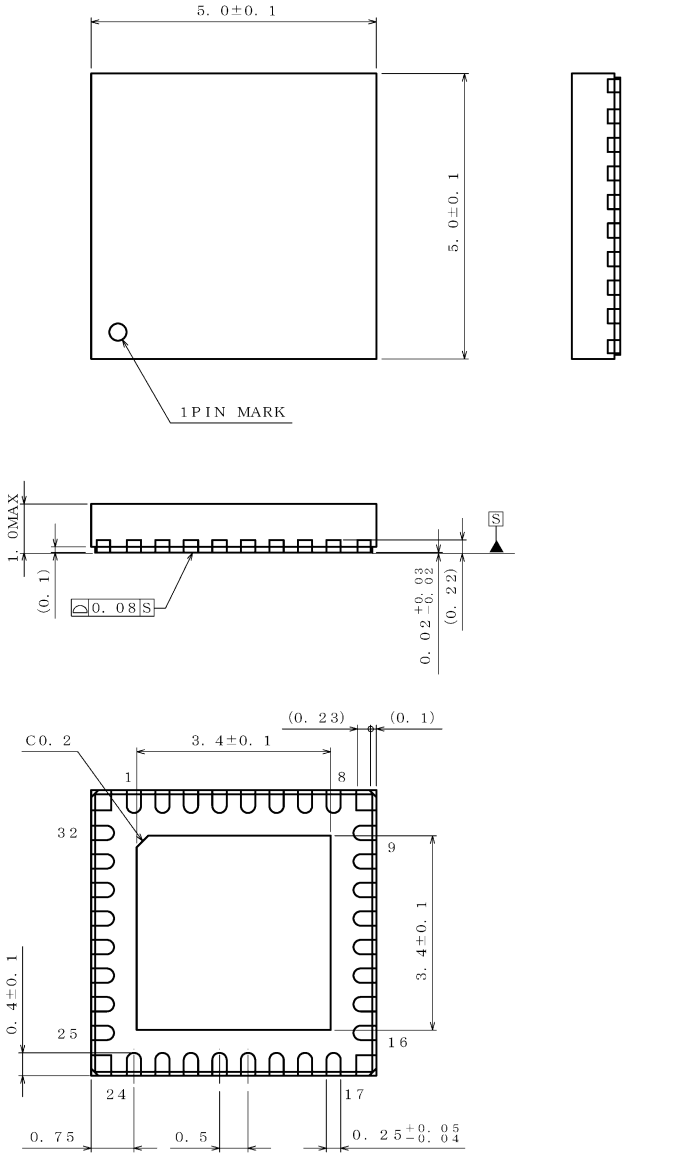
Marking Diagram

VQFN32FBV050 (TOP VIEW)



Physical Dimension and Packing Information

Package Name	VQFN32FBV050



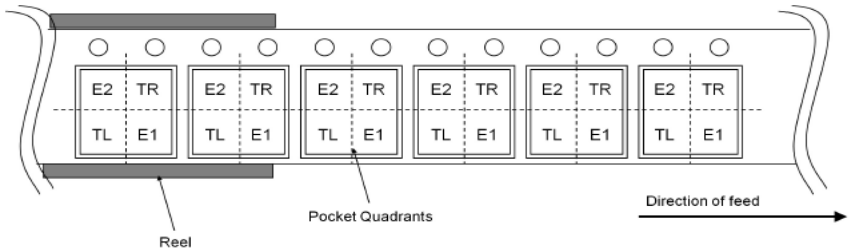
(UNIT : mm)

PKG : VQFN32FBV050
Drawing No. EX416-5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
29.Mar.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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