Capacitive Switch Controller ICs

Capacitive Switch Controller IC

BU21181FS

General Description

BU21181FS is a capacitive switch controller that detects capacitance change and judges the operation of Switch ON / OFF or Long Press. The function to prevent false detection of water enables it to be used at places using water.

Features

- 18 Capacitive Sensor Pins
- Switch ON / OFF / Long Press Detection
- Inform Detection Results by Interrupt Pin
- Prevention False Detection by Water
- Noise Calibration Function
- Drift Calibration Function
- Adjust Sampling Period Function
- 2-wire Serial Bus Interface
- Single Power Supply

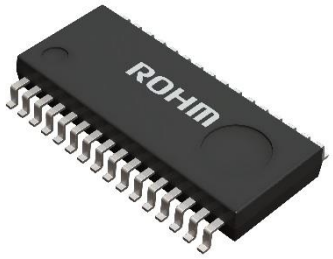
Applications

- Home Appliance such as IH Cooker, Refrigerator and Rice Cooker
- AV Appliance such as TV and HDD Recorder
- Office Automation Appliance such as Printer
- Electrical Equipment with Multiple Switches

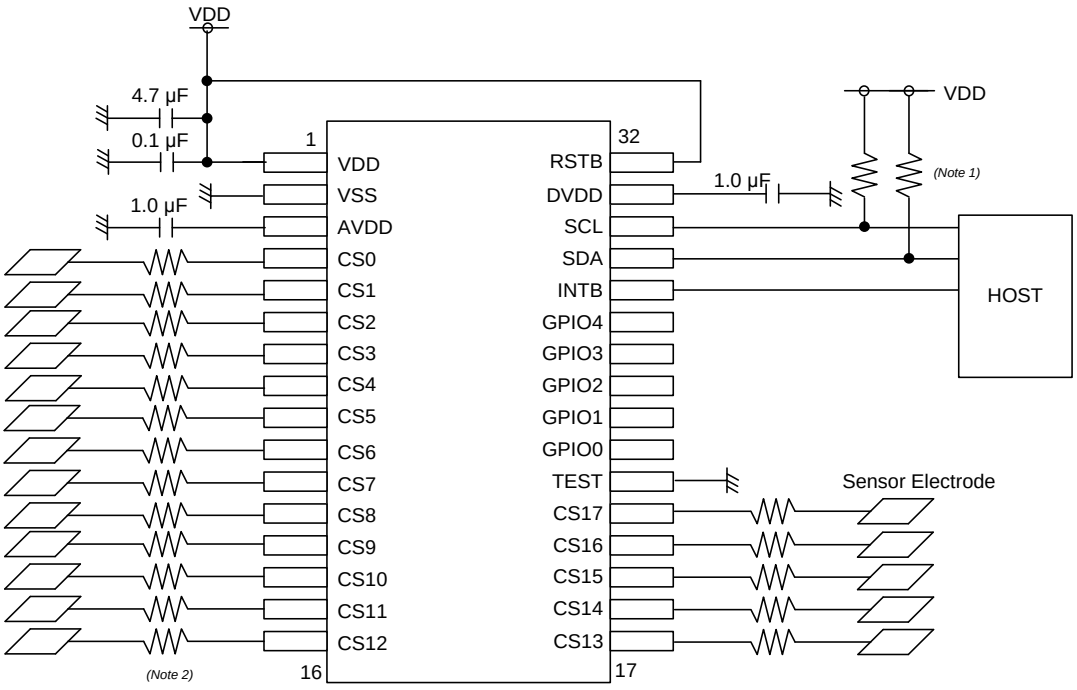
Key Specifications

- Power Supply Voltage Range: 3.0 V to 5.5 V
- Operating Temperature Range: -25 °C to +85 °C
- Operating Current: 2.5 mA (Typ)

Package	W (Typ) x D (Typ) x H (Max)
SSOP-A32	13.6 mm x 7.8 mm x 2.01 mm



Typical Application Circuit

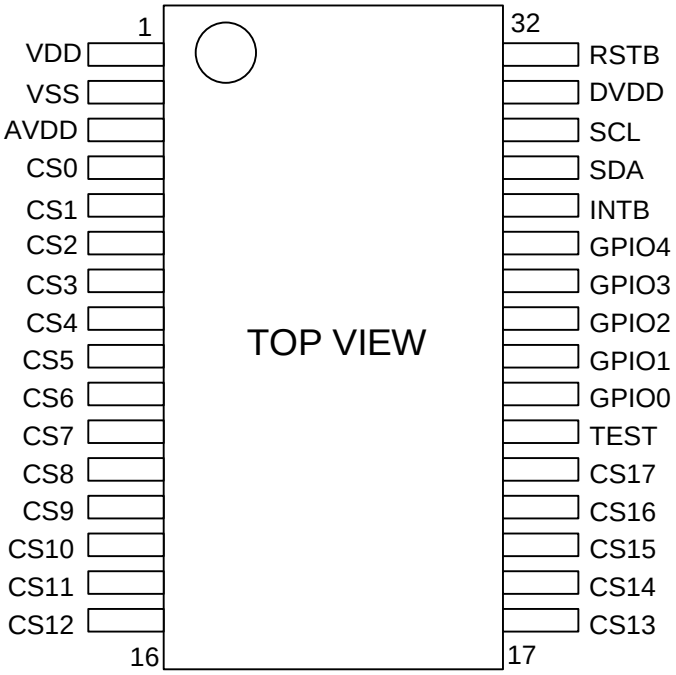


(Note 1) The pull-up resistors for the SDA and SCL pins must be connected to VDD.
Choose the value of the pull-up resistors so as to meet 2-wire Serial Bus Interface Electrical Characteristics.
(Note 2) The resistors on sensor lines are for noise countermeasure, choose the value of the resistors by evaluation.

○Product structure: Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration



Pin Description

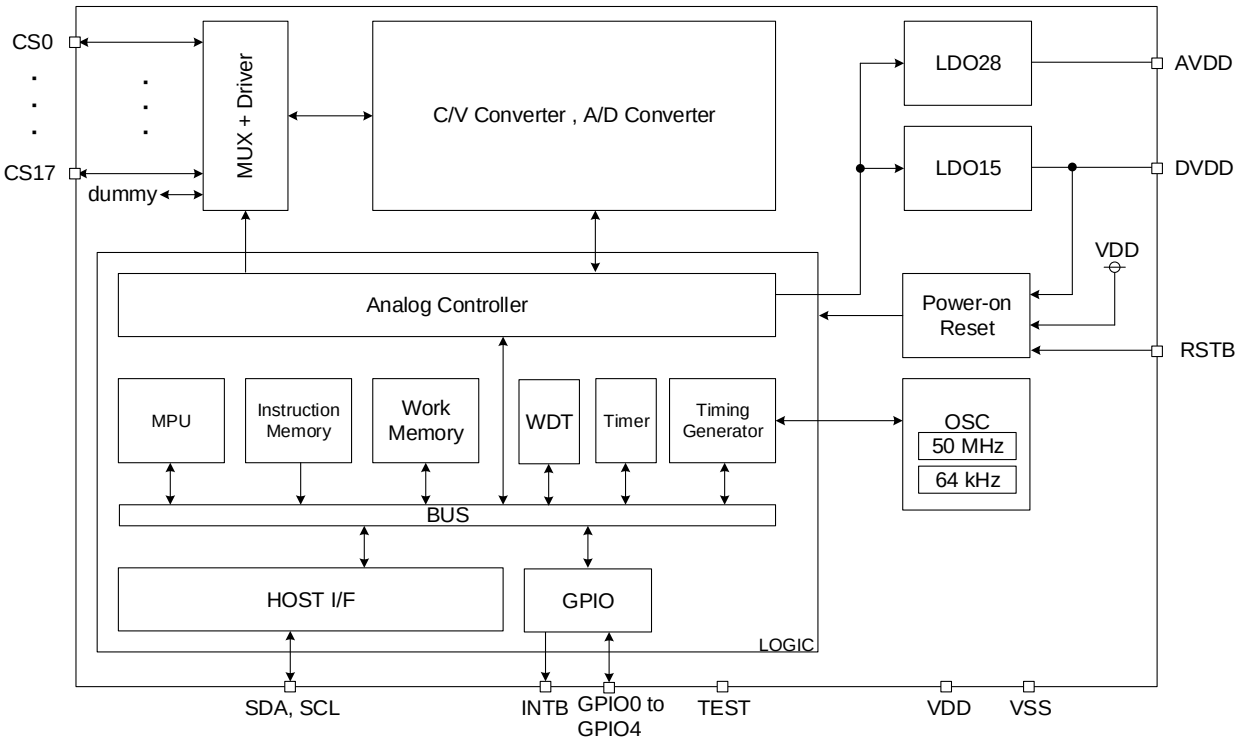
Pin No.	Pin Name	I/O Type	Function	Power	Initial Condition (RSTB = Low)
1	VDD	-	Power	-	-
2	VSS	-	Ground	-	-
3	AVDD	OUT	LDO pin for sensor block	-	0 V
4	CS0	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
5	CS1	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
6	CS2	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
7	CS3	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
8	CS4	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
9	CS5	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
10	CS6	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
11	CS7	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
12	CS8	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
13	CS9	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
14	CS10	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
15	CS11	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
16	CS12	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
17	CS13	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
18	CS14	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ

Pin Description - continued

Pin No.	Pin Name	I/O Type	Function	Power	Initial Condition (RSTB = Low)
19	CS15	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
20	CS16	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
21	CS17	IN/OUT	Sensor pin*(Note 3)*	AVDD	HIZ
22	TEST	IN	Test pin Connect to ground.	VDD	Low
23	GPIO0	IN/OUT	GPIO pin	VDD	Pull-up
24	GPIO1	IN/OUT	GPIO pin	VDD	Pull-up
25	GPIO2	IN/OUT	GPIO pin	VDD	Pull-up
26	GPIO3	IN/OUT	GPIO pin	VDD	Pull-up
27	GPIO4	IN/OUT	GPIO pin	VDD	Pull-up
28	INTB	OUT	Interrupt pin Active low interrupt	VDD	High
29	SDA	IN/OUT	Host interface pin: Serial data line	VDD	HIZ
30	SCL	IN/OUT	Host interface pin: Serial clock line	VDD	HIZ
31	DVDD	OUT	LDO pin for digital block	-	0 V
32	RSTB	IN	Reset pin Active low reset	VDD	Low

(Note 3) If not used, this pin must be left as an open circuit.

Block Diagram



Description of Block

MUX, Driver, C/V Converter, A/D Converter
This block converts from capacitance to voltage and the voltage to digital value.

LDO28
This block is LDO that supplies 2.8 V to MUX, Driver, C/V Converter and A/D Converter. Referred to as AVDD in this datasheet.

LDO15
This block is LDO that supplies 1.5 V to OSC and LOGIC. Referred to as DVDD in this datasheet.

OSC
This block supplies system clock. It consists of two oscillators which are 50 MHz and 64 kHz.

Power-on Reset
This block is Power-on Reset circuit. It supplies system reset.

MPU
This block determines states of switches based on the detection value. The detection results are informed to the host by the INTB pin.

Instruction Memory
This block is Program ROM for MPU.

Work Memory
This block is Working RAM for MPU.

HOST I/F
2-wire serial bus interface compatible with I^2C protocol.

Analog Controller
This block is a control sequencer for MUX, Driver, C/V Converter and A/D Converter.

WDT
This block is a watchdog timer. When WDT is not cleared by MPU, it supplies system reset.

Description of Block - continued

Timing Generator
This block generates clock for MPU peripherals based on OSC clock.

GPIO
Support Tact Switch input, output of switch detection result, etc.

Timer
Measure the time for intermittent sensing, periodical calibration, Long Press, etc.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Terminal Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Maximum Junction Temperature	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
SSOP-A32				
Junction to Ambient	θ_{JA}	82.9	45.2	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	6	6	°C/W

(Note 4) Based on JESD51-2A(Still-Air)
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.
(Note 7) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.0	5.0	5.5	V
Operating Temperature	Topr	-25	+25	+85	°C

Electrical Characteristics (Unless otherwise specified V_{DD} = 5.0 V, Ta = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage	V_{IH}	V_{DD} x 0.7	-	V_{DD} + 0.3	V	-
Input Low Voltage	V_{IL}	V_{SS} - 0.3	-	V_{DD} x 0.3	V	-
Output High Voltage	V_{OHCS}	V_{AVDD} x 0.7	-	V_{AVDD}	V	I_{OH} = -1 mA (The CSm pin (m = 0 to 17))
	V_{OH1}	V_{DD} x 0.7		V_{DD}	V	I_{OH} = -6 mA (The INTB/GPIOn pin (n = 0 to 4))
Output Low Voltage	V_{OLCS}	V_{SS}	-	V_{AVDD} x 0.3	V	I_{OL} = +1 mA (The CSm pin (m = 0 to 17))
	V_{OL1}	V_{SS}	-	V_{SS} + 0.4	V	I_{OL} = +3 mA (The SDA/SCL/INTB/GPIOn pin (n = 0 to 4))
	V_{OL2}	V_{SS}	-	V_{SS} + 0.6	V	I_{OL} = +6 mA (The SDA/SCL/INTB/GPIOn pin (n = 0 to 4))
Pull-up Resistor	R_{PU}	25	50	100	kΩ	GPIOn pin (n = 0 to 4)
Oscillator Clock Frequency	f_{OSC}	42.5	50.0	57.5	MHz	-
DVDD LDO Output Voltage	V_{DVDD}	1.35	1.50	1.65	V	-
AVDD LDO Output Voltage	V_{AVDD}	2.67	2.80	2.93	V	-
Standby Current	I_{STBY}	-	-	5	μA	RSTB = Low
Operating Current at Intermittent Sensing	I_{ACTI}	50	80	120	μA	Non-sensing period current.
Operating Current at Normal Sensing	I_{ACTN}	1.8	2.5	3.5	mA	Sensor pins: No load. No using Capacitance Cancel Drive.

Interface Specification

2-wire Serial Bus Interface
Compatible with I^2C Protocol
Support Slave Mode Only
7-bit Slave Address = 0x6C
Support Sequential Read
Clock Stretching (the SCL pin drive Low) while MPU receives the Interrupts

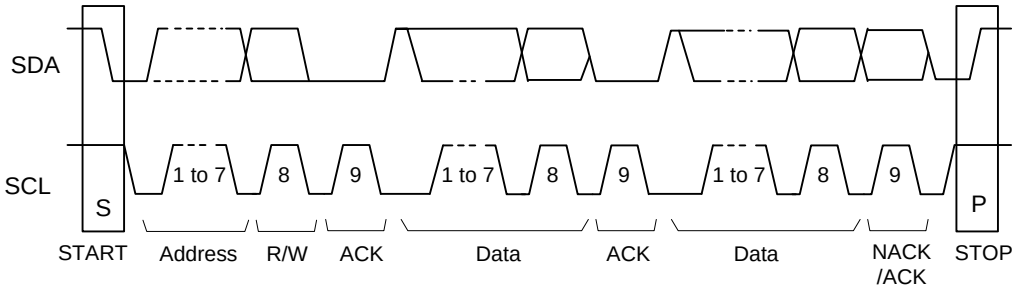


Figure 1. 2-wire Serial Bus Data Format

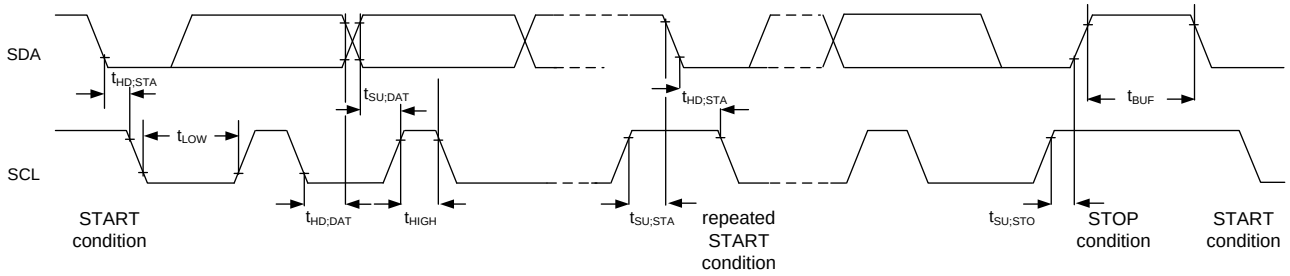


Figure 2. 2-wire Serial Bus Data Timing Chart

2-wire Serial Bus Interface Electrical Characteristics (Unless otherwise specified V_{DD} = 5.0 V, Ta = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
SCL Clock Frequency	f_{SCL}	0	-	400	kHz	-
Hold Time (repeated) START Condition	$t_{HD;STA}$	0.6	-	-	µs	-
Low Period of the SCL Clock	t_{LOW}	1.3	-	-	µs	-
High Period of the SCL Clock	t_{HIGH}	0.6	-	-	µs	-
Data Hold Time	$t_{HD;DAT}$	0	-	-	µs	-
Data Set-up Time	$t_{SU;DAT}$	0.1	-	-	µs	-
Set-up Time for a Repeated START Condition	$t_{SU;STA}$	0.6	-	-	µs	-
Set-up Time for STOP Condition	$t_{SU;STO}$	0.6	-	-	µs	-
Bus Free Time between STOP and START Condition	t_{BUF}	1.3	-	-	µs	-

Interface Specification - continued

2-wire Serial Bus Protocol

Write Protocol

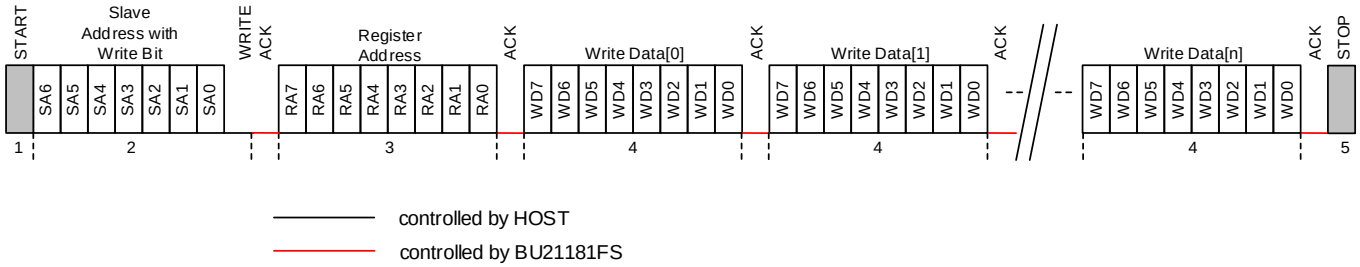


Figure 3. 2-wire Serial Bus Write Protocol

1: The communication starts when the START condition is sent.
2: 7-bit slave address and a write bit are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
3: 8-bit write register address are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
4: 8-bit write data are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing. IC supports sequential write. So the register address is incremented, and the next of 0xFF becomes 0x00.
5: The communication finishes when the STOP condition is sent.

Read Protocol

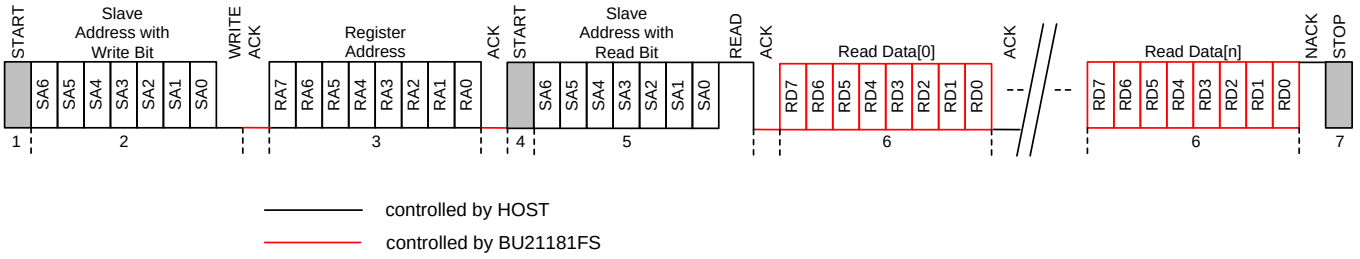


Figure 4. 2-wire Serial Bus Read Protocol

1: The communication starts when the START condition is sent.
2: 7-bit slave address and a write bit are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
3: 8-bit read register address are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
4: The communication continues when the START condition is sent.
5: 7-bit slave address and a read bit are sent and ACK signal is transmitted. IC carries out processing by MPU after the transmission of ACK signal. Clock stretch is carried out during the processing.
6: 8-bit read data is transmitted and ACK signal (if continue read) or NACK signal (if not continue read) is sent. IC carries out processing by MPU after sending of ACK/NACK signal. Clock stretch is carried out during the processing. IC supports sequential read. So the register address is incremented, and the next of 0xFF becomes 0x00.
7: The communication finishes when the STOP condition is sent.

Power-on Sequence / Reset Timing

Built-in LDO (DVDD) boots by setting the RSTB pin from low to high after VDD power is supplied. After DVDD booted, IC is accessible from the host after initializing MPU. When the RSTB pin is connected to VDD, IC is accessible from the host after initializing MPU at the built-in Power-on Reset circuit was released.

Power-on Flowchart

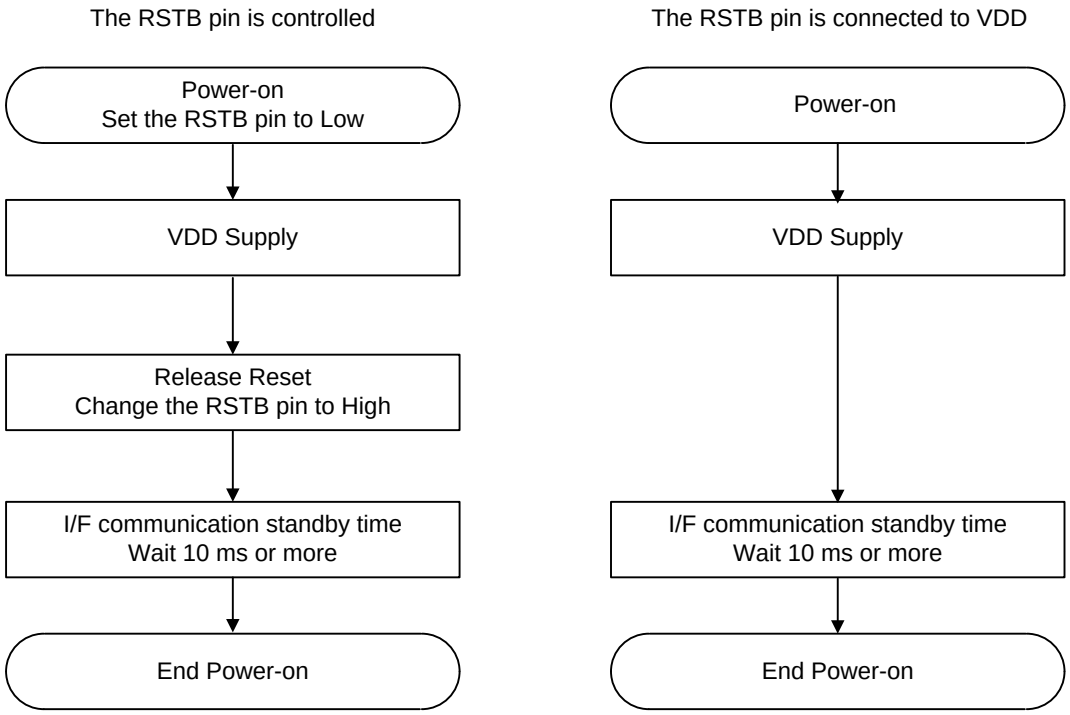


Figure 5. Power-on Flowchart

Power-on Timing

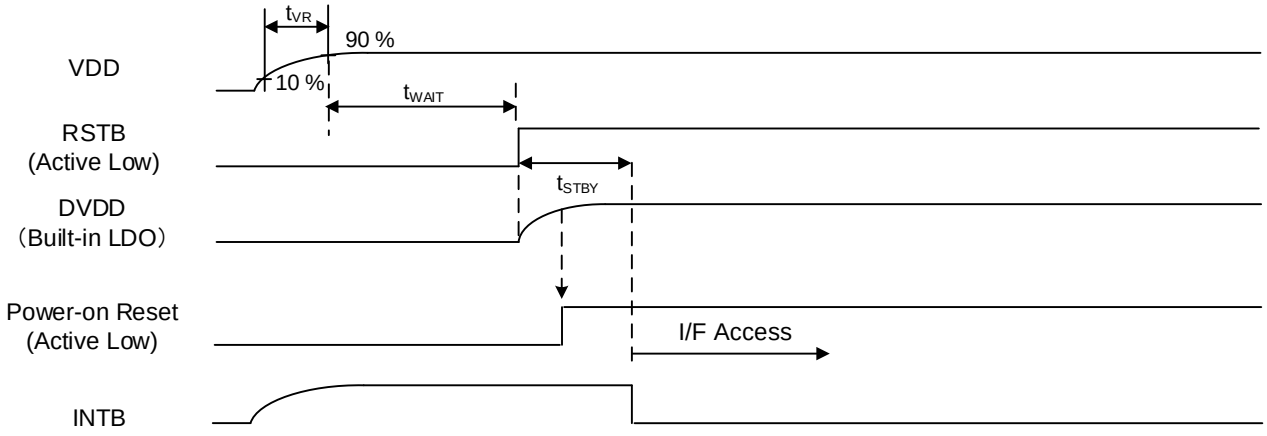


Figure 6. Power-on Timing Chart

Power-on Timing Characteristics (Unless otherwise specified V_{DD} = 5.0 V, Ta = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VDD Rise Time	t_{VR}	1	-	10	ms	-
RSTB Release Waiting Time	t_{WAIT}	1	-	-	ms	-
I/F Communication Standby Time	t_{STBY}	-	-	10	ms	-

Power-on Sequence / Reset Timing - continued

Power-restart Timing

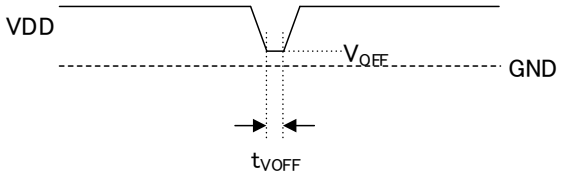


Figure 7. Power-restart Timing Chart

Power-restart Timing Characteristics (Unless otherwise specified V_{DD} = 5.0 V, Ta = 25 °C) *(Note 8)*

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Maximum Power-off Voltage	V_{OFF}	-	-	0.5	V	-
Minimum Restart Width	t_{VOFF}	20	-	-	ms	-

(Note 8) Power-on Reset is not guaranteed when the time of VDD ≤ 0.5 V is less than 20 ms at power restarting.

Reset Timing

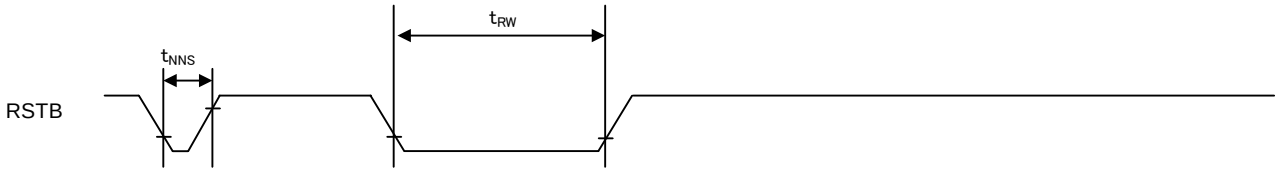


Figure 8. Reset Timing Chart

Reset Timing Characteristics (Unless otherwise specified V_{DD} = 5.0 V, Ta = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
RSTB Pulse Cancel Time	t_{NNS}	-	-	30	ns	-
RSTB Pulse Width	t_{RW}	1	-	-	µs	-

External Capacitor Specification

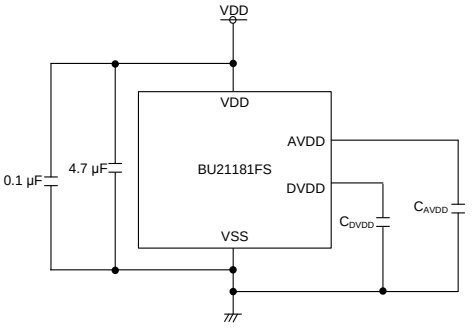


Figure 9. External Capacitor Circuit

External Capacitor Specification *(Note 9)*

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
AVDD Decoupling Capacitor	C_{AVDD}	0.6	1.0	2.0	µF	Ceramic capacitor recommended
DVDD Decoupling Capacitor	C_{DVDD}	0.6	1.0	2.0	µF	Ceramic capacitor recommended

(Note 9) Set the capacity of the capacitor not to be less than the minimum in consideration for characteristics of temperature, DC bias etc.

Register Map

The time setting in this datasheet is based on the value when the oscillator is typical (50 MHz).
The initial value is the value after initialization by MPU.
It is prohibited to write the different value from the initial value to reserved areas.
It is prohibited to write 1 to the bit written as 0 on this register map.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	R	0x00	VAL_SENS_CS0							
0x01	R	0x00	VAL_SENS_CS1							
0x02	R	0x00	VAL_SENS_CS2							
0x03	R	0x00	VAL_SENS_CS3							
0x04	R	0x00	VAL_SENS_CS4							
0x05	R	0x00	VAL_SENS_CS5							
0x06	R	0x00	VAL_SENS_CS6							
0x07	R	0x00	VAL_SENS_CS7							
0x08	R	0x00	VAL_SENS_CS8							
0x09	R	0x00	VAL_SENS_CS9							
0x0A	R	0x00	VAL_SENS_CS10							
0x0B	R	0x00	VAL_SENS_CS11							
0x0C	R	0x00	VAL_SENS_CS12							
0x0D	R	0x00	VAL_SENS_CS13							
0x0E	R	0x00	VAL_SENS_CS14							
0x0F	R	0x00	VAL_SENS_CS15							
0x10	R	0x00	VAL_SENS_CS16							
0x11	R	0x00	VAL_SENS_CS17							
0x12	R	0x00	Reserved							
0x13	R	0x19	Reserved							
0x14	R	0x00	MONI_OUT_CS0[15:8]							
0x15	R	0x00	MONI_OUT_CS0[7:0]							
0x16	R	0x00	MONI_OUT_CS1[15:8]							
0x17	R	0x00	MONI_OUT_CS1[7:0]							
0x18	R	0x00	MONI_OUT_CS2[15:8]							
0x19	R	0x00	MONI_OUT_CS2[7:0]							
0x1A	R	0x00	MONI_OUT_CS3[15:8]							
0x1B	R	0x00	MONI_OUT_CS3[7:0]							
0x1C	R	0x00	MONI_OUT_CS4[15:8]							
0x1D	R	0x00	MONI_OUT_CS4[7:0]							
0x1E	R	0x00	MONI_OUT_CS5[15:8]							
0x1F	R	0x00	MONI_OUT_CS5[7:0]							
0x20	R	0x00	MONI_OUT_CS6[15:8]							
0x21	R	0x00	MONI_OUT_CS6[7:0]							
0x22	R	0x00	MONI_OUT_CS7[15:8]							
0x23	R	0x00	MONI_OUT_CS7[7:0]							
0x24	R	0x00	MONI_OUT_CS8[15:8]							
0x25	R	0x00	MONI_OUT_CS8[7:0]							
0x26	R	0x00	MONI_OUT_CS9[15:8]							
0x27	R	0x00	MONI_OUT_CS9[7:0]							
0x28	R	0x00	MONI_OUT_CS10[15:8]							
0x29	R	0x00	MONI_OUT_CS10[7:0]							
0x2A	R	0x00	MONI_OUT_CS11[15:8]							
0x2B	R	0x00	MONI_OUT_CS11[7:0]							
0x2C	R	0x00	MONI_OUT_CS12[15:8]							
0x2D	R	0x00	MONI_OUT_CS12[7:0]							
0x2E	R	0x00	MONI_OUT_CS13[15:8]							
0x2F	R	0x00	MONI_OUT_CS13[7:0]							

Register Map - continued

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	R	0x00	MONI_OUT_CS14[15:8]							
0x31	R	0x00	MONI_OUT_CS14[7:0]							
0x32	R	0x00	MONI_OUT_CS15[15:8]							
0x33	R	0x00	MONI_OUT_CS15[7:0]							
0x34	R	0x00	MONI_OUT_CS16[15:8]							
0x35	R	0x00	MONI_OUT_CS16[7:0]							
0x36	R	0x00	MONI_OUT_CS17[15:8]							
0x37	R	0x00	MONI_OUT_CS17[7:0]							
0x38 to 0x39	R	0x00	Reserved							
0x3A	R	0x00	SW_STAT_CS7	SW_STAT_CS6	SW_STAT_CS5	SW_STAT_CS4	SW_STAT_CS3	SW_STAT_CS2	SW_STAT_CS1	SW_STAT_CS0
0x3B	R	0x00	SW_STAT_CS15	SW_STAT_CS14	SW_STAT_CS13	SW_STAT_CS12	SW_STAT_CS11	SW_STAT_CS10	SW_STAT_CS9	SW_STAT_CS8
0x3C	R	0x00	SW_STAT_EXT4	SW_STAT_EXT3	SW_STAT_EXT2	SW_STAT_EXT1	SW_STAT_EXT0	0	SW_STAT_CS17	SW_STAT_CS16
0x3D to 0x3F	R	0x00	Reserved							
0x40	R	0x01	INT_DET_NOISE	0	0	0	INT_FAL_CAL	INT_FIN_CAL	0	INT_FIN_INI
0x41	R	0x00	DINFO_B	DINFO_A	INT_MLT_OFF	INT_MLT_ON	INT_HLDRPT	INT_HLD	INT_SW_OFF	INT_SW_ON
0x42	R	0x00	DET_ON_CS7	DET_ON_CS6	DET_ON_CS5	DET_ON_CS4	DET_ON_CS3	DET_ON_CS2	DET_ON_CS1	DET_ON_CS0
0x43	R	0x00	DET_ON_CS15	DET_ON_CS14	DET_ON_CS13	DET_ON_CS12	DET_ON_CS11	DET_ON_CS10	DET_ON_CS9	DET_ON_CS8
0x44	R	0x00	DET_ON_EXT4	DET_ON_EXT3	DET_ON_EXT2	DET_ON_EXT1	DET_ON_EXT0	0	DET_ON_CS17	DET_ON_CS16
0x45	R	0x00	DET_OFF_CS7	DET_OFF_CS6	DET_OFF_CS5	DET_OFF_CS4	DET_OFF_CS3	DET_OFF_CS2	DET_OFF_CS1	DET_OFF_CS0
0x46	R	0x00	DET_OFF_CS15	DET_OFF_CS14	DET_OFF_CS13	DET_OFF_CS12	DET_OFF_CS11	DET_OFF_CS10	DET_OFF_CS9	DET_OFF_CS8
0x47	R	0x00	DET_OFF_EXT4	DET_OFF_EXT3	DET_OFF_EXT2	DET_OFF_EXT1	DET_OFF_EXT0	0	DET_OFF_CS17	DET_OFF_CS16
0x48	R	0x00	DET_HLD_CS7	DET_HLD_CS6	DET_HLD_CS5	DET_HLD_CS4	DET_HLD_CS3	DET_HLD_CS2	DET_HLD_CS1	DET_HLD_CS0
0x49	R	0x00	DET_HLD_CS15	DET_HLD_CS14	DET_HLD_CS13	DET_HLD_CS12	DET_HLD_CS11	DET_HLD_CS10	DET_HLD_CS9	DET_HLD_CS8
0x4A	R	0x00	DET_HLD_EXT4	DET_HLD_EXT3	DET_HLD_EXT2	DET_HLD_EXT1	DET_HLD_EXT0	0	DET_HLD_CS17	DET_HLD_CS16
0x4B	R	0x00	DET_HLDRPT_CS7	DET_HLDRPT_CS6	DET_HLDRPT_CS5	DET_HLDRPT_CS4	DET_HLDRPT_CS3	DET_HLDRPT_CS2	DET_HLDRPT_CS1	DET_HLDRPT_CS0
0x4C	R	0x00	DET_HLDRPT_CS15	DET_HLDRPT_CS14	DET_HLDRPT_CS13	DET_HLDRPT_CS12	DET_HLDRPT_CS11	DET_HLDRPT_CS10	DET_HLDRPT_CS9	DET_HLDRPT_CS8
0x4D	R	0x00	DET_HLDRPT_EXT4	DET_HLDRPT_EXT3	DET_HLDRPT_EXT2	DET_HLDRPT_EXT1	DET_HLDRPT_EXT0	0	DET_HLDRPT_CS17	DET_HLDRPT_CS16
0x4E	R	0x00	0	0	0	0	0	DET_MLT_ON_PC	DET_MLT_ON_PB	DET_MLT_ON_PA
0x4F	R	0x00	0	0	0	0	0	DET_MLT_OFF_PC	DET_MLT_OFF_PB	DET_MLT_OFF_PA

Register Map - continued

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x50	R	0x00	DINFO_X[7:0]							
0x51	R	0x00	DINFO_X[15:8]							
0x52	R	0x00	DINFO_X[23:16]							
0x53	R	0x00	DINFO_Y[7:0]							
0x54	R	0x00	DINFO_Y[15:8]							
0x55	R	0x00	DINFO_Y[23:16]							
0x56	R	0x00	FAL_CAL_CS7	FAL_CAL_CS6	FAL_CAL_CS5	FAL_CAL_CS4	FAL_CAL_CS3	FAL_CAL_CS2	FAL_CAL_CS1	FAL_CAL_CS0
0x57	R	0x00	FAL_CAL_CS15	FAL_CAL_CS14	FAL_CAL_CS13	FAL_CAL_CS12	FAL_CAL_CS11	FAL_CAL_CS10	FAL_CAL_CS9	FAL_CAL_CS8
0x58	R	0x00	0	0	0	0	0	0	FAL_CAL_CS17	FAL_CAL_CS16
0x59	R	0x00	0	0	0	0	0	SLEEP	RUN_CAL	RUN_AFE
0x5A	R	0x00	SENS_STAT_CS7	SENS_STAT_CS6	SENS_STAT_CS5	SENS_STAT_CS4	SENS_STAT_CS3	SENS_STAT_CS2	SENS_STAT_CS1	SENS_STAT_CS0
0x5B	R	0x00	SENS_STAT_CS15	SENS_STAT_CS14	SENS_STAT_CS13	SENS_STAT_CS12	SENS_STAT_CS11	SENS_STAT_CS10	SENS_STAT_CS9	SENS_STAT_CS8
0x5C	R	0x00	SENS_STAT_EXT4	SENS_STAT_EXT3	SENS_STAT_EXT2	SENS_STAT_EXT1	SENS_STAT_EXT0	0	SENS_STAT_CS17	SENS_STAT_CS16
0x5D	R	0x00	RINFO[7:0]							
0x5E	R	0x00	RINFO[15:8]							
0x5F	R	0x00	RINFO[23:16]							
0x60	R/W	0x33	0	SINFO_W1	CCD_CS1	RX_CS1	0	SINFO_W0	CCD_CS0	RX_CS0
0x61	R/W	0x33	0	SINFO_W3	CCD_CS3	RX_CS3	0	SINFO_W2	CCD_CS2	RX_CS2
0x62	R/W	0x33	0	SINFO_W5	CCD_CS5	RX_CS5	0	SINFO_W4	CCD_CS4	RX_CS4
0x63	R/W	0x33	0	SINFO_W7	CCD_CS7	RX_CS7	0	SINFO_W6	CCD_CS6	RX_CS6
0x64	R/W	0x33	0	SINFO_W9	CCD_CS9	RX_CS9	0	SINFO_W8	CCD_CS8	RX_CS8
0x65	R/W	0x33	0	SINFO_W11	CCD_CS11	RX_CS11	0	SINFO_W10	CCD_CS10	RX_CS10
0x66	R/W	0x33	0	SINFO_W13	CCD_CS13	RX_CS13	0	SINFO_W12	CCD_CS12	RX_CS12
0x67	R/W	0x33	0	SINFO_W15	CCD_CS15	RX_CS15	0	SINFO_W14	CCD_CS14	RX_CS14
0x68	R/W	0x33	0	SINFO_W17	CCD_CS17	RX_CS17	0	SINFO_W16	CCD_CS16	RX_CS16
0x69	R/W	0x00	Reserved							
0x6A	R/W	0x8E	VAL_TH_ON_CS0				VAL_GAIN_CS0			
0x6B	R/W	0x8E	VAL_TH_ON_CS1				VAL_GAIN_CS1			
0x6C	R/W	0x8E	VAL_TH_ON_CS2				VAL_GAIN_CS2			
0x6D	R/W	0x8E	VAL_TH_ON_CS3				VAL_GAIN_CS3			
0x6E	R/W	0x8E	VAL_TH_ON_CS4				VAL_GAIN_CS4			
0x6F	R/W	0x8E	VAL_TH_ON_CS5				VAL_GAIN_CS5			
0x70	R/W	0x8E	VAL_TH_ON_CS6				VAL_GAIN_CS6			
0x71	R/W	0x8E	VAL_TH_ON_CS7				VAL_GAIN_CS7			
0x72	R/W	0x8E	VAL_TH_ON_CS8				VAL_GAIN_CS8			
0x73	R/W	0x8E	VAL_TH_ON_CS9				VAL_GAIN_CS9			
0x74	R/W	0x8E	VAL_TH_ON_CS10				VAL_GAIN_CS10			
0x75	R/W	0x8E	VAL_TH_ON_CS11				VAL_GAIN_CS11			
0x76	R/W	0x8E	VAL_TH_ON_CS12				VAL_GAIN_CS12			
0x77	R/W	0x8E	VAL_TH_ON_CS13				VAL_GAIN_CS13			
0x78	R/W	0x8E	VAL_TH_ON_CS14				VAL_GAIN_CS14			
0x79	R/W	0x8E	VAL_TH_ON_CS15				VAL_GAIN_CS15			
0x7A	R/W	0x8E	VAL_TH_ON_CS16				VAL_GAIN_CS16			
0x7B	R/W	0x8E	VAL_TH_ON_CS17				VAL_GAIN_CS17			
0x7C	R/W	0x00	Reserved							
0x7D	R/W	0x40	VAL_TH_OFF				0	0	0	0
0x7E to 0x7F	R/W	0x00	Reserved							

Register Map - continued

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x80	R/W	0x00	SINFO_A							
0x81	R/W	0x00	SINFO_B							
0x82	R/W	0x00	SINFO_C							
0x83 to 0x85	R/W	0x00	Reserved							
0x86	R	0x00	DET_CAL_CS7	DET_CAL_CS6	DET_CAL_CS5	DET_CAL_CS4	DET_CAL_CS3	DET_CAL_CS2	DET_CAL_CS1	DET_CAL_CS0
0x87	R	0x00	DET_CAL_CS15	DET_CAL_CS14	DET_CAL_CS13	DET_CAL_CS12	DET_CAL_CS11	DET_CAL_CS10	DET_CAL_CS9	DET_CAL_CS8
0x88	R	0x00	CAL_NOISE	CAL_OFS	CAL_DRIFT	CAL_MINUS	0	0	DET_CAL_CS17	DET_CAL_CS16
0x89	R	0x00	SOFT_CAL_ERR_CS7	SOFT_CAL_ERR_CS6	SOFT_CAL_ERR_CS5	SOFT_CAL_ERR_CS4	SOFT_CAL_ERR_CS3	SOFT_CAL_ERR_CS2	SOFT_CAL_ERR_CS1	SOFT_CAL_ERR_CS0
0x8A	R	0x00	SOFT_CAL_ERR_CS15	SOFT_CAL_ERR_CS14	SOFT_CAL_ERR_CS13	SOFT_CAL_ERR_CS12	SOFT_CAL_ERR_CS11	SOFT_CAL_ERR_CS10	SOFT_CAL_ERR_CS9	SOFT_CAL_ERR_CS8
0x8B	R	0x00	0	0	0	0	0	0	SOFT_CAL_ERR_CS17	SOFT_CAL_ERR_CS16
0x8C to 0x9F	R/W	0x00	Reserved							
0xA0	R/W	0x00	MIN_FRAME_PERIOD							
0xA1	R/W	0x00	CHECK_PERIOD_IN_SLEEP							
0xA2	R/W	0x00	SLEEP_IN_TIME							
0xA3	R/W	0x00	SLEEP_OUT_TIME							
0xA4	R/W	0x00	HLD_DET_TIME							
0xA5	R/W	0x00	HLDRPT_DET_TIME							
0xA6	R/W	0x00	MLT_DET_TIME							
0xA7	R/W	0x00	MLT_PA_CS7	MLT_PA_CS6	MLT_PA_CS5	MLT_PA_CS4	MLT_PA_CS3	MLT_PA_CS2	MLT_PA_CS1	MLT_PA_CS0
0xA8	R/W	0x00	MLT_PA_CS15	MLT_PA_CS14	MLT_PA_CS13	MLT_PA_CS12	MLT_PA_CS11	MLT_PA_CS10	MLT_PA_CS9	MLT_PA_CS8
0xA9	R/W	0x00	0	0	0	0	0	0	MLT_PA_CS17	MLT_PA_CS16
0xAA	R/W	0x00	MLT_PB_CS7	MLT_PB_CS6	MLT_PB_CS5	MLT_PB_CS4	MLT_PB_CS3	MLT_PB_CS2	MLT_PB_CS1	MLT_PB_CS0
0xAB	R/W	0x00	MLT_PB_CS15	MLT_PB_CS14	MLT_PB_CS13	MLT_PB_CS12	MLT_PB_CS11	MLT_PB_CS10	MLT_PB_CS9	MLT_PB_CS8
0xAC	R/W	0x00	0	0	0	0	0	0	MLT_PB_CS17	MLT_PB_CS16
0xAD	R/W	0x00	MLT_PC_CS7	MLT_PC_CS6	MLT_PC_CS5	MLT_PC_CS4	MLT_PC_CS3	MLT_PC_CS2	MLT_PC_CS1	MLT_PC_CS0
0xAE	R/W	0x00	MLT_PC_CS15	MLT_PC_CS14	MLT_PC_CS13	MLT_PC_CS12	MLT_PC_CS11	MLT_PC_CS10	MLT_PC_CS9	MLT_PC_CS8
0xAF	R/W	0x00	0	0	0	0	0	0	MLT_PC_CS17	MLT_PC_CS16
0xB0	R/W	0x10	OST_EXT_SW				OST_SW			
0xB1	R/W	0x00	Reserved							
0xB2	R/W	0x02	FIL_IIR				0	0	FIL_MEDIAN	
0xB3	R/W	0x02	0	0	0	0	0	0	FREQ_AFE	
0xB4	R/W	0x03	Reserved							
0xB5	R/W	0x00	Reserved							
0xB6	R/W	0x27	0	0	SINFO_D	CAL_PERIOD_EN	CAL_OFS_EN	CAL_MINUS_EN	CAL_DRIFT_EN	CAL_NOISE_EN
0xB7	R/W	0x03	NUM_CS_DET_DRIFT							
0xB8	R/W	0x21	NUM_FRAME_CORRECT_OFS							
0xB9	R/W	0x00	GPIO_EXT_IN_POL	0	0	GPIO4_EXT_SW_IN	GPIO3_EXT_SW_IN	GPIO2_EXT_SW_IN	GPIO1_EXT_SW_IN	GPIO0_EXT_SW_IN
0xBA	R/W	0x00	0	0	0	GPIO4_REG_OUT	GPIO3_REG_OUT	GPIO2_REG_OUT	GPIO1_REG_OUT	GPIO0_REG_OUT
0xBB	R/W	0x00	GPIO_EXT_OUT_POL	0	0	GPIO4_CS4_SW_OUT	GPIO3_CS3_SW_OUT	GPIO2_CS2_SW_OUT	GPIO1_CS1_SW_OUT	GPIO0_CS0_SW_OUT

Register Map - continued

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBC	R/W	0x00	TIME_PERCAL							
0xBD	R/W	0x00	0	0	0	TIMOUT_SOFT_CALIB				
0xBE	R/W	0x01	NUM_CS_DET_NOISE							
0xBF	R/W	0x00	0	FMOD_EN	DET_NOISE_ FSFT_EN	MLT_EN	CAL_FAL_ FSFT_EN	0	SLEEP_ ADJ_OFS	SLEEP_EN
0xC0	R/W	0x00	HLD_EN_ CS7	HLD_EN_ CS6	HLD_EN_ CS5	HLD_EN_ CS4	HLD_EN_ CS3	HLD_EN_ CS2	HLD_EN_ CS1	HLD_EN_ CS0
0xC1	R/W	0x00	HLD_EN_ CS15	HLD_EN_ CS14	HLD_EN_ CS13	HLD_EN_ CS12	HLD_EN_ CS11	HLD_EN_ CS10	HLD_EN_ CS9	HLD_EN_ CS8
0xC2	R/W	0x00	HLD_EN_ EXT4	HLD_EN_ EXT3	HLD_EN_ EXT2	HLD_EN_ EXT1	HLD_EN_ EXT0	0	HLD_EN_ CS17	HLD_EN_ CS16
0xC3	R/W	0x00	HLDRPT_EN_ CS7	HLDRPT_EN_ CS6	HLDRPT_EN_ CS5	HLDRPT_EN_ CS4	HLDRPT_EN_ CS3	HLDRPT_EN_ CS2	HLDRPT_EN_ CS1	HLDRPT_EN_ CS0
0xC4	R/W	0x00	HLDRPT_EN_ CS15	HLDRPT_EN_ CS14	HLDRPT_EN_ CS13	HLDRPT_EN_ CS12	HLDRPT_EN_ CS11	HLDRPT_EN_ CS10	HLDRPT_EN_ CS9	HLDRPT_EN_ CS8
0xC5	R/W	0x00	HDLRPT_EN_ EXT4	HDLRPT_EN_ EXT3	HDLRPT_EN_ EXT2	HDLRPT_EN_ EXT1	HDLRPT_EN_ EXT0	0	HLDRPT_EN_ CS17	HLDRPT_EN_ CS16
0xC6 to 0xDD	R/W	0x00	Reserved							
0xDE	R/W	0x38	Reserved							
0xDF	R/W	0x00	Reserved							
0xE0	R/W	0x00	CLR_ FACT_CAL	0	0	0	CLR_ FAL_CAL	CLR_ FIN_CAL	0	CLR_ FIN_INI
0xE1	R/W	0x00	Reserved							
0xE2	R/W	0x00	CLR_DET_ ON_CS7	CLR_DET_ ON_CS6	CLR_DET_ ON_CS5	CLR_DET_ ON_CS4	CLR_DET_ ON_CS3	CLR_DET_ ON_CS2	CLR_DET_ _ON_CS1	CLR_DET_ _ON_CS0
0xE3	R/W	0x00	CLR_DET_ ON_CS15	CLR_DET_ ON_CS14	CLR_DET_ ON_CS13	CLR_DET_ ON_CS12	CLR_DET_ ON_CS11	CLR_DET_ ON_CS10	CLR_DET_ _ON_CS9	CLR_DET_ _ON_CS8
0xE4	R/W	0x00	CLR_DET_ ON_EXT4	CLR_DET_ ON_EXT3	CLR_DET_ ON_EXT2	CLR_DET_ ON_EXT1	CLR_DET_ ON_EXT0	0	CLR_DET_ _ON_CS17	CLR_DET_ _ON_CS16
0xE5	R/W	0x00	CLR_DET_ OFF_CS7	CLR_DET_ OFF_CS6	CLR_DET_ OFF_CS5	CLR_DET_ OFF_CS4	CLR_DET_ OFF_CS3	CLR_DET_ OFF_CS2	CLR_DET_ _OFF_CS1	CLR_DET_ _OFF_CS0
0xE6	R/W	0x00	CLR_DET_ OFF_CS15	CLR_DET_ OFF_CS14	CLR_DET_ OFF_CS13	CLR_DET_ OFF_CS12	CLR_DET_ OFF_CS11	CLR_DET_ OFF_CS10	CLR_DET_ _OFF_CS9	CLR_DET_ _OFF_CS8
0xE7	R/W	0x00	CLR_DET_ OFF_EXT4	CLR_DET_ OFF_EXT3	CLR_DET_ OFF_EXT2	CLR_DET_ OFF_EXT1	CLR_DET_ OFF_EXT0	0	CLR_DET_ _OFF_CS17	CLR_DET_ _OFF_CS16
0xE8	R/W	0x00	CLR_DET_ HLD_CS7	CLR_DET_ HLD_CS6	CLR_DET_ HLD_CS5	CLR_DET_ HLD_CS4	CLR_DET_ HLD_CS3	CLR_DET_ HLD_CS2	CLR_DET_ HLD_CS1	CLR_DET_ HLD_CS0
0xE9	R/W	0x00	CLR_DET_ HLD_CS15	CLR_DET_ HLD_CS14	CLR_DET_ HLD_CS13	CLR_DET_ HLD_CS12	CLR_DET_ HLD_CS11	CLR_DET_ HLD_CS10	CLR_DET_ HLD_CS9	CLR_DET_ HLD_CS8
0xEA	R/W	0x00	CLR_DET_ HLD_EXT4	CLR_DET_ HLD_EXT3	CLR_DET_ HLD_EXT2	CLR_DET_ HLD_EXT1	CLR_DET_ HLD_EXT0	0	CLR_DET_ HLD_CS17	CLR_DET_ HLD_CS16
0xEB	R/W	0x00	CLR_DET_ HLDRPT_CS7	CLR_DET_ HLDRPT_CS6	CLR_DET_ HLDRPT_CS5	CLR_DET_ HLDRPT_CS4	CLR_DET_ HLDRPT_CS3	CLR_DET_ HLDRPT_CS2	CLR_DET_ HLDRPT_CS1	CLR_DET_ HLDRPT_CS0
0xEC	R/W	0x00	CLR_DET_ HLDRPT_CS15	CLR_DET_ HLDRPT_CS14	CLR_DET_ HLDRPT_CS13	CLR_DET_ HLDRPT_CS12	CLR_DET_ HLDRPT_CS11	CLR_DET_ HLDRPT_CS10	CLR_DET_ HLDRPT_CS9	CLR_DET_ HLDRPT_CS8
0xED	R/W	0x00	CLR_DET_ HLDRPT_EXT4	CLR_DET_ HLDRPT_EXT3	CLR_DET_ HLDRPT_EXT2	CLR_DET_ HLDRPT_EXT1	CLR_DET_ HLDRPT_EXT0	0	CLR_DET_ HLDRPT_CS17	CLR_DET_ HLDRPT_CS16
0xEE	R/W	0x00	0	0	0	0	0	CLR_DET_ MLT_ON_PC	CLR_DET_ MLT_ON_PB	CLR_DET_ MLT_ON_PA
0xEF	R/W	0x00	0	0	0	0	0	CLR_DET_ MLT_OFF_PC	CLR_DET_ MLT_OFF_PB	CLR_DET_ MLT_OFF_PA
0xF0	R/W	0x00	CINFO_X[7:0]							
0xF1	R/W	0x00	CINFO_X[15:8]							
0xF2	R/W	0x00	CINFO_X[23:16]							
0xF3	R/W	0x00	CINFO_Y[7:0]							
0xF4	R/W	0x00	CINFO_Y[15:8]							
0xF5	R/W	0x00	CINFO_Y[23:16]							
0xF6	R/W	0x00	SWRST_H							
0xF7	R/W	0x00	SWRST_L							
0xF8 to 0xFC	R/W	0x00	Reserved							
0xFD	R/W	0x00	CINFO_Z							
0xFE	R/W	0x00	0	0	0	CNT_GPIO4	CNT_GPIO3	CNT_GPIO2	CNT_GPIO1	CNT_GPIO0
0xFF	R/W	0x00	0	0	0	0	0	SET	CAL	ACT

Register Description

0x00 to 0x11: Sensor Value

Name: VAL_SENS_CSm (m = 0 to 17)
Address: 0x00 to 0x11
Description: These registers show the value of each sensor compared with the value of ON threshold / OFF threshold.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	R	0x00	VAL_SENS_CS0							
0x01	R	0x00	VAL_SENS_CS1							
0x02	R	0x00	VAL_SENS_CS2							
0x03	R	0x00	VAL_SENS_CS3							
0x04	R	0x00	VAL_SENS_CS4							
0x05	R	0x00	VAL_SENS_CS5							
0x06	R	0x00	VAL_SENS_CS6							
0x07	R	0x00	VAL_SENS_CS7							
0x08	R	0x00	VAL_SENS_CS8							
0x09	R	0x00	VAL_SENS_CS9							
0x0A	R	0x00	VAL_SENS_CS10							
0x0B	R	0x00	VAL_SENS_CS11							
0x0C	R	0x00	VAL_SENS_CS12							
0x0D	R	0x00	VAL_SENS_CS13							
0x0E	R	0x00	VAL_SENS_CS14							
0x0F	R	0x00	VAL_SENS_CS15							
0x10	R	0x00	VAL_SENS_CS16							
0x11	R	0x00	VAL_SENS_CS17							

Register Description - continued

0x14 to 0x37: RAW Data

Name: MONI_OUT_CSm (m = 0 to 17)
Address: 0x14 to 0x37
Description: These registers show the detection value of each sensor.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	R	0x00	MONI_OUT_CS0[15:8]							
0x15	R	0x00	MONI_OUT_CS0[7:0]							
0x16	R	0x00	MONI_OUT_CS1[15:8]							
0x17	R	0x00	MONI_OUT_CS1[7:0]							
0x18	R	0x00	MONI_OUT_CS2[15:8]							
0x19	R	0x00	MONI_OUT_CS2[7:0]							
0x1A	R	0x00	MONI_OUT_CS3[15:8]							
0x1B	R	0x00	MONI_OUT_CS3[7:0]							
0x1C	R	0x00	MONI_OUT_CS4[15:8]							
0x1D	R	0x00	MONI_OUT_CS4[7:0]							
0x1E	R	0x00	MONI_OUT_CS5[15:8]							
0x1F	R	0x00	MONI_OUT_CS5[7:0]							
0x20	R	0x00	MONI_OUT_CS6[15:8]							
0x21	R	0x00	MONI_OUT_CS6[7:0]							
0x22	R	0x00	MONI_OUT_CS7[15:8]							
0x23	R	0x00	MONI_OUT_CS7[7:0]							
0x24	R	0x00	MONI_OUT_CS8[15:8]							
0x25	R	0x00	MONI_OUT_CS8[7:0]							
0x26	R	0x00	MONI_OUT_CS9[15:8]							
0x27	R	0x00	MONI_OUT_CS9[7:0]							
0x28	R	0x00	MONI_OUT_CS10[15:8]							
0x29	R	0x00	MONI_OUT_CS10[7:0]							
0x2A	R	0x00	MONI_OUT_CS11[15:8]							
0x2B	R	0x00	MONI_OUT_CS11[7:0]							
0x2C	R	0x00	MONI_OUT_CS12[15:8]							
0x2D	R	0x00	MONI_OUT_CS12[7:0]							
0x2E	R	0x00	MONI_OUT_CS13[15:8]							
0x2F	R	0x00	MONI_OUT_CS13[7:0]							
0x30	R	0x00	MONI_OUT_CS14[15:8]							
0x31	R	0x00	MONI_OUT_CS14[7:0]							
0x32	R	0x00	MONI_OUT_CS15[15:8]							
0x33	R	0x00	MONI_OUT_CS15[7:0]							
0x34	R	0x00	MONI_OUT_CS16[15:8]							
0x35	R	0x00	MONI_OUT_CS16[7:0]							
0x36	R	0x00	MONI_OUT_CS17[15:8]							
0x37	R	0x00	MONI_OUT_CS17[7:0]							

Register Description - continued

0x3A to 0x3C: Switch State

Name: SW_STAT_CSm (m = 0 to 17), SW_STAT_EXTn (n = 0 to 4)
Address: 0x3A to 0x3C
Description: These registers show the sensor recognized as Switch ON.

SW_STAT_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

SW_STAT_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

When Multi-Touch of switches is disabled (“Multi-Touch of Switches Function MLT_EN (register 0xBF[4])” = 0),
- The only one bit corresponding to the sensor recognized as Switch ON is set to 1
- The multiple bits matched to any of “Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)” and corresponding to the sensor recognized as Switch ON are set to 1

When Multi-Touch of switches is enabled (“Multi-Touch of Switches Function MLT_EN (register 0xBF[4])” = 1),
- The all bits corresponding to the sensor recognized as Switch ON are set to 1.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3A	R	0x00	SW_STAT_CS7	SW_STAT_CS6	SW_STAT_CS5	SW_STAT_CS4	SW_STAT_CS3	SW_STAT_CS2	SW_STAT_CS1	SW_STAT_CS0
0x3B	R	0x00	SW_STAT_CS15	SW_STAT_CS14	SW_STAT_CS13	SW_STAT_CS12	SW_STAT_CS11	SW_STAT_CS10	SW_STAT_CS9	SW_STAT_CS8
0x3C	R	0x00	SW_STAT_EXT4	SW_STAT_EXT3	SW_STAT_EXT2	SW_STAT_EXT1	SW_STAT_EXT0	0	SW_STAT_CS17	SW_STAT_CS16

Register Description - continued

0x40 to 0x41: Interrupt Factor

Name: INT_FIN_INI, INT_FIN_CAL, INT_FAL_CAL, INT_DET_NOISE, INT_SW_ON, INT_SW_OFF, INT_HLD, INT_HLDRPT, INT_MLT_ON, INT_MLT_OFF

Address: 0x40 to 0x41

Description: These registers show the interrupt factors. The INTB pin outputs low level when any bit of these registers has 1. The INTB pin outputs High when all bits of these registers have 0.

INT_FIN_INI:
When the initialization of MPU is completed, this bit is set to 1. This bit is cleared by setting 0 to the bit “Clear Interrupt Factor CLR_FIN_INI (register 0xE0[0])”.

INT_FIN_CAL:
When software calibration from the host is completed, this bit is set to 1. This bit is cleared by setting 0 to the bit “Clear Interrupt Factor CLR_FIN_CAL (register 0xE0[2])”.

INT_FAL_CAL:
When calibration error is detected, this bit is set to 1. This bit is cleared by setting 0 to the bit “Clear Interrupt Factor CLR_FAL_CAL (register 0xE0[3])”. The details of calibration error are shown in “Calibration Failure (register 0x56 to 0x58)”.

INT_DET_NOISE:
When the noise state is detected, this bit is set to 1. (About noise, refer to “Noise Judgment Setting (register 0xBE)”.) This bit is cleared by setting 0 to the bit “Clear Interrupt Factor CLR_FACT_CAL (register 0xE0[7])”. The details of the sensors that detected the noise are shown in “Calibration Factor (register 0x86 to 0x88)”.

INT_SW_ON:
When Switch ON is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_SW_ON Details (register 0x42 to 0x44)”. This bit is cleared when all bits of “Interrupt Factor INT_SW_ON Details” are cleared.

INT_SW_OFF:
When Switch OFF is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_SW_OFF details (register 0x45 to 0x47)”. This bit is cleared when all bits of “Interrupt Factor INT_SW_OFF Details” are cleared.

INT_HLD:
When Long Press is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_HLD Details (register 0x48 to 0x4A)”. This bit is cleared when all bits of “Interrupt Factor INT_HLD Details” are cleared.

INT_HLDRPT:
When Long Press Repeat is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_HLDRPT Details (register 0x4B to 0x4D)”. This bit is cleared when all bits of “Interrupt Factor INT_HLDRPT Details” are cleared.

INT_MLT_ON:
When Multi-Touch Combination ON is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_MLT_ON Details (register 0x4E)”. This bit is cleared when all bits of “Interrupt Factor INT_MLT_ON Details” are cleared.

INT_MLT_OFF:
When Multi-Touch Combination OFF is detected, this bit is set to 1. The details are shown in “Interrupt Factor INT_MLT_OFF Details (register 0x4F)”. This bit is cleared when all bits of “Interrupt Factor INT_MLT_OFF Details” are cleared.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x40	R	0x01	INT_ DET_NOISE	0	0	0	INT_ FAL_CAL	INT_ FIN_CAL	0	INT_ FIN_INI
0x41	R	0x00	DINFO_B	DINFO_A	INT_ MLT_OFF	INT_ MLT_ON	INT_ HLDRPT	INT_ HLD	INT_ SW_OFF	INT_ SW_ON

Register Description - continued

0x42 to 0x44: Interrupt Factor INT_SW_ON Details (Switch ON)

Name: DET_ON_CSm (m = 0 to 17), DET_ON_EXTn (n = 0 to 4)
Address: 0x42 to 0x44
Description: These registers show the detail of “Interrupt Factor INT_SW_ON (register 0x41[0])”.
These registers show the detected result of each Switch ON.

DET_ON_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

DET_ON_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

These are the detected results after chattering cancellation.
These are kept until cleared by setting 0 to “Clear Interrupt Factor Details CLR_DET_ON_CSm (m = 0 to 17), or CLR_DET_ON_EXTn (n = 0 to 4) (register 0xE2 to 0xE4)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x42	R	0x00	DET_ON_CS7	DET_ON_CS6	DET_ON_CS5	DET_ON_CS4	DET_ON_CS3	DET_ON_CS2	DET_ON_CS1	DET_ON_CS0
0x43	R	0x00	DET_ON_CS15	DET_ON_CS14	DET_ON_CS13	DET_ON_CS12	DET_ON_CS11	DET_ON_CS10	DET_ON_CS9	DET_ON_CS8
0x44	R	0x00	DET_ON_EXT4	DET_ON_EXT3	DET_ON_EXT2	DET_ON_EXT1	DET_ON_EXT0	0	DET_ON_CS17	DET_ON_CS16

0x45 to 0x47: Interrupt Factor INT_SW_OFF Details (Switch OFF)

Name: DET_OFF_CSm (m = 0 to 17), DET_OFF_EXTn (n = 0 to 4)
Address: 0x45 to 0x47
Description: These registers show the detail of “Interrupt Factor INT_SW_OFF (register 0x41[1])”.
These registers show the detected result of each Switch OFF.

DET_OFF_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

DET_OFF_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

These are the detected results after chattering cancellation.
These are kept until cleared by setting 0 to “Clear Interrupt Factor Datails CLR_DET_OFF_CSm (m = 0 to 17), or CLR_DET_OFF_EXTn (n = 0 to 4) (register 0xE5 to 0xE7)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x45	R	0x00	DET_OFF_CS7	DET_OFF_CS6	DET_OFF_CS5	DET_OFF_CS4	DET_OFF_CS3	DET_OFF_CS2	DET_OFF_CS1	DET_OFF_CS0
0x46	R	0x00	DET_OFF_CS15	DET_OFF_CS14	DET_OFF_CS13	DET_OFF_CS12	DET_OFF_CS11	DET_OFF_CS10	DET_OFF_CS9	DET_OFF_CS8
0x47	R	0x00	DET_OFF_EXT4	DET_OFF_EXT3	DET_OFF_EXT2	DET_OFF_EXT1	DET_OFF_EXT0	0	DET_OFF_CS17	DET_OFF_CS16

0x48 to 0x4A: Interrupt Factor INT_HLD Details (Long Press)

Name: DET_HLD_CSm (m = 0 to 17), DET_HLD_EXTn (n = 0 to 4)
Address: 0x48 to 0x4A
Description: These registers show the detail of “Interrupt Factor INT_HLD (register 0x41[2])”.
These registers show switches detected as Long Press.
About Long Press refer to “Long Press / Long Press Repeat Setting (register 0xA4 to 0xA5)”.

DET_HLD_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

DET_HLD_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

These are kept until cleared by setting 0 to “Clear Interrupt Factor Datails CLR_DET_HLD_CSm (m = 0 to 17), or CLR_DET_HLD_EXTn (n = 0 to 4) (register 0xE8 to 0xEA)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x48	R	0x00	DET_HLD_CS7	DET_HLD_CS6	DET_HLD_CS5	DET_HLD_CS4	DET_HLD_CS3	DET_HLD_CS2	DET_HLD_CS1	DET_HLD_CS0
0x49	R	0x00	DET_HLD_CS15	DET_HLD_CS14	DET_HLD_CS13	DET_HLD_CS12	DET_HLD_CS11	DET_HLD_CS10	DET_HLD_CS9	DET_HLD_CS8
0x4A	R	0x00	DET_HLD_EXT4	DET_HLD_EXT3	DET_HLD_EXT2	DET_HLD_EXT1	DET_HLD_EXT0	0	DET_HLD_CS17	DET_HLD_CS16

Register Description - continued

0x4B to 0x4D: Interrupt Factor INT_HLDRPT Details (Long Press Repeat)

Name: DET_HLDRPT_CSm (m = 0 to 17), DET_HLDRPT_EXTn (n = 0 to 4)
Address: 0x4B to 0x4D
Description: These registers show the detail of “Interrupt Factor INT_HLDRPT (register 0x41[3])”.
These registers show switches detected as Long Press Repeat.
About Long Press Repeat refer to “Long Press / Long Press Repeat Setting (register 0xA4 to 0xA5)”.

DET_HLDRPT_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

DET_HLDRPT_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

These are kept until cleared by setting 0 to “Clear Interrupt Factor Details CLR_DET_HLDRPT_CSm (m = 0 to 17), or CLR_DET_HLDRPT_EXTn (n = 0 to 4) (register 0xEB to 0xED)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4B	R	0x00	DET_HLDRPT_CS7	DET_HLDRPT_CS6	DET_HLDRPT_CS5	DET_HLDRPT_CS4	DET_HLDRPT_CS3	DET_HLDRPT_CS2	DET_HLDRPT_CS1	DET_HLDRPT_CS0
0x4C	R	0x00	DET_HLDRPT_CS15	DET_HLDRPT_CS14	DET_HLDRPT_CS13	DET_HLDRPT_CS12	DET_HLDRPT_CS11	DET_HLDRPT_CS10	DET_HLDRPT_CS9	DET_HLDRPT_CS8
0x4D	R	0x00	DET_HLDRPT_EXT4	DET_HLDRPT_EXT3	DET_HLDRPT_EXT2	DET_HLDRPT_EXT1	DET_HLDRPT_EXT0	0	DET_HLDRPT_CS17	DET_HLDRPT_CS16

0x4E: Interrupt Factor INT_MLT_ON Details (Multi-Touch Combination ON)

Name: DET_MLT_ON_Px (x = A to C)
Address: 0x4E
Description: This register shows the detail of “Interrupt Factor INT_MLT_ON (register 0x41[4])”.
This register shows the state of “Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)” detected as ON.
These results do not output to “Interrupt Factor INT_SW_ON Details DET_ON_CSm (m = 0 to 17) (register 0x42 to 0x44)”.
These are kept until cleared by setting 0 to “Clear Interrupt Factor Details CLR_DET_MLT_ON_Px (x = A to C) (register 0xEE)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4E	R	0x00	0	0	0	0	0	DET_MLT_ON_PC	DET_MLT_ON_PB	DET_MLT_ON_PA

0x4F: Interrupt Factor INT_MLT_OFF Details (Multi-Touch Combination OFF)

Name: DET_MLT_OFF_Px (x = A to C)
Address: 0x4F
Description: This register shows the detail of “Interrupt Factor INT_MLT_OFF (register 0x41[5])”.
This register shows the state of “Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)” detected as OFF.
These results do not output to “Interrupt Factor INT_SW_OFF Details DET_OFF_CSm (m = 0 to 17) (register 0x45 to 0x47)”.
These are kept until cleared by setting 0 to “Clear Interrupt Factor Details CLR_DET_MLT_OFF_Px (x = A to C) (register 0xEF)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4F	R	0x00	0	0	0	0	0	DET_MLT_OFF_PC	DET_MLT_OFF_PB	DET_MLT_OFF_PA

Register Description - continued

0x56 to 0x58: Calibration Failure

Name: FAL_CAL_CSm (m = 0 to 17)
Address: 0x56 to 0x58
Description: These registers show the calibration failure sensor.
These are updated in the timing to set 1 to “Interrupt Factor INT_FAL_CAL (register 0x40[3])”.
These are kept until “Interrupt Factor INT_FAL_CAL (register 0x40[3])” is cleared by “Clear Interrupt Factor Details CLR_FAL_CAL (register 0xE0[3])”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x56	R	0x00	FAL_CAL_CS7	FAL_CAL_CS6	FAL_CAL_CS5	FAL_CAL_CS4	FAL_CAL_CS3	FAL_CAL_CS2	FAL_CAL_CS1	FAL_CAL_CS0
0x57	R	0x00	FAL_CAL_CS15	FAL_CAL_CS14	FAL_CAL_CS13	FAL_CAL_CS12	FAL_CAL_CS11	FAL_CAL_CS10	FAL_CAL_CS9	FAL_CAL_CS8
0x58	R	0x00	0	0	0	0	0	0	FAL_CAL_CS17	FAL_CAL_CS16

0x59: Sensing State

Name: SLEEP, RUN_CAL, RUN_AFE
Address: 0x59
Description: This register shows the current sensing state.

RUN_AFE: Normal sensing

RUN_CAL: Calibration sensing

SLEEP: Intermittent sensing

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x59	R	0x00	0	0	0	0	0	SLEEP	RUN_CAL	RUN_AFE

0x5A to 0x5C: Sensor State

Name: SENS_STAT_CSm (m = 0 to 17), SENS_STAT_EXTn (n = 0 to 4)
Address: 0x5A to 0x5C
Description: These registers show the sensor recognized Switch ON.

SENS_STAT_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

SENS_STAT_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

Even though Multi-Touch of switches is disabled (“Multi-Touch of Switches Function MLT_EN (register 0xBF[4])” = 0), any bit corresponding to the sensor which is upper than ON threshold is set to 1.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x5A	R	0x00	SENS_STAT_CS7	SENS_STAT_CS6	SENS_STAT_CS5	SENS_STAT_CS4	SENS_STAT_CS3	SENS_STAT_CS2	SENS_STAT_CS1	SENS_STAT_CS0
0x5B	R	0x00	SENS_STAT_CS15	SENS_STAT_CS14	SENS_STAT_CS13	SENS_STAT_CS12	SENS_STAT_CS11	SENS_STAT_CS10	SENS_STAT_CS9	SENS_STAT_CS8
0x5C	R	0x00	SENS_STAT_EXT4	SENS_STAT_EXT3	SENS_STAT_EXT2	SENS_STAT_EXT1	SENS_STAT_EXT0	0	SENS_STAT_CS17	SENS_STAT_CS16

Register Description - continued

0x60 to 0x68: Sensor Setting

Name: CCD_CSm, RX_CSm (m = 0 to 17)
Address: 0x60 to 0x68
Description: These registers configure the operation of each sensor.

RX_CSm (m = 0 to 17):
0: Sensor Disable
1: Sensor Enable

CCD_CSm (m = 0 to 17):
0: Capacitance Cancel Drive Disable
1: Capacitance Cancel Drive Enable

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x60	R/W	0x33	0	SINFO_W1	CCD_CS1	RX_CS1	0	SINFO_W0	CCD_CS0	RX_CS0
0x61	R/W	0x33	0	SINFO_W3	CCD_CS3	RX_CS3	0	SINFO_W2	CCD_CS2	RX_CS2
0x62	R/W	0x33	0	SINFO_W5	CCD_CS5	RX_CS5	0	SINFO_W4	CCD_CS4	RX_CS4
0x63	R/W	0x33	0	SINFO_W7	CCD_CS7	RX_CS7	0	SINFO_W6	CCD_CS6	RX_CS6
0x64	R/W	0x33	0	SINFO_W9	CCD_CS9	RX_CS9	0	SINFO_W8	CCD_CS8	RX_CS8
0x65	R/W	0x33	0	SINFO_W11	CCD_CS11	RX_CS11	0	SINFO_W10	CCD_CS10	RX_CS10
0x66	R/W	0x33	0	SINFO_W13	CCD_CS13	RX_CS13	0	SINFO_W12	CCD_CS12	RX_CS12
0x67	R/W	0x33	0	SINFO_W15	CCD_CS15	RX_CS15	0	SINFO_W14	CCD_CS14	RX_CS14
0x68	R/W	0x33	0	SINFO_W17	CCD_CS17	RX_CS17	0	SINFO_W16	CCD_CS16	RX_CS16

Register Description - continued

0x6A to 0x7B: Sensitivity, ON Threshold Setting

Name: VAL_TH_ON_CSm, VAL_GAIN_CSm (m = 0 to 17)
Address: 0x6A to 0x7B
Description: These registers configure the sensor sensitivity and the ON threshold for each sensor.

VAL_GAIN_CSm (m = 0 to 17): Sensitivity setting.
Allowable setting value range is from 0x0 to 0xF.
The smaller setting value makes the sensor sensitivity higher.

VAL_TH_ON_CSm (m = 0 to 17): ON threshold setting.
Allowable setting value range is from 0x2 to 0xF.
ON threshold value = VAL_TH_ON_CSm x 16
When “Sensor Value (register 0x00 to 0x11)” becomes larger than the ON threshold value, the sensor detects ON.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x6A	R/W	0x8E	VAL_TH_ON_CS0				VAL_GAIN_CS0			
0x6B	R/W	0x8E	VAL_TH_ON_CS1				VAL_GAIN_CS1			
0x6C	R/W	0x8E	VAL_TH_ON_CS2				VAL_GAIN_CS2			
0x6D	R/W	0x8E	VAL_TH_ON_CS3				VAL_GAIN_CS3			
0x6E	R/W	0x8E	VAL_TH_ON_CS4				VAL_GAIN_CS4			
0x6F	R/W	0x8E	VAL_TH_ON_CS5				VAL_GAIN_CS5			
0x70	R/W	0x8E	VAL_TH_ON_CS6				VAL_GAIN_CS6			
0x71	R/W	0x8E	VAL_TH_ON_CS7				VAL_GAIN_CS7			
0x72	R/W	0x8E	VAL_TH_ON_CS8				VAL_GAIN_CS8			
0x73	R/W	0x8E	VAL_TH_ON_CS9				VAL_GAIN_CS9			
0x74	R/W	0x8E	VAL_TH_ON_CS10				VAL_GAIN_CS10			
0x75	R/W	0x8E	VAL_TH_ON_CS11				VAL_GAIN_CS11			
0x76	R/W	0x8E	VAL_TH_ON_CS12				VAL_GAIN_CS12			
0x77	R/W	0x8E	VAL_TH_ON_CS13				VAL_GAIN_CS13			
0x78	R/W	0x8E	VAL_TH_ON_CS14				VAL_GAIN_CS14			
0x79	R/W	0x8E	VAL_TH_ON_CS15				VAL_GAIN_CS15			
0x7A	R/W	0x8E	VAL_TH_ON_CS16				VAL_GAIN_CS16			
0x7B	R/W	0x8E	VAL_TH_ON_CS17				VAL_GAIN_CS17			

0x7D: OFF Threshold Setting

Name: VAL_TH_OFF
Address: 0x7D
Description: This register configures the OFF threshold common to all sensors.

VAL_TH_OFF: OFF threshold setting.
Allowable setting value range is from 0x1 to 0xE.
OFF threshold value = VAL_TH_OFF x 16
Switch OFF is detected when “Sensor Value (register 0x00 to 0x11)” becomes smaller than the OFF threshold value.
Constraint on setting: ON threshold value > OFF threshold value.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x7D	R/W	0x40	VAL_TH_OFF				0	0	0	0

Register Description - continued

0x86 to 0x88: Calibration Factor

Name: DET_CAL_CSm (m = 0 to 17), CAL_NOISE, CAL_OFS, CAL_DRIFT, CAL_MINUS
Address: 0x86 to 0x88
Description: These registers show the calibration factors and the sensors which detected calibration factors.
Software calibration and retrial calibration are not included.
These are not updated until cleared.
These are cleared by setting 0 to “Clear Interrupt Factor CLR_FACT_CAL (register 0xE0[7])”.

DET_CAL_CSm (m = 0 to 17): Any bits corresponding to the sensors which detected calibration factor are set to 1.

CAL_MINUS: This bit is set to 1 when the factor of Minus Detection Value Calibration is detected.

CAL_DRIFT: This bit is set to 1 when the factor of Drift Calibration is detected.

CAL_OFS: This bit is set to 1 when the factor of Offset Calibration is detected.

CAL_NOISE: This bit is set to 1 when the factor of Noise Calibration is detected.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x86	R	0x00	DET_CAL_CS7	DET_CAL_CS6	DET_CAL_CS5	DET_CAL_CS4	DET_CAL_CS3	DET_CAL_CS2	DET_CAL_CS1	DET_CAL_CS0
0x87	R	0x00	DET_CAL_CS15	DET_CAL_CS14	DET_CAL_CS13	DET_CAL_CS12	DET_CAL_CS11	DET_CAL_CS10	DET_CAL_CS9	DET_CAL_CS8
0x88	R	0x00	CAL_NOISE	CAL_OFS	CAL_DRIFT	CAL_MINUS	0	0	DET_CAL_CS17	DET_CAL_CS16

0x89 to 0x8B: Software Calibration Error Sensors

Name: SOFT_CAL_ERR_CSm (m = 0 to 17)
Address: 0x89 to 0x8B
Description: Any bits corresponding to the sensors detected the Calibration error by Software Calibration are set to 1.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x89	R	0x00	SOFT_CAL_ERR_CS7	SOFT_CAL_ERR_CS6	SOFT_CAL_ERR_CS5	SOFT_CAL_ERR_CS4	SOFT_CAL_ERR_CS3	SOFT_CAL_ERR_CS2	SOFT_CAL_ERR_CS1	SOFT_CAL_ERR_CS0
0x8A	R	0x00	SOFT_CAL_ERR_CS15	SOFT_CAL_ERR_CS14	SOFT_CAL_ERR_CS13	SOFT_CAL_ERR_CS12	SOFT_CAL_ERR_CS11	SOFT_CAL_ERR_CS10	SOFT_CAL_ERR_CS9	SOFT_CAL_ERR_CS8
0x8B	R	0x00	0	0	0	0	0	0	SOFT_CAL_ERR_CS17	SOFT_CAL_ERR_CS16

Register Description - continued

0xA0: Sampling Period Setting

Name: MIN_FRAME_PERIOD
Address: 0xA0
Description: This register configures the sampling period.
Sampling period = setting value x approximately 10 ms.
Allowable setting value range is from 0x0 to 0xF.
When the detection sensing time + the data processing time > sampling period, sampling period is determined by the detection sensing time + the data processing time.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA0	R/W	0x00	0	0	0	0	MIN_FRAME_PERIOD			

0xA1 to 0xA3: Intermittent Sensing Setting

Name: CHECK_PERIOD_IN_SLEEP, SLEEP_IN_TIME, SLEEP_OUT_TIME
Address: 0xA1 to 0xA3
Description: When Intermittent Sensing Function is enabled ("Intermittent Sensing Function SLEEP_EN (register 0xBF[0])" = 1), these settings are enabled.

CHECK_PERIOD_IN_SLEEP: This register configures the interval of check sensing for detecting touch operation during intermittent sensing. If detect touch operation during intermittent sensing, move on to normal sensing.
The interval of check sensing = (setting value + 1) x approximately 0.02 s

SLEEP_IN_TIME: This register configures the transition time from detection of the Switch OFF to intermittent sensing.
The transition time = (setting value + 1) x approximately 0.2 s

SLEEP_OUT_TIME: This register configures the checking times of the intermittent sensing.
The checking times = (setting value + 1) times
When the setting value is 0xFF, self-shifting to normal sensing is disabled.

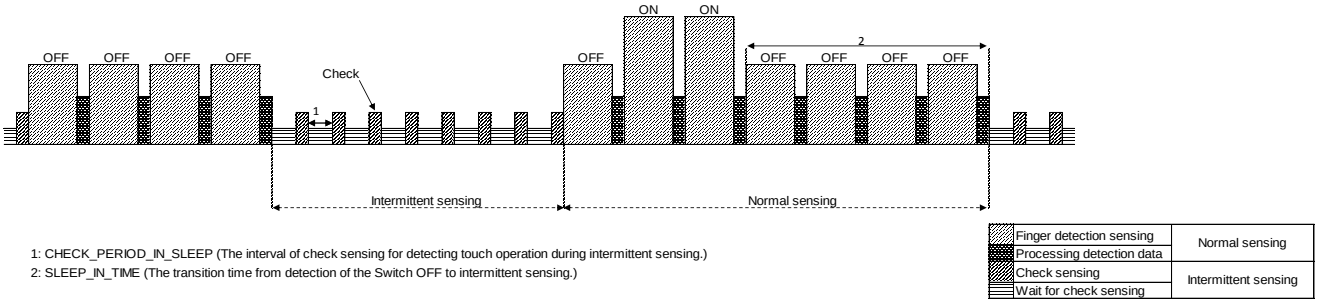


Figure 10. Intermittent Sensing Setting

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA1	R/W	0x00	CHECK_PERIOD_IN_SLEEP							
0xA2	R/W	0x00	SLEEP_IN_TIME							
0xA3	R/W	0x00	SLEEP_OUT_TIME							

0xA4 to 0xA5: Long Press / Long Press Repeat Setting

Name: HLD_DET_TIME, HLDRPT_DET_TIME
Address: 0xA4 to 0xA5
Description: HLD_DET_TIME: This register configures the time of Long Press detection. When a Switch ON state continues for setting value x approximately 0.1 s after Switch ON recognition, it detects Long Press.
HLDRPT_DET_TIME: This register configures the time of Long Press Repeat detection. When a Switch ON state continues for setting value x approximately 0.1 s after Long Press recognition, it detects Long Press Repeat. The Long Press Repeat is detected repeatedly until Switch OFF is detected.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA4	R/W	0x00	HLD_DET_TIME							
0xA5	R/W	0x00	HLDRPT_DET_TIME							

Register Description - continued

0xA6: Switch Detectable Time Setting

Name: MLT_DET_TIME
Address: 0xA6
Description: This register configures the permission period of touch to the different sensors after Switch ON. This register is enabled when Multi-Touch of switches is disabled (“Multi-Touch of Switches Function MLT_EN (register 0xBF[4])” = 0). The permission period is from the first Switch ON to the time that is setting value x approximately 0.01 s. It needs the time for “Chattering Cancellation Setting OST_SW (register 0xB0[3:0])” by the timing of first Switch ON.

The touch for the other sensor is detected during the permission period of touch.
When the detection result of touch matched with “Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)”, “Interrupt Factor INT_MLT_ON (register 0x41[4])” is set to 1. The detail of Multi-Touch is shown to “Interrupt Factor INT_MLT_ON Details (register 0x4E)” and “Switch State (register 0x3A to 0x3C)”.
When the detection result of touch unmatched with “Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)”, there is no sensor detected Switch ON.

The touch to the other sensors is not detected after the permission period gone.
Only the first sensor recognized ON is detected as Switch ON. “Interrupt Factor INT_SW_ON Details (register 0x42 to 0x44)” is set to 1.

After the states of all sensors are Switch OFF, the touch is permitted in the next time.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA6	R/W	0x00	MLT_DET_TIME							

0xA7 to 0xAF: Multi-Touch Combination Assignment Setting

Name: MLT_Px_CSm (m = 0 to 17, x = A to C)
Address: 0xA7 to 0xAF
Description: These registers configure the 3 types of the combination assignments that are permitted to Multi-Touch Combination detection. Multi-Touch Combination are enable when Multi-Touch of switches is disabled (“Multi-Touch of Switches Function MLT_EN (register 0xBF[4])” = 0).

MLT_PA_CSm (m = 0 to 17): Set Multi-Touch Combination Assignment Setting A
MLT_PB_CSm (m = 0 to 17): Set Multi-Touch Combination Assignment Setting B
MLT_PC_CSm (m = 0 to 17): Set Multi-Touch Combination Assignment Setting C

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA7	R/W	0x00	MLT_PA_CS7	MLT_PA_CS6	MLT_PA_CS5	MLT_PA_CS4	MLT_PA_CS3	MLT_PA_CS2	MLT_PA_CS1	MLT_PA_CS0
0xA8	R/W	0x00	MLT_PA_CS15	MLT_PA_CS14	MLT_PA_CS13	MLT_PA_CS12	MLT_PA_CS11	MLT_PA_CS10	MLT_PA_CS9	MLT_PA_CS8
0xA9	R/W	0x00	0	0	0	0	0	0	MLT_PA_CS17	MLT_PA_CS16
0xAA	R/W	0x00	MLT_PB_CS7	MLT_PB_CS6	MLT_PB_CS5	MLT_PB_CS4	MLT_PB_CS3	MLT_PB_CS2	MLT_PB_CS1	MLT_PB_CS0
0xAB	R/W	0x00	MLT_PB_CS15	MLT_PB_CS14	MLT_PB_CS13	MLT_PB_CS12	MLT_PB_CS11	MLT_PB_CS10	MLT_PB_CS9	MLT_PB_CS8
0xAC	R/W	0x00	0	0	0	0	0	0	MLT_PB_CS17	MLT_PB_CS16
0xAD	R/W	0x00	MLT_PC_CS7	MLT_PC_CS6	MLT_PC_CS5	MLT_PC_CS4	MLT_PC_CS3	MLT_PC_CS2	MLT_PC_CS1	MLT_PC_CS0
0xAE	R/W	0x00	MLT_PC_CS15	MLT_PC_CS14	MLT_PC_CS13	MLT_PC_CS12	MLT_PC_CS11	MLT_PC_CS10	MLT_PC_CS9	MLT_PC_CS8
0xAF	R/W	0x00	0	0	0	0	0	0	MLT_PC_CS17	MLT_PC_CS16

Register Description - continued

0xB0: Chattering Cancellation Setting

Name: OST_EXT_SW, OST_SW
Address: 0xB0
Description: This register configures the number of oversampling to reject chattering. When ON / OFF judgment is same consecutively (setting value + 1) times, “Switch ON” or “Switch OFF” is detected.

OST_EXT_SW: Tact Switches (The GPIOn pin (n = 0 to 4))
Writing a value 0x0 is prohibited.
Sampling period of Tact Switches: approximately 20 ms.

OST_SW: Capacitive Switches (The CSm pin (m = 0 to 17))

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB0	R/W	0x10	OST_EXT_SW				OST_SW			

0xB2: Filter Setting

Name: FIL_IIR, FIL_MEDIAN
Address: 0xB2
Description: This register configures the setting of the filter for capacitive switch.

FIL_MEDIAN: This register configures the number of Median Filter tap.
Number of Median Filter tap = setting value x 2 + 1
When the setting value is 0, Median Filter is disabled.

FIL_IIR: This register configures the coefficient of linear IIR Filter.
Filter coefficient k = setting value + 1
IIR Filter output = ADC level / k + last time’s IIR Filter output x (k - 1) / k
When the setting value is 0, IIR Filter is disabled.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB2	R/W	0x02	FIL_IIR				0	0	FIL_MEDIAN	

0xB3: Sensing Frequency Setting

Name: FREQ_AFE
Address: 0xB3
Description: This register configures the sensing frequency.
The sensing frequency is related to the registers below.
The sensing frequency modulation “Sensing Frequency Modulate Function FMOD_EN (register 0xBF[6])”
The number of Median Filter tap “Filter Setting FIL_MEDIAN (register 0xB2[1:0])”

Average sensing frequency (Unit: kHz)

FMOD_EN		0	1			
FIL_MEDIAN		x	0	1	2	3
FREQ_AFE	0	781	781	781	781	694
	1	595	595	595	595	509
	2	446	446	441	434	363
	3	245	245	237	222	124

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB3	R/W	0x02	0	0	0	0	0	0	FREQ_AFE	

0xB4: Reserved

Address: 0xB4
Description: This register is a reserved area. Writing a value different from the initial value is prohibited. The initial value is 0x03.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB4	R/W	0x03	Reserved							

Register Description - continued

0xB6: Calibration Setting

Name: CAL_PERIOD_EN, CAL_OFS_EN, CAL_MINUS_EN, CAL_DRIFT_EN, CAL_NOISE_EN
Address: 0xB6
Description: This register configures the calibration function. It is enabled by setting with 1.

CAL_NOISE_EN: Noise Calibration
About Noise Calibration, refer to “Noise Judgment Setting (register 0xBE)”.

CAL_DRIFT_EN: Drift Calibration
About Drift Calibration, refer to “Drift Judgment Setting (register 0xB7)”.

CAL_MINUS_EN: Minus Detection Value Calibration
Only the sensor whose downward value is under than OFF threshold value from the standard value is calibrated.

CAL_OFS_EN: Offset Calibration
About Offset Calibration, refer to “Offset Correction Frequency Setting (register 0xB8)”.

CAL_PERIOD_EN: Periodical Calibration
About Periodical Calibration, refer to “Periodical Calibration Time Setting (register 0xBC)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB6	R/W	0x27	0	0	SINFO_D	CAL_ PERIOD_EN	CAL_ OFS_EN	CAL_ MINUS_EN	CAL_ DRIFT_EN	CAL_ NOISE_EN

0xB7: Drift judgment Setting

Name: NUM_CS_DET_DRIFT
Address: 0xB7
Description: This register is enabled when Drift Calibration is enabled (“Drift Calibration CAL_DRIFT_EN (register 0xB6[1])” = 1).
When the numbers of sensors whose value is more than a half of OFF threshold value from the standard value are more than the setting value of this register, drift state is detected.
When drift state keeps on 10 sampling, Drift Calibration is performed excluding the sensor whose value is over the ON threshold value or the sensor which is ON.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB7	R/W	0x03	NUM_CS_DET_DRIFT							

0xB8: Offset Correction Frequency Setting

Name: NUM_FRAME_CORRECT_OFS
Address: 0xB8
Description: This register is enabled when Offset Calibration is enabled (“Calibration Setting CAL_OFS_EN (register 0xB6[3])” = 1).
This register configures the interval at which Offset correction is performed. Offset correction is to move ADC value closer to the standard value.
The larger the setting value is, the lower the frequency of Offset correction is. When the setting value is set to 0, Offset correction is disabled.
When the accumulated corrected offset value is higher than a certain value, Offset Calibration is executed.
Offset Correction is performed excluding the sensor which value is over the ON threshold value or the sensor which is ON.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB8	R/W	0x21	NUM_FRAME_CORRECT_OFS							

Register Description - continued

0xB9: GPI Tact Switch Setting

Name: GPIO_EXT_IN_POL, GPIOn_EXT_SW_IN (n = 0 to 4)
Address: 0xB9
Description: This register configures GPIO ports to input for Tact Switches.

GPIOn_EXT_SW_IN (n = 0 to 4): This register corresponding to the GPIO port used as input Tact Switch is set to 1.

GPIO setting priority
1st: GPI Tact Switch Setting (register 0xB9)
2nd: GPO Output Setting (register 0xBA)
3rd: CS-to-GPO Linked Output Setting (register 0xBB)

GPIO_EXT_IN_POL: Select input polarity of Tact Switch.
0: Low level input makes Switch ON.
1: High level input makes Switch ON.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xB9	R/W	0x00	GPIO_EXT_IN_POL	0	0	GPIO4_EXT_SW_IN	GPIO3_EXT_SW_IN	GPIO2_EXT_SW_IN	GPIO1_EXT_SW_IN	GPIO0_EXT_SW_IN

0xBA: GPO Output Setting

Name: GPIOn_REG_OUT (n = 0 to 4)
Address: 0xBA
Description: This register configures GPIO ports to output the value of “GPO Control (register 0xFE)”.

GPIO0_REG_OUT: Register 0xFE[0] is output from GPIO0
GPIO1_REG_OUT: Register 0xFE[1] is output from GPIO1
GPIO2_REG_OUT: Register 0xFE[2] is output from GPIO2
GPIO3_REG_OUT: Register 0xFE[3] is output from GPIO3
GPIO4_REG_OUT: Register 0xFE[4] is output from GPIO4

GPIO setting priority
1st: GPI Tact Switch Setting (register 0xB9)
2nd: GPO Output Setting (register 0xBA)
3rd: CS-to-GPO Linked Output Setting (register 0xBB)

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBA	R/W	0x00	0	0	0	GPIO4_REG_OUT	GPIO3_REG_OUT	GPIO2_REG_OUT	GPIO1_REG_OUT	GPIO0_REG_OUT

Register Description - continued

0xBB: CS-to-GPO Linked Output Setting

Name: GPIO_EXT_OUT_POL, GPIOn_CSn_SW_OUT (n = 0 to 4)
Address: 0xBB
Description: This register configures GPIO ports to output “Sensor State (register 0x5A)” of sensor from CS0 to CS4.

GPIO0_CS0_SW_OUT: A switch state of CS0 is output from GPIO0
GPIO1_CS1_SW_OUT: A switch state of CS1 is output from GPIO1
GPIO2_CS2_SW_OUT: A switch state of CS2 is output from GPIO2
GPIO3_CS3_SW_OUT: A switch state of CS3 is output from GPIO3
GPIO4_CS4_SW_OUT: A switch state of CS4 is output from GPIO4

GPIO setting priority
1st: GPI Tact Switch Setting (register 0xB9)
2nd: GPO Output Setting (register 0xBA)
3rd: CS-to-GPO Linked Output Setting (register 0xBB)

GPO_EXT_OUT_POL: Select output polarity.
0: Output high at Switch ON
1: Output low at Switch ON

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBB	R/W	0x00	GPIO_EXT_OUT_POL	0	0	GPIO4_CS4_SW_OUT	GPIO3_CS3_SW_OUT	GPIO2_CS2_SW_OUT	GPIO1_CS1_SW_OUT	GPIO0_CS0_SW_OUT

0xBC: Periodical Calibration Time Setting

Name: TIME_PERCAL
Address: 0xBC
Description: This register configures the interval time of the periodical calibration.
This register is enabled when Periodical Calibration is enabled (“Calibration Setting CAL_PERIOD_EN (register 0xB6[4])” = 1).
When this register is set to 0, the periodical calibration is not performed.
When periodical calibration is failed, recalibration is not performed.
Periodical calibration is performed excluding the sensor which value is over ON threshold value or the sensor which is Switch ON

Interval time of the periodical calibration = TIME_PERCAL x approximately 5 s

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBC	R/W	0x00	TIME_PERCAL							

0xBD: Software Calibration Time-out Setting

Name: TIMOUT_SOFT_CALIB
Address: 0xBD
Description: This register configures a function to prevent the non-responsive of the sensors due to the fact that the software calibration by the command from the host does not finish. The sensors that have failed consecutively (setting value x 3) times to the software calibration are shown “Software Calibration Error Sensors (register 0x89 to 0x8B)”. The sensors cannot be used until the next software calibration has been executed and succeeded.
When this register is set to 0, the software calibration is repeated until the calibration of all sensors is finished.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBD	R/W	0x00	0	0	0	TIMOUT_SOFT_CALIB				

Register Description - continued

0xBE: Noise Judgment Setting

Name: NUM_CS_DET_NOISE
Address: 0xBE
Description: This register configures the operating conditions of Noise Calibration. When Noise Calibration is enabled ("Calibration Setting CAL_NOISE_EN (register 0xB6[0])" = 1), this register is enabled.
When the number of sensors which downward value is under than the ON threshold value from the standard value are equal to or more than this register setting value, noise state is detected.
When the "Interrupt Factor INT_DET_NOISE (register 0x40[7])" is set to 1, Noise Calibration is performed to all sensors.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBE	R/W	0x01	NUM_CS_DET_NOISE							

0xBF: Function Enable Setting

Name: FMOD_EN, DET_NOISE_FSFT_EN, MLT_EN, CAL_FAL_FSFT_EN, SLEEP_ADJ_OFS, SLEEP_EN
Address: 0xBF
Description: This register configures enable of each function.

SLEEP_EN: Intermittent Sensing Function.
0: Intermittent sensing is disabled.
1: Intermittent sensing is enabled.

SLEEP_ADJ_OFS: Offset Adjustment Function during intermittent sensing.
0: Offset adjustment function is disabled during intermittent sensing.
1: Offset adjustment function is enabled during intermittent sensing.

CAL_FAL_FSFT_EN: Sensing Frequency Shift Function at failing the software calibration or the noise calibration. At the time of 3 consecutive times failure of software calibration or the noise calibration, it shifts the sensing frequency.
0: Sensing frequency shift is disabled.
1: Sensing frequency shift is enabled.

MLT_EN: Multi-Touch of Switches Function.
0: Multi-Touch of switch is disabled. (Except three patterns of "Multi-Touch Combination Assignment Setting (register 0xA7 to 0xAF)")
1: Multi-Touch of switch is enabled.

DET_NOISE_FSFT_EN: Sensing Frequency Shift Function at detecting noise state. To avoid the effects of noise, shift the sensing frequency before acting the noise calibration.
0: Sensing frequency shift is disabled.
1: Sensing frequency shift is enabled.

FMOD_EN: Sensing Frequency Modulate Function.
When Median Filter is disabled ("Filter Setting FIL_MEDIAN (register 0xB2[1:0])" = 0), sensing frequency modulate function is disable.
0: Sensing frequency modulate function is disabled.
1: Sensing frequency modulate function is enabled.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xBF	R/W	0x00	0	FMOD_EN	DET_NOISE_ FSFT_EN	MLT_EN	CAL_FAL_ FSFT_EN	0	SLEEP_ ADJ_OFS	SLEEP_EN

Register Description - continued

0xC0 to 0xC2: Long Press Enable Setting

Name: HLD_EN_CSm (m = 0 to 17), HLD_EN_EXTn (n = 0 to 4)
Address: 0xC0 to 0xC2
Description: These registers configure the Long Press.
0: Long Press is disabled.
1: Long Press is enabled.

HLD_EN_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

HLD_EN_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC0	R/W	0x00	HLD_EN_CS7	HLD_EN_CS6	HLD_EN_CS5	HLD_EN_CS4	HLD_EN_CS3	HLD_EN_CS2	HLD_EN_CS1	HLD_EN_CS0
0xC1	R/W	0x00	HLD_EN_CS15	HLD_EN_CS14	HLD_EN_CS13	HLD_EN_CS12	HLD_EN_CS11	HLD_EN_CS10	HLD_EN_CS9	HLD_EN_CS8
0xC2	R/W	0x00	HLD_EN_EXT4	HLD_EN_EXT3	HLD_EN_EXT2	HLD_EN_EXT1	HLD_EN_EXT0	0	HLD_EN_CS17	HLD_EN_CS16

0xC3 to 0xC5: Long Press Repeat Enable Setting

Name: HLDRPT_EN_CSm (m = 0 to 17), HLDRPT_EN_EXTn (n = 0 to 4)
Address: 0xC3 to 0xC5
Description: These registers configure the Long Press Repeat.
0: Long Press Repeat is disabled.
1: Long Press Repeat is enabled.

HLDRPT_EN_CSm (m = 0 to 17): Capacitive Switches (The CSm pin (m = 0 to 17))

HLDRPT_EN_EXTn (n = 0 to 4): Tact Switches (The GPIOn pin (n = 0 to 4))

Long Press Repeat is disabled to the sensor that Long Press is disabled.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC3	R/W	0x00	HLDRPT_EN_CS7	HLDRPT_EN_CS6	HLDRPT_EN_CS5	HLDRPT_EN_CS4	HLDRPT_EN_CS3	HLDRPT_EN_CS2	HLDRPT_EN_CS1	HLDRPT_EN_CS0
0xC4	R/W	0x00	HLDRPT_EN_CS15	HLDRPT_EN_CS14	HLDRPT_EN_CS13	HLDRPT_EN_CS12	HLDRPT_EN_CS11	HLDRPT_EN_CS10	HLDRPT_EN_CS9	HLDRPT_EN_CS8
0xC5	R/W	0x00	HDLRPT_EN_EXT4	HDLRPT_EN_EXT3	HDLRPT_EN_EXT2	HDLRPT_EN_EXT1	HDLRPT_EN_EXT0	0	HLDRPT_EN_CS17	HLDRPT_EN_CS16

0xDE: Reserved

Address: 0xDE
Description: This register is a reserved area. Writing a value different from the initial value is prohibited. The initial value is 0x38.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDE	R/W	0x38	Reserved							

Register Description - continued

0xE0: Clear Interrupt Factor

Name: CLR_FACT_CAL, CLR_FAL_CAL, CLR_FIN_CAL, CLR_FIN_INI
Address: 0xE0
Description: This register is for clearing “Interrupt Factor (register 0x40)”.
0: Clear interrupt factor.
1: Not clear interrupt factor.

CLR_FIN_INI: This bit is for clearing “Interrupt Factor INT_FIN_INI (register 0x40[0])”.

CLR_FIN_CAL: This bit is for clearing “Interrupt Factor INT_FIN_CAL (register 0x40[2])”.

CLR_FAL_CAL: This bit is for clearing “Interrupt Factor INT_FAL_CAL (register 0x40[3])”.

CLR_FACT_CAL: This bit is for clearing “Interrupt Factor INT_DET_NOISE (register 0x40[7])” and “Calibration Factor (register 0x86 to 0x88)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	R/W	0x00	CLR_ FACT_CAL	0	0	0	CLR_ FAL_CAL	CLR_ FIN_CAL	0	CLR_ FIN_INI

Register Description - continued

0xE2 to 0xEF: Clear Interrupt Factor Details

Name: CLR_DET_ON_CSm, CLR_DET_ON_EXTn, CLR_DET_OFF_CSm, CLR_DET_OFF_EXTn, CLR_DET_HLD_CSm, CLR_DET_HLD_EXTn, CLR_DET_HLDRPT_CSm, CLR_DET_HLDRPT_EXTn, CLR_DET_MLT_ON_Px, CLR_DET_MLT_OFF_Px (m = 0 to 17, n = 0 to 4, x = A to C)

Address: 0xE2 to 0xEF

Description: These registers are for clearing each “Interrupt Factor Details (register 0x42 to 0x4F)”.
0: Clear interrupt factor.
1: Not clear interrupt factor.

CLR_DET_ON_CSm (m = 0 to 17) and CLR_DET_ON_EXTn (n = 0 to 4) (register 0xE2 to 0xE4): These registers are for clearing “Interrupt Factor INT_SW_ON Details (register 0x42 to 0x44)”.

CLR_DET_OFF_CSm (m = 0 to 17) and CLR_DET_OFF_EXTn (n = 0 to 4) (register 0xE5 to 0xE7): These registers are for clearing “Interrupt Factor INT_SW_OFF Details (register 0x45 to 0x47)”.

CLR_DET_HLD_CSm (m = 0 to 17) and CLR_DET_HLD_EXTn (n = 0 to 4) (register 0xE8 to 0xEA): These registers are for clearing “Interrupt Factor INT_HLD Details (register 0x48 to 0x4A)”.

CLR_DET_HLDRPT_CSm (m = 0 to 17) and CLR_DET_HLDRPT_EXTn (n = 0 to 4) (register 0xEB to 0xED): These registers are for clearing “Interrupt Factor INT_HLDRPT Details (register 0x4B to 0x4D)”.

CLR_DET_MLT_ON_Px (x = A to C) (register 0xEE): This register is for clearing “Interrupt Factor INT_MLT_ON Details (register 0x4E)”.

CLR_DET_MLT_OFF_Px (x = A to C) (register 0xEF): This register is for clearing “Interrupt Factor INT_MLT_OFF Details (register 0x4F)”.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE2	R/W	0x00	CLR_DET_ON_CS7	CLR_DET_ON_CS6	CLR_DET_ON_CS5	CLR_DET_ON_CS4	CLR_DET_ON_CS3	CLR_DET_ON_CS2	CLR_DET_ON_CS1	CLR_DET_ON_CS0
0xE3	R/W	0x00	CLR_DET_ON_CS15	CLR_DET_ON_CS14	CLR_DET_ON_CS13	CLR_DET_ON_CS12	CLR_DET_ON_CS11	CLR_DET_ON_CS10	CLR_DET_ON_CS9	CLR_DET_ON_CS8
0xE4	R/W	0x00	CLR_DET_ON_EXT4	CLR_DET_ON_EXT3	CLR_DET_ON_EXT2	CLR_DET_ON_EXT1	CLR_DET_ON_EXT0	0	CLR_DET_ON_CS17	CLR_DET_ON_CS16
0xE5	R/W	0x00	CLR_DET_OFF_CS7	CLR_DET_OFF_CS6	CLR_DET_OFF_CS5	CLR_DET_OFF_CS4	CLR_DET_OFF_CS3	CLR_DET_OFF_CS2	CLR_DET_OFF_CS1	CLR_DET_OFF_CS0
0xE6	R/W	0x00	CLR_DET_OFF_CS15	CLR_DET_OFF_CS14	CLR_DET_OFF_CS13	CLR_DET_OFF_CS12	CLR_DET_OFF_CS11	CLR_DET_OFF_CS10	CLR_DET_OFF_CS9	CLR_DET_OFF_CS8
0xE7	R/W	0x00	CLR_DET_OFF_EXT4	CLR_DET_OFF_EXT3	CLR_DET_OFF_EXT2	CLR_DET_OFF_EXT1	CLR_DET_OFF_EXT0	0	CLR_DET_OFF_CS17	CLR_DET_OFF_CS16
0xE8	R/W	0x00	CLR_DET_HLD_CS7	CLR_DET_HLD_CS6	CLR_DET_HLD_CS5	CLR_DET_HLD_CS4	CLR_DET_HLD_CS3	CLR_DET_HLD_CS2	CLR_DET_HLD_CS1	CLR_DET_HLD_CS0
0xE9	R/W	0x00	CLR_DET_HLD_CS15	CLR_DET_HLD_CS14	CLR_DET_HLD_CS13	CLR_DET_HLD_CS12	CLR_DET_HLD_CS11	CLR_DET_HLD_CS10	CLR_DET_HLD_CS9	CLR_DET_HLD_CS8
0xEA	R/W	0x00	CLR_DET_HLD_EXT4	CLR_DET_HLD_EXT3	CLR_DET_HLD_EXT2	CLR_DET_HLD_EXT1	CLR_DET_HLD_EXT0	0	CLR_DET_HLD_CS17	CLR_DET_HLD_CS16
0xEB	R/W	0x00	CLR_DET_HLDRPT_CS7	CLR_DET_HLDRPT_CS6	CLR_DET_HLDRPT_CS5	CLR_DET_HLDRPT_CS4	CLR_DET_HLDRPT_CS3	CLR_DET_HLDRPT_CS2	CLR_DET_HLDRPT_CS1	CLR_DET_HLDRPT_CS0
0xEC	R/W	0x00	CLR_DET_HLDRPT_CS15	CLR_DET_HLDRPT_CS14	CLR_DET_HLDRPT_CS13	CLR_DET_HLDRPT_CS12	CLR_DET_HLDRPT_CS11	CLR_DET_HLDRPT_CS10	CLR_DET_HLDRPT_CS9	CLR_DET_HLDRPT_CS8
0xED	R/W	0x00	CLR_DET_HLDRPT_EXT4	CLR_DET_HLDRPT_EXT3	CLR_DET_HLDRPT_EXT2	CLR_DET_HLDRPT_EXT1	CLR_DET_HLDRPT_EXT0	0	CLR_DET_HLDRPT_CS17	CLR_DET_HLDRPT_CS16
0xEE	R/W	0x00	0	0	0	0	0	CLR_DET_MLT_ON_PC	CLR_DET_MLT_ON_PB	CLR_DET_MLT_ON_PA
0xEF	R/W	0x00	0	0	0	0	0	CLR_DET_MLT_OFF_PC	CLR_DET_MLT_OFF_PB	CLR_DET_MLT_OFF_PA

Register Description - continued

0xF6 to 0xF7: Software Reset

Name: SWRST_H, SWRST_L
Address: 0xF6 to 0xF7
Description: These registers configure software reset. When the data of SWRST_H is set to 0x55 and the data of SWRST_L is set to 0xAA, IC is initialized and all registers are cleared.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF6	R/W	0x00	SWRST_H							
0xF7	R/W	0x00	SWRST_L							

0xFE: GPO Control

Name: CNT_GPIOn (n = 0 to 4)
Address: 0xFE
Description: This register configures the output data to GPIO which chose an output function by “GPO Output Setting (register 0xBA)”.
0: Output low level.
1: Output high level.

CNT_GPIO0: Control the output to GPIO0.
CNT_GPIO1: Control the output to GPIO1.
CNT_GPIO2: Control the output to GPIO2.
CNT_GPIO3: Control the output to GPIO3.
CNT_GPIO4: Control the output to GPIO4.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFE	R/W	0x00	0	0	0	CNT_GPIO4	CNT_GPIO3	CNT_GPIO2	CNT_GPIO1	CNT_GPIO0

0xFF: AFE Control

Name: SET, CAL, ACT
Address: 0xFF
Description: This register configures operation for detection.

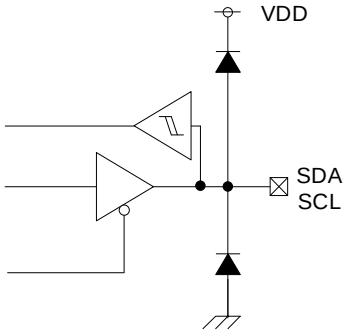
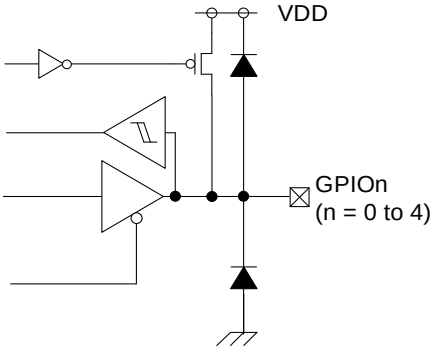
ACT: Control Sensing
0: Stop sensing
1: Start sensing

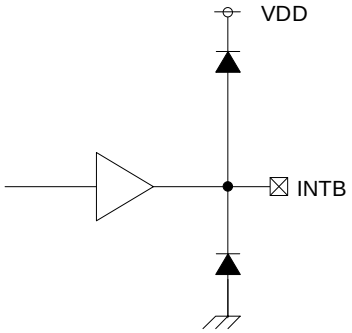
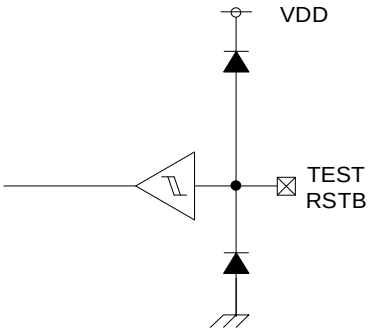
CAL: Software Calibration
0: Calibration is not performed
1: Calibration is performed

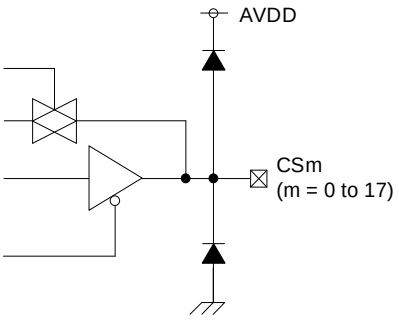
SET: Update Configuration Registers
0: Not update configuration
1: Update configuration
Setting 1 to this bit, the value set in registers 0x60 to 0xDF are reflected to ICs operations.
It is also necessary that the software calibration is performed at updating configuration.

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFF	R/W	0x00	0	0	0	0	0	SET	CAL	ACT

I/O Equivalence Circuit

29. SDA, 30. SCL	23 to 27. GPIOn (n = 0 to 4)
	

28. INTB	22. TEST, 32. RSTB
	

4 to 21. CSm (m = 0 to 17)


Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

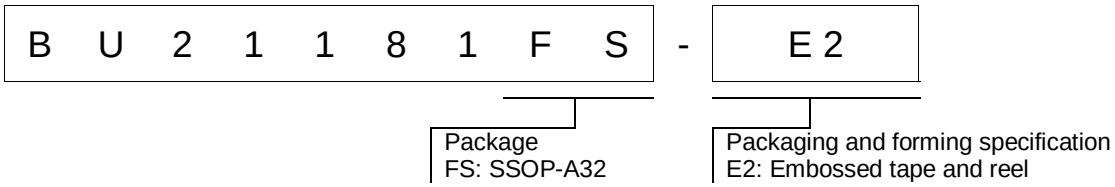
9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

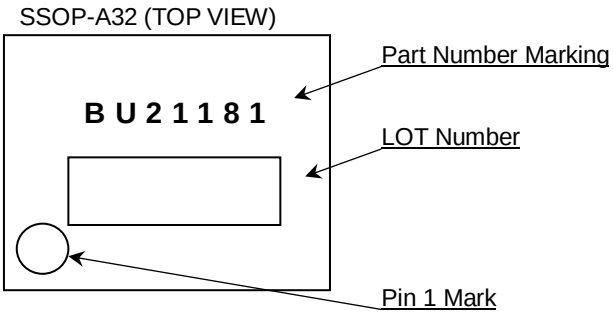
11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. **Over Current Protection Circuit (OCP)**
    This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

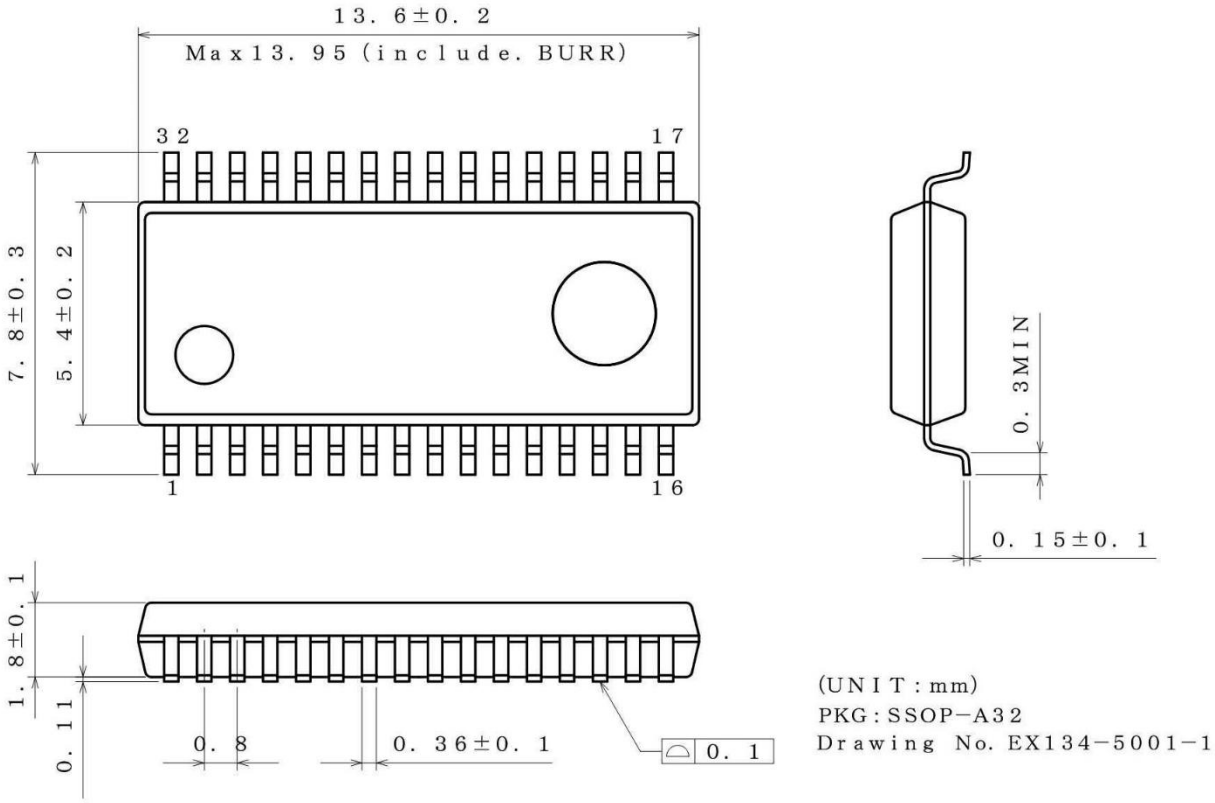


Marking Diagram



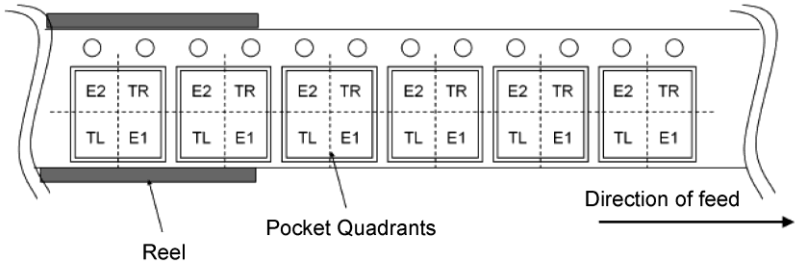
Physical Dimension and Packing Information

Package Name	SSOP-A32



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
18.Dec.2019	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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