

Ultra Low Quiescent Current LDO Regulator BD750L2EFJ / Load Response

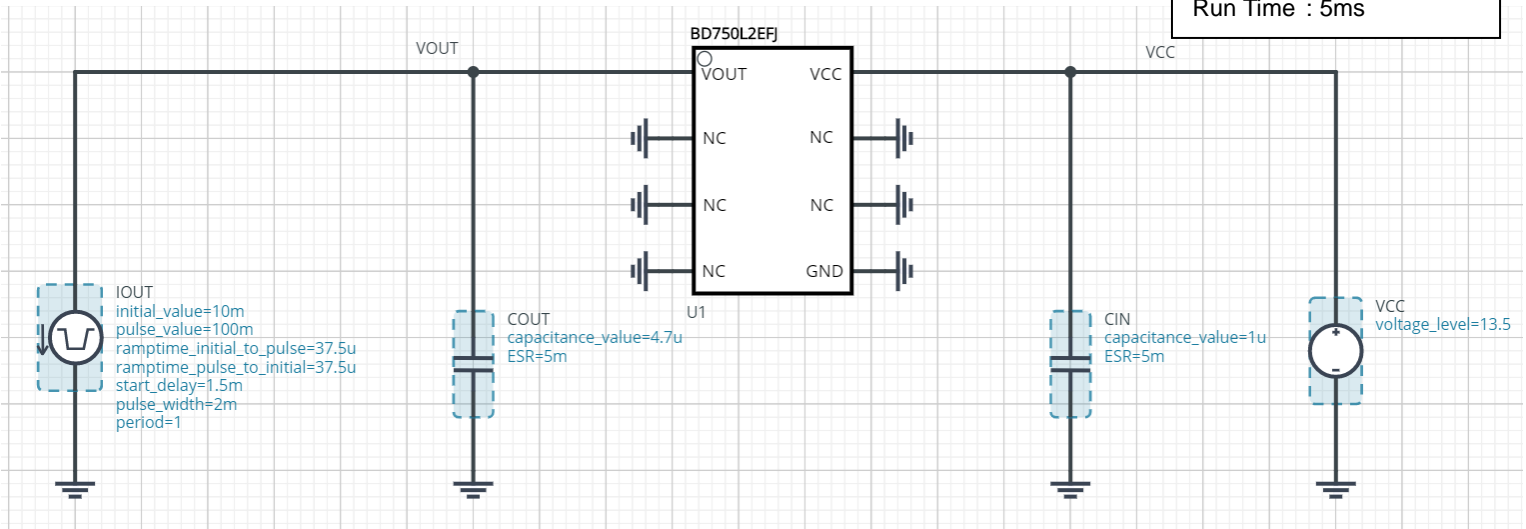
This Circuit simulates the Load Response.

You can check the fluctuation of the output voltage when the load current is abruptly changed.

Simulation Schematic

Simulation Setting

Type : Time Domain
Run Time : 5ms



Peripheral Components

Instance Name	Type	Parameter	Default Value	Variable Range		Unit
				Min	Max	
CIN	Capacitor	capacitance_value	1	0.1	no constraint ^(Note 1)	μF
		ESR	5	1	10000	mΩ
COUT	Capacitor	capacitance_value	4.7	4.7	no constraint ^(Note 1)	μF
		ESR	5	1	10000	mΩ

Simulation Conditions

Instance Name	Type	Parameter	Default Value	Variable Range		Unit
				Min	Max	
VCC	Voltage Source	voltage_level	13.5	5.8	45	V
IOUT	Current Source	initial_value	10	0	200	mA
		pulse_value	100	0	200	mA
		ramptime_initial_to_pulse	37.5	no constraint ^(Note 1)		μs
		ramptime_pulse_to_initial	37.5	no constraint ^(Note 1)		μs
		start_delay	1.5	no constraint ^(Note 1)		ms
		pulse_width	2	no constraint ^(Note 1)		ms
		period	1	no constraint ^(Note 1)		s

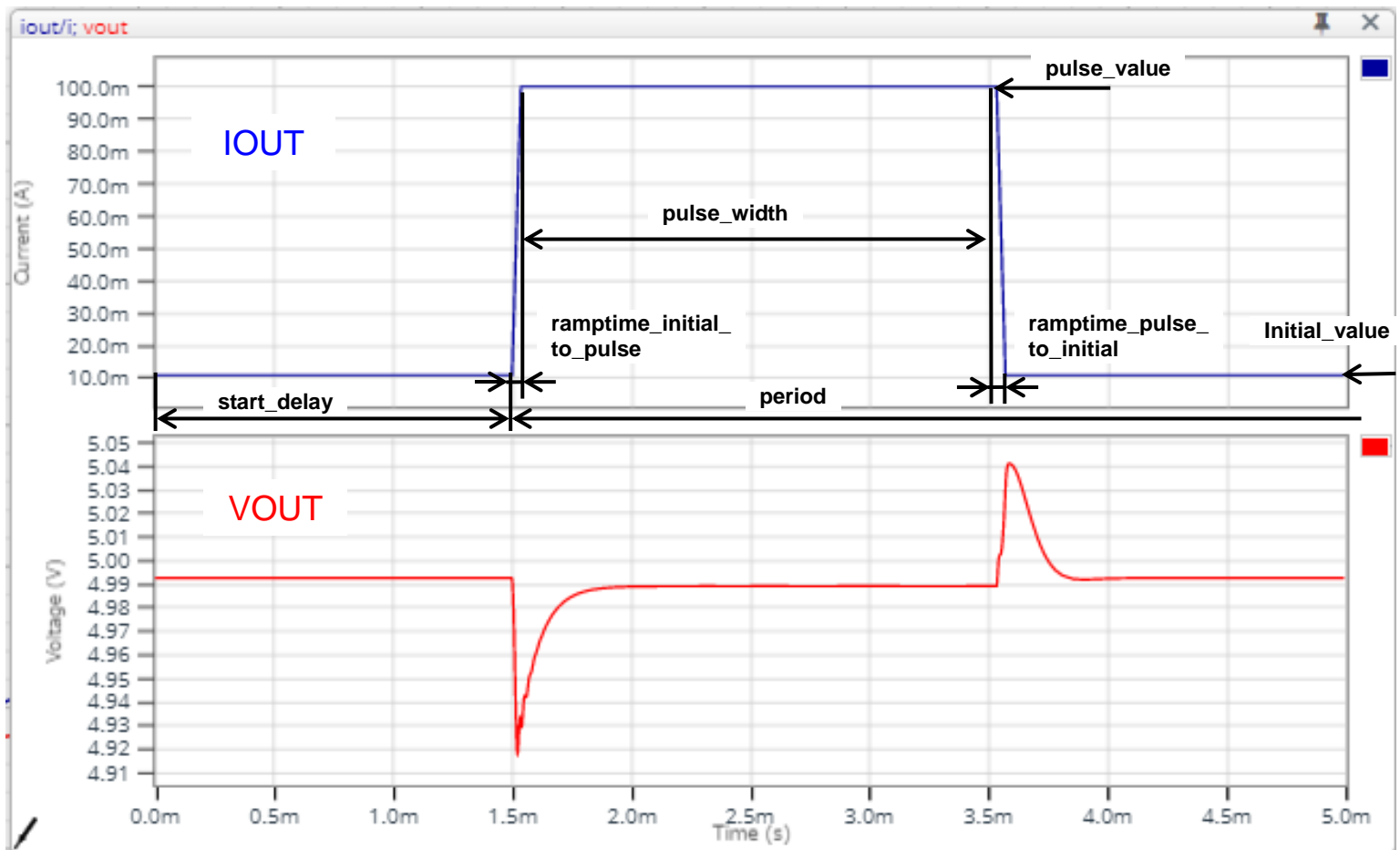
(Note 1) This is a constraint of the simulation settings and does not guarantee the operation of the IC.

Caution 1: The values from the simulation results are not guaranteed. Please use these results as a guide for your design.

Caution 2: These model characteristics are specifically at Ta=25°C. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).

Caution 3: Please refer to the datasheet for details of the technical information

Simulation Result



Notes

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