

1. Overview of the EVK

This manual outlines the procedures for operating the TO247 three-phase inverter evaluation board. Users are advised to read this document thoroughly before initiating any tests. The board is equipped with LEDs and terminals that facilitate status monitoring and evaluation. For detailed technical specifications, please refer to the user guide.

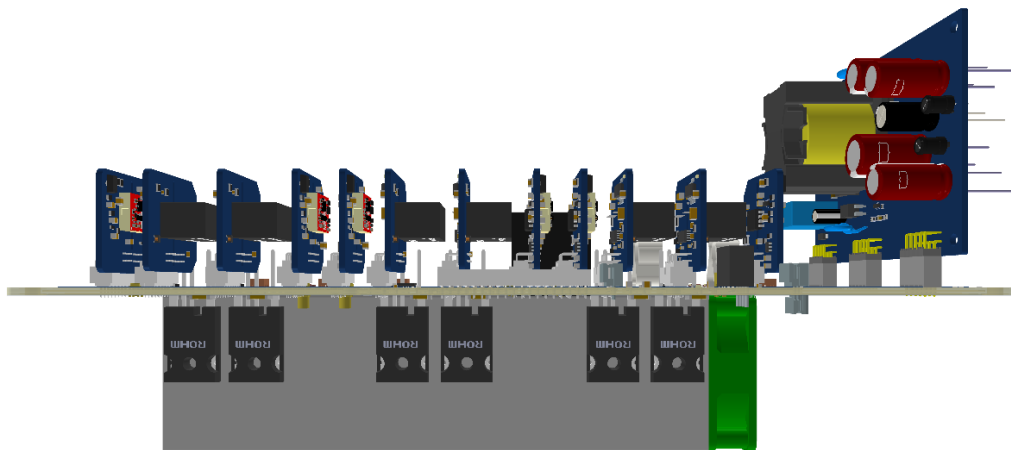


Figure 1. Power Board side view

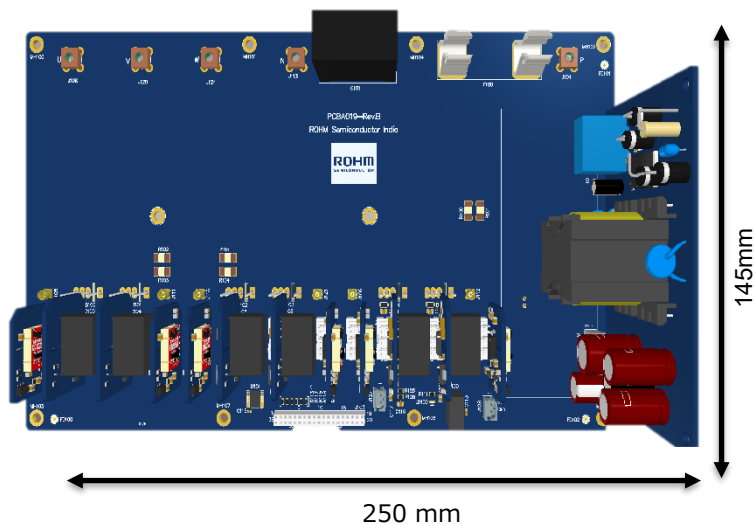


Figure 2. Power Board Top View

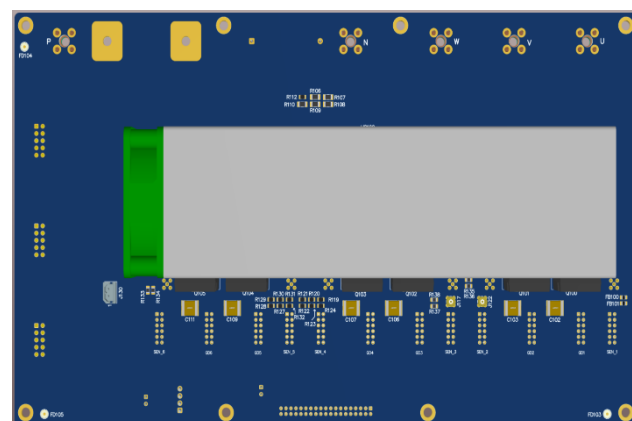


Figure 3. Power Board Bottom View

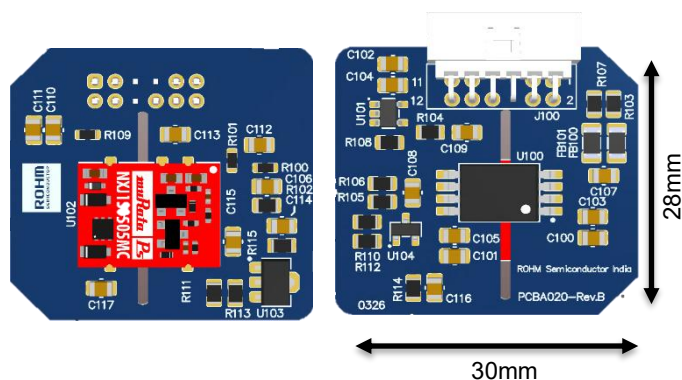


Figure 4. Sensing Board Top and Bottom view

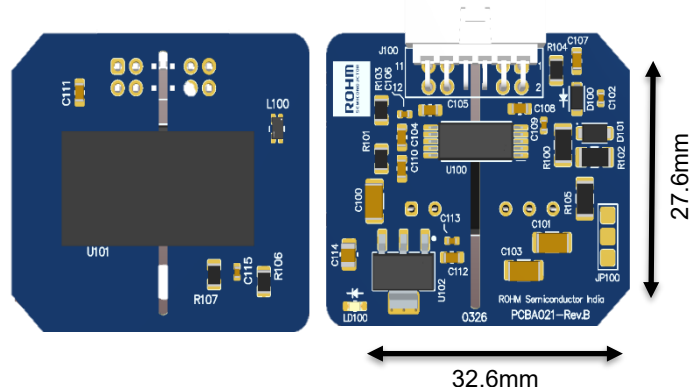


Figure 5. Gate Driver Board Top and Bottom view

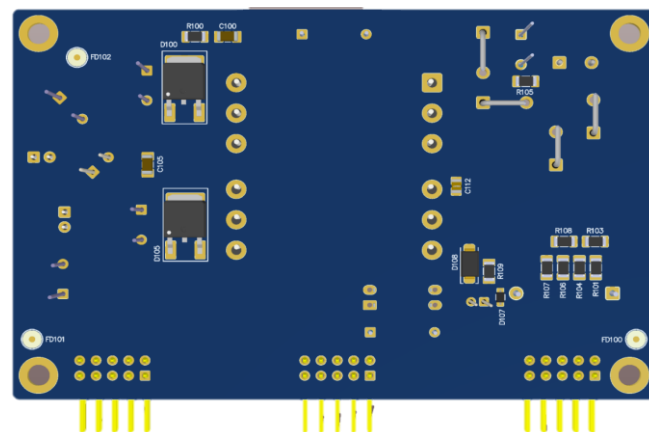


Figure 7. Aux Board Bottom View

2. Pin assignment

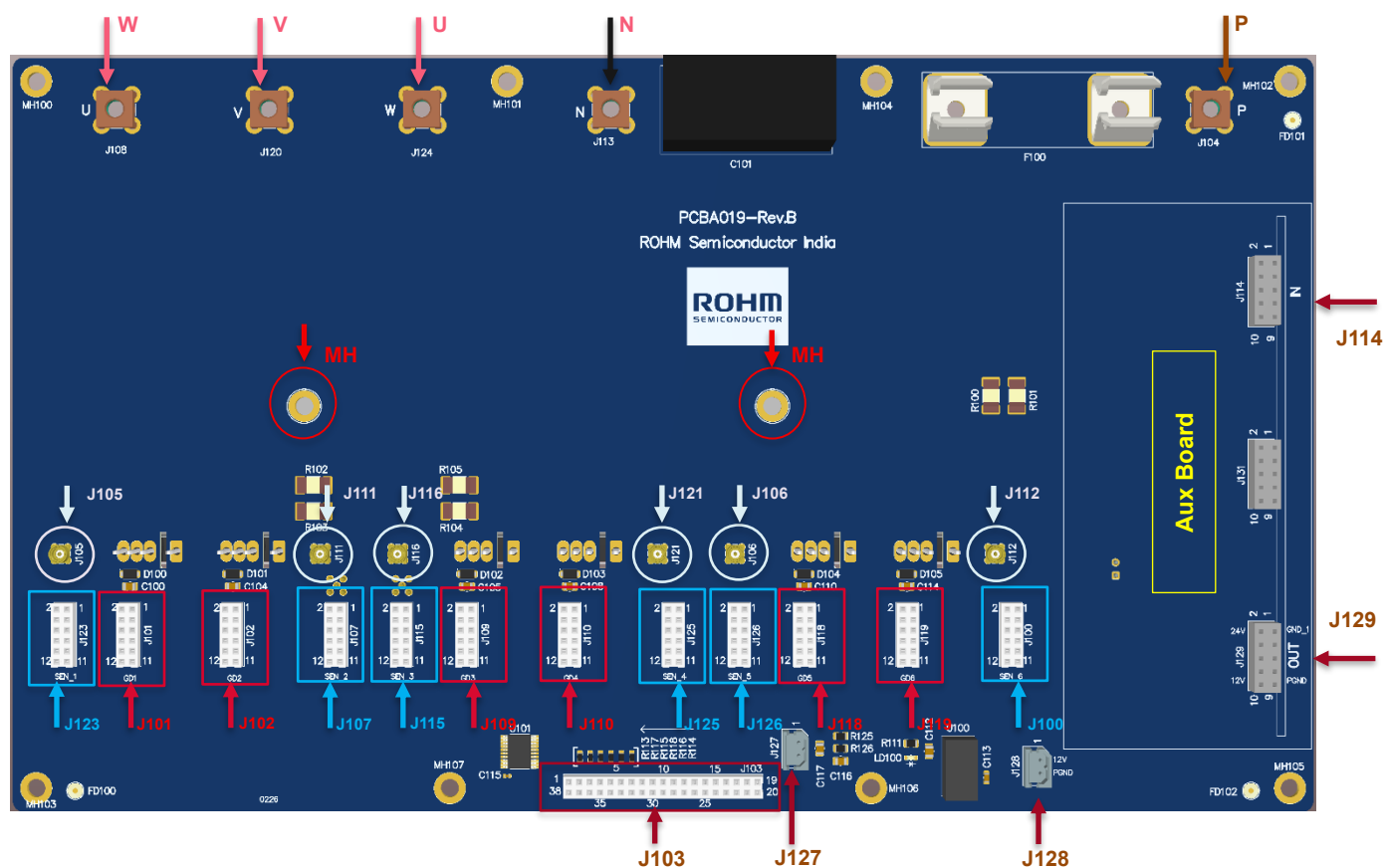


Figure 8. Pin connection diagram

Table 1. Board Connector List

Pin No	Pin name	Comment
Input Terminal		
1	P	Input DC
2	N	Neutral
Output Load Terminal		
3	U	U Phase Terminal
4	V	V Phase Terminal
5	W	W Phase Terminal
Gate Drive Connector List		
6	J101	U high Side gate
7	J102	U Low Side gate
8	J109	V high Side gate
9	J110	V Low Side gate
10	J118	W high Side gate
11	J119	W Low Side gate
Voltage Sense Board Connector List		
12	J123	Vdc Sensing
13	J125	VU Phase Voltage Sensing
14	J126	WV Phase Voltage Sensing
Current Sense Board Connector List		
15	J100	Idc Sensing
16	J107	U phase Current sensing
17	J115	V Phase Current sensing
PWM connector List		
18	J103	PWM Signals
Axillary Power supply connector		
19	J128	12V Connector
20	J130	24V Connector
Aux Power Board Connector		
21	J114	Input DC Connector
22	J129	24V and 12V Connector

2.1 Gate drive connector

Table 2. Gate drive connector Pin assignment

Pin No.	Pin Name	I/O	Details
1	SOURCE_U(Phase)_HS(LS)	O	Gate Source Pin for the MOSFET
2	GATE_U(Phase)_HS(LS)	O	Gate Drive Output which is connected to the MOSFET gate pin
3	N.C	-	-
4	N.C	-	-
5	N.C	-	-
6	N.C	-	-
7	N.C	-	-
8	N.C	-	-
9	Gate_U(Phase)_L	I	Low side logic signal Input to the gate driver from the buffer
10	Gate_U(Phase)_H	I	High side logic signal Input to the gate driver from the buffer
11	PGND	-	PGND
12	+12V	-	12V supply to the Gate driver Board

Table 3. Sense Board connector Pin assignment

Pin No.	Pin Name	I/O	Details
1	Idc_Sense+	I	Positive sense input
2	Idc_Sense-	I	Negative Sense Input
3	N.C	-	-
4	N.C	-	-
5	N.C	-	-
6	N.C	-	-
7	N.C	-	-
8	+12V	-	12V Supply to the Sense Board
9	PGND	-	PGND
10	+5V	-	5V supply to the amplifier in the sense Board
11	AGND	-	AGND
12	Idc_AD	O	Sense output from the amplifier

2.2 Control Signal Connector

Table 4. PWM connector Pin assignment

Pin No.	Pin Name	I/O	Details
1	AGND	-	AGND
2	PWM_U_HS	I	U Phase High side input signal to the gate driver
3	PWM_U_LS	I	U Phase Low side input signal to the gate driver
4	PWM_V_HS	I	V Phase High side input signal to the gate driver
5	PWM_V_LS	I	V Phase Low side input signal to the gate driver
6	PWM_W_HS	I	W Phase High side input signal to the gate driver
7	PWM_W_LS	I	W Phase Low side input signal to the gate driver
8	GB	-	-
9	N.C	-	-
10	N.C	-	-
11	N.C	-	-
12	Idc_AD	O	Input Line Current sense output signal
13	Iw_AD	O	W phase Current sense output signal
14	Iv_AD	O	V phase Current sense output signal
15	Vdc_AD	O	Input DC voltage sense Output
16	Vuv_AD	O	UV phase voltage sense Output
17	Vvw_AD	O	VW phase voltage sense Output
18	AGND	-	AGND
19	N.C	-	-
20	+5V	-	5V
21	AGND	-	AGND
22	NTC_AD	O	Temperature sensor output (Still not implemented)
23	AGND	-	AGND
24	AGND	-	AGND
25	AGND	-	AGND
26	AGND	-	AGND
27	AGND	-	AGND
28	AGND	-	AGND
29	AGND	-	AGND
30	AGND	-	AGND
31	AGND	-	AGND
32	AGND	-	AGND
33	AGND	-	AGND
34	AGND	-	AGND

35	AGND	-	AGND
36	AGND	-	AGND
37	AGND	-	AGND
38	AGND	-	AGND

**Note: PWM Signals are active low

2.3 Measurement (MMCX) connector

Table 5. Measurement connector list

1	J105	U Phase high side Vgs measurement
2	J106	W Phase high side Vgs measurement
3	J111	U Phase low side Vgs measurement
4	J112	W Phase low side Vgs measurement
5	J116	V Phase high side Vgs measurement
6	J117	V phase Current Sense measurement
7	J121	V Phase low side Vgs measurement
8	J122	U phase Current Sense measurement

3. Connection Diagram

The diagram below shows the connections for the gate driver, sensing circuits, load, and input power supply to the board.

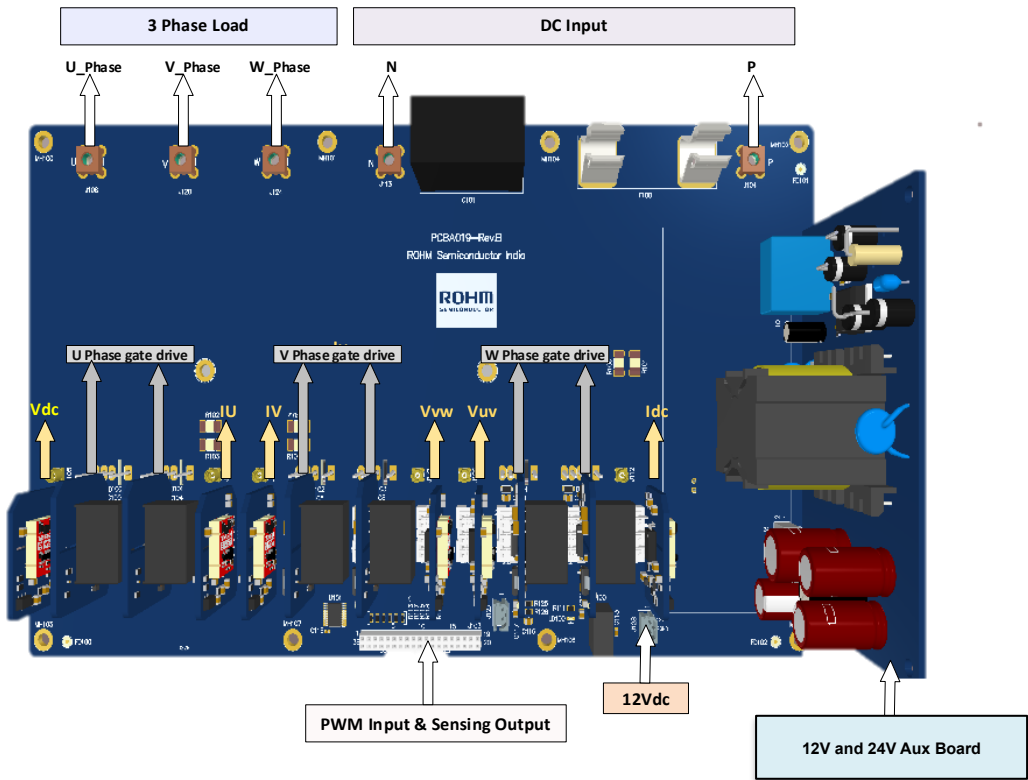


Figure 9. Connection Diagram

***Note: The Aux board generates 12V and 24V from the DC input. If external 12V and/or 24V is required, a dedicated connector is available to provide it externally.**

- Connect all gate driver boards to their respective positions on the main board using designated connectors.
- Attach voltage and current sensing boards to the appropriate input/output terminals as per the wiring diagram (Fig 6).
- Verify that the cooling fan is properly mounted and connected to the 24 V supply on the main board.

3.1 Pre-Power Checks

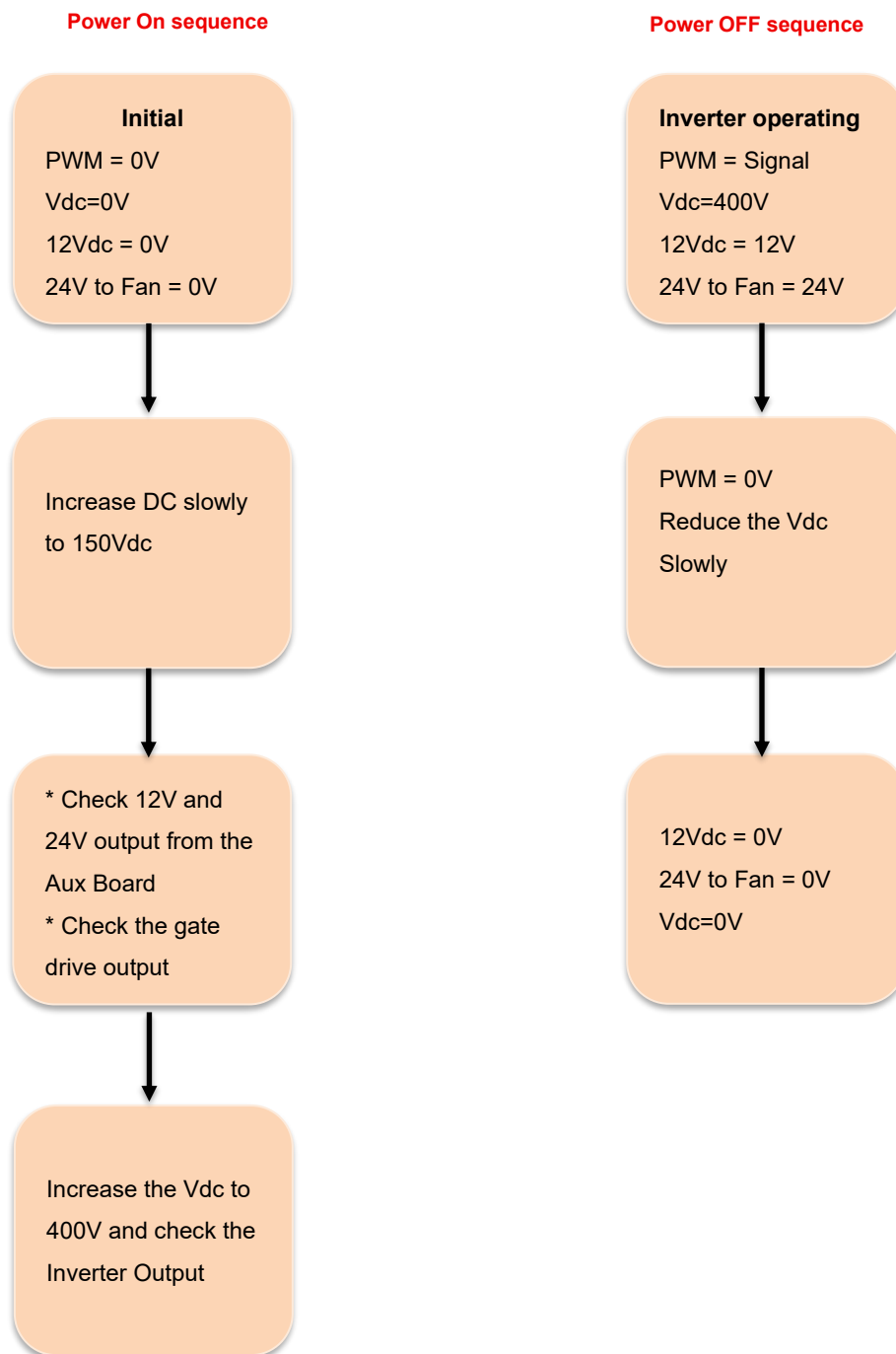
Before powering the system, perform the following checks:

- **Visual Inspection:** Ensure all components are securely mounted, connectors are properly seated, and no foreign objects are present.
- **Continuity Test:** Verify that there are no short circuits between power rails and ground.
- **Auxiliary Board:** Check the Aux Board Connection and check the 12V and 24V output.
- **Gate Driver Status:** Verify proper isolation and ensure gate driver connectivity with external PWM signals before powering the DC input.
- **Dead Time Validation:** Ensure appropriate dead time is configured between high-side and low-side gate pulses. Confirm timing aligns with the 120° phase shift requirement for three-phase operation.
- **Cooling System:** Ensure the fan is operational and airflow is unobstructed.
- **Signal Verification:** Confirm PWM signals are present and correctly mapped to gate driver inputs.

4. How to use the Board

4.1 Power ON/OFF sequence

Please follow the power ON/OFF sequence outlined below. Failure to do so may result in voltage overshooting, which can severely damage the power module.



4.2 LED Indication

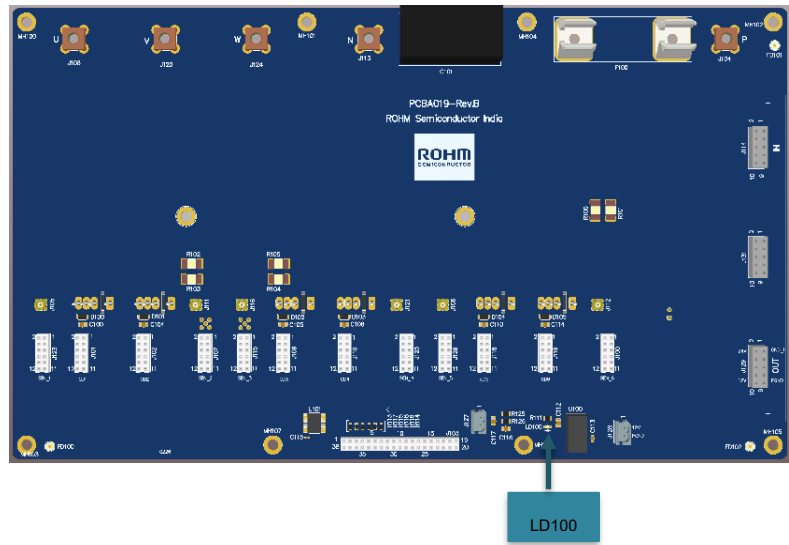


Figure 10. Main Board LED Indication

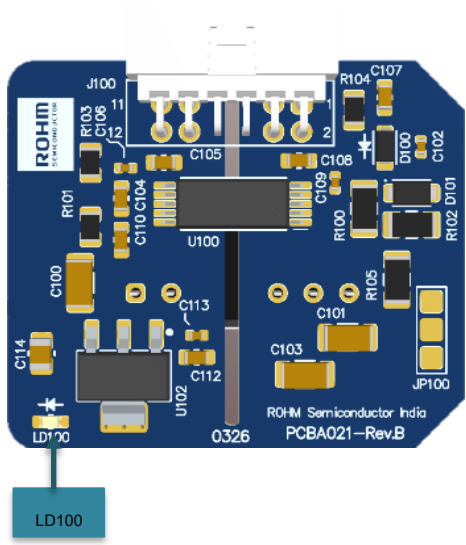


Figure 11. Gate Driver Board LED Indication

Table 6. LED Indication

Category	Side	Designator	Description
Auxiliary power	Main Board	LD100	Color: Green LED ON: +5V is normal OFF: +5V is abnormal
Auxiliary power	Gate Driver Board	LD100	Color: Green LED ON: +5V is normal OFF: +5V is abnormal

4.3 Functions of the EVK board

The TO247 SiC device evaluation board can be conveniently used for double-pulse testing and three-phase inverter evaluations. Please follow the assembly guide carefully when mounting the evaluation board

4.3.1 Fixed load (RL-load) test

For testing with RL load, users should be more careful of power ON sequence due to uncontrolled line currents. Users must prepare their own firmware and provide the controlling signals at the specific connectors. Test the board within specified limits mentioned in the user guide.

4.3.2 Motor bench test

For motor bench evaluation, users must prepare their own control software, as it is not included with the TO247 evaluation board. Additionally, a cable to connect the board to the control software is required. Please refer to table. 4 for socket pin and connector details and ensure you use the specified connector type.

4.4 Gate Resistor

The switching speed can be adjusted using gate resistors. While gate resistors which are there on the Board, users may replace them by soldering alternative values. However, safe operation of the power module with modified resistors cannot be guaranteed. Figure 10 shows the gate resistor in the schematic, Tables 7 and 8 list the available resistor values, and Figure 11 indicates the physical location on the board.

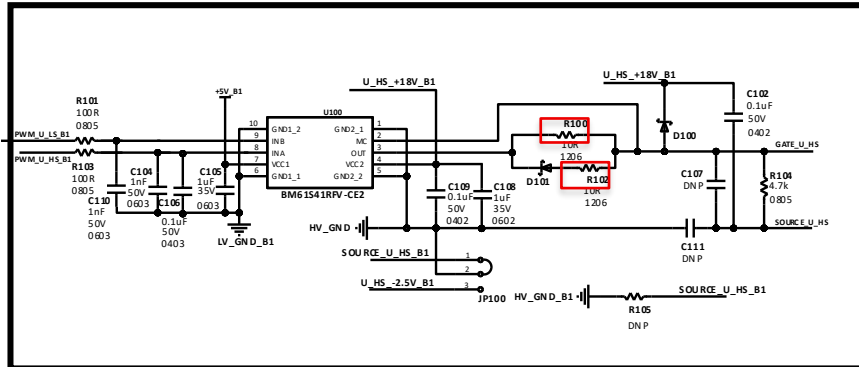


Figure 12. Gate resistor indication

Table 7. Gate turn On and Turn OFF resistors

	UH	UL	VH	VL	WH	WL
Turn on R	R100	R200	R300	R400	R500	R600
Turn off R	R100 R102	R200 R202	R300 R302	R400 R402	R500 R502	R600 R602

Note: The gate driver board is designed as a daughter card, and the same daughter boards are used for all phases.

Table 8. Existing Turn ON/OFF resistor on the Board

	Default gate resistor	
	Turn ON(Ω)	Turn OFF(Ω)
Package	(1206)	(1206)
Value	6.8R	6.8II6.8 R

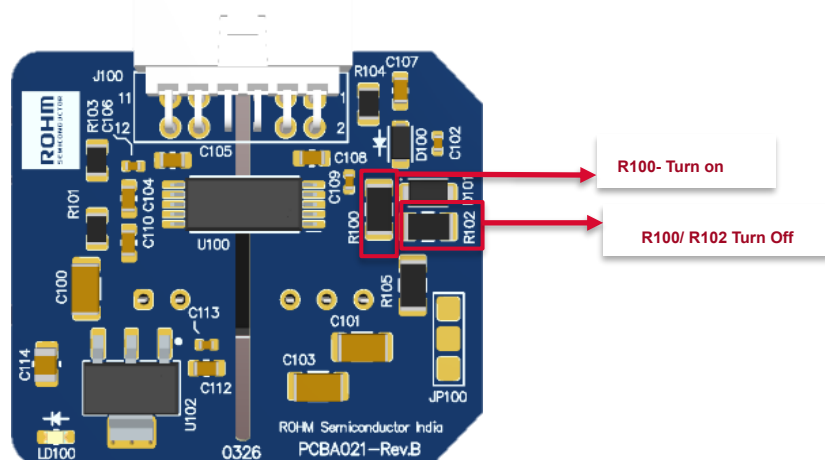


Figure 13. Gate resistor indication

5. Revision History

Table 9. Revision History

Revision	Date	Description of change
1	July 2026	Initial version

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